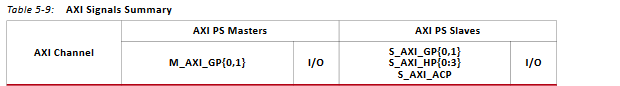
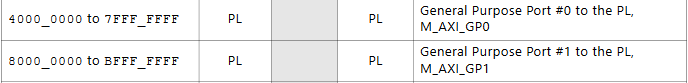
**AXI Non-Secure Enablement**

By setting AXI Non Secure Enablement to '0' I think it disables the security checking feature on AXI interconnect. If we enable it, the AXI interconnect will check the AxPROT[1] bit, namely non-secure bit, on the master/salve IP, and bypass or generate the bus error on the non-secure to secure transaction. For M\_AXI\_GP0\_AxPROT[1] bit, it indicates the GP0 is in secure (show '0') world or non-secure (show '1') world. I think the Xilinx TrustZone document says that there is no option to change value of this bit on Xilinx master IP or port.

**General Purpose (AXI\_GPx [x = 1 or 0])**

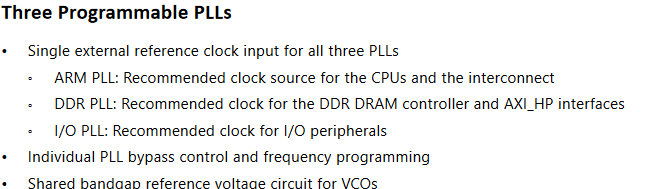


4.1 Address Map



**What is purpose of PL reset?**

**FCLK\_CLKX[x=0-3]**



**FCLK\_RESETX\_N [x = 0-3]**

Pick the one that is associated to the FCLK\_CLKX[x=0-3]

