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January 25, 2019

Lab 1

1. After which step, we finished building the hardware platform for the embedded system?

   Step 3 handles the hardware component of the project. It creates the ties needed for the software side of the project, which is why the following step is to launch the SDK.

2. Briefly describe the major components in the hardware platform.

   There is the IP, which is all the embedded/internal hardware components of the board, and there is the PL, programmable logic, side which handles the modules that can be instantiated through VHDL/Verilog. For this lab the hardware components used are UART1 and DDR Memory from the ZYNQ processor.

3. What is the top-level design file for hardware platform? Copy the contents in this file that support the answer you provide in the previous question.

   The top-level design file for the hardware platform system_wrapper (system_wrapper.vhd)

```
1.  system_i: component system
2.      port map (
3.       DDR_addr(14 downto 0) => DDR_addr(14 downto 0),
4.       DDR_ba(2 downto 0) => DDR_ba(2 downto 0),
5.       DDR_cas_n => DDR_cas_n,
6.       DDR_ck_n => DDR_ck_n,
7.       DDR_ck_p => DDR_ck_p,
8.       DDR_cke => DDR_cke,
9.       DDR_cs_n => DDR_cs_n,
10.      DDR_dm(3 downto 0) => DDR_dm(3 downto 0),
11.      DDR_dq(31 downto 0) => DDR_dq(31 downto 0),
12.      DDR_dqs_n(3 downto 0) => DDR_dqs_n(3 downto 0),
13.      DDR_dqs_p(3 downto 0) => DDR_dqs_p(3 downto 0),
14.      DDR_odt => DDR_odt,
15.      DDR_ras_n => DDR_ras_n,
16.      DDR_reset_n => DDR_reset_n,
17.      DDR_we_n => DDR_we_n,
18.      FIXED_IO_ddr_vrn => FIXED_IO_ddr_vrn,
19.      FIXED_IO_ddr_vrp => FIXED_IO_ddr_vrp,
20.      FIXED_IO_mio(53 downto 0) => FIXED_IO_mio(53 downto 0),
21.      FIXED_IO_ps_clk => FIXED_IO_ps_clk,
22.      FIXED_IO_ps_porb => FIXED_IO_ps_porb,
23.      FIXED_IO_ps_srstb => FIXED_IO_ps_srstb
24.     );
```

4. What does a bit stream file do? Is there a bit stream file generated for the hardware platform we built in this lab?

   An FPGA bitstream is a file that contains the programming information for an FPGA. A Xilinx FPGA device must be programmed using a specific bitstream in order for it to behave as an embedded hardware platform. This bitstream is typically provided by the hardware designer who creates the embedded platform. No bit stream was generated.

5. What is the step that transitions our design from hardware platform to software platform? What are the tools used for hardware design and software design respectively? What information are passed from hardware design tool to software design tool?

   The step that transitions the lab from hardware to software is step 4, where the user is indicated to launch the Xilinx SDK tool from the File menu. The files generated in Vivado are transferred and used to generate 1 project file in the Xilinx SDK.

6. How many projects are created for building the software platform? Briefly describe the key design information provide in each one of them and the role each one of them play in the software platform.

   When the Xilinx SDK tool is launched from a project in Vivado, the SDK generates 3 project files. The first file generated is the system wrapper, which contains the specifications and constraint implemented in vivado(.bit file). The folder contains a .hdf (Hardware Description File) which contains hardware configuration information. It determines the hardware peripherals in the system. And their addressing map location. The second folder is the mem_test file. It is a memory test using a project template from the SDK library. The third folder is the bsp folder, which provides the drivers for the software/hardware. The BSP (board support packages) provides the driver information. One of the key files in this folder, other than the main that will be used to mount/run on board is the file with the .mss extension.

7. What is BSP? What information does it provide and what role does it play in building the software platform?

   BSP is Board support packages. BSP is a layer of software that allows the OS or device to function with a specific hardware environment. In this case, the drivers allow the FGPA and other PL to communicate with the PS's in the system.

8. What is the top-level design file for software platform? Briefly describe the key information in this file and support your answer by copying the related contents of this file.

   The top level is the Mem_test folder. It contains all the C code and headers for embedded application. It contains all the executable files in order to build and run the program.

9. What is an .elf file? Is there an .elf file generated in this lab?

   An .elf file is a executable loadable file. The .elf file is generated by the software side, which is the Xilinx SDK. When the project is ran, the .elf file is transferred to the board. It contains an executable CPU code image(standalone or OS).

10. Please provide a screenshot of your embedded systems output