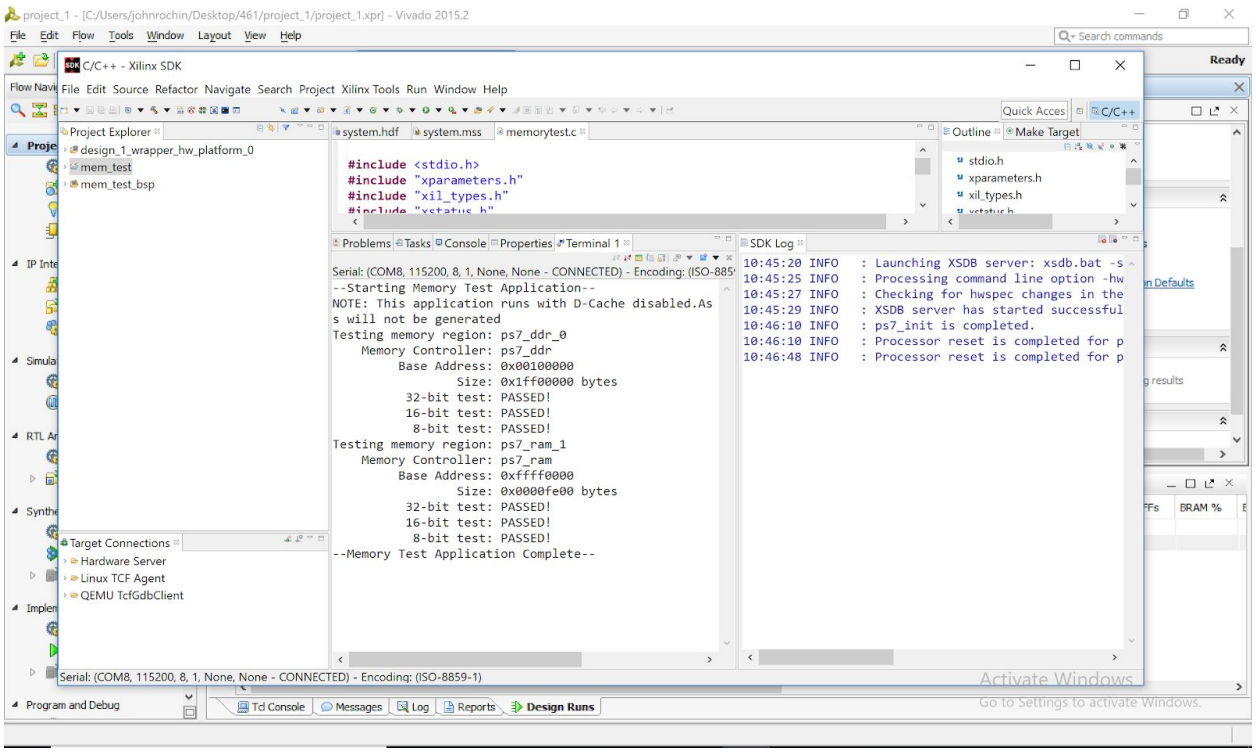
Lab 1 ScreenShot



Lab Questions:

1. Step 3 handles the hardware component of the project. It creates the ties needed for the software side of the project, which is why the following step is to launch the SDK.
2. There is the IP, which is all the embedded/internal hardware components of the the board, and there is the PL, programmable logic, side which handles the modules that can be instantiated through VHDL/Verilog. For this lab the hardware components used are UART1 and DDR Memory from the ZYNQ processor.
3. design1_WRAPPER(design1_wrapper.vhd)

```
design_1_i: component design_1
    port map (
     DDR_addr(14 downto 0) => DDR_addr(14 downto 0),
     DDR_ba(2 downto 0) => DDR_ba(2 downto 0),
     DDR_cas_n => DDR_cas_n,
     DDR_ck_n => DDR_ck_n,
     DDR_ck_p => DDR_ck_p,
     DDR_cke => DDR_cke,
     DDR_cs_n => DDR_cs_n,
```

```
  DDR_dm(3 downto 0) => DDR_dm(3 downto 0),
  DDR_dq(31 downto 0) => DDR_dq(31 downto 0),
  DDR_dqs_n(3 downto 0) => DDR_dqs_n(3 downto 0),
  DDR_dqs_p(3 downto 0) => DDR_dqs_p(3 downto 0),
  DDR_odt => DDR_odt,
  DDR_ras_n => DDR_ras_n,
  DDR_reset_n => DDR_reset_n,
  DDR_we_n => DDR_we_n,
  FIXED_IO_ddr_vrn => FIXED_IO_ddr_vrn,
  FIXED_IO_ddr_vrp => FIXED_IO_ddr_vrp,
  FIXED_IO_mio(53 downto 0) => FIXED_IO_mio(53 downto 0),
  FIXED_IO_ps_clk => FIXED_IO_ps_clk,
  FIXED_IO_ps_porb => FIXED_IO_ps_porb,
  FIXED_IO_ps_srstb => FIXED_IO_ps_srstb
);
```

4. There are two major file components when implementing the design. There is a hardware design aspect, where a .bit (bitstream) file is generated(vivado IP integrator. There is also a software side(Xilinx SDK), which generates the .elf (executable loadable file). The bitstream is a file that specifies the constraints and designs of the FPGA components.
5. The step that transitions the lab from hardware to software is step 4, where the user is indicated to launch the Xilinx SDK tool from the File menu. The files generated in Vivado are transferred and used to generate 1 project file in the Xilinx SDK.
6. When the Xilinx SDK tool is launched from a project in Vivado, the SDK generates 3 project files. The first file generated is the system wrapper, which contains the specifications and constraint implemented in vivado(.bit file). The folder contains a .hdf (Hardware Description File) which contains hardware configuration information. It determines the hardware peripherals in the system. And their addressing map location. The second folder is the mem_test file. It is a memory test using a project template from the SDK library. The third folder is the bsp folder, which provides the drivers for the software/hardware. The BSP (board support packages) provides the driver information. One of the key files in this folder, other than the main that will be used to mount/run on board is the file with the .mss extension.
7. BSP is Board support packages. BSP is a layer of software that allows the OS or device to function with a specific hardware environment. In this case, the drivers allow the FGPA and other PL to communicate with the PS's in the system.
8. The top level is the Mem_test folder. It contains all the C code and headers for embedded application. It contains all the executable files in order to build and run the program.
9. An .elf file is a executable loadable file. The .elf file is generated by the software side, which is the Xilinx SDK. When the project is ran, the .elf file is transferred to the board. It contains an executable CPU code image(standalone or OS).

10. See above.