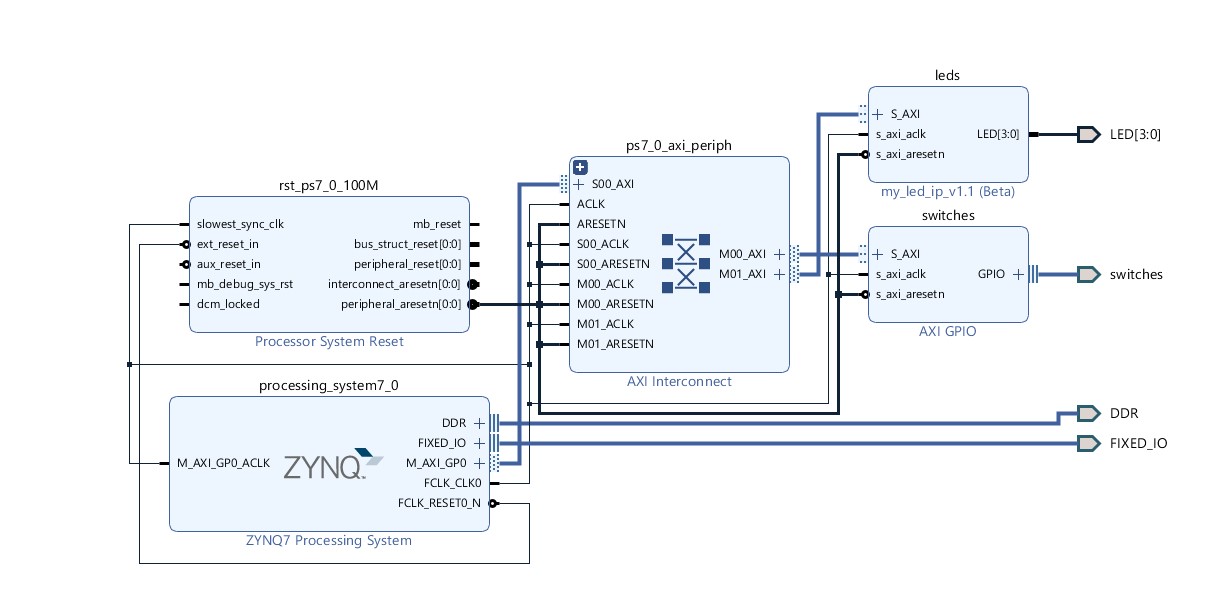
Hardware/Software Codesign Midterm 2 Lab Test – Lauro Cabral

1. Software source code: midterm2.c
2. Hardware source code: user\_gpio\_ip \_user\_logic.v. For extra challenge: include all three HDL files for your custom IP.
3. Block diagram (screenshot is ok)



1. Answer the following questions:
2. Specify the location(s) for the DDR3 Controller and DDR3 memory: inside [Xilinx Zynq-7000 (XC7Z010-1CLG400C)](http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/silicon-devices.html) or outside? If inside, specify if it is a hard core or soft cores and where does it locate in XC7Z010-1CLG400C: in PS or PL.

**DDR3 Controller inside Zynq PS, hard core.**

**DDR3 Memory outside Zynq**

1. Specify the location(s) for the user\_gpio \_ip instance: inside [Xilinx Zynq-7000 (XC7Z010-1CLG400C)](http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/silicon-devices.html) or outside? If inside, specify if it is a hard core or soft cores and where does it locate in XC7Z010-1CLG400C: in PS or PL.

**Both inside Zynq PL, soft core**

1. List all the external peripherals in the embedded system you build in this project.

**LED’s , dip switches**