```
1 || -
  -- This component synchronizes input signals produced from outside the
3 -- board with the clock signal on the board. This is done to avoid
  -- metastability. Also this component makes sure that these signals will
  -- only be asserted for one clock cycle each, even if the input signals
5
  -- are asserted from outside the board for several clock cycles.
7
8
  library ieee;
9
  use ieee.std logic 1164.all;
10
11
  entity input synchronizer is
12
      port(clock
                      : in std logic;
13
            buy btn
                      : in std logic;
14
            buy_out : out std_logic;
15
            coin1_btn : in std_logic;
16
            coin1 out : out std logic;
17
            coin2_btn : in std_logic;
18
            coin2 out : out std logic;
19
            coin5 btn : in std logic;
20
            coin5_out : out std_logic;
21
            cola sw : in std logic;
22
            cola_out : out std_logic;
23
            hash_sw : in std_logic;
24
            hash out : out std logic;
25
            aqua_sw : in std_logic;
26
                      : out std_logic;
27
            aqua_out
                            std logic);
           Reset
                      : in
28
  end input synchronizer;
29
30
  architecture Structure of input synchronizer is
31
      signal buy_btn_synk, buy_btn_synk_new
32
                                                  : std_logic;
      signal coin1 btn synk, coin1 btn synk new : std logic;
33
      signal coin2_btn_synk, coin2_btn_synk_new : std_logic;
34
      signal coin5_btn_synk, coin5_btn_synk_new : std_logic;
35
      signal cola sw synk, cola sw synk new
                                                  : std logic:
36
      signal hash_sw_synk, hash_sw_synk_new
                                                 : std logic;
37
      signal aqua sw synk, aqua sw synk new
                                                  : std logic;
38
39
  begin
40
41
42
      -- the seven processes below asserts the signal out only when
43
      -- the synkd version of the input signal is '1' and the synk new
44
      -- version of the input signal is '0'. This makes signal_out
45
      -- last for exactly one clock cycle.
46
47
48
```

```
49
       -- buy button
       process(buy btn synk)
50
       begin
51
            buy_out <= '0';</pre>
52
            if buy_btn_synk = '1' AND buy_btn_synk_new = '0' then
53
                buy_out <= '1';
54
            end if;
55
       end process;
56
57
       -- coin1 button
58
59
       process(coin1_btn_synk)
       begin
60
            coin1_out <= '0';
61
            if coin1_btn_synk = '1' AND coin1_btn_synk_new = '0' then
62
                coin1 out <= '1';</pre>
63
            end if;
64
       end process:
65
66
       -- coin2 button
67
       process(coin2 btn synk)
68
       begin
69
            coin2_out <= '0';</pre>
70
            if (coin2_btn_synk = '1' AND coin2_btn_synk_new = '0') then
71
                coin2 out <= '1';
72
            end if;
73
       end process;
74
75
       -- coin5 button
76
77
       process(coin5 btn synk)
       begin
78
            coin5 out <= '0';</pre>
79
            if coin5_btn_synk = '1' AND coin5_btn_synk_new = '0' then
80
                coin5 out <= '1';</pre>
81
            end if;
82
       end process;
83
84
       -- cola switch
85
       process(cola sw synk)
86
       begin
87
            cola_out <= '0';</pre>
88
            if cola_sw_synk = '1' AND cola_sw_synk_new = '0' then
89
                cola out <= '1';
90
            end if;
91
       end process;
92
93
       -- hash switch
94
       process(hash sw synk)
95
96
       begin
```

```
hash_out <= '0';
97
            if hash_sw_synk = '1' AND hash_sw_synk_new = '0' then
98
                 hash out <= '1';
99
            end if:
100
        end process;
101
102
        -- aqua switch
103
        process(aqua_sw_synk)
104
        begin
105
            aqua out <= '0';
106
            if aqua_sw_synk = '1' AND aqua_sw_synk_new = '0' then
107
                 agua out <= '1';
108
            end if;
109
        end process;
110
111
112
        -- This process keeps updating registers
113
        -- on every rising clock edge
114
115
        process(clock)
116
        begin
117
            if rising edge(clock) then
118
                 -- buy button
119
                 buy_btn_synk <= buy_btn;</pre>
120
                 buy_btn_synk_new <= buy_btn_synk;</pre>
121
122
                 -- coin1 button
123
                 coin1 btn synk <= coin1 btn;</pre>
124
125
                 coin1_btn_synk_new <= coin1_btn_synk;</pre>
126
                 -- coin2 button
127
128
                 coin2_btn_synk <= coin2_btn;</pre>
                 coin2 btn synk new <= coin2 btn synk;</pre>
129
130
                 -- coin5 button
131
                 coin5 btn synk <= coin5 btn;</pre>
132
                 coin5_btn_synk_new <= coin5_btn_synk;</pre>
133
134
                 -- cola switch
135
136
                 cola_sw_synk <= cola_sw;</pre>
                 cola sw synk new <= cola sw synk;
137
138
                 -- hash switch
139
                 hash sw synk
                                    <= hash sw;
140
                 hash_sw_synk_new <= hash_sw_synk;
141
142
                 -- aqua switch
143
144
                 aqua_sw_synk <= aqua_sw;
```

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```
aqua_sw_synk_new <= aqua_sw_synk;
end if;
end process;
end Structure;</pre>
```