```vhdl
145                         anTemp <= NOT "0001";
146                         d      <= "10000";
147                 when "01" =>
148                         anTemp <= NOT "0010";
149                         d      <= "10001";
150                 when "10" =>
151                         anTemp <= NOT "0100";
152                         d      <= "01010";
153                 when "11" =>
154                         anTemp <= NOT "1000";
155                         d      <= "10000";
156                 when others =>
157                         anTemp <= NOT "0000";
158                         d      <= "00000";
159             end case;
160         else
161             case m is
162                 when "00" =>
163                         anTemp <= NOT "0001";
164                         d      <= sumL;
165                 when "01" =>
166                         anTemp <= NOT "0010";
167                         d      <= sumH;
168                 when "10" =>
169                         anTemp <= NOT "0100";
170                         d      <= priceL;
171                 when "11" =>
172                         anTemp <= NOT "1000";
173                         d      <= priceH;
174                 when others =>
175                         anTemp <= NOT "0000";
176                         d      <= "00000";
177             end case;
178         end if;
179     end process;
180
181     ----------------------------------------------------------------
182     -- if the alarm signal is asserted, the whole display will blink on th
183     -- 3Hz clock. This process runs parallel with the above process, meani
184     -- that e.g. the alarm signal can be asserted while 'cola' is displaye
185     ----------------------------------------------------------------
186     process(alarm, clk_3)
187     begin
188         an <= anTemp;
189         if (alarm = '1' AND clk_3 = '0') then
190             an <= NOT "0000";
191         end if;
192     end process;
```