```
component display driver is
49
50
           port(price : in
                              unsigned(5 downto 0);
                 sum
                       : in
                              unsigned(5 downto 0);
51
                       : out std logic vector(3 downto 0);
52
                 an
                             std logic;
                 reset : in
53
                 clock : in
                              std_logic;
54
                 clk 3 : in
                              std_logic;
55
                             std_logic;
                 alarm : in
56
                 cola
                       : in
                             std logic;
57
                             std logic;
                 hash
                       : in
58
                             std logic;
59
                 aqua
                       : in
                       : out std logic vector(1 to 8));
                 led
60
       end component;
61
62
       component input_synchronizer is
63
                                  std logic;
           port(clock
                           : in
64
                 buy btn
                           : in
                                  std logic;
65
                           : out std logic;
                 buy_out
66
                 coin1 btn : in
                                  std logic;
67
                 coin1 out : out std logic;
68
                 coin2 btn : in
                                  std logic;
69
                 coin2 out : out std logic;
70
                 coin5 btn : in std logic;
71
                 coin5_out : out std_logic;
72
                 cola sw
                           : in
                                  std logic;
73
                           : out std_logic;
                 cola_out
74
75
                 hash_sw
                           : in
                                  std_logic;
                           : out std logic;
                 hash out
76
                                  std_logic;
                           : in
77
                 aqua sw
                           : out std logic;
                 aqua out
78
                                  std logic);
                 Reset
                            : in
79
80
       end component;
81
82
       component processing_unit is
83
           port(clock
                            : in
                                   std logic;
84
85
                 buy
                             : in
                                   std logic;
                                   std logic;
                 coin1
                            : in
86
                                   std logic;
                 coin2
                             : in
87
                 coin5
                            : in
                                   std_logic;
88
                                   std logic;
89
                 price cola : in
                                   std_logic;
                 price_hash : in
90
91
                 price aqua : in
                                   std logic;
                Reset
                            : in
                                   std logic;
92
                            : out unsigned(5 downto 0);
93
                 sum out
                 price out : out unsigned(5 downto 0);
94
                 alarm out : out std logic;
95
                            : out std logic;
96
                 cola out
```