```
1 || -----
  -- Top component of the vending machine for the course:
3 -- 02139 Digital electronics 2 at the Technical University of Denmark
4 || ---
  -- This component declares and instantiates all the components of the
5
  -- vending machine.
7
8
  library ieee;
9
  use ieee.std_logic_1164.all;
10
  use ieee.numeric_std.all;
11
12
  entity vending_machine is
13
       port(clk 50 : in std logic;
14
            clk_man : in std_logic;
sel_man : in std_logic;
15
16
            reset : in std logic;
17
            coin1_btn : in std_logic;
18
            coin2_btn : in std_logic;
19
            coin5_btn : in std_logic;
20
            buy_btn : in std_logic;
cola_sw : in std_logic;
21
22
            hash_sw : in std_logic;
aqua_sw : in std_logic;
23
24
            an : out std logic vector(3 downto 0);
25
            led : out std_logic_vector(1 to 8));
26
27
  end vending_machine;
28
  architecture struct of vending_machine is
29
       signal clk
                                                    : std logic;
30
       signal clk 3
                                                    : std logic;
31
       signal buy
                                                   : std_logic;
32
       signal coin1, coin2, coin5
                                                    : std logic;
33
       signal price_cola, price_hash, price_aqua : std_logic;
34
       signal alarm, cola, aqua, hash : std_logic;
35
                                                    : unsigned(5 downto 0);
       signal sum, price
36
37
38
       -- Component declarations
39
40
41
       component clock manager is
           port(clk_50 : in std_logic;
42
43
                clk man : in std logic;
                sel man : in std logic;
44
                clk : out std_logic;
45
                clk 3 : out std logic);
46
       end component;
47
48
```

```
component display driver is
49
50
           port(price : in
                              unsigned(5 downto 0);
                 sum
                       : in
                              unsigned(5 downto 0);
51
                       : out std logic vector(3 downto 0);
52
                 an
                             std logic;
                 reset : in
53
                 clock : in
                              std_logic;
54
                 clk 3 : in
                              std_logic;
55
                             std_logic;
                 alarm : in
56
                 cola
                       : in
                             std logic;
57
                             std logic;
                 hash
                       : in
58
                             std logic;
59
                 aqua
                       : in
                       : out std logic vector(1 to 8));
                 led
60
       end component;
61
62
       component input_synchronizer is
63
                                  std logic;
           port(clock
                           : in
64
                 buy btn
                           : in
                                  std logic;
65
                           : out std logic;
                 buy_out
66
                 coin1 btn : in
                                  std logic;
67
                 coin1 out : out std logic;
68
                 coin2 btn : in
                                  std logic;
69
                 coin2 out : out std logic;
70
                 coin5 btn : in std logic;
71
                 coin5_out : out std_logic;
72
                 cola sw
                           : in
                                  std logic;
73
                           : out std_logic;
                 cola_out
74
75
                 hash_sw
                           : in
                                  std_logic;
                           : out std logic;
                 hash out
76
                                  std_logic;
                           : in
77
                 aqua sw
                           : out std logic;
                 aqua out
78
                                  std logic);
                 Reset
                            : in
79
80
       end component;
81
82
       component processing_unit is
83
           port(clock
                            : in
                                   std logic;
84
85
                 buy
                             : in
                                   std logic;
                                   std logic;
                 coin1
                            : in
86
                                   std logic;
                 coin2
                             : in
87
                 coin5
                            : in
                                   std_logic;
88
                                   std logic;
89
                 price cola : in
                                   std_logic;
                 price_hash : in
90
91
                 price aqua : in
                                   std logic;
                Reset
                            : in
                                   std logic;
92
                            : out unsigned(5 downto 0);
93
                 sum out
                 price out : out unsigned(5 downto 0);
94
                 alarm out : out std logic;
95
                            : out std logic;
96
                 cola out
```

```
97
                  hash_out
                              : out std logic;
                  aqua_out : out std_logic);
98
        end component;
99
100
101
   -- signal assignments
102
103
104
   begin
105
        clock_manager1 : clock_manager
106
            port map(clk_50 => clk_50,
107
                      clk man => clk man,
108
                      sel man => sel man,
109
                      clk
                               => clk,
110
                               => clk 3);
                      clk 3
111
112
        display_driver1 : display_driver
113
            port map(sum
                             => sum,
114
115
                      price => price,
116
                      an
                             => an,
                       reset => reset,
117
                      clock => clk,
118
                      clk 3 \Rightarrow clk 3,
119
                      alarm => alarm,
120
                      cola => cola,
121
122
                      hash => hash,
                      aqua
                            => aqua,
123
                             => led);
124
                      led
125
        input synchronizer1 : input synchronizer
126
            port map(clock
127
                                => clk,
128
                      buy_btn
                                 => buy_btn,
                      buy out
                                 => buy,
129
                      coin1_btn => coin1_btn,
130
131
                      coin1_out => coin1,
                      coin2 btn => coin2 btn,
132
                      coin2_out => coin2,
133
                      coin5 btn => coin5 btn,
134
                      coin5 out => coin5,
135
                      cola_sw
                               => cola_sw,
136
                      cola out => price cola,
137
                      hash_sw
                                 => hash_sw,
138
                      hash out => price hash,
139
                      aqua_sw
                                 => aqua_sw,
140
                      aqua_out
                                 => price aqua,
141
                                 => reset);
                      Reset
142
143
144
        processing_unit1 : processing_unit
```

```
145
            port map(clock
                                  => clk,
146
                      buy
                                  => buy,
147
                      coin1
                                  => coin1,
148
                      coin2
                                  => coin2,
                      coin5
                                  => coin5,
149
150
                      price_cola => price_cola,
151
                      price_hash => price_hash,
                      price_aqua => price_aqua,
152
153
                      Reset
                                  => reset,
                      sum_out
154
                                  => sum,
155
                      price_out => price,
                      alarm out => alarm,
156
                      cola_out
                                  => cola,
157
158
                      hash out
                                  => hash,
                                  => aqua);
159
                      aqua_out
160
   end struct;
161
162
```