```
97              hash_out   : out std_logic;
98              aqua_out   : out std_logic);
99      end component;
100
101 ---------------------
102 -- signal assignments
103 ---------------------
104
105 begin
106     clock_manager1 : clock_manager
107         port map(clk_50  => clk_50,
108                  clk_man => clk_man,
109                  sel_man => sel_man,
110                  clk     => clk,
111                  clk_3   => clk_3);
112
113     display_driver1 : display_driver
114         port map(sum   => sum,
115                  price => price,
116                  an    => an,
117                  reset => reset,
118                  clock => clk,
119                  clk_3 => clk_3,
120                  alarm => alarm,
121                  cola  => cola,
122                  hash  => hash,
123                  aqua  => aqua,
124                  led   => led);
125
126     input_synchronizer1 : input_synchronizer
127         port map(clock     => clk,
128                  buy_btn   => buy_btn,
129                  buy_out   => buy,
130                  coin1_btn => coin1_btn,
131                  coin1_out => coin1,
132                  coin2_btn => coin2_btn,
133                  coin2_out => coin2,
134                  coin5_btn => coin5_btn,
135                  coin5_out => coin5,
136                  cola_sw   => cola_sw,
137                  cola_out  => price_cola,
138                  hash_sw   => hash_sw,
139                  hash_out  => price_hash,
140                  aqua_sw   => aqua_sw,
141                  aqua_out  => price_aqua,
142                  Reset     => reset);
143
144     processing_unit1 : processing_unit
```