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High-end Microelectronics Design

Citiroc 1b feasibility study

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Version document record

Issue	Date	Total pages	Modified pages	Notes
1(a)	9/11/2017	17	-	Initial version

List of acronyms

Acronym	Full meaning
NSB	Night Sky Background
DAC	Digital to Analogue Converter
GBWP	Gain BandWidth Product

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1 References

1.1 Applicable documents

The following documents are applicable to this report.

Ref	Document name	Reference
AD-1		
AD-2		
AD-3		

Table 1 - Applicable document

1.2 Reference documents

The following documents are referenced to this report.

Ref	Document name	Reference
RD-1		
RD-2		
RD-3		

Table 2 - Reference document

2 Introduction

The aim of that document is to study the feasibility of a respin of Citiroc 1A in an improved Citiroc1B version (minor changes, pin-to pin compatible) to improve a few side effects detected by the ASTRI collaboration.
There are two effects to correct in the 1B version of the chip:

- The ASIC baseline is changing when NSB is too high, ie background count rate is getting larger than TBD.
- The ASIC is inducing fake OCT because of pile up of dark count rate in the trigger line giving effect that two photons looks like a two-photon dark count event.

3 Citiroc 1A simulation

The current version of Citiroc has been simulated to identify the causes of the side effect in the ASIC.

3.1 Input DAC leakage current sensitivity

That simulation shows how the input DAC behaves when leakage current increases. Simulation has been performed for lower and highest DAC value to take into account any bias corner in the DAC transistors.

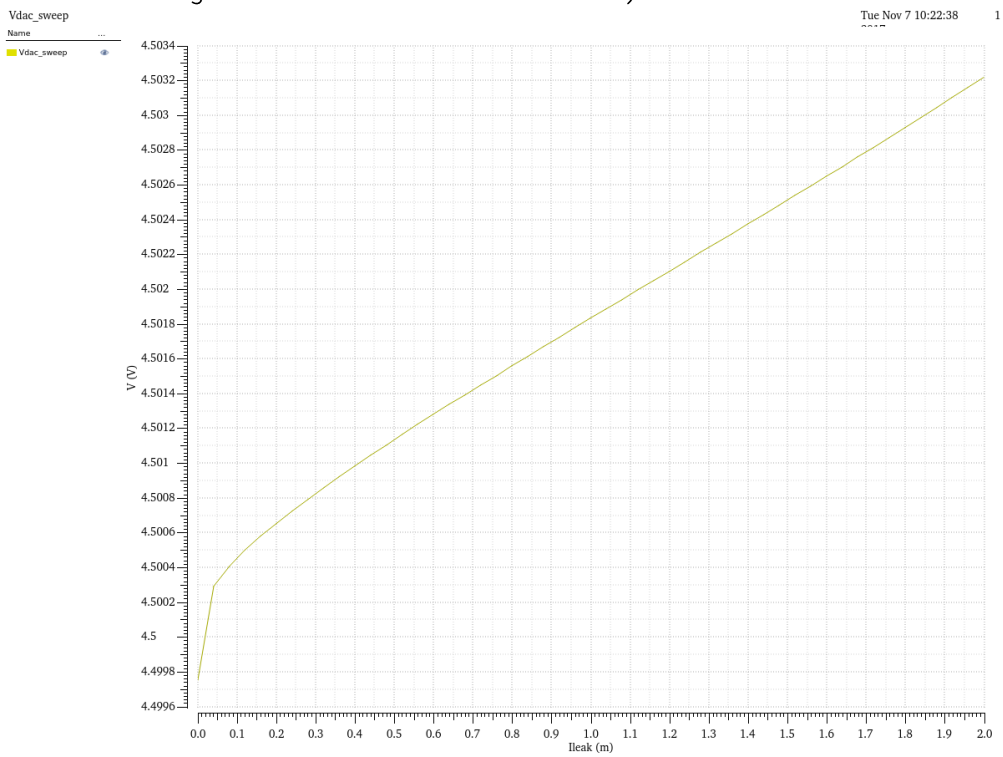

Figure 1 - Vdac versus leakage current - from 0 to 2mA - Highest DAC voltage

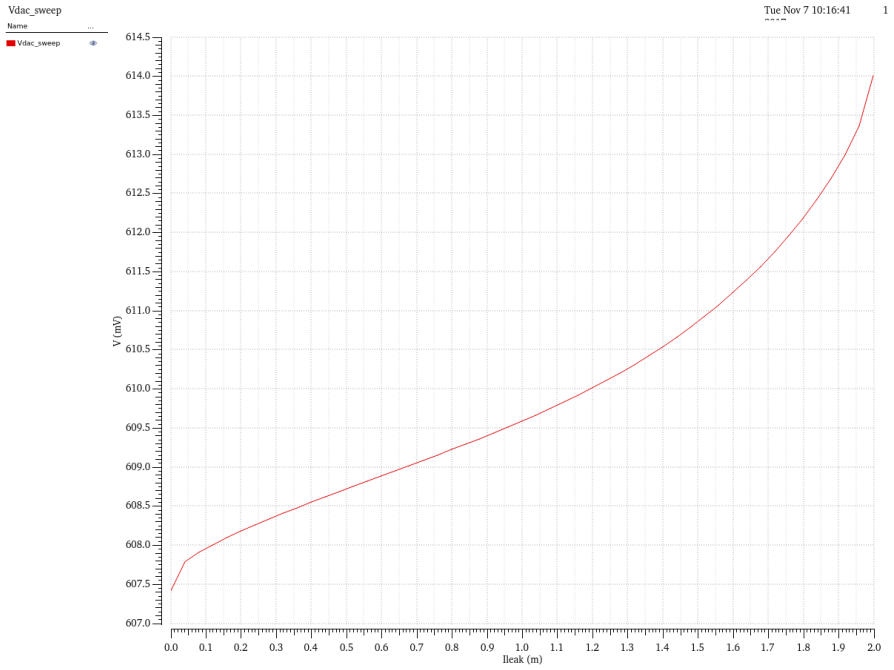

Figure 2 - Vdac versus leakage current - from 0 to 2mA - Lowest DAC voltage

Simulation shows that the input DAC is insensitive to leakage up to very large value in regard of dark current of SiPM. The voltage drift of the input DAC is contained within 3 to 7mV for a 2mA leakage. There is no problem on that part of the chip which is not responsible of the pedestal shift during large NSB acquisition periods. Other simulation must be conducted to understand that pedestal shift and will be conducted in a next version of the present report. That baseline shift is certainly induced by a pile up effect that requires very long simulation to detect.

3.2 Trigger line bandwidth

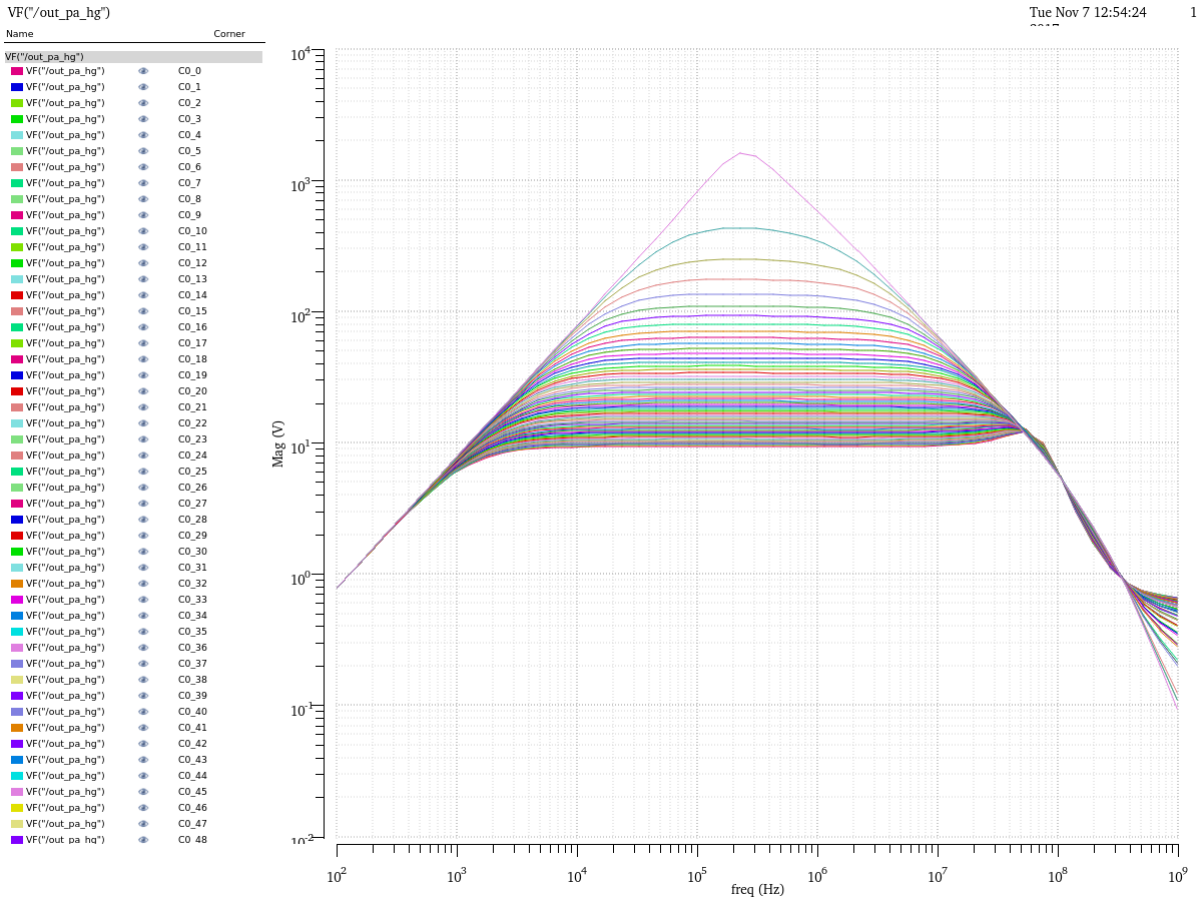

Figure 3 - CLosed loop high-gain preamplifier bode diagram for all 64 gain

The preamplifier GBWP is constant thus the higher the gain the lower the bandwidth as shown in Figure 3. The choice of the gain is very important to analyse the bandwidth of the trigger line.
The open loop bandwidth of that preamplifier is 472kHz and the GBWP is 358MHz as shown in Figure 4.

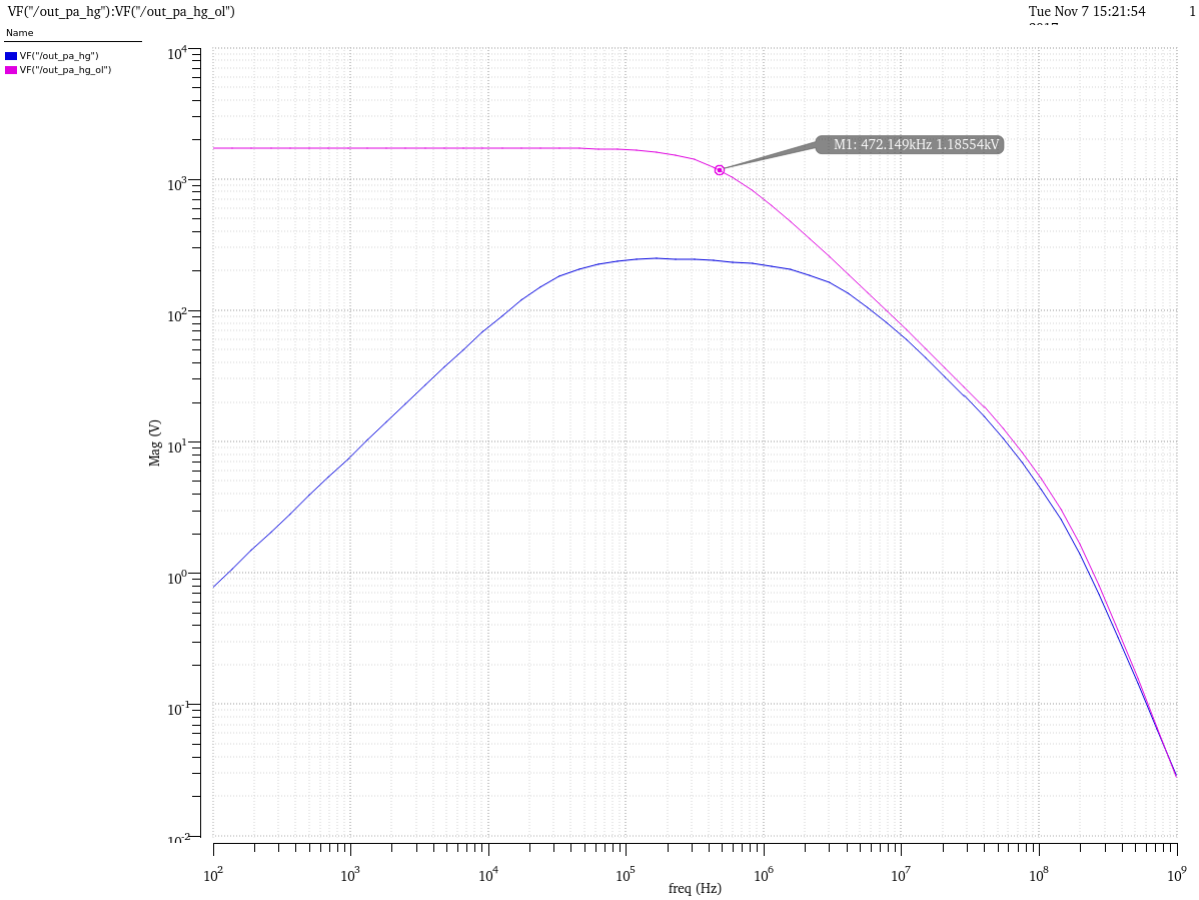

Figure 4 - Open and closed loop high gain preamplifier bode diagram (Cf=100fF)

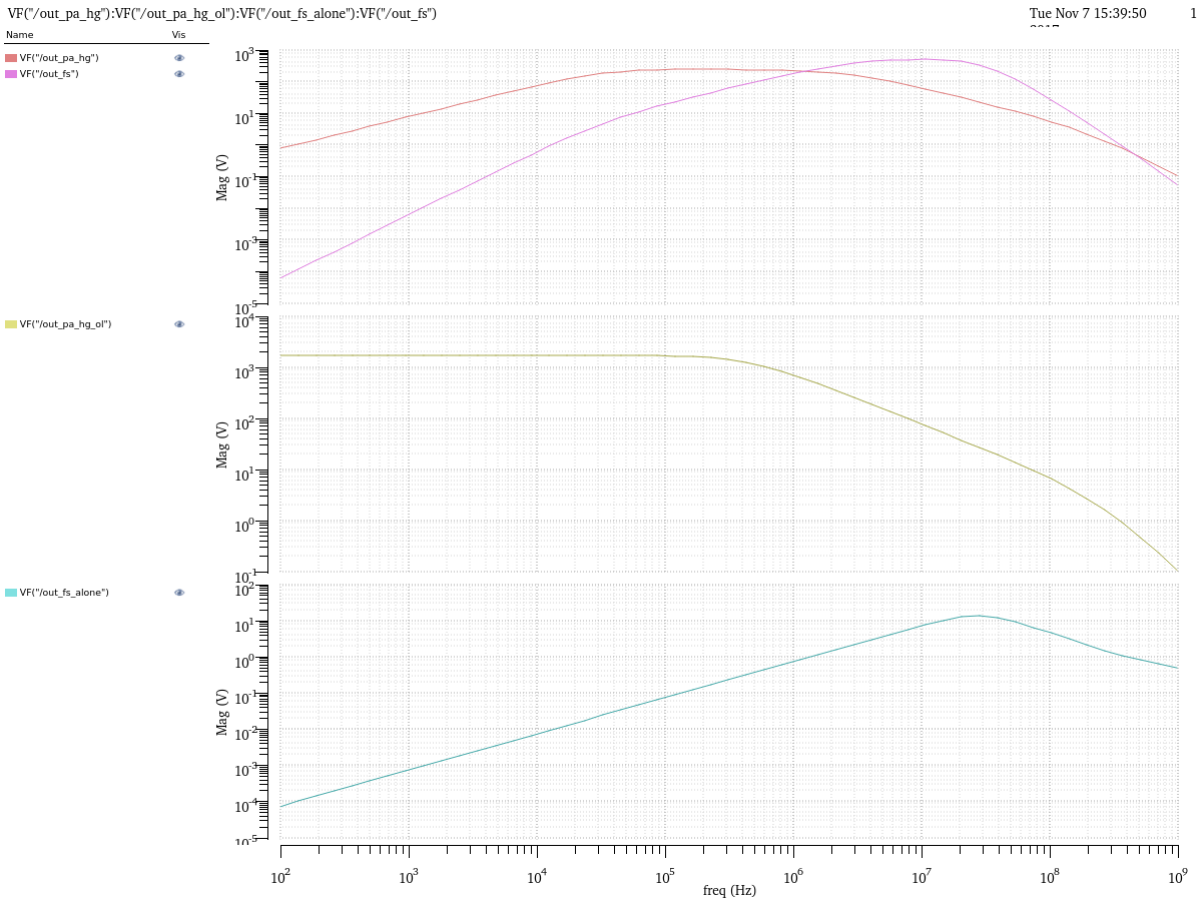

Figure 5 - Bode diagram of the trigger line

Top : red closed loop preamplifier bode – purple : whole chain bode
Middle : open loop preamplifier bode
Bottom : closed loop fast shaper alone

The preamplifier and fast shaper bandwidth has been simulated at 25MHz when the fast shaper alone as a bandwidth of 40MHz. This is due to the fact that the active band of fast shaper is above the cutoff frequency of the preamplifier at the given gain (300).
In order to get a gigher bandwidth targeted at 100MHz, two blocks must be optimized:

- High gain preamplifier
- Fast shaper

The discriminator used in Citiroc1A has been studied in Petiroc2A project and has a bandwidth in the 1GHz range. It will not be studied here as it is not impacting the bandwidth of the system.

3.3 Real versus ideal analysis

Ideal blocks with infinite bandwidth have been designed for simulation purpose. The aim of these blocks (preamplifier and shaper) is to better understand the impact of blocks improvement.

3.3.1 Preamplifier

An ideal preamplifier has been designed and the bode diagram of both real and ideal preamplifiers are shown in Figure 6.

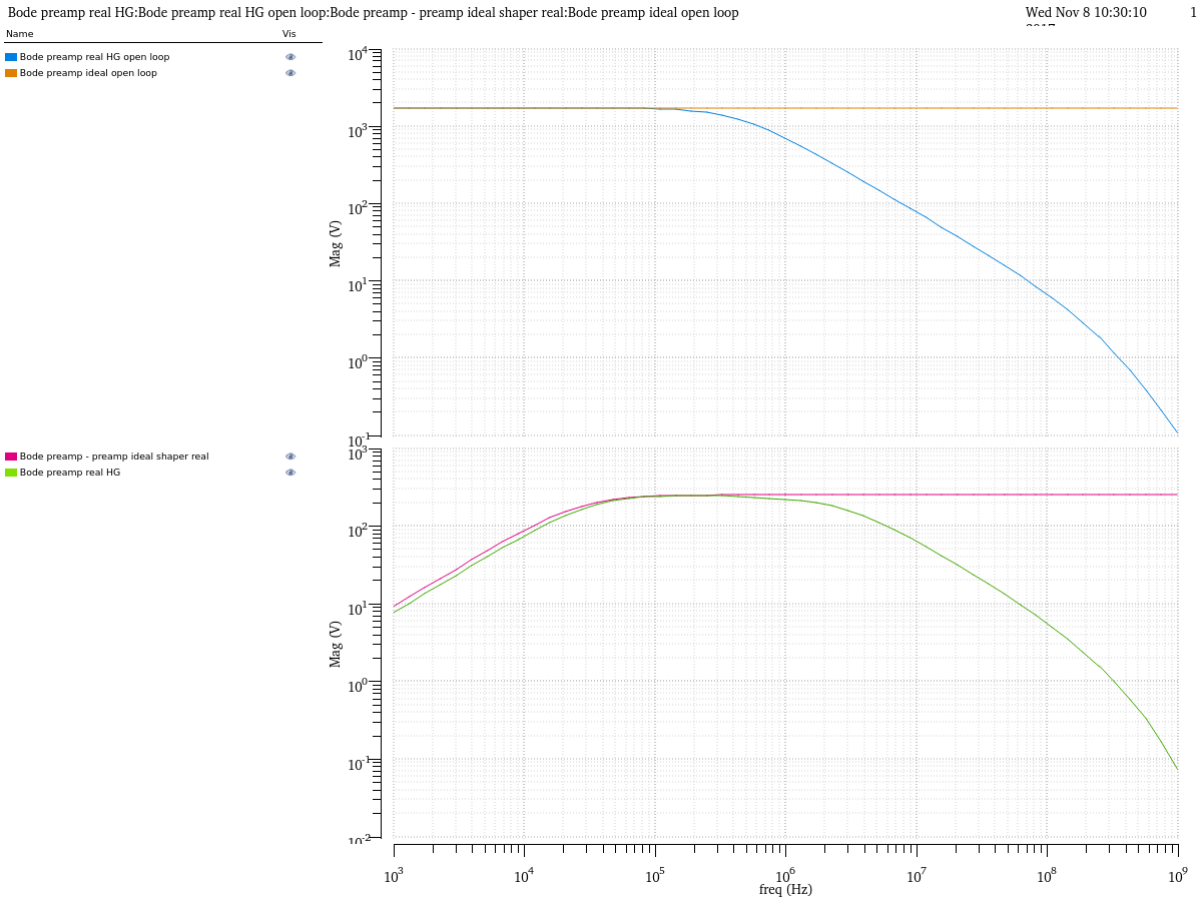

Figure 6 - Real and ideal bode diagram for high gain preamplifier

Top – open loop
Bottom – closed loop

The bandwidth of the ideal preamplifier is infinite as there is no low pass filtering on the preamplifier. Real preamplifier bandwidth is limited by the bandwidth of the amplifier (forward path) and depends on the feedback, thus the gain of the closed loop preamplifier.

3.3.2 Shaper

An ideal fast shaper has been designed and the bode diagram of both real and ideal shapers are shown in Figure 7.

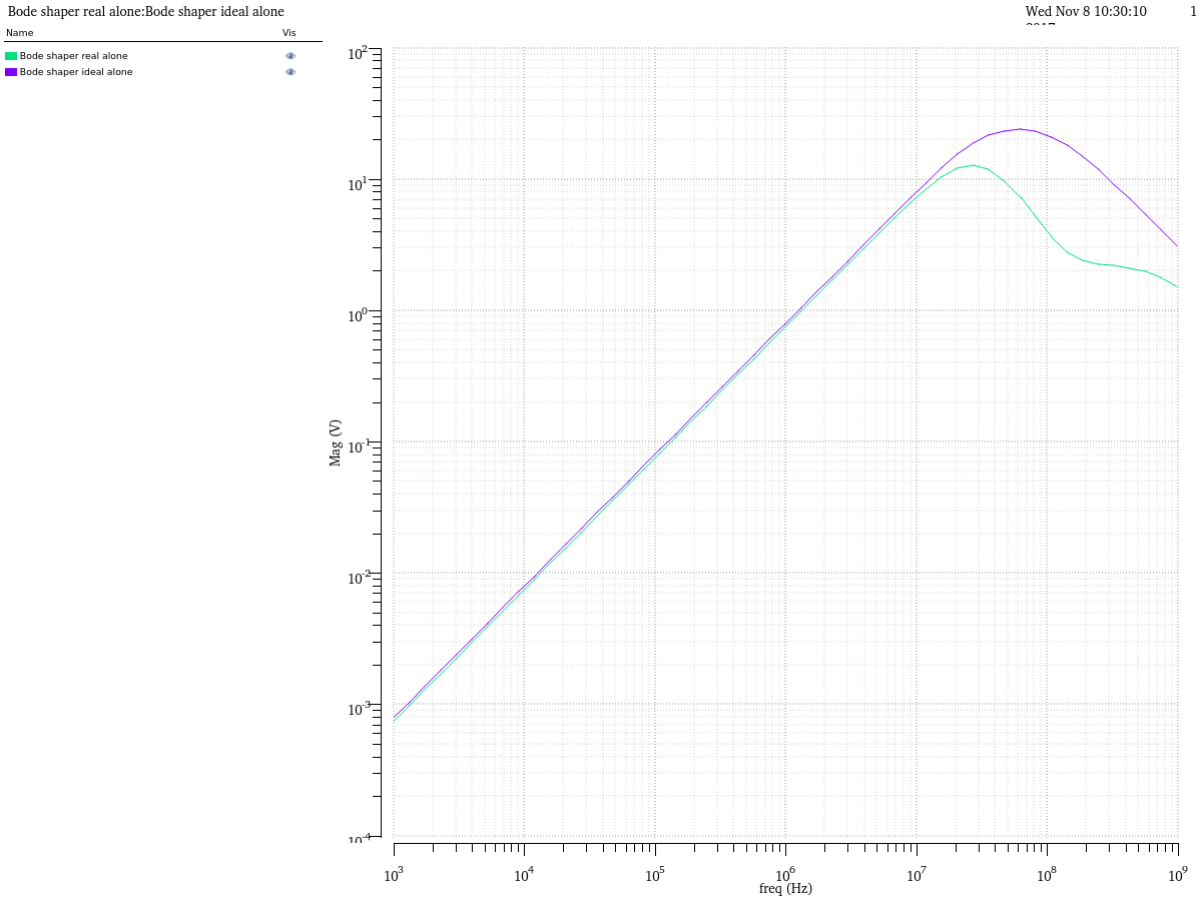

Figure 7 - Bode diagram of ideal and real fast shaper (alone, no preamp)

Simulation shows a bandwidth limitation of the real shaper due to amplifier bandwidth limitation. That induces a higher shaping time and a lower gain compared to the ideal shaper with infinite bandwidth. That effect is seen in measurement and improving the bandwidth of the shaper amplifier will improve the peaking time. The bandwidth of the real shaper alone has been simulated at 38MHz when the ideal shaper has a bandwidth of 137MHz.

3.3.3 Trigger line

The complete trigger line has been simulated with different configuration:

- Real preamplifier and real fast shaper
- Ideal preamplifier and real fast shaper
- Real preamplifier and ideal fast shaper
- Ideal preamplifier and ideal fast shaper

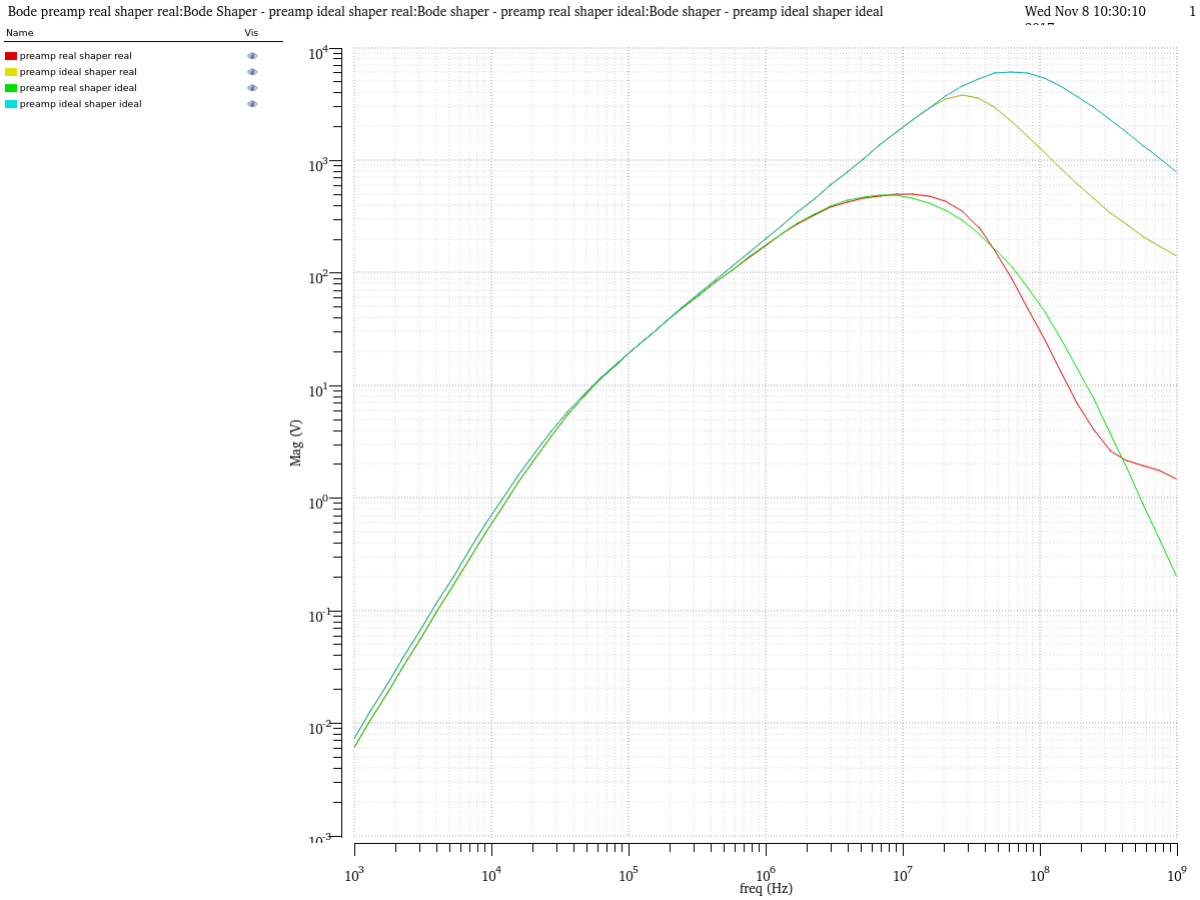

Figure 8 - Bode diagram of whole trigger chain with 4 different block configuration

The obtained bandwidths have been calculated and are shown in the table below.

Preamplifier type	Shaper type	Bandwidth
Real	Real	25.4 MHz
Real	Ideal	19.6MHz
Ideal	Real	39.6 MHz
Ideal	Ideal	131 MHz

Table 3 - Bandwidths of the whole trigger chain

As a conclusion, it is sufficient but necessary to respin both preamplifier and shaper to obtain the target bandwidth of 100MHz.

4 Conclusion

The respin of Citiroc1A is feasible to obtain the target requirement specification. It is mandatory to respin both Preamplifier and fast shaper to obtain such performances. The technology parameters allow such performances.
It is important to study non-regression of the respin. This can be done in the first part of the respin project.
Another issue detected during high luminosity night thus large NSB is still to be investigated; it will affect the charge measurement path. Work on that part is already ongoing.