Asociación Civil para la Investigación, Promoción y Desarrollo de los Sistemas Electrónicos Embebidos

Seminario de Electrónica Sistemas Embebidos

Laboratorio de Sistemas Embebidos

LPCXpresso - Salidas

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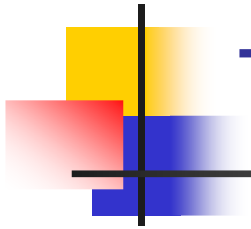
Buenos Aires, 25 de Agosto de 2016

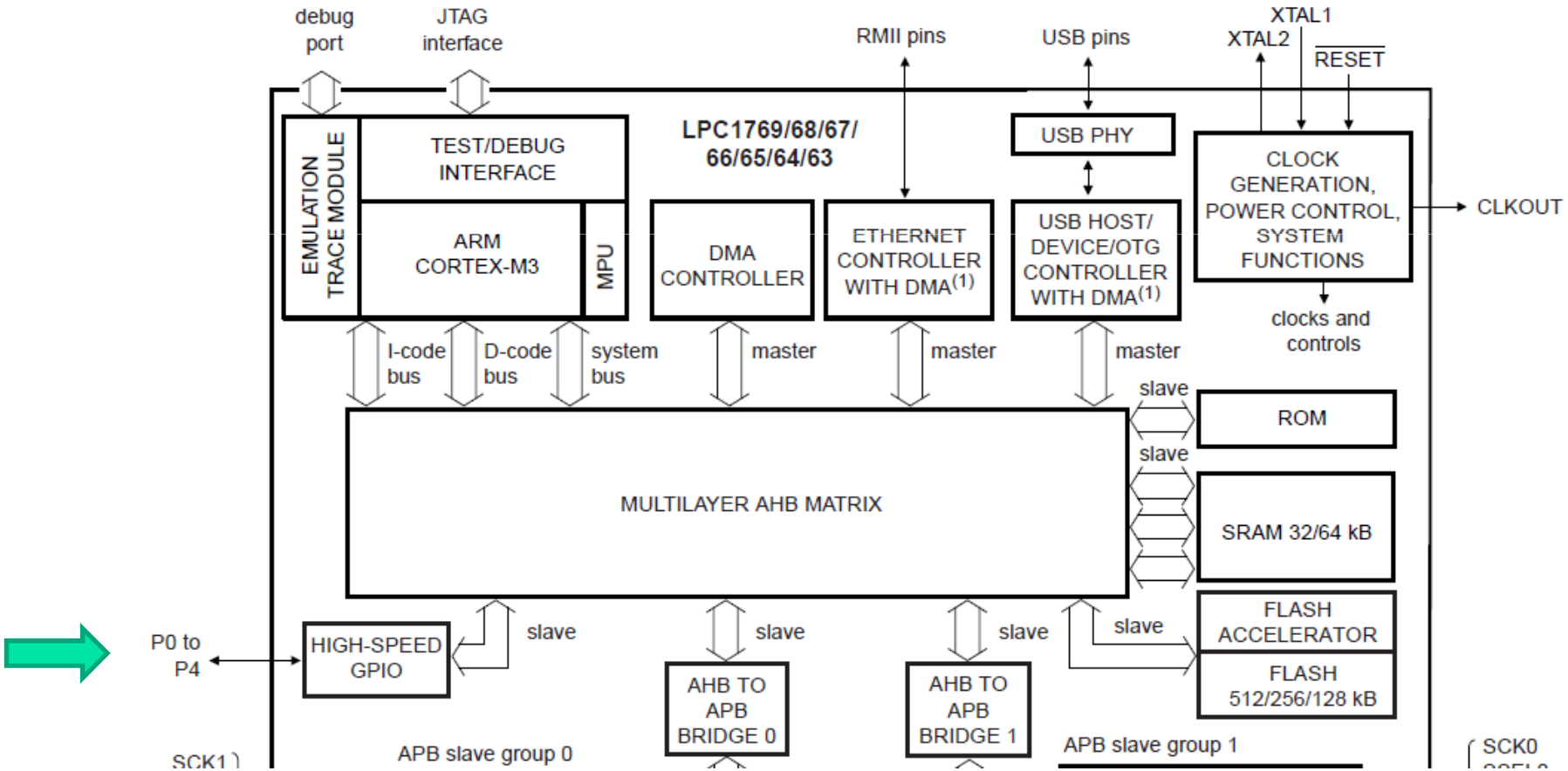


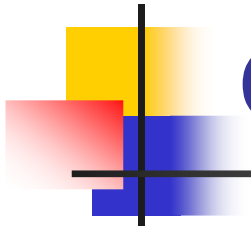
Temario

- Manejo de Salidas
  - GPIOs del uC LPC1769
  - Led del LPC1769 LPCXpresso Board
  - LED => Actividad Práctica => TP1
  - Leds del LPCXpresso/MBED Base Board
  - LED RGB LPCXpresso/MBED Base Board
  - LED RGB => Actividad Práctica => TP1

<http://www.sase.com.ar/asociacion-civil-sistemas-embebidos/escuela/>

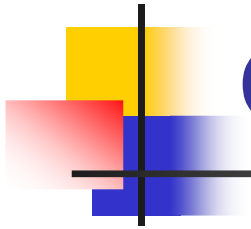
GPIOs del uC LPC1769





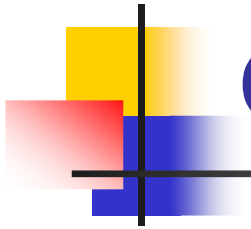
GPIOs del uC LPC1769

- **Fast general purpose parallel I/O**
  - Los pines no conectados a un peripérico específico pueden ser controlados mediante los registros de GPIO
  - Estos pines **pueden configurarse dinámicamente** como entradas o salidas
  - Registros separados permiten **forzar** a nivel alto o bajo **simultáneamente** el número de salidas que se desee (hasta 32)
  - Es posible **leer** el valor almacenado en un **registro de salida** así como el **estado** en que se encuentran **los pines de un port**



GPIOs del uC LPC1769

- **LPC17xx use accelerated GPIO functions:**
  - Los registros de **GPIO** se acceden vía AHB multilayer bus pudiéndose lograr el más **rápido** tiempo de **acceso** posible a I/O
  - Mediante registro de máscara se puede tratar conjuntos de bits de un port como un grupo, manteniendo inalterable al resto de los bits
  - Los registros de GPIO son direccionables: **byte/half-word/word**
  - Soporta el modo **bit banding** de Cortex-M3
  - Soporta el **uso mediante** el controlador **GPDMA**



GPIOs del uC LPC1769

- Los pines del **Port 0** y **Port 2** (en total **42 pines**) provistos de función digital para **generar interrupción** por flanco ascendente, descendente o ambos
- Como la **detección** de flanco es **asicrónica**, pude operar sin clock (durante Power-down mode), de modo que cualquier interrupción habilitada puede usarse para **despertar al uC**
- Prestaciones
  - Registros de **Set/Clear** nivel de bit level permiten activar/pasivar cuantos bit desee de un port mediante una sóla instrucción
  - Control individual de **Dirección de bit**
  - Todas las I/O por default se configuran como **inputs** desde **reset**
  - Se puede programar cada GPIO pin con **Pull-up/pull-down** resistor y **open-drain** mediante **pin connect block**

GPIOs del uC LPC1769

- **Pin connect block**: **PINSEL/PINMODE** controlan función/modo asignada/o a cada pin (dos bits de PINSEL y tres bits PMODE por pin)

Table 74. Summary of PINSEL registers

Register	Controls	Table
PINSEL0	P0[15:0]	Table 79
PINSEL1	P0 [31:16]	Table 80
PINSEL2	P1 [15:0] (Ethernet)	Table 81
PINSEL3	P1 [31:16]	Table 82
PINSEL4	P2 [15:0]	Table 83
PINSEL5	P2 [31:16]	not used
PINSEL6	P3 [15:0]	not used
PINSEL7	P3 [31:16]	Table 84
PINSEL8	P4 [15:0]	not used
PINSEL9	P4 [31:16]	Table 85
PINSEL10	Trace port enable	Table 86

Table 75. Pin function select register bits

PINSEL0 to PINSEL9 Values	Function	Value after Reset
00	Primary (default) function, typically GPIO port	00
01	First alternate function	
10	Second alternate function	
11	Third alternate function	

Table 76. Pin Mode Select register Bits

PINMODE0 to PINMODE9 Values	Function	Value after Reset
00	Pin has an on-chip pull-up resistor enabled.	00
01	Repeater mode (see text below).	
10	Pin has neither pull-up nor pull-down resistor enabled.	
11	Pin has an on-chip pull-down resistor enabled.	

Table 77. Open Drain Pin Mode Select register Bits

PINMODE_OD0 to PINMODE_OD4 Values	Function	Value after Reset
0	Pin is in the normal (not open drain) mode.	00
1	Pin is in the open drain mode.	

GPIOs del uC LPC1769

Table 79. Pin function select register 0 (PINSEL0 - address 0x4002 C000) bit description

PINSEL0	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P0.0	GPIO Port 0.0	RD1	TXD3	SDA1	00
3:2	P0.1	GPIO Port 0.1	TD1	RXD3	SCL1	00
5:4	P0.2	GPIO Port 0.2	TXD0	AD0.7	Reserved	00
7:6	P0.3	GPIO Port 0.3	RXD0	AD0.6	Reserved	00
9:8	P0.4[1]	GPIO Port 0.4	I2SRX_CLK	RD2	CAP2.0	00
11:10	P0.5[1]	GPIO Port 0.5	I2SRX_WS	TD2	CAP2.1	00
13:12	P0.6	GPIO Port 0.6	I2SRX_SDA	SSEL1	MAT2.0	00
15:14	P0.7	GPIO Port 0.7	I2STX_CLK	SCK1	MAT2.1	00
17:16	P0.8	GPIO Port 0.8	I2STX_WS	MISO1	MAT2.2	00
19:18	P0.9	GPIO Port 0.9	I2STX_SDA	MOSI1	MAT2.3	00
21:20	P0.10	GPIO Port 0.10	TXD2	SDA2	MAT3.0	00
23:22	P0.11	GPIO Port 0.11	RXD2	SCL2	MAT3.1	00
29:24	-	Reserved	Reserved	Reserved	Reserved	0
31:30	P0.15	GPIO Port 0.15	TXD1	SCK0	SCK	00

[1] Not available on 80-pin package.

GPIOs del uC LPC1769

Table 87. Pin Mode select register 0 (PINMODE0 - address 0x4002 C040) bit description

PINMODE0	Symbol	Value	Description	Reset value
1:0	P0.00MODE		Port 0 pin 0 on-chip pull-up/down resistor control.	00
		00	P0.0 pin has a pull-up resistor enabled.	
		01	P0.0 pin has repeater mode enabled.	
		10	P0.0 pin has neither pull-up nor pull-down.	
		11	P0.0 has a pull-down resistor enabled.	
3:2	P0.01MODE		Port 0 pin 1 control, see P0.00MODE.	00
5:4	P0.02MODE		Port 0 pin 2 control, see P0.00MODE.	00
7:6	P0.03MODE		Port 0 pin 3 control, see P0.00MODE.	00
9:8	P0.04MODE[1]		Port 0 pin 4 control, see P0.00MODE.	00
11:10	P0.05MODE[1]		Port 0 pin 5 control, see P0.00MODE.	00
13:12	P0.06MODE		Port 0 pin 6 control, see P0.00MODE.	00
15:14	P0.07MODE		Port 0 pin 7 control, see P0.00MODE.	00
17:16	P0.08MODE		Port 0 pin 8 control, see P0.00MODE.	00
19:18	P0.09MODE		Port 0 pin 9control, see P0.00MODE.	00
21:20	P0.10MODE		Port 0 pin 10 control, see P0.00MODE.	00
23:22	P0.11MODE		Port 0 pin 11 control, see P0.00MODE.	00
29:24	-		Reserved.	NA
31:30	P0.15MODE		Port 0 pin 15 control, see P0.00MODE.	00

[1] Not available on 80-pin package.

GPIOs del uC LPC1769

Table 100. GPIO pin description

Pin Name	Type	Description
P0[30:0][1]; P1[31:0][2]; P2[13:0]; P3[26:25]; P4[29:28]	Input/ Output	General purpose input/output. These are typically shared with other peripherals functions and will therefore not all be available in an application. Packaging options may affect the number of GPIOs available in a particular device. Some pins may be limited by requirements of the alternate functions of the pin. For example, the pins containing the I^2C0 functions are open-drain for any function selected on that pin. Details may be found in Section 7.1.1.

[1] P0[14:12] are not available.

[2] P1[2], P1[3], P1[7:5], P1[13:11] are not available.

Table 94. Open Drain Pin Mode select register 0 (PINMODE_OD0 - address 0x4002 C068) bit description

PINMODE_OD0	Symbol	Value	Description	Reset value
0	P0.00OD[3]		Port 0 pin 0 open drain mode control.	0
		0	P0.0 pin is in the normal (not open drain) mode.	
		1	P0.0 pin is in the open drain mode.	
1	P0.01OD[3]		Port 0 pin 1 open drain mode control, see P0.00OD	0
2	P0.02OD		Port 0 pin 2 open drain mode control, see P0.00OD	0
3	P0.03OD		Port 0 pin 3 open drain mode control, see P0.00OD	0
4	P0.04OD		Port 0 pin 4 open drain mode control, see P0.00OD	0
5	P0.05OD		Port 0 pin 5 open drain mode control, see P0.00OD	0
6	P0.06OD		Port 0 pin 6 open drain mode control, see P0.00OD	0
7	P0.07OD		Port 0 pin 7 open drain mode control, see P0.00OD	0
8	P0.08OD		Port 0 pin 8 open drain mode control, see P0.00OD	0
9	P0.09OD		Port 0 pin 9 open drain mode control, see P0.00OD	0

GPIOs del uC LPC1769

Table 100. GPIO pin description

Pin Name	Type	Description
P0[30:0][1]; P1[31:0][2]; P2[13:0]; P3[26:25]; P4[29:28]	Input/ Output	General purpose input/output. These are typically shared with other peripherals functions and will therefore not all be available in an application. Packaging options may affect the number of GPIOs available in a particular device. Some pins may be limited by requirements of the alternate functions of the pin. For example, the pins containing the I^2C0 functions are open-drain for any function selected on that pin. Details may be found in Section 7.1.1.

[1] P0[14:12] are not available.

[2] P1[2], P1[3], P1[7:5], P1[13:11] are not available.

GPIOs del uC LPC1769

Table 101. GPIO register map (local bus accessible registers - enhanced GPIO features)

Generic Name	Description	Access	Reset value[1]	PORTn Register Name & Address
FIODIR	Fast GPIO Port Direction control register. This register individually controls the direction of each port pin.	R/W	0	FIO0DIR - 0x2009 C000 FIO1DIR - 0x2009 C020 FIO2DIR - 0x2009 C040 FIO3DIR - 0x2009 C060 FIO4DIR - 0x2009 C080
FIOMASK	Fast Mask register for port. Writes, sets, clears, and reads to port (done via writes to FIOPIN, FIOSET, and FIOCLR, and reads of FIOPIN) alter or return only the bits enabled by zeros in this register.	R/W	0	FIO0MASK - 0x2009 C010 FIO1MASK - 0x2009 C030 FIO2MASK - 0x2009 C050 FIO3MASK - 0x2009 C070 FIO4MASK - 0x2009 C090
FIOPIN	Fast Port Pin value register using FIOMASK. The current state of digital port pins can be read from this register, regardless of pin direction or alternate function selection (as long as pins are not configured as an input to ADC). The value read is masked by ANDing with inverted FIOMASK. Writing to this register places corresponding values in all bits enabled by zeros in FIOMASK. **Important:** if an FIOPIN register is read, its bit(s) masked with 1 in the FIOMASK register will be read as 0 regardless of the physical pin state.	R/W	0	FIO0PIN - 0x2009 C014 FIO1PIN - 0x2009 C034 FIO2PIN - 0x2009 C054 FIO3PIN - 0x2009 C074 FIO4PIN - 0x2009 C094
FIOSET	Fast Port Output Set register using FIOMASK. This register controls the state of output pins. Writing 1s produces highs at the corresponding port pins. Writing 0s has no effect. Reading this register returns the current contents of the port output register. Only bits enabled by 0 in FIOMASK can be altered.	R/W	0	FIO0SET - 0x2009 C018 FIO1SET - 0x2009 C038 FIO2SET - 0x2009 C058 FIO3SET - 0x2009 C078 FIO4SET - 0x2009 C098
FIOCLR	Fast Port Output Clear register using FIOMASK. This register controls the state of output pins. Writing 1s produces lows at the corresponding port pins. Writing 0s has no effect. Only bits enabled by 0 in FIOMASK can be altered.	WO	0	FIO0CLR - 0x2009 C01C FIO1CLR - 0x2009 C03C FIO2CLR - 0x2009 C05C FIO3CLR - 0x2009 C07C FIO4CLR - 0x2009 C09C

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

GPIOs del uC LPC1769

Table 103. Fast GPIO port Direction register FIO0DIR to FIO4DIR - addresses 0x2009 C000 to 0x2009 C080) bit description

Bit	Symbol	Value	Description	Reset value
31:0	FIO0DIR FIO1DIR FIO2DIR FIO3DIR FIO4DIR		Fast GPIO Direction PORTx control bits. Bit 0 in FIOxDIR controls pin Px.0, bit 31 in FIOxDIR controls pin Px.31.	0x0
		0	Controlled pin is input.	
		1	Controlled pin is output.	

Table 105. Fast GPIO port output Set register (FIO0SET to FIO4SET - addresses 0x2009 C018 to 0x2009 C098) bit description

Bit	Symbol	Value	Description	Reset value
31:0	FIO0SET FIO1SET FIO2SET FIO3SET FIO4SET		Fast GPIO output value Set bits. Bit 0 in FIOxSET controls pin Px.0, bit 31 in FIOxSET controls pin Px.31.	0x0
		0	Controlled pin output is unchanged.	
		1	Controlled pin output is set to HIGH.	

Table 107. Fast GPIO port output Clear register (FIO0CLR to FIO4CLR- addresses 0x2009 C01C to 0x2009 C09C) bit description

Bit	Symbol	Value	Description	Reset value
31:0	FIO0CLR FIO1CLR FIO2CLR FIO3CLR FIO4CLR		Fast GPIO output value Clear bits. Bit 0 in FIOxCLR controls pin Px.0, bit 31 controls pin Px.31.	0x0
		0	Controlled pin output is unchanged.	
		1	Controlled pin output is set to LOW.	

GPIOs del uC LPC1769

Table 109. Fast GPIO port Pin value register (FIO0PIN to FIO4PIN- addresses 0x2009 C014 to 0x2009 C094) bit description

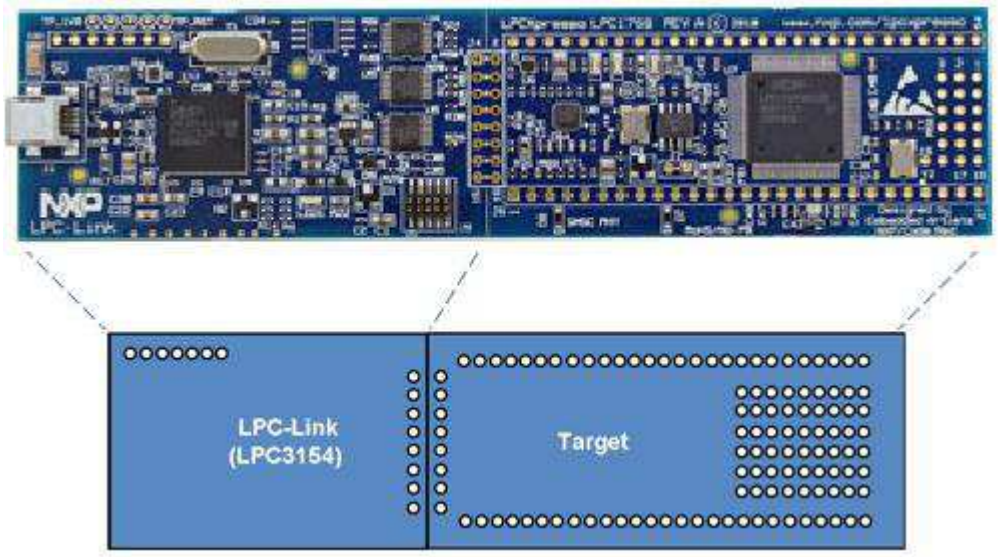
Bit	Symbol	Value	Description	Reset value
31:0	FIO0VAL FIO1VAL FIO2VAL FIO3VAL FIO4VAL		Fast GPIO output value bits. Bit 0 corresponds to pin Px.0, bit 31 corresponds to pin Px.31. Only bits also set to 0 in the FIOxMASK register are affected by a write or show the pin's actual logic state.	0x0
		0	Reading a 0 indicates that the port pin's current state is LOW. Writing a 0 sets the output register value to LOW.	
		1	Reading a 1 indicates that the port pin's current state is HIGH. Writing a 1 sets the output register value to HIGH.	

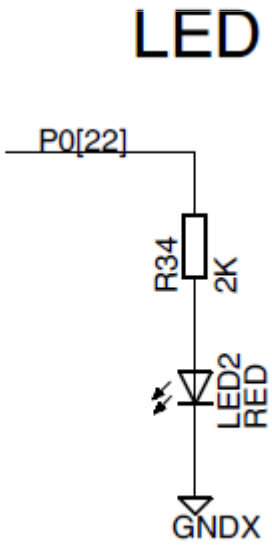
Table 111. Fast GPIO port Mask register (FIO0MASK to FIO4MASK - addresses 0x2009 C010 to 0x2009 C090) bit description

Bit	Symbol	Value	Description	Reset value
31:0	FIO0MASK FIO1MASK FIO2MASK FIO3MASK FIO4MASK		Fast GPIO physical pin access control.	0x0
		0	Controlled pin is affected by writes to the port's FIOxSET, FIOxCLR, and FIOxPIN register(s). Current state of the pin can be read from the FIOxPIN register.	
		1	Controlled pin is not affected by writes into the port's FIOxSET, FIOxCLR and FIOxPIN register(s). When the FIOxPIN register is read, this bit will not be updated with the state of the physical pin.	

Led del LPCXpresso LPC1769 board

- **Circuito** => **LPCXpressoLPC1769revB.pdf**
  - **1 led rojo** => p/experimentar con Salidas Digitales
  - **LED** => **P0[22]** (Port 0, Pin 22)
  - "**1**" => **Enciende** / "**0**" => **Apaga**





Led LPCXpresso/MBED Base Board

- **Manual =>LPCXpresso_BaseBoard_rev_B_Users_Guide.pdf**
- **Circuito => LPCXpresso_Base_Board_revB1.pdf**

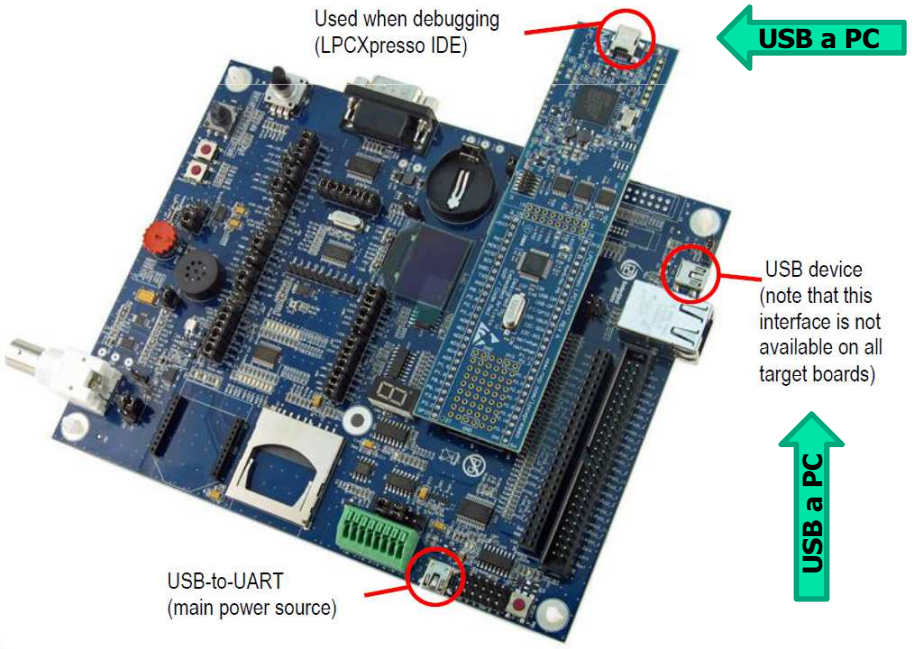
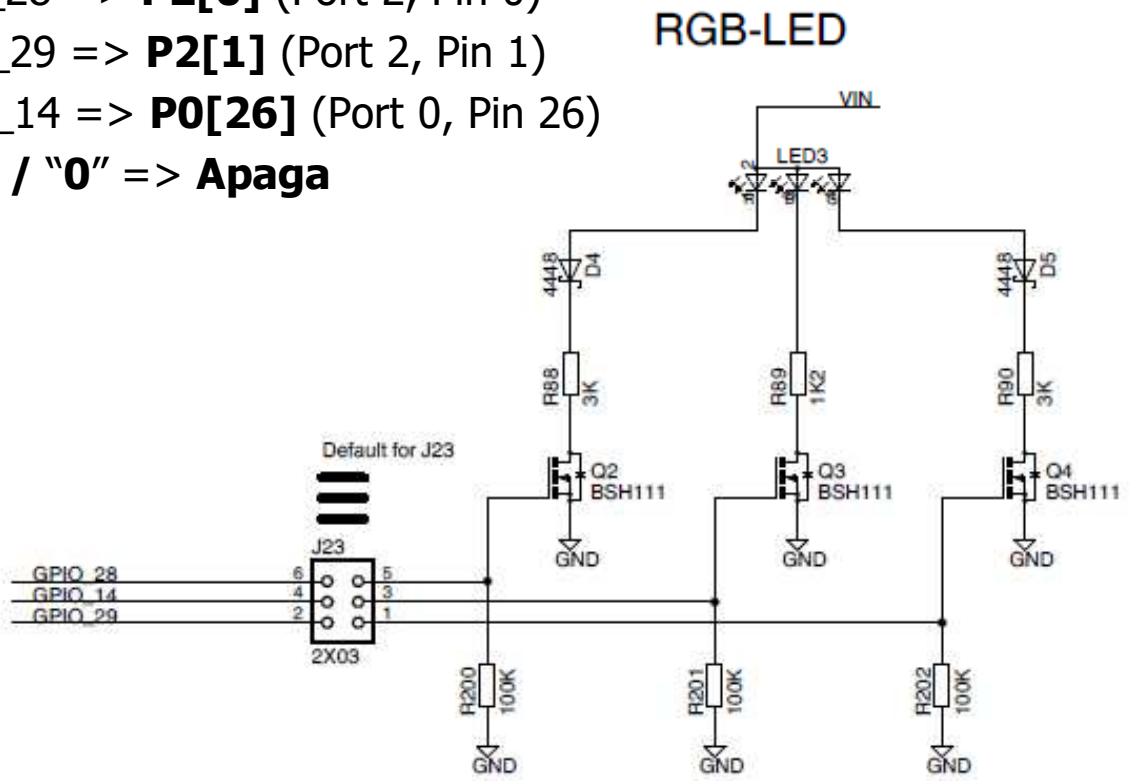


Figure 3 – Base Board with a mounted LPCXpresso LPC1343 board

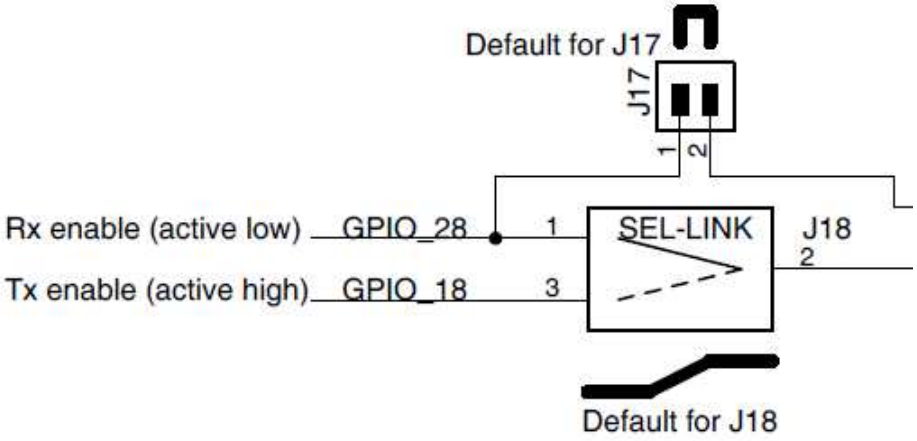
RGB LPCXpresso/MBED Base Board

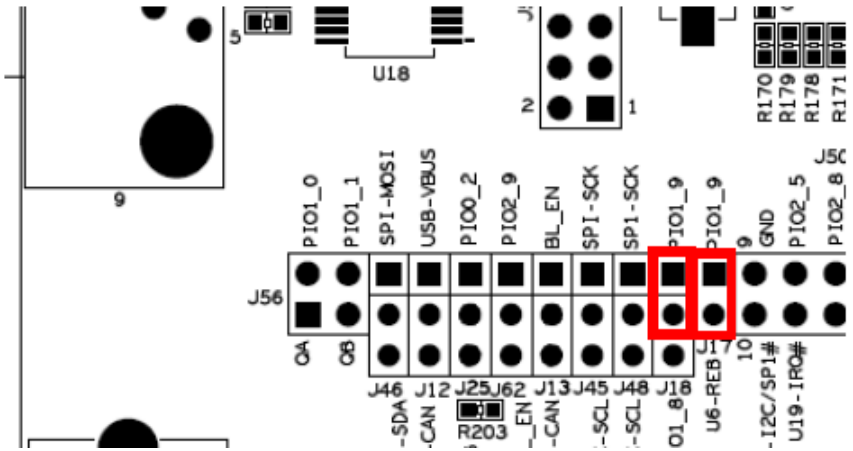
- **1 RGB LED** => p/experimentar con Salidas Digitales
  - **RED** => GPIO_28 => **P2[0]** (Port 2, Pin 0)
  - **GREEN** => GPIO_29 => **P2[1]** (Port 2, Pin 1)
  - **BLUE** => GPIO_14 => **P0[26]** (Port 0, Pin 26)
  - "**1**" => **Enciende** / "**0**" => **Apaga**



RGB LPCXpresso/MBED Base Board

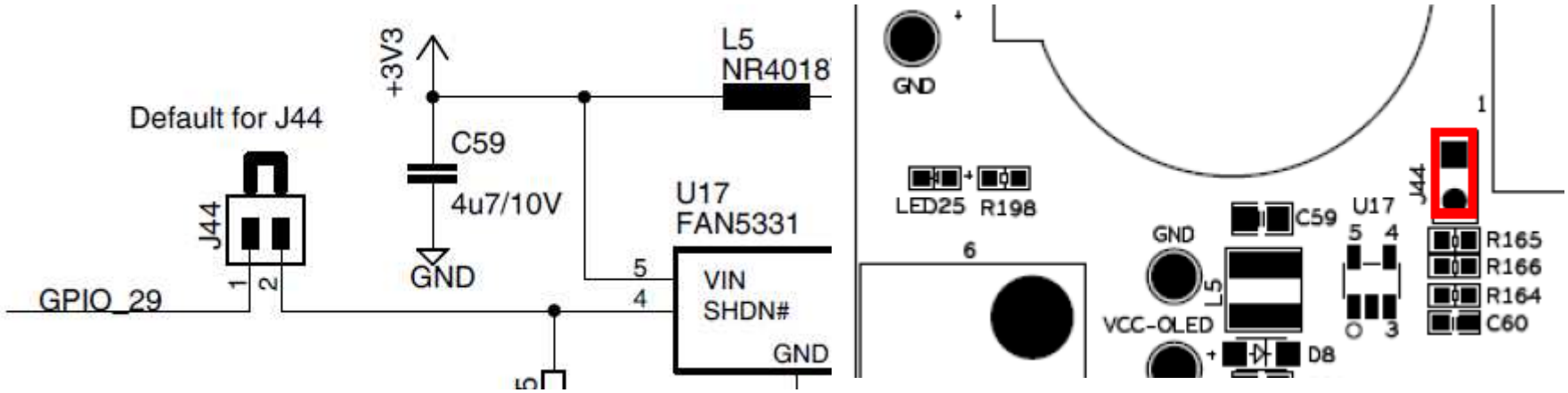
- Verifique en el circuito: c/GPIO del **RGB LED** se conecte al mismo y no se comparta con otro componente de la placa e identifique en el manual cómo colocar los jumpers
  - **RED** => GPIO_28 => **P2[0]** (Port 2, Pin 0)
  - Remover **J17**





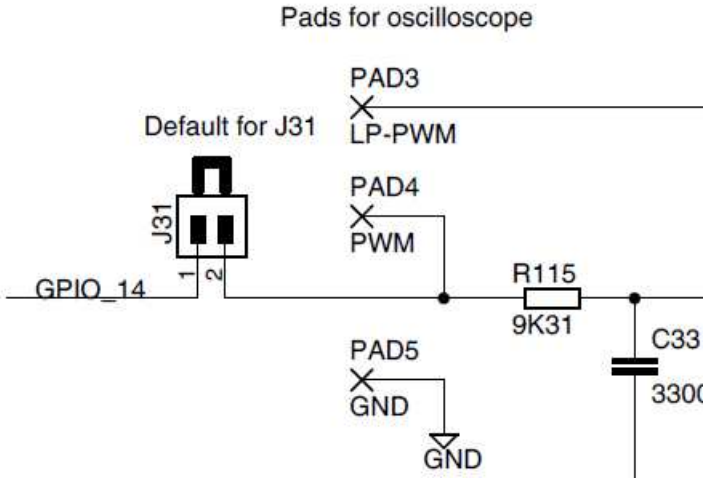
RGB LPCXpresso/MBED Base Board

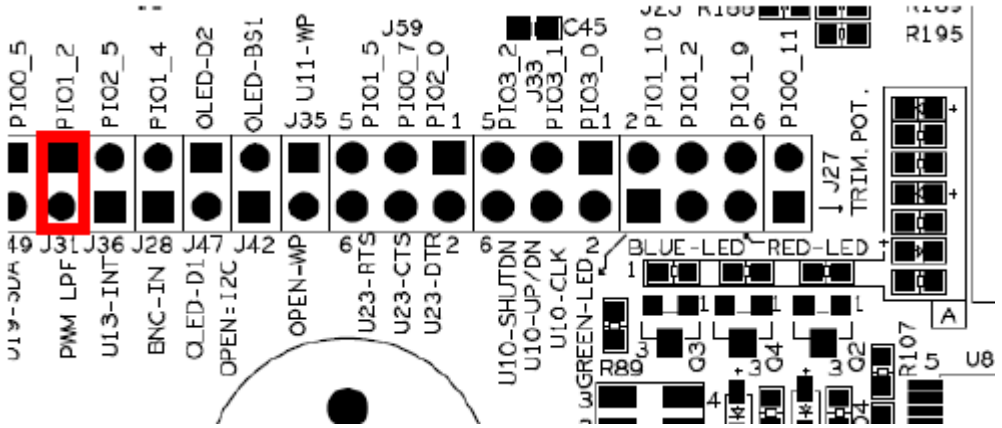
- Verifique en el circuito: c/GPIO del **RGB LED** se conecte al mismo y no se comparta con otro componente de la placa e identifique en el manual cómo colocar los jumpers
  - **GREEN** => GPIO_29 => **P2[1]** (Port 2, Pin 1)
  - Remover **J44**



RGB LPCXpresso/MBED Base Board

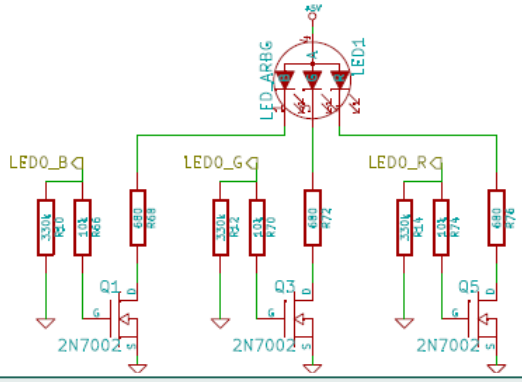
- Verifique en el circuito: c/GPIO del **RGB LED** se conecte al mismo y no se comparta con otro componente de la placa e identifique en el manual cómo colocar los jumpers
  - **BLUE** => GPIO_14 => **P0[26]** (Port 0, Pin 26)
  - Remover **J31**

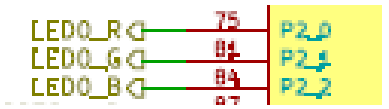




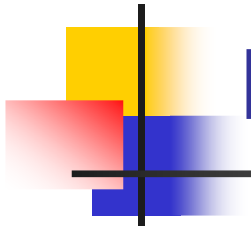
RGB EDU-CIAA-NXP

- **1 RGB LED** => p/experimentar con Salidas Digitales
  - **RED** => **P2[0]** (Port 2, pin 0) ⇔ **GPIO5[0]** (GPIO 2, bit 0)
  - **GREEN** => **P2[1]** (Port 2, pin 1) ⇔ **GPIO5[1]** (GPIO 2, bit 1)
  - **BLUE** => **P2[2]** (Port 2, pin 2) ⇔ **GPIO5[2]** (GPIO 2, bit 2)
  - "**1**" => **Enciende** / "**0**" => **Apaga**





Pin	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6	FUNC7	ANALOG SEL
P2_1	SGPIO5	U0_RXD	EMC_A12	USB0_PWR_FAULT	GPIO5[1]	R	T3_CAP1	R	
P2_2	SGPIO6	U0_UCLK	EMC_A11	USB0_IND1	GPIO5[2]	CTIN_6	T3_CAP2	R	
P2_0	SGPIO4	U0_TXD	EMC_A13	USB0_PPWR	GPIO5[0]	R	T3_CAP0	ENET_MDC	



Referencias

- **LPC1769**
  - **LPC1769_68_67_66_65_64_63.pdf** (Product data sheet, 86 pág.)
  - **UM10360.pdf** (User manual, 840 pág.)
  - **LPCXpressoLPC1769revB.pdf** (Schematics, 7 pág.)
  - **LPCXpresso_target_board_pinning_rev_A.xlsx** (Excel, 1 hoja)
  - **LPCXpresso_Base_Board_revB1.pdf** (Schematics, 11 pág.)
  - **LPCXpresso_BaseBoard_rev_B_Users_Guide.pdf** (User´s guide, 57 pág.)
- **LPC4337**
  - **LPC435X_3X_2X_1X.pdf** (Product data sheet, 161 pág.)
  - **UM10503.pdf** (User manual, 1433 pág.)
  - **EDU-CIAA-NXP_rev_1.0** (7 pág.)