# Embedded Software Essentials

Makefiles Part 1

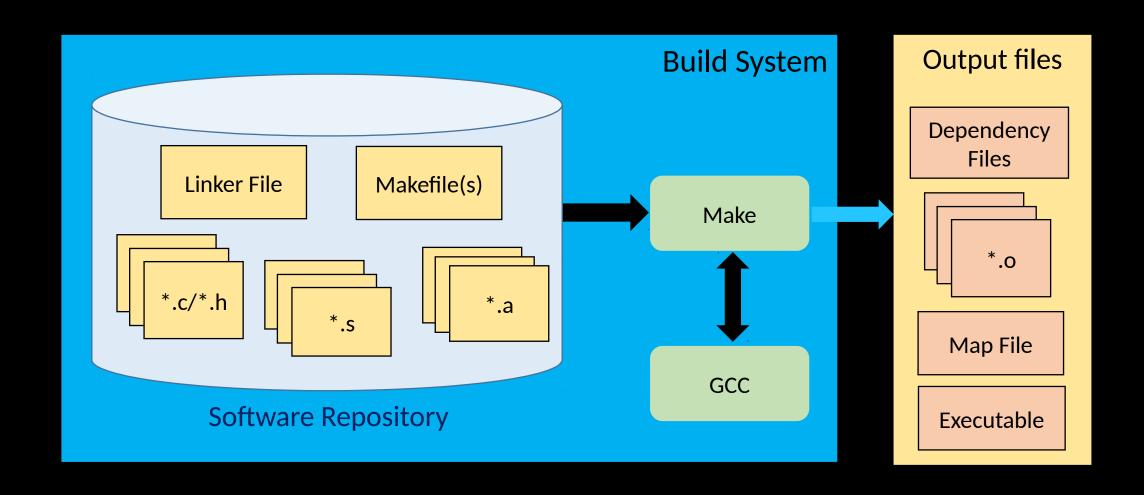
C1 M2 V7

# Copyright

 Copyright (C) 2017 by Alex Fosdick. Redistribution, modification or use of this presentation is permitted as long as the files maintain this copyright. Users are permitted to modify this and use it to learn about the field of embedded software. Alex Fosdick and the University of Colorado are not liable for any misuse of this material.

### Build System [S1] Makefile(s) Linker File **GNU Make** Executable \*.c/\*.h Dependency Map Files \*.0 Files \$ make all **Generated Files Object Files**

### Version Controlled Build System [S2]



### Makefiles [S3]

• One or more files used to tell make how to build a particular project

```
makefile, Makefile, sources.mk, includes.mk, ...
```

Makefiles have build targets or build rules

Targets can have dependencies or prerequisites

```
main.out: main.o my_file.o
gcc -g -Wl,-Map=main.map -o main.out main.o my_file.o
```

### Makefiles - Rules [S4]

- Build rules require a specific syntax of target: prerequisites, and commands
- These are **recipes** for how to build a particular executable or non-source file
- A recipe can only be executed if the dependencies are met



• Simple my\_file.o build rule: Depends on my\_file.c and my\_file.h

```
$ make my_file.o

Generates the my_file.o target by executing the following rule
```

```
my_file.o: my_file.c my_file.h
    gcc -c my_file.c -o my_file.o
```

# Makefile Syntax [\$5] is a comment

- Comments start with a #
- Can include other makefiles
- Line continuation is done with a \
- Can create and use variables
- Can have multiple rules
- Command lines start with a tab
- Targets can depend on other targets

```
# This includes another file
include sources.mk
# Variable & Line Continuance
FLAGS = -g
        -Werror \
        -std=c99
# my_file.o target binary
my_file.o: my_file.h my_file.c
    gcc $(FLAGS) -c -o my_file.o my_file.c
# main.o target binary
main.o: my_file.h
    gcc $(FLAGS) -c -o main.o main.c
# Main Target Executable
main.out: main.o my_file.o
    gcc -o main.out main.o my_file.o
```

- Comments start with a #
- Can include other makefiles
- Line continuation is done with a \
- Can create and use variables
- Can have multiple rules
- Command lines start with a tab
- Targets can depend on other targets

```
# This is a comment
# This includes another file
include sources.mk
# Variable & Line Continuance
FLAGS = -g
        -Werror \
        -std=c99
# my_file.o target binary
my_file.o: my_file.h my_file.c
    qcc $(FLAGS) -c -o my file.o my file.c
# main.o target binary
main.o: my_file.h
    gcc $(FLAGS) -c -o main.o main.c
# Main Target Executable
main.out: main.o my_file.o
    gcc -o main.out main.o my_file.o
```

- Comments start with a #
- Can include other makefiles
- Line continuation is done with a \
- Can create and use variables
- Can have multiple rules
- Command lines start with a tab
- Targets can depend on other targets

```
# This is a comment
# This includes another file
include sources.mk
# Variable & Line Continuance
FLAGS = -g
        -Werror \
        -std=c99
# my_file.o target binary
my_file.o: my_file.h my_file.c
    gcc $(FLAGS) -c -o my_file.o my_file.c
# main.o target binary
main.o: my_file.h
   gcc $(FLAGS) -c -o main.o main.c
# Main Target Executable
main.out: main.o my_file.o
    gcc -o main.out main.o my_file.o
```

- Comments start with a #
- Can include other makefiles
- Line continuation is done with a
- Can create and use variables
- Can have multiple rules
- Command lines start with a tab
- Targets can depend on other targets

```
# This is a comment
# This includes another file
include sources.mk
# Variable & Line Continuance
FLAGS = -g
        -Werror \
        -std=c99
# my_file.o target binary
my_file.o: my_file.h my_file.c
    gcc $(FLAGS) -c -o my_file.o my_file.c
# main.o target binary
main.o: my_file.h
    gcc $(FLAGS) -c -o main.o main.c
# Main Target Executable
main.out: main.o my_file.o
    gcc -o main.out main.o my_file.o
```

- Comments start with a #
- Can include other makefiles
- Line continuation is done with a \
- Can create and use variables
- Can have multiple rules
- Command lines start with a tab
- Targets can depend on other targets

```
# This is a comment
# This includes another file
include sources.mk
# Variable & Line Continuance
FLAGS = -g
        -Werror \
        -std=c99
# my_file.o target binary
my_file.o: my_file.h my_file.c
    gcc $(FLAGS) -c -o my_file.o my_file.c
# main.o target binary
main.o: my_file.h
   gcc $(FLAGS) -c -o main.o main.c
# Main Target Executable
main.out: main.o my_file.o
    gcc -o main.out main.o my_file.o
```

- Comments start with a #
- Can include other makefiles
- Line continuation is done with a \
- Can create and use variables
- Can have multiple rules
- Command lines start with a tab
- Targets can depend on other targets

```
# This is a comment
# This includes another file
include sources.mk
# Variable & Line Continuance
FLAGS = -g
        -Werror \
        -std=c99
# my_file.o target binary
my_file.o: my_file.h my_file.c
    gcc $(FLAGS) -c -o my_file.o my_file.c
# main.o target binary
main.o: my_file.h
   gcc $(FLAGS) -c -o main.o main.c
# Main Target Executable
main.out: main.o my_file.o
    gcc -o main.out main.o my_file.o
```

- Comments start with a #
- Can include other makefiles
- Line continuation is done with a \
- Can create and use variables
- Can have multiple rules
- Command lines start with a tab
- Targets can depend on other targets

```
# This is a comment
# This includes another file
include sources.mk
# Variable & Line Continuance
FLAGS = -g
        -Werror \
        -std=c99
# my_file.o target binary
my_file.o: my_file.h my_file.c
    gcc $(FLAGS) -c -o my_file.o my_file.c
# main.o target binary
main.o: my_file.h
   gcc $(FLAGS) -c -o main.o main.c
# Main Target Executable
main.out: main.o my_file.o
   gcc -o main.out main.o my_file.o
```

- Comments start with a #
- Can include other makefiles
- Line continuation is done with a \
- Can create and use variables
- Can have multiple rules
- Command lines start with a tab
- Targets can depend on other targets

```
# This is a comment
# This includes another file
include sources.mk
# Variable & Line Continuance
FLAGS = -g
        -Werror \
        -std=c99
# my_file.o target binary
my_file.o: my_file.h my_file.c
    gcc $(FLAGS) -c -o my_file.o my_file.c
# main.o target binary
main.o: my_file.h
   gcc $(FLAGS) -c -o main.o main.c
# Main Target Executable
main.out: main.o my_file.o
    gcc -o main.out main.o my_file.o
```

### Makefile Variables [S6]

- Variables can be set to strings of text and can include other variables
  - Variable access is done with the \$(variable-name) syntax

### Example Recursively Expanded Variables

CSTD=c89
CPU=cortex-m0plus
CC=arm-none-eabi-gcc

- Recursively Expanded Variables (=)
  - Expands whenever used
- Simply Expanded Variables (:=)
  - Expands once at the time of definition

### Example Simply Expanded Variables

```
ARCH:=$(shell arch)
CWD:=$(shell pwd)
OS:=$(shell uname)
```

Special examples that run Linux commands to set data

- Use variables for things like
  - Compiler flags -> CFLAGS
  - Linker Flags -> LDFLAGS

#### **C-Flags Example Variables**

```
CFLAGS = -g - std = s(CSTD) - mcpu = s(CPU) - mthumb
```

### Include Paths and Sources [S7]

- Can control what directories and source files are used for building
  - Includes provide path to code (absolute or relative paths)
  - Sources determine what needs to be built

- Can reference a variable for include directories and sources files
  - Creates dynamic targets instead of statically defined targets

## Building the Executable [S8]

Use variables in your target rules

```
main.out: main.o my_file.o
    gcc -Wl,map=main.map -I./inc -o main.out main.o my_file.o

$(TARGET): $(OBJS)
    $(CC) $(CFLAGS) $(INCLUDES) $(LDFLAGS) -o $(TARGET) $(OBJS)
```

Automatic Variables - variables in a recipe with a scope

```
$@ - Target $(TARGET): $(OBJS)

$^ - All Prerequisites $(CC) $(CFLAGS) $(LDFLAGS) $(INCLUDES) -o $@ $^
$< - First Prerequisite</pre>
```