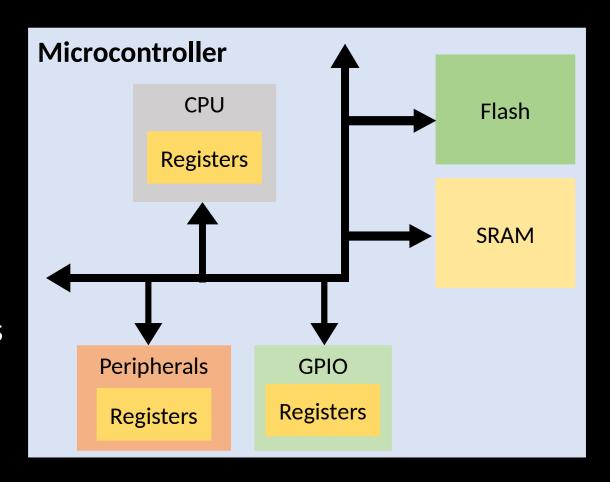
# Memory Alignment

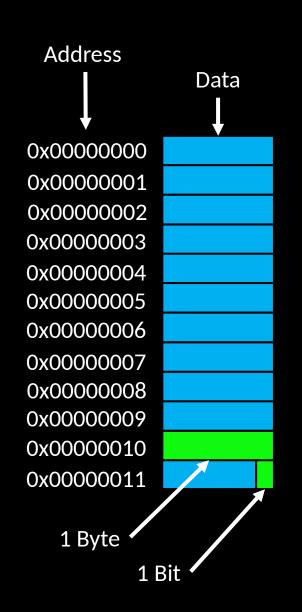
Embedded Software Essentials C2M1V5

#### Memory [S1]

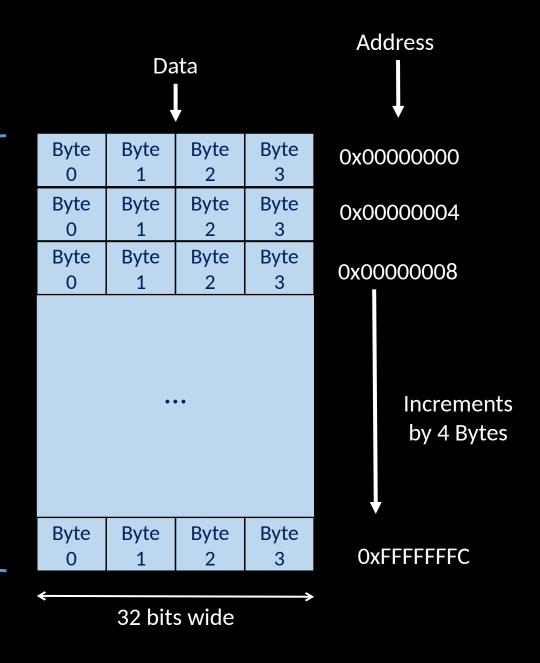
- Memory storage interacting with the CPU
  - Code Memory
  - Data Memory
  - Registers (Peripherals)
- Memory interfaces to CPU through Busses
- Load-Store architecture requires operations to occur in CPU
  - Data gets loaded into CPU
  - Data is operated on
  - Data is stored back



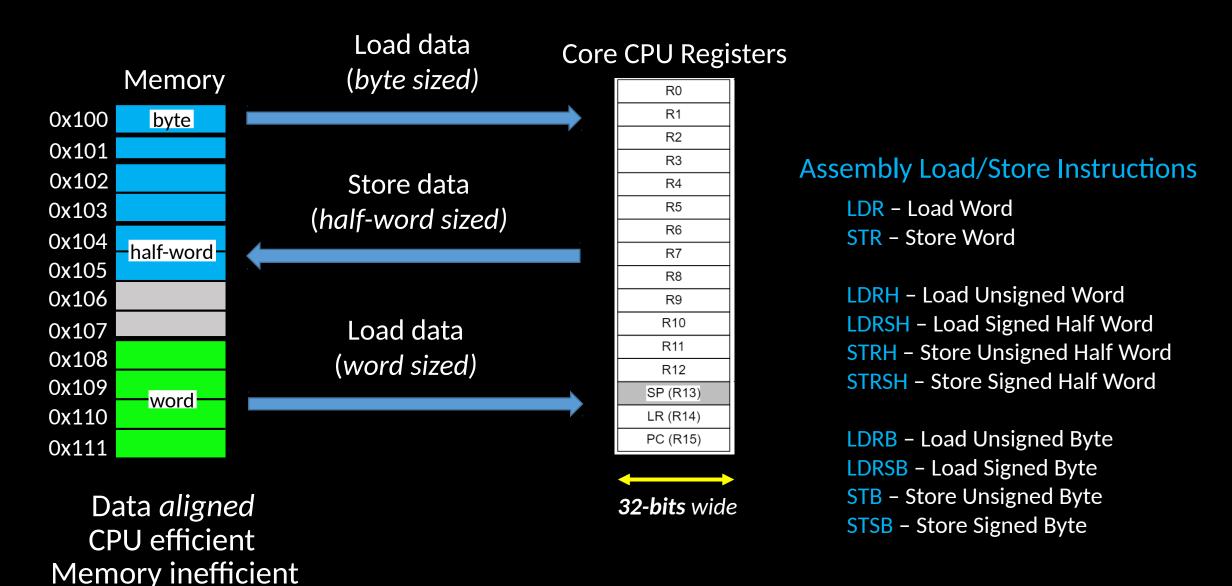
# Memory Model [S2]



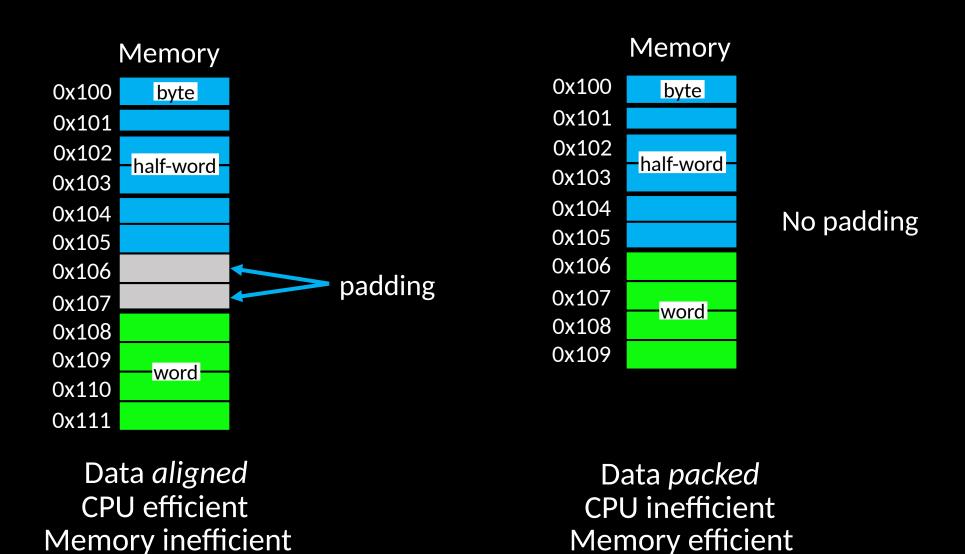




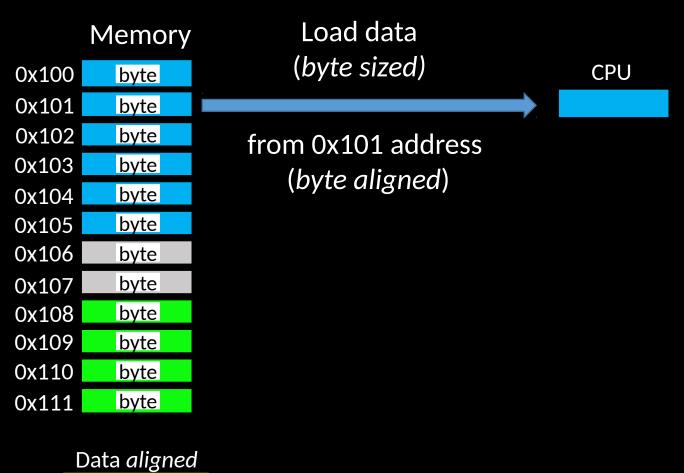
# Memory Organization [S3]



#### Memory Alignment [S4]



#### Byte Load/Stores from Memory [S5]



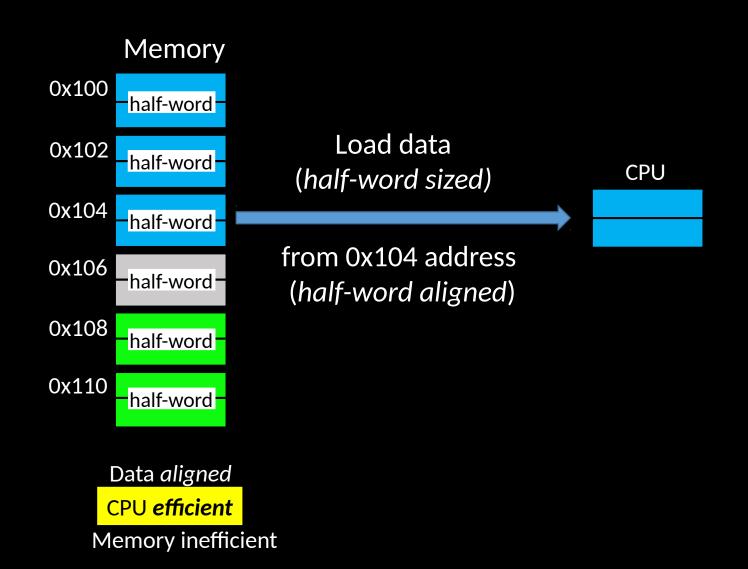
Load/store data occurs only at *aligned addresses* in memory

Data aligned

CPU efficient

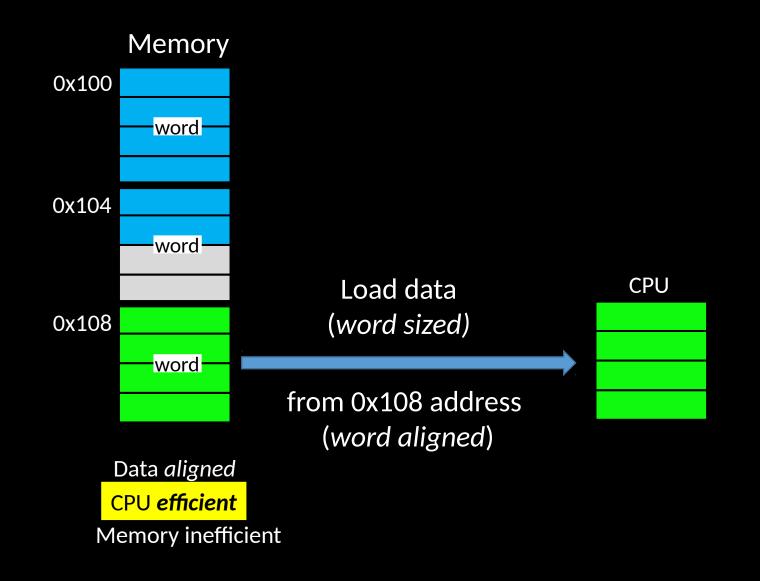
Memory inefficient

#### Half-Word Load/Stores from Memory [S6]



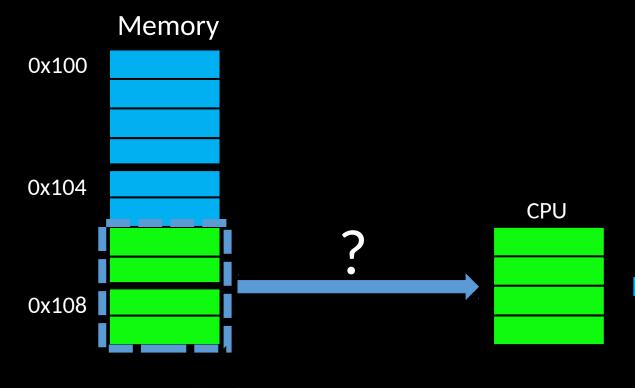
Load/store data occurs only at *aligned addresses* in memory

#### Word Load/Stores from Memory [S7]



Load/store data occurs only at aligned addresses in memory

#### Unaligned Access [S8]

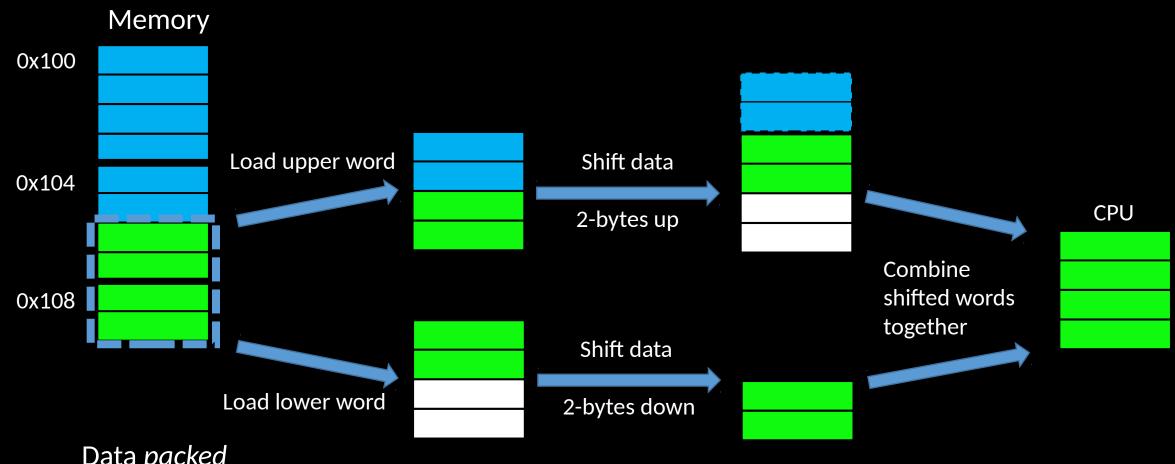


Load/store data occurs only at aligned addresses in memory

How to load **misaligned data?** 

Data *packed*CPU inefficient
Memory efficient

# Unaligned Word Example [S9]



Data packed

**CPU** inefficient

Memory efficient

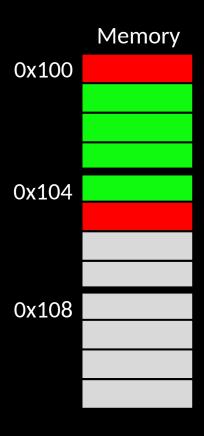
# Struct in Memory [S10a]

```
      Struct struct_name {
      0x104

      char var1;
      0x104

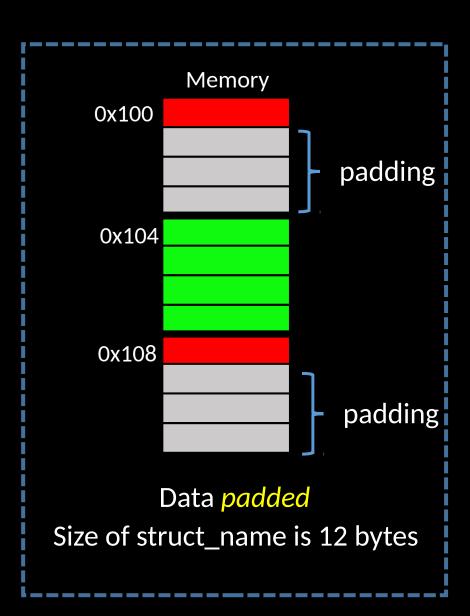
      int var2;
      0x108

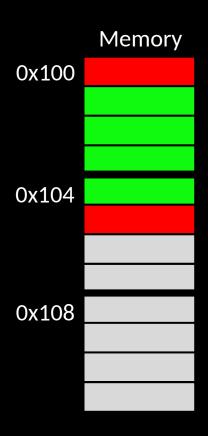
      };
```



# Struct in Memory [S10b]

```
struct struct_name {
  int_fast8_t var1;
  int_fast16_t var2;
  int_fast8_t var3;
};
```





# Struct in Memory [S10c]

