SEMESTER END EXAMINATION, APRIL-MAY, 2025

Course Name: - B Tech **Semester:- IV**

Paper Name: - Computer Organization & Architecture

Paper Code:- TCS 404

Time - 3 Hrs + 20 minutes per hour extra time for V.I. & examinees with writer. **Max Marks-70**

Additional 30 Minutes for Mid-Test.

समय– 3 घण्टे + 20 मिनट प्रति घंटे अतिरिक्त–दृष्टिबाधित एवं सह लेखक परीक्षार्थियों के लिए। अधिकतम अंक–70

30 मिनट अतिरिक्त मिड–टेस्ट के लिए।

Instructions:

- The question paper consists of three sections namely A, B, C. All sections are compulsory.
- Section A- Each question carries **3 mark. All questions are compulsory**.
- Section B- Answer any **5 out of 7** given questions. Each question carries **7 marks**.
- Section C- Answer any **2 out of 3** given questions. Each question carries **10 marks**.
- Section D- Each question carries **02 mark**. All questions are compulsory.

Section – A (खण्ड–अ)

Objective Questions(वस्तुनिष्ठ प्रश्न)

1. Answer all the following questions. 5x3 =15

निम्नलिखित सभी प्रश्न अनिवार्य हैं।

i) What does ISA stand for?

A) Instruction Set Architecture
B) Information Set Architecture
C) Indian Set Architecture
D) None of the above

ii) Which of the architecture is power efficient

A) RISC
B) CISC
C) ISA
D) IANA

iii) The register that contains the instruction to be executed is called.

A) Stack Pointer
B) General Purpose Register
C) Program Counter
D) None of the above

iv) To reduce the memory access time, we generally make use of -

A) ROM
B) RAM
C) Caches
D) None of the above

v) Hardwired control unit is –

A) Faster than microprogrammed control unit
B) Slower than microprogrammed control unit
C) Contains complex programming
D) All of the above

Section – B (खण्ड–ब)

Short Answer Questions (लघुउत्तरीय प्रश्न)

2. Answer any five of the following questions. 5x7=35

निम्नलिखित में से किन्हीं पाँच प्रश्नों के उत्तर दें।

i. What is POST? What is memory hierarchy according to speed and capacity? Explain each level of memory in detail.

ii. Write down about various addressing modes with their suitable explanations of a generic processor (may be 8085).

iii. What are the characteristics of ripple carry adder and carry look ahead adder? Explain with mathematical expressions.

iv. What are the differences between Associative and set Associative mapping. Explain with an example.

v. Explain the concept of pipelining in processor design. What are the advantages and challenges associated with pipelined processors?

vi. Describe the role of caches in a computer system. How does cache organization impact system performance?

vii. Discuss the various types of memory used in computer systems (e.g., RAM, ROM, registers). What are their respective roles and characteristics?

Section – C (खण्ड–स)

Descriptive Questions (विवरणात्मक प्रश्न)

3. Answer any two of the following question. 2x10=20

निम्नलिखित में से किन्हीं दो प्रश्नों के उत्तर दें।

i) Write down the concept of pipelining with suitable diagram. Explain the types of hazards of it.

ii) Explain the differences of hardwired and microprogrammed control unit. Explain the design of a simple hypothetical CPU.

iii) Consider a set-associative cache with 8 sets, each containing 4 cache lines. The main memory consists of 1024 blocks. Calculate:

The size of each cache line in bytes if the cache is byte-addressable.

The total number of cache sets.

The number of bits required for cache index and block offset. (Assume block size is 64B)

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Mid-Test

Course Name:- B. Tech **Semester:-** IVth

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Time - 30 minutes. Max Marks-20

All questions are compulsory. 2×10=20

सभी प्रश्न अनिवार्य हैं।

Objective Questions.

बहुविकल्पीय प्रश्न।

1. What does the term "Von Neumann architecture" refer to?

A) Separate memory for instructions and data

B) Data and instructions stored in the same memory

C) Only data memory

D) Only instruction memory

2. Which register holds the address of the next instruction to be executed?
A) MAR
B) PC
C) IR
D) MDR

3. The ALU is part of the:
A) Control Unit
B) Memory Unit
C) Central Processing Unit
D) Input Unit

4. A CPU can directly access:
A) ROM
B) Cache
C) Hard Disk
D) Floppy Disk

5. What is the function of the control unit in the CPU?
A) Performing calculations
B) Storing data
C) Interpreting instructions
D) Fetching data

6. Which memory is non-volatile and can be electrically erased and reprogrammed?
A) ROM
B) RAM
C) Cache
D) Flash

7. What does RISC stand for?
A) Reduced Instruction Set Computing
B) Random Integrated Signal Controller
C) Rapid Instruction Set Computing
D) Read Instruction Set Controller

8. Pipelining improves:
A) Memory speed
B) Processing power
C) Instruction throughput
D) Instruction latency

9. In which memory type is access time the fastest?
A) RAM
B) Cache
C) Hard Disk
D) ROM

10. Which register is used to store intermediate data in the CPU?
A) PC
B) IR
C) Accumulator
D) MAR

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