EEL2020 Digital Design Lab Report

Sem II AY 2023-24

Experiment No.	:	**01**
Name	:	**Lavangi Parihar**
Roll No.	:	**B22EE044**
Partner Name (Partner Roll No.)	:	**Aastha Bhore (B22EE002)**

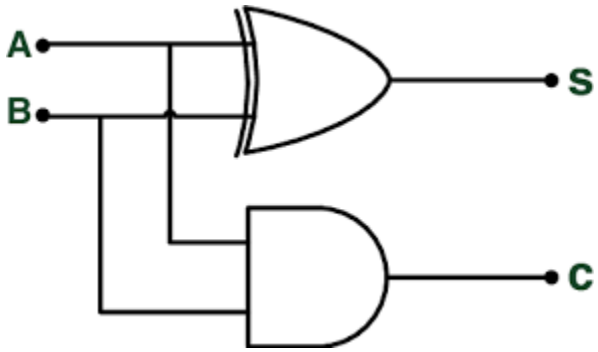
Objective

To implement a half adder using Verilog on the PYNQ Z2 Development Board using the Vivado Design Suite

Logic Design

A Half adder adds two 1-bit binary numbers and produces two outputs: the sum (S) and the carry(C). The logic design for a half adder is based on the truth table ,where the inputs are the binary digits (bits) A and B.

Circuit Diagram



Truth Table:-

Input(a)	Input(b)	Sum(S)	Carry(c)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Logic Expressions:-

1) Sum(S):- The sum is obtained from the XOR operation of A and B
2) Carry(C):- The carry is obtained from the AND operation of A and B C=A.B

Verilog Representation:-

```
module half_adder(input a,b,output s,c);
        assign s=a^b;
         assign c=a&b;
endmodule
```

Source Description

Design Source:- Verilog(or VHDL) files containing the logic description of the implemented circuit.
Constraint file (XDC):- Specifies pin assignments, I/O standards, and timing constraints for the FPGA

- Design source

Module name: half_adder.v Input ports: a, b; Output ports: s, c

- Constraint file

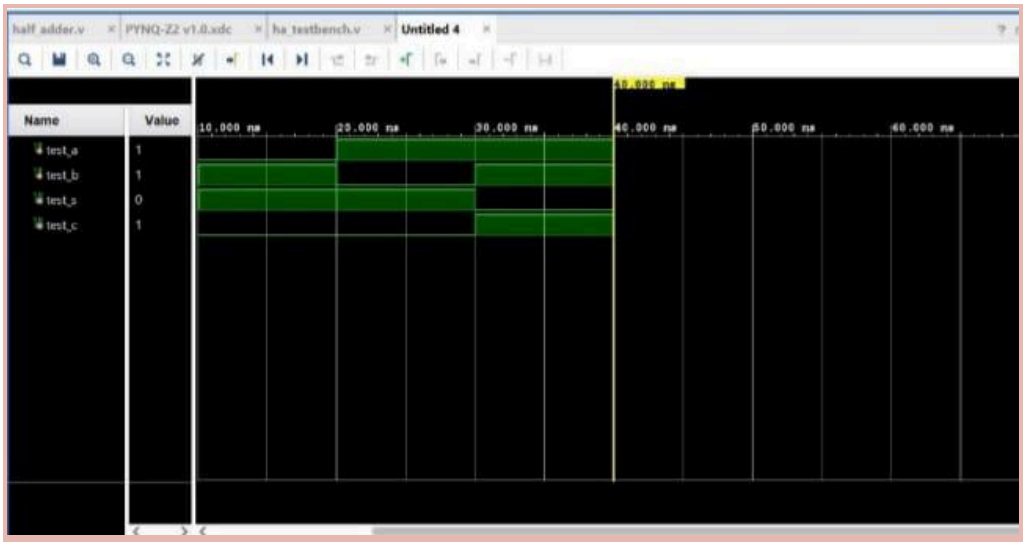
The XDC file was updated with the following changes:

Ports (from Verilog module)	**Designation** (Input/Output)	PYNQ Component Type (Button/LED/Switch etc. along with number, eg. LD01, BTN2, etc.)	Pin Configuration (from the PYNQ User Manual)
a	input	SW0	M20
b	input	SW1	M19
s	output	LED1	R14
c	output	LED0	P14

- **Simulation source** **(if any)**

Testbench for ab = 00, 01, 10, 11 has been included in the design source itself. OR Testbench for ab = 00, 01, 10, 11 has been included as a simulation source.

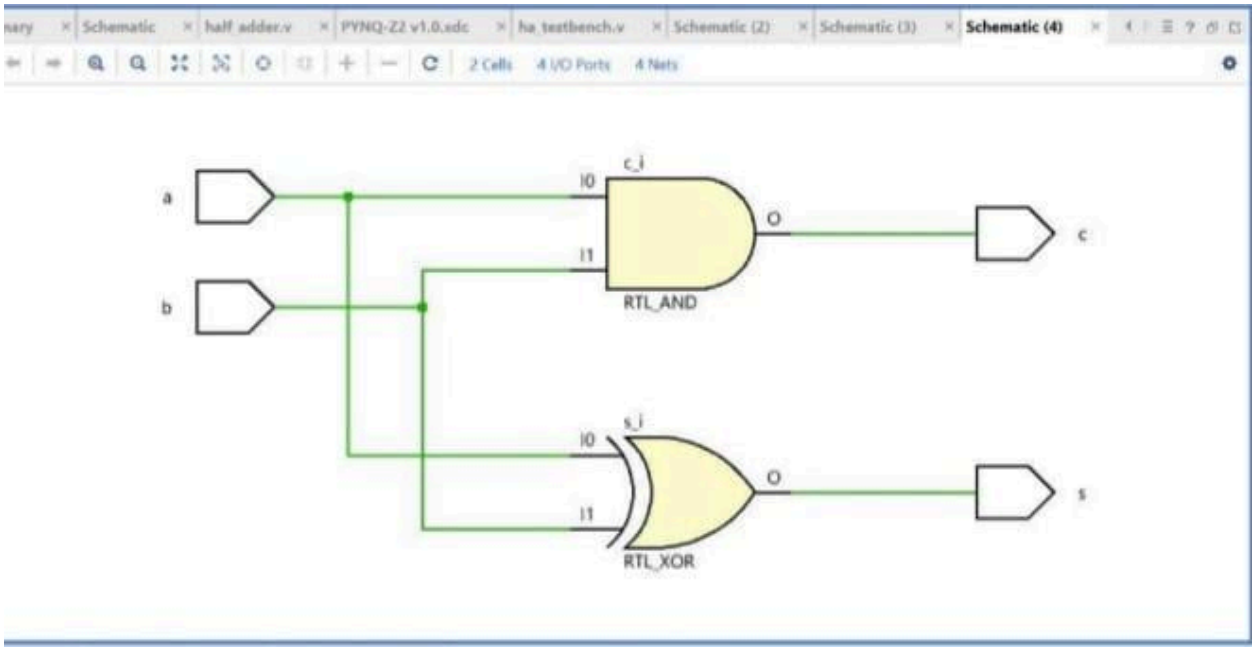
Simulation Results **(Timing diagram)**



For Half Adder

Expected Truth Table				**From the Timing Diagram**			
a	***b***	***s***	***c***	***a***	***b***	***s***	***c***
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0	**1**	**1**	**0**	**1**	**1**	**1**	**0**
1	**0**	**1**	**0**	**1**	**0**	**1**	**0**
1	**1**	**0**	**1**	**0**	**1**	**0**	**1**

Elaborated Design



The design in Vivado matches the planned half-adder circuit.it correctly uses the XOR gate for sum(S) and the AND gate for carry(C).the connections follows the Verilog code,ensuring the circuit operates as expected .this verification aligns with the truth table,confirming the accuracy of the design

PYNQ Working Video (to be recorded during lab session)
(with voiceover briefly explaining the working, not exceeding 1-2 minutes)
Video: Link