EEL2020 Digital Design Lab Report

Sem II AY 2023-24

Experiment No.	:	**3**
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Objective

Simulate and implement the 4-bit adder on the PYNQ Z2 board and display the 2-digit decimal sum on two seven-segment displays.

Source Description

New code to convert binary to decimal and extracting tens and ones digits:

```
module BinaryToDecimal(input [4:0] binary, output reg [4:0] decimal, output reg [3:0] dec_tens, output reg [3:0] dec_ones);
  integer i;
  integer power;
  integer tens_digit;
  integer ones_digit;

  always @(*)
    begin
      decimal = 5'b00000;
      for( i=0 ; i<5 ; i=i+1 )
        begin
          power = 2**i ;
          decimal = decimal + (binary[i]*power);
        end
      tens_digit = decimal / 10;
      ones_digit = decimal % 10;
    end

  always @(*)
    begin
      dec_tens = 4'b0000;
```

```
        dec_ones = 4'b0000;
        for ( i=3 ; i>=0 ; i=i-1)
          begin
            if( tens_digit>=(2**i) )
              begin
                dec_tens[i] = 1;
                tens_digit = tens_digit-(2**i) ;
              end
            if( ones_digit>=(2**i) )
              begin
                dec_ones[i] = 1;
                ones_digit = ones_digit-(2**i) ;
              end
          end
    end

endmodule
```

- Constraint file

The XDC file was updated with the following changes:

Ports (from Verilog module)	Designation (Input/Output)	PYNQ Component Type (Button/LED/Switch etc. along with number, e.g. LD01, BTN2, etc.)	Pin Configuration (from the PYNQ User Manual)
SSD_ones [0]	Output	JA1_P	Y18
SSD_ones [1]	Output	JA1_N	Y19
SSD_ones [2]	Output	JA2_P	Y16
SSD_ones [3]	Output	JA2_N	Y17
SSD_ones [4]	Output	JA3_P	U18
SSD_ones [5]	Output	JA3_N	U19

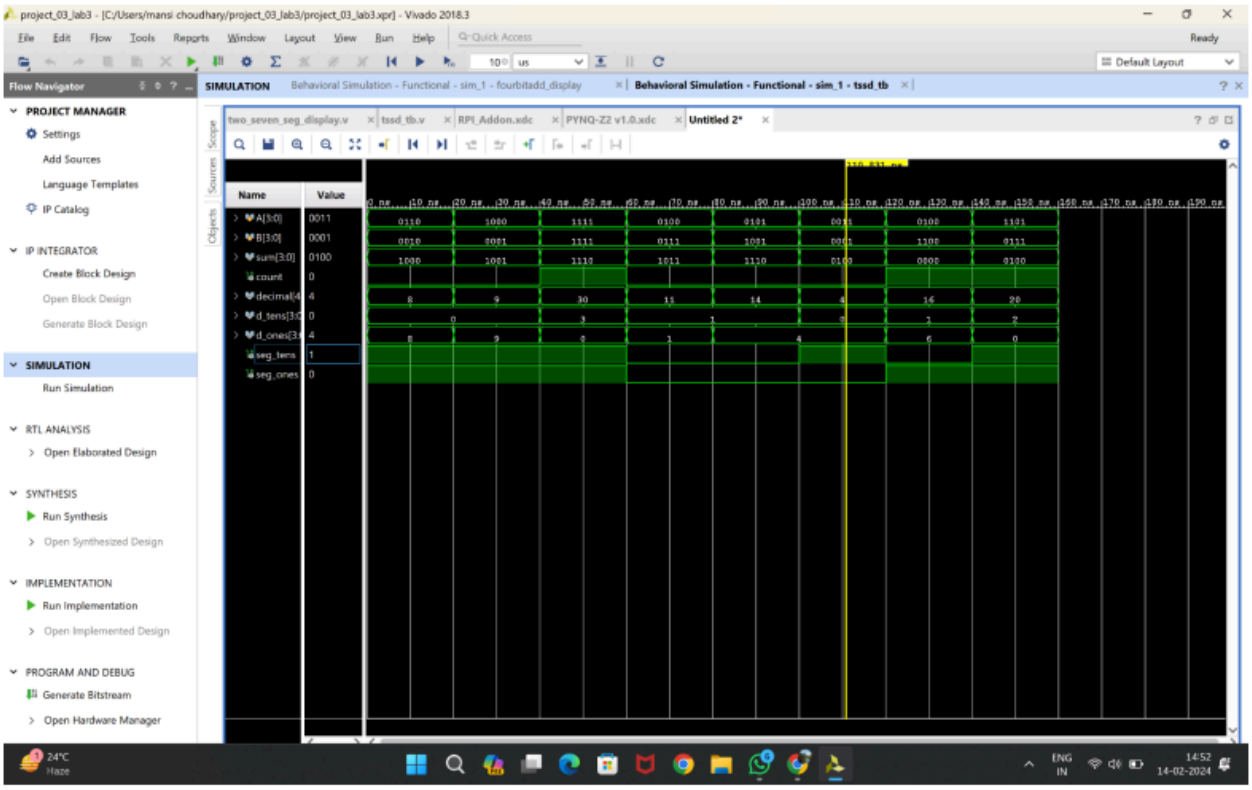
SSD_ones [6]	Output	JA4_P	W18
SSD_tens [0]	Output	JB1_P	W14
SSD_tens [1]	Output	JB1_N	Y14
SSD_tens [2]	Output	JB2_P	T11
SSD_tens [3]	Output	JB2_N	T10
SSD_tens [4]	Output	JB3_P	V16
SSD_tens [5]	Output	JB3_N	W16
SSD_tens [6]	Output	JB4_P	V12

The RPI file was updated with the following changes:

Ports	**Designation**	**Component Type**	**Pin configuration**
B [0]	input	get_ports (SWA)	V6
B [1]	input	get_ports (SWB)	Y6
B [2]	input	get_ports (SWC)	B19
B [3]	input	get_ports (SWD)	U7
A [0]	input	get_ports (SWE)	C20
A [1]	input	get_ports (SWF)	Y8
A [2]	input	get_ports (SWG)	A20
A [3]	input	get_ports (SWH)	W9

- Simulation source (if any)
Testbench includes: - Time = 20ns 6 different values for both A and B

Simulation Results (Timing diagram)



Expected Truth Table				From the Timing Diagram			
A	B	d_tens	d_ones	A	B	d_tens	d_ones
0110	0010	0	8	0110	0010	0	8
1000	0001	0	9	1000	0001	0	9
1111	1111	3	0	1111	1111	3	0
0100	0111	1	1	0100	0111	1	1
0101	1001	1	4	0101	1001	1	4
0100	1100	1	6	0100	1100	1	6
0011	0001	0	4	0011	0001	0	4
1101	0111	2	0	1101	0111	2	0

PYNQ Working Video (to be recorded during lab session)
(with voiceover briefly explaining the working, not exceeding 1-2 minutes)
video link

List of Attachments
Both XDC files, Testbench code and Module code
Lab3.zip