Experiment 04

Objectives

Simulate and implement a BCD Adder/Subtractor circuit.

The selection of addition/subtraction operation should be done by another input. The sign (in case of subtraction) and carry (in case of addition) should be shown on an LED, while the BCD difference or sum should be shown on a 7-segment display. You may use Verilog operators of addition and subtraction.

Apparatus

Vivado Design Suite, PYNQ Z2 board, Breadboard, one 7-segment display, RPI module, jumper cables

Procedure

Note that the maximum value of BCD addition of two BCD numbers can be 18, and the minimum value of subtraction of two BCD numbers can be −9.

A. Verilog modules

Refer to the module hierarchical structure shown in Fig. 1.

Step 1: Allow the program to proceed only for valid 4-bit BCD inputs, *A* and *B*. For the selection variable *M*, allow subtraction when *M* = 1 and addition when *M* = 0. Represent the output of the program in terms of status of LED (*Carry/Sign*) and 7-bit SSD combination (SSD).

Step 2: If *M* = 1, perform BCD subtraction as follows:

If $A \geq B$, the difference will be positive or zero. Hence, assign *Sign* = 0 (for positive), and difference $(D) = A - B$.

If $A < B$, the difference will be negative. Hence, assign *Sign* = 1 (for positive), and difference $(D) = B - A$.

If *M* = 0, perform BCD addition as follows:

If $A + B \leq 9$, the sum is a valid BCD and there is no Carry. Set $S = A + B$ and *Carry* = 0.

If $A + B > 9$, the BCD sum representation is equivalent to having a carry with an excess-6 binary sum. Set $S = A + B + 0110$ and $C = 1$.

Step 3: Convert the sum or difference from BCD to a seven-segment display pattern.

Step 4: Create a testbench with at least three additions and three subtractions. Show mixed combinations of negative subtractions and carry-out additions.

Insert the timing diagram (simulation results) in your report.

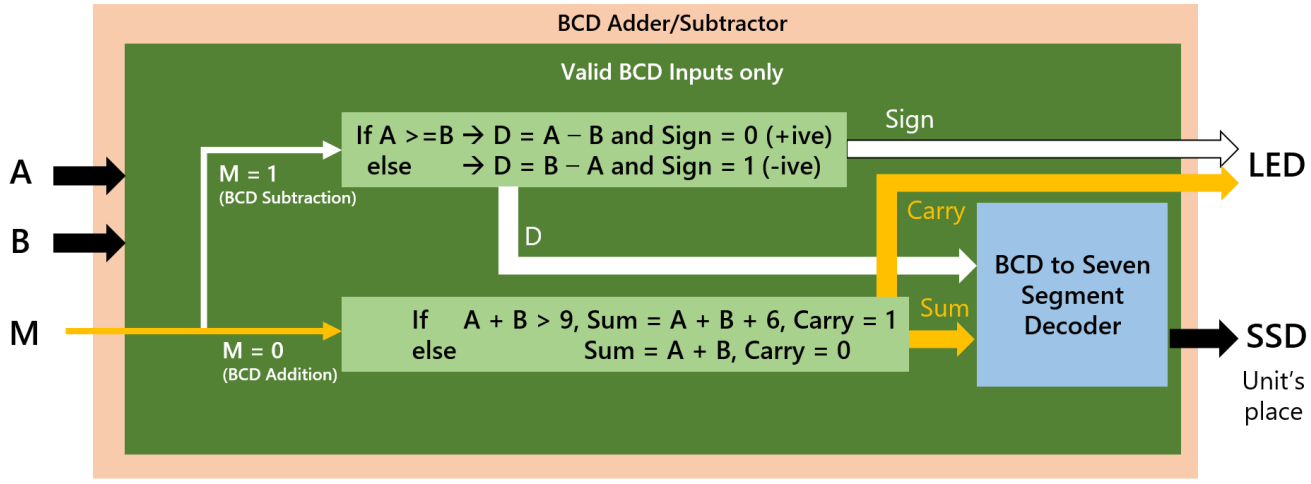

Figure 1 Module structure

B. Circuit

Refer to Fig. 2 for the circuit of the design.

Step 1: Use the slide switches on the RPI module to provide the 4-bit inputs, *A* and *B* (as shown in Fig. 2). Use the slide switch (eg. SW1) on the PYNQ Z2 board to select the mode of operation (*M*) (*M* = 1 implies BCD subtraction, *M* = 0 implies BCD addition).

Step 2: Use Pmod B to connect the seven-segment display, corresponding to the the unit's place. (Refer to the pin configuration of the Pmod and SSD from Experiment 2). Use the LED, eg. LD0, on the PYNQ Z2 board to represent the carry/sum.

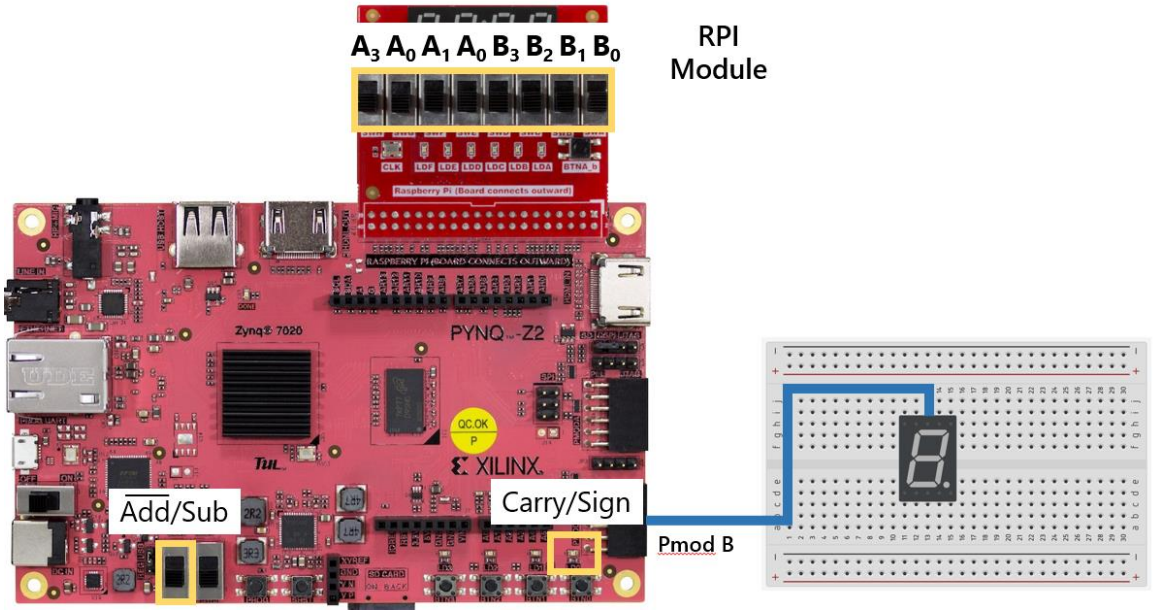

Figure 2 Circuit Schematic of the connections

Step 3: Update the **input** ports on the Constraint files:

XDC file of the RPI module: 08 switches {SWH, SWG, SWF, SWE} = $A_3A_2A_1A_0$ and {SWD, SWC, SWB, SWA} = $B_3B_2B_1B_0$.

XDC file of the PYNQ Z2 board: slide switch (SW1) = *M*

Step 4: Update the **output** ports on the Constraint files:

XDC file of the PYNQ Z2 board: LED (*LD*0) = *Carry/Sign* and Pmod Pins {1, 2, 3, 4, 7, 8, 9} = Seven-segment Pattern {abcdefg} (Refer to the pin diagrams from previous manuals).

Step 4: Generate the bitstream and program the device with the generated stream.

Step 5: Verify the display with all combinations of inputs.

Record the video showing the input/output ports and seven segment outputs for at least ten combinations of inputs from both addition and subtraction operation.

Online Reference

R. Chouhan, *BCD Adder/Subtractor* (https://youtu.be/vGZX1VUhhNY)