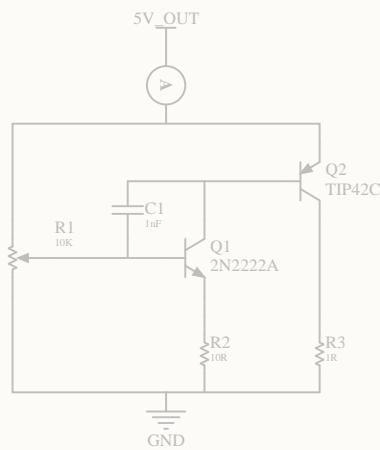
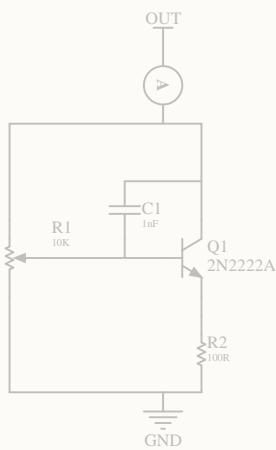


ADJUSTABLE HIGH CURRENT LOAD

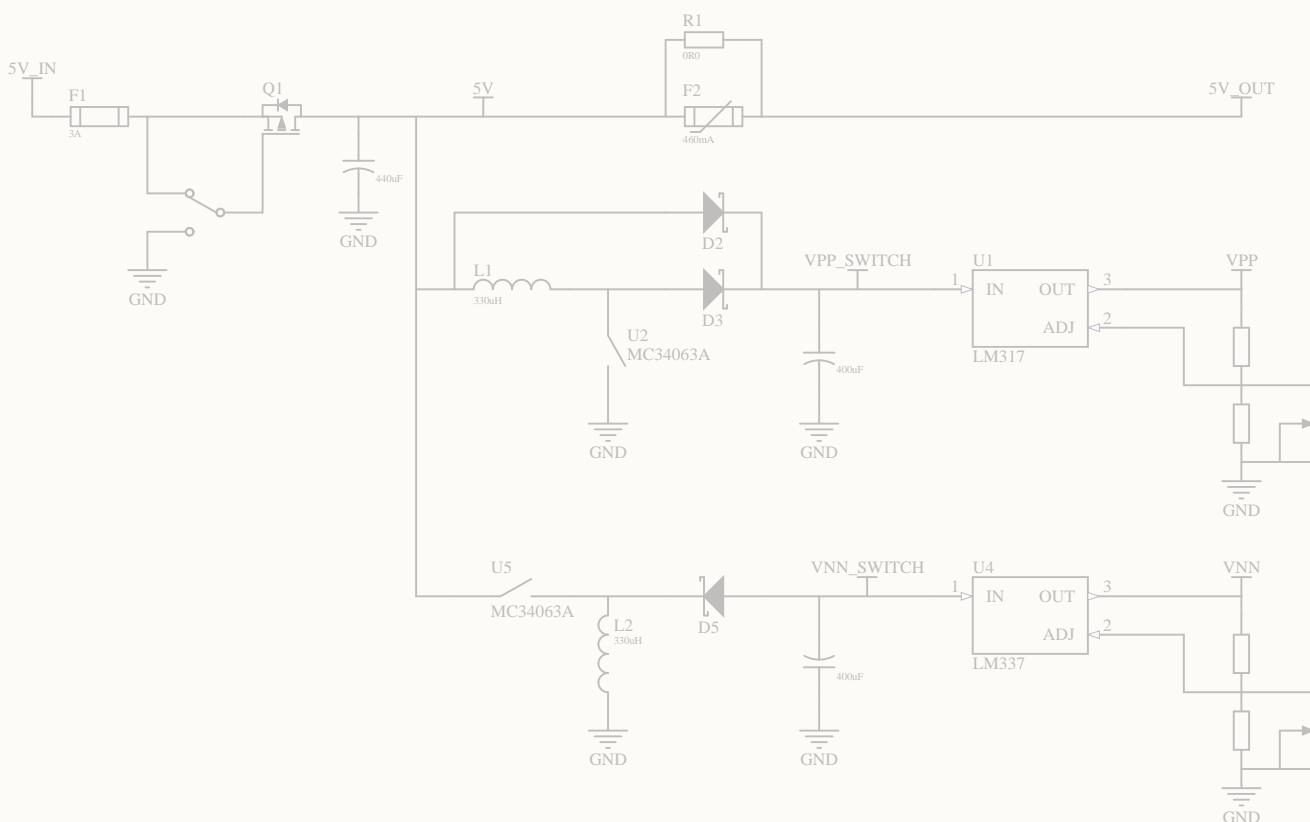


ADJUSTABLE CURRENT LOAD



Illustrations 3			University of Cape Town
Size: A4	Number: 1	Revision: v4.3	Department of Electrical Engineering
Date: 2021/11/27	Time: 14:57:45	Sheet 1 of 1	Rondebosch Cape Town South Africa 7701
File: Illustrations 3.SchDoc		Author: LD Stanton	

A



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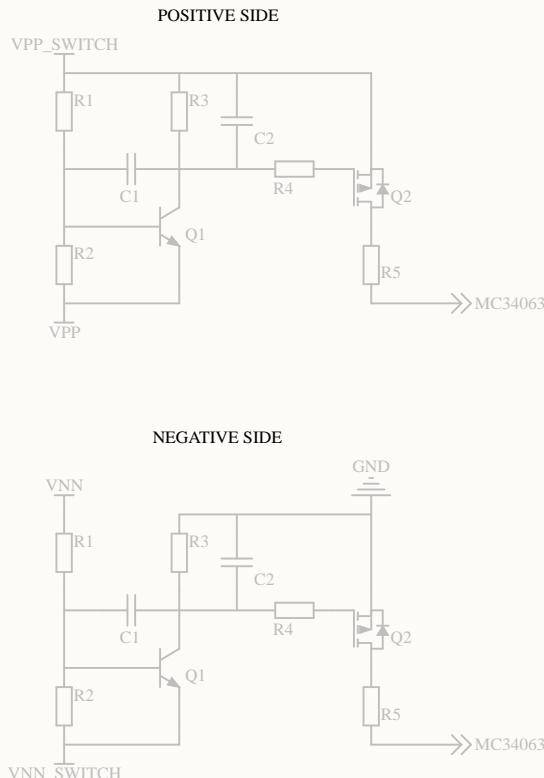
C

D

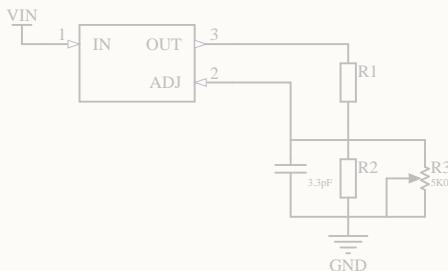
Functional Diagram

Size: A4	Number: 2	Revision: v4.3
Date: 2021/11/27	Time: 14:57:45	Sheet 2 of 4
File: Functional Diagram.SchDoc	Author: LD Stanton	University of Cape Town Department of Electrical Engineering Rondebosch Cape Town South Africa 7701

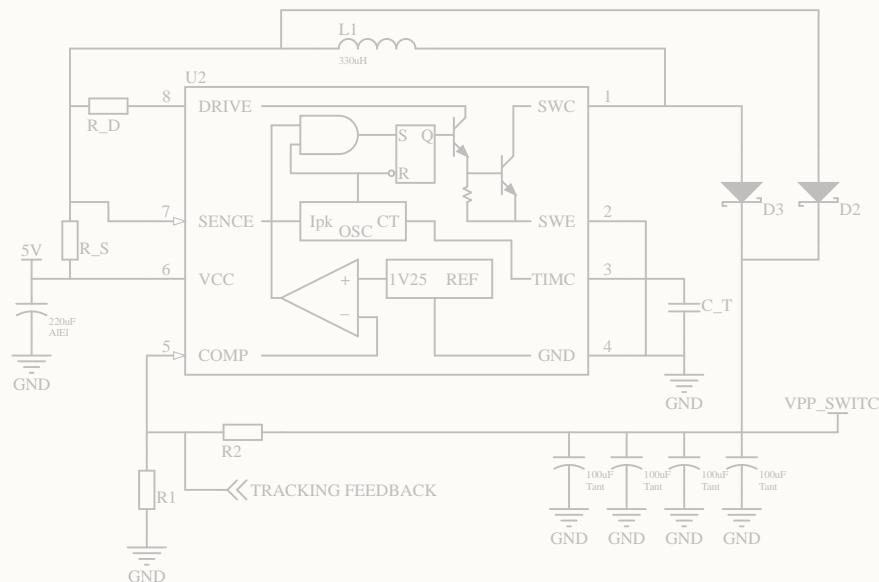
VOLTAGE FOLLOWING FEEDBACK



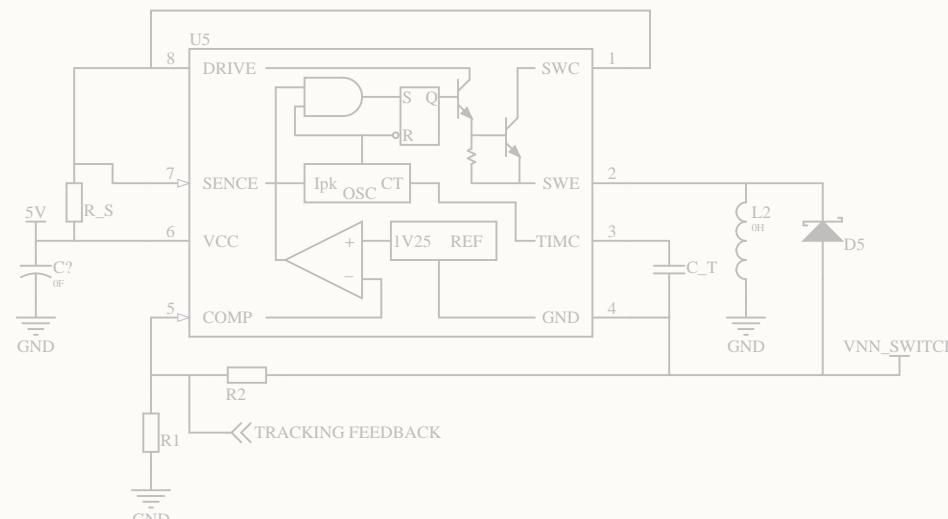
LINEAR REGULATOR FEEDBACK



BOOSTING REGULATOR



INVERTING REGULATOR

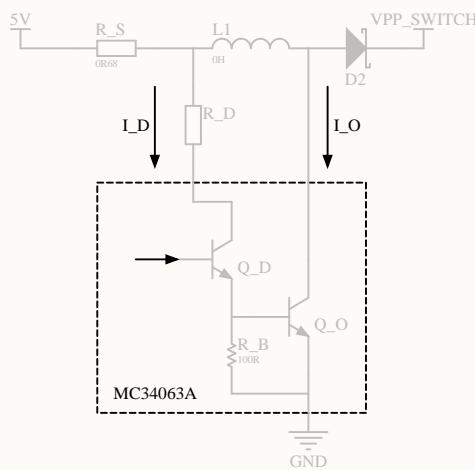


Illustrations 1

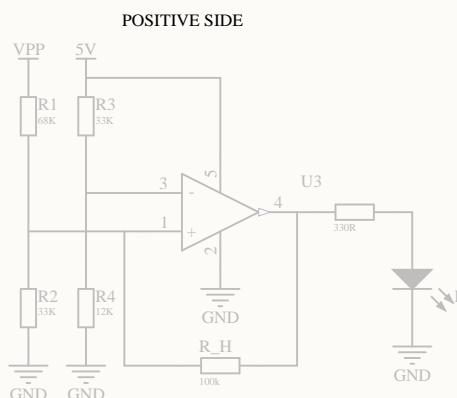
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Date: 2021/11/27	Time: 14:57:45	Sheet 3 of 4
File: Illustrations 1.SchDoc		Author: LD Stanton



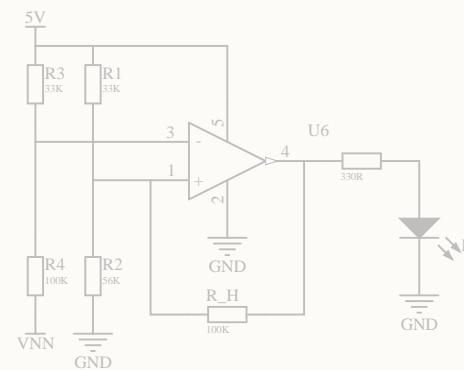
FORCED GAIN



LED HYSTERESIS



NEGATIVE SIDE



Illustrations 2

Size: A4	Number: 3	Revision: v4.3
Date: 2021/11/27	Time: 14:57:45	Sheet 4 of 4
File: Illustrations 2.SchDoc	Author: LD Stanton	



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E

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RELEASE HISTORY

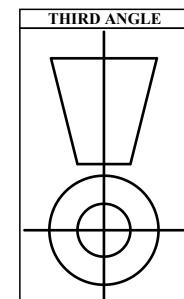
REVISION	DESCRIPTION	DATE
v1.0	Initial Prototype	09/04/2021
v2.0	Second Prototype	07/06/2021
v3.0	Design Candidate	05/08/2021
v4.3	Final Design	10/12/2021

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Item	Page
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Layer Stack Legend	2
Region Map	3
Transmission Line Table	4
Drill Table	4
Drill Drawing	5
Layer Views	6

Board Fabrication Statistics

Item	Value
Board Height	63.50mm
Board Width	50.00mm
Board Area	3171.61sq.mm
Net Count	50
Pad Count	304
Hole Count	131
Via Count	56
Slot Hole Count	10



APPROVALS	DATE
ENGINEER: LD STANTON	10/12/2021
CHECKER: JC Pead	--/-/----

REFERENCE DOCUMENTS

BOM DOC: Bill of Materials.csv

CPL DOC: Pick and Place.csv

ASM DOC: Assembly.PCDBdwf

SCH DOC: Main.SchDoc

PCB DOC: PCB.PcbDoc

UNIVERSITY OF CAPE TOWN
DEPARTMENT OF ELECTRICAL ENGINEERING
CAPE TOWN
SOUTH AFRICA
7701

CONTACT: LAWRENCE STANTON JUSTIN PEAD
STNLAW003@myuct.ac.za justin.pead@uct.ac.za

TITLE:

SIO2MKR

USB Split Rail Power Supply for Breadboards

VARIANT: [No Variations] REVISION v4.3 2021/12/10

SIZE:
A4

DWG:

FABRICATION

SCALE: 5:2

FILE: Fabrication.PCDBdwf

SHEET 1 OF 11

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Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.03mm	SM-001	Solder Mask	GTS
Lead-Free	Top Surface Finish	0.02mm		Surface Finish	
CF-004	Top Layer	0.04mm		Signal	GTL
	<i>Core</i>		<i>FR-4</i>	<i>Dielectric</i>	
CF-004	Bottom Layer	0.04mm		Signal	GBL
Lead-Free	Bottom Surface Finish	0.02mm		Surface Finish	
Surface Material	Bottom Solder	0.03mm	SM-001	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
Total thickness: 1.60mm					

A

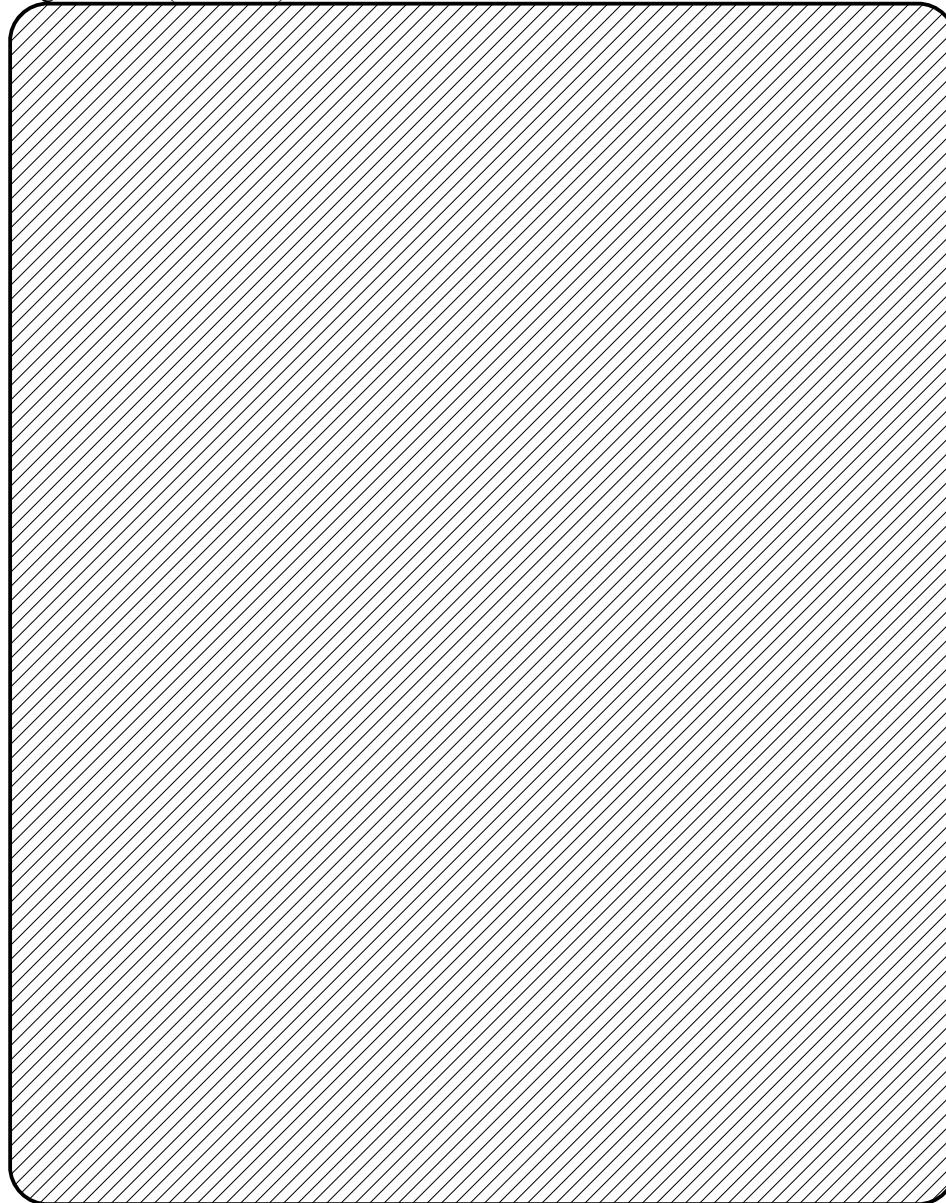
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Region View (Scale 5:2)



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SIZE:	A4	DWG:	FABRICATION	
SCALE:	5:2	FILE:	Fabrication.PCBDwf	SHEET 3 OF 11

A

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Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via / Pad	Pad Shape	Hole Tolerance	Hole Length
◇	49	0.50mm(20mil)	Plated	Round	Top Layer - Bottom Layer	Via		+0.13mm(5mil)/-0.08mm(3mil)	
▽	4	0.60mm(24mil)	Plated	Slot	Top Layer - Bottom Layer	Pad	Rounded		1.30mm(51mil)
○	2	0.70mm(28mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded		
□	10	0.79mm(31mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded		
◎	3	0.80mm(31mil)	Plated	Round	Top Layer - Bottom Layer	Pad	(Mixed)		
❖	8	0.80mm(31mil)	Plated	Round	Top Layer - Bottom Layer	(Mixed)	(Mixed)	+0.13mm(5mil)/-0.08mm(3mil)	
▣	20	0.90mm(35mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded	+0.13mm(5mil)/-0.08mm(3mil)	
▼	22	0.90mm(35mil)	Plated	(Mixed)	Top Layer - Bottom Layer	Pad	Rounded		(Mixed)
¤	3	0.91mm(36mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded		
☒	6	1.10mm(43mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded	+0.13mm(5mil)/-0.08mm(3mil)	
☒	5	1.15mm(45mil)	Non-Plated	Round	Top Layer - Bottom Layer	Pad	Rounded	+0.13mm(5mil)/-0.08mm(3mil)	
✚	5	1.20mm(47mil)	Plated	Round	Top Layer - Bottom Layer	Pad	Rounded	+0.13mm(5mil)/-0.08mm(3mil)	
☒	4	1.80mm(71mil)	Plated	Slot	Top Layer - Bottom Layer	Pad	Rounded	+0.13mm(5mil)/-0.08mm(3mil)	2.20mm(87mil)
141 Total									

A B C D E

Drill Drawing View (Scale 5:2)

1

1

2

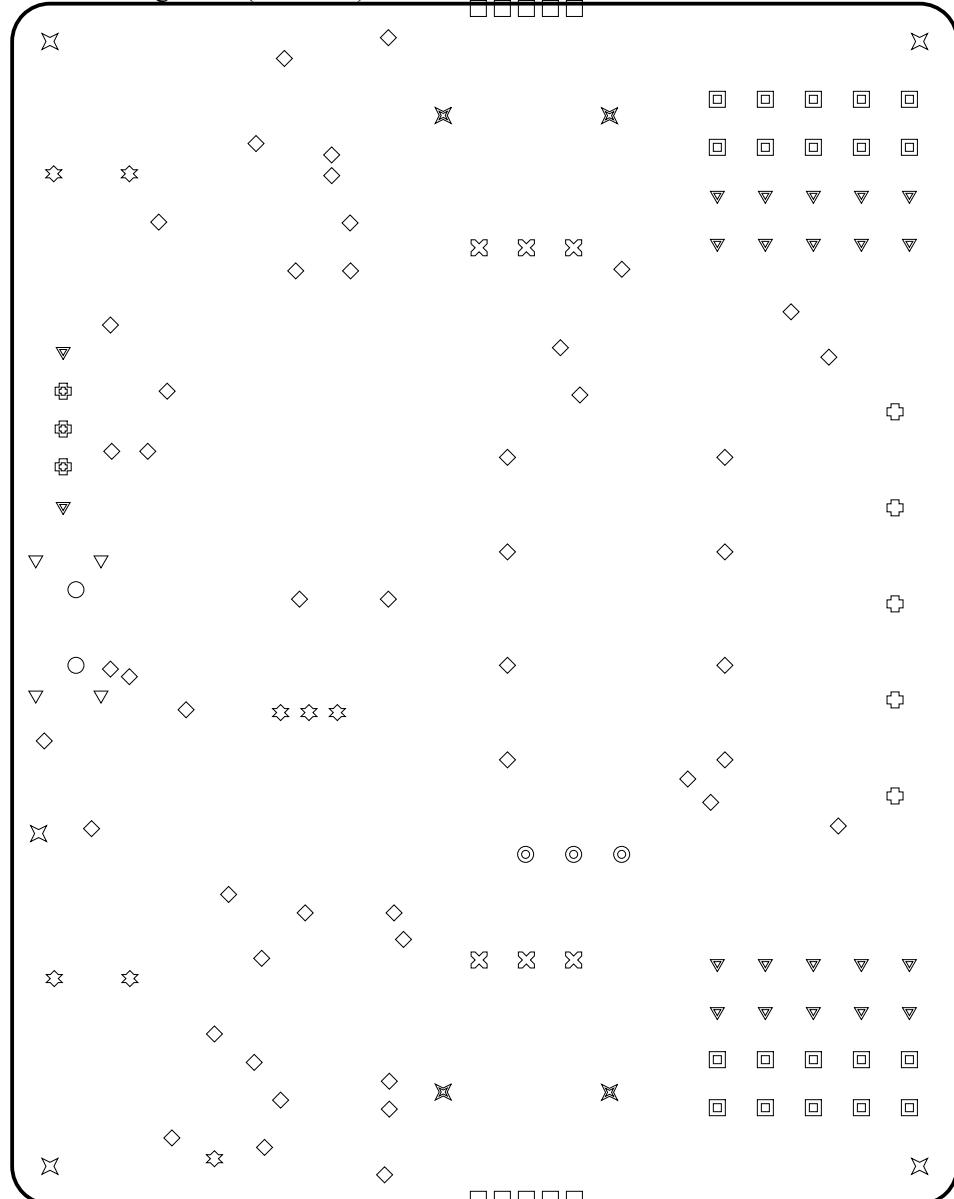
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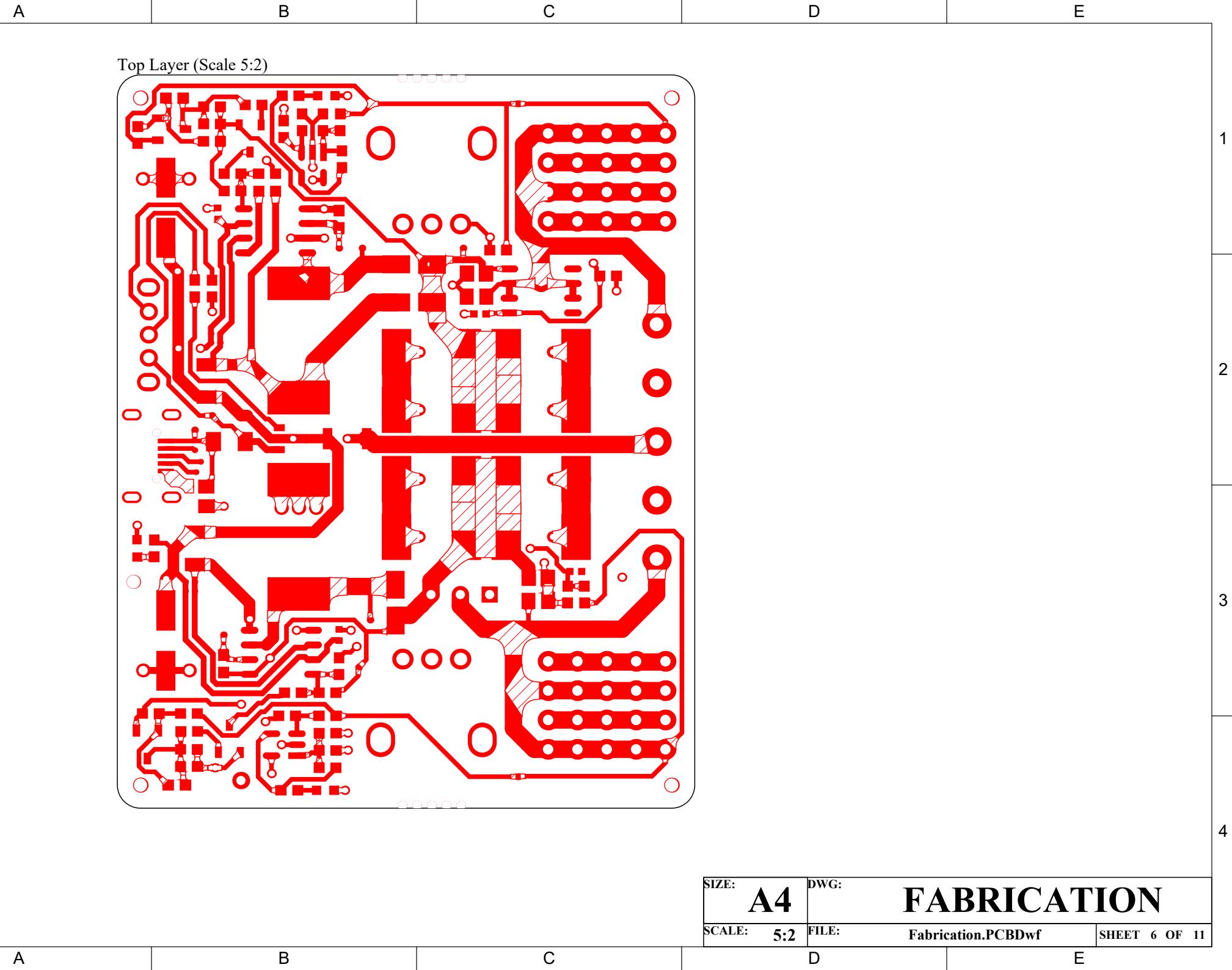
4

4



SIZE:	A4	DWG:	FABRICATION	
SCALE:	5:2	FILE:	Fabrication.PCBDwf	SHEET 5 OF 11

A B C D E



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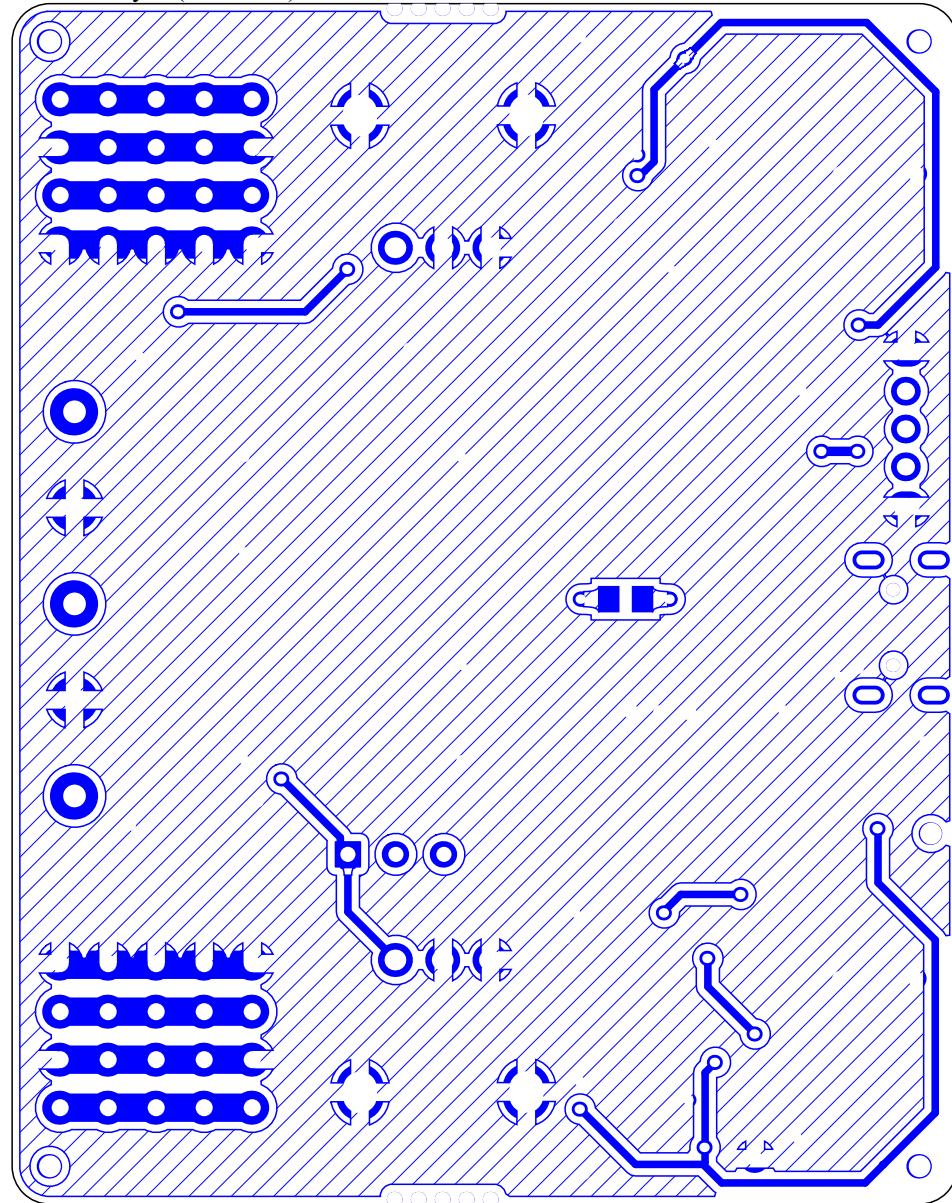
B

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Bottom Layer (Scale 5:2)



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SIZE:
A4

DWG:

FABRICATION

SCALE: 5:2

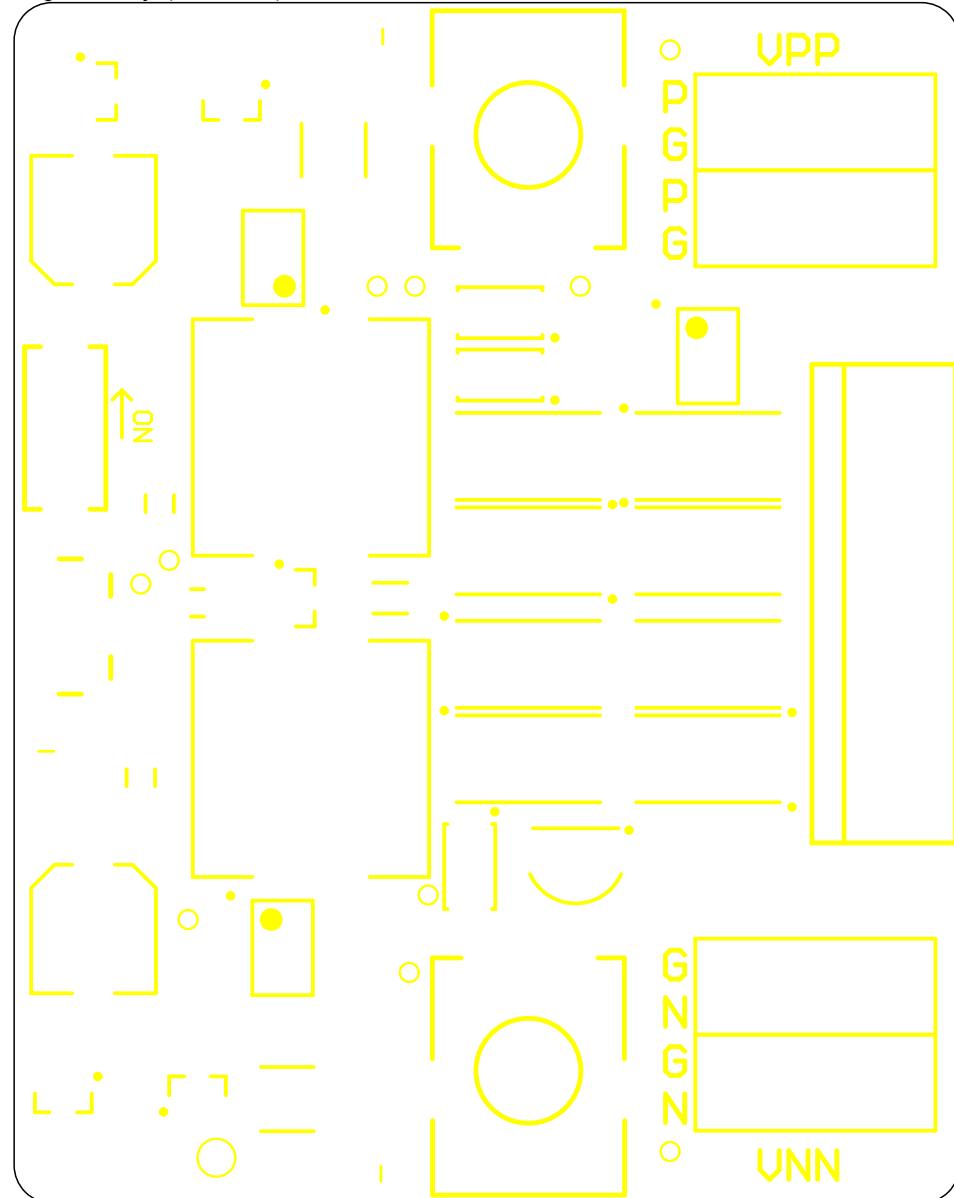
FILE:

Fabrication.PCDBdwf

SHEET 7 OF 11

A B C D E

Top Overlay (Scale 5:2)



A B C D E

SIZE:	A4	DWG:	FABRICATION		
SCALE:	5:2	FILE:	Fabrication.PCDBdwf	SHEET	8 OF 11

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E

Bottom Overlay (Scale 5:2)

SOLDER 1 ONLY



STO2MKR v4.3

USB SPLIT RAIL PSU



LD STANTON NOVEMBER 2021

GITHUB.COM/LAWRENCESTANTON/

SPECIFICATIONS

	MIN	TYP	MAX
USB P	4.6V	5.0V	5.6V
USB U	5W	5W	5W
REG I	1V2	10V5	10V5
REG I (5V)	40mA	0A46	0A46

(C) UCT 2021
UPP GND 5V GND UNN

SOLDER 1 ONLY

SIZE:
A4

DWG:

FABRICATIONSCALE:
5:2

FILE:

Fabrication.PCDBdwf

SHEET 9 OF 11

A

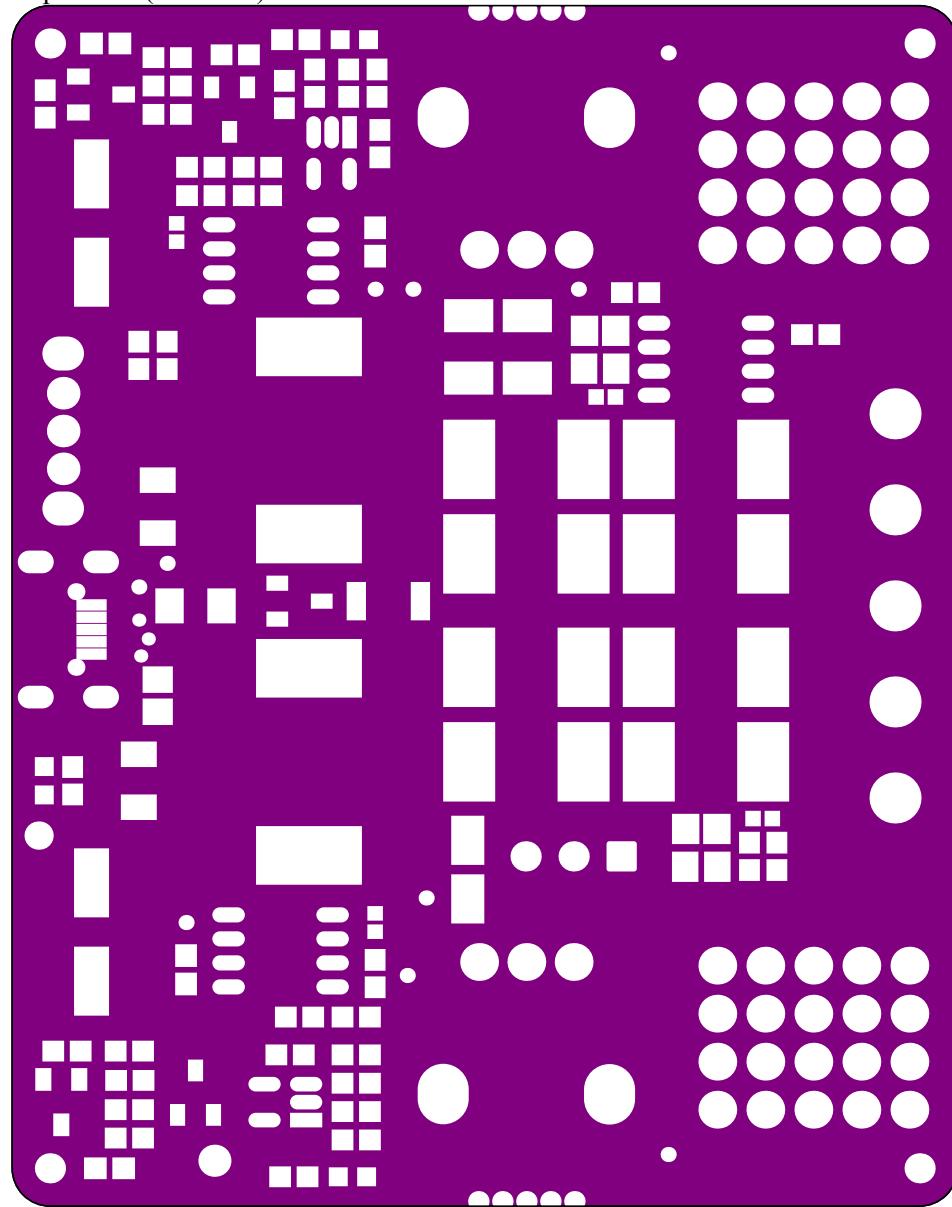
B

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D

E

Top Solder (Scale 5:2)



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SIZE:
A4

DWG:

FABRICATION

SCALE: 5:2

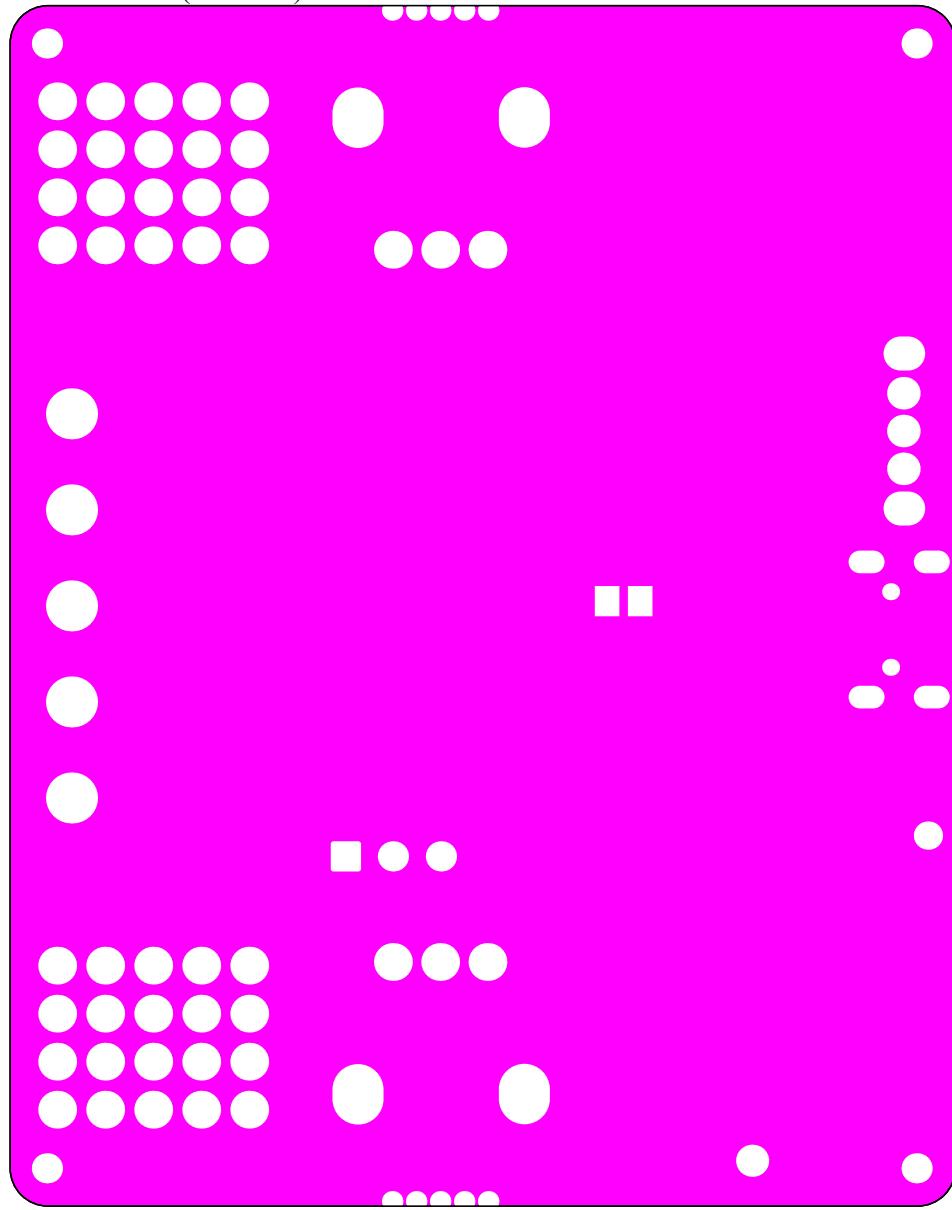
FILE:

Fabrication.PCBDwf

SHEET 10 OF 11

A B C D E

Bottom Solder (Scale 5:2)



1
2
3
4

1
2
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4

A B C D E

SIZE: A4 DWG: **FABRICATION**
SCALE: 5:2 FILE: Fabrication.PCBDwf SHEET 11 OF 11

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RELEASE HISTORY

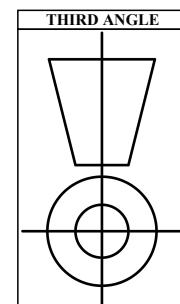
REVISION	DESCRIPTION	DATE
v1.0	Initial Prototype	09/04/2021
v2.0	Second Prototype	07/06/2021
v3.0	Design Candidate	05/08/2021
v4.3	Final Design	27/11/2021

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Component Placement Bottom Side	6
Bill of Materials	7

Board Assembly Statistics

Item	Value
Board Height	63.50mm
Board Width	50.00mm
Board Area	3171.61sq.mm
Component Count	109
Board Density	35%
Net Count	50
Pad Count	304



APPROVALS ENGINEER: LD STANTON DATE: 27/11/2021 CHECKER: JC Pead ---/---/---	UNIVERSITY OF CAPE TOWN DEPARTMENT OF ELECTRICAL ENGINEERING CAPE TOWN SOUTH AFRICA 7701	CONTACT: LAWRENCE STANTON STNLAW003@myuct.ac.za ALTERNATIVE: JUSTIN PEAD justin.pead@uct.ac.za
REFERENCE DOCUMENTS BOM DOC: Bill of Materials.csv	TITLE: SIO2MKR	
CPL DOC: Pick and Place.csv FAB DOC: Fabrication.PCDBdwf SCH DOC: Main.SchDoc	VARIANT: [No Variations]	REVISION: v4.3 2021/12/10
PCB DOC: PCB.PcbDoc	SIZE: A4 DWG:	ASSEMBLY
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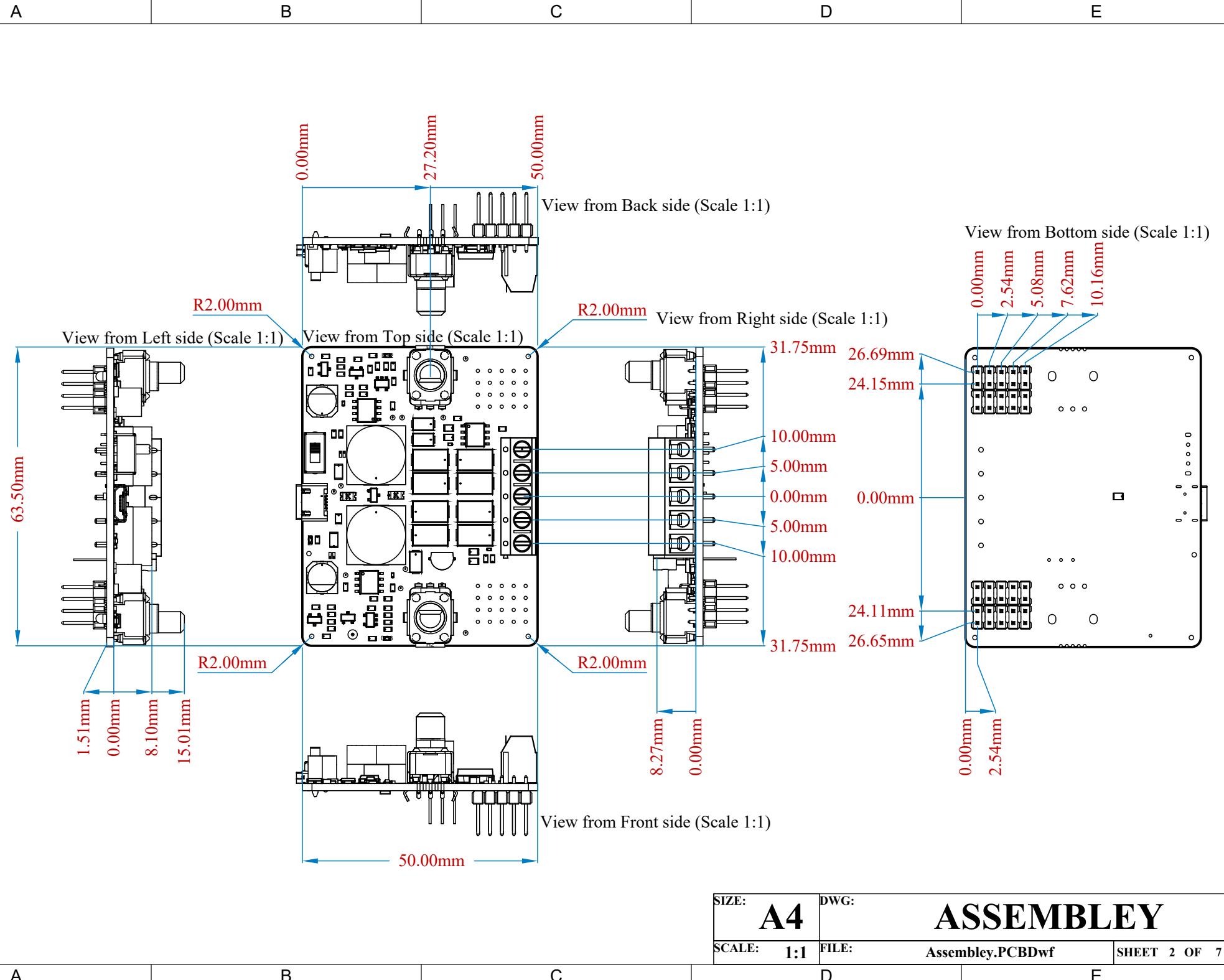
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B

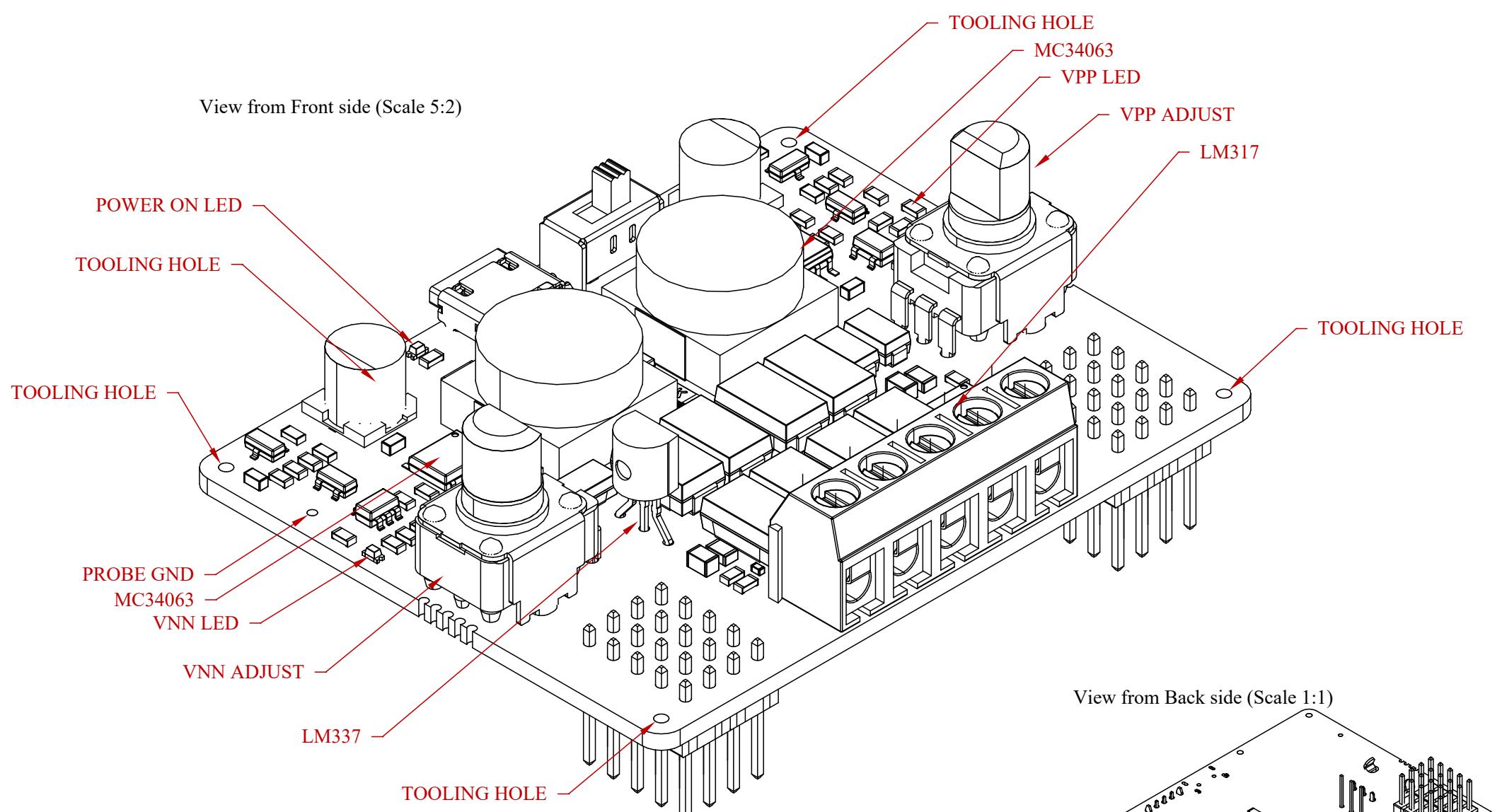
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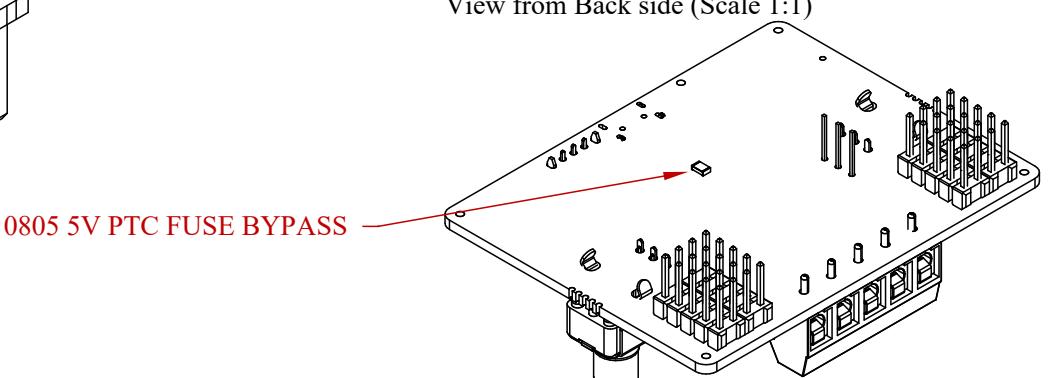
E



A B C D E

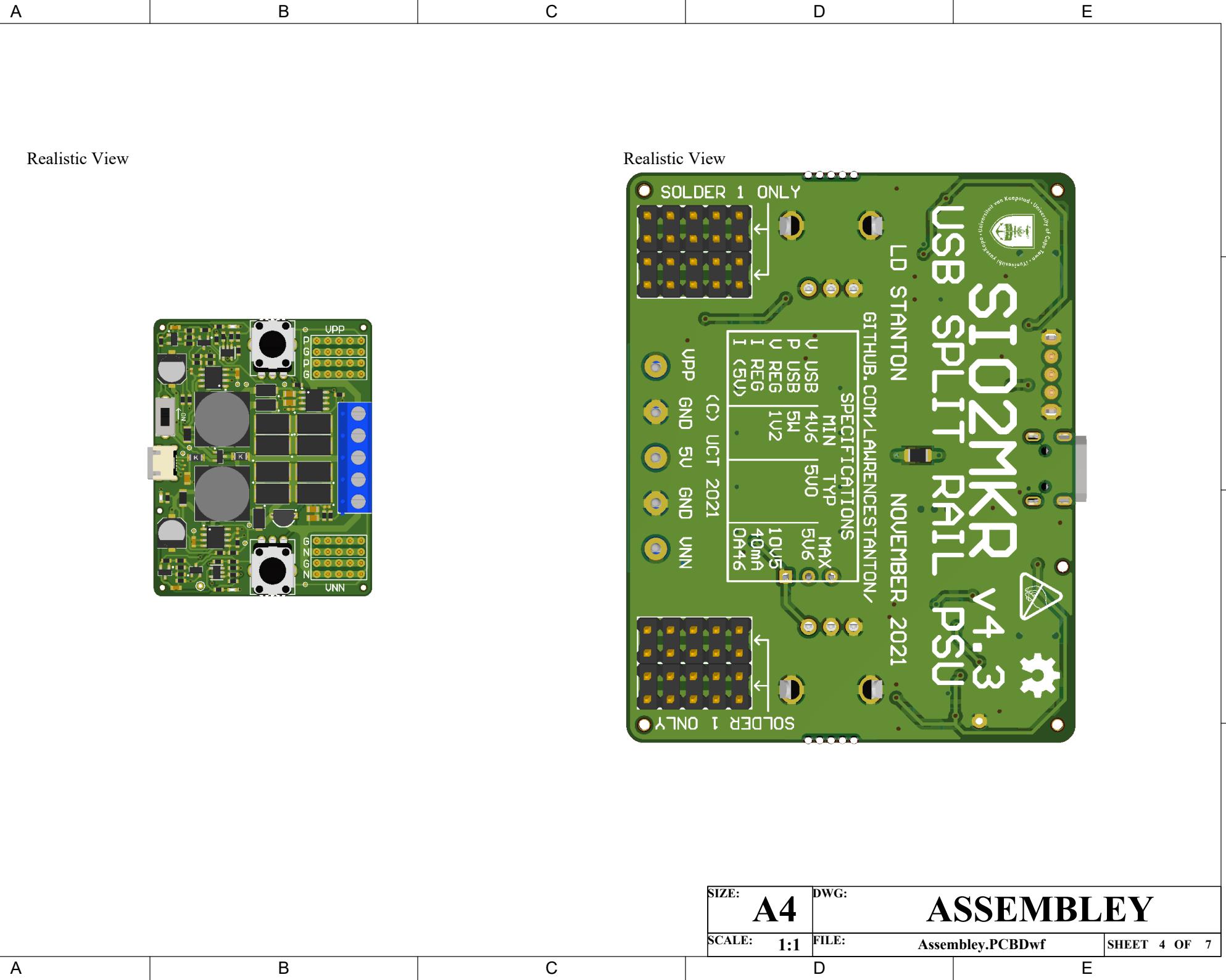


View from Back side (Scale 1:1)

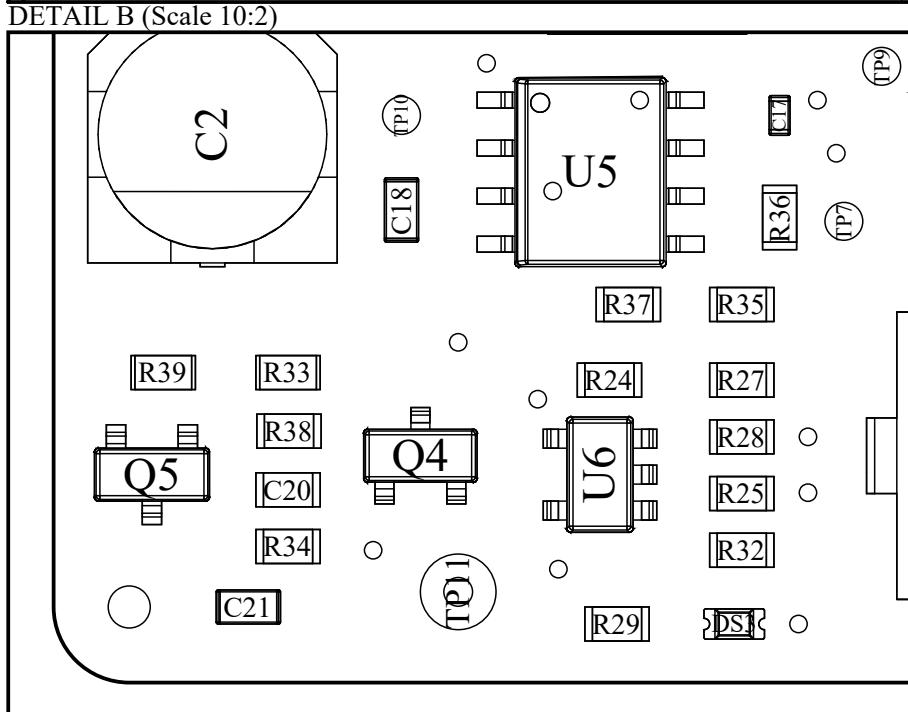
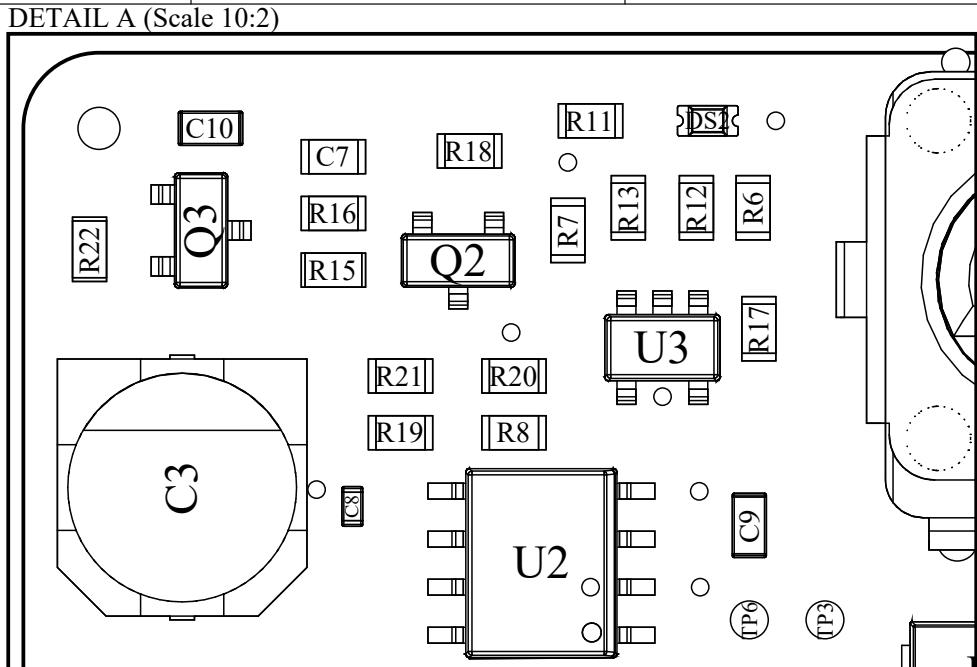
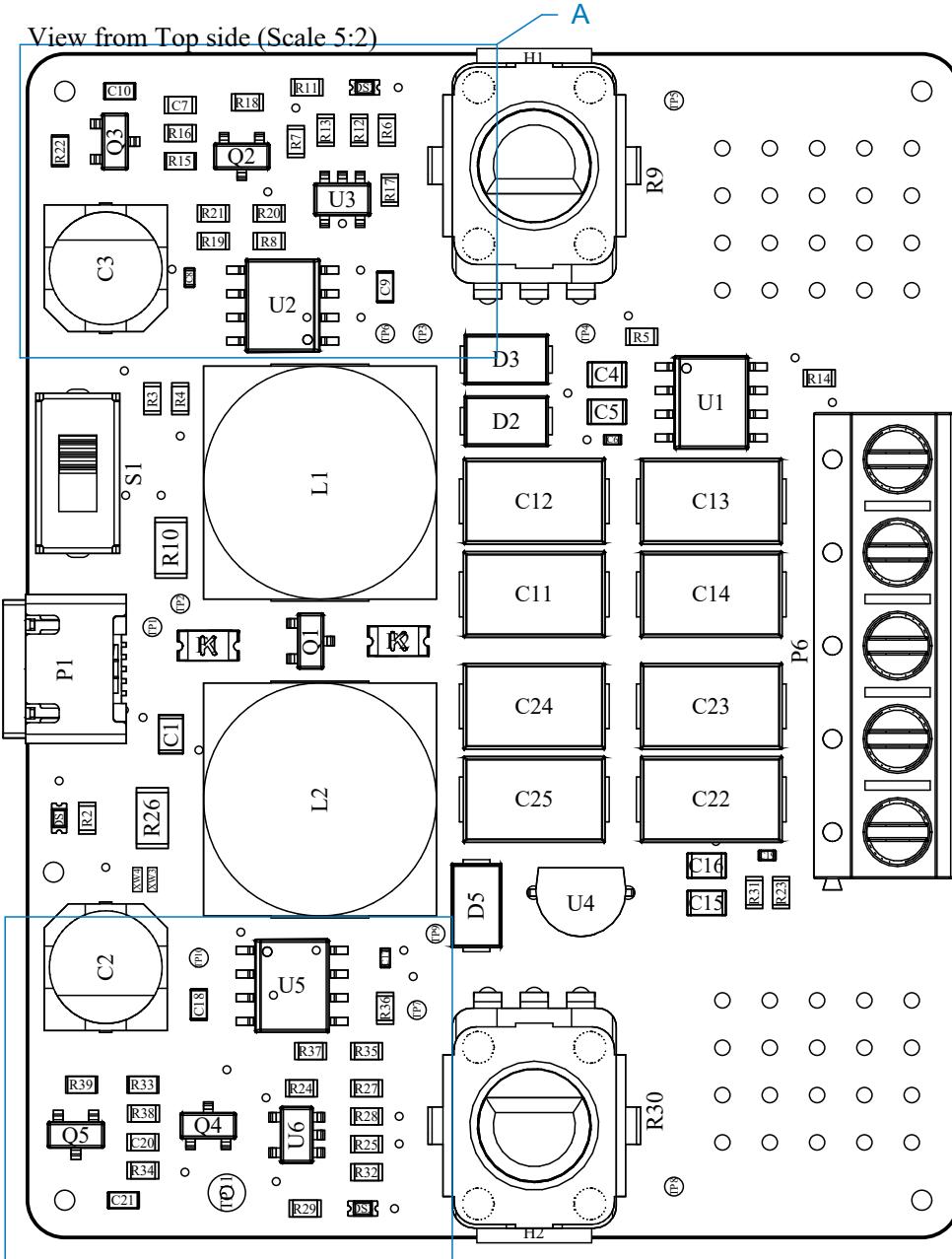


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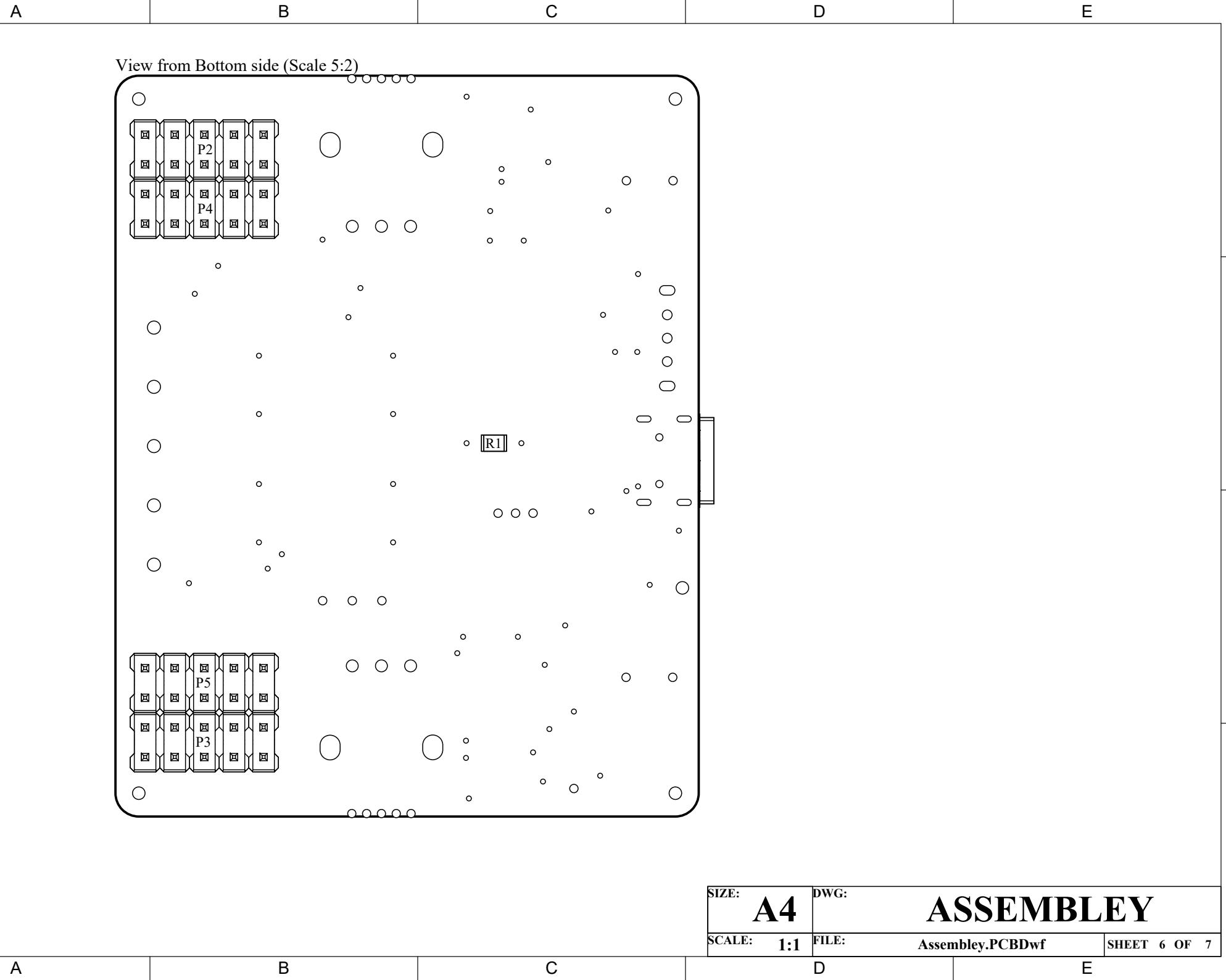
A B C D E



SIZE:	A4	DWG:	ASSEMBLY		
SCALE:	1:1	FILE:	Assembly.PCBDwf		



SIZE: A4 DWG: ASSEMBLY
SCALE: 1:1 FILE: Assembly.PCBDwf SHEET 5 OF 7



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Bill Of Materials Page 1

Line #	Designator	Comment	Quantity
1	C1	CL21B103KBANNNC	1
2	C2, C3	RVT1A221M0605	2
3	C4, C16	CC0805KRX7R9BB104	2
4	C5, C15	CL21B105KBFNNNE	2
5	C6, C19	0402CG3R3C500NT	2
6	C7, C20	CC0603KRX7R9BB104	2
7	C8, C17	CL05B104KO5NNNC	2
8	C9, C18	CL10B102KB8NNNC	2
9	C10, C21	MLCC 10pF 0603 50V C0G	2
10	C11, C12, C13, C14, C22, C23, C24, C25	293D107X9016D2TE3	8
11	D2, D3, D5	SS34	3
12	DS1, DS2, DS3	19-217/GHC-YR1S2/3T	3
13	F1	0468001.NRHF	1
14	F2	nSMD020-30V	1
15	L1, L2	SWRB1207S-331MT	2
16	P1	MICRO 4P DIP	1
17	P2, P3, P4, P5	A2541WV-2x5P	4
18	P6	CZM5,08-4E	1
19	Q1	AO3401A	1
20	Q2, Q4	LBSS84LT1G	2
21	Q3, Q5	SS8050	2
22	R1	0805W8F0000T5E	1
23	R2, R11, R29	0603WAF3300T5E	3
24	R3, R38	0603WAF1002T5E	2
25	R4, R8	0603WAF1200T5E	2
26	R5, R23	0603WAF2400T5E	2
27	R6	0603WAF6802T5E	1
28	R7, R12, R24, R25	0603WAF3302T5E	4
29	R9	RK09K1130AU2	1
30	R10, R26	1206W4F680LT5E	2
31	R13	0603WAF1202T5E	1
32	R14, R31	0603WAF2701T5E	2
33	R15, R33	0603WAF4702T5E	2
34	R16, R34	0603WAF2702T5E	2
35	R17, R27, R32	0603WAF1003T5E	3
36	R18	0603WAF1002T5E	1
37	R19, R36	0603WAF5602T5E	2
38	R20, R21, R35, R37	0603WAF5601T5E	4
39	R22, R39	0603WAF1002T5E	2
40	R28	0603WAF5602T5E	1
41	R30	RK09K1130AU2	1
42	S1	SS12D07L2B	1
43	U1	LM317LBDR2G	1
44	U2, U5	MC34063ADR2G	2

Bill Of Materials Page 2

SIZE: A4 **DWG:**

SCALE: 1:1 FILE: Assembly.PCBDwf SHEET 7 OF 7

A

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