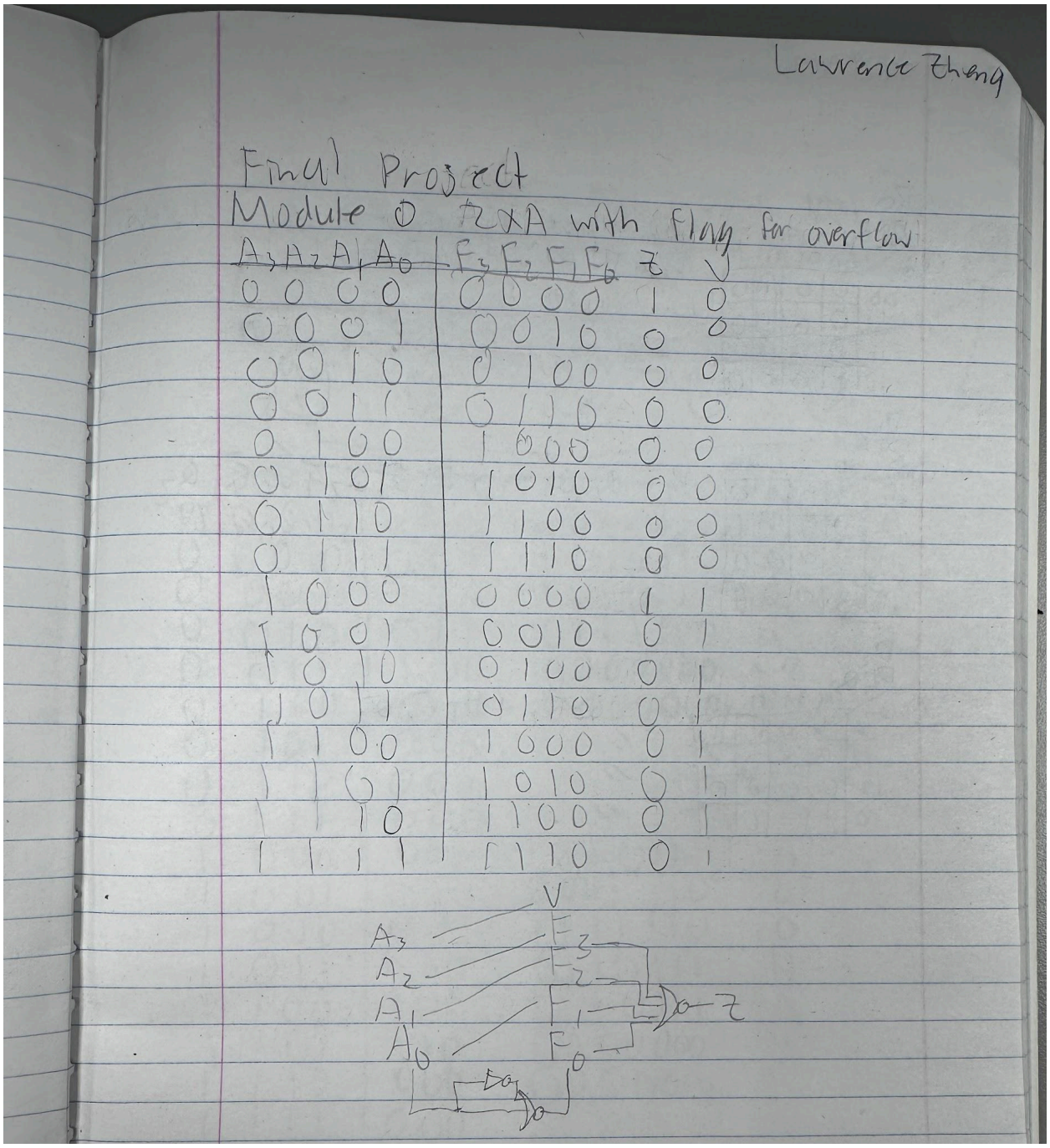
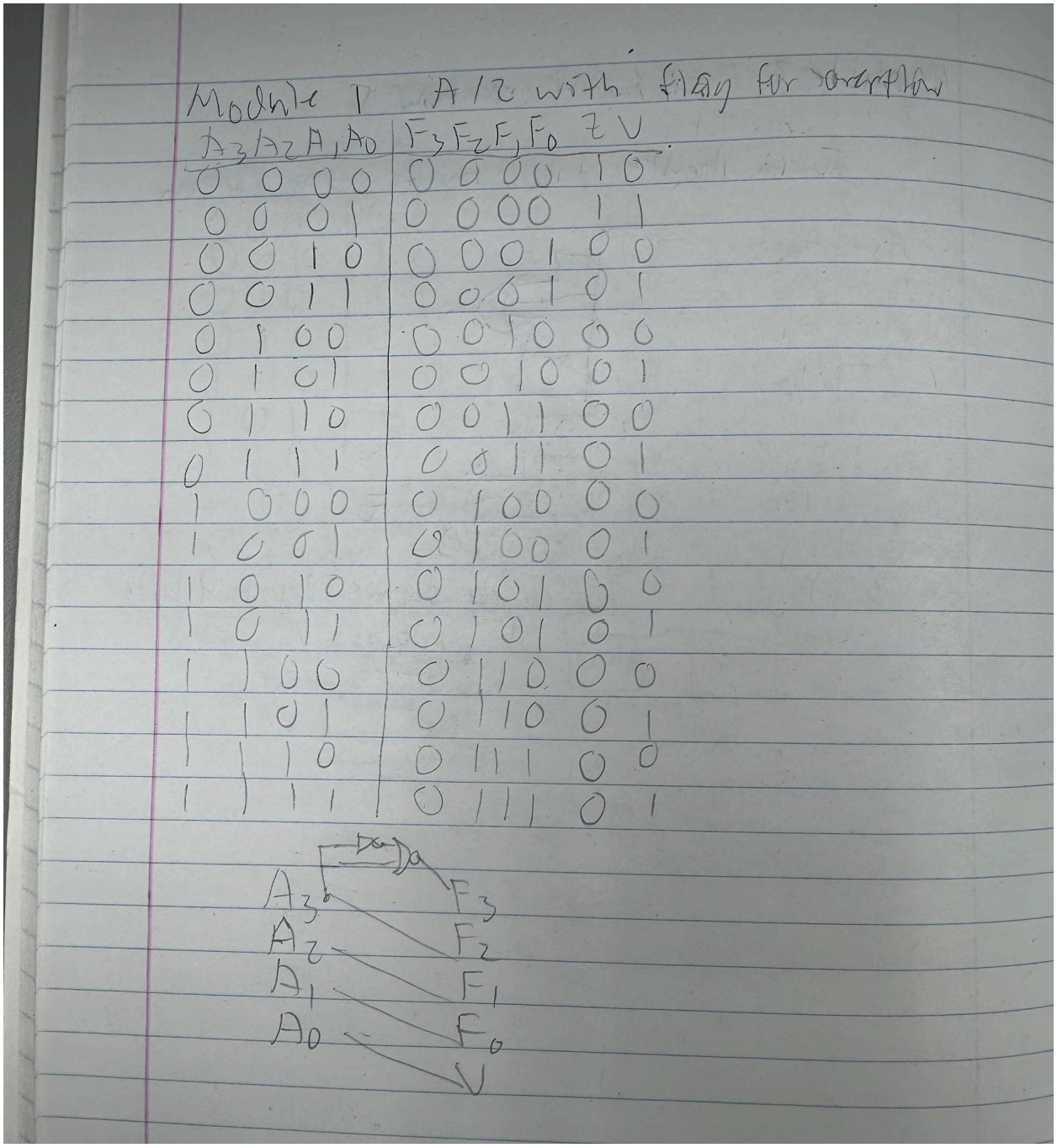
Task 1:

Module 0:



Module 1:

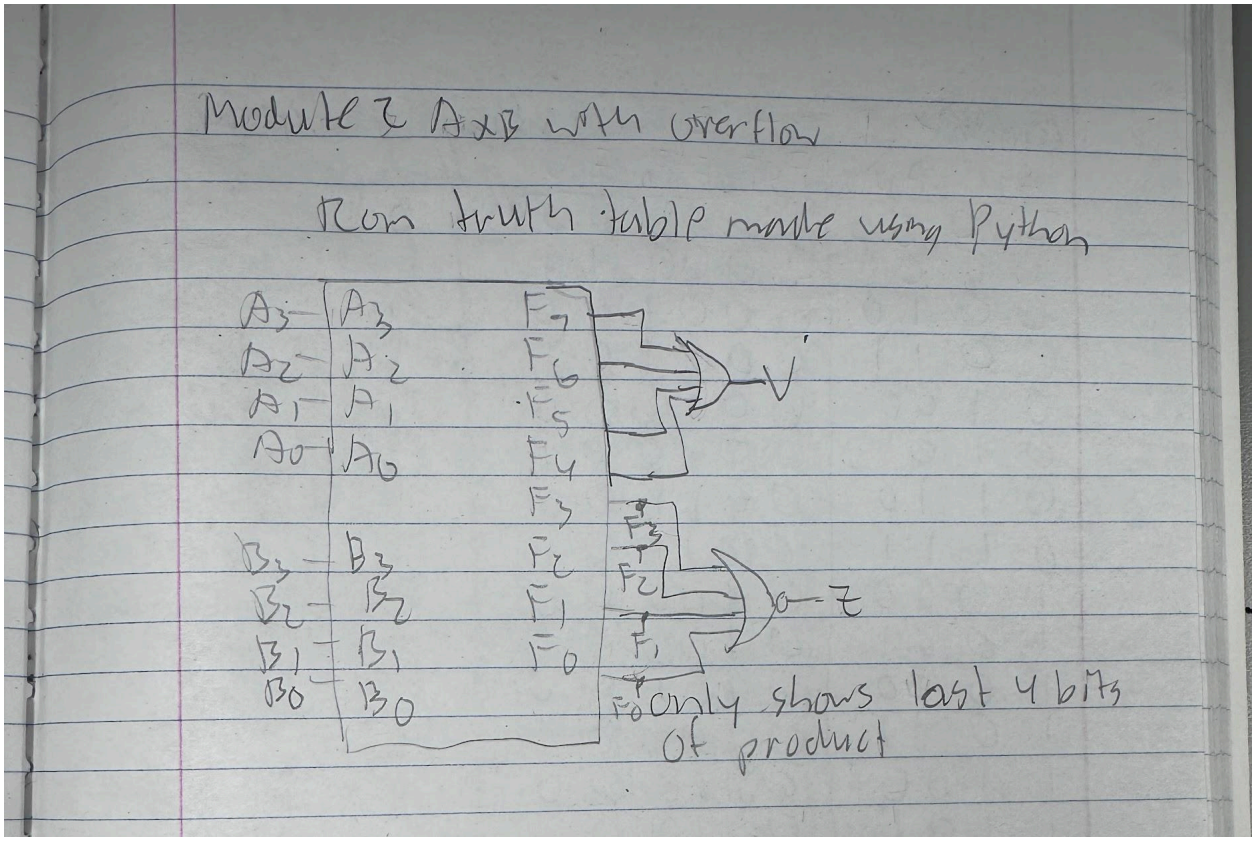


Module 1 A/2 with flag for overflow

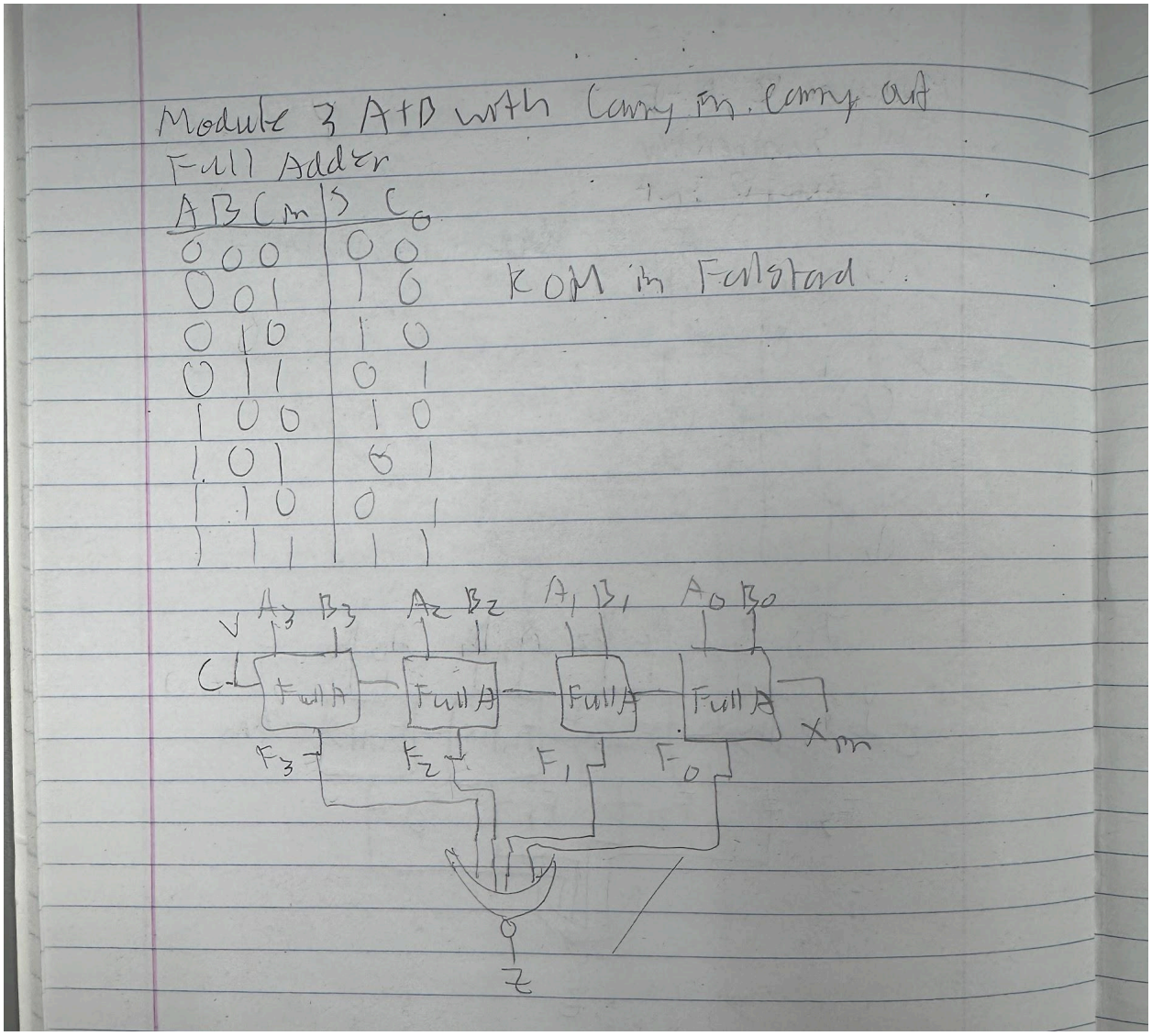
A_3	A_2	A_1	A_0	F_3	F_2	F_1	F_0	Z	V
0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	1	0	0
0	0	1	0	0	0	1	0	0	0
0	0	1	1	0	0	1	1	0	0
0	1	0	0	0	1	0	0	0	0
0	1	0	1	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0	0
0	1	1	1	0	1	1	1	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	1	1	0	0	1	0	0
1	0	1	0	1	0	1	0	0	0
1	0	1	1	1	0	1	1	0	0
1	1	0	0	1	1	0	0	0	0
1	1	0	1	1	1	0	1	0	0
1	1	1	0	1	1	1	0	0	0
1	1	1	1	1	1	1	1	0	0

Module 2:

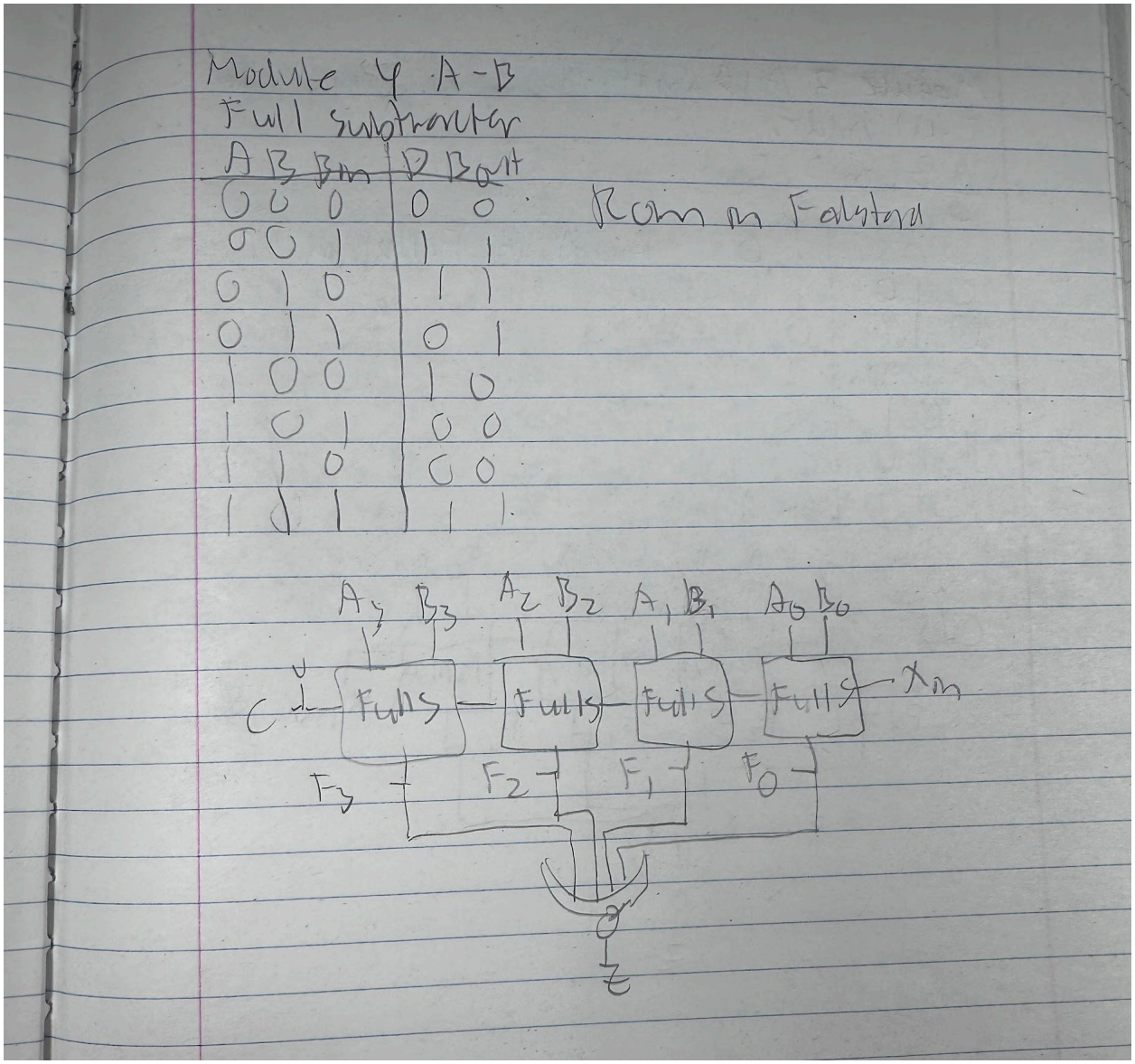
```
for i in range(16):
    for j in range(16):
        print(f'{i:04b}{j:04b}={i*j:08b}')
```



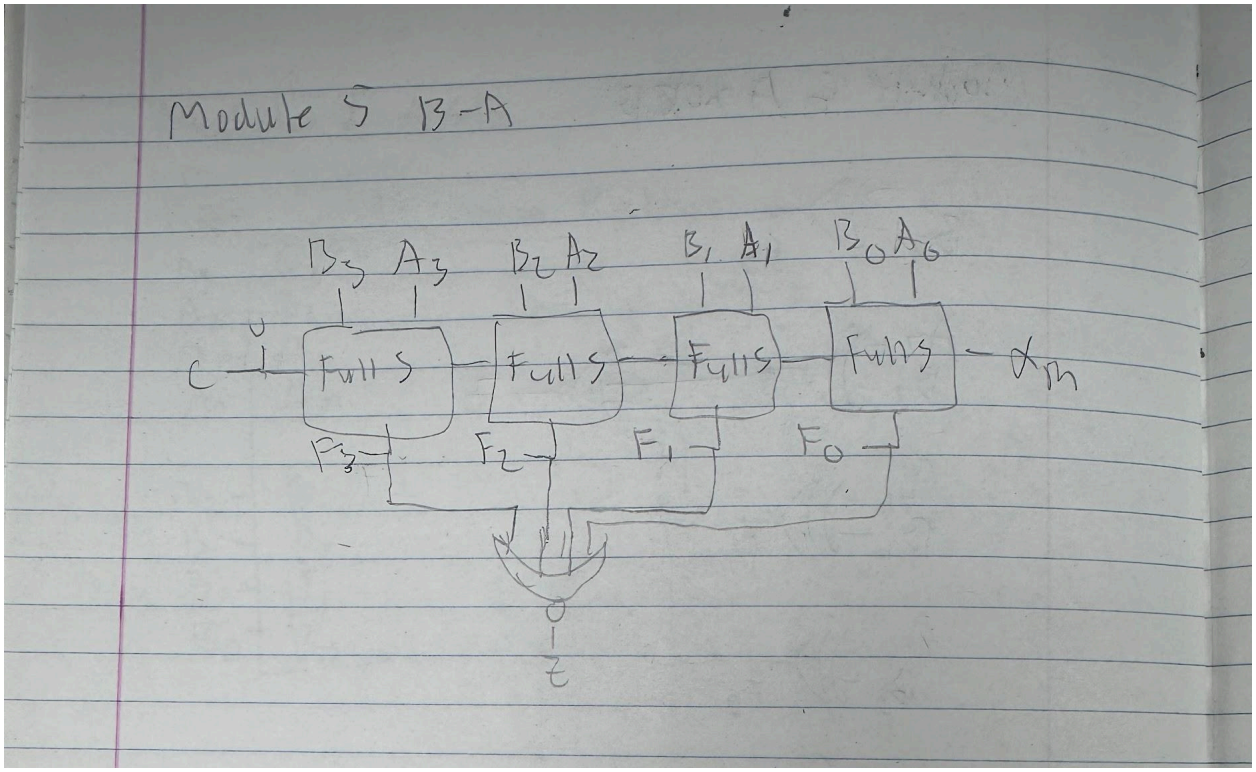
Module 3:


Module 3 A+B with Carry in, Carry out
Full Adder
A B Cm | S Co
0 0 0 | 0 0
0 0 1 | 1 0
0 1 0 | 1 0
0 1 1 | 0 1
1 0 0 | 1 0
1 0 1 | 0 1
1 1 0 | 0 1
1 1 1 | 1 1
KOM in Fullstand
A3 B3 A2 B2 A1 B1 A0 B0
Cin
Full A
Full A
Full A
Full A
Xm
F3
F2
F1
F0
Z

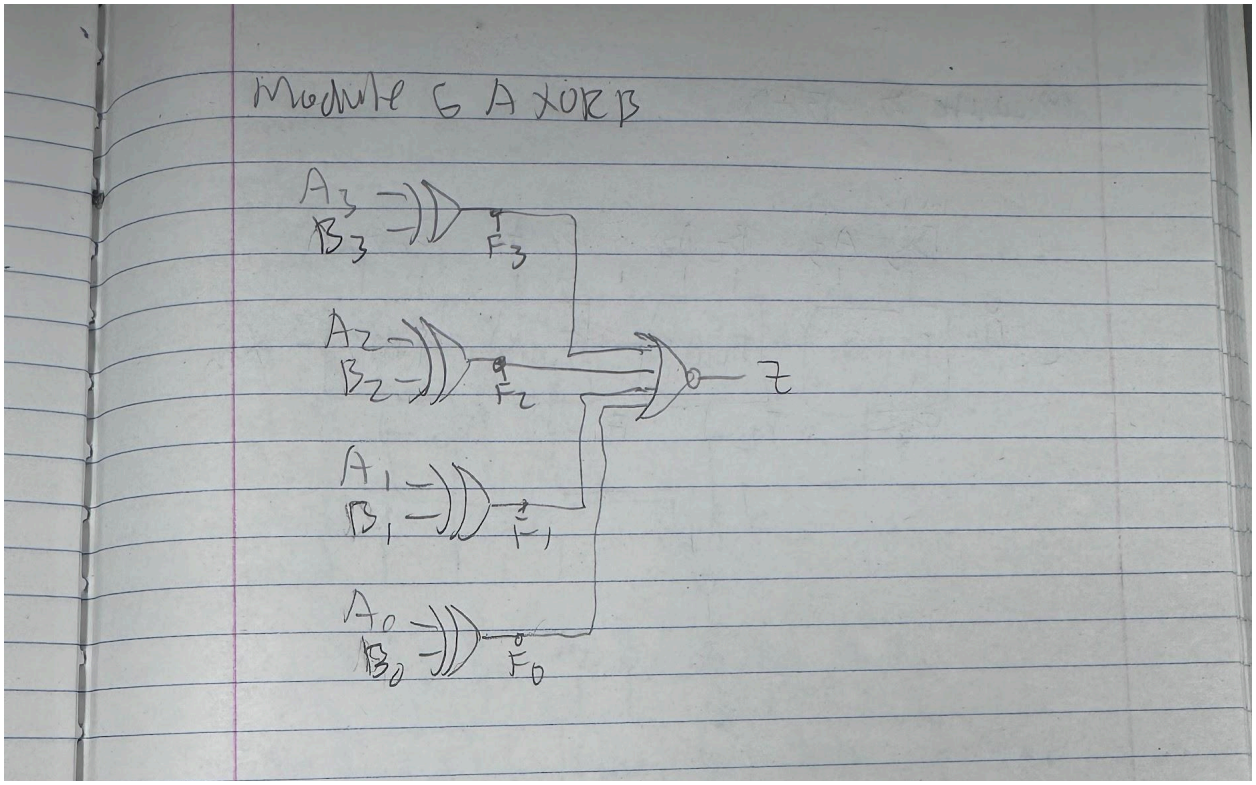
Module 4:



Module 5:

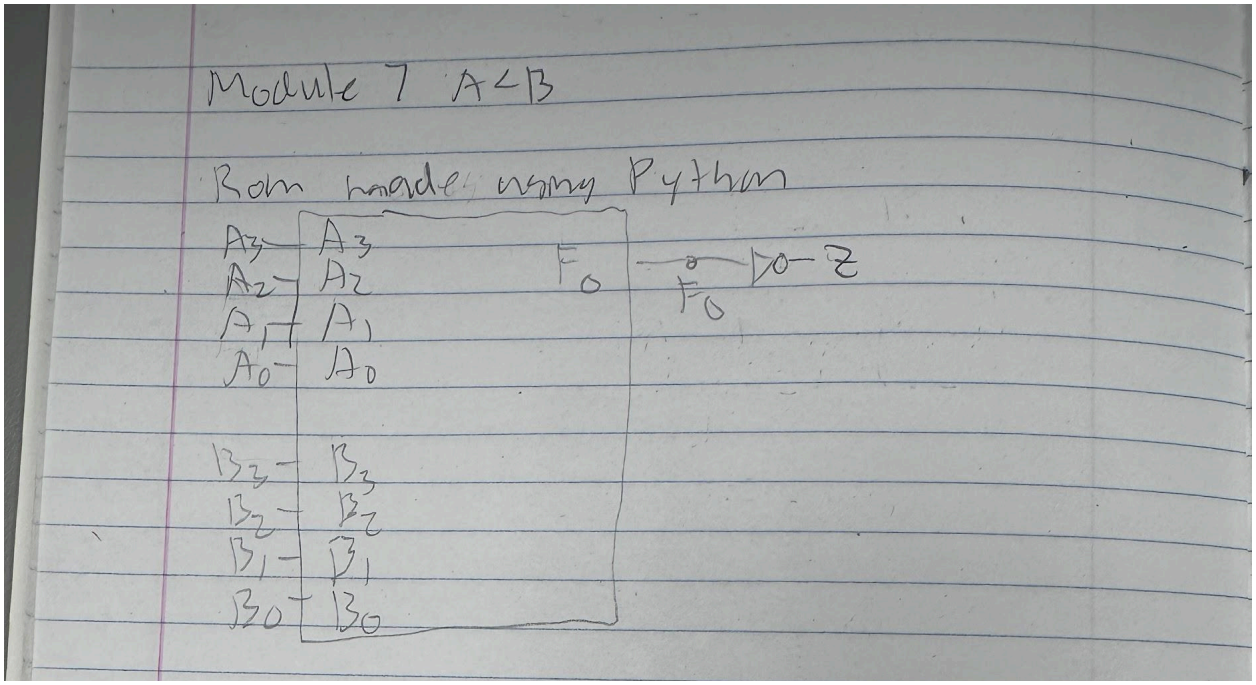

Module 5 B-A
B3 A3
B2 A2
B1 A1
B0 A0
C
Full S
Full S
Full S
Full S
Cout
F3
F2
F1
F0
Z

Module 6:


Module 6 A XOR B
A3
B3
F3
A2
B2
F2
Z
A1
B1
F1
A0
B0
F0

Module 7:

```
for i in range(16):
    for j in range(16):
        print(f'{i:04b}{j:04b}={i<j:b}')
```



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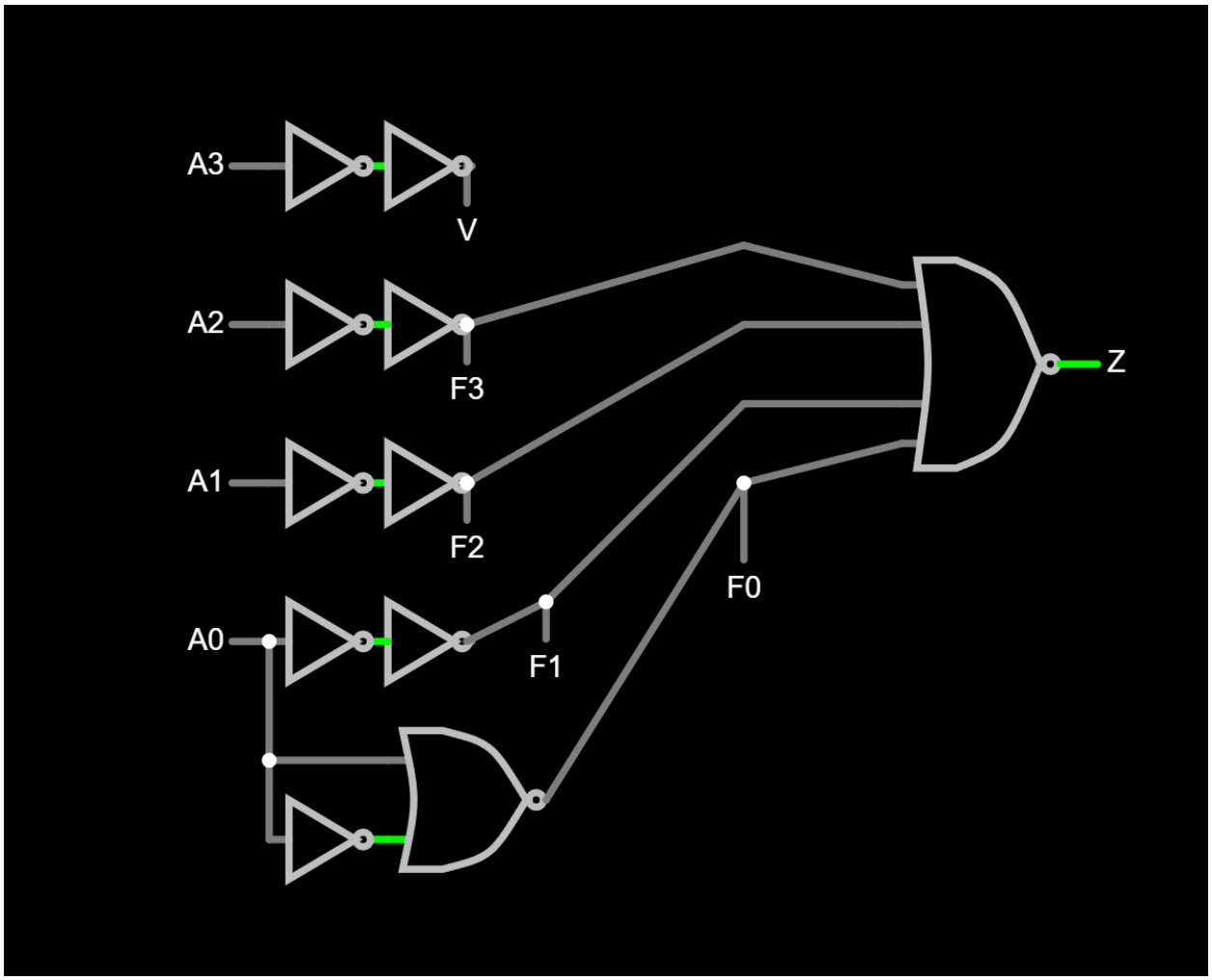
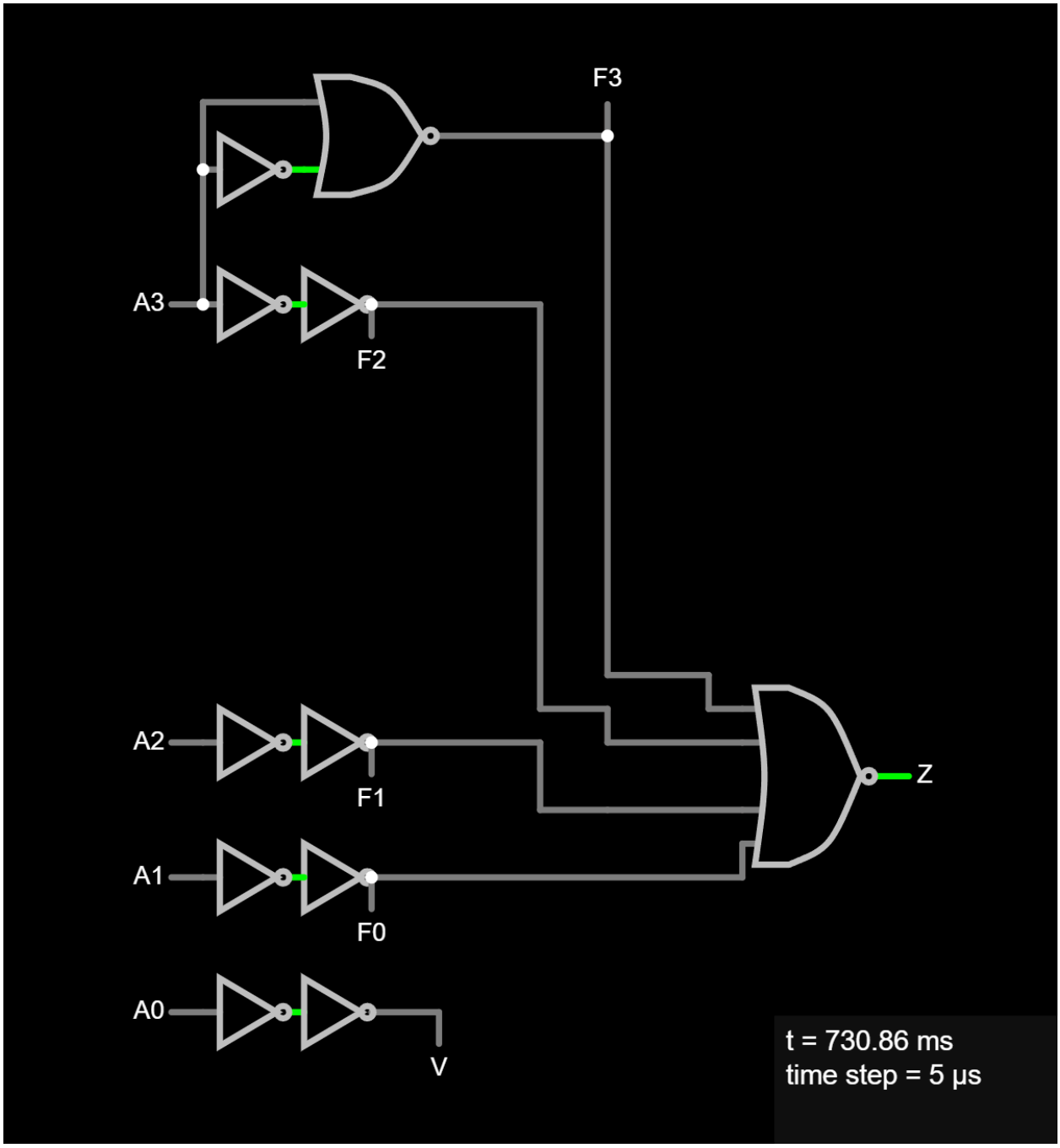
Task 2:

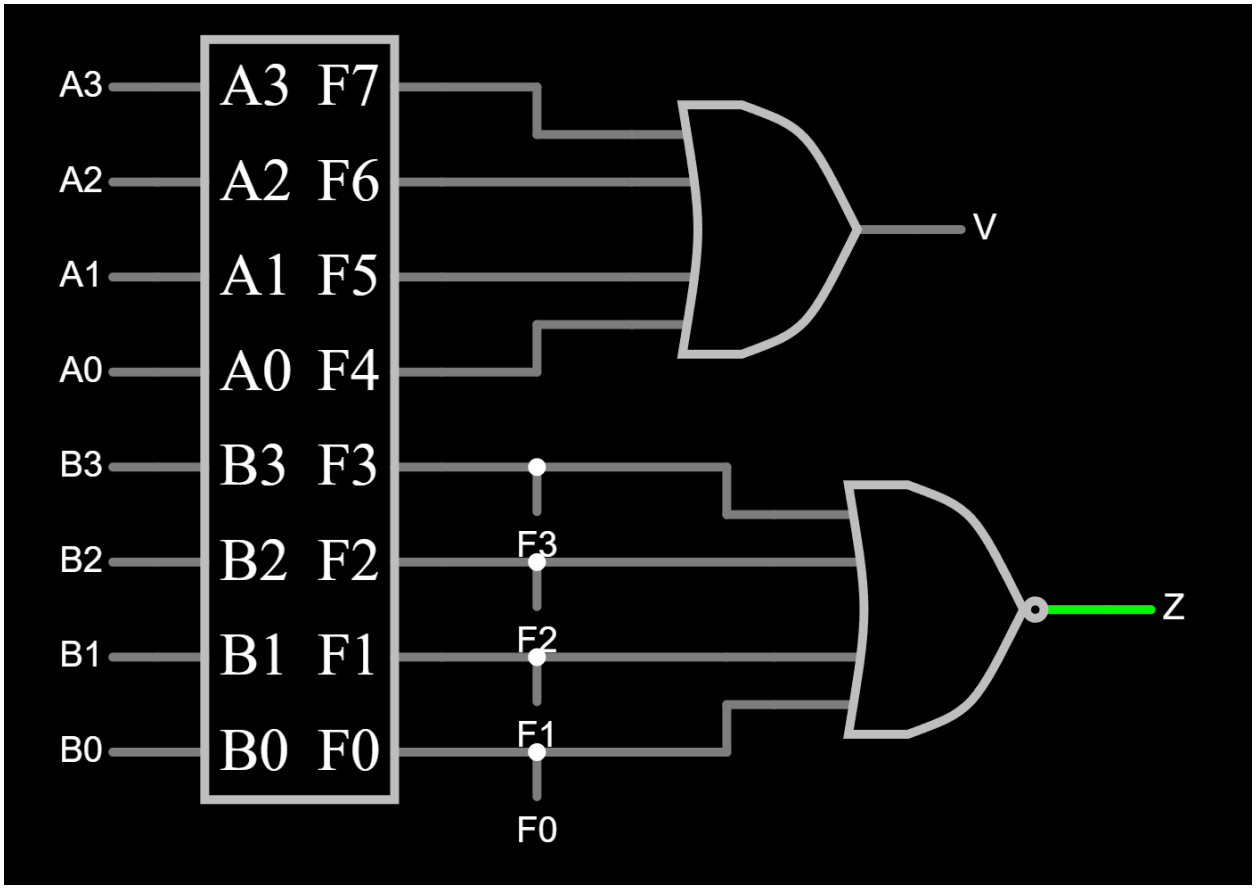
Module 0:



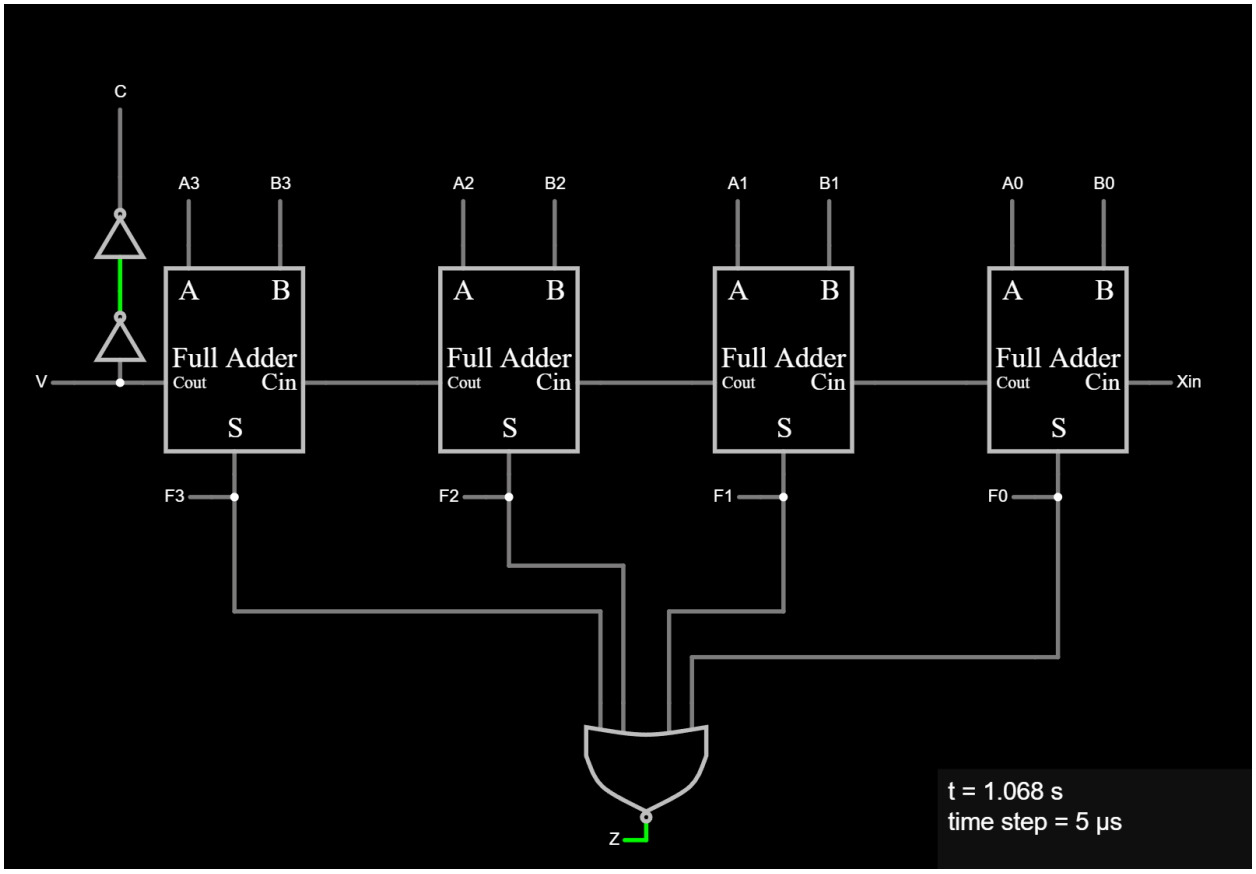
Module 1:



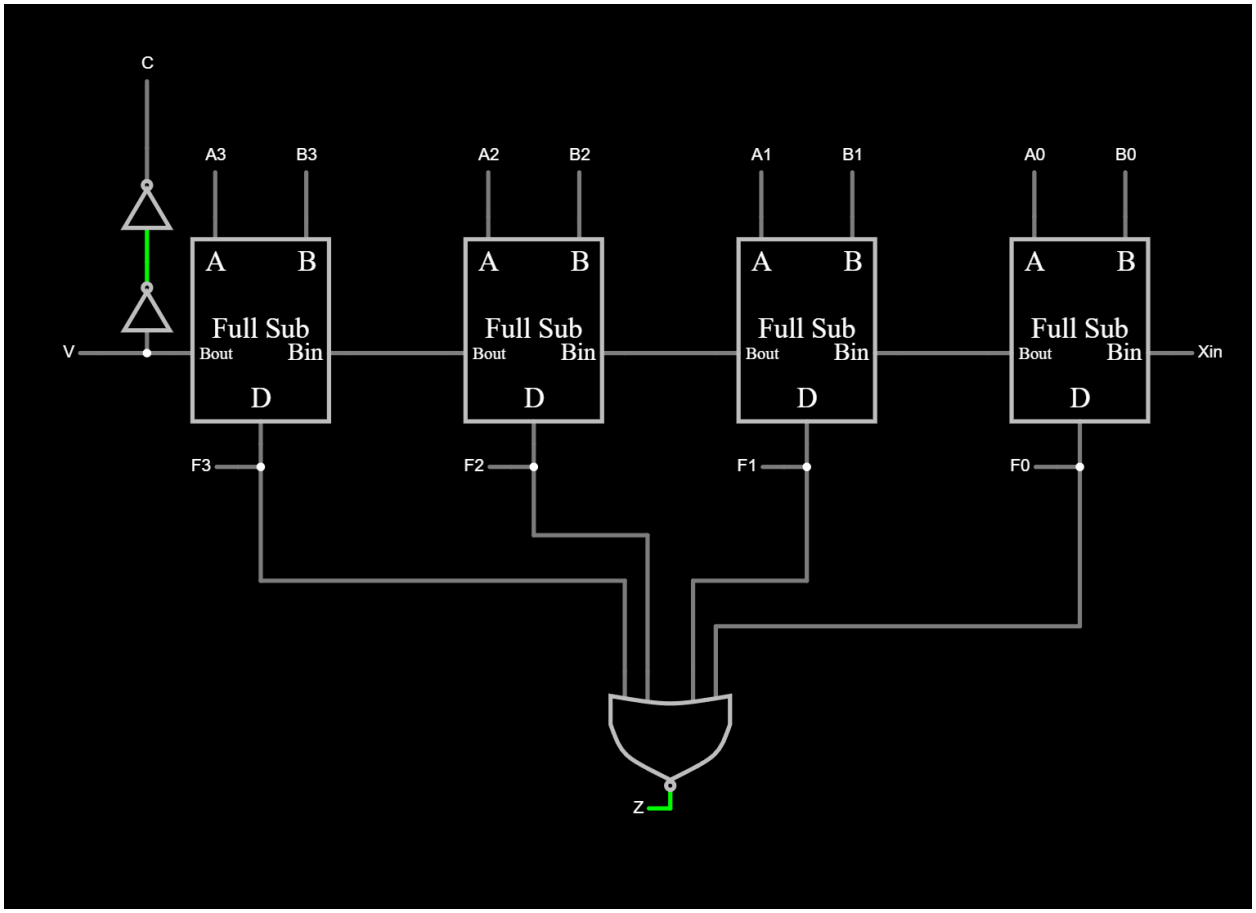
Module 2:


A3
A2
A1
A0
B3
B2
B1
B0
A3 F7
A2 F6
A1 F5
A0 F4
B3 F3
B2 F2
B1 F1
B0 F0
F3
F2
F1
F0
V
Z

Module 3:


C
A3
B3
A2
B2
A1
B1
A0
B0
A
B
Full Adder
Cout
Cin
S
V
Xin
F3
F2
F1
F0
Z
t = 1.068 s
time step = 5 µs

Module 4:



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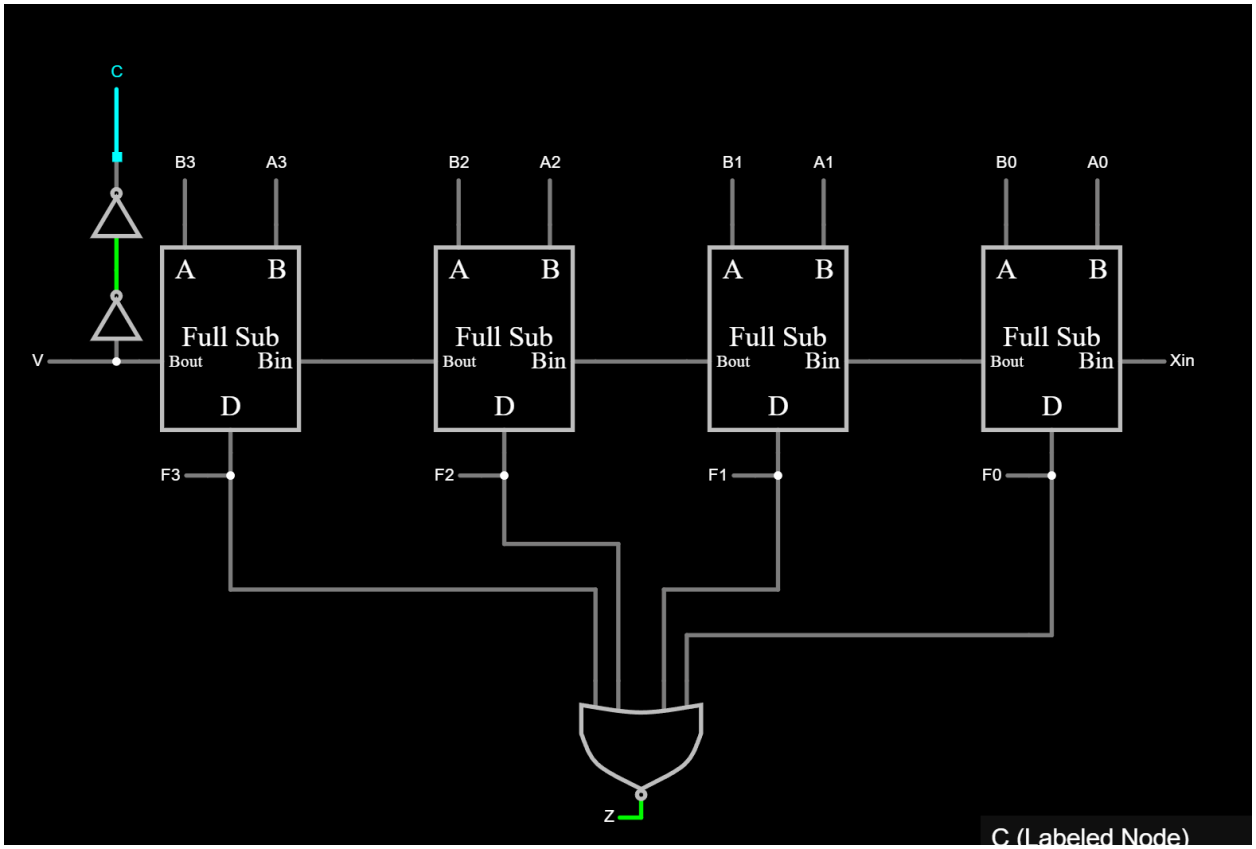
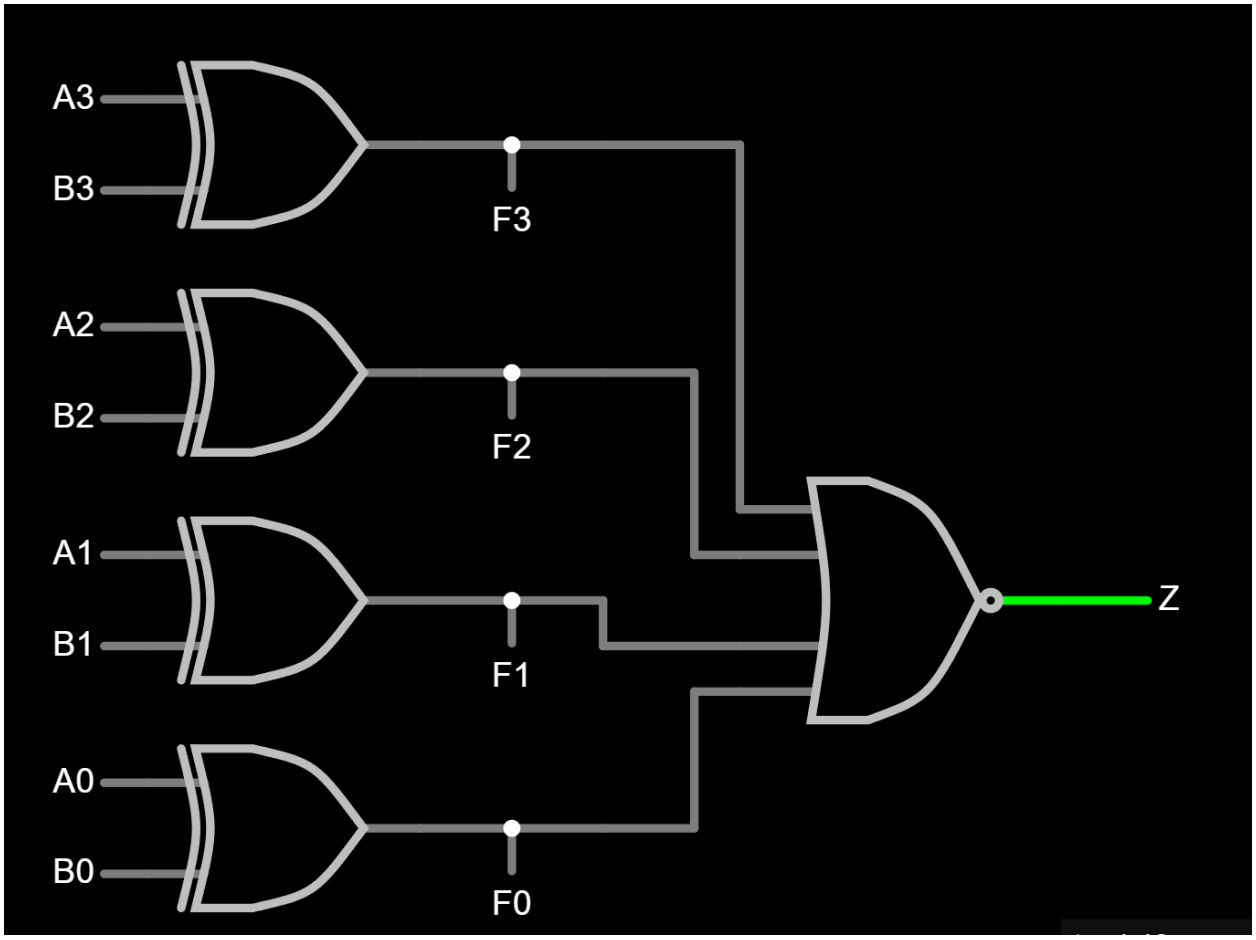
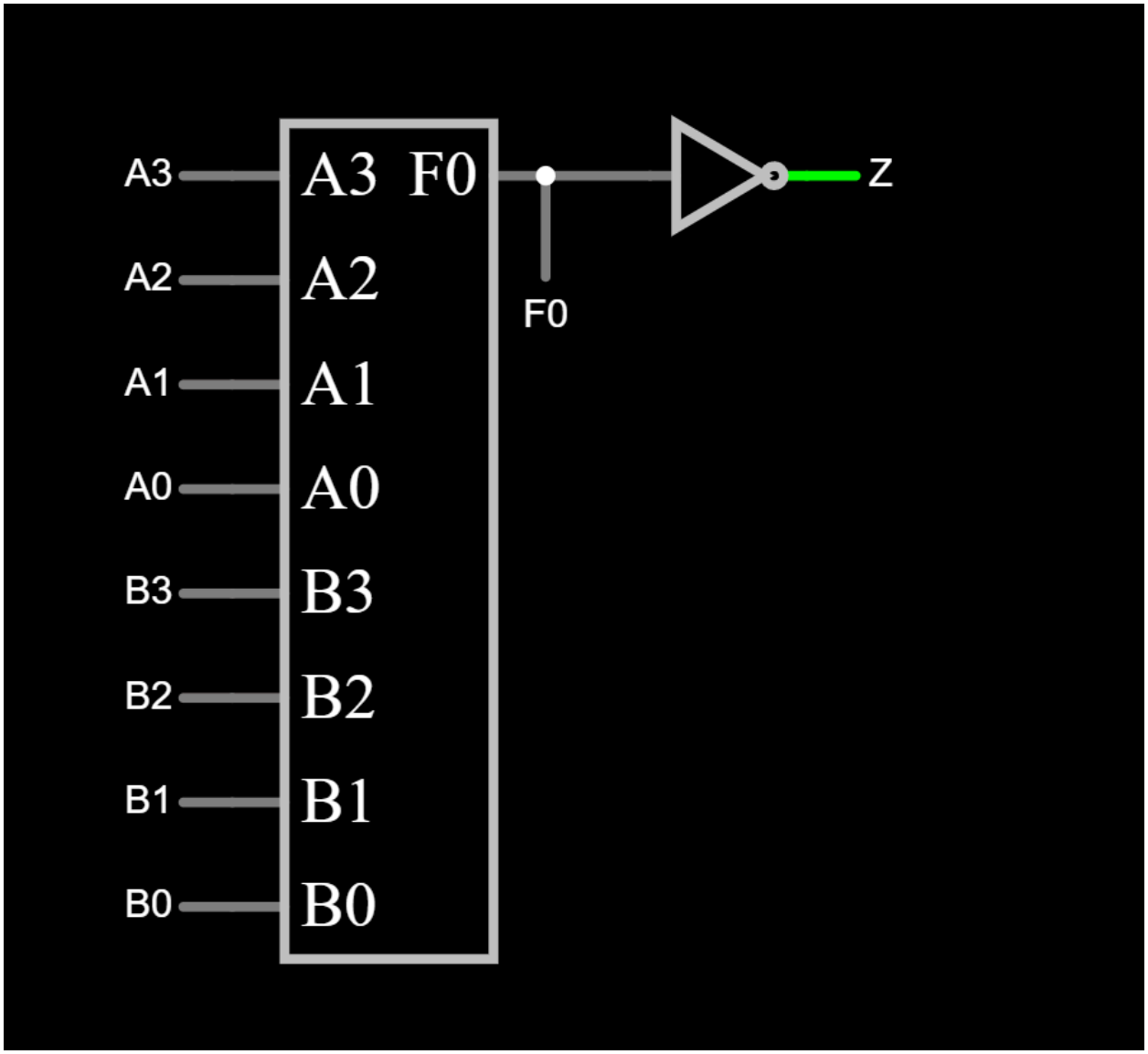
Module 5:



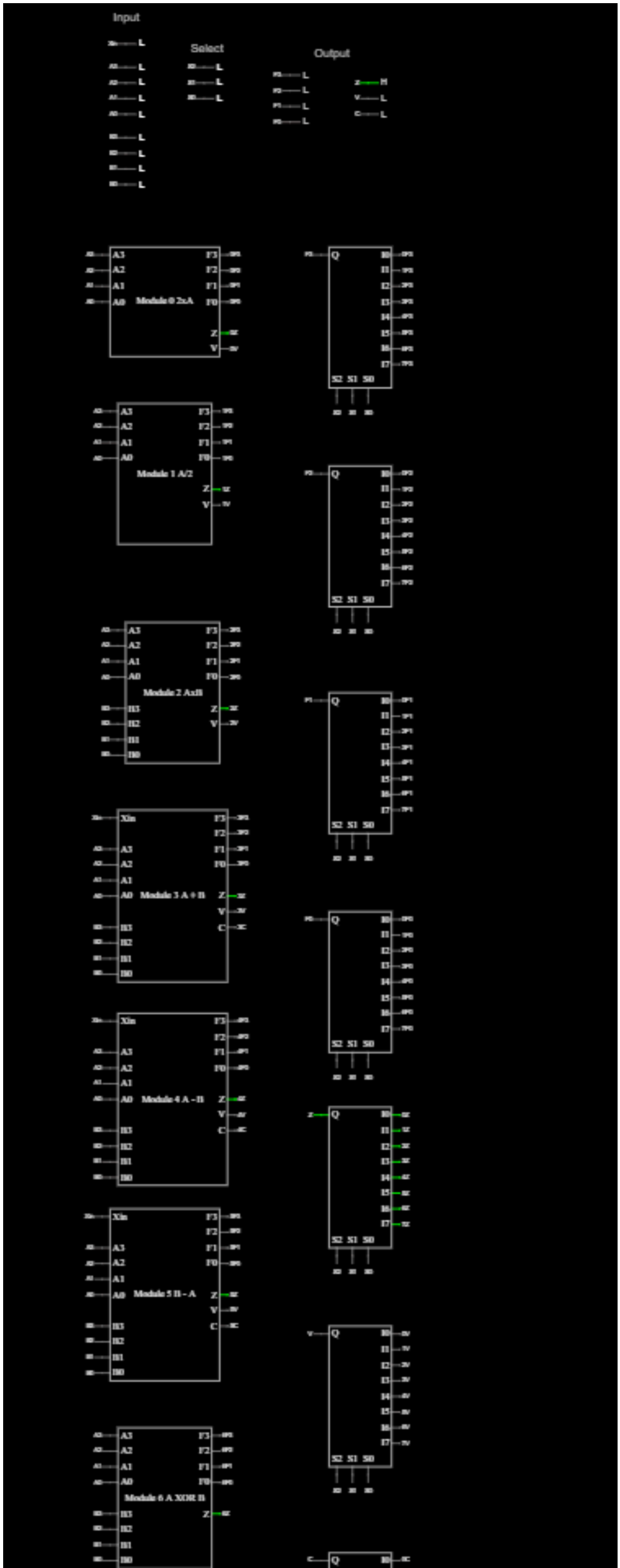
Module 6:



Module 7:



Combined circuit attached in ALU.txt


Input
Select
Output
Module 0 2xA
Module 1 A/2
Module 2 Ax8
Module 3 A + B
Module 4 A - B
Module 5 B - A
Module 6 A XOR B

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Task 3:

Attached EDA link in case file doesn’t convert properly