


# *Final Project - Two Stage OP*



# Design Flow

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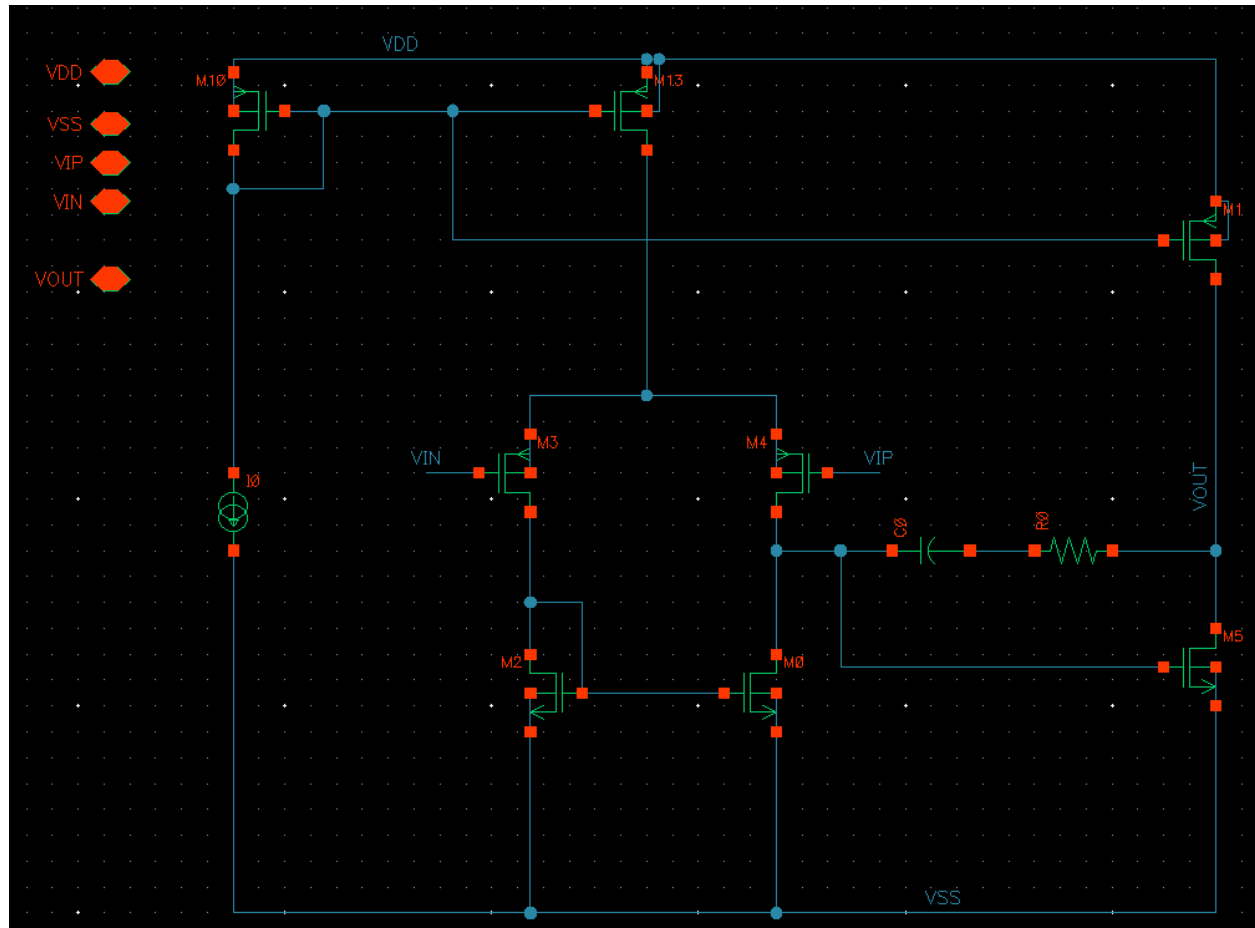
- Reference:
  - P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design," 2012
  - Chapter 6.3

## 6.3 Design of the Two-Stage Op Amp

- You can finish the two stage OP Amp step by step



# Schematic



# Spec

	SPEC	Unit
VDD	1.8	V
$C_L$	1	pF
DC Gain	> 70	dB
GBW	> 5	MHz
Phase Margin	$\geq 60$	degree
Slew Rate	> 5	V/ $\mu$ s
Power Dissipation	< 50	$\mu$ W
FoM	$\frac{A_v(dB) \times GBW(MHz)}{P(mW)}$	The larger the better



# 報告要求

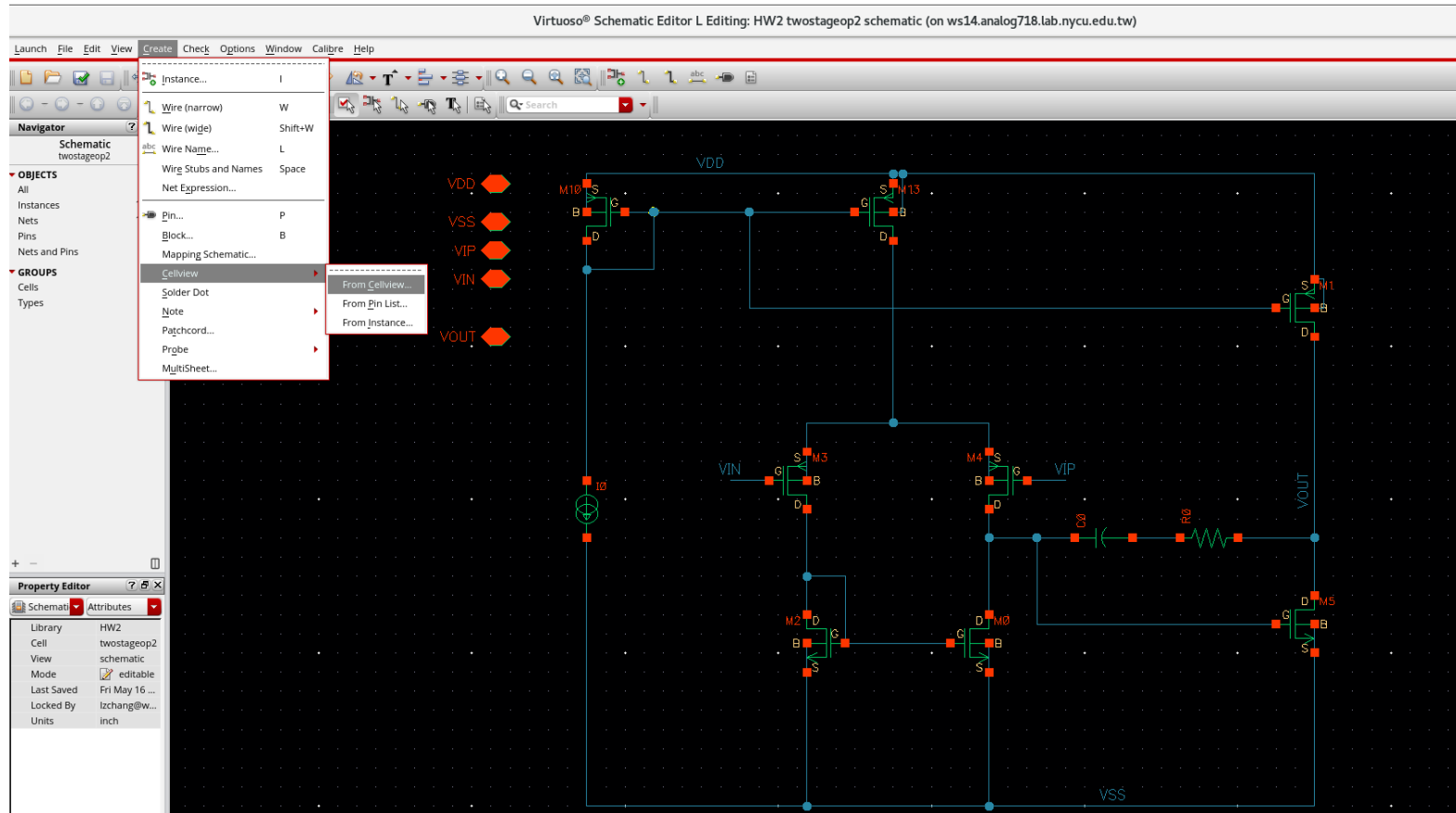
- 報告中須包含設計流程，模擬結果須一併附上自己的觀察看法
- 報告中須包含performance table，如下

	SPEC	This Work	Unit
VDD	1.8	1.8	V
$C_L$	1	1	pF
DC Gain	> 70	89.9	dB
GBW	> 5	8.76	MHz
Phase Margin	$\geq 60$	64	degree
Slew Rate	> 5	6.98	V/ $\mu$ s
Power Dissipation	< 50	34.92	$\mu$ W
FoM	$\frac{A_v(dB) \times GBW(MHz)}{P(\mu W)}$	22.55	The larger the better



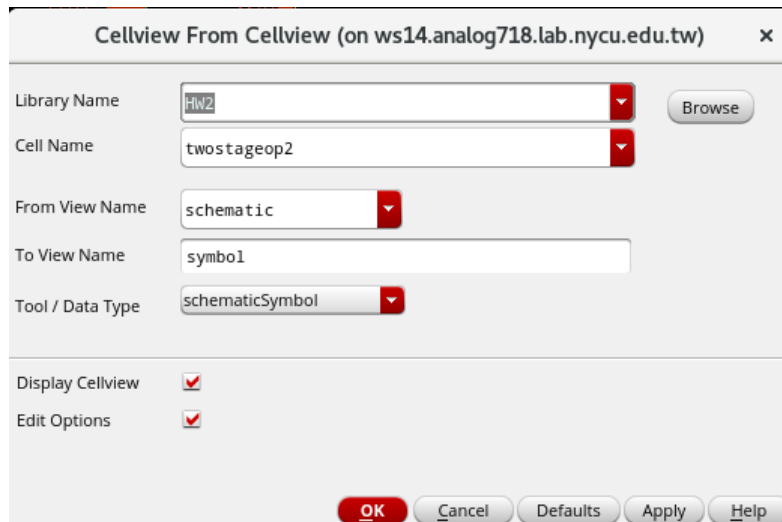
# Appendix – 建立symbol

- Create – cellview – from cellview



# Appendix – 建立symbol

- 按ok



Cellview From Cellview (on ws14.analog718.lab.nycu.edu.tw)

Library Name: HW2 (dropdown) [Browse]

Cell Name: twostageop2 (dropdown)

From View Name: schematic (dropdown)

To View Name: symbol

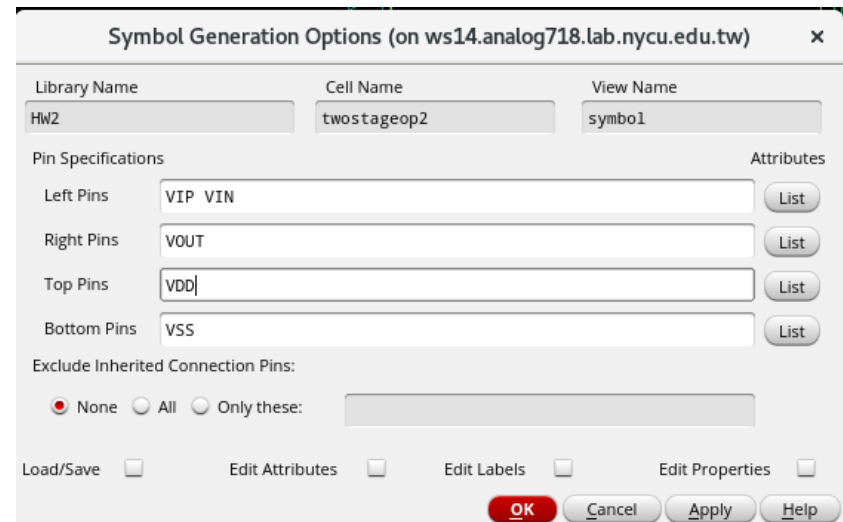
Tool / Data Type: schematicSymbol (dropdown)

Display Cellview: ☒

Edit Options: ☒

[OK] [Cancel] [Defaults] [Apply] [Help]

- 依照個人需求擺放PIN的位置



Symbol Generation Options (on ws14.analog718.lab.nycu.edu.tw)

Library Name: HW2 Cell Name: twostageop2 View Name: symbol

Pin Specifications

	Attributes
Left Pins: VIP VIN	[List]
Right Pins: VOUT	[List]
Top Pins: VDD	[List]
Bottom Pins: VSS	[List]

Exclude Inherited Connection Pins:  
☒ None ☐ All ☐ Only these: [ ]

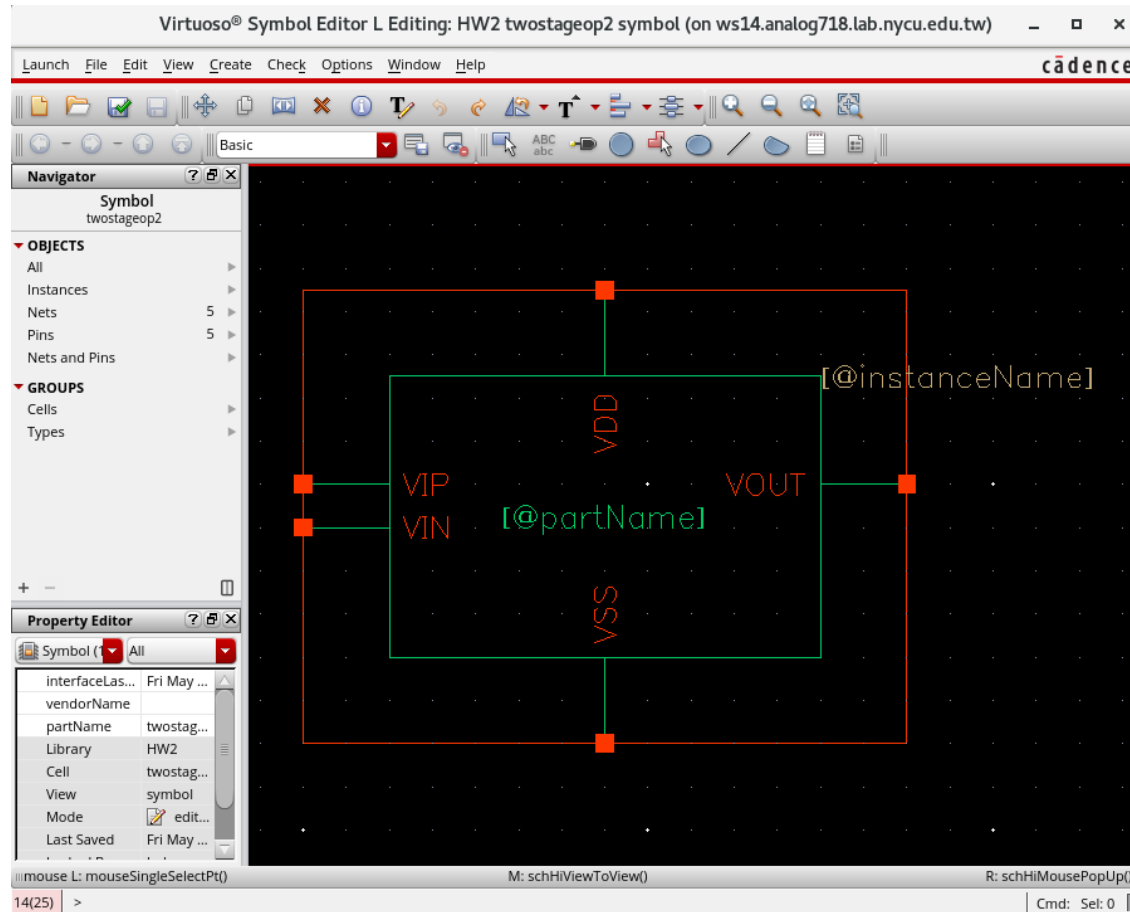
Load/Save: ☐ Edit Attributes: ☐ Edit Labels: ☐ Edit Properties: ☐

[OK] [Cancel] [Apply] [Help]



# Appendix – 建立symbol

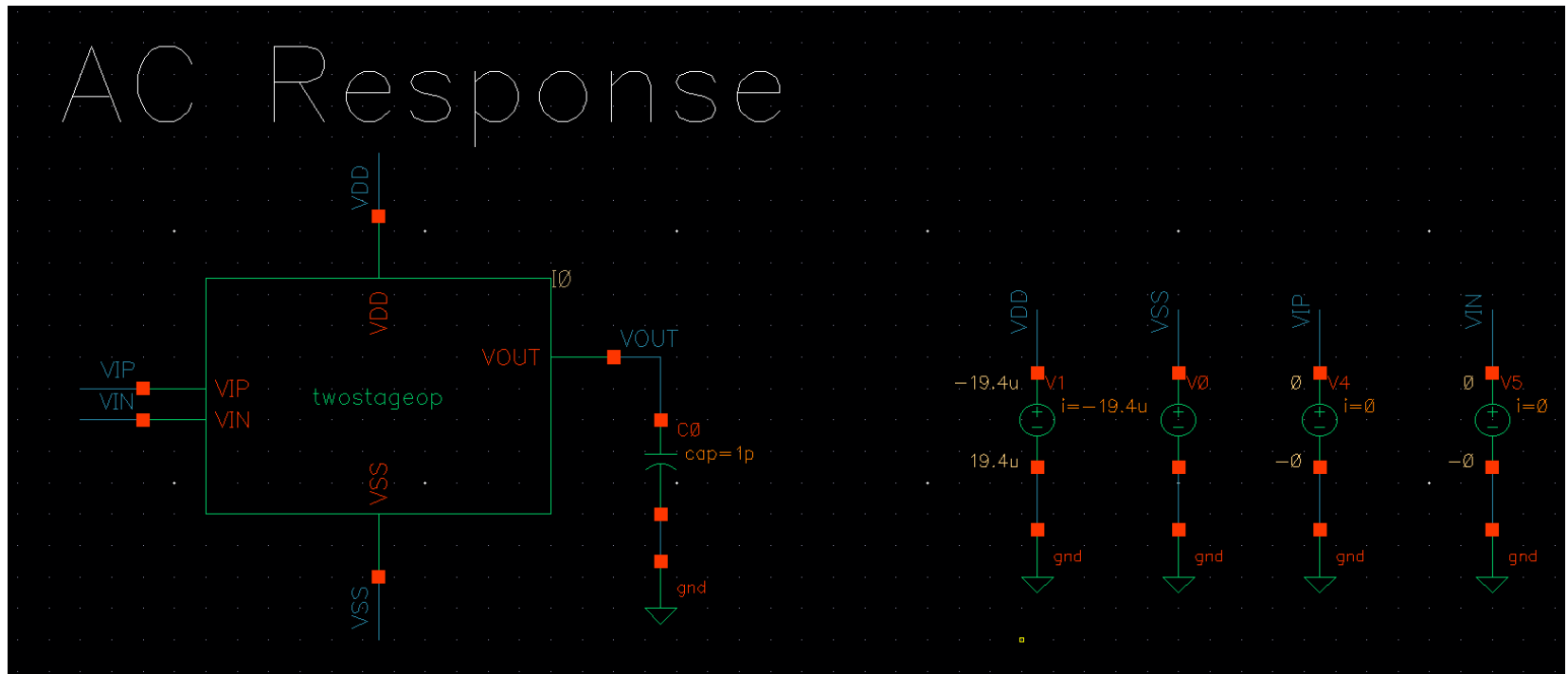
- 完成symbol，可直接關掉此視窗



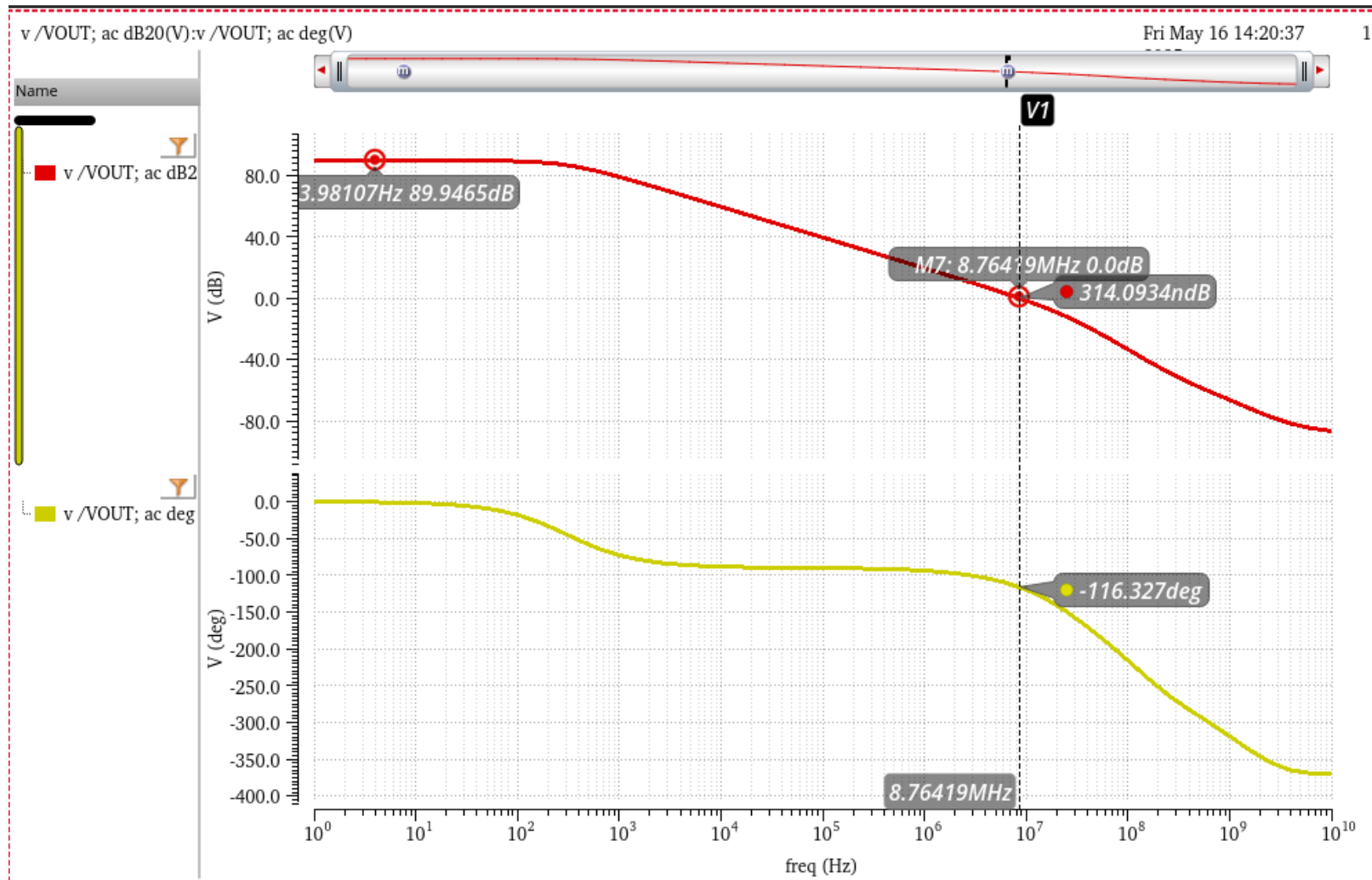


# Appendix – testbench

- 新建一個schematic
- 用i叫出剛剛產生的symbol，接上各電位後，後續模擬步驟與先前作業相同(ADEL.....)

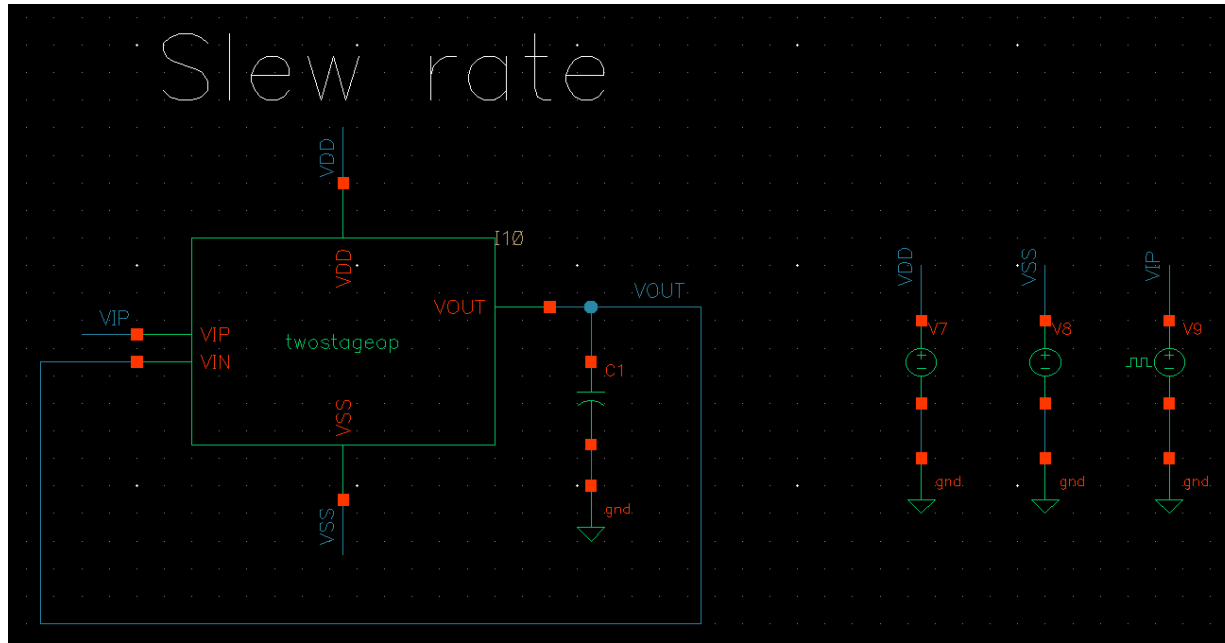


# Example – AC Response



# Example – Slew Rate

- 接成unit gain buffer
- 測量在rise時，vout的斜率



Edit Object Properties (on ws14.analog718.lab.nycu.edu.tw) x

Apply To  instance  Or

Show ☐ system ☒ user ☒ CDF

Property	Value	Display
Library Name	analoglib	off
Cell Name	vpu1se	off
View Name	symbol	off
Instance Name	V9	off

Change ☐ All ☐ User Property ☐ Ignore

Master Value	Local Value	Display
TRUE		off

CDF Parameter

Parameter	Value	Display
Frequency name for 1/period		off
Noise file name		off
Number of noise/freq pairs	0	off
DC voltage		off
AC magnitude		off
AC phase	0	off
XF magnitude		off
PAC magnitude		off
PAC phase		off
Voltage 1	500.0m V	off
Voltage 2	1.3 V	off
Period	10m s	off
Delay time	5m s	off
Rise time	1n s	off
Fall time	1n s	off
Pulse width	5m s	off
Temperature coefficient 1		off
Temperature coefficient 2		off
Nominal temperature		off
Type of rising & falling edge		off



# Example – Slew Rate

