Final Project - Two Stage OP

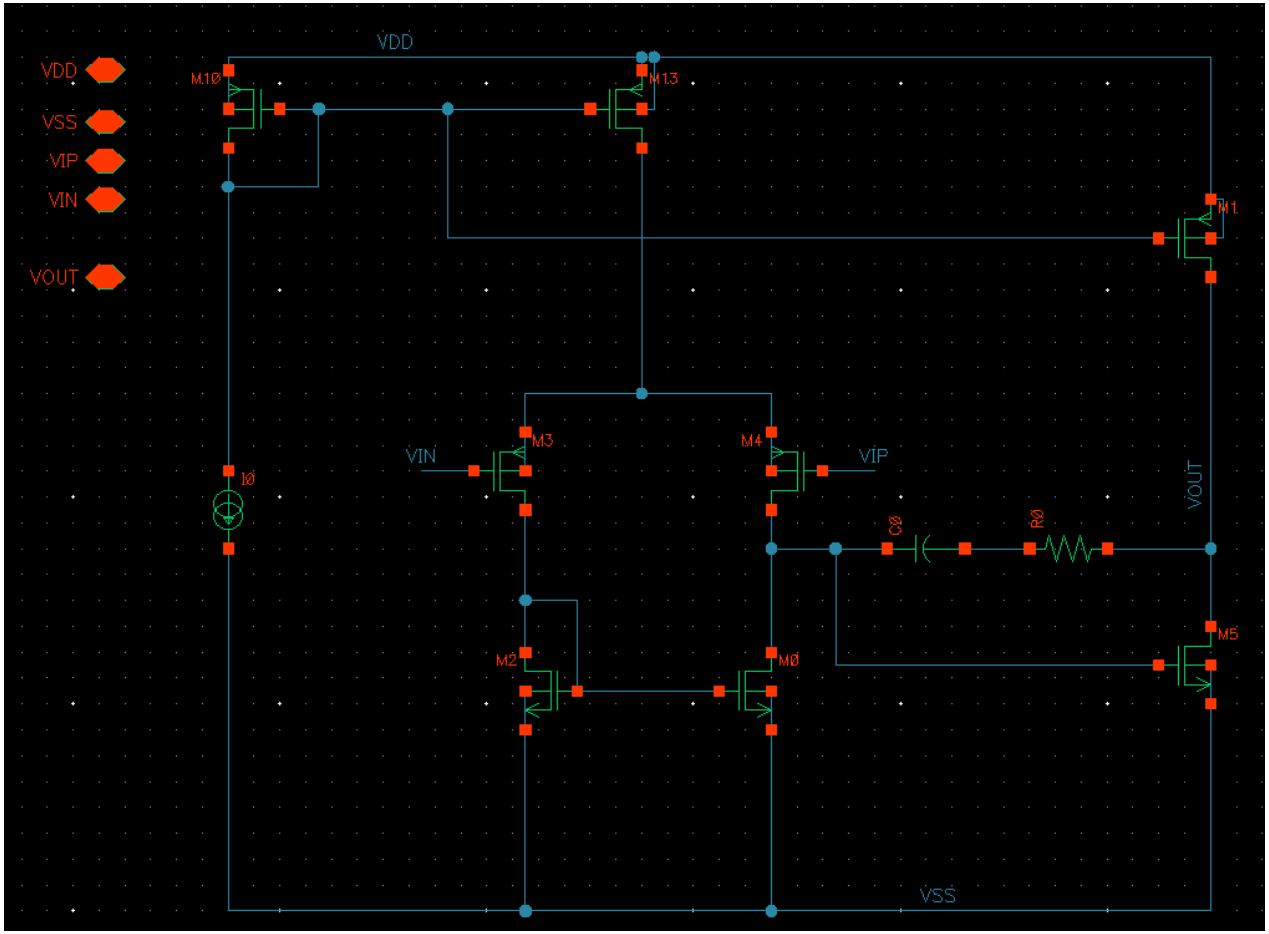
Design Flow

- Reference:
  - P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design," 2012
  - Chapter 6.3

6.3 Design of the Two-Stage Op Amp

  - You can finish the two stage OP Amp step by step

Schematic


VDD
VSS
VIP
VIN
VOUT
M10
M13
M1
M3
M4
VIN
VIP
I0
C0
R0
VOUT
M5
M2
M0
VSS

Spec

	SPEC	Unit
VDD	1.8	V
C_L	1	pF
DC Gain	> 70	dB
GBW	> 5	MHz
Phase Margin	≥ 60	degree
Slew Rate	> 5	V/μs
Power Dissipation	< 50	μW
FoM	$\frac{A_v(dB) \times GBW(MHz)}{P(mW)}$	The larger the better

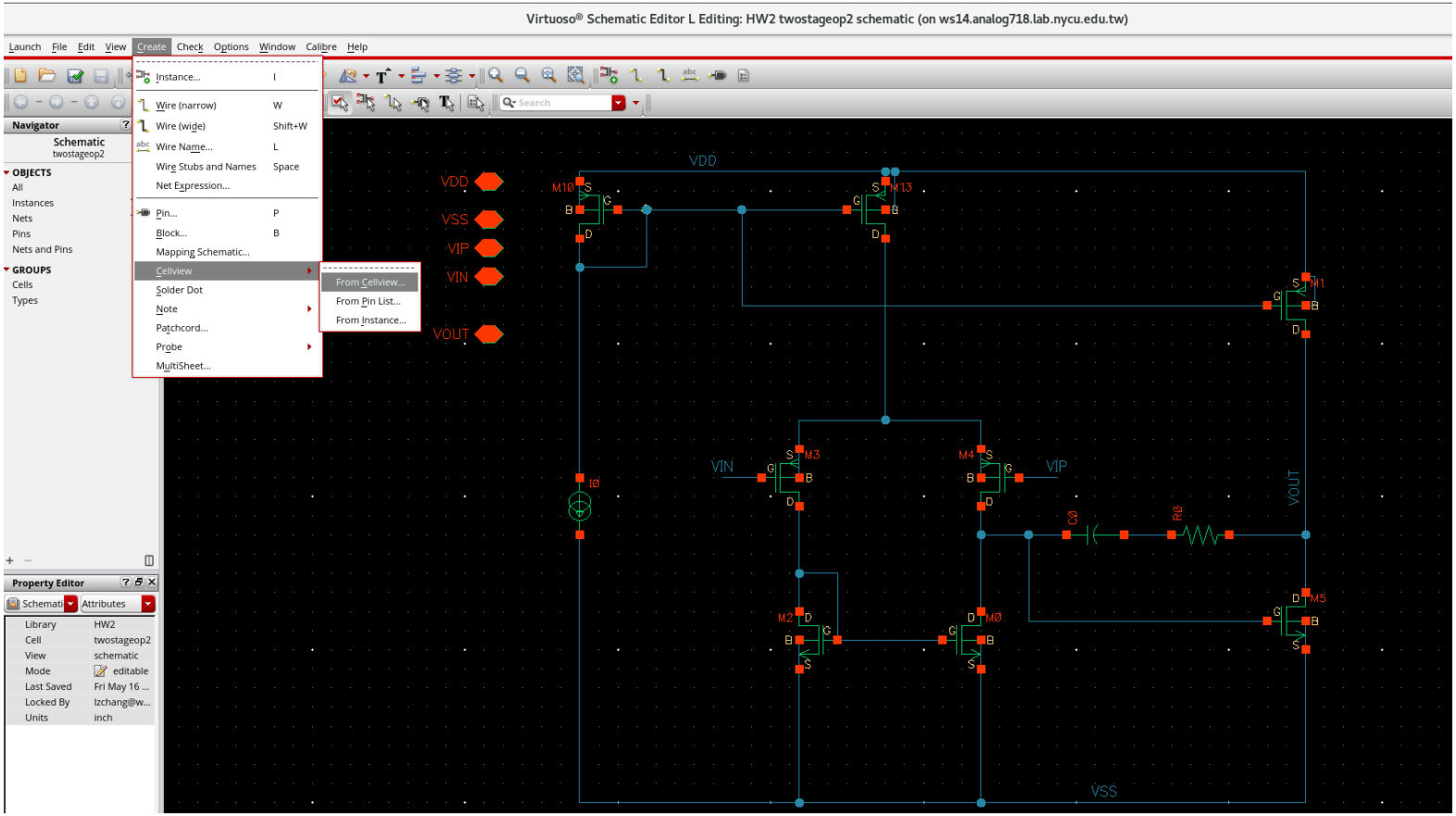
報告要求

- 報告中須包含設計流程，模擬結果須一併附上自己的觀察看法
- 報告中須包含performance table，如下

	SPEC	This Work	Unit
VDD	1.8	1.8	V
C_L	1	1	pF
DC Gain	> 70	89.9	dB
GBW	> 5	8.76	MHz
Phase Margin	≥ 60	64	degree
Slew Rate	> 5	6.98	V/μs
Power Dissipation	< 50	34.92	μW
FoM	$\frac{A_v(dB) \times GBW(MHz)}{P(\mu W)}$	22.55	The larger the better

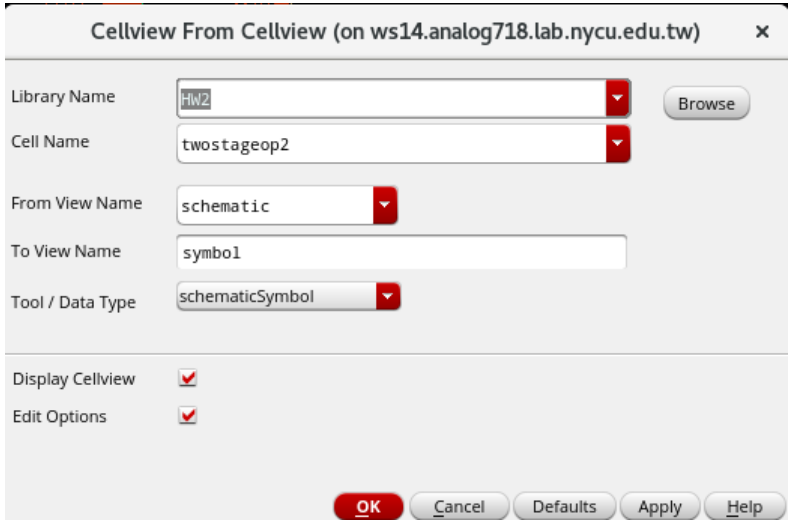
Appendix – 建立symbol

- Create – cellview – from cellview

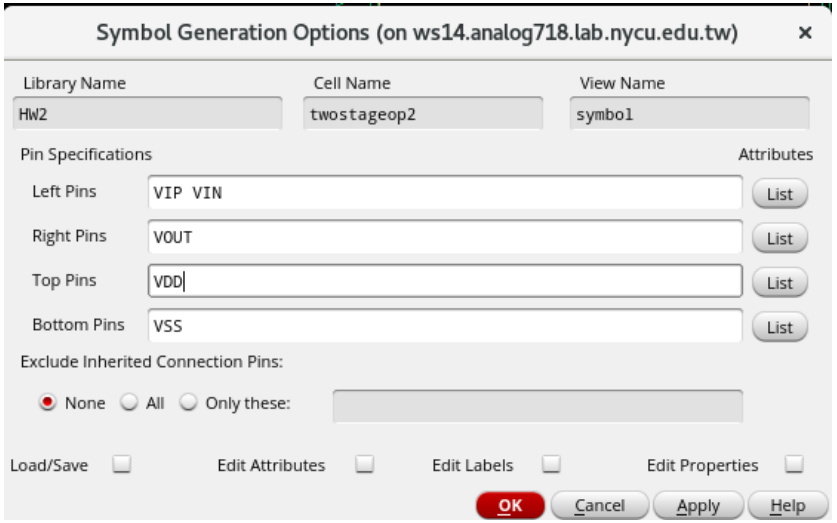


Appendix – 建立symbol

- 按ok

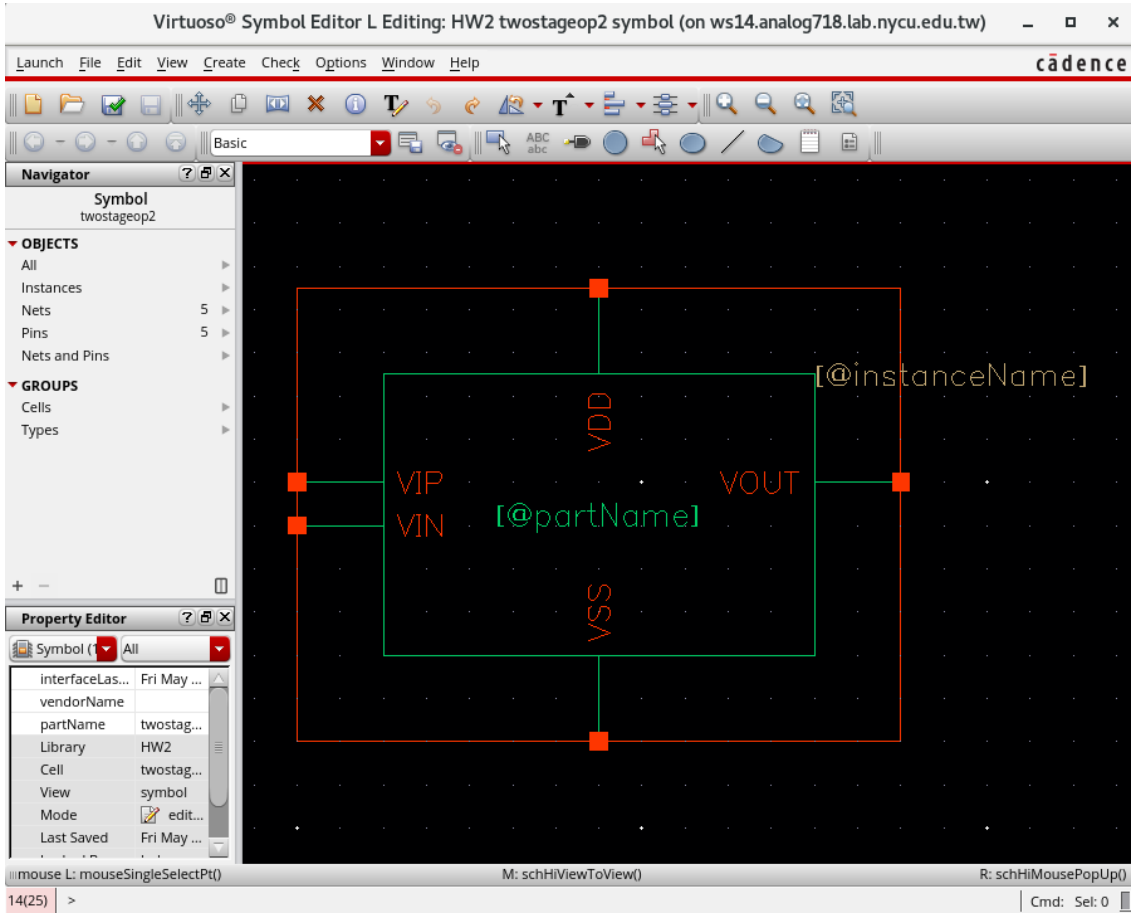


- 依照個人需求擺放PIN的位置



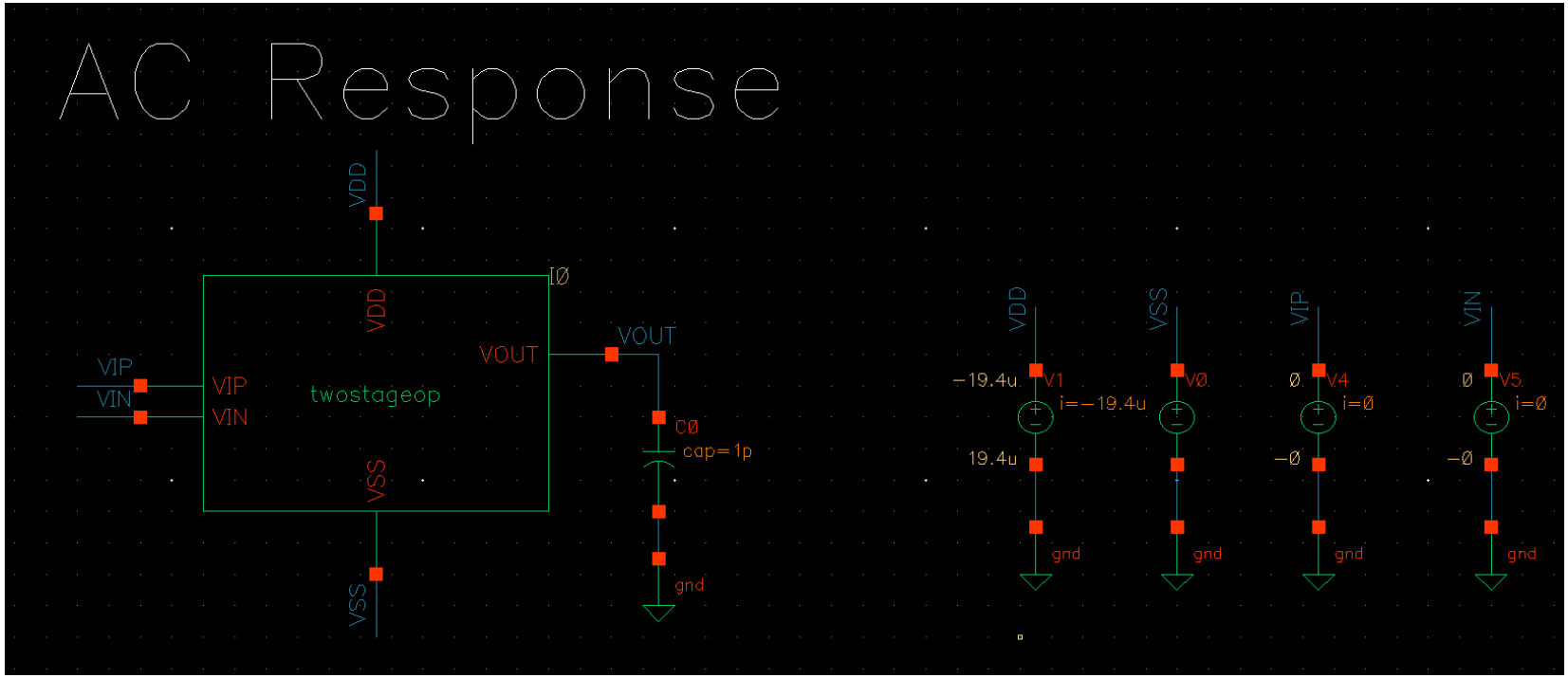
Appendix – 建立symbol

- 完成symbol，可直接關掉此視窗

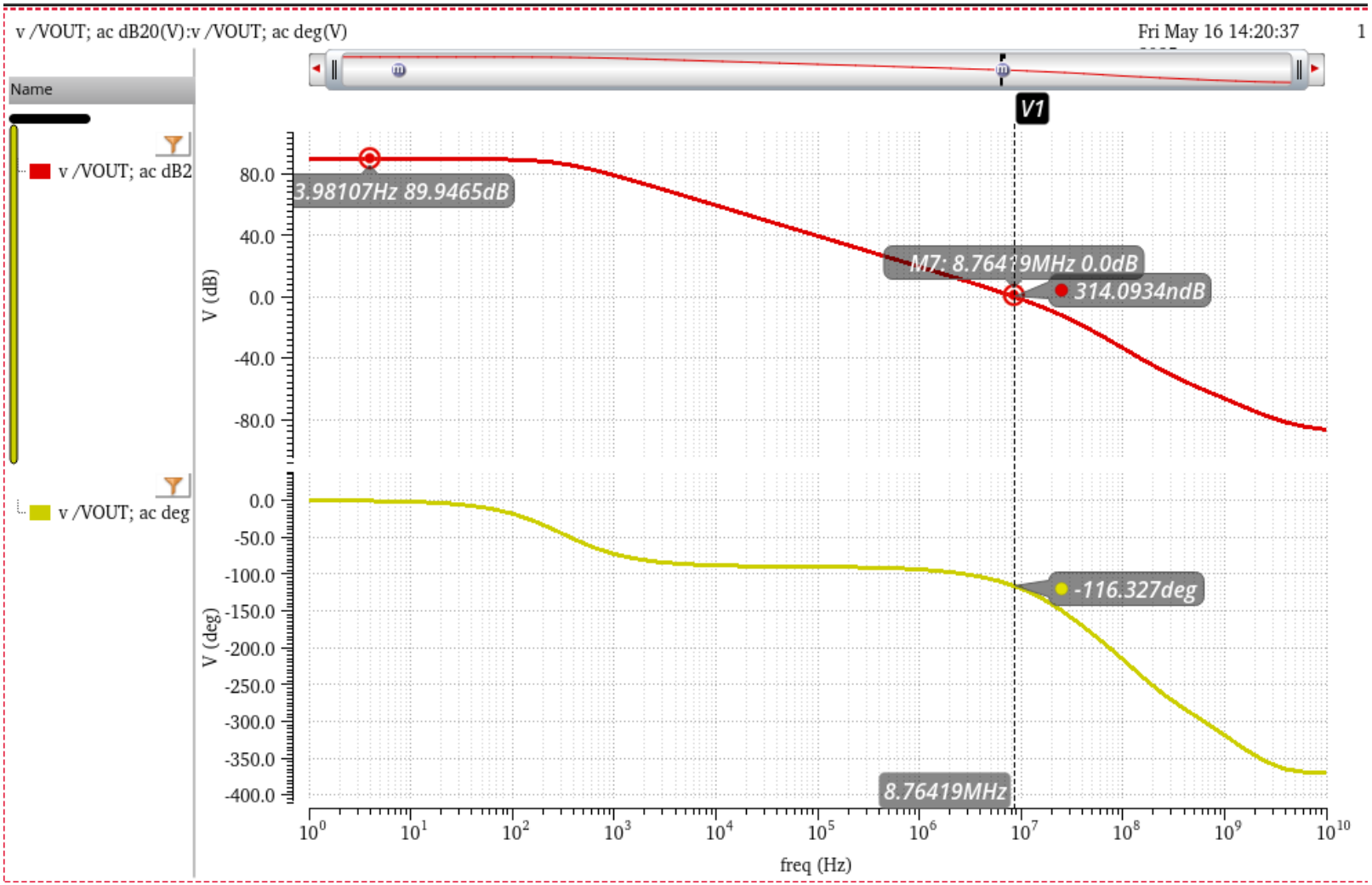


Appendix – testbench

- 新建一個schematic
- 用i叫出剛剛產生的symbol，接上各電位後，後續模擬步驟與先前作業相同(ADEL……)

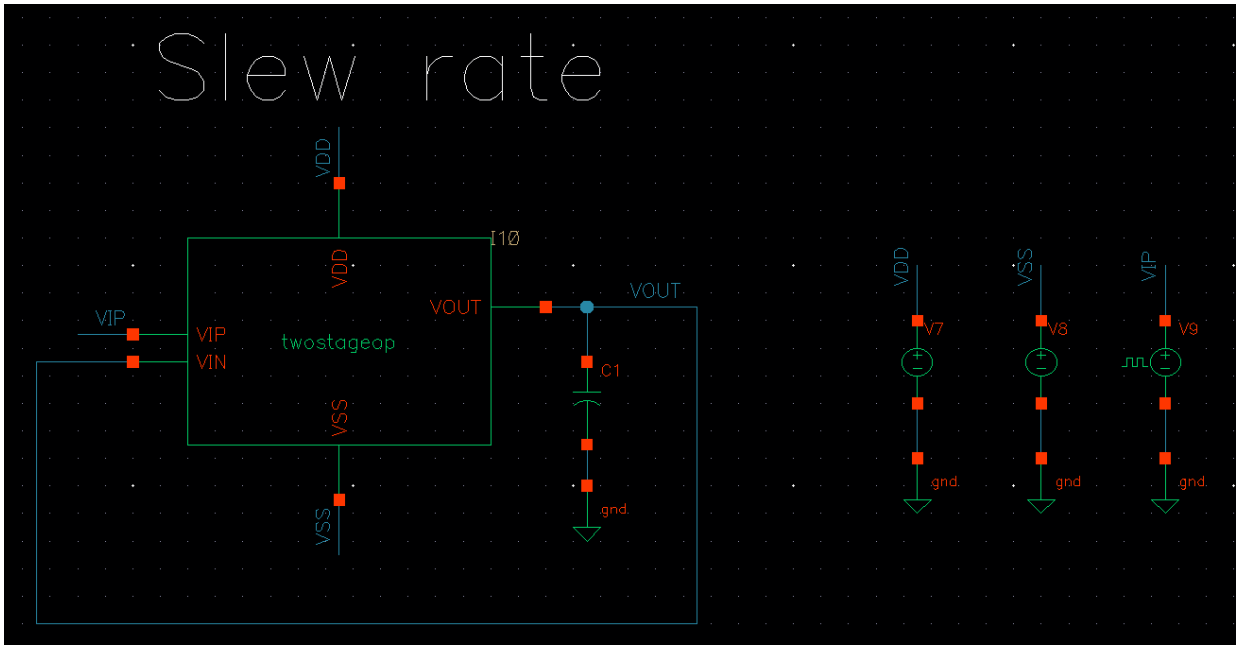


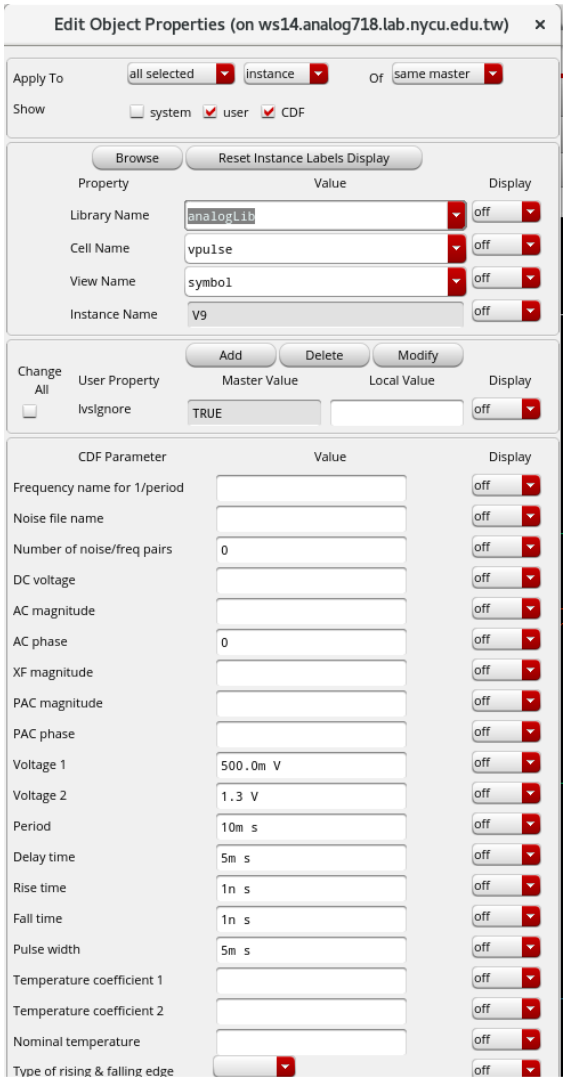
Example – AC Response



Example – Slew Rate

- 接成unit gain buffer
- 測量在rise時，vout的斜率





Example – Slew Rate