COL216

STAGE2

K LAXMAN

2018CS50408

- I Have used eda playground for simulation and running the code of vhdl and aldec Riviera pro 2020 simulator .

- This stage involves putting together the four modules designed at stage 1, namely ALU, Register File, Program Memory and Datat Memory, to form a simple processor which can execute the following subset of ARM instructions

- Though all the instructions of data processing are implemented in alu part previous assignment and I have implemented dt(data transfer) in dt.vhd now.

- I have implemented the program counter which updates the Program Counter on every clock by adding 4 and whenever the branch instruction is given it adds appropriate offset to the program counter.

- Files I have submitted are :
  Alu,program_mem,data_mem,register,program_counter,processor,decoder,myTypes,dt.vhd etc.
  Here processor contains the whole code of parts which has to be added for making a circuit with error free .