COL216 STAGE4

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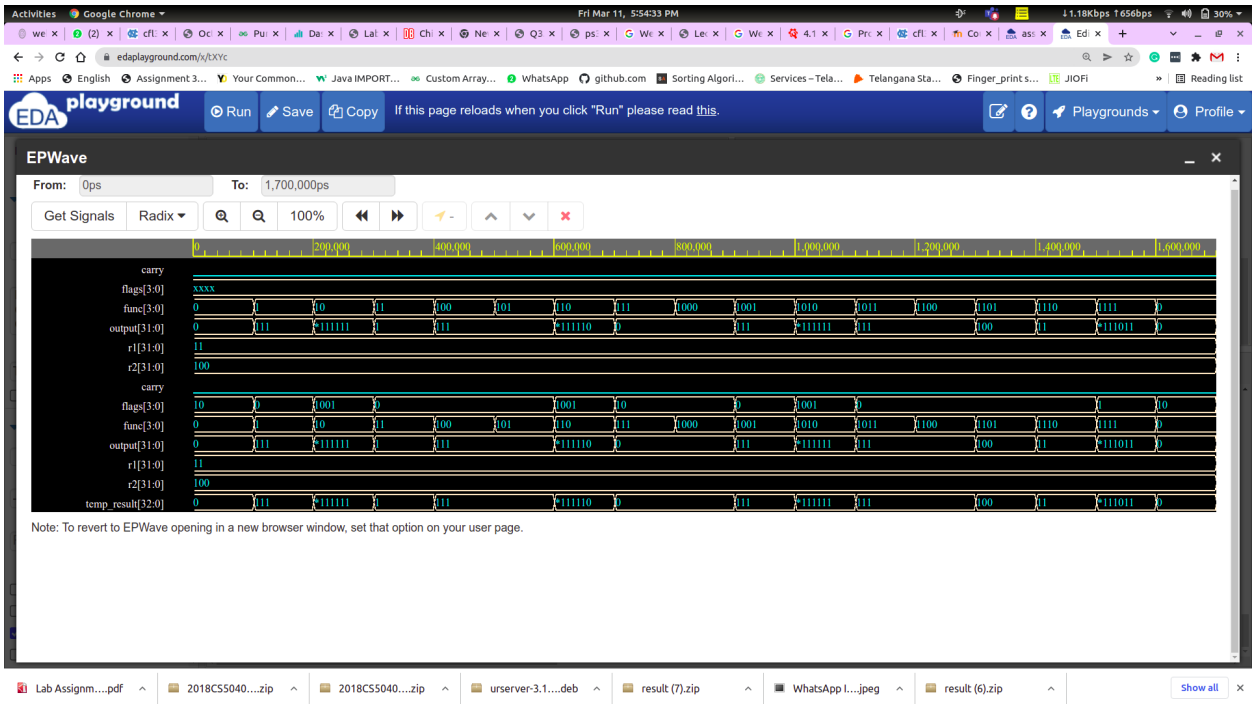
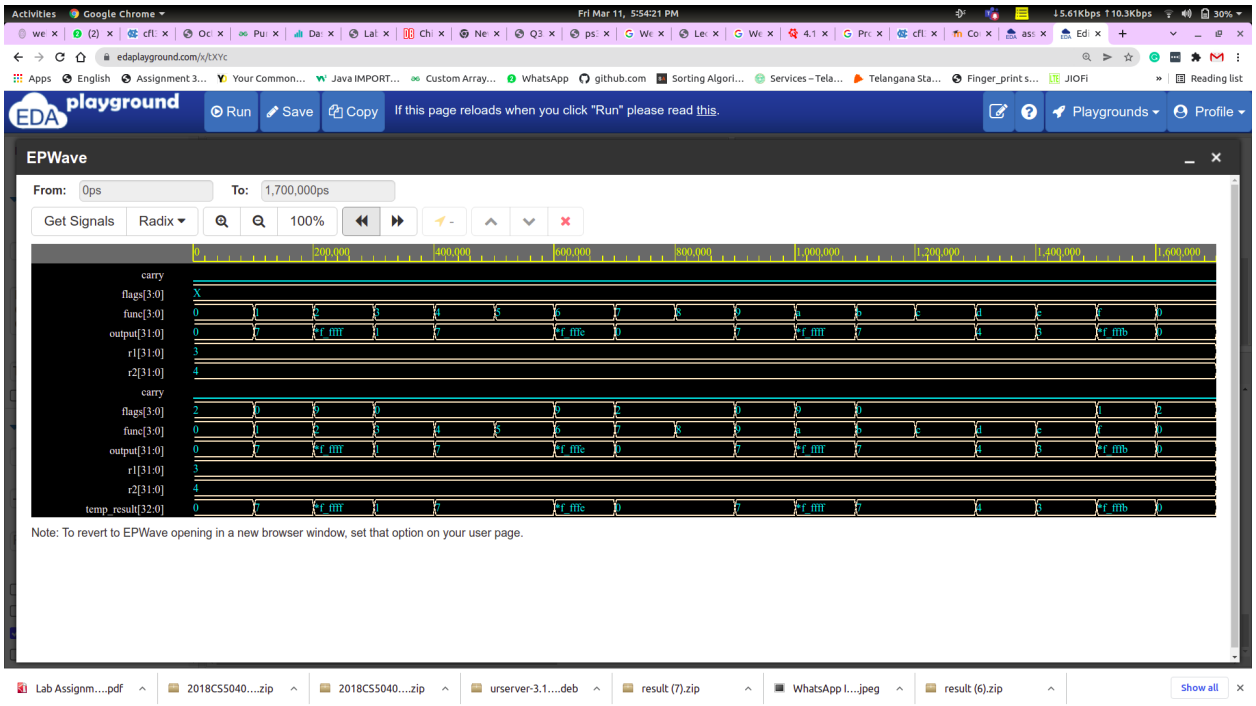
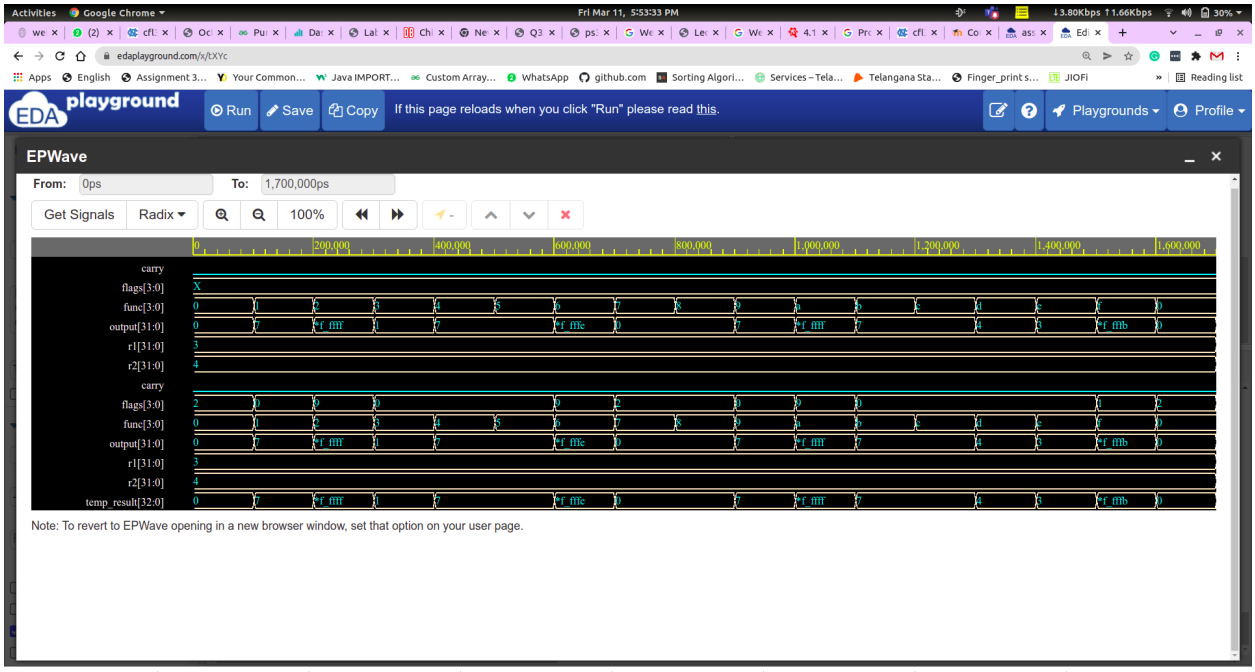
2018CS50408

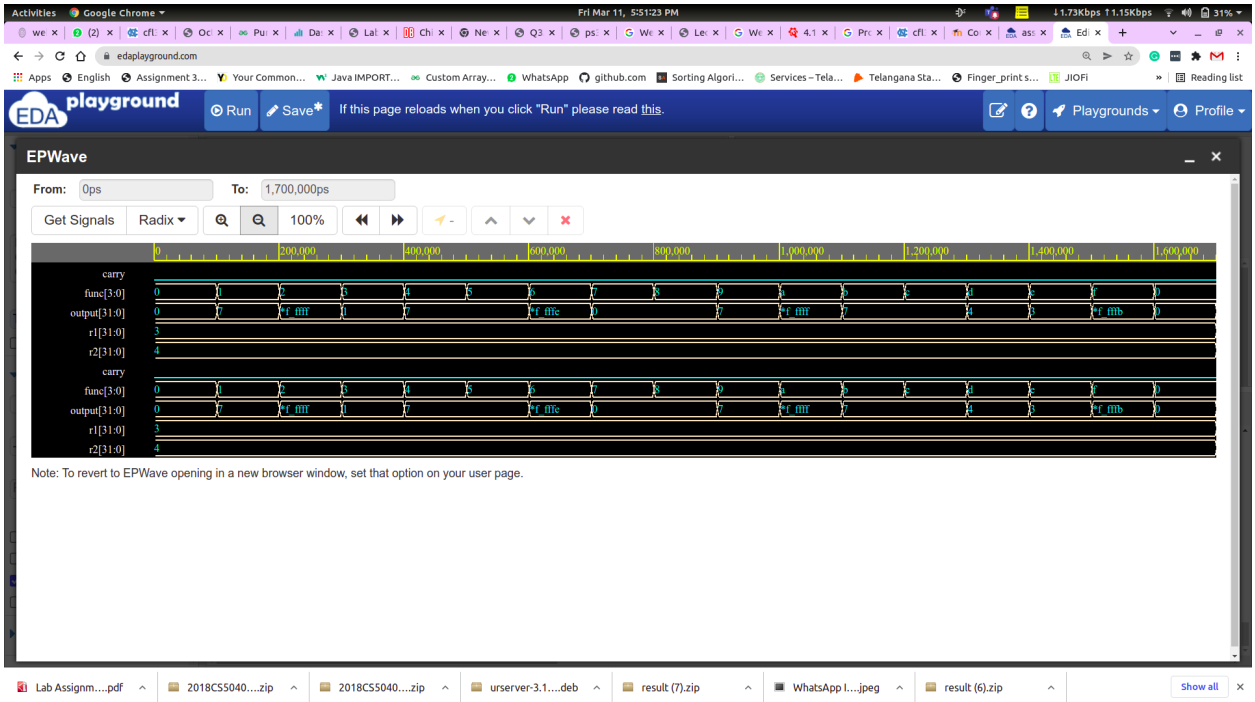
- I have used EDA playground for simulation and synthesis of the components.
- I have run all the components separately without zero errors
- All components are combined and it is free of errors
- I have successfully able to simulate the code and got the ep wave
- I have submitted 22 VHDL files in total they are 5 mux, Alu, Data register ,instruction register, program counter, temp registers,memory,flags ,immediate extension,register file etc.
- I have done the 4th part with the extension of the 3rd one and submitted the fully runnable code

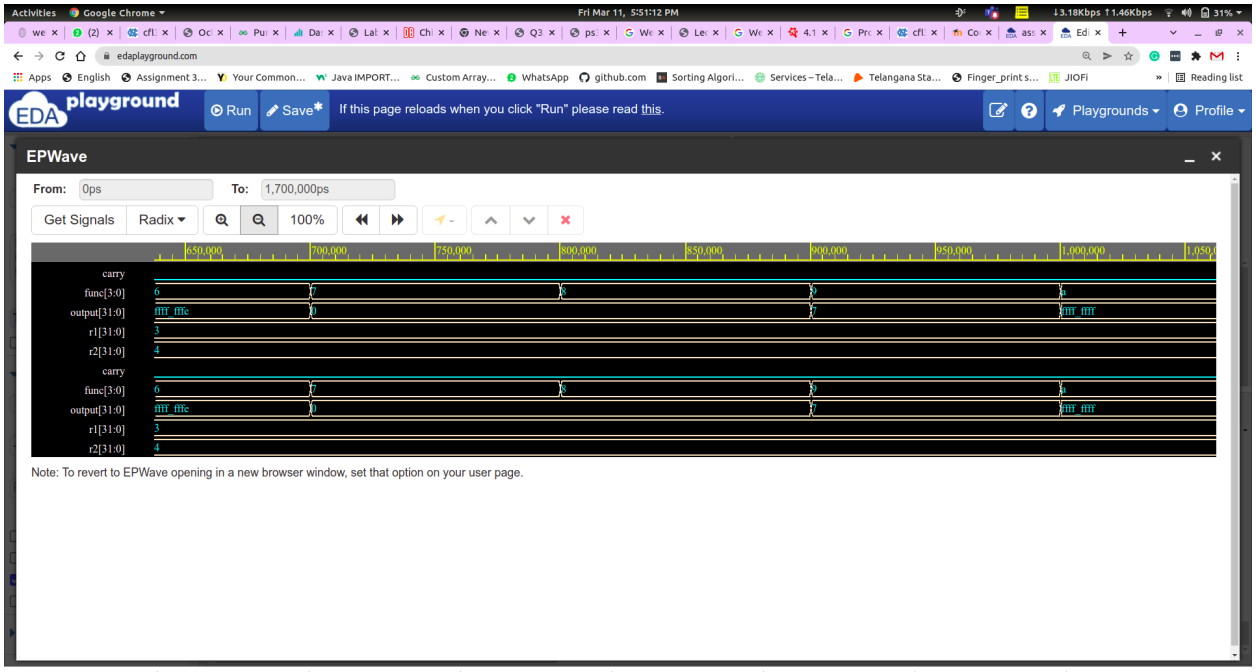
- I am hereby attaching the screenshots of the runnable code

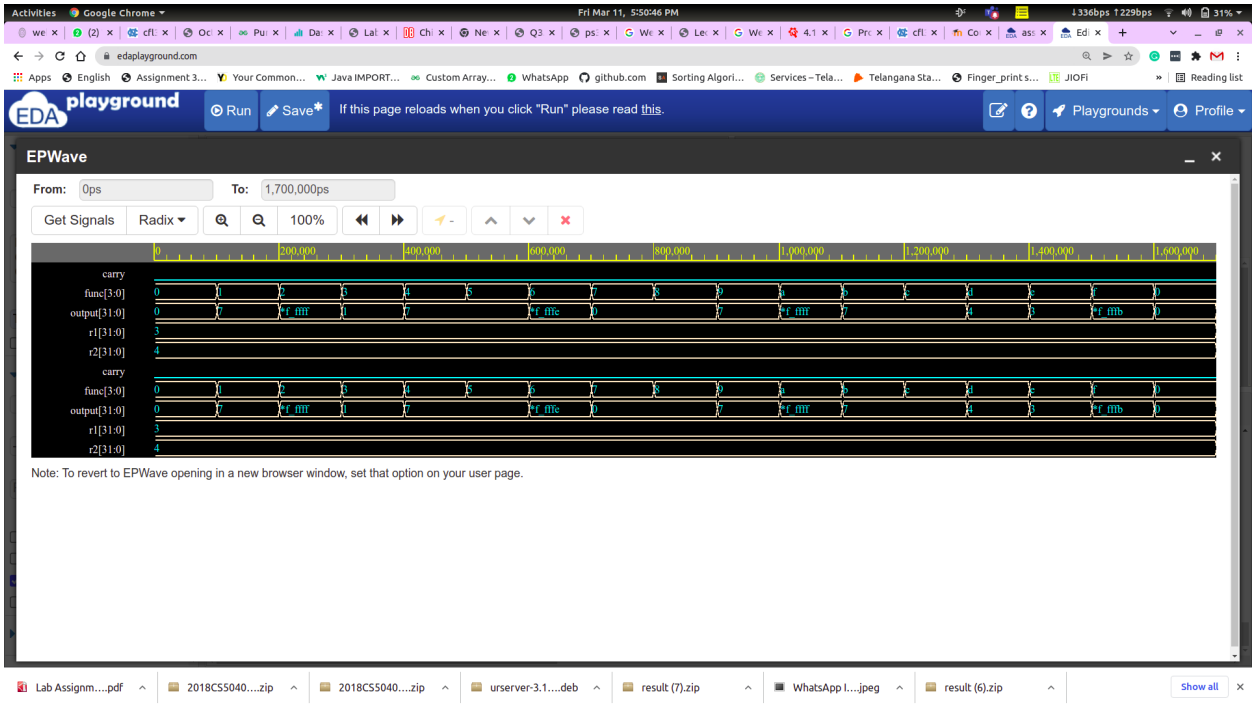


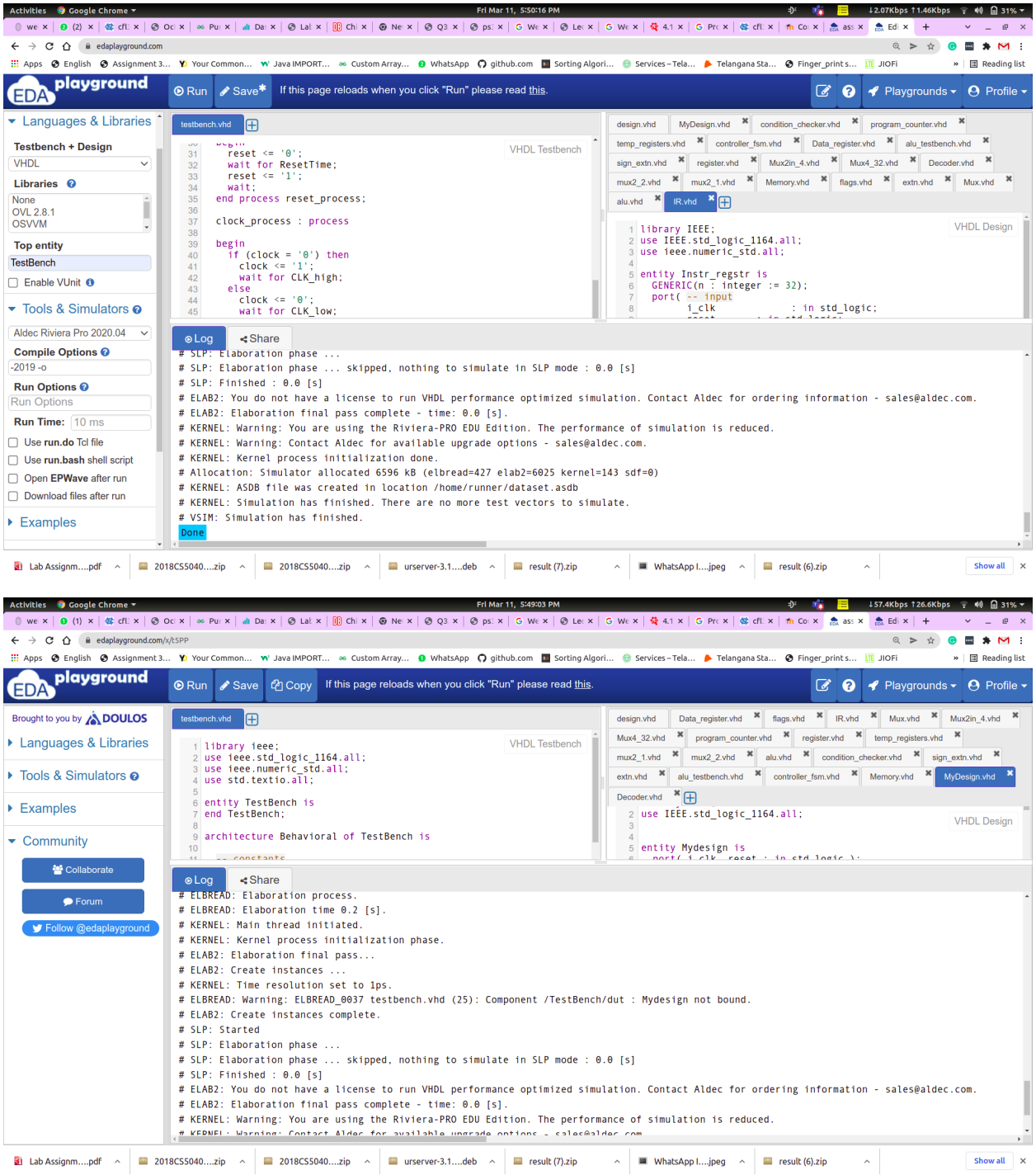



Activities
Google Chrome
Fri Mar 11, 5:53:33 PM
edaplayground.com/x/tXYc
EDA playground
Run
Save
Copy
If this page reloads when you click "Run" please read this.
Playgrounds
Profile
EPWave
From: 0ps
To: 1,700,000ps
Get Signals
Radix
100%
carry
flags[3:0]
func[3:0]
output[31:0]
r1[31:0]
r2[31:0]
temp_result[32:0]
Note: To revert to EPWave opening in a new browser window, set that option on your user page.
Lab Assignm....pdf
2018CS5040....zip
urserver-3.1....deb
result (7).zip
WhatsApp I....jpeg
result (6).zip
Show all


Activities
Google Chrome
Fri Mar 11, 5:51:23 PM
edaplayground.com
EDA playground
Run
Save*
If this page reloads when you click "Run" please read this.
Playgrounds
Profile
EPWave
From: 0ps
To: 1,700,000ps
Get Signals
Radix
100%
carry
func[3:0]
output[31:0]
r1[31:0]
r2[31:0]
Note: To revert to EPWave opening in a new browser window, set that option on your user page.
Lab Assignm....pdf
2018CS5040....zip
urserver-3.1....deb
result (7).zip
WhatsApp I....jpeg
result (6).zip
Show all


Activities
Google Chrome
Fri Mar 11, 5:51:12 PM
edaplayground.com
EDA playground
Run
Save*
If this page reloads when you click "Run" please read this.
Playgrounds
Profile
EPWave
From: 0ps
To: 1,700,000ps
Get Signals
Radix
100%
650,000
700,000
750,000
800,000
850,000
900,000
950,000
1,000,000
carry
func[3:0]
output[31:0]
r1[31:0]
r2[31:0]
Note: To revert to EPWave opening in a new browser window, set that option on your user page.
Lab Assignm....pdf
2018CS5040....zip
urserver-3.1....deb
result (7).zip
WhatsApp I....jpeg
result (6).zip
Show all


Activities
Google Chrome
Fri Mar 11, 5:50:46 PM
edaplayground.com
EDA playground
Run
Save*
If this page reloads when you click "Run" please read this.
Playgrounds
Profile
EPWave
From: 0ps
To: 1,700,000ps
Get Signals
Radix
100%
0
200,000
400,000
600,000
800,000
1,000,000
1,200,000
1,400,000
1,600,000
carry
func[3:0]
output[31:0]
r1[31:0]
r2[31:0]
Note: To revert to EPWave opening in a new browser window, set that option on your user page.
Lab Assignm....pdf
2018CS5040....zip
urserver-3.1....deb
result (7).zip
WhatsApp I....jpeg
result (6).zip
Show all


Activities
Google Chrome
Fri Mar 11, 5:50:16 PM
edaplayground.com
EDA playground
Run
Save*
If this page reloads when you click "Run" please read this.
Playgrounds
Profile
Languages & Libraries
Testbench + Design
VHDL
Libraries
None
OVL 2.8.1
OSVVM
Top entity
TestBench
Enable VUnit
Tools & Simulators
Aldec Riviera Pro 2020.04
Compile Options
-2019 -o
Run Options
Run Options
Run Time:
10 ms
Use run.do Tcl file
Use run.bash shell script
Open EPWave after run
Download files after run
Examples
testbench.vhd
VHDL Testbench
reset <= '0';
wait for ResetTime;
reset <= '1';
wait;
end process reset_process;
clock_process : process
begin
if (clock = '0') then
clock <= '1';
wait for CLK_high;
else
clock <= '0';
wait for CLK_low;
design.vhd
MyDesign.vhd
condition_checker.vhd
program_counter.vhd
temp_registers.vhd
controller_fsm.vhd
Data_register.vhd
alu_testbench.vhd
sign_extn.vhd
register.vhd
Mux2in_4.vhd
Mux4_32.vhd
Decoder.vhd
mux2_2.vhd
mux2_1.vhd
Memory.vhd
flags.vhd
extn.vhd
Mux.vhd
alu.vhd
IR.vhd
VHDL Design
library IEEE;
use IEEE.std_logic_1164.all;
use ieee.numeric_std.all;
entity Instr_regstr is
GENERIC(n : integer := 32);
port(-- input
i_clk : in std_logic;
Log
Share
SLP: Elaboration phase ...
SLP: Elaboration phase ... skipped, nothing to simulate in SLP mode : 0.0 [s]
SLP: Finished : 0.0 [s]
ELAB2: You do not have a license to run VHDL performance optimized simulation. Contact Aldec for ordering information - sales@aldec.com.
ELAB2: Elaboration final pass complete - time: 0.0 [s].
KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is reduced.
KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
KERNEL: Kernel process initialization done.
Allocation: Simulator allocated 6596 kB (elbread=427 elab2=6025 kernel=143 sdf=0)
KERNEL: ASDB file was created in location /home/runner/dataset.asdb
KERNEL: Simulation has finished. There are no more test vectors to simulate.
VSIM: Simulation has finished.
Done
Lab Assignm....pdf
2018CS5040....zip
2018CS5040....zip
urserver-3.1....deb
result (7).zip
WhatsApp I....jpeg
result (6).zip
Show all

Activities
Google Chrome
Fri Mar 11, 5:49:03 PM
edaplayground.com/x/t5PP
EDA playground
Run
Save
Copy
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Playgrounds
Profile
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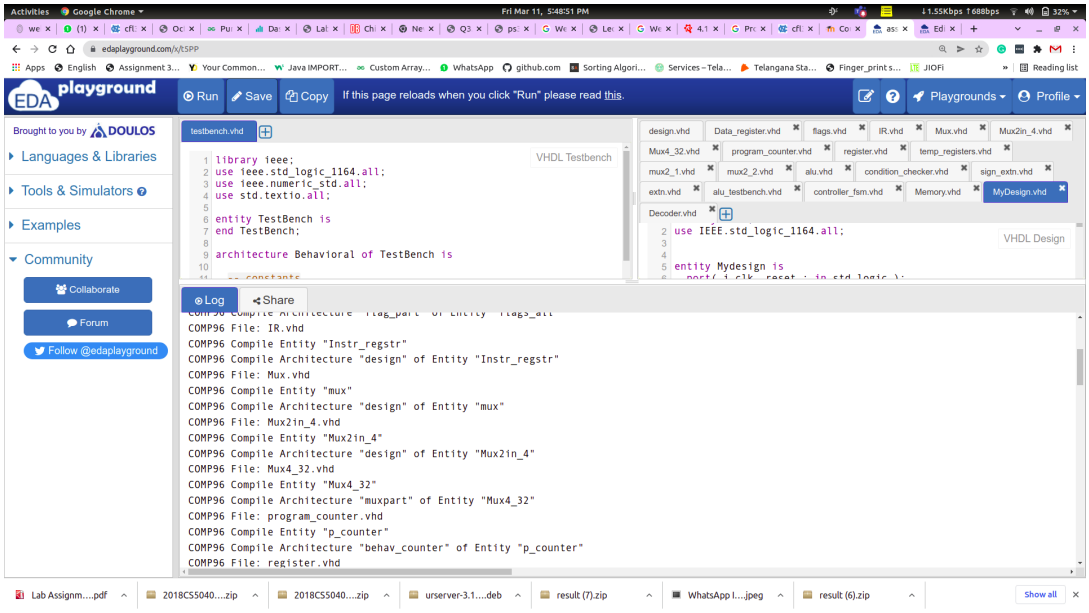
Languages & Libraries
Tools & Simulators
Examples
Community
Collaborate
Forum
Follow @edaplayground
testbench.vhd
VHDL Testbench
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use std.textio.all;
entity TestBench is
end TestBench;
architecture Behavioral of TestBench is
design.vhd
Data_register.vhd
flags.vhd
IR.vhd
Mux.vhd
Mux2in_4.vhd
Mux4_32.vhd
program_counter.vhd
register.vhd
temp_registers.vhd
mux2_1.vhd
mux2_2.vhd
alu.vhd
condition_checker.vhd
sign_extn.vhd
extn.vhd
alu_testbench.vhd
controller_fsm.vhd
Memory.vhd
MyDesign.vhd
Decoder.vhd
VHDL Design
use IEEE.std_logic_1164.all;
entity Mydesign is
Log
Share
ELBREAD: Elaboration process.
ELBREAD: Elaboration time 0.2 [s].
KERNEL: Main thread initiated.
KERNEL: Kernel process initialization phase.
ELAB2: Elaboration final pass...
ELAB2: Create instances ...
KERNEL: Time resolution set to 1ps.
ELBREAD: Warning: ELBREAD_0037 testbench.vhd (25): Component /TestBench/dut : Mydesign not bound.
ELAB2: Create instances complete.
SLP: Started
SLP: Elaboration phase ...
SLP: Elaboration phase ... skipped, nothing to simulate in SLP mode : 0.0 [s]
SLP: Finished : 0.0 [s]
ELAB2: You do not have a license to run VHDL performance optimized simulation. Contact Aldec for ordering information - sales@aldec.com.
ELAB2: Elaboration final pass complete - time: 0.0 [s].
KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is reduced.
Lab Assignm....pdf
2018CS5040....zip
2018CS5040....zip
urserver-3.1....deb
result (7).zip
WhatsApp I....jpeg
result (6).zip
Show all


Activities
Google Chrome
Fri Mar 11, 5:48:51 PM
edaplayground.com/x/tSPP
EDA playground
Run
Save
Copy
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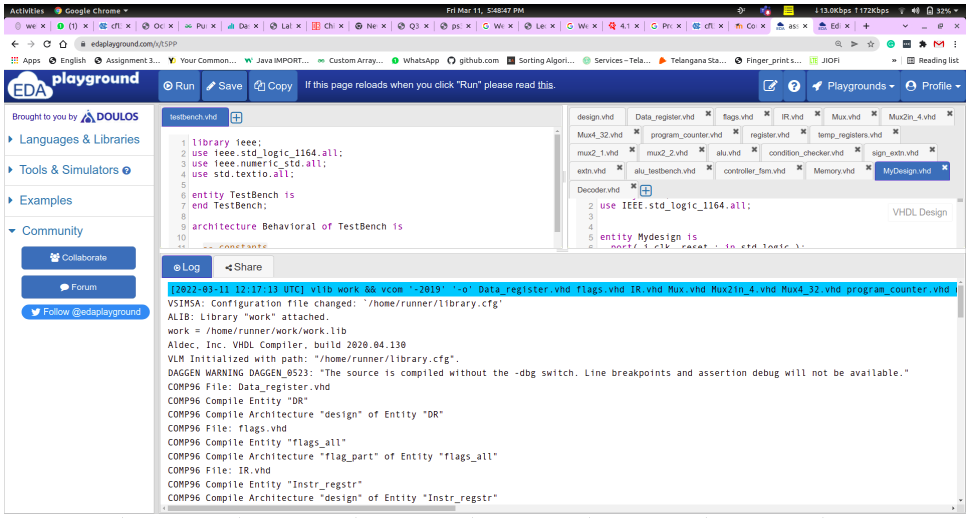
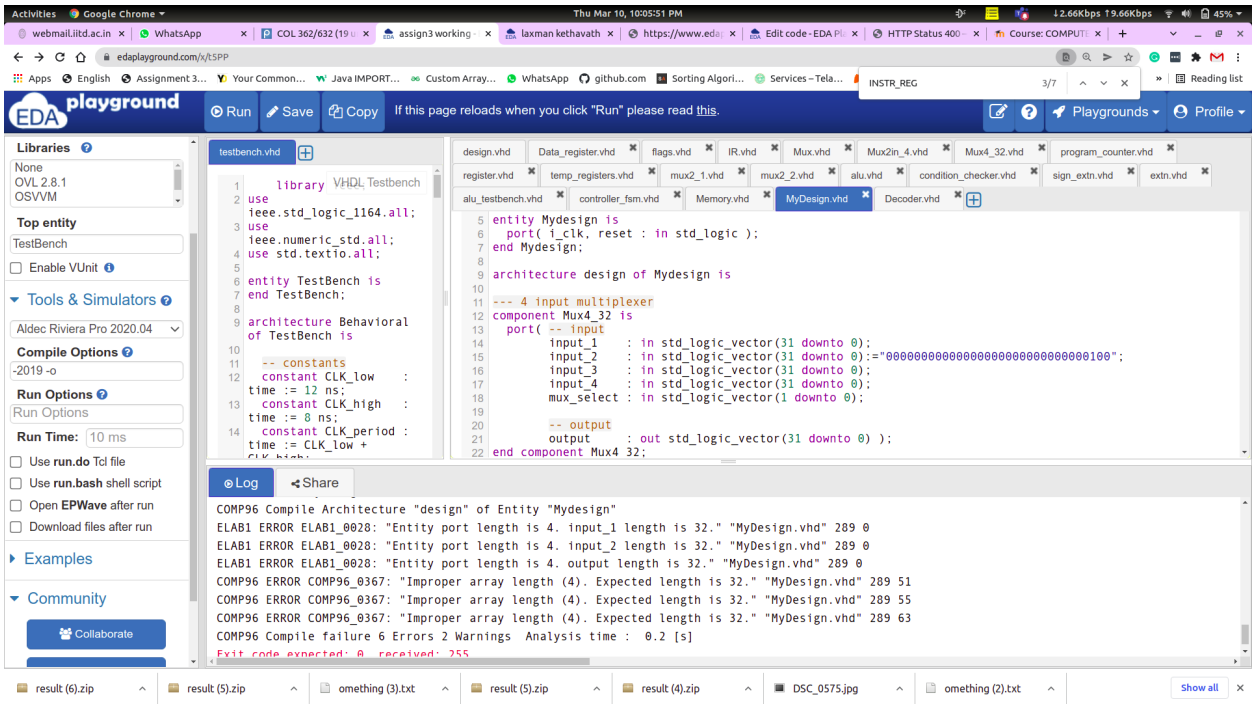
Tools & Simulators
Examples
Community
Collaborate
Forum
Follow @edaplayground
testbench.vhd
VHDL Testbench
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use std.textio.all;
entity TestBench is
end TestBench;
architecture Behavioral of TestBench is
design.vhd
Data_register.vhd
flags.vhd
IR.vhd
Mux.vhd
Mux2in_4.vhd
Mux4_32.vhd
program_counter.vhd
register.vhd
temp_registers.vhd
mux2_1.vhd
mux2_2.vhd
alu.vhd
condition_checker.vhd
sign_extn.vhd
extn.vhd
alu_testbench.vhd
controller_fsm.vhd
Memory.vhd
MyDesign.vhd
Decoder.vhd
VHDL Design
use IEEE.std_logic_1164.all;
entity Mydesign is
Log
Share
COMP96 File: IR.vhd
COMP96 Compile Entity "Instr_regstr"
COMP96 Compile Architecture "design" of Entity "Instr_regstr"
COMP96 File: Mux.vhd
COMP96 Compile Entity "mux"
COMP96 Compile Architecture "design" of Entity "mux"
COMP96 File: Mux2in_4.vhd
COMP96 Compile Entity "Mux2in_4"
COMP96 Compile Architecture "design" of Entity "Mux2in_4"
COMP96 File: Mux4_32.vhd
COMP96 Compile Entity "Mux4_32"
COMP96 Compile Architecture "muxpart" of Entity "Mux4_32"
COMP96 File: program_counter.vhd
COMP96 Compile Entity "p_counter"
COMP96 Compile Architecture "behav_counter" of Entity "p_counter"
COMP96 File: register.vhd
Lab Assignm....pdf
2018CS5040....zip
2018CS5040....zip
urserver-3.1....deb
result (7).zip
WhatsApp I....jpeg
result (6).zip
Show all


playground
Run
Save
Copy
If this page reloads when you click "Run" please read this.
Playgrounds
Profile
testbench.vhd
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use std.textio.all;
entity TestBench is
end TestBench;
architecture Behavioral of TestBench is
Log
Share
[2022-03-11 12:17:13 UTC] vlib work && vcom '-2019' '-o' Data_register.vhd flags.vhd IR.vhd Mux.vhd Mux2in_4.vhd Mux4_32.vhd program_counter.vhd
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
Aldec, Inc. VHDL Compiler, build 2020.04.130
VLM Initialized with path: "/home/runner/library.cfg".
DAGGEN WARNING DAGGEN_0523: "The source is compiled without the -dbg switch. Line breakpoints and assertion debug will not be available."
COMP96 File: Data_register.vhd
COMP96 Compile Entity "DR"
COMP96 Compile Architecture "design" of Entity "DR"
COMP96 File: flags.vhd
COMP96 Compile Entity "flags_all"
COMP96 Compile Architecture "flag_part" of Entity "flags_all"
COMP96 File: IR.vhd
COMP96 Compile Entity "Instr_regstr"
COMP96 Compile Architecture "design" of Entity "Instr_regstr"


playground
Run
Save
Copy
If this page reloads when you click "Run" please read this.
Playgrounds
Profile
INSTR_REG
Libraries
Top entity
TestBench
Enable VUnit
Tools & Simulators
Aldec Riviera Pro 2020.04
Compile Options
-2019 -o
Run Options
Run Time:
Examples
Community
Collaborate
testbench.vhd
entity Mydesign is
port(i_clk, reset : in std_logic);
end Mydesign;
architecture design of Mydesign is
--- 4 input multiplexer
component Mux4_32 is
Log
Share
COMP96 Compile Architecture "design" of Entity "Mydesign"
ELAB1 ERROR ELAB1_0028: "Entity port length is 4. input_1 length is 32." "MyDesign.vhd" 289 0
ELAB1 ERROR ELAB1_0028: "Entity port length is 4. input_2 length is 32." "MyDesign.vhd" 289 0
ELAB1 ERROR ELAB1_0028: "Entity port length is 4. output length is 32." "MyDesign.vhd" 289 0
COMP96 ERROR COMP96_0367: "Improper array length (4). Expected length is 32." "MyDesign.vhd" 289 51
COMP96 ERROR COMP96_0367: "Improper array length (4). Expected length is 32." "MyDesign.vhd" 289 55
COMP96 ERROR COMP96_0367: "Improper array length (4). Expected length is 32." "MyDesign.vhd" 289 63
COMP96 Compile failure 6 Errors 2 Warnings Analysis time : 0.2 [s]