COL216 ASSIGNMENT 2

STAGE 1

K Laxman

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- I have used edaplayground to simulate the code
- The Files which I have submitted are first one is design.vhd and second is testbench.vhd
    - alu and test alu_testbench
    - register and reg_testbench
    - program-mem and prog_testbench
    - data_mem.vhd

    total of 7 files and one report file .

    My files are simulating and error free

    Mainly in alu part I have implemented the whole opcode operations too.