# COL216 STAGE 3

# REPORT

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- I have used eda playground in this stage for simulation and synthesis

- I have implemented multi cycle path here with total 18 components which consists all the parts of the cycle design and another MY Design ,test bench for running the whole code with respective to the triggered clock

- As shown in the figure of multi cycle path I have implemented glue logic as MyDesign.vhd which contains all the glue logic(multiplexers, control logic) and controlFsm .

- I have submitted 20 vhdl files in total they are 5 mux,Alu,Data register, instruction register, program counter, temp registers,meory,flags ,immediate extension,register file