CSE331 – Computer Organization

Project #02 Report

This is the report for second project of GTU - Computer Organization lecture, Fall2017. Homework and report written by Deniz Can Erdem Yılmaz - 151044001

shiftModule

Input(s): shiftData[31:0], shiftAmount[4:0], funct[5:0]

Output(s): outData[31:0]

This module takes a 32-bit data to shift. Shift amount determined by 5-bit input. Three kinds of shift operation is supported. SRA (shift right arithmetic), SRL (shift right logic), SLL (shift left logic) determined by the 6-bit funct input. Result will be assigned 32-bit outData output.

ALU

Input(s): inpData1[31:0], inpData2[31:0], funct[5:0]

Output(s): outData[31:0]

This module simulates an ALU (arithmetic-logic unit). Takes two 32-bit inputs (inpData1, inpData2) and calculates the result. Six operation is supported by thi ALU. Addition (add), unsigned addition (addu), subtruction (sub), and, or, set-less-than-unsigned (sltu) determined by the 6-bit funct input. Result will be assigned 32-bit outData output.

mips_registers

Input(s): read_reg_1[4:0], read_reg_2[4:0], write_reg[4:0], signal_reg_write, clk

Output(s): read_data_1[31:0], read_data_2[31:0], write_data[31:0]

This module has given inside the project template. It holds 32 32-bit registers to simulate MIPS register block. Register content read from file named “register.mem”. Inputs read_reg_1 and read_reg_2 reads register contents and assigns to read_data_1 and read_data_2. If clk is on rising edge and signal_reg_write is 1, write_data will be written to register[write_reg].

mips_core

Input(s): instruction[31:0]

Output(s): result[31:0]

This module also has given inside the project template. This is the top level entity, takes an 32-bit instruction as input and operates it. This simulation of MIPS supports only 9 R-Type instructions (add, addu, sub, and, or, sra, srl, sll, sltu). Result will written into 32-bit result output.

Test Benches

All of modules have test bench to test them. Each have different amount of tests to see if every functionality works without an error.

—Here is a sketch to show my intent and preparation for the project: