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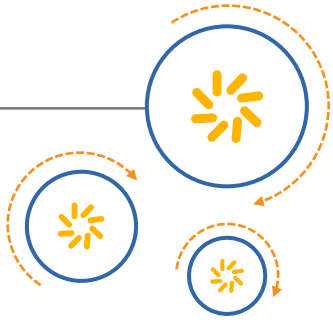

IPQ4019/IPQ4029 AP.DK04 Reference Design

Hardware Reference Guide

80-Y9700-5 Rev. K

March 20, 2017

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Revision history

Revision	Date	Description
A	September 2015	Initial release
B	November 2015	▪ Updated 1.1 Additional references ▪ Updated 3.18 GPIO ▪ Updated Table 3-23 DDR3 DRAM design guidelines ▪ Updated 4.4 Power sequencing ▪ Added 5.3 PWB construction ▪ Updated 6.1.6 5 GHz external power amplifier ▪ Updated 6.2.8 Additional guidelines ▪ Added 6.3 Antenna placement on the AP ▪ Added A Performance Characteristics
C	December 2015	Updated for AP.DK04.3 ▪ Section 1.1: Added design package for AP.DK04.3. ▪ Section 2.1: Added supported DDR memory size for AP.DK04.3.
D	January 2016	▪ Section 1.1 Additional references: updated design packages ▪ Section 2.1 AP.DK04 block diagram: updated clock frequency and SD card reader ▪ Section 3.2 Reset: updated CHIP_RST_OUT description in Table 3 4 IPQ4019/IPQ4029 reset signals ▪ Section 3.16 DDR3L DRAM: added spacing to Table 3-23 DDR3 DRAM design guidelines; added DDR_A_14 and DDR_A_15 to Table 3-24 Internal length of chip − DDR3L DRAM. ▪ Section 7.3 Power: updated Figure 7-4 QCA8075 power supply ▪ Section A Performance Characteristics: updated A.1 EVM limitation, A.2 Tx power, and A.3 Rx sensitivity
E	January 2016	Added section 6.1.10 Board designs with on-chip 2.4 GHz-only Wi-Fi, section 6.1.11 DC regulator for AVDD11_2G and AVDD11_5G power supply, and section A.2 Tx power
F	January 2016	Updated section 8.1 Stackup
G	April 2016	▪ Section 3.16 DDR3L DRAM: added DDR_CS_N[0] to Table 3-24 Internal length of chip − DDR3L DRAM ▪ Section 7.1 Reset: updated 3.3 V rising duration
H	May 2016	CPU frequency changed to 716.8 MHz DDR frequency changed to 672 MHz Updated 7.7 Layout guidelines
J	December 2016	Sedated Section 1.1, Additional References
K	March 2017	Updated 3.13 VoIP

Contents

Figures

Tables

1 Overview

This document is a generic design guideline for board designs based on the IPQ4019/IPQ4029 single chip AP solution. It is based on development boards and reference designs implemented with this SoC.

This document is an aid to the design and should be supplemented by thorough reviews with the Qualcomm Technologies customer engineering team before and during any board design effort.

For clarity, this document makes reference to and describes the interfaces of the IPQ4019/IPQ4029 device where required.

1.1 Additional references

Reference design HDKs and documentation should be consulted and reviewed before implementing board design. Additionally, details of the interface implementations may require reference to the corresponding standards specifications of those interfaces and device data sheets of connected devices.

For topics that are not addressed in this document, see:

Doc number	Title
80-Y9347-19	*IPQ4019 Access Point SoC Preliminary Device Specification*
80-Y9347-29	*IPQ4029 Access Point SoC Preliminary Device Specification*
80-Y9112-1	*QCA8075 Five-Port 10/100/1000 Mbps Ethernet Transceiver Preliminary Device Specification*
80-Y0619-4	*QCA8337N Seven-port Gigabit Ethernet Switch Data Sheet*
DP25-Y9761-112	*Design Package, IPQ4019.AP.DK04.1, DAKOTA 1.0 2X2 DBDC 11AC XPA(HP) XLNA 5GE 1PCIE 2USB EMMC/SD LCD RET BGA, Full Build*
DP25-Y9761-213	*Design Package, IPQ4029.AP.DK04.2, DAKOTA 1.0 2X2 DBDC 11AC XPA(HP) XLNA 5GE 1PCIE 2USB EMMC/SD LCD ENT BGA, Full Build*

2 AP.DK04 Overview

AP.DK04 is a low to medium end AP reference design. The AP.DK04 reference design has the following chip solution:

The IPQ4019/IPQ4029 is a highly integrated system-on-chip (SoC) designed for high-performance, power efficient, and cost-effective 2×2, 802.11ac, dual-band concurrent access-point applications. The SoC incorporates a quad-core ARM Cortex A7 processor, two dual-band, concurrent 802.11ac Wave-2 Wi-Fi subsystems, and a five-port Gigabit Ethernet Layer2/3/4 multilayer switch supporting hardware network address translation (NAT). It supports one USB3.0 and one USB2.0.It also supports miscellaneous interfaces such as SD/eMMC card reader, PCIe 2.0, I²S, PCM, SPDIF, I²C, SMI, UART, JTAG, etc., which can be configured as general-purpose I/O pins

QCA8075 Ethernet transceiver is a five-port, 10/100/1000 Mbps tri-speed Ethernet PHY. The QCA8075 Ethernet transceiver provides physical layer functions for half/full-duplex 10BASE-Te, 100BASE-TX, and full-duplex 1000BASE-T Ethernet to transmit and receive data over standard Category 5 (CAT-5) unshielded twisted-pair cable. QCA8075 is connected to the PSGMII interface of IPQ4019/IPQ4029.

2.1 AP.DK04 block diagram

The AP.DK04 reference design consists of the following functional blocks:

- IPQ4019/IPQ4029 has a quad-core ARM Cortex A7 processor that operates at a clock frequency of 716.8 MHz, 32 KB instruction cache, and 32 KB data cache per core, 256 KB L2 cache (shared)
- IPQ4019/IPQ4029 on-chip dual-band concurrent (DBDC) 2×2 2.4 GHz 802.11n (256QAM) and 2×2 5 GHz 802.11ac, two dedicated CPUs for Wi-Fi offloading and feature growth. Cooperates with RFMD/SKY front-end chips.
- A QCA8075 five-port, 10/100/1000 Mbps tri-speed Ethernet PHY connected to the PSGMII of IPQ4018/IPQ4028, to provide LAN/WAN network connectivity.
- One USB3.0 connector and one USB2.0 connector that operate in the host mode.
- The AP.DK04 reference design comprises of four memory components:
  - Single 16 MByte SPI NOR Flash
  - 16-bit maximum of 256 MByte (AP.DK04.1 and AP.DK04.2) and 512 MByte (AP.DK04.3) capacity low-power DDR3 memory, implemented in a single rank configuration running at 672 MHz clock speed and 1344 MT/s data rate
  - Parallel NAND Flash 1 Gbit (128 M x 8 bit)
  - eMMC/SD

- DC/DC switching regulators to provide the different DC voltage levels for main chip usage
- Single 48 MHz crystal for IPQ4019/IPQ4029
- SD card reader slot, support SD card, eMMC to MMC+ card
- LCD port supports MIPI DBI type-B (Intel 8080 mode)
- Touch Panel with I²C0 touch-panel controller
- Audio interfaces support both input and output for I²S/TDM/SPDIF
- WCI interface (Wi-Fi LTE co-exist)
- JTAG interface, UART (2-wire) for CPU debugging and HS-UART(4-wire) for Bluetooth
- LEDs
- PCIe mini 2.0 slot
- Support PCM and SPI for VoIP

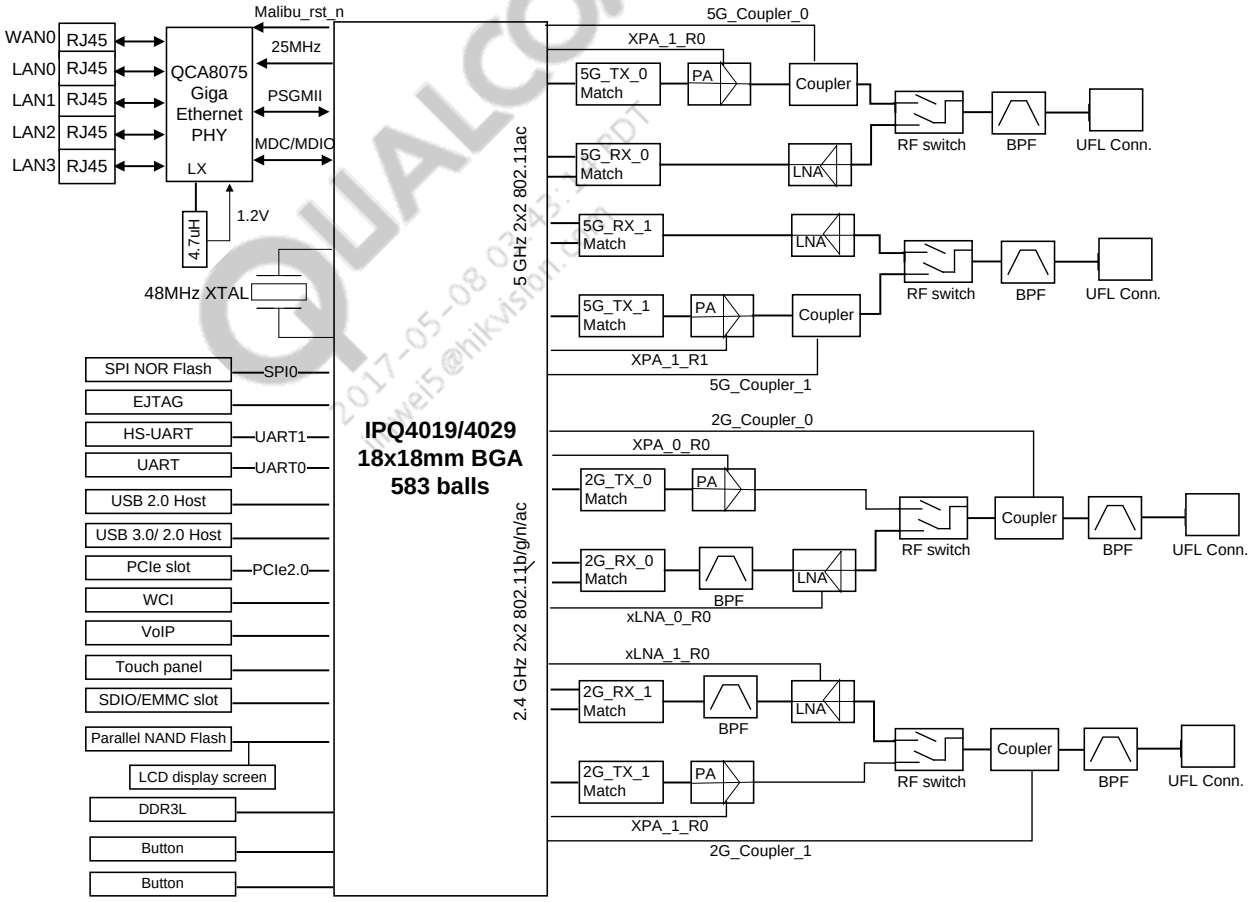


Figure 2-1 AP.DK04 block diagram

3 Board Design Guidelines

3.1 Clock

The IPQ4019/IPQ4029 device can operate with a single 48 MHz crystal clock reference. The crystal part number is CX2016DB48000E0DLFA1 from Kyocera. Adhere to the guidelines in this chapter for the critical interface shown in Figure 3-1.

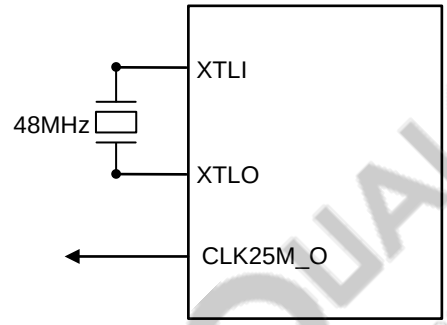


Figure 3-1 IPQ4019/IPQ4029 clock diagram

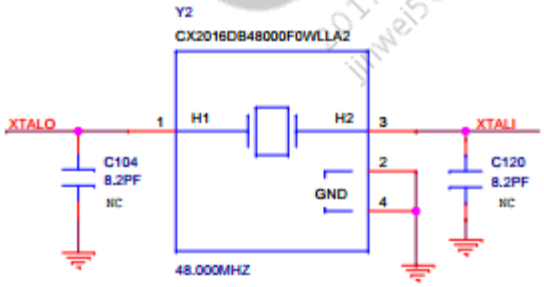
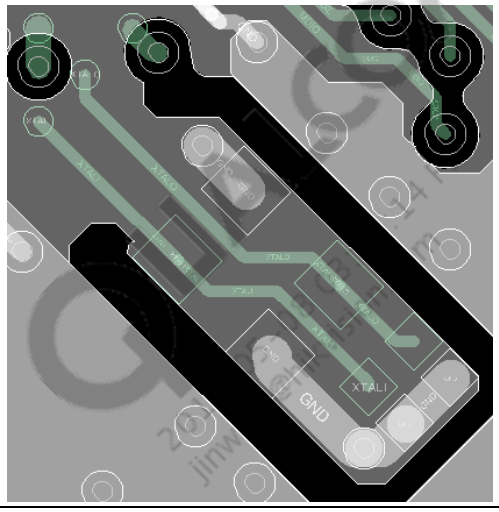
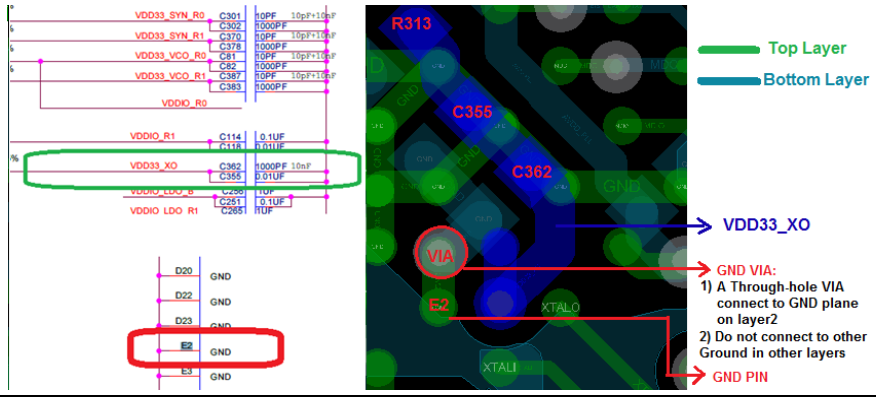


Figure 3-2 Schematic implementation

Table 3-1 IPQ4019/IPQ4029 crystal clock connection pins

Pin ID	Pin name	Description and guideline
E1	XTALI	Crystal clock connection pins
F1	XTALO	

Table 3-2 Crystal schematic guidelines

Category	Guideline
Component	48 MHz crystal Use a fundamental mode crystal of 20 ppm accuracy. An SMD package is recommended.
Placement	If the routing precludes the crystal from being placed close to the IPQ4019/IPQ4029 on the top side with sufficient isolation, it is acceptable to place the crystal on the bottom side. Place the tuning capacitors close to the crystal and place the shunt element without any stub in the path as shown in the reference.
Spacing	Maintain >2 w spacing for these traces. An isolated GND pour is recommended around the crystal that nets to a GND moat below it.
Moating	Moat the GND shape around the crystal. Include the crystal and its associate components within the moat and run the separation around this block. No other signal via should transit this moat and no other GND connection should be made into it. Merge the moat to the main GND under the IPQ4019/IPQ4029 as shown: 
Routing	Route wide short traces from the crystal pins to the IPQ4019/IPQ4029.
Ground	Isolate GND connection for pin E2 and decouple capacitor on pin F2(VDD33_XO) ▪ A through-hole VIA connect to GND plane on layer2 ▪ Do not connect to others GND pins of IPQ4019/IPQ4029 and GND pad of decoupling capacitors in other layers 

The IPQ4019/IPQ4029 device generates a 25 MHz clock output, which is used for external Ethernet PHY.

Table 3-3 IPQ4019/IPQ4029 clock pins

Pin ID	Pin name	Description and guideline
AF27	CLK_25M_OUT	25 MHz clock output at 1.1 V. This clock can be used to feed external Ethernet device. Maintain a separation (2 W) from neighboring traces. Recommend to provide for a series damping resistor at the source pin (populated with 0 Ω) and reserve one 10 pf parallel cap to GND

3.2 Reset

The IPQ4019/IPQ4029 reset signals should be handled as shown in Table 3-4.

Table 3-4 IPQ4019/IPQ4029 reset signals

Pin ID	Pin name	Description and guideline
A16	CHIP_PWD_L	Fundamental reset input Recommend that RC circuit is 10 K pull-up with 1 µF pull-down.
M1	CHIP_RST_OUT	System reset out from IPQ4019/IPQ4029, used to reset peripheral device such as flash. Low pulse from this pin is about 10 µs. To get longer low pulse, choose other unoccupied GPIO to simulate as reset signal.

3.3 Boot configuration straps

At power-up, the IPQ4019/IPQ4029 device reconfigures several GPIO pins as input to sense boot configuration settings. The configuration settings are latched before the IPQ4019/IPQ4029 releases CHIP_RST_OUT output.

The configuration straps are described in the device documentation; see the device specification for more details. All options listed therein may not be supported in reference design and software releases.

Table 3-5 IPQ4019/IPQ4029 boot configuration pins

Pin ID	Pin name boot_config[n]	Alternate function	Type	Function description
U26	10	GPIO56	I	Mode ▪ 0 = Native mode ▪ 1 = Test mode
A18	0	GPIO3	I	Apps authentication Enable. Enables authentication for various AP code segments. Send to security control ▪ 0 = No authentication ▪ 1 = Enable authentication
K3 V25	1 7	GPIO14 GPIO51	I	▪ 00 <GPIO51:14> = Boot interface is SPI ▪ 01 <GPIO51:14>= Boot interface is eMMC ▪ 10 <GPIO51:14>= Boot interface is QPIC ▪ 11<GPIO51:14> = Boot from USB
AB24	3	GPIO36	I	▪ 0 = Boot from code RAM ▪ 1 = Boot from ROM
N24	11	GPIO62	I	JTAG enable: ▪ 0 = GPIO0 to GPIO5 are normal GPIO. Can be configured by the FUN_SEL registers ▪ 1 = GPIO0 to GPIO5 are used as JTAG interface. Cannot be changed by the FUN_SEL registers
AB25 AB26	4 5	GPIO37 GPIO38	I	APPS PBL boot speed (APSS PLL) ▪ 00 <GPIO38:37> = XO clock – 48 MHz ▪ 01 <GPIO38:37>= FE_PLL clock – 200 MHz ▪ 10 <GPIO38:37>= FE_PLL clock – 500 MHz ▪ 11 <GPIO38:37>= Reserved
P26	12	GPIO69	I	Select ROM PK hash index source ▪ 0 = From QC eFuse ▪ 1 = From OEM eFuse
U25	9	GPIO55	I	▪ 0 = Normal boot ▪ 1 = Force boot from USB
AG10	2	GPIO33	I	Use Serial Number for secure boot authentication ▪ 0 = Use Serial Number ▪ 1 = Use OEM ID
L1	6	GPIO15	I	Watchdog_enable ▪ 0 = Watchdog disable ▪ 1 = Watchdog enable

1. Schematic implementation as recommended. Their recommended value for pull-up or pull-down is 4.7 K with the appropriate components.
2. GPIO pull-up voltage depends on its power domain. For example, if power domain is 1.8 V, GPIO should pull up to 1.8 V.

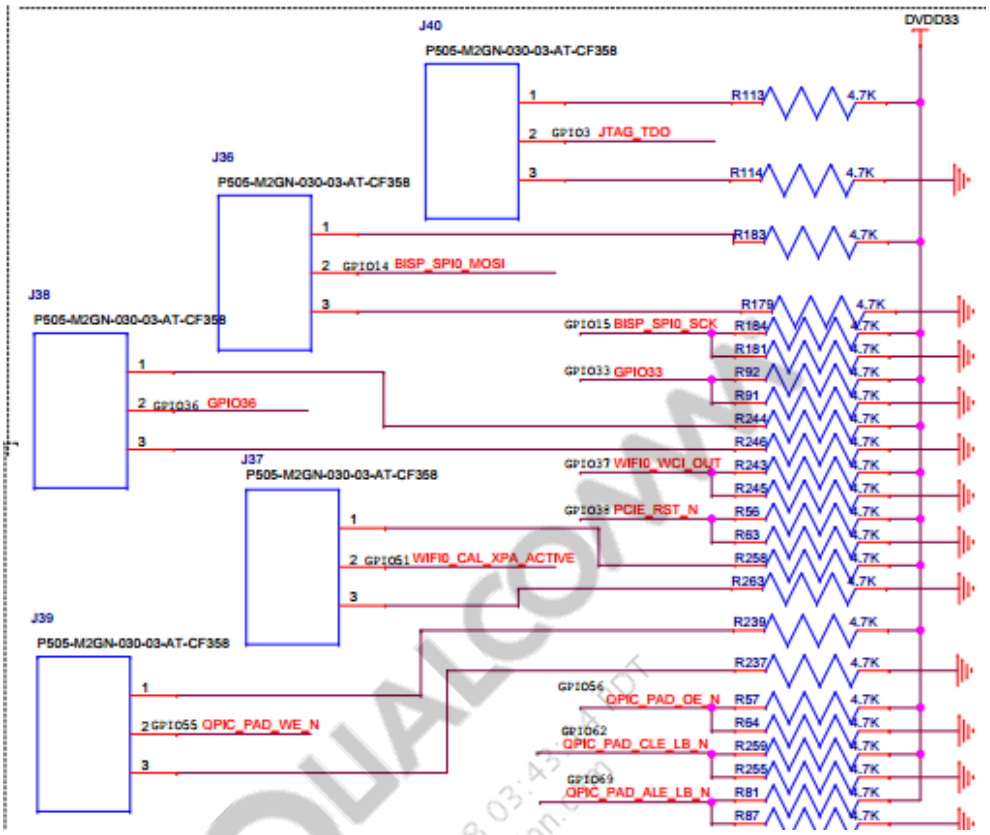


Figure 3-3 Power strapping

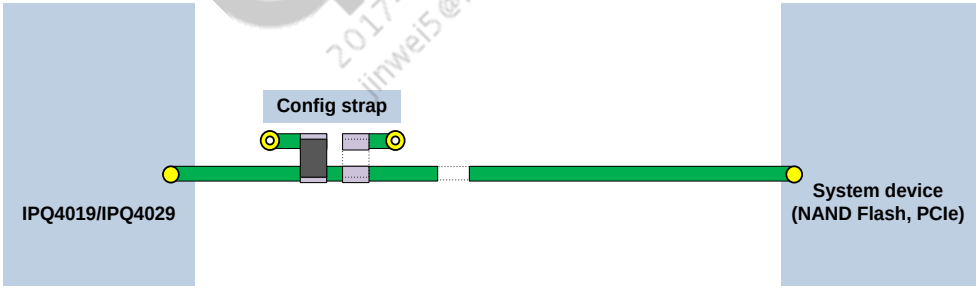


Figure 3-4 Configuration strap layout

- Minimize stubs routing of the configuration straps to the IPQ4019/IPQ4029 lines.
- Minimize the length of the stub if branched routing is used.
- Suggest to place the configuration strap resistor in the path or the routed trace where possible and close to the IPQ4019/IPQ4029. Populate the pull-up or pull-down as required.

3.4 Reference resistors

The IPQ4019/IPQ4029 uses several reference resistors. This section describes the designated values and design guidelines.

Table 3-6 IPQ4019/IPQ4029 reference resistors

Pin ID	Pin name	Value
AD27	Rbias	5.90K 1%

Table 3-7 Reference resistors design guidelines

Category	Guidelines/Remarks
Signals/ Groups	Reference resistors as per Table 3-6.
Placement	Place these resistors as close as possible to the IPQ4019/IPQ4029 device. Route them with wide traces within 200 mils.
Spacing	Provide as much spacing from these traces/resistors to neighboring board features as practically possible (at least 2 w).
Routing and Other	Connect the other end of these resistors directly to GND with dedicated vias. Avoid sharing vias on the return path as doing so can cause noise pickup from the other elements tied to the GND trace.

3.5 Ethernet interfaces

3.5.1 PSGMII

One PSGMII is available on the IPQ4019/IPQ4029. Table 3-8 shows the routing guidelines for these interfaces.

Table 3-8 PSGMII interface routing guidelines

Category	Guidelines/Remarks
Groups	PSGMII Tx, PSGMII Rx
Route type	Differential pair, 100 Ω impedance
Length	< 1.5 in., try to route as short as possible.
Length match within pair	±5 mils (refer to Table 3-9)
Length match across pairs	There is no requirement to length match the Tx and Rx pairs.
Spacing requirements	3 W spacing between pairs and to other signals
Vias/ layer transitions	Minimize layer transitions; where necessary limit to 2 vias per signal trace. Provide return vias interconnecting the GNDs in the immediate vicinity of the signal vias.
AC coupling	Use 0.1 µF capacitors on each signal line; place them symmetrically at the same point on the pair.

Chip internal delay should be take into consideration for length control.

Table 3-9 Internal length of chip − PSGMII

PSGMII	Pin ID	Internal wire (mm)
PSGMII_RXN	AG25	8.268
PSGMII_RXP	AF25	8.02
PSGMII_TXN	AG24	6.25
PSGMII_TXP	AF24	6.067

Figure 3-5 shows a reference implementation of the PSGMII layout.

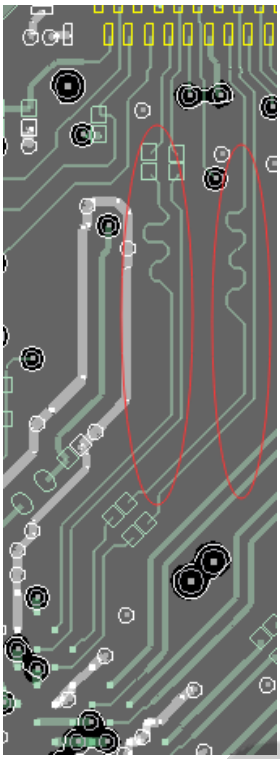


Figure 3-5 PSGMII routing

3.5.2 MDIO

The MDIO and MDC signals used to communicate with and control the external Ethernet devices (such as GE PHY) are multiplexed out on the pin H2 GPIO[6] (MDIO) and pin H3 GPIO[7] (MDC). The reference designs implemented shown in Table 3-10.

Table 3-10 MDIO level shifters

Category	Guidelines/Remarks		
Signal/group	**Configurable function**	**Pin ID**	**Pin name**
	MDC	H3	GPIO7
	MDIO	H2	GPIO6
Spacing	Because open drain signaling is used by MDIO, this signal is susceptible to crosstalk from strongly driven aggressors. A spacing of 2 w is recommended at a minimum from other signals for both MDIO and MDC.		
Loading	Run the traces short to the devices and reduce capacitive load.		
Voltage	MDC is 3.3 V push-pull output. MDIO is open drain-gate and need an external pull-up. Reference design pulls up to QCA8075 2.7 V.		

3.6 USB

The IPQ4019/IPQ4029 device has two USB host ports. One supports USB3.0 (with both SS and HS PHY), the other only supports USB2.0 with HS PHY. Implement the design guidelines shown in Table 3-11 and Table 3-12.

Table 3-11 USB 3.0 design guidelines

Category	Guidelines/Remarks
Groups	USB_TXP, USB_TXN USB_RXP, USB_RXN
Route type	Differential pair, 90 Ω impedance for the super speed pairs according to USB3.0 specification
Return path	Ensure continuous and unbroken return path without voids
Length	< 5 in.
Length match within pair	±5 mils
Length match across pairs	There is no requirement to length match the Tx and Rx pairs
Spacing requirements	3 W spacing between pairs and to other signals after the breakout from the BGA
Vias/ layer transitions	Avoid layer transitions. The reference design has been routed without vias on this interface with the signals traversing on top layer throughout. Recommend to follow this layout.
AC coupling	Use 0.1 µF capacitors on each signal line of the Tx pair from IPQ4019/IPQ4029; place them symmetrically at the same point on the pair.
Other	Clear the GND pour under the signal pads of the connector where SMD connectors are used.

Table 3-12 USB 2.0 design guidelines

Category	Guidelines/Remarks
Groups	(USB2_DP, USB2_DM) and (USB1_DP, USB1_DM)
Route type	Differential pair, 90 Ω impedance for the USB2.0 pair according to USB2.0 specification
Return path	Ensure continuous and unbroken return path without voids
Length	< 5 in.
Length match within pair	±5 mils
Length match across pairs	Not applicable
Spacing requirements	3 W spacing between pairs and to other signals after the breakout from the package
Vias/ layer transitions	Avoid layer transitions; the reference design has been routed without vias on this interface with the signals traversing on top layer throughout and recommend to follow this layout over continuous GND return path.
AC coupling	Not applicable; the lines must be DC connected.
Other	Clear the GND pour under the signal pads of the connector where SMD connectors are used.

Chip internal delay must be take into consideration for length control.

Table 3-13 Internal length of chip − USB

Pin name	Pin ID	Internal wire (mm)
USB2.0 port		
USB2_DM	AG17	4.789
USB2_DP	AF17	4.693
USB3.0 port		
USB1 _DM	AG22	5.388
USB1 _DP	AF22	5.236
USB_ RXN	AG21	5.245
USB_ RXP	AF21	5.213
USB_ TXN	AG19	4.952
USB_ TXP	AF19	4.86

The layout has been implemented in the reference designs as shown in Figure 3-6 and Figure 3-7.

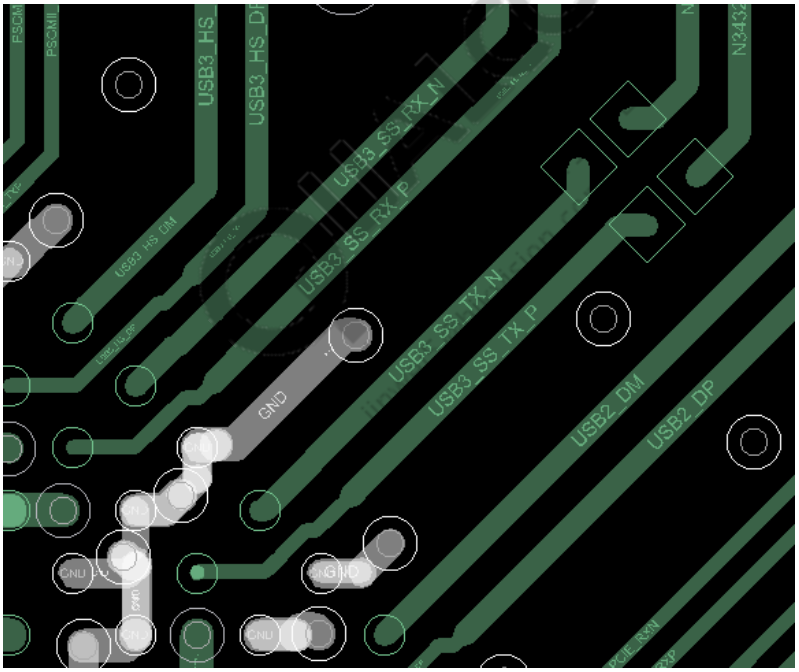


Figure 3-6 USB trace breakout at the IPQ4019/IPQ4029

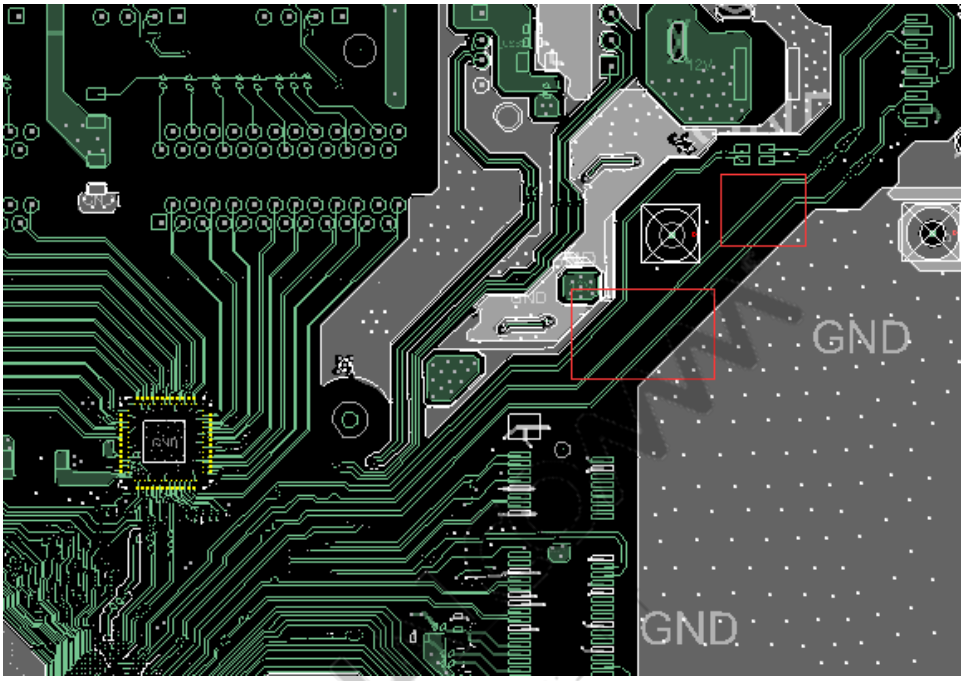


Figure 3-7 USB routing overview

The signals are routed without vias in the top layer end-to-end.

NOTE: In implementations of designs with radio or WLAN modules, recommend to maximize the separation of the USB 3.0 routing from these sections. Adverse co-location of these interfaces has been seen to elevate the noise floor of the radio spectrum in the 2.4 GHz band. In addition, reserve shielding box on top of USB3.0 signal to minimize potential radiation of USB3.0, and connector with fully enclosure for USB3.0 is necessary.

Layout rules

- Spatial isolation of the USB connector and device from the antennas significantly mitigates the issue. This can be implemented by careful placement of the USB and the RF circuitry and antennas relative to each other.
- Merging chassis GND to digital GND significantly mitigates the issue.
- Pour GND between the USB connectors as well and ensure good isolation to the super speed lines.
- The use of SMD fully closure connectors has considerable impact.
- Use of common-mode chokes on the USB lines has some impact.
- Routing the antenna connectors/cables for antennas should be optimal.
- Where required, covering/enclosing the USB connector, especially with absorptive material, mitigates the issue. Use of shielded connectors may be considered.

3.7 SPI

There are two SPI controllers on IPQ4019/IPQ4029. SPI0 connect with SPI NOR flash to boot SoC and mux with GPIO[12:15], and SPI1 is used to connect other SPI compatible device, on reference design, configured as VoIP interface.

Table 3-14 SPI design guidelines

Category	Guidelines/Remarks		
Signal/group	**Configurable function**	**Pin ID**	**Pin name**
	SPI_MOSI	K3	GPIO14
	SPI_MISO	K2	GPIO13
	SPI_CLK	L1	GPIO15
	SPI_CS	K1	GPIO12
Route type	Single-ended 50 Ωz controlled trace		
Spacing	2 W spacing is recommended especially for SPI_CLK, and place one 22 Ω damping resistor near SoC, and add one 15 pf capacitor to ground.		
Length	Run the traces short to the devices; keep within 5 in.		
Length match	Overall length match between the group (MISO, MOSI, CLK, and CS) is recommended to be within 500 mils		
Voltage	3.3 V logic		
Other	A moderate pull-up is recommended on the chip select line SPI_CS at the flash device		

3.8 Parallel NAND flash

8-bit parallel NAND that support booting from NAND flash.

The interface may realize either a NAND or LCD or audio connection. The reference design implements a 1G*8-bit NAND flash device.

Table 3-15 NAND flash design guidelines

Category	Guidelines/Remarks
Signal/group	▪ QPIC_PAD_NAND_CS_N ▪ QPIC_PAD_CLE_LB_N ▪ QPIC_PAD_ALE_LB_N ▪ QPIC_PAD _WE_N ▪ QPIC_PAD_OE_N ▪ QPIC_PAD_BUSY_N ▪ QPIC_PAD_DATA[7:0]
Route type	Single-ended
Return path	Ensure continuous and unbroken return path without voids
Length	< 5 in.
Length match	200 mils within group, 400 mils across groups
Spacing requirements	2 w spacing to other signals
GND shielding	Not required
Vias/ layer transitions	Vias are acceptable
Voltage	3.3 V

Category	Guidelines/Remarks
Decoupling and power layout	Follow best design practices and provide decoupling close to the NAND device. ▪ Allocate one 0201 decap per pin and locate it close to the pin ▪ A bulk capacitor in the order of 1 µF or more is advised for the device ▪ Share the 3.3 V power plane
Other	Some NAND controller output lines are used at power-up to sense boot configuration straps (see section 3.4). Take care to minimize stubs in the path. A 10 K pull-up is recommended on the NAND_CS signal at the flash device.

The implementation of the NAND routing on reference design is as shown in Figure 3-8.

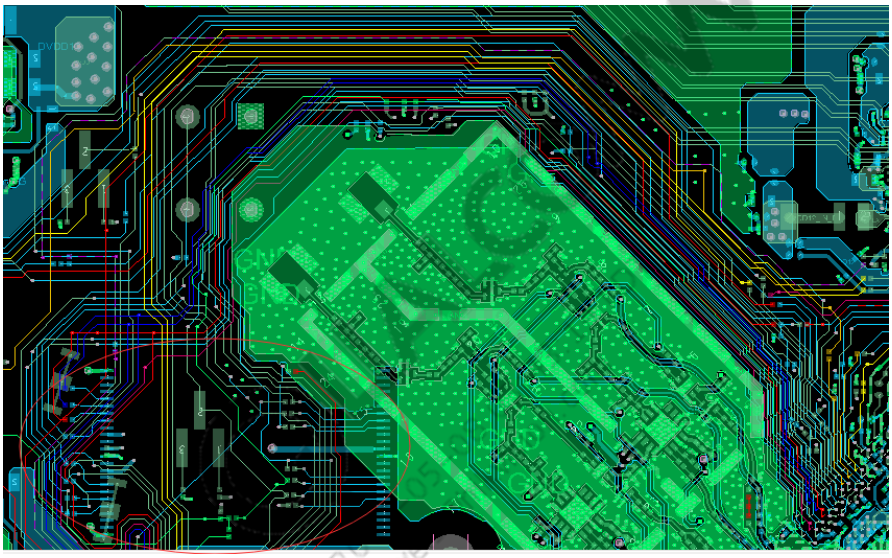


Figure 3-8 NAND flash routing overview

3.9 LCD port

The LCD controller supports the MIPI DBI type B device standard interface.

The LCD controller supports the following:

- Writing parallel 16-bit or 18-bit memory mapped LCD interfaces
- Reading parallel 16-bit memory mapped LCD interfaces
- VGA mode: 16-bits per pixel, 30 frames per second (BW: 18.4 MBytes/second)
- VGA mode: 18-bits per pixel, 15 frames per second (BW: 10.4 MBytes/second)
- QVGA mode: 16-bit/18-bits per pixel, 30 frames per second (BW: 4.6 MBytes/second)

The supported color depth is max 18 bits per pixel over 9 pins interface. It also supports VSync synchronous mode to avoid tearing effects.

The LCD controller has the device register writes/reads and device data writes support, when device register transfers are treated over 8 pins interface and allow 4 or less bytes to be read or written, while device data writes allow “endless” pixel data streams over 9 pins interface.

The LCD controller can be operated either by software for both control and data or by BAM for both control and data. When working in BAM mode, one single BAM pipe is used for sending data to device, configuring the LCD controller, configuring the LCD device and for reading status from controller and device, by the means of BAM's command elements feature.

The control logic for device register read and write paths is similar, the configuration data route is different. The write data flows through a FIFO that improves AHB interface performance by aggregating bursts of data or configuration accesses, and the read data directly returns back to AHB, bypassing the FIFO. The device read path is rarely used and any such read operation may result in multiple clock cycle wait states on the peripheral AHB.

Since the LCD controller shares the pad interface with the NAND and XMEM controllers, it needs to arbitrate accesses to the device pins.

This interface share pin with NAND flash and the same 2*10 2.54 mm pitch connector with Audio interface. On reference board that supports touch panel, I^{2}C0 is configured as touch-panel controller.

Table 3-16 LCD design guidelines

Category	Guidelines/Remarks
Signal/group	▪ QPIC_PAD_LCD_CS_N ▪ QPIC_PAD_CLE_LB_N ▪ QPIC_PAD_LCD_RS_N ▪ QPIC_PAD_ALE_LB_N ▪ QPIC_PAD _WE_N ▪ QPIC_PAD_OE_N ▪ QPIC_PAD_BUSY_N ▪ QPIC__PAD _DATA_[8:0] ▪ BLSP_I2C0_SCK ▪ BLSP_I2C0_SDA ▪ TP_Wake ▪ TP_INT
Route type	Single-ended 50 Ω impedance
Return path	Ensure continuous and unbroken return path without voids
Length	< 5 in.
Spacing requirements	2 w spacing to other signals
GND shielding	Not required
Vias/ layer transitions	Vias are acceptable
Voltage	3.3 V
Decoupling and power layout	Follow best design practices and provide decoupling close to the NAND device. ▪ Allocate one 0201 decap per pin and locate it close to the pin ▪ A bulk capacitor in the order of 1µF or more is advised for the device ▪ Share the 3.3 V power plane

3.10 I^{2}C

The I^{2}C port is muxed with GPIO and used to connect with touch-panel connector or audio device on reference design.

Table 3-17 I²C design guidelines

Category	Guidelines/Remarks
Signal/group	I²C_SDA, I²C_SCL
Spacing	As open drain signaling is used by the interface, these signals are susceptible to crosstalk from strongly driven aggressors. A spacing of 2 w is recommended at the minimum from other signals.
Loading	Run the traces short to the devices and reduce capacitive load.
Voltage	The IPQ4019/IPQ4029 device operates this interface at 1.8 V and the input will not withstand higher voltage. Level converters are recommended to work with I²C devices at higher voltage.

3.11 Audio ports

- 3 x I²S Tx ports
- 1 x I²S Rx port
- 1 x TDM Tx/Rx ports that share pins with the I²S port 0
- SPDIF input and output
- PCM port for Tx/Rx
- 4 x PWM ports for CXO and LCD brightness control

Audio interface also shares most pins with NAND flash and LCD.

3.12 SD/eMMC port

- Support 4/8-bit SD 3.0 card up to SD104 mode
- Support 4/8-bit eMMC 4.5 up to HS200 mode
- DDR50 mode
- Support eMMC boot with TLMM setting up the pin connection automatically

There is one SD/eMMC+ connector on reference board. One SD card can be inserted to enlarge storage capacity. This interface also muxes with GPIO.

IPQ4019/IPQ4029 can configure bootstrap to boot from eMMC card.

Table 3-18 SDIO design guidelines

Category	Guidelines/Remarks		
Signal/group	**Configurable function**	**Pin ID**	**Pin Name**
	SDIO_CD	AE9	GPIO22
	SDIO_CLK	AF9	GPIO27
	SDIO_DAT[0]	AE10	GPIO23
	SDIO_DAT[1]	AF8	GPIO24
	SDIO_DAT[2]	AE12	GPIO25
	SDIO_DAT[3]	AE11	GPIO26
	SDIO_DAT[4]	AF11	GPIO29

Category	Guidelines/Remarks		
	SDIO_DAT[5]	AF12	GPIO30
	SDIO_DAT[6]	AF10	GPIO31
	SDIO_DAT[7]	AG9	GPIO32
Route type	Single-ended 50 Ω impedance		
Return path	Ensure continuous and unbroken return path without voids		
Length	< 4.5 in.		
Length match	10 mils within group		
Spacing requirements	2 w spacing to other signals		
GND shielding	Not required		
Vias/ layer transitions	Vias are acceptable		
Voltage	1.8 V /3.3 V auto change according to SD card If configured as eMMC interface, it is fixed 1.8 V.		
Decoupling and power layout	Follow best design practices and provide decoupling close to the SDIO device. ▪ Allocate one 0201 decap per pin and locate it close to the pin ▪ A bulk capacitor in the order of 1 MF or more is advised for the device		
Other	Pay attention to SDIO_CLK, add 22 Ω damping resistor and 5.0 pf paralleled cap to GND.		

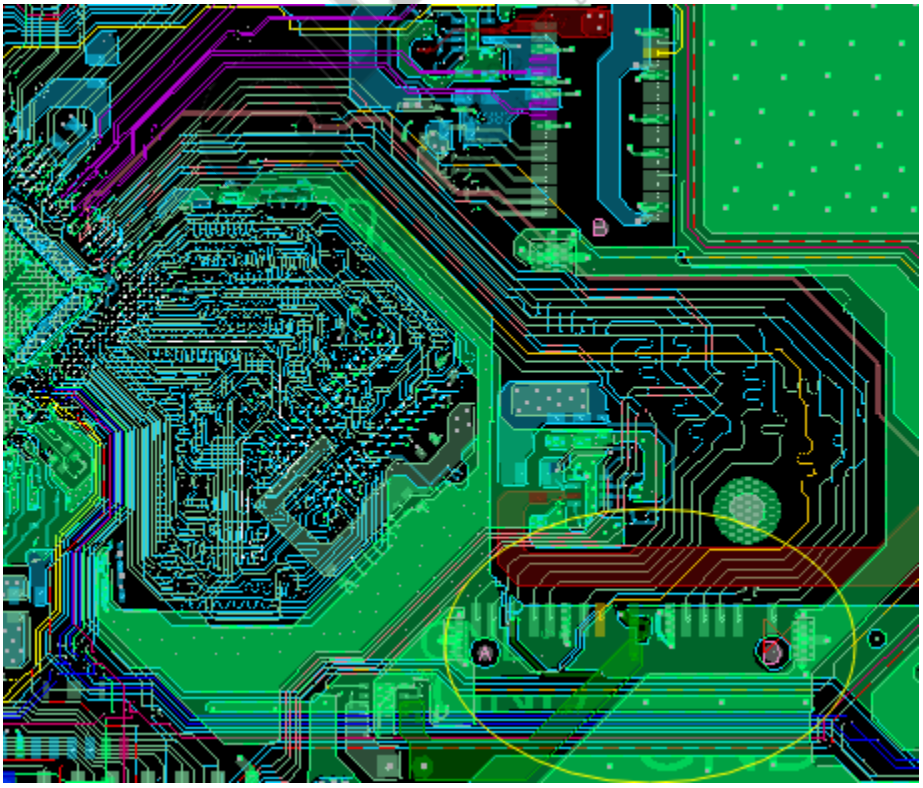


Figure 3-9 SDIO routing overview

3.13 VoIP

This interface is composed of one SPI plus one PCM interface. SPI1 controller mux with GPIO [44:47] on IPQ4019/IPQ4029. PCM interface is mux with GPIO [48:51].

There is one VoIP connector on reference board that can connect with TB724 to achieve the VoIP solution.

Table 3-19 VoIP design guidelines

Category	Guidelines/Remarks			
Signal/group	**Configurable function**		**Pin ID**	**Pin name**
	VOIP_RSTn			
	VOIP_INTn			
	SPI	VOIP_SCLK	Y26	GPIO44
		VOIP_CS	Y27	GPIO 45
		VOIP_MOSI	W24	GPIO 46
		VOIP_MISO	W25	GPIO 47
	PCM	VOIP_DTX	W26	GPIO 48
		VOIP_DRX	W27	GPIO 49
		VOIP_PCLK	V24	GPIO 50
		VOIP_FSYNC	V25	GPIO 51
Route type	Single-ended 50 Ω impedance			
Return path	Ensure continuous and unbroken return path without voids			
Length	< 5 in.			
Spacing requirements	2 w spacing to other signals			
GND shielding	Not required			
Vias/ layer transitions	Vias are acceptable			
Voltage	3.3 V			
Decoupling and power layout	Follow best design practices and provide decoupling close to the NAND device. ▪ Allocate one 0201 decap per pin and locate it close to the pin ▪ A bulk capacitor in the order of 1 µF or more is advised for the device ▪ Share the 3.3 V power plane			

3.14 PCIe

The reference design implements mini-PCIe connectors that can accommodate radio daughtercards.

Three PCIe 2.0 ports of 1x lane width as root complex (RC) are implemented on the IPQ4019/IPQ4029. Table 3-20 and Table 3-21 show the applicable design guidelines.

Table 3-20 PCIe design guidelines for data signals

Category	Guidelines/Remarks
Signal/group	PCIE_TXP, PCIE_TXN PCIE_RXP, PCIE_RXN
Route type	Differential pair, 100 Ω impedance
Return path	Ensure continuous and unbroken return path without voids
Length	< 5 in.
Length match within pair	+/- 5 mils
Length match across pairs	There is no requirement to length match the Tx and Rx pairs
Spacing requirements	3 w spacing between pairs and to other signals after the breakout from the BGA
GND shielding	Provide GND shield at 3 w spacing away from the signal pairs. The GND shape must be stitched to the main GND in inner layers with vias at regular intervals of 100 mils.
Vias/ layer transitions	Avoid layer transitions. The reference design has been routed without vias on this interface with the signals traversing on top layer throughout and recommend to follow this layout over continuous GND return path.
AC coupling	Use 0.1 µF capacitors on each signal line of the Tx pair from the IPQ4019/IPQ4029; place them symmetrically at the same point on the pair.
Voltage	The voltage rails for the PCIe interface are implemented with filters for the PLL (AVDDPLL_PCIE) and the I/O (AVDD) rails as described in chapter 4.
Other	Clear the GND pour under the paired signal pads of the connector where SMD connectors are used.

Table 3-21 PCIe design guidelines for REFCLK

Category	Guidelines/Remarks
Signal/group	PCIE_CLKOUTN, PCIE_CLKOUTTP
Route type	Differential pair, 100 Ω impedance
Return path	Ensure continuous and unbroken return path without voids
Length	< 5 in.
Length match within pair	±5 mils
Length match across pairs	There are no specific requirements to match lengths across different REFCLK pairs.
Spacing requirements	3 w spacing between pairs and to other signals after the breakout from the BGA
GND shielding	Provide GND shield at 3 w spacing away from the signal pairs. The GND shape must be stitched to the main GND in inner layers with vias at regular intervals of 100 mils.
Vias/ layer transitions	Minimize layer transitions. The reference layout is implemented with no transitions. Where necessary, limit to 2 vias per signal trace. Provide return vias interconnecting the GNDs in the immediate vicinity of the signal vias. These vias should form a symmetric GSSG pattern and recommend to clear an oblong void at this transition point through layers.
AC coupling	Should not be used. The REFCLK must be DC connected to the loads. A series damping provision is made on the reference design but populated with 0 Ω.

Category	Guidelines/Remarks
Other	A shunt termination provision is made at the connector but not used (No_Load).

The reference design implements a PCIe port terminated in mini-PCIe connectors. This layout is illustrated in Figure 3-10 through Figure 3-12.

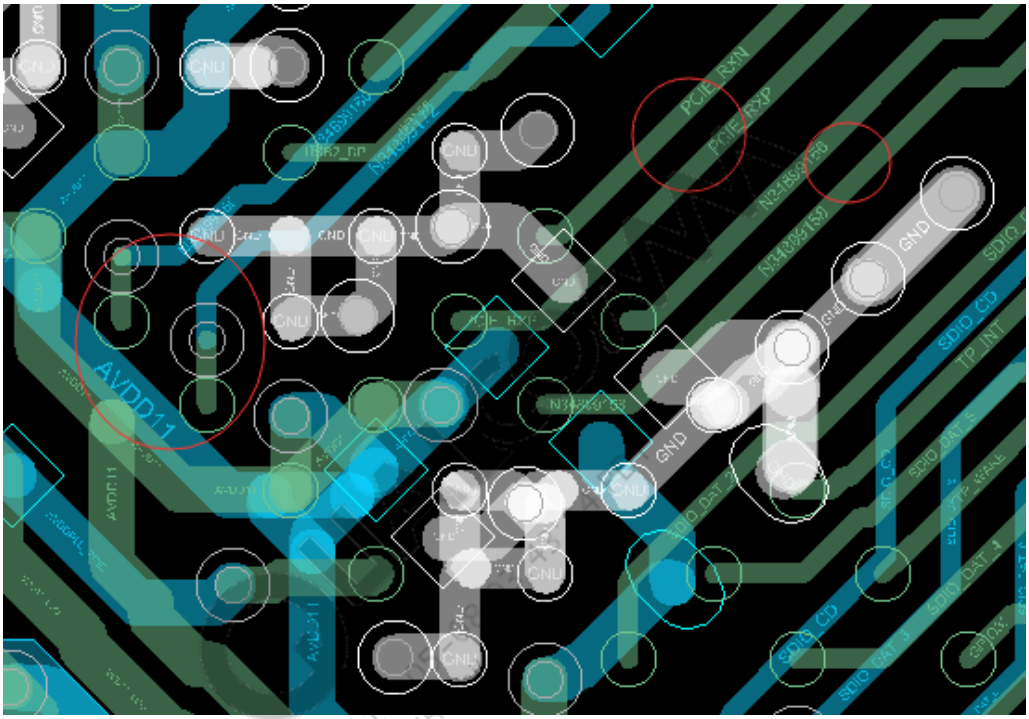


Figure 3-10 PCIe trace breakout at the IPQ4019/IPQ4029

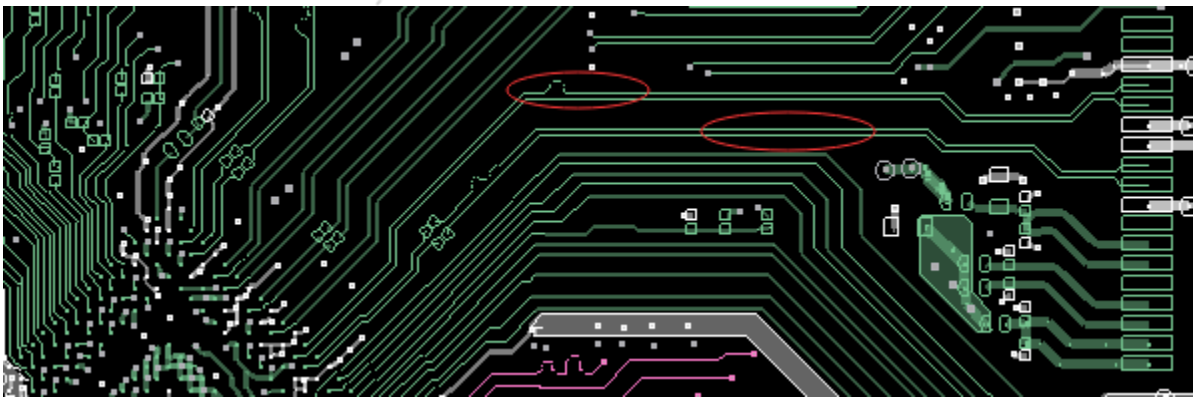


Figure 3-11 PCIe routing overview

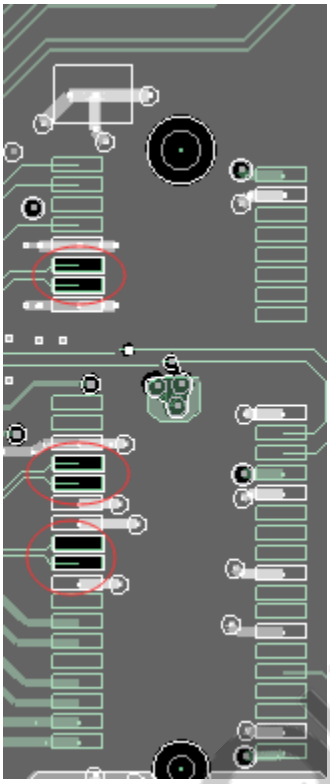


Figure 3-12 Mini-PCIe connector with cutouts in GND under the SMD pads

3.15 WCI

The reference design implements a WCI interface (Wi-Fi LTE co-exist) with GPIO[37](wci_out), GPIO[42](wci_in[0]), and GPIO[43](wci_in[1]). There is connector on reference board to connect with IPQ4019/IPQ4029 WCI interface.

Wi-Fi LTE co-ex support two modes:

- 2-wire mode: wifi0/1_wci_out and wifi_wci_in(0). Wifi_wci_in(1) is not used.
- 3-wire mode: wifi0/1_wci_out, wifi_wci_in(0), and wifi_wci_in(1).

In 2-wire mode and 3-wire mode, wifi0 and 1 share GPIO. TLMM can control which Wi-Fi use this group of GPIO to control LTE.

Table 3-22 WCI design guidelines

Category	Guidelines/Remarks
Signal/group	▪ wci_out ▪ wci_in[0] ▪ wci_in[1]
Route type	Single-ended
Return path	Ensure continuous and unbroken return path
Spacing requirements	3w spacing between pairs and to other signals after the breakout from the BGA

3.16 DDR3L DRAM

The IPQ4019/IPQ4029 package implements a 16-bit wide DDR3L interface. The memory topology described in this document uses one 16-bit DDR3L device.

The command address (CA) bus and data bus are routed in point-to-point topology, as shown in Figure 3-13. VTT terminations are used for CA lines.

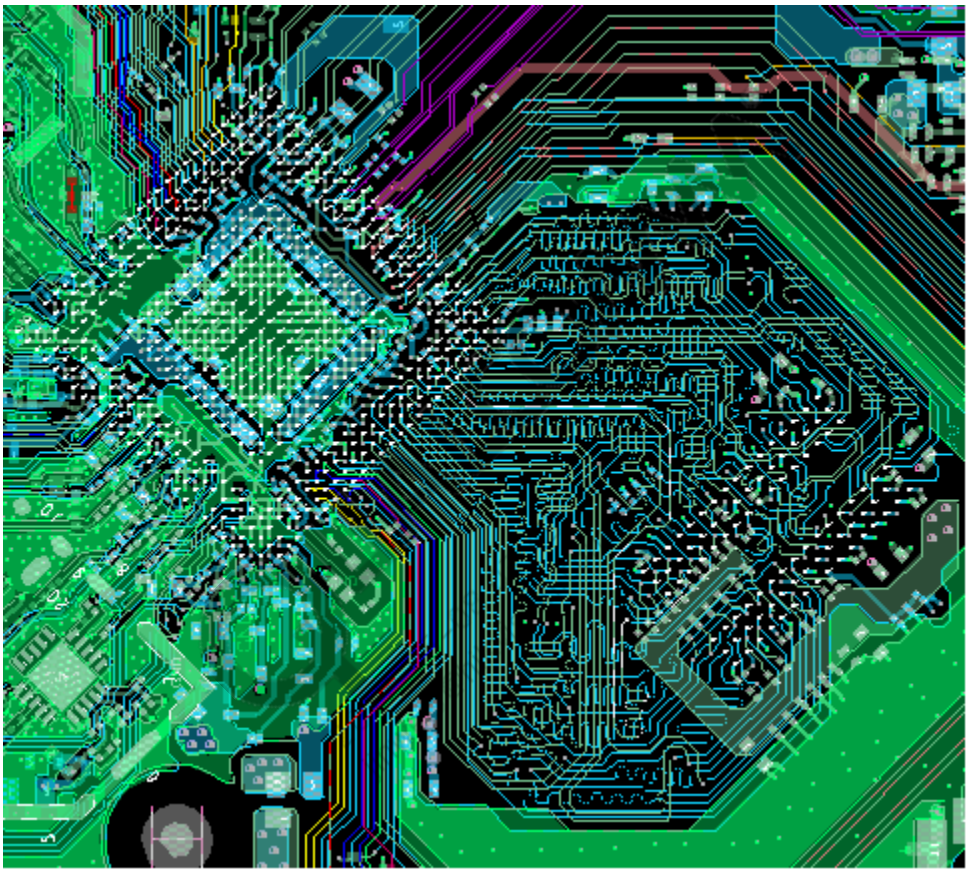


Figure 3-13 DDR3 Routing Topology

The design guidelines are summarized in Table 3-23.

Table 3-23 DDR3 DRAM design guidelines

Category	Guidelines/Remarks	
Groups	**Group**	**Signals**
	Differential pairs	
	Clock	DDR3_CLK_N, DDR3_CLK
	DQS0	DDR_DQS_0, DDR_DQS_N_0
	DQS1	DDR_DQS_1, DDR_DQS_N_1
	Single-ended	
	DDR_CA group	DDR_ADDR_[15:0], DDR_BA_[2:0], DDR_CAS_N, DDR_WE_N, DDR_ODT, DDR_RAS_N, DDR_RST_N
	DDR_DQ byte0 (data, mask, dqs)	DDR_DQ_[7:0], DDR_DQM_0, (DDR_DQS_0, DDR_DQS_N_0)

Category	Guidelines/Remarks	
	DDR_DQ byte1 (data, mask, dqs)	DDR_DQ_[15:8], DDR_DQM_1, (DDR_DQS_1, DDR_DQS_N_1)
Route type	▪ DQS: 110 Ω differential impedance ▪ DDR Clock: 100 Ω differential impedance ▪ Single-ended signals: 60 Ω impedance Because external calibration resistor is 240 Ω and internal VTT resistor on DQ line is 240/4=60 Ω, external VTT resistor on command/address line is also 60.4 Ω. For impedance match, single-ended signal is 60 Ω. Though differential is 60 *2=120 ohm, use 110 Ω for PCB process reason.	
Return path	Ensure continuous and unbroken return path without voids	
Length	Recommend to keep the routed length to within 3 in. for the CA group. Recommend to route DQ lanes as short as possible and keep within 2 in..	
Spacing	▪ DQS/DQ: 3 W ▪ Clock: 3 W ▪ Other: 3 W is preferred and at least 2 W. ▪ When adding trace lengths, follow 3x spacing within serpentine loops to the extent possible	
Length match rules	Use the following length match per group:	
	Signal type	**Length-match within**
	DQ, DM, DQS (within group)	±50 mils
	DQSp-to-DQSN (intra-pair)	±5 mils
	CA-to-CK	400 mils
	CK-to-CKB (intra-pair)	±5 mils
	DQS-to-CK	≤600 mils
	The length match includes via length in the trace match. The groups should be formed with vias accounted for.	
Vias/layer transitions	Minimize layer transitions where necessary limit to 2 vias per signal trace.	
VREF	▪ Use a 1 K 1% resistor divider with accompanying 0.1 µF filter to each rail, colocated with a small copper pour. Route thick short trace from this island to the VREF pins ▪ Keep a 2 w spacing from the trace to its neighbors ▪ Separate dividers can be used. One close to the IPQ4019/IPQ4029 device, one close to DDR_VREFCA, and one close to DDR VREF_DQ.	
ZQ/Cal resistors	For DDR devices, recommend to place the 240 Ω resistor close to the device ball and route to GND with a 2 w separation.	
Decoupling and power layout	▪ Provide individual 0201 capacitors per pin for the VDDQ and VDDL close to the pins ▪ Connect them up with minimal inductance on both VDD and GND paths ▪ Provide one bulk capacitor of 10 µF at least	
Voltage	1.35 V The reference design is populated and validated with PCDDR3L devices.	

Chip internal wire length must be take into consideration for PCB length match.

Table 3-24 Internal length of chip − DDR3L DRAM

DDR ADD/CMD	Internal wire (mm)
DDR_A_0 [ADD/CMD]	4.885
DDR_A_1 [ADD/CMD]	5.448
DDR_A_2 [ADD/CMD]	5.636

DDR ADD/CMD	Internal wire (mm)
DDR_A_3 [ADD/CMD]	3.583
DDR_A_4 [ADD/CMD]	4.699
DDR_A_5 [ADD/CMD]	5.166
DDR_A_6 [ADD/CMD]	5.009
DDR_A_7 [ADD/CMD]	6.274
DDR_A_8 [ADD/CMD]	6.039
DDR_A_9 [ADD/CMD]	4.154
DDR_A_10 [ADD/CMD]	5.568
DDR_A_11 [ADD/CMD]	4.261
DDR_A_12 [ADD/CMD]	5.622
DDR_A_13 [ADD/CMD]	5.078
DDR_A_14 [ADD/CMD]	5.279
DDR_A_15 [ADD/CMD]	9.266
DDR_BA_0 [ADD/CMD]	5.988
DDR_BA_1 [ADD/CMD]	4.922
DDR_BA_2 [ADD/CMD]	5.144
DDR_CAS_N [ADD/CMD]	5.373
DDR_CKE_M [ADD/CMD]	5.282
DDR_CK_N [ADD/CMD]	5.522
DDR_CK_P [ADD/CMD]	5.575
DDR_ODT [ADD/CMD]	5.841
DDR_RAS_N [ADD/CMD]	4.258
DDR_WE_N [ADD/CMD]	4.914
DDR_CS_N[0] [ADD/CMD]	4.419
DATA0	
DDR_DM_0 [DATA0]	6.813
DDR_DQSN_0 [DATA0]	6.868
DDR_DQS_0 [DATA0]	6.734
DDR_DQ_0 [DATA0]	7.266
DDR_DQ_1 [DATA0]	7.795
DDR_DQ_2 [DATA0]	6.232
DDR_DQ_3 [DATA0]	6.284
DDR_DQ_4 [DATA0]	4.959
DDR_DQ_5 [DATA0]	6.422
DDR_DQ_6 [DATA0]	4.735
DDR_DQ_7 [DATA0]	6.79
DATA1	
DDR_DM_1 [DATA1]	7.405
DDR_DQSN_1 [DATA1]	7.512
DDR_DQS_1 [DATA1]	7.639
DDR_DQ_8 [DATA1]	6.501

DDR ADD/CMD	Internal wire (mm)
DDR_DQ_9 [DATA1]	6.043
DDR_DQ_10 [DATA1]	6.554
DDR_DQ_11 [DATA1]	5.861
DDR_DQ_12 [DATA1]	5.68
DDR_DQ_13 [DATA1]	6.227
DDR_DQ_14 [DATA1]	6.898
DDR_DQ_15 [DATA1]	6.089

3.17 Debug interfaces

The reference design includes debug interface for the ARM (JTAG). It also includes a header for an RS232 UART daughtercard used for the debug console.

NOTE: The JTAG/UART connector of the debug cable/card is not suitable for hot plug-in.

3.17.1 JTAG

There is a 20-pin JTAG connector on reference design. It can connect to TRACE32 directly to debug ARM core.

Table 3-25 JTAG debug interface design guidelines

Category	Guidelines/Remarks
Signals/ Group	JTAG_TRST_N, JTAG_TDI, JTAG_TDO, JTAG_TMS, JTAG_TCK, JTAG_RST_N (SRST)
Mechanical	Ensure sufficient clearance for placement of debug headers
Spacing	2 w spacing is desirable
Routing	Route short (<5 in.) and direct traces with impedance control
Length match	No critical requirement; recommend to keep the signals matched within 500 mils
Voltage	Operates at 3.3 V; the PowerTrace debugger can be connected directly

3.17.2 UART

There are two UART connectors on reference design.

- UART0 is used to debug system CPU with no hardware flow control support.
- UART1 is used to connect with Bluetooth with hardware flow control.

3.18 GPIO

The IPQ4019/IPQ4029 has a total of 69 GPIO pins. Many of these GPIOs are muxed with other functionality as described in below table, such as JTAG, MDIO/MDC, SPI, UART.

After power-up, some GPIOs are configured as special function pin as below table.

Table 3-26 GPIO configurable function

GPIO_NUM	Bootstrap signal (GPIO number)	Default feature
GPIO_12 to GPIO_15	Boot_interface[1:0]({GPIO_51,GPIO_14})	If boot_interface is 2'b00, default feature is SPI0. If boot_interface is not 2'b00, default feature is GPIO
GPIO_19		Default feature is chip_rst_out
GPIO_22 to GPIO_32	Boot_interface[1:0]({GPIO_51,GPIO_14})	If boot_interface is 2'b01, default feature is SDCC. If boot_interface is not 2'b01, default feature is GPIO Note: Since GPIO_22 is used as sdio_cd, configure it as normal GPIO, and enable the GPIO direct interrupt feature.
GPIO_52 to GPIO_69	Boot_interface[1:0]({GPIO_51,GPIO_14})	If boot_interface is 2'b10, default feature is QPIC. If boot_interface is not 2'b10, default feature is GPIO.
Other GPIOs		Default feature is GPIO

There are no critical guidelines for routing generic GPIO signals that connect to switches, LEDs, interrupts, and so on.

Notice that the function of each GPIO is limited; only can achieve as below table.

Table 3-27 GPIO

GPIO	GPIO Function	GPIO_CFG[5:2] (FUNC_SEL)	Function description
0	GPIO_IN_OUT(0)	0	General Purpose Input/Output
	jtag_tdi	1	JTAG test data input
	audio_rxbclk	3	Bit clock of Audio I^2S/TDM Rx interface
1	GPIO_IN_OUT(1)	0	General Purpose Input/Output
	jtag_tck	1	JTAG test clock input
	audio_rxfsync	3	Left or Right indication of Audio I^2S Rx interface and frame start indication of Audio TDM Rx interface
2	GPIO_IN_OUT(2)	0	General Purpose Input/Output
	jtag_tms	1	JTAG test mode selection
	audio_rxd	3	Serial digital data of Audio Rx interface
3	GPIO_IN_OUT(3)	0	General Purpose Input/Output
	jtag_tdo	1	JTAG test data output
4	GPIO_IN_OUT(4)	0	General Purpose Input/Output
	jtag_rst_n	1	Chip function reset input
5	GPIO_IN_OUT(5)	0	General Purpose Input/Output
	jtag_trst_n	1	JTAG tap controller reset input
6	GPIO_IN_OUT(6)	0	General Purpose Input/Output
	mdio	1	Management Data Input/Output
7	GPIO_IN_OUT(7)	0	General Purpose Input/Output

GPIO	GPIO Function	GPIO_CFG[5:2] (FUNC_SEL)	Function description
	mdc	1	Management Data Clock
8	GPIO_IN_OUT(8)	0	General Purpose Input/Output
	blsp_uart1_txd	1	UART1 transmit data
	wifi0_uart_txd	2	wifi_2g UART transmit data
	wifi1_uart_txd	3	wifi_5g UART transmit data
9	GPIO_IN_OUT(9)	0	General Purpose Input/Output
	blsp_uart1_rxd	1	UART1 receive data
	wifi0_uart_rxd	2	wifi_2g UART receive data
	wifi1_uart_rxd	3	wifi_5g UART receive data
	wifi0_uart_txd	5	wifi_2g UART transmit data
10	GPIO_IN_OUT(10)	0	General Purpose Input/Output
	blsp_uart1_cts	1	UART 1 clear to send
	wifi0_uart_cts	2	wifi_2g UART clear to send
	wifi1_uart_cts	3	wifi_5g UART clear to send
	blsp_i2c0_sck	4	I^2C0 clock
11	GPIO_IN_OUT(11)	0	General Purpose Input/Output
	blsp_uart1_rts	1	Uart1 ready to send
	wifi0_uart_rts	2	wifi_2g UART ready to send
	wifi1_uart_rts	3	wifi_5g UART ready to send
	blsp_i2c0_sda	4	I^2C0 data
12	GPIO_IN_OUT(12)	0	General Purpose Input/Output
	blsp_spi0_ss0_n	1	SPI0 chip select 0
	blsp_i2c1_sck	2	I^2C1 clock
13	GPIO_IN_OUT(13)	0	General Purpose Input/Output
	blsp_spi0_miso	1	SPI0 master-in slave-out data
	blsp_i2c1_sda	2	I^2C1 data
14	GPIO_IN_OUT(14)	0	General Purpose Input/Output
	blsp_spi0_mosi	1	SPI0 Master out Slave in data
15	GPIO_IN_OUT(15)	0	General Purpose Input/Output
	blsp_spi0_sck	1	SPI0 serial clock output
16	GPIO_IN_OUT(16)	0	General Purpose Input/Output
	blsp_uart0_rxd	1	UART0 receive data
	led(0)	2	LED0
17	GPIO_IN_OUT(17)	0	General Purpose Input/Output
	blsp_uart0_txd	1	UART0 transmit data
	led(1)	2	LED1
18	GPIO_IN_OUT(18)	0	General Purpose Input/Output
	wifi0_uart_cts	1	wifi_2g UART clear to send
	wifi1_uart_cts	2	wifi_5g UART clear to send
19	GPIO_IN_OUT(19)	0	General Purpose Input/Output
	chip_rst_out	1	Chip reset out, low active

GPIO	GPIO Function	GPIO_CFG[5:2] (FUNC_SEL)	Function description
	wifi0_uart_rts	2	wifi_2g UART ready to send
	wifi1_uart_rts	3	wifi_5g UART ready to send
20	GPIO_IN_OUT(20)	0	General Purpose Input/Output
	blsp_i2c0_sck	1	I2C0 clock
	audio_rxmclk	2	Master clock source of Audio I^{2}S/TDM Rx interface
21	GPIO_IN_OUT(21)	0	General Purpose Input/Output
	blsp_i2c0_sda	1	I^{2}C0 data
	audio_rxbclk	2	Bit clock of Audio I^{2}S/TDM Rx interface
22	GPIO_IN_OUT(22)	0	General Purpose Input/Output
	rgmii_rxd(0)	1	RGMII Data input 0
	audio_rxfsync	2	Left or Right indication of Audio I^{2}S Rx interface and frame start indication of Audio TDM Rx interface
23	GPIO_IN_OUT(23)	0	General Purpose Input/Output
	sdio_dat(0)	1	SDIO Data input/output 0
	rgmii_rxd(1)	2	RGMII Data input 1
	audio_rxd	3	Serial digital data of Audio Rx interface
24	GPIO_IN_OUT(24)	0	General Purpose Input/Output
	sdio_dat(1)	1	SDIO Data input/output 1
	rgmii_rxd(2)	2	RGMII Data input 2
	audio_txmclk	3	Master clock source of Audio I^{2}S/TDM Tx interface
25	GPIO_IN_OUT(25)	0	General Purpose Input/Output
	sdio_dat(2)	1	SDIO Data input/output 2
	rgmii_rxd(3)	2	RGMII Data input 3
	audio_txbclk	3	Bit clock of Audio I2S/TDM Tx interface
26	GPIO_IN_OUT(26)	0	General Purpose Input/Output
	sdio_dat(3)	1	SDIO Data input/output 3
	rgmii_rx_ctl	2	RGMII Rx control
	audio_txfsync	3	Left or Right indication of Audio I^{2}S Tx interface and frame start indication of Audio TDM Tx interface
27	GPIO_IN_OUT(27)	0	General Purpose Input/Output
	sdio_clk	1	SDIO CLK
	rgmii_txc	2	RGMII Tx clock
	audio_td1	3	Serial digital data output 1 of Audio multi-channel I^{2}S Tx interface and serial digital data of Audio TDM Tx interface
28	GPIO_IN_OUT(28)	0	General Purpose Input/Output
	sdio_cmd	1	SDIO card detect
	rgmii_txd(0)	2	RGMII Tx Data 0
	audio_td2	3	Serial digital data output 2 of Audio multi-channel I^{2}S Tx interface
29	GPIO_IN_OUT(29)	0	General Purpose Input/Output
	sdio_dat(4)	1	SDIO Data input/output 4
	rgmii_txd(1)	2	RGMII Tx Data 1

GPIO	GPIO Function	GPIO_CFG[5:2] (FUNC_SEL)	Function description
	audio_td3	3	Serial digital data output 3 of Audio multi-channel I2S Tx interface
30	GPIO_IN_OUT(30)	0	General Purpose Input/Output
	sdio_dat(5)	1	SDIO Data input/output 5
	rgmii_txd(2)	2	RGMII Tx Data 2
	audio_pwm0	3	Audio Pulse Width Modulation interface 0
31	GPIO_IN_OUT(31)	0	General Purpose Input/Output
	sdio_dat(6)	1	SDIO Data input/output 6
	rgmii_txd(3)	2	RGMII Tx Data 3
	audio_pwm1	3	Audio Pulse Width Modulation interface 1
32	GPIO_IN_OUT(32)	0	General Purpose Input/Output
	sdio_dat(7)	1	SDIO Data input/output 7
	rgmii_rxc	2	RGMII Rx clock
	audio_pwm2	3	Audio Pulse Width Modulation interface 2
33	GPIO_IN_OUT(33)	0	General Purpose Input/Output
	rgmii_tx_ctl	1	RGMII Tx control
	audio_pwm3	2	Audio Pulse Width Modulation interface 3
34	GPIO_IN_OUT(34)	0	General Purpose Input/Output
	blsp_i2c1_sck	1	I^2C1 clock
	audio_spdifin	2	Audio SPDIF input
35	GPIO_IN_OUT(35)	0	General Purpose Input/Output
	blsp_i2c1_sda	1	I^2C1 data
	audio_spdifout	2	Audio SPDIF output
36	GPIO_IN_OUT(36)	0	General Purpose Input/Output
	rmii0_txd(0)	1	RMII0 Tx data 0
	led(2)	2	LED2
	led(0)	3	LED0
37	GPIO_IN_OUT(37)	0	General Purpose Input/Output
	rmii0_txd(1)	1	RMII0 Tx data 1
	wifi0_wci_out	2	wifi_2g LTE Coex output
	wifi1_wci_out	3	wifi_5g LTE Coex output
	led(1)	4	LED1
38	GPIO_IN_OUT(38)	0	General Purpose Input/Output
	rmii0_tx_en	1	RMII0 Tx enable
	led(2)	2	LED2
39	GPIO_IN_OUT(39)	0	General Purpose Input/Output
	rmii0_rx_er	1	RMII0 Rx error in master mode; RMII0 Tx error in slave mode
	pcie_clk_req_n	2	PCIe clock request, low active
	led(3)	3	LED3
40	GPIO_IN_OUT(40)	0	General Purpose Input/Output

GPIO	GPIO Function	GPIO_CFG[5:2] (FUNC_SEL)	Function description
	rmii0_refclk	1	RMII0 Input reference clock in RMII0 Slave mode; RMII0 Output reference clock in master mode
	wifi0_rfsilient_bb	2	wifi_2g RF silent signal (RF_kill)
	wifi1_rfsilient_bb	3	wifi_5g RF silent signal (RF_kill)
	led(4)	5	LED4
41	GPIO_IN_OUT(41)	0	General Purpose Input/Output
	rmii0_rxd(0)	1	RMII0 Rx data 0
	wifi0_cal_xpa_active	2	wifi_2g xPA control signal used for test purpose
	wifi1_cal_xpa_active	3	wifi_5g xPA control signal used for test purpose
42	GPIO_IN_OUT(42)	0	General Purpose Input/Output
	rmii0_rxd(1)	1	RMII0 Rx data 1
	wifi_wci_in(0)	2	Wi-Fi LTE Coex input
43	GPIO_IN_OUT(43)	0	General Purpose Input/Output
	rmii0_dv	1	RMII0 Rx valid
	wifi_wci_in(1)	2	Wi-Fi LTE Coex input
44	GPIO_IN_OUT(44)	0	General Purpose Input/Output
	rmii1_refclk	1	RMII1 Input reference clock in slave mode; RMII1 Output clock when master mode
	blsp_spi1_sck	2	SPI1 serial clock output
	smart_ant4	3	wifi_2g TXPCU_ANTENNA_INFO[0] (from MAC) wifi_2g serial clock for smart antenna (serial mode)
	led(5)	4	LED5
45	GPIO_IN_OUT(45)	0	General Purpose Input/Output
	rmii1_rxd(0)	1	RMII1 Rx data 0
	blsp_spi1_ss0_n	2	SPI1 chip select 0
	smart_ant5	4	wifi_2g TXPCU_ANTENNA_INFO[1] (from MAC) wifi_2g serial Data for smart antenna (serial mode)
	led(6)	5	LED6
46	GPIO_IN_OUT(46)	0	General Purpose Input/Output
	rmii1_rxd(1)	1	RMII1 Rx data 1
	blsp_spi1_mosi	2	SPI1 master-out slave-in data
	smart_ant6	3	wifi_5g TXPCU_ANTENNA_INFO[0] (from MAC) wifi_5g serial clock for smart antenna (serial mode)
	led(7)	4	LED7
47	GPIO_IN_OUT(47)	0	General Purpose Input/Output
	rmii1_dv	1	RMII1 Rx valid
	blsp_spi1_miso	2	SPI1 master-in slave-out data
	smart_ant7	3	wifi_5g TXPCU_ANTENNA_INFO[1] (from MAC) wifi_5g serial Data for smart antenna (serial mode)
	led(8)	4	LED8
48	GPIO_IN_OUT(48)	0	General Purpose Input/Output
	rmii1_tx_en	1	RMII1 Tx enable

GPIO	GPIO Function	GPIO_CFG[5:2] (FUNC_SEL)	Function description
	aud_pin_pcm_dtx	2	Transmitted data of Audio PCM interface
	led(9)	4	LED9
49	GPIO_IN_OUT(49)	0	General Purpose Input/Output
	rmii1_rx_er	1	RMII1 Rx error in master mode; RMII1 Tx error in slave mode
	aud_pin_pcm_drx	2	Received data of Audio PCM interface
	led(10)	4	LED10
50	GPIO_IN_OUT(50)	0	General Purpose Input/Output
	rmii1_txd(0)	1	RMII1 Tx data 0
	aud_pin_pcm_pclk	2	Clock of Audio PCM interface
	wifi0_rfsilient_bb	3	wifi_2g RF silent signal (RF_kill)
	wifi1_rfsilient_bb	4	wifi_5g RF silent signal (RF_kill)
	led(11)	5	LED11
51	GPIO_IN_OUT(51)	0	General Purpose Input/Output
	rmii1_txd(1)	1	RMII1 Tx data 0
	aud_pin_pcm_fsync	2	Frame start indication of Audio PCM interface
	wifi0_cal_xpa_active	3	wifi_2g xPA control signal used for test purpose
	wifi1_cal_xpa_active	4	wifi_5g xPA control signal used for test purpose
52	GPIO_IN_OUT(52)	0	General Purpose Input/Output
	qpic_pad_te	1	LCDC TE, VSYNC input
	mdc	2	Management Data Clock
	pcie_clk_req_n	3	PCIe clock request, low active
	audio_txmclk	4	Master clock source of Audio I^2S/TDM Tx interface
53	GPIO_IN_OUT(53)	0	General Purpose Input/Output
	qpic_pad_busy_n	1	NAND busy_not_ready input. Active low.
	mdio	2	Management Data Input/Output
	audio_txbclk	3	Bit clock of Audio I^2S/TDM Tx interface
54	GPIO_IN_OUT(54)	0	General Purpose Input/Output
	qpic_pad_lcd_rs_n	1	LCDC RESX, reset signal. Active low.
	blsp_spi0_ss0_n	2	SPI0 chip select 0
	audio_td1	3	Serial digital data output 1 of Audio multi-channel I^2S Tx interface and serial digital data of Audio TDM Tx interface
55	GPIO_IN_OUT(55)	0	General Purpose Input/Output
	qpic_pad_we_n	1	NAND/LCDC write enable
	blsp_spi0_mosi	2	SPI0 master-out slave-in data
	audio_td2	3	Serial digital data output 2 of Audio multi-channel I^2S Tx interface
56	GPIO_IN_OUT(56)	0	General Purpose Input/Output
	qpic_pad_oe_n	1	NAND/LCDC read enable
	blsp_spi0_sck	2	SPI0 serial clock output
	audio_td3	3	Serial digital data output 3 of Audio multi-channel I2S Tx interface

GPIO	GPIO Function	GPIO_CFG[5:2] (FUNC_SEL)	Function description
57	GPIO_IN_OUT(57)	0	General Purpose Input/Output
	qpic_pad_dat(4)	1	NAND/LCDC data
	blsp_spi0_miso	2	SPI0 master-in slave-out data
	audio_txfsync	3	Left or Right indication of Audio I²S Tx interface and frame start indication of Audio TDM Tx interface
58	GPIO_IN_OUT(58)	0	General Purpose Input/Output
	qpic_pad_dat(5)	1	NAND/LCDC data
	led(2)	2	led2
	blsp_i2c0_sck	3	I²C0 clock
	smart_ant6	5	wifi_5g TXPCU_ANTENNA_INFO[0] (from MAC) wifi_5g serial clock for smart antenna (serial mode)
	audio_rxmclk	6	Master clock source of Audio I²S/TDM Rx interface
59	GPIO_IN_OUT(59)	0	General Purpose Input/Output
	qpic_pad_dat(6)	1	NAND/LCDC data
	blsp_i2c0_sda	2	I²C0 data
	smart_ant7	4	wifi_5g TXPCU_ANTENNA_INFO[1] (from MAC) wifi_5g serial Data for smart antenna (serial mode)
	audio_spdifin	5	Audio SPDIF input
60	GPIO_IN_OUT(60)	0	General Purpose Input/Output
	qpic_pad_dat(7)	1	NAND/LCDC data
	blsp_uart0_rxd	2	UART0 receive data
	smart_ant4	3	wifi_2g TXPCU_ANTENNA_INFO[0] (from MAC) ifi_2g serial clock for smart antenna (serial mode)
	led(0)	5	LED0
	audio_txbclk	6	Bit clock of Audio I²S/TDM Tx interface
	audio_rxbclk	7	Bit clock of Audio I²S/TDM Rx interface
61	GPIO_IN_OUT(61)	0	General Purpose Input/Output
	qpic_pad_lcd_cs_n	1	LCD chip select
	blsp_uart0_txd	2	uart0 transmit data
	smart_ant5	3	wifi_2g TXPCU_ANTENNA_INFO[1] (from MAC) wifi_2g serial Data for smart antenna (serial mode)
	led(1)	5	LED1
	audio_txfsync	6	Left or Right indication of Audio I²S Tx interface and frame start indication of Audio TDM Tx interface
	audio_rxfsync	7	Left or Right indication of Audio I²S Rx interface and frame start indication of Audio TDM Rx interface
62	GPIO_IN_OUT(62)	0	General Purpose Input/Output
	qpic_pad_cle_lb_n	1	NAND CLE/LCDC DCX CLE is command latch enable. Active high. DCX is data/commend. 1 is data, and 0 is command.
	chip_rst_out	2	Chip reset out, low active
	wifi0_uart_txd	3	wifi_2g UART transmit data
	wifi1_uart_txd	4	wifi_5g UART transmit data

GPIO	GPIO Function	GPIO_CFG[5:2] (FUNC_SEL)	Function description
	audio_spdifout	5	Audio SPDIF output
63	GPIO_IN_OUT(63)	0	General Purpose Input/Output
	qpic_pad_nand_cs_n	1	NAND chip select
	wifi0_uart_rxd	2	wifi_2g UART receive data
	wifi1_uart_rxd	3	wifi_5g UART receive data
	wifi1_uart_txd	4	wifi_5g UART transmit data
	audio_td1	5	Serial digital data output 1 of Audio multi-channel I^2S Tx interface and serial digital data of Audio TDM Tx interface
	audio_rxd	6	Serial digital data of Audio Rx interface
	audio_spdifout	7	Audio SPDIF output
	audio_spdifin	8	Audio SPDIF input
64	GPIO_IN_OUT(64)	0	General Purpose Input/Output
	qpic_pad_dat(1)	1	NAND/LCDC data
	audio_pwm0	2	Audio Pulse Width Modulation interface 0
65	GPIO_IN_OUT(65)	0	General Purpose Input/Output
	qpic_pad_dat(2)	1	NAND/LCDC data
	audio_pwm1	2	Audio Pulse Width Modulation interface 1
66	GPIO_IN_OUT(66)	0	General Purpose Input/Output
	qpic_pad_dat(3)	1	NAND/LCDC data
	audio_pwm2	2	Audio Pulse Width Modulation interface 2
67	GPIO_IN_OUT(67)	0	General Purpose Input/Output
	qpic_pad_dat(0)	1	NAND/LCDC data
	audio_pwm3	2	Audio Pulse Width Modulation interface 3
68	GPIO_IN_OUT(68)	0	General Purpose Input/Output
	qpic_pad_dat(8)	1	NAND/LCDC data
69	GPIO_IN_OUT(69)	0	General Purpose Input/Output
	qpic_pad_ale_lb_n	1	NAND ALE. Active high.

4 Power

4.1 Power rails

The power rails on AP.DK04 are as below:

- 12 V to 5 V for USB operation
- 12 V to 5 V for xPA
- 12 V to 3.3 V for IPQ4019/IPQ4029 VDD33, 2 GHz XLNA, and Ethernet PHY
- 12 V to 3.3 V for PCIe mini card
- 12 V to 1.35 V for IPQ4019/IPQ4029 1.5/1.35 V DDR3/L
- 12 V to 1.1 V for IPQ4019/IPQ4029 DVDD11
- 12 V to 1.1 V for IPQ4019/IPQ4029 2 GHz and 5 GHz radio

Refer to DP25-Y9761-212 for detailed power rail and regulator design.

4.2 Internal regulators in IPQ4019/IPQ4029

- One VTT LDO, 80 mA, providing common mode voltage for DDR3 Address/CMD/control signals
- PLL LDO. This LDO output cleans 1.1 V from pin AA4, then feed to internal PLL including AVDD_PLL, AVDDPLL_FEPHY, AVDDPLL_PCIE, AVDDPLL_PSGMII, AVDDPLL_USB3, AVDDTXCLK_USB3, VDD11_PLL, and VDD11_PLL_D.

NOTE: This LDO is dedicated for internal PLL and not for the rest 1.1 V.

- 2.7 V LDO, 20 mA, only for BIAS generator

4.3 GPIO power domain

GPIO is to distribute top/bottom/left/right of chip, and power rail is also independent. Table 4-1 shows detailed power domain information for GPIO.

Table 4-1 GPIO power domain

Group	Power source pin	Internal LDO source pin	GPIO	note
Top	D17		0/1/2/3/4/5	This domain can be feed with power no more than 3.3 V.
Left	J4/K4		6-19	These two power pins bond together internally and should feed same voltage no more than 3.3 V externally.
Bottom	AD12	AD11	20-35	Powered by internal LDO, can be configured as 1.5 V/1.8 V/2.5 V/3.0 V, and pin AD11 is 3.3 V power input pin to internal LDO.
Right0	AA24/Y24		36-51	These two power pins bond together internally and should feed same voltage no more than 3.3 V externally.
Right1	R24	T24	52-69	Powered by internal LDO, can be configured as 1.5 V/1.8 V/2.5 V/3.0 V, and pin T24 is 3.3 V power input pin to internal LDO.

4.4 Power sequencing

The IPQ4019/IPQ4029 devices must be powered up in a definite sequence to ensure safe and reliable operation. Figure 4-1 shows the details on power sequencing for an IPQ4019/IPQ4029 system.

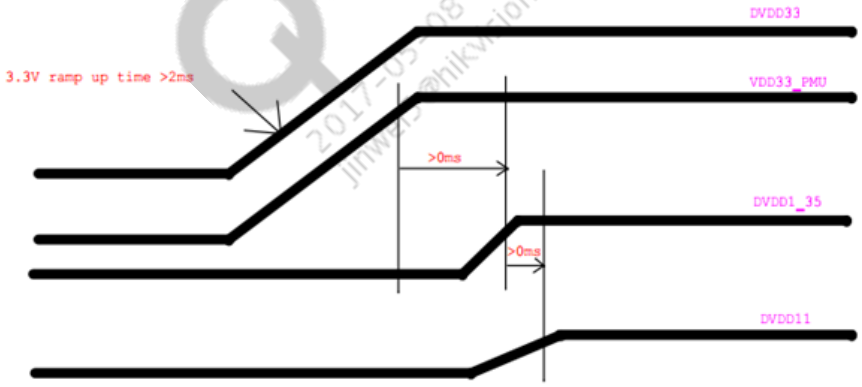


Figure 4-1 Power sequencing for an IPQ4019/IPQ4029 system

For DVDD11 and DVDD1_35 DCDC controller, enable signal is from 3.3 V, then to tune power on sequence between DVDD33/DVDD11 DVDD1_35.

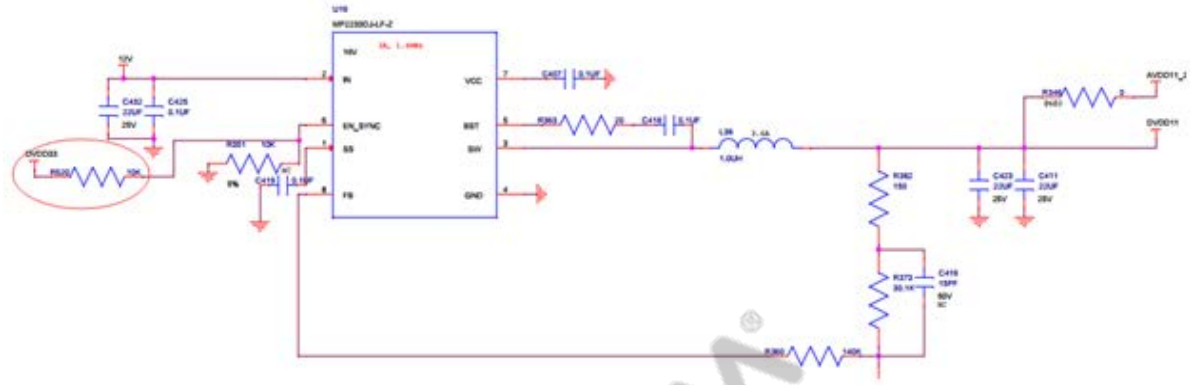


Figure 4-2 DVDD11 DCDC part schematic

Figure 4-3 DVDD1_35 DCDC part schematic

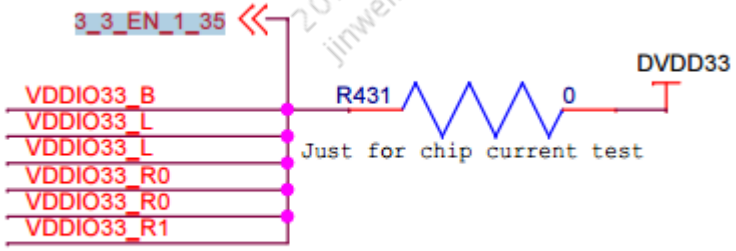


Figure 4-4 Net 3_3_EN_1_35 schematic

To get reliable warm hardware reset, keep asserting CHIP_PWD_L low for at least 10 ms.

A power-up RC (10 k/1 µF) circuit is suggested as shown in Figure 4-5.

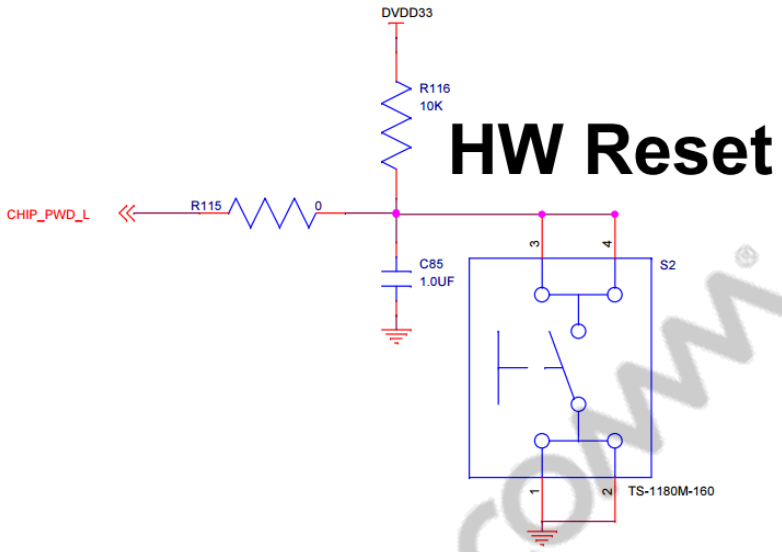


Figure 4-5 Recommended Power-up RC circuit

NOTE: It is acceptable to power down the system without a particular sequence. However, ensure a reasonable time to the next power-on to verify that the rails have drained so the subsequent power-on does not violate the power sequence. Recommend to keep the power off for a few seconds for this purpose.

4.5 IPQdecoupling

Table 4-2 shows the recommended IPQ4019/IPQ4029 decoupling values.

Table 4-2 Recommended IPQ4019/IPQ4029 decoupling values

Qualcomm® Internet Processor (IPQ) rail	Voltage (nominal) (V)	Capacitance value	Quantity
DVDD11	1.1	22 µF	2
		2.2 µF	4
		1 µF	1
		0.1 µF	31
AVDD	1.1	0.1 µF	7
AVDD_DLL	1.1	0.1 µF	1
AVDDPLL_FEPHY	1.1	0.1 µF	1
AVDD_PLL	1.1	0.1 µF	1
AVDDPLL_PCIE	1.1	0.1 µF	1
AVDDPLL_PSGMII	1.1	0.1 µF	1
AVDDPLL_USB3	1.1	0.1 µF	1
AVDDTXCLK_USB3	1.1	0.1 µF	1
VDD11_PLL	1.1	0.1 µF	1

Qualcomm® Internet Processor (IPQ) rail	Voltage (nominal) (V)	Capacitance value	Quantity
VDD11_PLL_D	1.1	0.1 µF	1
VDD11_BIAS_R0	1.1	0.1 µF	1
		0.01 µF	1
VDD11_BIAS_R1	1.1	0.1 µF	1
		0.01 µF	1
VDD11_CLKBUF_R0	1.1	47 µF	2
		0.01 µF	1
VDD11_LO_R0	1.1	10 pF	1
		1000 pF	1
VDD11_LO_R1	1.1	4.7 µF	1
		10 pF	1
		1000 pF	1
VDD11_ADDAC_R0	1.1	4.7 µF	1
		0.1 µF	1
		1000 pF	1
VDD11_ADDAC_R1	1.1	4.7 µF	1
		0.1 µF	1
		1000 pF	1
VDD11_BB_R0	1.1	0.1 µF	1
		0.01 µF	1
VDD11_BB_R1	1.1	0.1 µF	1
		0.01 µF	1
VDD11_BIAS_R0	1.1	0.1 µF	1
		0.01 µF	1
VDD11_BIAS_R1	1.1	0.1 µF	1
		0.01 µF	1
VDD11_LDO	1.1	4.7 µF	1
		0.1 µF	1
VDD11_T/RX_CH0 VDD11_T/RX_CH1	1.1	2.2 µF	1
		0.1 µF	4
VDD11_T/RX_CH2 VDD11_T/RX_CH3	1.1	2.2 µF	1
		0.1 µF	4
VDD33_BB_R0	3.3	0.1 µF	1
		0.01 µF	1
VDD33_BB_R1	3.3	0.1 µF	1
		0.01 µF	1
VDD33_BBPLL_R0	3.3	2.2 µF	1
		0.01 µF	1
VDD33_BBPLL_R1	3.3	2.2 µF	1
		0.01 µF	1
VDD33_PMU	3.3	4.7 µF	1

Qualcomm® Internet Processor (IPQ) rail	Voltage (nominal) (V)	Capacitance value	Quantity
		0.1 µF	1
VDD33_SYN_R0	3.3	10 pF	1
		1000 pF	1
VDD33_SYN_R1	3.3	10 pF	1
		1000 pF	1
VDD33_VCO_R0	3.3	10 pF	1
		1000 pF	1
VDD33_VCO_R1	3.3	10 pF	1
		1000 pF	1
VDD33_XO	3.3	0.01 µF	1
		1000 pF	1
VDDIO_LDO_B	1.8	1 µF	1
		0.1 µF	1
VDDIO_LDO_R1	3.3	1 µF	1
		0.01 µF	1
VDDIO_R0	1.5	10 µF	1
		0.1 µF	5
VDDIO_R1	3.3	0.1 µF	2
VDDIO33_B	1.1	0.1 µF	1
VDDIO33_L_1	3.3	0.1 µF	1
VDDIO33_L_2	3.3	0.1 µF	1
VDDIO33_R0_1	3.3	0.1 µF	1
VDDIO33_R0_2	3.3	0.1 µF	1
VDDIO33_R1	3.3	0.1 µF	1
VDDIO33_T	3.3	0.1 µF	1
VDD15	1.35	1.0 µF	1
		0.1 µF	5
		10 pF	1
VTT	0.675	10 µF	1
		1.0 µF	1
		0.1 µF	6
		10 pF	1
VDDQ	1.35	10 µF	1
		1.0 µF	1
		0.1 µF	6
		10 pF	1
AVDD25_REG	2.62	1 µF	1
		0.1 µF	1

NOTE: Detailed configurations will be updated base on final test result.

See Figure 4-6 for the recommended layout for the decap vias. Short wide connections to vias as close as possible using a symmetric pattern minimizing the inductance on both power lead and GND lead. Where possible, 0201 components can be inlined with the vias. 0402 components can be placed side-on.

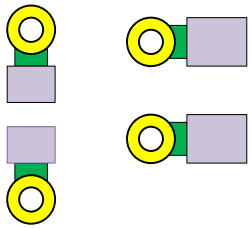


Figure 4-6 Via placement for decaps (0201, 0402)

While it is possible to use multiple vias to reduce inductance, it is not recommended due to the adverse impact on the copper plane area in the inner layers. In severely constrained areas, it may even be necessary to share vias across two capacitors. PDN simulations and board validation have shown satisfactory results with these approaches.

5 Thermal Considerations

Careful consideration is required of the thermal dissipation on the system board taking the power dissipation of the IPQ4019/IPQ4029 and other system peripherals into account. Thermal simulation is recommended.

5.1 IPQ4019/IPQ4029 thermal characteristics

Table 5-1 lists the thermal characteristics of the IPQ4019/IPQ4029.

Table 5-1 IPQ4019/IPQ4029 thermal characteristics

Parameter		Comment	Typical
θ_{JA}	Junction-to-Ambient	▪ JEDEC JESD51-2A ▪ JEDEC JESD51-7	21 °C/W
θ_{JB}	Junction-to-Board	▪ JEDEC JESD51-7 ▪ JEDEC JESD51-8 ▪ Cold plate ring maintained at 25°C at top and bottom of PCB	4.89 °C/W
θ_{JC}	Junction-to-Case	▪ No thermal vias ▪ JEDEC JESD51-7 ▪ JEDEC JESD51-8 ▪ Cu block at top of package maintained at 25°C	3.59 °C/W
ψ_{JT}	Junction-to-Top	▪ JESD51-2A ▪ JESD51-7	0.03 °C/W

5.1.1 Thermal design guidelines

- Thermal flow equals GND current flow
  - Essentially the same problem, heat flows where current flows – in copper
  - Greater copper cross section
    - More heat flow, more current flow Via and GND structure under chip
- Vertical copper cross section
  - Move the heat to other layers
  - Internal layers conduct heat horizontally
- Horizontal copper cross section
  - Avoid a fence of non-GND vias (reduces horizontal copper)
  - Internal layers cannot get rid of heat

- Heat can be trapped on inner layers

- Top and bottom layers
  - Only way of radiating heat
  - Must have maximum GND copper possible
  - Must have vertical copper (vias) to move heat from inner layers

5.2 System thermal characteristics

The thermal dissipation of the system should be budgeted considering the overall loads, including other devices, board design, enclosure design and implementation. Try to keep complete copper plane and enough thermal vias.

5.3 PWB construction

The more copper the PWB contains, the better the thermal performance.

- Maximize the size and number of thermal vias under the devices. The AP.DK04 includes many filled vias on the GND pad for IPQ4019/IPQ4029, and puts vias on the GND pad for RF xPA (SE2623L-R and RFPA5542).
- Maximize the exposed ground plane area on the back side of the PWB.

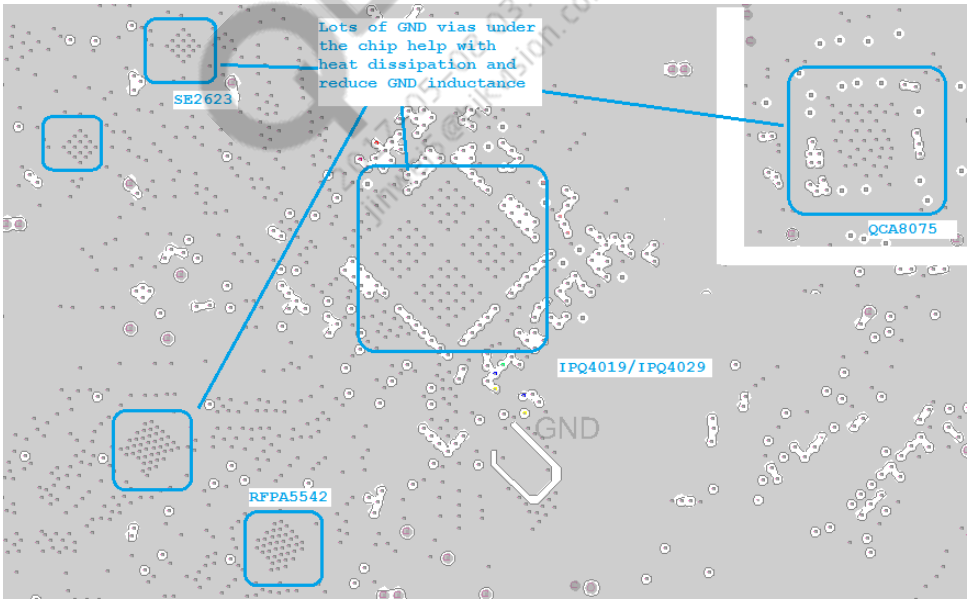


Figure 5-1 AP.DK04 thermal considerations

6 RF Design

6.1 AP.DK04 RF block description

AP.DK04 RF front-end parts include:

- U.FL connector on the board
- Tx/Rx switch
- External Tx power amplifier (xPA) per a 5 GHz radio chain
- External low noise amplifier (XLNA) 5 GHz radio chain
- External Tx power amplifier (xPA) per a 2.4 GHz radio chain
- External low noise amplifier (XLNA) 2.4 GHz radio chain
- Coupler
- RF filters, including 2 GHz RF BPF, 5 GHz RF BPF, and other T or pi networks

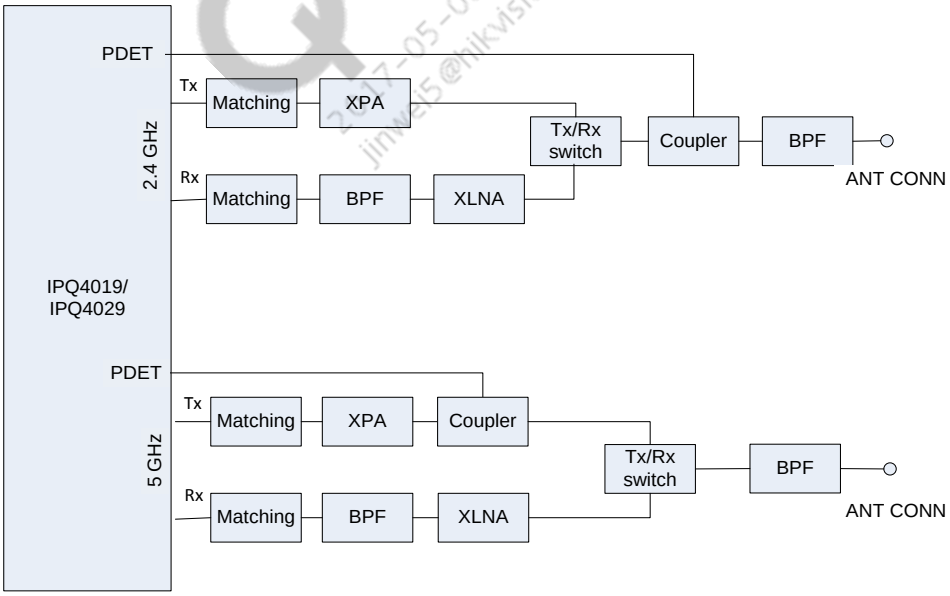


Figure 6-1 AP.DK04 RF block diagram

6.1.1 2.4 GHz external power amplifier

Each transmit radio chain has an external power amplifier (xPA) to increase WLAN rates over range and WLAN coverage. The Skyworks SE2623L-R xPA provides a system mask compliance output power above 22 dBm for HT20/40 rates when operating from a 4.5 V supply, and can exceed 15 dBm of Tx power for the highest modulation rate of 256 QAM.

6.1.2 2.4 GHz external low noise amplifier

Each receive radio chain has an external low noise amplifier (XLNA) to increase receive dynamic range and sensitivity beyond the capabilities of the internal LNAs of the IPQ4019/IPQ4029. The XLNA design uses NXP Semiconductors BGU7224, a fully integrated MMIC low noise power amplifier.

6.1.3 2.4 GHz and 5 GHz Tx/Rx switch

The Tx/Rx switch is used to toggle the antenna back and forth between transmit and receive. It must have an appropriate output, as not to degrade the Tx/Rx performance. The SKY13370-374LF switch is selected for moderately high Tx power handling, and modest loss and low-cost tradeoffs.

6.1.4 2.4 GHz band pass filter

Two different band pass filters (BPFs) are used. The BPF near ANT is used to filter out the high 2/3 LOs, and 4/3 LOs leaked from the IPQ4019/IPQ4029, and to retain some of the spurs that fall in restricted bands below the FCC limit (-41 dBm/MHz in conducted 50 Ω system or 500 μV/m at 3 mts in field strength). The BPF on the Rx path near IPQ4019/IPQ4029 is used to filter out the 5 GHz radio for DBDC operation and cellular signal.

6.1.5 2.4 GHz and 5 GHz coupler

Coupler TDK TFSC06054125-2120A1 is used to feed the Tx signal back to the IPQ4019/IPQ4029 for digital pre-distortion (DPD). The IPQ4019/IPQ4029 uses this signal to allow the DSP process and to achieve better Tx linearity with the same power consumption. DPD reads during normal mode. This path is also used for close loop power control (CLPC).

The 5 GHz design includes a coupler behind the PA to avoid LO signal coupling to the Rx path.

6.1.6 5 GHz external power amplifier

Each Tx radio chain has an external power amplifier (xPA) to increase WLAN rates over range and WLAN coverage. The RFMD RFPA5542 5 GHz xPA provides a system mask compliance output power above 22 dBm for HT20/40 rates when operating from a 5.0 V supply, and can exceed 15 dBm of Tx power for the highest modulation rate of 256 QAM, 5/6 encoding and 80 MHz bandwidth (VHT80 MSC9).

6.1.7 5 GHz external low noise amplifier

Each Rx radio chain has an external low noise amplifier (XLNA) to increase the Rx dynamic range and sensitivity beyond the capabilities of the internal LNAs of the IPQ4019/IPQ4029. The LNA design uses the NXP Semiconductors BGU7258, a fully integrated MMIC LNA.

6.1.8 5 GHz band pass filter

The band pass filter (BPF) is used to filter out the high 2/3 LOs, and 4/3 LOs leaked from the IPQ4019/IPQ4029, and to retain some of the spurs that fall in restricted bands below the FCC limit (-41 dBm/MHz in conducted 50 Ω system or 500 μV/m at 3 MTS in field strength).

6.1.9 5 GHz high pass filter

The discrete HPF is used in DBDC operation. The HPF filters out the high 2 GHz Tx power transmitted by other 2 GHz WLAN radios, and prevents saturation of the 5 GHz RF front end.

6.1.10 Board designs with on-chip 2.4 GHz-only Wi-Fi

Based on the IPQ4018/IPQ4019/IPQ4028/IPQ4029 hardware architecture, crystal calibration can be achieved only with the on-chip 5 GHz Wi-Fi radio. For products where the on-chip 5 GHz radio is not used, Qualcomm recommends adding an RF test point at 5 GHz DA output, see Figure 6-2.

- Add RF connector on C8 (DA5_CH2) through 2.2 pF capacitor.

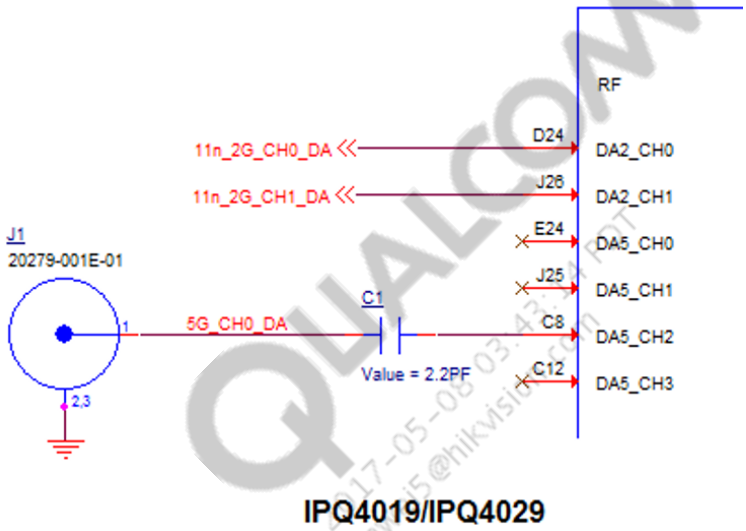


Figure 6-2 RF connector is added on 5 GHz DA output

See *IPQ4018/IPQ4019/IPQ4028/IPQ4029 Crystal Calibration for 2.4 GHz-only Design Application Note* (80-Y9700-7) for more information.

6.1.11 DC regulator for AVDD11_2G and AVDD11_5G power supply

In AP.DK04 design, the MPS MP1498DJ-LF DC regulator (U18) provides power supply for AVDD11_2G and AVDD11_5G. Tx EVM performance can benefit from separate power supply for these two power domains. Qualcomm recommends following AP.DK04 design.

Requirement of regulator specifications:

- Switching frequency at least 1.0 MHz
- Output current at least 2.0 A

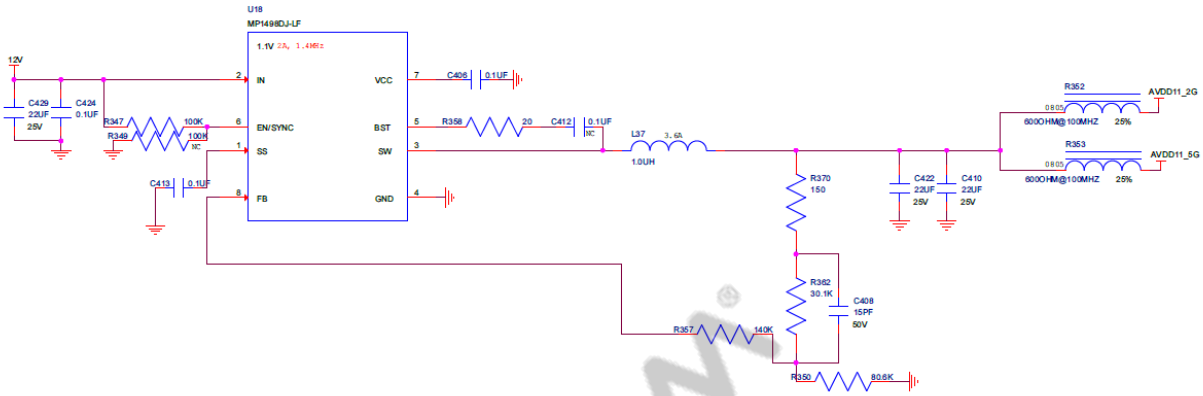


Figure 6-3 DC regulator for AVDD11_2G and AVDD11_5G power supply

6.2 RF layout guidelines

6.2.1 RF traces

All RF, Rx, and Tx traces must be 50 Ω. Qualcomm Technologies recommends all RF components and traces to be on the same side of the board.

Via should be avoided in the RF traces as much as possible. Do not use any test points on any RF traces or component.

- Ground plane with enough asymmetric via close to RF trace.
- Ground via should close to component pad as possible.

Minimize the length of all RF traces since FR4 material incurs losses at RF frequencies. Minimizing trace length reduces the overall signal loss.

With the AP.DK04 stackup, the 50 Ω trace is a 7-mil wide microstrip on the top layer reference to the GND plane on the second layer and bottom layer reference to the GND plane on the third layer.

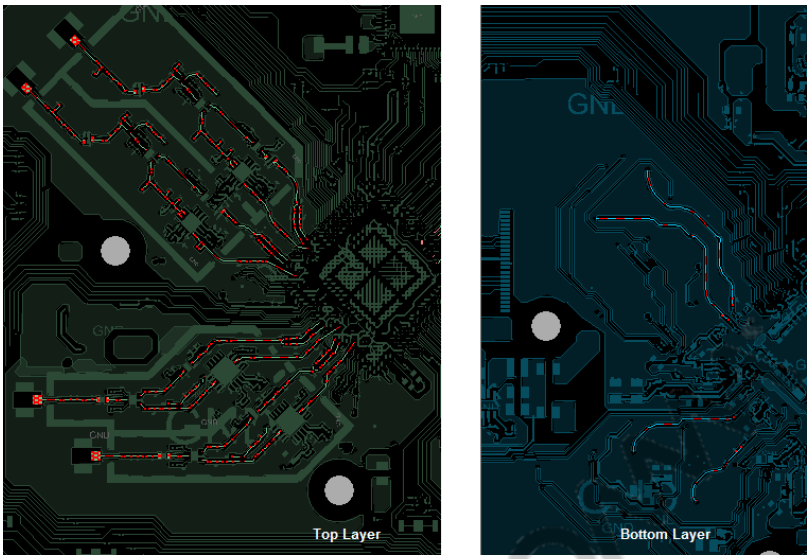


Figure 6-4 AP.DK04 RF traces

6.2.2 RF connector

Because the RF signal passes from an on-board RF trace to the middle pin of RF connector, the diameter of that pin is much thicker than RF trace that requires the reference GND be further away. Do not put metal under the U.FL connectors on layer 1 and 2. Make sure that the ground is present on all other layers of the board.

Do not put metal under the U.FL connectors (J26, J27, J28, and J30) on layer 1 to 2. Make sure that the ground is present on all other layers of the board to keep 50 Ω impedance control.

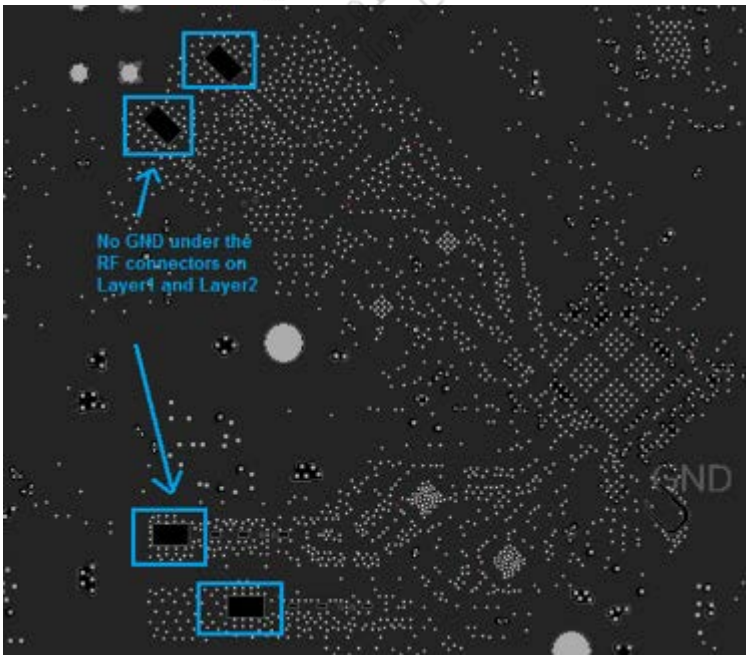


Figure 6-5 AP.DK04 RF connector layout guideline

6.2.3 DPD feedback traces

The IPQ4019/IPQ4029 design includes a coupler to feed the Tx signal back to chip to get the DPD scheme. Treat this path as a 50 Ω RF trace reference to solid GND.

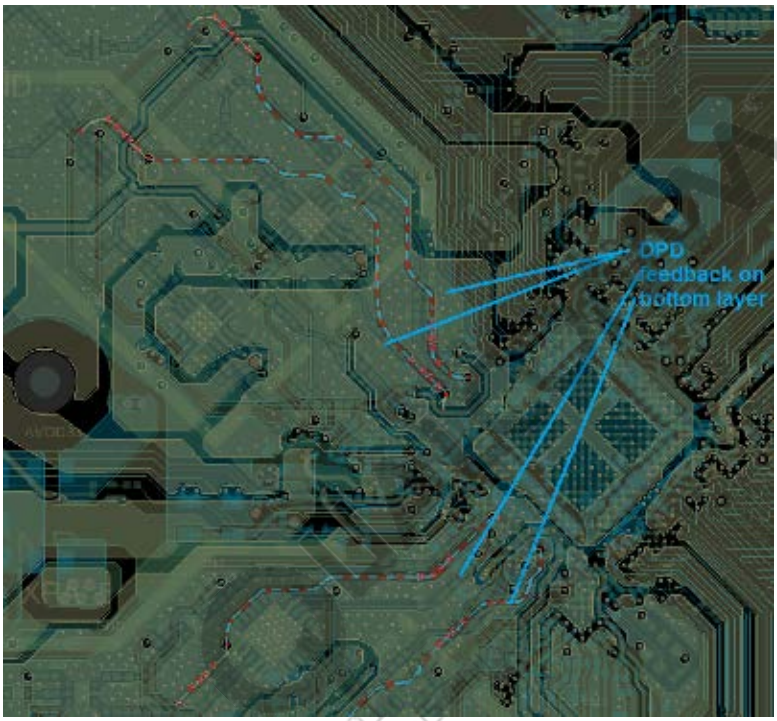


Figure 6-6 AP.DK04 DPD feedback layout guideline

6.2.4 Discrete Balun on Rx

The wrong placement of those 6 components can easily degrade Rx performance, thus the best approach is to follow the exact placement from the reference design and keep the whole circuit tight and close to IPQ4019/IPQ4029 input pins.

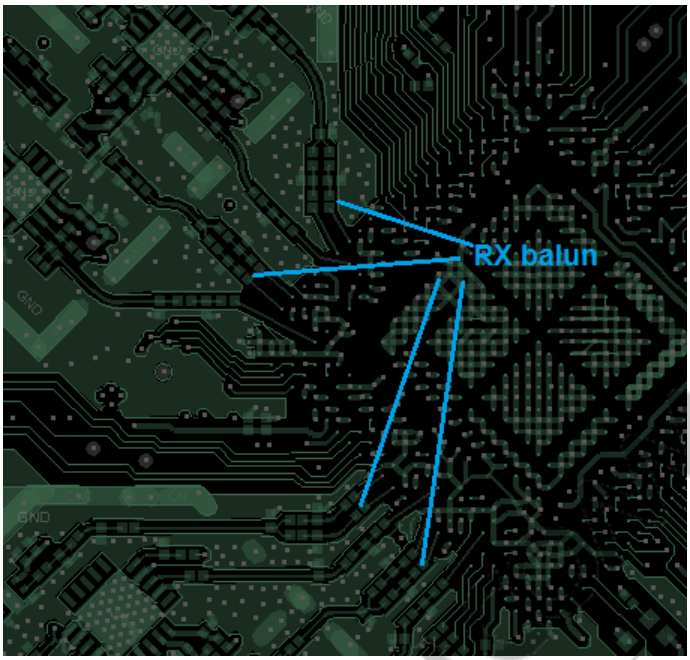


Figure 6-7 AP.DK04 Rx discrete Balun layout guideline

6.2.5 Matching circuit on Tx

Place the matching circuit (3 components) tight and close to IPQ4019/IPQ4029 output pins.

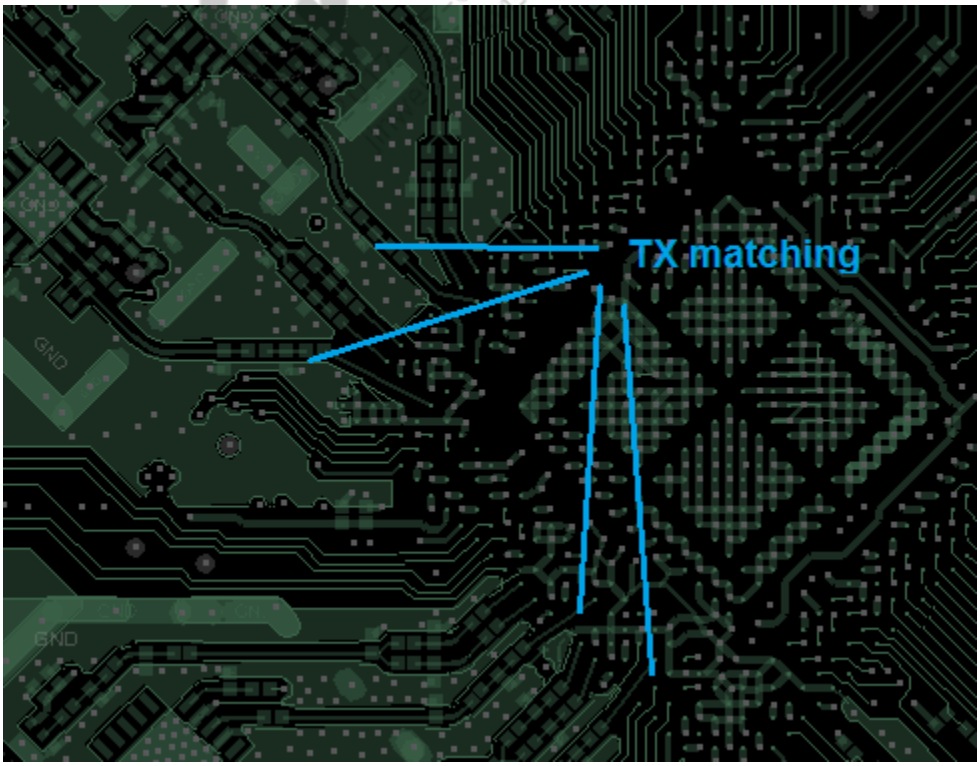


Figure 6-8 AP.DK04 Tx matching layout guideline

6.2.6 RF shields

RF shields are required for adequate operation of the AP.DK04 reference design. The shield compartments can prevent radio-to-radio coupling.

Place 5 GHz and 2.4 GHz in difference shields to reduce the coupling between each other. In addition, walls inside one shield help to isolate the chains and break up the larger cavity into smaller ones.

The number of shield openings must be reduced to a minimum needed, that is, for routing the RF traces to connect to the antenna connector. The shield openings should be as small as possible to reduce leakage.

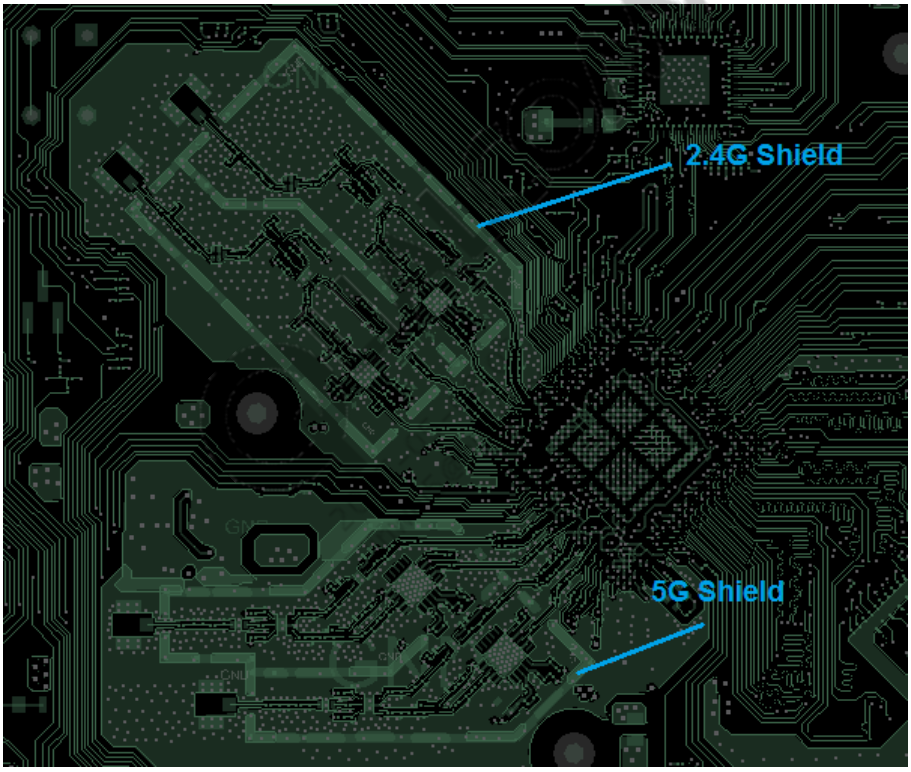


Figure 6-9 AP.DK04 RF Shield layout guideline

6.2.7 Layout guidelines for power supply

1. The Tx EVM is sensitive to noise from power.
   - Place 4.7 µF close to E5 to clean AVDD11_2G before supplying to VDD11_ADDAC_R0 (pin B19)
   - Place 4.7 µF close to E6 to clean AVDD11_5G before supplying to VDD11_ADDAC_R1 (pin C1)
   - Place C373 close to VDD11_LO_R1 (pin A3)
   - Place C317 close to VDD11_LO_R0 (pin A21)

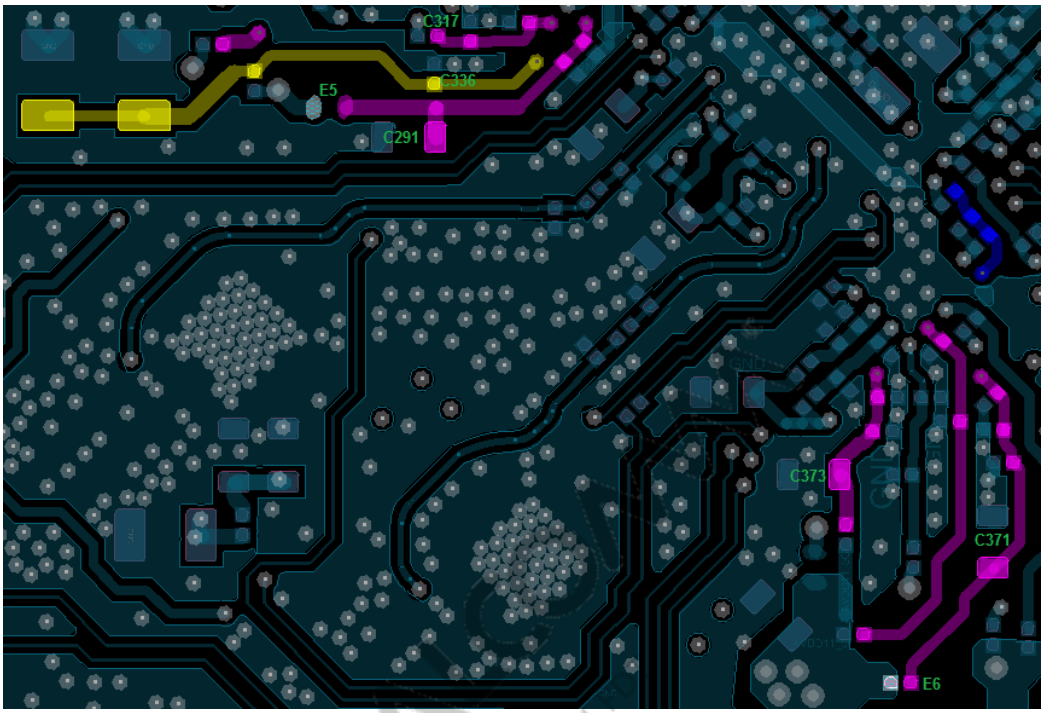


Figure 6-10 Place decoupling capacitors on AVDD11

2. Routing the power supply of AVDD11_2G, AVDD11_5G and AVDD33 by star burst topology. The placement of decoupling capacitors follows the AP.DK04 as far as possible. The decoupling capacitor should be placed as close to the power pins as possible and with minimal trace length to avoid inductance. Also, avoid long GND trace for the decoupling capacitor's GND, and provide quick via to GND plane rather than a long trace.

   The placement priority of decoupling capacitors:

   a. AVDD11

   b. AVDD33

   c. DVDD11, DVDD33, and others

   The smaller decoupling capacitors (10 pF) in schematic shall be placed close to IPQ4019/IPQ4029 pins.

   Most AVDD is routing on layer 3 and bottom layer, stay away from 48 MHz crystal areas. Only a few AVDD domains can be on the top layer; follow AP.DK04 as far as possible.

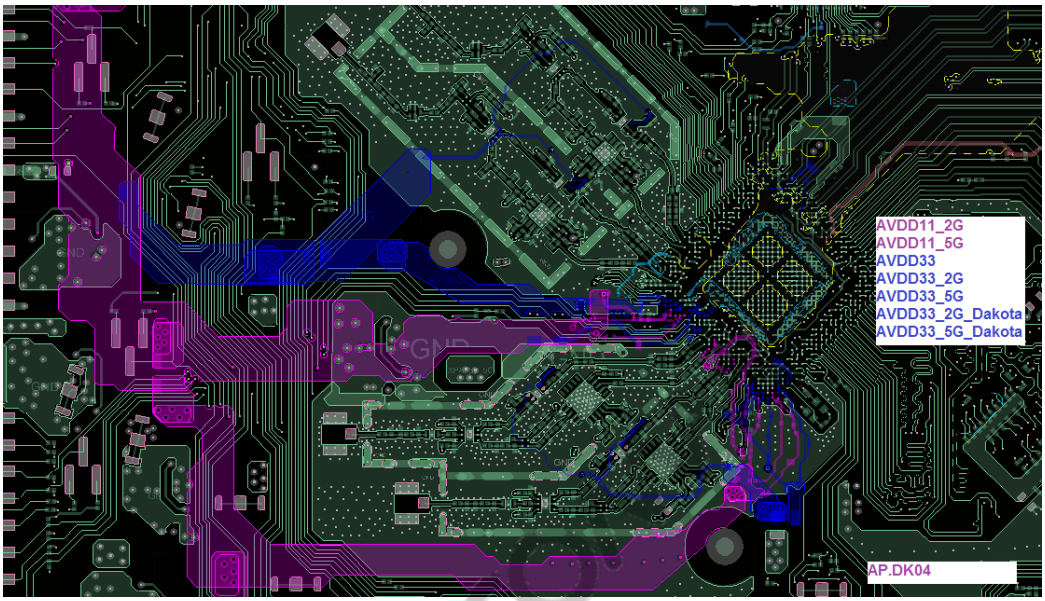


Figure 6-11 Layout guidelines for AVDD11 and AVDD33

6.2.8 Additional guidelines

- Use at least 0805 size 0 Ω for the AVDD11 and DVDD11 power source.
- Avoid using a thin trace for AVDD11 and DVDD11.
- Avoid an overlap between AVDD33 and the AVDD11 power plane.
- Avoid an overlap between VDD11_LDO and the AVDD11 power plane.
- Avoid an overlap between the AVDD11 power plane and all four XLNA_0/1 signal traces on the nearby layers.
- Separate the power source between XPA_5V_2G and XPA_5V_5G. Avoid an overlap between XPA_5V_2G and XPA_5V_5G.
- Avoid the coupling between AVDD11 and IPQ4019/IPQ4029 RF input traces.
- Avoid the coupling between DVDD11 and IPQ4019/IPQ4029 RF input traces.
- Avoid the coupling between XLNA_0/1 lines and IPQ4019/IPQ40299 RF input traces.
- Avoid the coupling between PDET traces and IPQ4019/IPQ4029 RF input traces.
- Avoid the coupling between PDET traces and ANT port.
- Avoid the coupling between PDET traces and xPA Tx input trace.
- Avoid the coupling between FEM_0/1 traces and XLNA_0/1 lines.
- Avoid routing XPA_5V (supply to xPA) and VDD11 on top layer or bottom layer.

6.3 Antenna placement on the AP

This section lists the recommendations to optimize antenna performance when using external dual-band dual-feed antennas.

- Maximize physical separation of all antennas.

  The minimum separation distance is 60 mm or 2.5 in. to get the minimum 15-dB isolation. Optimum performance at 2.4 GHz is typically achieved with spacing greater than 90 mm or 3.5 in.

- Allow the antennas to rotate so they are not all forced to remain vertical.

  Best MIMO performance is typically obtained with some polarization diversity. This frequently occurs with two antennas tilted -45 degrees from vertical and two tilted +45 degrees from vertical.

- Locate the antennas so they are clear of obstructions and not blocked by boards, shields, heat sinks, etc. Each antenna should have a clear omnidirectional path.

- Do not locate all of the antennas in a straight line.

  This typically results in nulls in the MIMO coverage when the line through the antennas points at the client device.

- Locate the antennas away from USB3 interface PWB traces, connectors, or cables.

  Separate by 90 mm or 3.5 in., if possible. Ideally, the USB port should be located near the center of the rear panel, thus placing the antennas on each of the corners far away from the USB port in the center. A shield cover over the USB3 traces is not required in the most recent Qualcomm Technologies designs.

- Locate the antenna away from PCIe bus, PCIe traces, and connectors.

  Test results indicate that radiating interference from PCIe 2.0 falls into the 2.4 GHz band and affects the 2.4 GHz radio.

- Locate the antenna away from QCA8075, PSGMII traces, and connectors.
- Antenna cable routing shall avoid high-speed I/O area (PSGMII, USB3.0 PCIe2.0 and DDR).
- Separate the 2.4 GHz and 5 GHz ANT traces to get at least 20 dB isolation for DBDC mode.

7 QCA8075 Five-Port 10/100/1000 Mbps Ethernet Transceiver

The QCA8075 Ethernet transceiver is a five-port, 10/100/1000 Mbps tri-speed Ethernet PHY.

The QCA8075 includes two SerDes. One can be configured to PSGMII or QSGMII for connection with MAC. The other can be configured to SGMII for connection with MAC or fiber port combined with copper port 4 to form a combo port.

AP.DK04 application as shown in Figure 7-1, IPQ4019/IPQ4029 connects with QCA8075 through PSGMII interface, which runs at 6.25 Gbps.

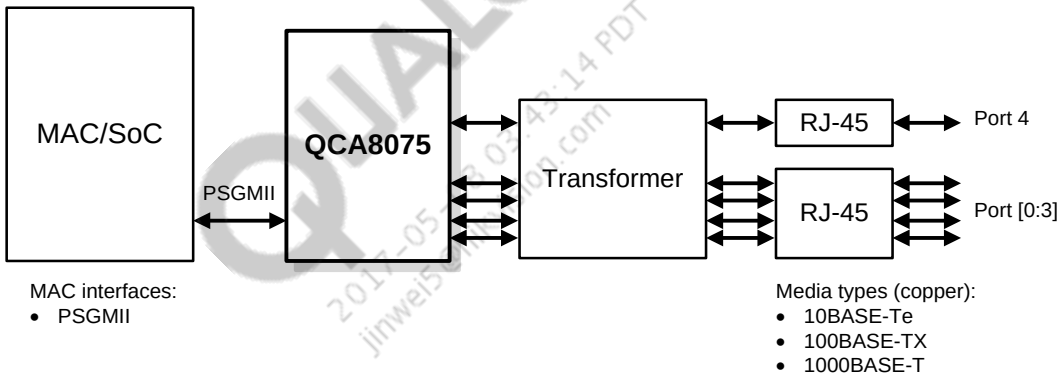


Figure 7-1 PSGMII connection

Besides PSGMII, there is MDC/MDIO, reset, and clock connection between the two chips.

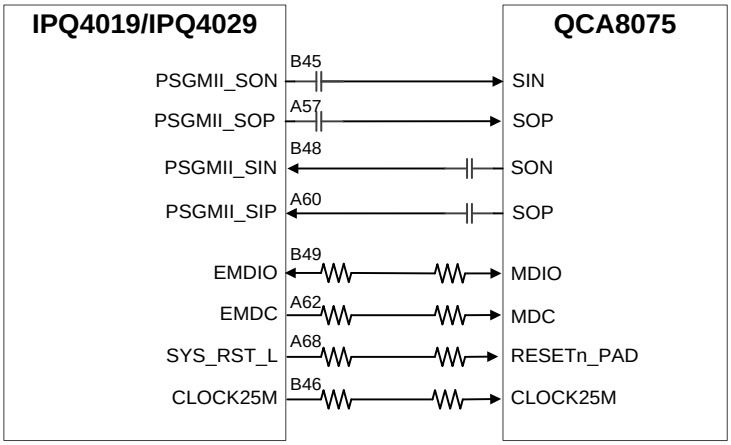


Figure 7-2 MDC/MDIO, reset, and clock connection

7.1 Reset

QCA8075 requires reset signal must be asserted and kept low for at least 1 ms after 3.3 V power and reference clock signals become stable. 3.3 V rising duration from 10% to 90% must be larger than 0.5 ms. The subsequent warm hardware reset needs at least 1 ms.

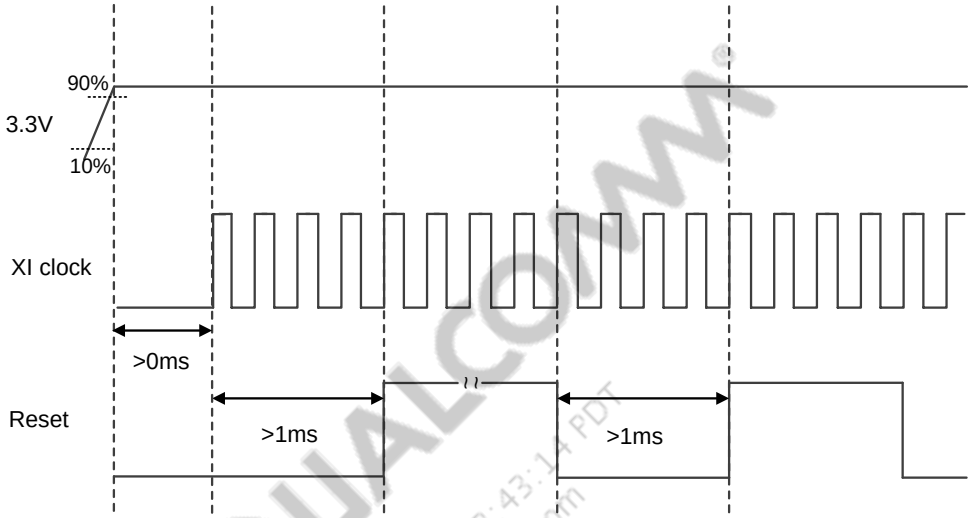


Figure 7-3 QCA8075 reset timing diagram

In AP.DK04, both the reset and clock source is from IPQ4019/IPQ4029, so a long enough power-up reset is needed for IPQ4019/IPQ4029. Follow the RC circuit setting.

7.2 Clock

QCA8075 requires an external 25 MHz clock input. In AP.DK04, it is sourced by IPQ4019/IPQ4029.

The clock amplitude is limited to 1.2 V.

7.3 Power

QCA8075 only requires 3.3 V input. All the other power rails are generated by internal regulators.

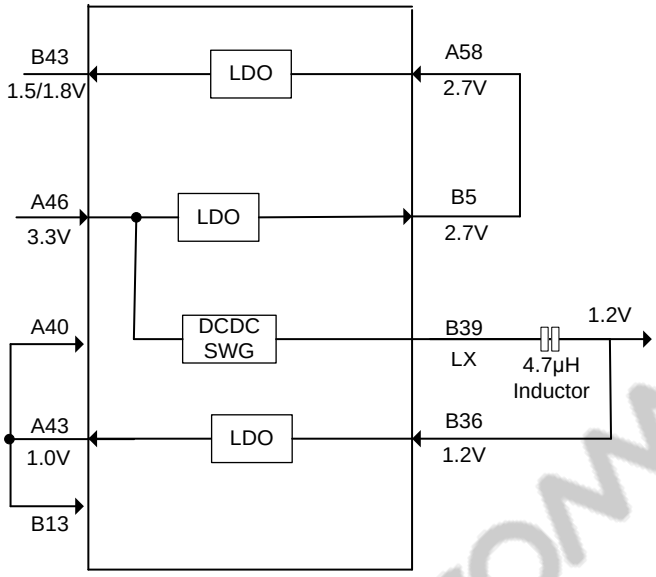


Figure 7-4 QCA8075 power supply

Table 7-1 QCA8075 power description

Symbol	Pin	Description
FILCAP_0	B7	1 µF + 0.1 µF
FILCAP_1	A27	1 µF + 0.1 µF
AVDD33	B2, B6, B10, A21,A24, B26, A37	3.3 V analog power input, 0.1 µF close to each pin
VDD33	A46	3.3 V digital power input for switch regulator, 22 µF+0.1 µF close to pin
AVDD12	A5, A10, A13, B15, B18, B21, A29, B28, B31, A55, B46, B52	1.2 V analog power input, 0.1 µF close to each pin
DVDD10	B13, A40	1.0 V digital power input, connect to pin A43, 0.1 µF close to each pin
VDDIO_25	A58	2.7 V digital I/O power and the power supply for VDD15_REG LDO 0.1 µF close to pin
AVDD12_S	B34	1.2 V analog power input for SGMII, connect to pin B36 with a bead. 0.1 µF close to pin
AVDD12_PQ	A56	1.2 V analog power input for PSGMII/QSGMII Connect to pin B36 with a bead. 0.1 µF close to pin
AVDD25	B23	Connect a 0.1 µF capacitor to ground. This pin is connected to VDD25_REG inside chip.
DVDD10_REG	A43	1.0 V regulator output for DVDD10 Connect a 4.7 µF and a 0.1 µF capacitors to stabilize this voltage.
VDD25_REG	B5	2.7 V regulator output Connect a 1 µF and a 0.1 µF capacitors to GND to stabilize this voltage.

Symbol	Pin	Description
VDD12	B36	1.2 V digital power input for 1.0 V LDO input Connect directly to the power inductor of switch regulator. Connect to AVDD12 through a bead. Place 0.1 µF close to this pin
VDD15_REG	B43	1.5/1.8 V regulator output and the I/O power for the MDC, MDIO, RESETn, INTn, WOL_INTn, and LOS Connect a 1 µF and a 0.1 µF capacitors to stabilize this voltage.
LX	B39	Inductor pin for 1.2 V switch regulator Connect an external 4.7 µH power inductor to this pin directly. Connect the other end of the inductor to B36 directly. Connect 22 µF + 1 µF + 0. 1µF ceramic capacitors to the other end of the inductor to stabilize this power supply.

NOTE: In AP.DK04, MDC, MDIO, and RESETn need to work with 3.3 V logic, so short VDD25_REG with VDD15_REG. Then, MDC, MDIO, and RESETn work at (VDD25_REG) 2.7 V rail, which can communicate with 3.3 V logic.

7.4 MDC/MDIO manage

The IEEE 802.3u clause 22-compliant management interface provides access to the internal registers of the QCA8075 transceiver via the MDC and MDIO pins.

IPQ4019/ IPQ4029 use GPIO[53] (MDIO), GPIO[52] (MDC) as MDC/MDIO interface.

The MDIO is an od-gate, which requires an external 1.5 K pull-up to QCA8075 2.7 V rail.

Table 7-2 Management interface frame fields

	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

7.5 Boot configuration

The QCA8075 includes 10 LED pins. During hardware reset, these 10 LED pins are used as input for Power-On Strapping (POS) usage. After hardware reset is released, these 10 LED pins are used as output driven by internal PHY status. The POS functions are listed in Table 7-3.

In AP.DK04, MODE[2:0] must be configured as 3’b111.

The PHY address upper 2 bits are configured as 2’b00 by default.

Table 7-3 QCA8075 POS configurations

Pin symbol	POS configuration	Description	Default internal weak pull-up/down
LED_100_0	MODE[0]	MODE[2:0] are latched to configure chip operation mode.	Pull up
LED_1000_0	MODE[1]		Pull up

Pin symbol	POS configuration	Description	Default internal weak pull-up/down
LED_100_1	MODE[2]	▪ 111 = PSGMII ▫ 5 copper ports ▪ 110 = PSGMII ▫ 4 copper ports + 1 COMBO port (copper/fiber) ▪ 101 = QSGMII +SGMII ▫ 5 copper ports ▪ Others = Reserved The operation mode can be overwritten by port4 register 0x1F[2:0].	Pull up
LED_1000_1	PHYAD3	The upper 2 bits of the physical address are set by PHYAD[4:3]. The PHYAD[2:0] are fixed to 0-5 for ports 0-4 and PSGMII respectively.	Pull down
LED_100_2	PHYAD4		Pull down
LED_1000_2	Reserved	Must be pulled up	Pull up
LED_100_3	Reserved	Must be pulled down	Pull up
LED_1000_3	Reserved	Must be pulled up	Pull up
LED_100_4	AZ_SEL	AZ_SEL is latched to MMD7 register 0x3C bits[2:1] to enable/disable IEEE 802.3 az.	Pull up
LED_1000_4	Reserved	Must be pulled up	Pull up

7.6 MDI connection

The 75 Ω termination resistors and 1 nF/2 kV capacitor between the center tap and the chassis ground (Bob Smith termination circuitry) is used to enhance the system EMI and ESD performance.

The 0.1 µF/50 V capacitors between the chassis ground and the system ground are used to enhance EMI performance. The capacitor values can be adjusted to minimize common noise.

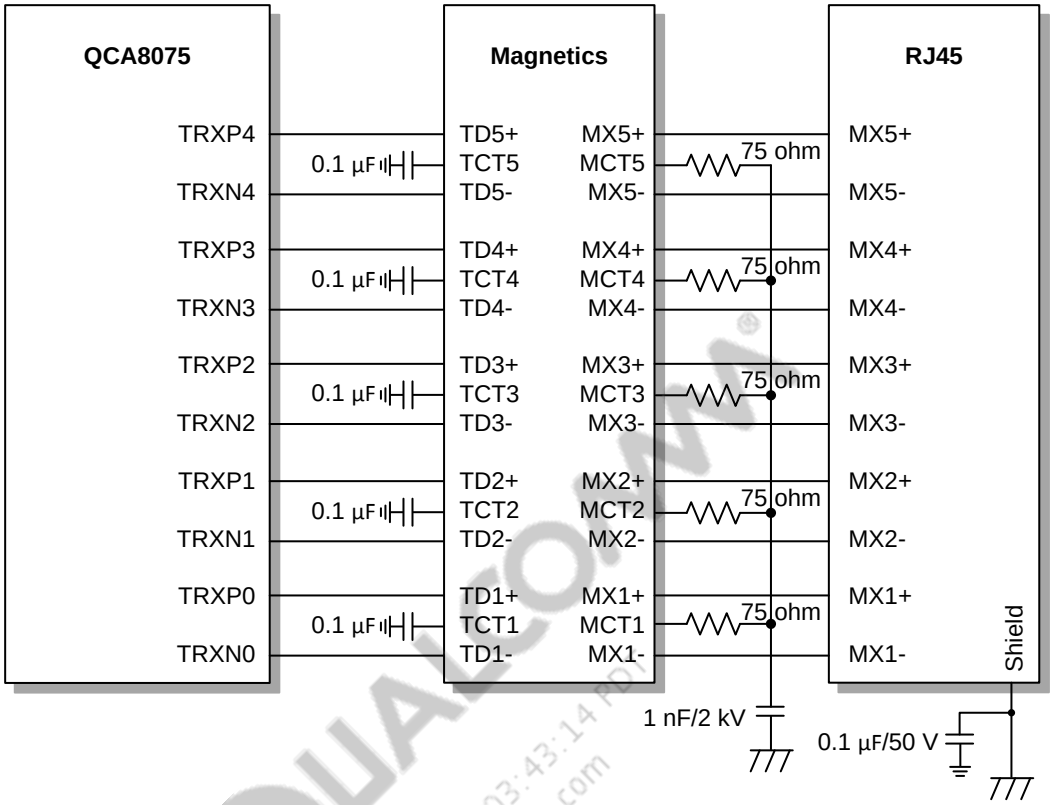


Figure 7-5 QCA8075 MDI connection

7.7 Layout guidelines

- Choose 4.7 µH inductor with 2 A current capability and low DCR.
- Place the 4.7 µH inductor on the same layer with PHY, no via. Close to chip.
- Place the decoupling capacitors for 1.2 V on the same layer with inductor.
- Pin A56 is used for PSGMII DLL. Pin B46 and A55 are used for PSGMII interface. 0 ohm or bead must place near 1.2V inductor and not allowed to share power trace. The width of AVDD12_PSGMII power trace is not less than 35 mil, and the width of AVDDPLL is not less than 12 mil.

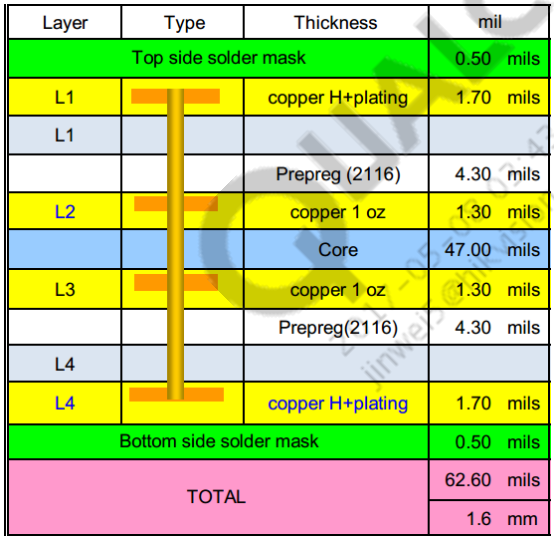
- The second layer must be solid reference GND layer for PHY. Care about the same side pin breakout vias may cut the ground under the chip.
- The chip and inductor, capacitors must be shielded with GND copper plane.
- 30 or more ground vias for E-pad.
- The length control of high-speed differential pair can refer to the edge of the package.
- Control PSGMII/MDI differential impedance 100 Ω.
- At least 80 mil isolation between magnetic two ends.
- DRQFN fan-outs, refer to section 8.3

8 Board Stackup and PCB Rules

The IPQ4019/IPQ4029 device is packaged as a 583-pin 18 x 18 0.65 mm pitched BGA. The packaging and pinout have been optimized to implement designs in as few layers as possible; a 4-layer implementation with IPQ4019/IPQ4029 is presented in this guideline.

8.1 Stackup

A cost-effective implementation can be done in four layers. Figure 8-1 illustrates a representative stackup.



Layer	Type	Thickness	mil
Top side solder mask			0.50 mils
L1		copper H+plating	1.70 mils
L1			
		Prepreg (2116)	4.30 mils
L2		copper 1 oz	1.30 mils
		Core	47.00 mils
L3		copper 1 oz	1.30 mils
		Prepreg(2116)	4.30 mils
L4			
L4		copper H+plating	1.70 mils
Bottom side solder mask			0.50 mils
TOTAL			62.60 mils
			1.6 mm

Figure 8-1 PCB stackup

- Four layer board
- Material: NAYA NP-140
- Dielectric constant 4.2 at 1 GHz

8.2 Routing features

Table 8-1 shows the trace features used for routing (in reference to the stackup in Figure 8-1). All signal traces routed on this board are micro-strip. The rules may vary by PCB manufacturer. It is more critical to meet the Z targets.

Table 8-1 Routing features

Category	Guideline/Remarks
Single-ended micro-strip trace	7 mils trace width for 50 Ωz, for RF/SDIO signal 4.5 mils trace width for 60 Ωz, for DDR3L signal
Micro-strip differential pair	4 mils trace width with 7 mils space for 100 Ωz, PCIE/PSGMII/Ethernet/DDR_CLK 7 mils trace width with 8 mils space for 90 Ωz, USB signal DDR DQS 110 Ω
Via/Drill	Smallest via: 8 mils drill; 16R8 Blind and buried vias are not used
Other notes	It is key to suppress unused pads in inner layers to obtain more space for any inner layer routing/copper. It is acceptable to neck down the traces to 4 mils wide to exit the BGA packages.

8.3 BGA fan-outs

Figure 8-2 shows the exit routing for IPQ4019/IPQ4029 in a reference design. The outermost two rows are exited on the top layer and inner pins are exited with vias on the bottom layer.

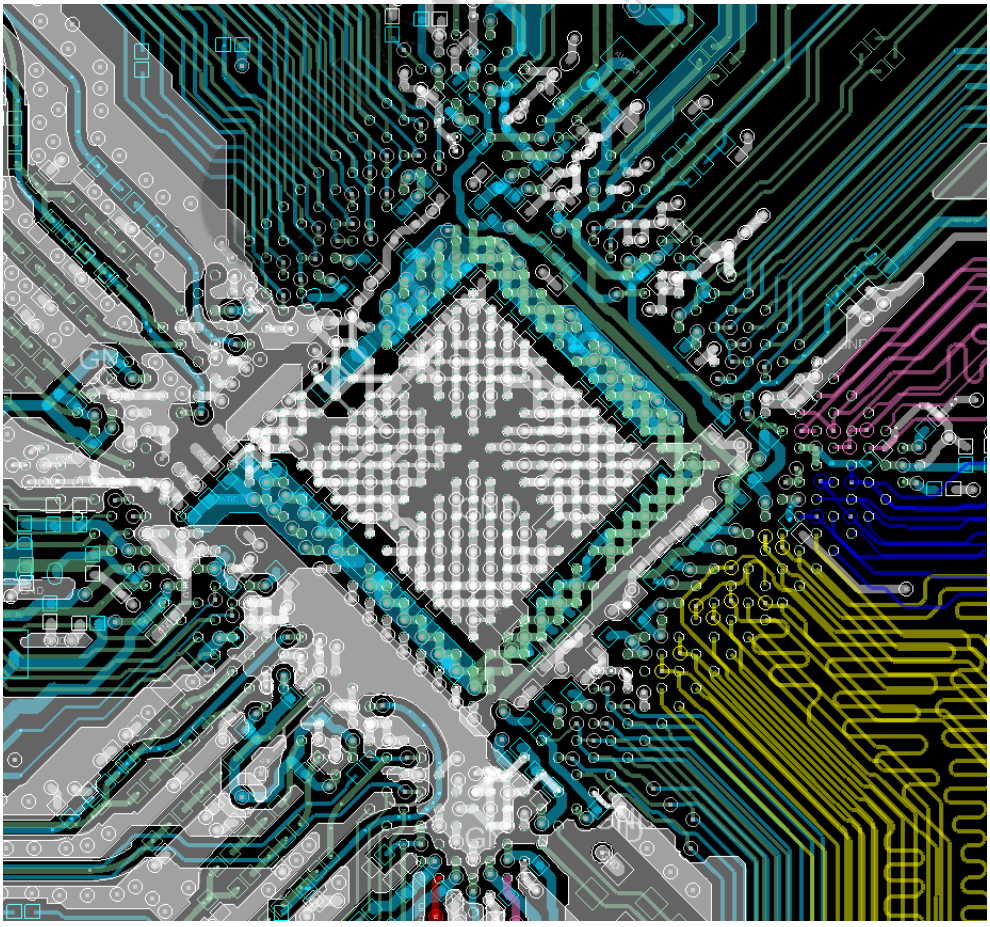


Figure 8-2 BGA exits and routing for IPQ4019/IPQ4029

It is acceptable to neck down the traces at the BGA breakouts to 4.5 mils wide, and line to line or SMD pad/VIA/hole, and so on, to four mils to obtain sufficient clearance. Unused interfaces with NC pins can ease the breakout. It is expected that most design implementations include some of these.

A Performance Characteristics

This section provides example RF performance characteristics for AP.DK04 reference design based on the IPQ4019/IPQ4029 chips.

A.1 EVM limitation

Table A-2 802.11a/g maximum EVM limits specification

Data Rate (Mbps)	Relative Constellation Error (dB, IEEE)	AP.DK04(dB) Single User	AP.DK04(dB) Multi-User
6	-5	-6	-7
9	-8	-9	-10
12	-10	-11	-12
18	-13	-14	-15
24	-16	-17	-18
36	-19	-20	-21
48	-22	-23	-24
54	-25	-26	-27

Table A-3 802.11n maximum EVM limits specification

MCS Index	Modulation	Coding Rate	Relative Constellation Error (dB, IEEE)	AP.DK04(dB) Single User	AP.DK04(dB) Multi-User
MCS 0	BPSK	1/2	-5	-6	-7
MCS 1	QPSK	1/2	-10	-11	-12
MCS 2	QPSK	3/4	-13	-14	-15
MCS 3	16-QAM	1/2	-16	-17	-18
MCS 4	16-QAM	3/4	-19	-20	-21
MCS 5	64-QAM	2/3	-22	-23	-24
MCS 6	64-QAM	3/4	-25	-26	-27
MCS 7	64-QAM	5/6	-27	-28	-29
MCS 8	BPSK	1/2	-5	-6	-9
MCS 9	QPSK	1/2	-10	-11	-14
MCS 10	QPSK	3/4	-13	-14	-17
MCS 11	16-QAM	1/2	-16	-17	-20
MCS 12	16-QAM	3/4	-19	-20	-23
MCS 13	64-QAM	2/3	-22	-23	-26
MCS 14	64-QAM	3/4	-25	-26	-29
MCS 15	64-QAM	5/6	-27	-28	-31

Table A-4 802.11ac maximum EVM limits specification

MCS Index	Modulation	Coding Rate	Relative Constellation Error (dB, IEEE)	AP.DK04(dB) Single User	AP.DK04(dB) Multi-User
MCS 0	BPSK	1/2	-5	-6	-7
MCS 1	QPSK	1/2	-10	-11	-12
MCS 2	QPSK	3/4	-13	-14	-15
MCS 3	16-QAM	1/2	-16	-17	-18
MCS 4	16-QAM	3/4	-19	-20	-21
MCS 5	64-QAM	2/3	-22	-23	-24
MCS 6	64-QAM	3/4	-25	-26	-27
MCS 7	64-QAM	5/6	-27	-28	-29
MCS 8	256-QAM	3/4	-30	-32	-32
MCS 9	256-QAM	5/6	-32	-33	-34
MCS 10	BPSK	1/2	-5	-6	-9
MCS 11	QPSK	1/2	-10	-11	-14
MCS 12	QPSK	3/4	-13	-14	-17
MCS 13	16-QAM	1/2	-16	-17	-20
MCS 14	16-QAM	3/4	-19	-20	-23
MCS 15	64-QAM	2/3	-22	-23	-26
MCS 16	64-QAM	3/4	-25	-26	-29
MCS 17	64-QAM	5/6	-27	-28	-31
MCS 18	256-QAM	3/4	-30	-32	-34
MCS 19	256-QAM	5/6	-32	-33	-36

A.2 Tx power

Table A-5 Tx power

Mode		Targeted Power(dBm) Single User	Targeted Power(dBm) Multi-User
802.11b (2.4 GHz)	1Mbps_L	23	NA
	11Mbps_S	23	NA
802.11g (2.4 GHz)	6 Mbps	23	23
	54 Mbps	20	19
802.11n (2.4 GHz)	MCS0, HT20	23	23
	MCS7, HT20	18	17
	MCS0, HT40	23	23
	MCS7, HT40	18	17
802.11a (5 GHz)	6 Mbps	23	23
	54 Mbps	22	22
802.11n (5 GHz)	MCS0, HT20	23	23
	MCS7, HT20	21	19
	MCS0, HT40	23	23
	MCS7, HT40	21	19
802.11ac (2.4 GHz)	MCS0, VHT20	23	23
	MCS8, VHT20	17	16
	MCS0, VHT40	23	23
	MCS9, VHT40	17	16
802.11ac (5 GHz)	MCS0, VHT20	23	23
	MCS8, VHT20	20	17
	MCS0, VHT40	23	23
	MCS9, VHT40	20	17
	MCS0, VHT80	23	23
	MCS7, VHT80	21	19
	MCS9, VHT80	20	17

A.3 Rx sensitivity

Table A-6 Rx sensitivity

Mode		Condition	AP.DK04 sensitivity limitation(dBm) @ANT ---2X2, chain mask=3	Notes
802.11b (2.4 GHz)	1Mbps_L	PER < 8%	-99.5	1. For mask=3, nss=1 2. Sensitivity tolerance+/-1.5dB
	11Mbps_S	PER < 8%	-91.5	
802.11g (2.4 GHz)	6 Mbps	PER < 10%	-95	
	54 Mbps	PER < 10%	-79	
802.11a (5 GHz)	6 Mbps	PER < 10%	-93.5	
	54 Mbps	PER < 10%	-78.5	
802.11n (2.4 GHz)	MCS0, HT20	PER < 10%	-92	1. For mask=3, nss=2 2. Sensitivity tolerance+/-1.5dB
	MCS7, HT20	PER < 10%	-75	
	MCS0, HT40	PER < 10%	-89.5	
	MCS7, HT40	PER < 10%	-72	
802.11n (5 GHz)	MCS0, HT20	PER < 10%	-92	
	MCS7, HT20	PER < 10%	-74.5	
	MCS0, HT40	PER < 10%	-89	
	MCS7, HT40	PER < 10%	-72	
802.11ac (2.4 GHz)	MCS0, VHT20	PER < 10%	-92	
	MCS8, VHT20	PER < 10%	-70.5	
	MCS0, VHT40	PER < 10%	-89.5	
	MCS9, VHT40	PER < 10%	-66.5	
802.11ac (5 GHz)	MCS0, VHT20	PER < 10%	-92	
	MCS8, VHT20	PER < 10%	-70	
	MCS0, VHT40	PER < 10%	-89	
	MCS9, VHT40	PER < 10%	-66	
	MCS0, VHT80	PER < 10%	-86	
	MCS7, VHT80	PER < 10%	-68.5	
	MCS9, VHT80	PER < 10%	-62.5	