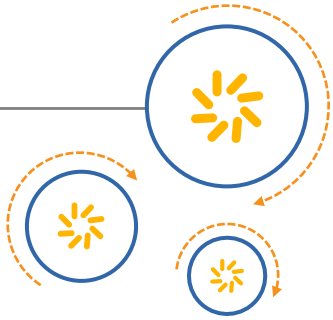
Qualcomm Atheros, Inc.



# IPQ4019/IPQ4029

## Device Revision Guide

80-Y9348-29 Rev. E

February 3, 2016

**For additional information or to submit technical questions go to https://createpoint.qti.qualcomm.com/**





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# Revision history

| Revision | Date | Description |
|---|---|---|
| A | October 2015 | Initial release |
| B | November 2015 | Section 3 “Known issues”: Refine issue descriptions. |
| C | December 2015 | Section 3 “Known issues”: added Issue 5 |
| D | January 2016 | Updated Table 3 Device identification details and Table 4 Known issues – all sample types and revisions |
| E | February 2016 | Section 2.2: Updated date codes. |

# Contents



## Figures



## Tables

# 1 Introduction

An IPQ4019/IPQ4029 chip is a highly integrated system-on-chip (SoC) designed for high-performance, power-efficient, and cost-effective 2×2, 802.11ac, dual-band concurrent access-point applications. The SoC incorporates a quad-core ARM Cortex A7 processor, two dual-band, concurrent 802.11ac Wave-2 Wi-Fi subsystems, and a five-port Gigabit Ethernet Layer 2/3/4 multilayer switch supporting line rate network address translation (NAT). It supports one USB3.0 and one USB2.0. It also supports miscellaneous interfaces such as I²S, SPDIF, I²C, SMI, UART, JTAG, etc., which can be configured as general purpose I/O pins.

Technical information for IPQ4019/IPQ4029 devices is primarily covered by the documents listed in Table 1.

**Table 1 IPQ4019/IPQ4029 documents**

| Doc Number | Title |
|---|---|
| 80-Y9347-19 | *IPQ4019 Access Point SoC Device Specification* |
| 80-Y9347-29 | *IPQ4029 Access Point SoC Device Specification* |

## Scope and intended audience

This device revision guide identifies issues with all IPQ4019/IPQ4029 samples released to date.

This device revision guide is intended for new product developers who are designing, testing, and/or evaluating products that include an IPQ4019/IPQ4029 device.

# 2 Device Identification

The IPQ4019/IPQ4029 devices can be identified by markings on the top surface; these identification techniques are described in Section 2.1. Further details about each sample type are presented in Section 2.2.

## 2.1 Device marking

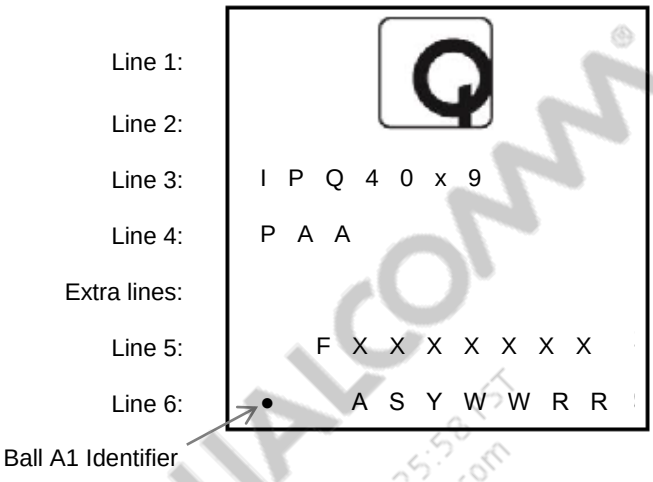


**Figure 1 IPQ40x9 marking (top view, not to scale)**

**Table 2 Marking table for IPQ40x9 devices**

| Line | Marking | Description |
|---|---|---|
| 1 and 2 | Logo | Qualcomm® logo |
| 3 | IPQ4019 or IPQ4029 | Qualcomm product name |
| 4 | PAA | P: product configuration code<br>AA: product feature code |
| 5 | FXXXXXXX | F: supply source code<br>XXXXXXX: wafer lot ID |
| 6 | ASYWWRR | A: assembly site code<br>S: assembly sequence number<br>Y: single, last digit of year<br>WW: work week (based on calendar year)<br>RR: product revision |
| Additional lines may appear on the part marking for some samples; this is manufacturing information that is only relevant to Qualcomm and Qualcomm suppliers. | | |

## 2.2 Device identification details

This section provides details for identifying each sample type.

**Table 3 Device identification details**

| Device | Product configuration code (P) | Product revision (RR) | Date code (YYWW) | Sample type |
|---|---|---|---|---|
| IPQ4019 | 0 | 00 | ≥ 1539 | ES |
| | 0 | 00 | ≥ 1603[1] | CS |
| IPQ4029 | 0 | 00 | ≥ 1539 | ES |
| | 0 | 00 | ≥ 1603[1] | CS |
| | 1 | 00 | ≥ 1603 | ES |

1. Lot 000NKPWTT.K0510, 000NKPWTT.K1510 with date code 1547 are CS materials.

## 2.3 Sample testing

The “Sample type” codes in Table 3 are defined below.

### 2.3.1 Engineering samples (ES)

These devices have undergone limited testing and sometimes have significant feature limitations. They are suitable to assist with PCB development, to conduct board-level electrical evaluation tests, and to explore manufacturing considerations. Engineering samples are not to be used for product-level qualification.

### 2.3.2 Commercial samples (CS)

These devices have undergone full production-level testing and meet the specifications and features described in the device specification, except as otherwise noted in this document. They have passed device-level qualification. Commercial samples are suitable to be used for performance testing, and also product-level production and qualification.

# 3 Known Issues

## 3.1 Summary of known issues

All known issues for each revision of IPQ4019/IPQ4029 devices are summarized in Table 4. The text within the "*Issue #*" column provides links to the sections of this document that explain the issues, regardless of the sample type (or types) on which they occur.

**NOTE:** An X in any of the other columns indicates that the issue occurs on the corresponding sample type. Absence of an X indicates the issue does not apply to the corresponding sample type.

**Table 4 Known issues – all sample types and revisions**

| # | Issues | Severity Level | Variants Affected | | | | Resolution |
|---|---|---|---|---|---|---|---|
| | | | IPQ4019 | | IPQ4029 | | |
| | | | ES | CS | ES | CS | |
| Issue 1 | SGMII not functional | M | X | X | X | X | No fix is currently planned |
| Issue 2 | SU/MU NDP heavy clip | L | X | X | X | X | No fix is currently planned |
| Issue 3 | USB 3.0 interoperability issue | L | X | X | X | X | No fix is currently planned |
| Issue 4 | LAN to LAN 1 Gbps traffic will not run at full line rate | L | X | X | X | X | No fix is currently planned |
| Issue 5 | HW breakpoints with self-hosted debuggers (GDB) are non-functional | L | X | X | X | X | No fix is currently planned |

## 3.2 Issues – description, impact, and workaround

### Issue 1

| | |
|---|---|
| **Description** | **SGMII not functional** |
| **System Impact** | The SGMII interface cannot be enabled |
| **Limitation** | IPQ4019/IPQ4029 cannot support single port Ethernet PHY |
| **Workaround** | Use QCA8072 2-port Ethernet PHY |

### Issue 2

| | |
|---|---|
| **Description** | **SU/MU NDP heavy clip** |
| **System Impact** | Under certain orientations at higher rates, a ~3-4 dB degradation has been observed |
| **Limitation** | Loss of performance at higher MCS rates in a bad channel |
| **Workaround** | No workaround available |

### Issue 3

| | |
|---|---|
| **Description** | **USB 3.0 interoperability issue** |
| **System Impact** | Cannot detect certain USB devices. Driver may time out after issuing an endpoint-specific command, and might require resetting of the host controller |
| **Limitation** | Observed with the following devices:<br>▪ PQI NANO USB3.0 Pen Drive<br>▪ Mach Xtreme Technology MXUB3MFX-16G Pen Drive<br>▪ Xtreme Technology MXUB3MFX-16G Pen Drive<br>▪ Sanwa UFD-3SW32GBK<br>▪ Transcend USB3.0 SSD |
| **Workaround** | A workaround has been found for the following devices and is available in a future release<br>▪ Transcend USB3.0 SSD<br>No workaround is available for the following devices:<br>▪ PQI NANO USB3.0 Pen Drive<br>▪ Mach Xtreme Technology MXUB3MFX-16G Pen Drive<br>▪ Xtreme Technology MXUB3MFX-16G Pen Drive<br>▪ Sanwa UFD-3SW32GBK |

### Issue 4

| | |
|---|---|
| **Description** | **LAN to LAN 1 Gbps traffic will not run at full line rate** |
| **System Impact** | Cannot run at line rate. Very minor degradation in throughput. |
| **Limitation** | In some cases, Wi-Fi calibration could cause the Ethernet clock to be slower than partner Ethernet device. |
| **Workaround** | No workaround available. |

### Issue 5

| | |
|---|---|
| **Description** | **HW breakpoints with self-hosted debuggers (GDB) are non-functional** |
| **System Impact** | None |
| **Limitation** | HW breakpoints will not work in the case of self-hosted debuggers |
| **Workaround** | JTAG interface should be used for debugging with HW breakpoints |