QCA9882 Dual-Band 2x2 MIMO 802.11ac/abgn WLAN SoC

Data Sheet

80-Y0962-1 Rev. E

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Confidential and Proprietary - Qualcomm Atheros, Inc.

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Revision history

Revision	Date	Description
A	December 2012	Initial version
B	March 2013	Updated radio characteristics
C	April 2013	Updated package dimensions
D	May 2013	Edits to Table 2-1, Signal-to-Pin Relationships and Descriptions. Updated Figure 5-2, Output voltages regulated by the chip.
E	October 2013	Updated INT_PIN register: Hardcoded to 1 (INTA only)

Contents

1 Introduction

1.1 General Description

The Qualcomm Atheros QCA9882 s a highly integrated wireless local area network (WLAN) system-on-chip (SoC) for 5 GHz 802.11ac, or 2.4/5 GHz 802.11n WLAN applications. The QCA9882 integrates an on-board CPU for low-level setup of WLAN physical layer (PHY) and RF to offload the host processor for other tasks. It enables high-performance 2x2 MIMO with two spatial streams for wireless applications demanding the highest robust link quality and maximum throughput and range. The QCA9882 integrates a multi-protocol MAC, PHY, analog-to-digital/digital-to-analog converters (ADC/DAC), 2x2 MIMO radio transceivers, and PCI Express interface in an all-CMOS device for low power consumption and small form-factor applications.

The QCA9882 implements half-duplex OFDM, CCK, and DSSS PHY, supporting 867 Mbps for 802.11ac 80 MHz channel operation. It supports 802.11n up to 150 Mbps for 20 MHz and 300 Mbps for 40 MHz channel operations, and IEEE 802.11a/b/g data rates. Additional features include Maximal Likelihood (ML) decoding, Low-Density Parity Check (LDPC), Maximal Ratio Combining (MRC), Space Time Block Code (STBC), and On-Chip One-Time Programmable (OTP) memory to eliminate the need for an external flash and to further reduce the external component count and BOM cost. The QCA9882 supports 802.11 wireless MAC protocol, 802.11i security, Rx/Tx filtering, error recovery, and 802.11e quality of service (QoS).

The QCA9882 supports up to two simultaneous traffic streams integrating two Tx and two Rx chains for high throughput and extended coverage. Tx chains combine PHY in-phase (I) and quadrature (Q) signals, convert them to the desired frequency, and drive the RF signal to multiple antennas. Rx chains use an integrated architecture. The frequency synthesizer supports 1-MHz steps to match frequencies defined by IEEE 802.11a/b/g/n specifications.The QCA9882 supports frame data transfer to and from the host using a PCIE interface providing interrupt generation and reporting, power save, and status reporting. Other external interfaces include EEPROM and GPIOs.

1.2 Features

- WLAN CPU supports low-level setup of PHY and RF to offload the host processor for other tasks
- Dynamic frequency selection (DFS) in required 5-GHz bands when used as an AP
- 2x2 MIMO technology improves effective throughput and range over existing 802.11a/b/g products
- Supports spatial multiplexing, cyclic-delay diversity (CDD), low-density parity check (LDPC), maximal ratio combining (MRC), Space Time Block Code (STBC)
- Smart antenna diversity
- Single-ended RF ports with integrated matching simplify board design and layout
- Integrated 1.2 V switching regulator
- Data rates of up to 867 Mbps in 802.11ac 80 MHz channels
- Data rates of up to 150 Mbps for 20 MHz channels and 300 Mbps for 40 MHz channels using reduced (short) guard interval in 802.11n mode
- Supports 20/40 MHz at 2.4 GHz
- Supports 20/40/80 MHz at 5 GHz
- On-Chip One-Time Programmable (OTP) memory
- Support for IEEE 802.11d, e, h, i, k, r, v time stamp, and w standards
- WEP, TKIP, AES, and WAPI hardware encryption
- PCI Express 1.1 interface
- 20 and 40 MHz channelization
- Frame aggregation, block ACK
- 802.11e-compatible bursting
- 108-pin, 12 mm x 12 mm LPCC package

1.3 Block Diagram

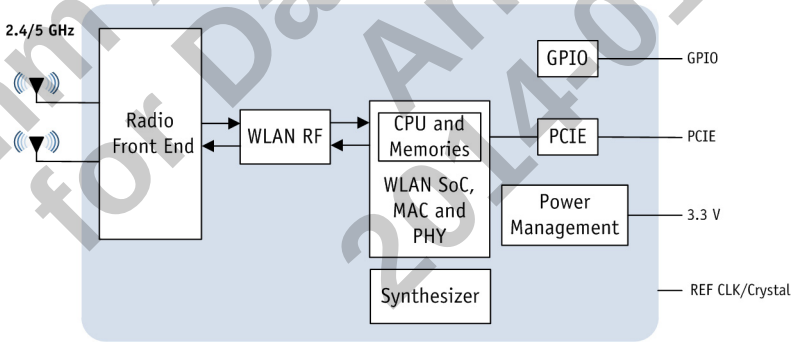

Figure 1-1 QCA9882 Block Diagram

2 Pin Descriptions

This section contains a package pinout (see Figure 2-1 and Table 2-1) and a tabular listing of the signal descriptions.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

I	Digital input signal
I/O	A digital bidirectional signal
IA	Analog input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
O	A digital output signal
OA	An analog output signal
OD	A digital output signal with open drain
P	A power or ground signal

Figure 2-1 shows the LPCC-108 package pinout.

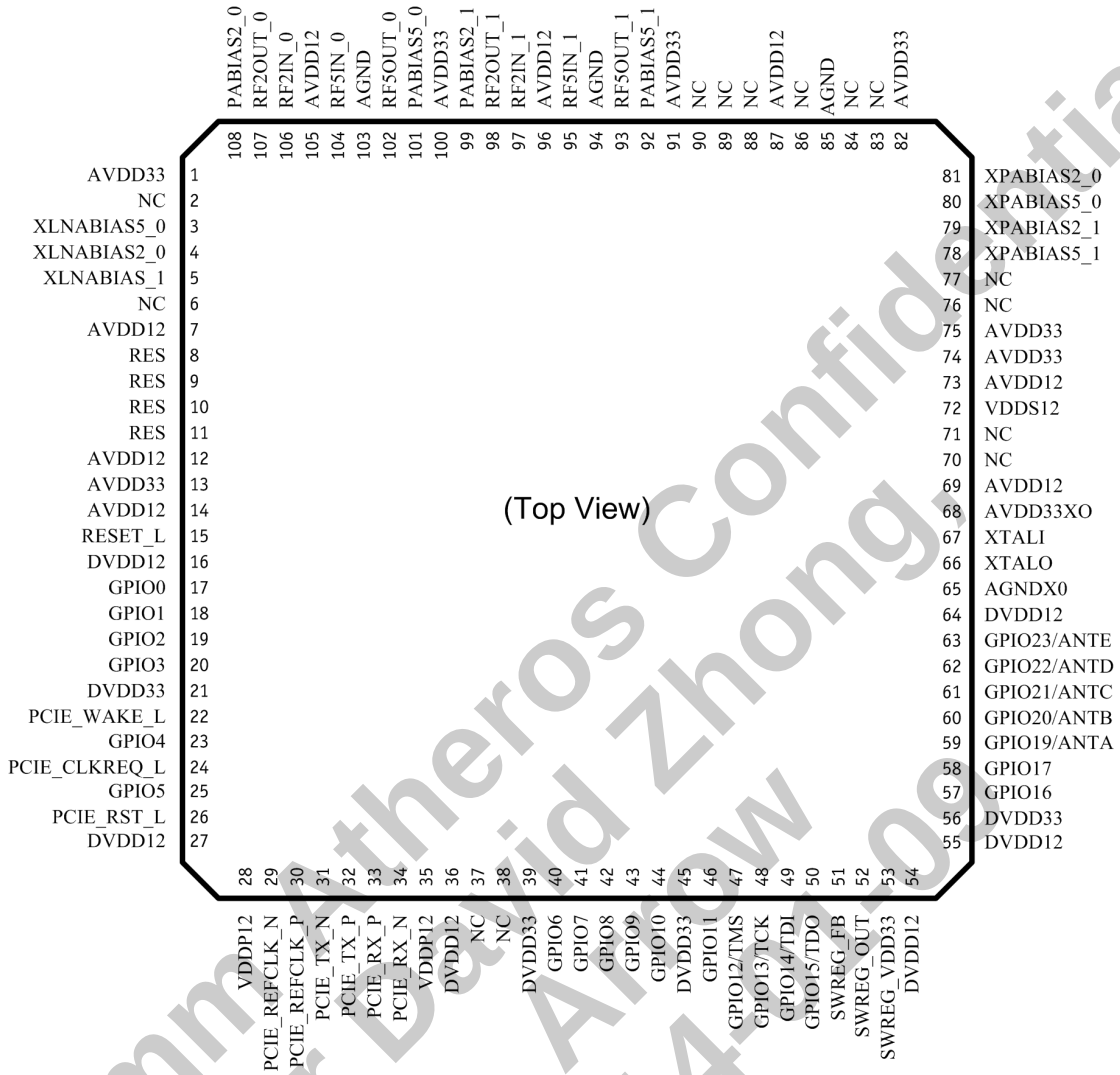

Figure 2-1 LPCC-108 Package Pinout

Table 2-1 Signal-to-Pin Relationships and Descriptions

Symbol	Pin	Type	Description
PCI Express			
PCIE_CLKREQ_L	24	OD	Reference clock request, open drain
PCIE_REFCLK_N	29	IA	Differential reference clock (100 MHz)
PCIE_REFCLK_P	30	IA	
PCIE_RST_L	26	IL	PCI Express reset with weak pull-down
PCIE_RX_N	34	IA	Differential receive
PCIE_RX_P	33	IA	
PCIE_TX_N	31	OA	Differential transmit
PCIE_TX_P	32	OA	
PCIE_WAKE_L	22	OD	Request to service a function-initiated wake event, open drain
Radio			
RF2IN_0	106	IA	Single-ended input at 2.4 GHz for chain 0
RF2IN_1	97	IA	Single-ended input at 2.4 GHz for chain 1
RF2OUT_0	107	OA	Single-ended 2.4 GHz power amplifier output for chain 0
RF2OUT_1	98	OA	Single-ended 2.4 GHz power amplifier output for chain 1
RF5IN_0	104	IA	Single-ended input at 5 GHz for chain 0
RF5IN_1	95	IA	Single-ended input at 5 GHz for chain 1
RF5OUT_0	102	OA	Single-ended 5 GHz power amplifier output for chain 0
RF5OUT_1	93	OA	Single-ended 5 GHz power amplifier output for chain 1
Analog Interface			
PABIAS2_0	108	IA	External bias for 2.4 GHz for chain 0
PABIAS2_1	99	IA	External bias for 2.4 GHz for chain 1
PABIAS5_0	101	IA	External bias for 5 GHz for chain 0
PABIAS5_1	92	IA	External bias for 5 GHz for chain 1
XLNABIAS_0	3	OA	External LNA Bias for chain 0
XLNABIAS_1	5	OA	External LNA Bias for chain 1
XPABIAS2_0	81	OA	External PA bias for 2.4 GHz for chain 0
XPABIAS2_1	79	OA	External PA bias for 2.4 GHz for chain 1
XPABIAS5_0	80	OA	External PA bias for 5 GHz for chain 0
XPABIAS5_1	78	OA	External PA bias for 5 GHz for chain 1

Table 2-1 Signal-to-Pin Relationships and Descriptions (cont.)

Symbol	Pin	Type	Description
General			
RESET_L	15	IH	Reset with weak pull-up for the QCA9882
XTALI	67	I	40 MHz crystal
XTALO	66	I/O	
GPIO			
GPIO0	17	I/O	General purpose input/output pins The GPIOs are used for a variety of purposes such as I^2C, SPI, JTAG, etc. GPIO12, GPIO13, GPIO14, and GPIO15 pins are multiplexed pins that default to the JTAG interface. GPIO19 through GPIO23 are multiplexed pins that default to external RF switch control.
GPIO1	18	I/O	
GPIO2	19	I/O	
GPIO3	20	I/O	
GPIO4	23	I/O	
GPIO5	25	I/O	
GPIO6	40	I/O	
GPIO7	41	I/O	
GPIO8	42	I/O	
GPIO9	43	I/O	
GPIO10	44	I/O	
GPIO11	46	I/O	
GPIO12/TMS	47	I/O	
GPIO13/TCK	48	I/O	
GPIO14/TDI	49	I/O	
GPIO15/TDO	50	I/O	
GPIO16	57	I/O	
GPIO17	58	I/O	
GPIO19/ANTA	59	I/O	
GPIO20/ANTB	60	I/O	
GPIO21/ANTC	61	I/O	
GPIO22/ANTD	62	I/O	
GPIO23/ANTE	63	I/O	
Internal Voltage Regulator			
SWREG_FB	51	I	1.2 V feedback to the internal switching regulator[1]
SWREG_OUT	52	P	1.2 V output from the internal switching regulator[1]
SWREG_VDD33	53	P	3.3 V input to the internal switching regulator

1. An LC circuit is required off-chip between the SWREG_OUT and SWREG_FB. See Figure 5-2.

Symbol	Pin	Description
Power		
AVDD12	7, 12, 14, 69, 73, 87, 96, 105	Analog 1.2 V power supply[1]
AVDD33	1, 13, 74, 75, 82, 91, 100	Analog 3.3 V power supply
AVDD33XO	68	Analog 3.3 V power supply
DVDD12	16, 27, 36, 54, 55, 64	Digital 1.2 V power supply[1]
DVDD33	21, 39, 45, 56	Digital 3.3 V power supply
VDDP12	28, 35	PCIE 1.2 V power supply[1]
VDDS12	72	1.2 V power supply [1]
Ground		
AGND	85, 94, 103	Analog ground
AGNDXO	65	Analog ground
Ground Pad		
Exposed Ground Pad		Tied to GND (see Package Dimensions)
No Connect		
NC	2, 4, 6, 37, 38, 70, 71, 76, 77, 83, 84, 86, 88, 89, 90	No connect
Reserved		
RES	8, 9, 10, 11	Reserved; tied to GND

1. All 1.2 V supplies need to be connected to the SWREG_FB pin. See Figure 5-2.

3 Functional Specification

3.1 Functional block diagram

Figure 3-1 illustrates the QCA9882 functional block diagram.

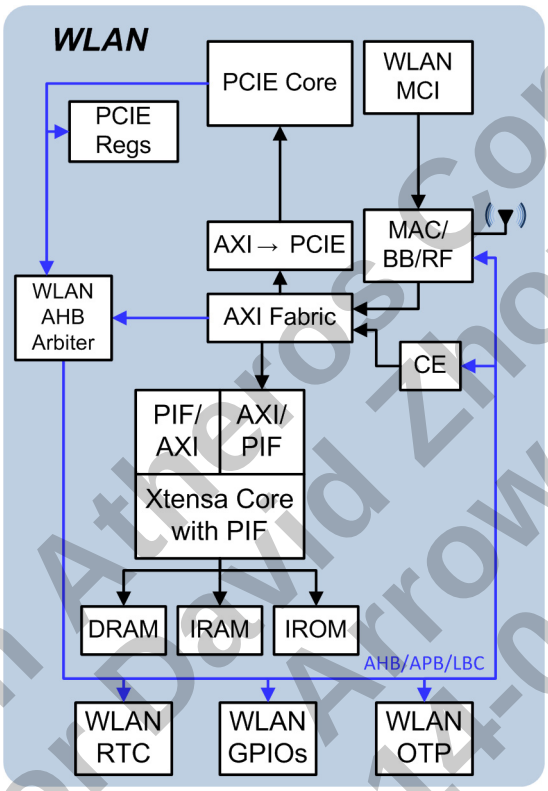

Figure 3-1 QCA9882 functional block diagram

The QCA9882 is comprised of several internal functional blocks, as summarized in Table 3-1.

Table 3-1 Functional blocks

Block	Description
AXI	The AXI bus is accessed simultaneously by multiple masters in the PCIE host memory, CPU memory, and all programmable registers. The WLAN portion of the AXI fabric supports split transactions to achieve higher utilization on the PCIE bus. All register access from the CPU route through the AXI fabric. A bridge converts AXI requests to AHB requests, and the AHB arbiter selects between PCIE register access requests and CPU register access requests on a round-robin basis. All register accesses for all modules including the MAC, CE, and blocks such as GPIOs, RTC, or OTP use the APB protocol. A bridge converts AHB requests into APB. It must be noted here that the entire AXI fabric, AHB, and APB interfaces all run synchronously on the SoC clock domain. See AXI.
CE	The copy engine (CE) establishes a communication channel between the firmware and the host. It performs a DMA copy from one memory location (source memory) to another memory location (destination memory), and it can perform this DMA copy operation in a batch, under control of software. A copy involves a read operation from the source memory, followed by a write operation to the destination memory.
WLAN Clocking	The MAC/baseband clock domain runs off of the WLAN PLL. The PLL runs at either at 160 MHz or 176 MHz. The CPU/SoC clock domain runs off of the CPU PLL. The AXI fabric together with the AHB and APB buses typically run at either half or quarter CPU clock. The PCIE clock domain runs at 125 MHz.
CPU Core and Memory Controller	The CPU is a Tensilica XTENSA 7.0 processor with a hardware abstraction layer (HAL) to support low level WLAN activity with minimal support from the PCIE host. The CPU is configured with a peripheral interface (PIF). The outbound PIF is used by the CPU for register access. The inbound PIF is used by the other AXI masters (MAC and CE) to access the data memory (DMEM) connected to the CPU.
MAC/Baseband/RF	The integrated 2.4/5 GHz 802.11ac MAC/baseband/radio includes the features of maximal likelihood (ML) decoding, low-density parity check (LDPC), and maximal ratio combining (MRC). The MAC includes a offload engine (OLE) block responsible for A-MSDU scatter and gather, L2 header encapsulation and decapsulation, IP/TCP/UDP checksum, and Rx classification.
PCIE Core	All programmable registers can be accessed by either the PCIE host or by the internal CPU. The PCIE core provides a simple proprietary low-bandwidth controller (LBC) interface for register accesses.
PCIE Configuration Space Registers	The QCA9882 PCIE configuration space maps to the host memory space. All programmable registers can be accessed either by the PCIE host or by the internal CPU. The PCIE core provides a simple proprietary low-bandwidth controller (LBC) interface for register accesses. A bridge converts this LBC interface into standard AHB. An AHB-AHB bridge synchronizes the clock domain from the PCIE clock domain to the SoC clock domain. Some additional registers are accessible only by the PCIE host. These registers run on the PCIE clock domain and are not routed through the main AHB arbiter. They allow the PCIE host to determine the sleep status of the SoC and to wake up the SoC if needed. See PCIE configuration space register descriptions.
WLAN AHB Arbiter	Selects between the PCIE register access requests and CPU register access requests on a round-robin basis.
WLAN GPIOs	All digital pins map to 16 GPIOs. These GPIOs are used for a variety of purposes such as BT coexistence, UART, I^2C, SPI, JTAG. Another set of digital outputs are the four antenna switches used as scan outputs during ATPG testing. The 16 GPIOs are divided into GPIOs dedicated to BT and to WLAN, 8 to BT and 8 to WLAN. See GPI/GPIO.
WLAN OTP	WLAN one-time programmable (OTP) memory
WLAN RTC	The RTC block controls the clocks and power going to other modules within the chip. Its inputs consist of sleep requests from these modules and its outputs consists of clock enable signals used to gate the clocks going to these modules. The RTC block also manages resets going to other modules within the device.

3.2 AXI

Figure 3-1 diagrams the AXI fabric.

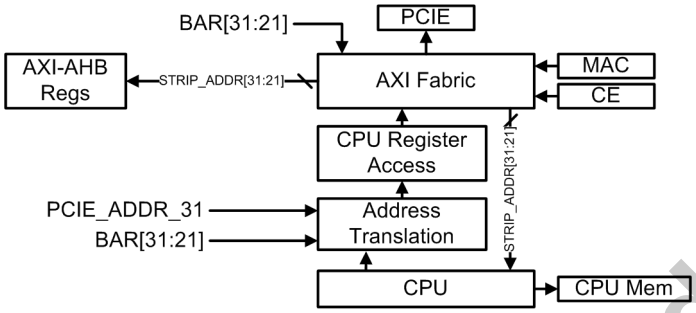

Figure 3-2 AXI fabric diagram

Because PCIE host memory, CPU memory, and all programmable registers can all be accessed simultaneously by multiple masters in the AXI bus, it is important to ensure that no address-related conflicts arise. Upon booting, the PCIE host provides a unique base address (BAR) to all devices. BAR location always aligns to the space requested by each device; in the QCA9882, it is 2 MBytes of space, thus the BAR aligns to 2 MBytes and only bits [31:21] are non-zero. AXI fabric uses these bits as input to steer incoming AXI requests to the appropriate slave. Note that BAR input to the AXI fabric is not directly connected to the BAR value programmed by the PCIE host, but comes from a programmable register. AXI fabric looks for BAR bits [31:21] for all incoming transfers. See Table 3-3.

Table 3-3 Address decoding logic

Address Bits [31:21]	Address Bits [20:0]	AXI Slave Decode
BAR not matching	—	PCIE
BAR matching	< 0x100000	AXI-AHB (register access)
	≥ 0x100000	For the CPU, address bits [31:20] are replaced with the programmable register CPU_ADDR_MSB_V, which is set by default to 4 to indicate a 4-Mbyte address range matching with the CPU's DMEM address space.

The Xtensa CPU memory address location must be in fixed address ranges: instruction memory (IMEM) must be 8-12 MBytes (0x800000-0xBFFFFF) and data memory (DMEM) 4-8 MBytes (0x400000-0x7FFFFF). Because these fixed address ranges could conflict with PCIE host memory allocation, the an address translation mechanism is used for all CPU access. See Figure 3-4.

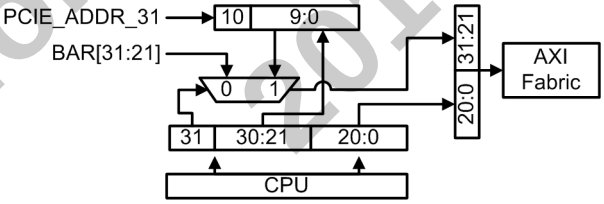

Figure 3-4 CPU address translation mechanism

All outbound transfers from the CPU pass through the address translation logic, which looks at the MSB of the address (bit [31]). If this bit is low, the transfer is deemed to be a register access and bits [31:21] of the address are appended with the BAR value. The AXI fabric steers the transfer to the AXI-AHB bridge as indicated in Table 3-3. If bit [31] is high, the transfer is deemed as intended to access PCIE memory, thus all but the MSB (bits [30:0]) must contain the intended address in PCIE host memory. The programmable register PCIE_ADDR_31 contains the MSB of the PCIE host memory location appended to the original address.

3.3 GPI/GPIO

The QCA9882 provides 16 configurable bi-directional general purpose I/O ports and 3 configurable input-only ports. Each GPI/GPIO port can be configured independently as input or output using the GPIO control registers. The GPIOs are used for a variety of purposes such as UART, I^2C, SPI, JTAG, and so on. Another set of digital outputs are the five antenna switches used as scan outputs during ATPG testing.

Most GPIOs have a normal mode functionality as well as a test-mode functionality. The mapping of the GPIOs is shown in Table 3-1. On reset all GPIOs are inputs and the bootstrap values are sampled. The global test mode is on GPIO4. If this pin is sampled high during initialization, then the chip enters test mode.

Table 3-1 Multiplexed pins

Pin	GPIO Pin	Description			
17	GPIO0	WLAN_DISABLE			
18	GPIO1	WLAN_LED			
19	GPIO2[1]	MCI_CLK_IN	SPI_MISO	I2C_SDA	BT_ACTIVE
20	GPIO3[1]	MCI_CLK_OUT	SPI_CS_L	—	BT_PRIORITY
23	GPIO4[1]	MCI_DATA_OUT	SPI_CLK	I2C_CLK	WL_ACTIVE
25	GPIO5[1]	MCI_DATA_IN	SPI_MOSI	—	BT_FREQ
40	GPIO6	UART1_RXD			
41	GPIO7	UART1_TXD			
42	GPIO8	UART2_TXD			
43	GPIO9	UART2_RTS			
44	GPIO10	UART2_RXD			
46	GPIO11	UART2_CTS			
47	GPIO12	TMS			
48	GPIO13	TCK			
49	GPIO14	TDI			
50	GPIO15	TDO			
57	GPIO16	Reserved			
58	GPIO17	Reserved			
59	GPIO19	ANTA			
60	GPIO20	ANTB			
61	GPIO21	ANTC			
62	GPIO22	ANTD			
63	GPIO23	ANTE			

1. GPIO2 through GPIO5 can be used for one of: I^2C, SPI, legacy Bluetooth coexistence, or MCI Bluetooth coexistence.

4 Register Descriptions

This section describes the CPU address space registers and PCIE configuration space registers for the QCA9882.

Table 4-1 summarizes the QCA9882 CPU address space registers.

Table 4-1 CPU address space registers summary

CPU Address Range	Description	Page
0x0000_4000 to 0x0000_43FF	Real-Time Clock Registers	page 20
0x0000_8000 to 0x0000_8FFF	SoC PCIE Registers	page 45
0x0000_9000 to 0x0000_9FFF	SoC Core Registers	page 46
0x0000_C000 to 0x0000_C01F	WLAN UART Registers	page 50
0x0001_0000 to 0x0001_003F	WLAN Serial Interface Registers	page 54
0x0001_4000 to 0x0001_40FF	WLAN GPIO Registers	page 59
0x57400 to 0x57450 0x57800 to 0x57850 0x57C00 to 0x57C50 0x58000 to 0x58050 0x58400 to 0x58450 0x58800 to 0x58850 0x58C00 to 0x58C50 0x59000 to 0x59050	Copy Engine [0 to 7] Registers	page 87
0x57000 to 0x57004	Copy Engine Wrapper Registers	page 94

The host accesses the QCA9882 PCIE configuration space registers at boot time to detect the type of card present and to perform low-level configuration, such as assigning the base address to the card. At reset, an on-chip one-time programmable memory (OTP) is used to initialize some registers, while the host or the QCA9882 hardware must program the others.

Table 4-2 PCIE configuration address space summary

Offset from Base Address Configured by the Host	Description	Page
0x0 to 0x82	PCIE Configuration Space Registers	page 95

4.1 Real-time clock registers

Table 4-3 summarizes the QCA9882 real-time clock registers and other configuration registers for the SoC block.

Table 4-3 Real-Time Clock Register Summary

Address	Name	Description	Page
0x00004000	SOC_RESET_CONTROL	Reset Control	page 22
0x00004020	SOC_CPU_CLOCK	Clock Control for CPU	page 23
0x00004028	SOC_CLOCK_CONTROL	Clock Control for Functional Blocks	page 23
0x00004030	SOC_WDT_CONTROL	Watchdog Timer Control	page 24
0x00004034	SOC_WDT_STATUS	Watchdog Timer Status	page 24
0x00004038	SOC_WDT	Watchdog Timer	page 24
0x0000403C	SOC_WDT_COUNT	Watchdog Timer Count	page 25
0x00004040	SOC_WDT_RESET	Watchdog Timer Reset	page 25
0x00004044	SOC_INT_STATUS	Interrupt Status for Local CPU Interrupts	page 26
0x00004048	SOC_LF_TIMER0	Low-Frequency Timer	page 27
0x0000404C	SOC_LF_TIMER_COUNT0	Low-Frequency Timer Current Value	page 27
0x00004050	SOC_LF_TIMER_CONTROL0	Clock Restart Policy and Reset for Low-Frequency Timer	page 27
0x00004054	SOC_LF_TIMER_STATUS0	Low Frequency Timer Raw Interrupt Status	page 28
0x00004058	SOC_LF_TIMER1	Low-Frequency Timer	page 28
0x0000405C	SOC_LF_TIMER_COUNT1	Low-Frequency Timer Current Value	page 28
0x00004060	SOC_LF_TIMER_CONTROL1	Clock Restart Policy and Reset for Low-Frequency Timer	page 29
0x00004064	SOC_LF_TIMER_STATUS1	Low Frequency Timer Raw Interrupt Status	page 29
0x00004068	SOC_LF_TIMER2	Low-Frequency Timer	page 30
0x0000406C	SOC_LF_TIMER_COUNT2	Low-Frequency Timer Current Value	page 30
0x00004070	SOC_LF_TIMER_CONTROL2	Clock Restart Policy and Reset for Low-Frequency Timer	page 30
0x00004074	SOC_LF_TIMER_STATUS2	Low Frequency Timer Raw Interrupt Status	page 31
0x00004078	SOC_LF_TIMER3	Low-Frequency Timer	page 31
0x0000407C	SOC_LF_TIMER_COUNT3	Low-Frequency Timer Current Value	page 31
0x00004080	SOC_LF_TIMER_CONTROL3	Clock Restart Policy and Reset for Low-Frequency Timer	page 32
0x00004084	SOC_LF_TIMER_STATUS3	Low Frequency Timer Raw Interrupt Status	page 32
0x00004088	SOC_HF_TIMER	High-Frequency Timer	page 33
0x0000408C	SOC_HF_TIMER_COUNT	High-Frequency Timer Current Value	page 33
0x00004090	SOC_HF_LF_COUNT	Low-Frequency Timer Value Synchronous with High-Frequency Timer Read	page 33

Table 4-3 Real-Time Clock Register Summary

Address	Name	Description	Page
0x00004094	SOC_HF_TIMER_CONTROL	High-Frequency Timer Enable, Clock Restart Policy, and Reset	page 34
0x00004098	SOC_HF_TIMER_STATUS	High Frequency Timer Raw Interrupt Status	page 34
0x0000409C	SOC_RTC_CONTROL	Controls Loading of SOC_RTC_CONFIG into the RTC Logic	page 35
0x000040A0	SOC_RTC_TIME	Real-Time Clock Current Time Values	page 35
0x000040A4	SOC_RTC_DATE	Real-Time Clock Date Value	page 36
0x000040A8	SOC_RTC_SET_TIME	Set Real-Time Clock Time	page 36
0x000040AC	SOC_RTC_SET_DATE	Real-Time Clock Date	page 37
0x000040B0	SOC_RTC_SET_ALARM	Real-Time Clock Alarm Set/Reset	page 37
0x000040B4	SOC_RTC_CONFIG	Real-Time Clock Configuration	page 38
0x000040B8	SOC_RTC_ALARM_STATUS	Real-Time Clock Alarm Interrupt Status	page 39
0x000040BC	SOC_UART_WAKEUP	UART Wakeup Event Control	page 39
0x000040C0	SOC_RESET_CAUSE	Reset Cause	page 40
0x000040C4	SOC_SYSTEM_SLEEP	System Sleep Control	page 40
0x000040C8	SOC_INT_STATUS1	Interrupt Status for Local CPU Interrupts	page 41
0x000040CC	SOC_INT_SLEEP_MASK	Sleep State Interrupt Mask for Interrupts to CPU	page 41
0x00004110	SOC_CORE_CLK_CTRL	Frequency of the Core Clock of the SoC Block	page 41
0x00004114	SOC_GPIO_WAKEUP_CONTROL	Controls whether GPIOs can Wake Up the System	page 42
0x000042B8	PMU	PMU Wakeup Time Select	page 42
0x000042BC	PMU_CONFIG	PMU Configuration Values	page 42
0x000042C0	PMU_PAREG	PMU PA Regulator Configuration Values	page 42
0x000042C4	PMU_BYPASS	PMU Regulator Bypass	page 43
0x000042F8	RTC_SLEEP_COUNT	Real-Time Clock Sleep Threshold	page 43
0x00004310	SRIF_CLOCK	SRIF Clock Selection between PCIE and CORE Clocks	page 43
0x00004314	SRIF_CLOCK_GATING	SRIF Clock Gating Controls for PCIE and CORE Clocks	page 44
0x00004318	RTC_SPARE0	Spare Programmable Flops 0	page 44
0x0000431C	RTC_SPARE1	Spare Programmable Flops 1	page 44

4.1.1 Reset control (SOC_RESET_CONTROL)

Address: 0x00004000
Access: See the field description
Reset Value: 0x00000800

Software can hold any target block in reset by writing a 1 to the corresponding bit in this register. Reset is held asserted to the target block as long as the corresponding bit is set. Multiple blocks can be held in reset simultaneously.

Bits	Name	Access	Reset	Description
31:19	RES	RO	0x0000	Reserved
18	CE_RST	R/W	0x0	Holds the copy engine (CE) in reset
17	UART2_RST	R/W	0x0	Holds second UART in reset
16:12	RES	RO	0x00	Reserved
11	CPU_INIT_RESET	R/W	0x1	An external mode signal called CPU_INIT_RST is latched on a GPIO upon system power up. If this signal is set, the CPU is held in reset until the host comes and clears this bit.
10	RES	RO	0x0	Reserved
9	RST_OUT	R/W	0x0	Asserts the RST_OUT_L pin. This pin is multiplexed with GPIO. Note that RST_OUT_L is also asserted during SYS_RST_L and COLD_RESET. **Value** / **Function** 0 – Drive the RST_OUT_L pin to 1 1 – Drive the RST_OUT_L pin to 0
8	COLD_RST	R/W	0x0	Resets all blocks with a cold reset. This bit is automatically cleared after the chip reset process is complete.
7	RES	RO	0x0	Reserved
6	CPU_WARM_RST	R/W	0x0	Resets the CPU block only with a warm reset. Support blocks, including the memory controller and interrupt controller blocks, are not reset. This bit is automatically cleared after the CPU reset process is complete.
5:3	RES	RO	0x0	Reserved
2	PCIE_RST_SHORT_OVRD	R/W	0x0	Separates the PCIE and PWR resets
1	UART_RST	R/W	0x0	Holds UART in reset
0	SI0_RST	R/W	0x0	Holds the serial interface (SPI and I^2C) logic block in reset

4.1.2 CPU clock (SOC_CPU_CLOCK)

Address: 0x00004020
Access: See the field description
Reset Value: 0x00000003

When the value of this register is changed, the CPU clock is gated for two high-speed clock cycles while the clock dividers are updated.

Bits	Name	Access	Reset	Description	
31:2	RES	RO	0x00000000	Reserved	
1:0	STANDARD	R/W	0x3	Controls the CPU speed during standard operation. The CPU clock speed is updated on the clock following the write to this register.	
				0	80/88 MHz (BB PLL)
				1	160/176 MHz (BB PLL)
				2	CPU PLL 3: REFCLK

4.1.3 Clock control (SOC_CLOCK_CONTROL)

Address: 0x00004028
Access: See the field description
Reset Value: 0x00000041

Software can gate off the clock to individual functional block to save power. Note that when a functional block has it clock gated, it cannot wake up, cause interrupts, or operate in any fashion until its clock gate has been released. Also, this register is used to select between the internally generated 32 KHz clock and the external signal coming through a GPIO pin.

Bits	Name	Access	Reset	Description
31:7	RES	RO	0x0000000	Reserved
6	RTC_CLK_AMBA	R/W	0x1	Set to 1 to gate off the RTC_CLK (32 KHz) going to USB block
5:3	RES	RO	0x0	Reserved
2	LF_CLK32	R/W	0x0	When this bit set to 1, the external 32 KHz input is selected. When this bit is cleared, the internally generated 32 KHz clock is selected.
1	RES	RO	0x0	Reserved
0	SI0_CLK	R/W	0x1	Set to 1 to gate off clock to the serial interface (SPI and I^2C) logic block

4.1.4 Watchdog timer control (SOC_WDT_CONTROL)

Address: 0x00004030
Access: See the field description
Reset Value: 0x00000002

Controls the watchdog timer actions.

Bits	Name	Access	Reset	Description	
31:3	RES	RO	0x00000000	Reserved	
2:0	ACTION	R/W	0x2	Control watchdog timer action on an expiration event	
				0xx	Watchdog actions disabled
				100	Watchdog reset action enabled, warm reset on expiration
				101	Watchdog actions disabled
				110	Watchdog interrupt action enabled on expiration
				111	Reserved

4.1.5 Watchdog timer status (SOC_WDT_STATUS)

Address: 0x00004034
Access: See the field description
Reset Value: 0x00000000

This signal asserts when WDT action is set to interrupt and a WDT expire event occurs.

Bits	Name	Access	Reset	Description
31:1	RES	RO	0x00000000	Reserved
0	INTERRUPT	R/W	0x0	When WDT expires, this bit is set by hardware. Software can also set this bit with a write. When this bit is set by either hardware or software, the corresponding interrupt bit in Interrupt status (SOC_INT_STATUS) is set.

4.1.6 Watchdog timer (SOC_WDT)

Address: 0x00004038
Access: See the field description
Reset Value: 0x003FFFFF

When the Watchdog timer count (SOC_WDT_COUNT) register equals the WDT, WDT logic takes the action specified by the Watchdog timer control (SOC_WDT_CONTROL) register. WDT operates at 32 KHz.

Bits	Name	Access	Reset	Description
31:22	RES	RO	0x000	Reserved
21:0	TARGET	R/W	0x3FFFFF	Watchdog timer target compare value, based on the core clock frequency. Software should reset the watchdog timer after changing this value.

4.1.7 Watchdog timer count (SOC_WDT_COUNT)

Address: 0x0000403C
Access: See the field description
Reset Value: 0x00000000

The current value of the watchdog timer (Watchdog timer (SOC_WDT)). This value is reset to 0 when the watchdog timer is reset. If the WDT_COUNT equals WDT, a watchdog expiration event occurs. The WDT_COUNT timer operates at the core clock frequency. When the core clock is gated off, the watchdog timer freezes.

Bits	Name	Access	Reset	Description
31:22	RES	RO	0x000	Reserved
21:0	VALUE	RO	0x000000	Watchdog timer current count value, in units of 32.768 KHz clocks.

4.1.8 Watchdog timer reset (SOC_WDT_RESET)

Address: 0x00004040
Access: See the field description
Reset Value: 0x00000000

This register resets the watchdog timer.

Bits	Name	Access	Reset	Description
31:1	RES	RO	0x00000000	Reserved
0	VALUE	R/W	0x0	This field is written by software periodically to reset the watchdog timer and prevent expiration under normal operation. When software writes a 1 to this field, the Watchdog timer count (SOC_WDT_COUNT) register is reset to 0. The watchdog timer expiration does not occur until WDT_COUNT equals WDT. When this field is read by software, a 0 is always returned.

4.1.9 Interrupt status (SOC_INT_STATUS)

Address: 0x00004044
Access: See the field description
Reset Value: 0x00000000

This register shows the interrupt status for local CPU interrupts.

Bits	Name	Access	Reset	Description
31:16	RES	RO	0x0000	Reserved
15	THERM	RO	0x0	Interrupt from the thermometer ADC control logic
14	EFUSE_OVERWRITE	RO	0x0	EFUSE overwrite interrupt
13	BTCOEX	RO	0x0	Interrupt from the external PTA/EPTA coexistence logic
12	RTC_POWER	RO	0x0	Power on from network sleep interrupt
11	MAC	RO	0x0	Wireless MAC interrupt 0
10	RTC_ALARM	RO	0x0	RTC alarm interrupt
9	HF_TIMER	RO	0x0	High frequency timer interrupt
8	LF_TIMER3	RO	0x0	Low frequency timer 3 interrupt
7	LF_TIMER2	RO	0x0	Low frequency timer 2 interrupt
6	LF_TIMER1	RO	0x0	Low frequency timer 1 interrupt
5	LF_TIMER0	RO	0x0	Low frequency timer 0 interrupt
4	RES	RO	0x0	Reserved
3	SI	RO	0x0	Serial interface, I^2S, or SPI (master) interrupt
2	GPIO	RO	0x0	GPIO interrupt
1	ERROR	RO	0x0	Address ERROR or AHB master hang interrupt
0	WDT_INT	RO	0x0	Watchdog timeout interrupt

4.1.10 LF timer 0 (SOC_LF_TIMER0)

Address: 0x00004048
Access: See the field description
Reset Value: 0x00000000

When the LF timer count 0 (SOC_LF_TIMER_COUNT0) register equals this register, a timer interrupt is generated if enabled. Software can write to this register at any time, and hardware performs the value synchronization across clock boundaries automatically after a write. When the chip is in the SLEEP state, it wakes up before the low frequency timer 0 (LF_TIMER0) reaches its target. Hardware automatically causes a wakeup XTAL_SETTLE cycles before the LF_TIMER 0 expires. If XTAL_SETTLE is larger than the time remaining before LF_TIMER 0 expires, the chip does not enter SLEEP. If the System sleep control (SOC_SYSTEM_SLEEP) register is set, early wakeup is not required, so wakeup occurs when LF_TIMER_COUNT equals LF_TIMER_TARGET.

Bits	Name	Access	Reset	Description
31:0	TARGET	R/W	0x00000000	LF timer target compare value, in units of 30.5 µs (1/32768 seconds)

4.1.11 LF timer count 0 (SOC_LF_TIMER_COUNT0)

Address: 0x0000404C
Access: See the field description
Reset Value: 0x00000000

This register shows the current value of LF timer 0 (SOC_LF_TIMER0). This value is continuously synchronized from the timer clock domain to the core clock domain.

Bits	Name	Access	Reset	Description
31:0	VALUE	RO	0x00000000	LF Timer current count value, in units of 30.5 µs (1/32768 seconds).

4.1.12 LF timer control 0 (SOC_LF_TIMER_CONTROL0)

Address: 0x00004050
Access: See the field description
Reset Value: 0x00000000

This register controls the clock restart policy and reset for LF timer 0 (SOC_LF_TIMER0).

Bits	Name	Access	Reset	Description	
31:3	RES	RO	0x00000000	Reserved	
2	ENABLE	R/W	0x0	This bit enables the interrupt to propagate up to the Interrupt status (SOC_INT_STATUS) register and to the CPU. If this bit is set to 0, this interrupt does not cause SOC_INT_STATUS or IP4 to be set.	
1	AUTO_RESTART	R/W	0x0	Timer automatic restart control	
				0	LF_TIMER0 continues counting after SOC_LF_TIMER_COUNT0 reaches LF_TIMER0.
				1	LF_TIMER0 resets to 0 and continue counting after SOC_LF_TIMER_COUNT0 reaches SOC_LF_TIMER0. Because the timer resets to 0, the period of the timer is LF_TIMER0 + 1 clocks.
0	RESET	R/W	0x0	Software writes a 1 to this field to reset the timer to 0. When software writes a 1, the timer begins counting from 0. Software can see this transition from 1 to 0 when the reset occurs.	

4.1.13 LF timer status 0 (SOC_LF_TIMER_STATUS0)

Address: 0x00004054
Access: See the field description
Reset Value: 0x00000000

This register holds LF timer 0 (SOC_LF_TIMER0) interrupt status before any interrupt enable masks are applied.

Bits	Name	Access	Reset	Description
31:1	RES	RO	0x00000000	Reserved
0	INTERRUPT	R/W	0x0	Low frequency timer 0 raw interrupt bit. When (SOC_LF_TIMER0 == SOC_LF_TIMER_COUNT0) or when (unsigned int)(SOC_LF_TIMER0 - SOC_LF_TIMER_COUNT0) > 2^31, this bit is set by hardware. This set is edge triggered, meaning hardware does not set the interrupt bit again until software writes to the SOC_LF_TIMER0 register. Software can also set this bit with a write. When this bit is set by either hardware or software, the LF timer source interrupt signal is asserted to the interrupt controller. Software clears the interrupt by writing 0 to this field.

4.1.14 LF timer 1 (SOC_LF_TIMER1)

Address: 0x00004058
Access: See the field description
Reset Value: 0x00000000

When the LF timer count 1 (SOC_LF_TIMER_COUNT1) register equals this register, a timer interrupt is generated if enabled. Software can write to this register at any time, and hardware performs the value synchronization across clock boundaries automatically after a write. When the chip is in SLEEP state, it wakes up before LF_TIMER 1 reaches its target. Hardware automatically causes a wakeup XTAL_SETTLE cycles before LF_TIMER 1 expires. If XTAL_SETTLE is larger than the time remaining before LF_TIMER 1 expires, the chip does not enter SLEEP. If the System sleep control (SOC_SYSTEM_SLEEP) register is set, early wakeup is not required, so the wakeup occurs when LF_TIMER_COUNT equals LF_TIMER_TARGET.

Bits	Name	Access	Reset	Description
31:0	TARGET	R/W	0x00000000	LF_TIMER1 target compare value, in units of 30.5 µs (1/32768 seconds)

4.1.15 LF timer count 1 (SOC_LF_TIMER_COUNT1)

Address: 0X0000405C
Access: See the field description
Reset Value: 0x00000000

This register shows the current value of LF_TIMER1. This value is continuously synchronized from the timer clock domain to the core clock domain.

Bits	Name	Access	Reset	Description
31:0	VALUE	RO	0x00000000	LF_TIMER1 current count value in units of 30.5 µs (1/32768 seconds).

4.1.16 LF timer control 1 (SOC_LF_TIMER_CONTROL1)

Address: 0x00004060
Access: See the field description
Reset Value: 0x00000000

This register controls the clock restart policy and reset for LF_TIMER1.

Bits	Name	Access	Reset	Description	
31:3	RES	RO	0x00000000	Reserved	
2	ENABLE	R/W	0x0	This bit enables the interrupt to propagate up to the Interrupt status (SOC_INT_STATUS) register and to the CPU. If this bit is set to 0, this interrupt does not cause SOC_INT_STATUS or IP4 to be set.	
1	AUTO_RESTART	R/W	0x0	Timer automatic restart control.	
				0	LF_TIMER1 continues counting after LF_TIMER_ COUNT1 reaches LF_TIMER1.
				1	LF_TIMER1 resets to 0 and continue counting after SOC_ LF_TIMER_COUNT1 reaches LF_TIMER1. Because the timer resets to 0, the period of the timer is LF_TIMER1 + 1 clocks.
0	RESET	R/W	0x0	Software writes a 1 to this field to reset the timer to 0. When software writes a 1, the timer begins counting from 0. Software can see this transition from 1 to 0 when the reset occurs.	

4.1.17 LF timer status 1 (SOC_LF_TIMER_STATUS1)

Address: 0x00004064
Access: See the field description
Reset Value: 0x00000000

This register holds the LF_TIMER1 interrupt status before any interrupt enable masks are applied.

Bits	Name	Access	Reset	Description
31:1	RES	RO	0x00000000	Reserved
0	INTERRUPT	R/W	0x0	LF_TIMER1 raw interrupt bit When (SOC_LF_TIMER1 == SOC_LF_TIMER_COUNT1) or when (unsigned int)(SOC_LF_TIMER1 - SOC_LF_TIMER_COUNT1) > 2^31, this bit is set by hardware. This set is edge triggered, meaning hardware does not set the interrupt bit again until software writes to the LF timer 1 (SOC_LF_TIMER1) register. Software can also set this bit with a write. When this bit is set by either hardware or software, the LF_TIMER1 source interrupt signal is asserted to the interrupt controller. Software clears the interrupt by writing 0 to this field.

4.1.18 LF timer 2 (SOC_LF_TIMER2)

Address: 0x00004068
Access: See the field description
Reset Value: 0x00000000

If the LF timer count 2 (SOC_LF_TIMER_COUNT2) register equals this register, a timer interrupt is generated if enabled. Software can write to this register at any time, and hardware performs the value synchronization across clock boundaries automatically after a write. When the chip is in SLEEP state, it wakes up before LF_TIMER2 reaches its target. Hardware automatically causes a wakeup XTAL_SETTLE before LF_TIMER2 expires. If XTAL_SETTLE is larger than the time remaining before LF_TIMER expires, the chip does not enter SLEEP. If the System sleep control (SOC_SYSTEM_SLEEP) register is set, early wakeup is not required, so wakeup occurs when LF_TIMER_COUNT equals LF_TIMER_TARGET.

Bits	Name	Access	Reset	Description
31:0	TARGET	R/W	0x00000000	LF_TIMER2 target compare value in units of 30.5 µs (1/32768 seconds).

4.1.19 LF timer count 2 (SOC_LF_TIMER_COUNT2)

Address: 0x0000406C
Access: See the field description
Reset Value: 0x00000000

This register shows the current value of LF_TIMER2. This value is continuously synchronized from the timer clock domain to the core clock domain.

Bits	Name	Access	Reset	Description
31:0	VALUE	RO	0x00000000	LF_TIMER2 current count value, in units of 30.5 µs (1/32768 seconds).

4.1.20 LF timer control 2 (SOC_LF_TIMER_CONTROL2)

Address: 0x00004070
Access: See the field description
Reset Value: 0x00000000

This register controls the clock restart policy and reset for LF_TIMER2.

Bits	Name	Access	Reset	Description	
31:3	RES	RO	0x00000000	Reserved	
2	ENABLE	R/W	0x0	This bit enables the interrupt to propagate up to the Interrupt status (SOC_INT_STATUS) register and to the CPU. If this bit is set to 0, this interrupt does not cause SOC_INT_STATUS or IP4 to be set.	
1	AUTO_RESTART	R/W	0x0	Timer automatic restart control	
				0	The LF timer continues counting after LF_TIMER_COUNT2 reaches LF_TIMER2.
				1	The LF timer resets to 0 and continue counting after LF_TIMER_COUNT2 reaches LF_TIMER2. Because the timer resets to 0, the period of the timer is LF_TIMER2 + 1 clocks.
0	RESET	R/W	0x0	Software writes a 1 to this field to reset the timer to 0. When software writes a 1, the timer begins counting from 0. Software can see this transition from 1 to 0 when the reset occurs.	

4.1.21 LF timer status 2 (SOC_LF_TIMER_STATUS2)

Address: 0x00004074
Access: See the field description
Reset Value: 0x00000000

This register holds the LF_TIMER2 interrupt status before any interrupt enable masks are applied.

Bits	Name	Access	Reset	Description
31:1	Reserved	RO	0x00000000	Reserved
0	INTERRUPT	R/W	0x0	LF_TIMER2 raw interrupt bit When (SOC_LF_TIMER2 == SOC_LF_TIMER_COUNT2) or when (unsigned int)(SOC_LF_TIMER2 - SOC_LF_TIMER_COUNT2) > 2^31, this bit is set by hardware. This set is edge triggered, meaning hardware does not set the interrupt bit again until software writes to the LF timer 2 (SOC_LF_TIMER2) register. Software can also set this bit with a write. When this bit is set by either hardware or software, the LF timer source interrupt signal is asserted to the interrupt controller. Software clears the interrupt by writing 0 to this field.

4.1.22 LF timer 3 (SOC_LF_TIMER3)

Address: 0x00004078
Access: See the field description
Reset Value: 0x00000000

When the LF timer 3 (SOC_LF_TIMER3) register equals this register, a timer interrupt is generated if enabled. Software can write to this register at any time, hardware performs the value synchronization across clock boundaries automatically after a write. When the chip is in the SLEEP state, it wakes up before the LF_TIMER3 reaches its target. Hardware automatically causes a wakeup XTAL_SETTLE cycles before the LF_TIMER3 expires. If XTAL_SETTLE is larger than the time remaining before LF_TIMER expires, the chip does not enter SLEEP. If the System sleep control (SOC_SYSTEM_SLEEP) register is set, early wakeup is not required, so wakeup occurs when LF_TIMER_COUNT equals LF_TIMER_TARGET.

Bits	Name	Access	Reset	Description
31:0	TARGET	R/W	0x00000000	LF_TIMER3 target compare value, in units of 30.5 µs (1/32768 seconds)

4.1.23 LF timer count 3 (SOC_LF_TIMER_COUNT3)

Address: 0X0000407C
Access: See the field description
Reset Value: 0x00000000

This register shows the current value of LF_TIMER3. This value is continuously synchronized from the timer clock domain to the core clock domain.

Bits	Name	Access	Reset	Description
31:0	VALUE	RO	0x00000000	LF_TIMER3 current count value, in units of 30.5 µs (1/32768 seconds)

4.1.24 LF timer control 3 (SOC_LF_TIMER_CONTROL3)

Address: 0x00004080
Access: See the field description
Reset Value: 0x00000000

This register controls the clock restart policy and reset for LF_TIMER3.

Bits	Name	Access	Reset	Description
31:3	RES	RO	0x00000000	Reserved
2	ENABLE	R/W	0x0	This bit enables the interrupt to propagate up to the Interrupt status (SOC_INT_STATUS) register and to the CPU. If the ENABLE bit is set to 0, this interrupt does not cause SOC_INT_STATUS or IP4 to be set.
1	AUTO_RESTART	R/W	0x0	Timer automatic restart control.
				0 — The LF timer continues counting after LF_TIMER_COUNT3 reaches LF_TIMER3.
				1 — The LF timer resets to 0 and continues counting after LF_TIMER_COUNT3 reaches LF_TIMER3. Because the timer resets to 0, the period of the timer is LF_TIMER3 + 1 clocks.
0	RESET	R/W	0x0	Software writes a 1 to this field to reset the timer to 0. When software writes a 1, the timer begins counting from 0. Software can see this transition from 1 to 0 when the reset occurs.

4.1.25 LF timer status 3 (SOC_LF_TIMER_STATUS3)

Address: 0x00004084
Access: See the field description
Reset Value: 0x00000000

This register holds the LF_TIMER3 interrupt status before any interrupt enable masks are applied.

Bits	Name	Access	Reset	Description
31:1	RES	RO	0x00000000	Reserved
0	INTERRUPT	R/W	0x0	LF_TIMER3 raw interrupt bit. When (SOC_LF_TIMER3 == SOC_LF_TIMER_COUNT3) or (unsigned int)(SOC_LF_TIMER3 - SOC_LF_TIMER_COUNT3) > 2^31, this bit is set by hardware. This set is edge triggered, meaning hardware does not set the interrupt bit again until software writes to SOC_LF_TIMER3. Software can also set this bit with a write. When this bit is set by either hardware or software, the LF_TIMER3 source interrupt signal is asserted to the interrupt controller. Software clears the interrupt by writing 0 to this field.

4.1.26 High-frequency timer (SOC_HF_TIMER)

Address: 0x00004088
Access: See the field description
Reset Value: 0x00000000

When the High-frequency timer count (SOC_HF_TIMER_COUNT) register equals this register, a timer interrupt is generated if enabled. Software can write to this register at any time. HF_TIMER does not run when the chip is in sleep mode and the HF clock is gated off.

Bits	Name	Access	Reset	Description
31:12	TARGET	R/W	0x00000	HF timer target compare value, in units of 40 MHz clocks. Note that this value is left-justified so software can use the sign bit for wrap detection.
11:0	RES	RO	0x000	Reserved

4.1.27 High-frequency timer count (SOC_HF_TIMER_COUNT)

Address: 0x0000408C
Access: See the field description
Reset Value: 0x00000000

The current value of the HF timer.

Bits	Name	Access	Reset	Description
31:12	VALUE	RO	0x00000	HF timer current count value, in units of 40 MHz clocks
11:0	RES	RO	0x000	Reserved

4.1.28 High-frequency LF timer count (SOC_HF_LF_COUNT)

Address: 0x00004090
Access: See the field description
Reset Value: 0x00000000

When software reads the High-frequency timer count (SOC_HF_TIMER_COUNT) register, hardware automatically copies the value of LF timer count 0 (SOC_LF_TIMER_COUNT0) to this register. This allows software to capture both high and low frequency counter at the same instant in time.

Bits	Name	Access	Reset	Description
31:0	VALUE	RO	0x00000000	LF timer value, captured on last read to SOC_HF_TIMER_COUNT, in units of 30.5 µs (1/32768 seconds).

4.1.29 High-frequency timer control (SOC_HF_TIMER_CONTROL)

Address: 0x00004094
Access: See the field description
Reset Value: 0x00000008

Controls the timer enable, clock restart policy, and reset for High-frequency timer (SOC_HF_TIMER).

Bits	Name	Access	Reset	Description	
31:4	RES	RO	0x0000000	Reserved	
3	ENABLE	R/W	0x1	This bit enables the interrupt to propagate up to the Interrupt status (SOC_INT_STATUS) register and to the CPU. If this bit is set to 0, this interrupt does not cause IP4 to be set.	
2	ON	R/W	0x0	Enables the timer operation. When not in use, the timer should be disabled to save power.	
				0	The HF timer is disabled
				1	The HF timer is enabled
1	AUTO_RESTART	R/W	0x0	Timer automatic restart control.	
				0	The HF timer continues counting after SOC_HF_TIMER_COUNT reaches HF_TIMER.
				1	The HF timer resets to 0 and continues counting after SOC_HF_TIMER_COUNT reaches SOC_HF_TIMER. Because the timer resets to 0, the timer period is HF_TIMER + 1 clocks.
0	RESET	R/W	0x0	When software writes a 1, the timer begins counting from 0.	

4.1.30 High-frequency timer status (SOC_HF_TIMER_STATUS)

Address: 0x00004098
Access: See the field description
Reset Value: 0x00000000

This register holds the HF_TIMER interrupt status before any interrupt enable masks are applied.

Bits	Name	Access	Reset	Description
31:1	RES	RO	0x00000000	Reserved
0	INTERRUPT	R/W	0x0	When SOC_HF_TIMER equals SOC_HF_TIMER_COUNT, this bit is set by hardware. Software can also set this bit with a write. When this bit is set by either hardware or software, the HF timer source interrupt signal is asserted to the interrupt controller. Software clears the interrupt by writing 0 to this field.

4.1.31 Real-time clock control (SOC_RTC_CONTROL)

Address: 0X0000409C
Access: See the field description
Reset Value: 0x00000000

Controls loading of Real-time clock configure (SOC_RTC_CONFIG) into the RTC logic. This register is only reset by RTC_RESET.

Bits	Name	Access	Reset	Description
31:3	RES	RO	0x00000000	Reserved
2	ENABLE	R/W	0x0	Enables real time clock and alarm feature. When this is disabled, clocks are gated to the alarm and clock functions. 0 Clock and alarm disabled 1 Clock and alarm enabled
1	LOAD_RTC	R/W	0x0	When software writes a 1 to this field, RTC logic is loaded with the Set real-time clock time (SOC_RTC_SET_TIME), Set real-time clock date (SOC_RTC_SET_DATE), and Real-time clock configure (SOC_RTC_CONFIG) registers. For accurate clock setting, the sub-second count is set to 0 when the write occurs. When this field is read by software, a 1 is returned while the load is in progress, a 0 is returned when the load is complete.
0	LOAD_ALARM	R/W	0x0	When software writes a 1 to this field, RTC alarm logic is loaded with the SOC_RTC_SET_ALARM register. When this field is read by software, a 1 is returned while the load is in progress, a 0 is returned when the load is complete.

4.1.32 Real-time clock time (SOC_RTC_TIME)

Address: 0x000040A0
Access: See the field description
Reset Value: 0x01120000

Returns current time values. This register is continuously synchronized by hardware to the core clock domain. This register is only reset by RTC_RESET.

Bits	Name	Access	Reset	Description
31:27	RES	RO	0x00	Reserved
26:24	WEEK_DAY	RO	0x1	Current weekday, changes at midnight; the number rolls over after 7 (1=Sun, 2=Mon, ...)
23:22	RES	RO	0x0	Reserved
21:16	HOUR	RO	0x12	Current hour 0-23 in 24-hour mode or AM/PM, 0-12 in 12-hour mode; resets to midnight, BCD
15	RES	RO	0x0	Reserved
14:8	MINUTE	RO	0x00	Current minute count, rolls over after 59
7	RES	RO	0x0	Reserved
6:0	SECOND	RO	0x00	Current second count, rolls over after 59

4.1.33 Real-time clock date (SOC_RTC_DATE)

Address: 0x000040A4
Access: See the field description
Reset Value: 0x00000101

Returns current time values. This register is continuously synchronized by hardware to the core clock domain. This register is only reset by RTC_RESET.

Bits	Name	Access	Reset	Description
31:24	RES	RO	0x00	Reserved
23:16	YEAR	RO	0x00	Current year, 0 is 2000.
15:13	RES	RO	0x0	Reserved
12:8	MONTH	RO	0x01	Current month count, rolls over after 12, (1=Jan, 2=Feb, ...)
7:6	RES	RO	0x0	Reserved
5:0	MONTH_DAY	RO	0x01	Current day of the month, rolls over at 28 (Feb), 29 (Feb leap year), 30, or 31; first day of the month is 1

4.1.34 Set real-time clock time (SOC_RTC_SET_TIME)

Address: 0x000040A8
Access: See the field description
Reset Value: 0x01000000

To set the RTC time of day, software writes the target time to the Set real-time clock time (SOC_RTC_SET_TIME) and Set real-time clock date (SOC_RTC_SET_DATE) registers, then writes a 1 to the LOAD_RTC bit of the Real-time clock control (SOC_RTC_CONTROL) register. The LOAD_RTC bit also sets the sub-second counter to 0. This register is only reset by RTC_RESET.

Bits	Name	Access	Reset	Description
31:27	RES	RO	0x00	Reserved
26:24	WEEK_DAY	R/W	0x1	Set weekday, 1-7 (1=Sun, 2=Mon, ...)
23:22	RES	RO	0x0	Reserved
21:16	HOUR	R/W	0x00	Set hour 0-23 in 24-hour mode or AM/PM, 0-12 in 12-hour mode; this setting must be consistent with the programming of BCD
15	RES	RO	0x0	Reserved
14:8	MINUTE	R/W	0x00	Set minutes, 0-59
7	RES	RO	0x0	Reserved
6:0	SECOND	R/W	0x00	Set seconds, 0-59

4.1.35 Set real-time clock date (SOC_RTC_SET_DATE)

Address: 0x000040AC
Access: See the field description
Reset Value: 0x00000101

To set the RTC date and year, software writes the target time to the Set real-time clock time (SOC_RTC_SET_TIME) and Set real-time clock date (SOC_RTC_SET_DATE) registers, then writes a 1 to the LOAD_RTC bit of the Real-time clock control (SOC_RTC_CONTROL) register. This register is only reset by RTC_RESET.

Bits	Name	Access	Reset	Description
31:24	RES	RO	0x00	Reserved
23:16	YEAR	R/W	0x00	Set year, 0 is 2000
15:13	RES	RO	0x0	Reserved
12:8	MONTH	R/W	0x01	Set month (1=Jan, 2=Feb, ...)
7:6	RES	RO	0x0	Reserved
5:0	MONTH_DAY	R/W	0x01	Set day of the month, 1-31

4.1.36 Set real-time clock alarm (SOC_RTC_SET_ALARM)

Address: 0x000040B0
Access: See the field description
Reset Value: 0x00000000

Returns current alarm time values on read, updates alarm time on write. The alarm time is only loaded into the RTC logic after software writes a 1 to the LOAD_ALARM bit in the Real-time clock control (SOC_RTC_CONTROL) register. If the time is set to an illegal value, the alarm never triggers (for example, it SECOND is set to 61). This register is only reset by RTC_RESET.

Bits	Name	Access	Reset	Description
31:22	RES	RO	0x000	Reserved
21:16	HOUR	R/W	0x00	Alarm hour 0-23 in 24-hour mode or AM/PM, 0-12 in 12-hour mode; this setting must be consistent with the programming of BCD
15	RES	RO	0x0	Reserved
14:8	MINUTE	R/W	0x00	Alarm minute, 0-59
7	RES	RO	0x0	Reserved
6:0	SECOND	R/W	0x00	Alarm second, 0-59

4.1.37 Real-time clock configure (SOC_RTC_CONFIG)

Address: 0x000040B4
Access: See the field description
Reset Value: 0x00000007

Read or write the configuration options for the RTC. When software changes the value of any of the fields in this register, it should also update the Set real-time clock time (SOC_RTC_SET_TIME) and Set real-time clock date (SOC_RTC_SET_DATE) registers and write a 1 to the LOAD_RTC bit in the Real-time clock control (SOC_RTC_CONTROL) register, as this pushes the configuration to the RTC logic. This register is only reset by RTC_RESET.

Bits	Name	Access	Reset	Description	
31:3	RES	RO	0x00000000	Reserved	
2	BCD	R/W	0x1	0	The RTC operates in binary mode. All accesses to Set real-time clock time (SOC_RTC_SET_TIME), Set real-time clock date (SOC_RTC_SET_DATE), and Real-time clock configure (SOC_RTC_CONFIG) are formatted in ordinary binary.
				1	The RTC operates in binary coded decimal. In BCD mode, all writes to the SOC_RTC_SET_TIME, SOC_RTC_SET_DATE, and SOC_RTC_SET_ALARM_TIME should be formatted in BCD. All reads from the SOC_RTC_TIME and SOC_RTC_DATE registers return BCD values when this bit is set.
1	TWELVE_HOUR	R/W	0x1	The RTC must be in BCD mode for 12-hour mode to engage. In 12-hour mode, all writes to SOC_RTC_SET_TIME and SET_RTC_TIME should use the 12-hour format. All reads to SOC_RTC_TIME are returned in 12-hour format when this bit is set.	
				0	RTC operates in 24-hour mode, with this bit decode:
				hour[7:6]	Always 0
				hour[5:4]	Tens hour
				hour[3:0]	Ones hour
				1	When this field and the BCD bit are both set, RTC operates in 12-hour mode, and the 8-bit hour fields have the meaning:
				hour[7:6]	Always 0
				hour[5]	AM/PM (AM=0)
				hour[4]	Tens hour
				hour[3:0]	Ones hour
0	DSE	R/W	0x1	0	No special updates occur
				1	Daylight savings updates are enabled: ■ First Sunday of April, time changes from 01:59:59 to 03:00:00 ■ Last Sunday of October, time changes from 01:59:59 to 01:00:00

4.1.38 Real-time clock alarm status (SOC_RTC_ALARM_STATUS)

Address: 0x000040B8
Access: See the field description
Reset Value: 0x00000000

Read or write the RTC alarm enable and interrupt bit. This register is only reset by RTC_RESET.

Bits	Name	Access	Reset	Description	
31:2	RES	RO	0x00000000	Reserved	
1	ENABLE	R/W	0x0	Enables the RTC_ALARM interrupt. If the alarm is disabled, it never wakes the phone from OFF or SLEEP state. This signal is synchronized to the RTC clock before it is sampled, so there is a ~45 µs delay between changing this signal and its taking effect.	
				0	RTC alarm is disabled
				1	RTC alarm is enabled
0	INTERRUPT	R/W	0x0	If the RTC hour, minute, and second values match the values set in the Set real-time clock alarm (SOC_RTC_SET_ALARM) register, this bit is set by hardware. Software can also set this bit with a write. When this bit is set by either hardware or software, the RTC_ALARM source interrupt signal is asserted to the interrupt controller.	

4.1.39 UART wakeup events (SOC_UART_WAKEUP)

Address: 0X000040BC
Access: See the field description
Reset Value: 0x00000000

This register is used to enable UART wakeup events (activity on the Rx line) to bring the system out of sleep.

Bits	Name	Access	Reset	Description	
31:1	RES	RO	0x00000000	Reserved	
0	ENABLE	R/W	0x0	0	UART Rx transitions do not cause a wakeup event
				1	UART Rx transitions cause a wakeup event

4.1.40 Reset cause (SOC_RESET_CAUSE)

Address: 0x000040C0
Access: See the field description
Reset Value: 0x00000000

This register holds the cause of the last reset event. This allows software to detect watchdog reset events and other initial conditions.

Bits	Name	Access	Reset	Description	
31:3	RES	RO	0x00000000	Reserved	
2:0	LAST	RO	0x0	The value of this register holds the last cause of RESET	
				0	The SYS_RST_L pin was asserted.
				1	Illegal
				2	Software wrote either the Reset control (SOC_RESET_CONTROL) COLD_RST bit the WLAN_RESET_CONTROL_COLD_RST
				3	Software wrote the WLAN_RESET_CONTROL_COLD_RST bit
				4	Software set the CPU_WARM_RST bit in Reset control (SOC_RESET_CONTROL)
				5	The watchdog timer expired
				7:6	Reserved

4.1.41 System sleep control (SOC_SYSTEM_SLEEP)

Address: 0x000040C4
Access: See the field description
Reset Value: 0x00000005

System sleep state is entered when all high frequency clocks are gated and the high frequency crystal is shut down. This register is used to indicate the status of each sleep control interface and to disable sleep in the WLAN subsystem.

Bits	Name	Access	Reset	Description	
31:3	RES	RO	0x00000000	Reserved	
2	MAC_IF	RO	0x1	0	The MAC block does not allow sleep state
					The MAC block has enabled the sleep state
1	LIGHT	R/W	0x0	This field gates clocks off in SLEEP, but keeps the crystal running for faster wakeup. If the crystal is turned off, less power is use during sleep but the wakeup time is slower.	
				0	System sleep is deep, with minimal power consumption
				1	System sleep is light
0	DISABLE	R/W	0x1	This field prevents the chip from entering sleep	
				0	System sleep is enabled
				1	System sleep is disabled

4.1.42 Interrupt status (SOC_INT_STATUS1)

Address: 0x000040C8
Access: See the field description
Reset Value: 0x00000000

This register shows the interrupt status for local CPU interrupts.

Bits	Name	Access	Reset	Description
31:4	RES	RO	0x0000000	Reserved
3	MAC_4	RO	0x0	Wireless MAC interrupt 4
2	MAC_3	RO	0x0	Wireless MAC interrupt 3
1	MAC_2	RO	0x0	Wireless MAC interrupt 2
0	MAC_1	RO	0x0	Wireless MAC interrupt 1

4.1.43 Interrupt sleep mask (SOC_INT_SLEEP_MASK)

Address: 0x000040CC
Access: See the field description
Reset Value: 0x00000000

Sleep State Interrupt Mask for interrupts going to the CPU.

Bits	Name	Access	Reset	Description
31:0	BITMAP	R/W	0x00000000	Selects interrupts which get masked off to the CPU just prior to entering sleep. By default, all the interrupts are masked off.

4.1.44 Core clock control (SOC_CORE_CLK_CTRL)

Address: 0x00004110
Access: See the field description
Reset Value: 0x00000000

This register determines the clock frequency (CORE_CLK) of the SoC block.

Bits	Name	Access	Reset	Description	
31:3	RES	RO	0x00000000	Reserved	
2:0	DIV	R/W	0x0	The decoding of this register is:	
				0x0	CPU PLL freq
				0x1	CPU PLL freq divide by 2
				0x2	CPU PLL freq divide by 4
				0x3	CPU PLL freq divide by 4
				0x4 through 0x7	Reserved

4.1.45 GPIO wakeup control (SOC_GPIO_WAKEUP_CONTROL)

Address: 0x00004114
Access: See the field description
Reset Value: 0x00000000

This register controls whether the GPIOs can wake up the system.

Bits	Name	Access	Reset	Description
31:1	RES	RO	0x00000000	Reserved
0	ENABLE	R/W	0x0	Enables GPIOs to wake up the system

4.1.46 PMU wakeup time select (PMU)

Address: 0x000042B8
Access: See the field description
Reset Value: 0x00000000

This register switches regulator wakeup time select as well as the PA regulator wakeup time select.

Bits	Name	Access	Reset	Description	
31:2	RES	RO	0x00000000	Reserved	
1:0	REG_WAKEUP_TIME_SEL	R/W	0x0	The switching regulator and the PA regulator wakeup time selection:	
				0x0	PA_REG = 64 µs, SW_REG = 96 µs
				0x1	PA_REG = 96 µs, SW_REG = 128 µs
				0x2	PA_REG = 128 µs, SW_REG = 160 µs
				0x3	PA_REG = 32 µs, SW_REG = 64 µs

4.1.47 PMU configuration (PMU_CONFIG)

Address: 0x000042BC
Access: See the field description
Reset Value: 0x00000000

Bits	Name	Access	Reset	Description
31:5	RES	RO	0x0000000	Reserved
4:0	VALUE	R/W	0x00	PMU configurations

4.1.48 PMU PA regulator configuration (PMU_PAREG)

Address: 0x000042C0
Access: See the field description
Reset Value: 0x00000004

Bits	Name	Access	Reset	Description
31:3	RES	RO	0x00000000	Reserved
2:0	LVL_CTR	R/W	0x4	PMU PAREG configurations

4.1.49 PMU bypass (PMU_BYPASS)

Address: 0x000042C4
Access: See the field description
Reset Value: 0x00000000

Bits	Name	Access	Reset	Description
31:2	RES	RO	0x00000000	Reserved
1	SWREG	R/W	0x0	If set, bypass the switching regulator
0	PAREG	R/W	0x0	If set, bypass the PA regulator

4.1.50 Real-time clock sleep count (RTC_SLEEP_COUNT)

Address: 0X000042F8
Access: See the field description
Reset Value: 0x00000036

Least cycle number hold in sleep state.

Bits	Name	Access	Reset	Description
31:6	RES	RO	0x0000000	Reserved
5:0	THRESHOLD	R/W	0x36	The minimum number of RTC clock cycles needed to stay in sleep state

4.1.51 SRIF clock select (SRIF_CLOCK)

Address: 0x00004310
Access: See the field description
Reset Value: 0x00000001

This register selects the SRIF clock.

Bits	Name	Access	Reset	Description	
31:2	RES	RO	0x00000000	Reserved	
1	CORE_DIV	R/W	0x0	0	Core clock
				1	Core clock divided by 2
0	SEL	R/W	0x1	0	PCIE clock
				1	Core clock

4.1.52 SRIF clock gating (SRIF_CLOCK_GATING)

Address: 0x00004314
Access: See the field description
Reset Value: 0x00000001

This register controls the SRIF clock gating for the PCIE and CORE clocks.

Bits	Name	Access	Reset	Description	
31:2	RES	RO	0x00000000	Reserved	
1	PCIE_CLK_EN	R/W	0x0	0	Disable PCIE clock for SRIF
				1	Enable PCIE clock for SRIF
0	CORE_CLK_EN	R/W	0x1	0	Disable CORE clock for SRIF
				1	Enable CORE clock for SRIF

4.1.53 RTC spare bits 0 (RTC_SPARE0)

Address: 0x00004318
Access: See the field description
Reset Value: 0x00000000

Bits	Name	Access	Reset	Description
31:0	BITS	R/W	0x00000000	Spare programmable bits

4.1.54 RTC spare bits 1 (RTC_SPARE1)

Address: 0x0000431C
Access: See the field description
Reset Value: 0x00000000

Bits	Name	Access	Reset	Description
31:0	BITS	R/W	0x00000000	Spare programmable bits

4.2 SoC PCIE registers

Table 4-4 summarizes the QCA9882 SoC PCIE registers.

Table 4-4 SoC PCIE Register Summary

Address	Name	Description	Page
0x0000800C	PCIE_CTRL	PCIE Control	page 45

4.2.1 PCIE control (PCIE_CTRL)

Address: 0x0000800C
Access: See the field description
Reset Value: See the field description

Bits	Name	Access	Reset	Description
31:21	RES	RO	0x000	Reserved
20	RST_MASK	R/W	0x0	If set, the PCIE core is not warm reset when PCIE reset is asserted
19:17	RES	RO	0x000	Reserved
16	IGNORE_AXI_PCIE_L1	R/W	0x0	If set, AXI_PCIE bridge status is ignored to enable L1
15	IGNORE_MAC_FOR_L1	R/W	0x0	If set, MAC status is ignored to enable L1
14	TARGET_L1_EN	R/W	0x0	One of the conditions needed for enabling L1
13	HOST_L1_EN	R/W	0x0	One of the conditions needed for enabling L1
12	TRAINING_RST_EN	R/W	0x0	If set, PCIE_WARM_RESET_L to the core is asserted when TRAINING_RST occurs
11	RDLH_LINK_RST_EN	R/W	0x0	If set, PCIE_WARM_RESET_L to the core is asserted when RDLH_LINK_UP occurs
10	LINK_REQ_RST_EN	R/W	0x0	If set, PCIE_WARM_RESET_L to the core is asserted when LINK_REQ_RST occurs
9	XMLH_LINK_RST_EN	R/W	0x1	If set, PCIE_WARM_RESET_L to the core is asserted when XMLH_LINK_UP occurs
8	APP_LTSSM_ENABLE	R/W	0x00000000	APP_LTSSM_ENABLE signal to PCIE core, enabling it to start communicating with the PCIE host
7	ASPM_TIMER_BASED_L1_DISABLE	R/W	0x00000000	SYS_AUX_PWR_DET signal to PCIE core
6	SYS_AUX_PWR_DET	R/W	0x00000000	SYS_AUX_PWR_DET signal to PCIE core
5:0	RES	RO	0x0	Reserved

4.3 SoC core registers

Table 4-5 summarizes the QCA9882 SoC core registers.

Table 4-5 SoC Core Register Summary

Address	Name	Description	Page
0x00009000	CORE_CTRL	SoC Core Control	page 46
0x00009004	CORE_PM	Power Management Status of PCIE	page 47
0x00009008	PCIE_INTR_ENABLE	PCIE Interrupt Enable	page 47
0x0000900C	PCIE_INTR_CAUSE	PCIE Interrupt Cause	page 47
0x00009010	CPU_INTR	CPU Interrupt Status	page 48
0x00009014	PCIE_INTR_CLR	PCIE Interrupt Cause Clear	page 48
0x00009018	SCRATCH_0	Scratch Register 0	page 48
0x0000901C	SCRATCH_1	Scratch Register 1	page 49
0x00009020	SCRATCH_2	Scratch Register 2	page 49
0x00009024	SCRATCH_3	Scratch Register 3	page 49

4.3.1 SoC core control (CORE_CTRL)

Address: 0x00009000
Access: See the field description
Reset Value: 0x00001000

Bits	Name	Access	Reset	Description
31:14	RES	RO	0x00000	Reserved
13	OUTBAND_PWRUP	R/W	0x0	Setting this bit triggers a PME message on PCIE
12	WAKE_L	R/W	0x1	Connects directly to the PCIE_WAKE pin
11	HOST_WAKE_INTR_CLR	W	0x0	Self-clearing clears the HOST_WAKE interrupt to the CPU
10	CPU_INTR	R/W	0x0	Setting this bit causes an interrupt to the CPU
9	PCIE_INTR	R/W	0x0	Setting this bit causes an interrupt to PCIE host
8	PCIE_REG_31	R/W	0x0	Bit [31] of the PCIE memory location to be accessed by the CPU; used by the address translation logic
7:0	PCIE_BAR	R/W	0x0	Bits [31:24] of the PCIE base address; used by the AXI fabric

4.3.2 SoC core power management status (CORE_PM)

Address: 0x00009004
Access: See the field description
Reset Value: 0x00000000

Bits	Name	Access	Reset	Description	
31:6	RES	RO	0x0000000	Reserved	
5:3	DSTATE	RO	0x00000000	The current system power management state:	
				0	D0_Active
				1	D1
				2	D2
				3	D3
				4	D0_Uninitialized
2	STATUS	RO	0x00000000	Indicates power management status	
1	AUX_PM_EN	RO	0x00000000	PM enable signal from PCIE core	
0	PME_EN	RO	0x00000000	PME enable from the PMCSR register inside the PCIE core	

4.3.3 PCIE interrupt enable (PCIE_INTR_ENABLE)

Address: 0x00009008
Access: See the field description
Reset Value: 0x00000000

Bits	Name	Access	Reset	Description
31:30	RES	RO	0x0	Reserved
29:0	VAL	R/W	0x00000000	Setting a bit in this register allows the corresponding interrupt source to interrupt the PCIE core

4.3.4 PCIE interrupt cause (PCIE_INTR_CAUSE)

Address: 0x0000900C
Access: See the field description
Reset Value: 0x00000000

Bits	Name	Access	Reset	Description
31:30	RES	RO	0x0	Reserved
29:0	VAL	RO	0x00000000	Interrupt cause register; setting a bit in this register causes an interrupt to the PCIE core

4.3.5 CPU interrupt status (CPU_INTR)

Address: 0x00009010
Access: See the field description
Reset Value: 0x00000000

Bits	Name	Access	Reset	Description
31:30	RES	RO	0x0	Reserved
29:0	STATUS	RO	0x00000000	Status of all the interrupt lines to the CPU

4.3.6 PCIE interrupt cause clear (PCIE_INTR_CLR)

Address: 0x00009014
Access: See the field description
Reset Value: 0x00000000

Bits	Name	Access	Reset	Description
31:30	RES	RO	0x0	Reserved
29:0	VAL	R/W	0x00000000	Self clearing interrupt cause clear to the PCIE core

4.3.7 Scratch register 0 (SCRATCH_0)

Address: 0x00009018
Access: Read-Only
Reset Value: 0x00000000

Bits	Name	Description
31:0	RES	Reserved; used for communication between host and target

4.3.8 Scratch register 1 (SCRATCH_1)

Address: 0x0000901C
Access: Read-Only
Reset Value: 0x00000000

Bits	Name	Description
31:0	RES	Reserved; used for communication between host and target

4.3.9 Scratch register 2 (SCRATCH_2)

Address: 0x00009020
Access: Read-Only
Reset Value: 0x00000000

Bits	Name	Description
31:0	RES	Reserved; used for communication between host and target

4.3.10 Scratch register 3 (SCRATCH_3)

Address: 0x00009024
Access: Read-Only
Reset Value: 0x00000000

Bits	Name	Description
31:0	RES	Reserved; used for communication between host and target

4.4 UART base registers

Table 4-6 summarizes the QCA9882 base registers for UART and UART2.

Table 4-6 UART base register summary

Address for UART	Address for UART2	Name	Description	Page
0x0000C000	0x00054C00	FIFO	UART Transmit and Receive	page 50
0x0000C004	0x00054C04	UART_CS	UART Configuration and Status	page 51
0x0000C008	0x00054C08	UART_CLOCK	UART Clock	page 52
0x0000C00C	0x00054C0C	UART_INT	UART Interrupt Control/Status	page 53
0x0000C010	0x00054C10	UART_INT_EN	UART Interrupt Enable	page 54

4.4.1 UART transmit and receive (FIFO)

Address: **UART**: 0x0000C000
UART2: 0x00054C00
Access: See the field description
Reset Value: 0x00000000

This register pushes data on the transmit FIFO and pops data off the receive FIFO. This interface can be used only if all other interfaces are disabled in UART configuration and status (UART_CS).

Bits	Name	Access	Reset	Description
31:10	RES	RO	0x000000	Reserved
9	UART_TX_CSR	R/W	0x0	A read returns the status of the transmit FIFO. If set, the transmit FIFO can accept more transmit data. Setting this bit pushes UART_TXRX_DATA on the transmit FIFO. Clearing this bit has no effect.
8	UART_RX_CSR	R/W	0x0	A read returns the status of the receive FIFO. If set, the receive data in UART_TXRX_DATA is valid. Setting this bit pops the receive FIFO if there is valid data. Clearing this bit has no effect.
7:0	UART_TXRX_DATA	R/W	0x00	A read returns receive data from the receive FIFO, but leave the FIFO unchanged. Receive data is valid only if UART_RX_CSR is also set. Write pushes the transmit data on the transmit FIFO if UART_TX_CSR is also set.

4.4.2 UART configuration and status (UART_CS)

Address: **UART:** 0x0000C004
UART2: 0x00054C04
Access: See the field description
Reset Value: See the field description

This register configures the UART operation and reports the operating status.

Bits	Name	Access	Reset	Description
31:16	RES	RO	0x0000	Reserved
15	UART_RX_BUSY	RO	(undef)	Set if there is receive data; cleared when receive is completely idle.
14	UART_TX_BUSY	RO	(undef)	Set when data is ready to transmit or being transmitted; cleared when transmit is completely idle
13	URT_HOST_INT_EN	R/W	0x0	Enables UART_HOST_INT
12	UART_HOST_INT	RO	(undef)	Set while the host interrupt is being asserted; cleared when host interrupt is deasserted
11	UART_TX_BREAK	R/W	0x0	Blocks the transmit FIFO and causes a break to be continuously transmitted. The transmit FIFO resumes normal operation when this bit is clear.
10	UART_RX_BREAK	RO	(undef)	Set while a break is being received; cleared when the receive break stops
9	UART_SERIAL_TX_ READY	RO	(undef)	Set while serial Tx ready is asserted; cleared when serial Tx ready is deasserted
8	UART_TX_READY_ OVERRIDE	R/W	0x0	Overrides Tx ready flow control. If clear, Tx ready is controlled by UART_FLOW_CONTROL_MODE. If set, Tx ready is true.
7	UART_RX_READY_ OVERRIDE	R/W	0x0	Overrides Rx ready flow control. If clear, Rx ready is controlled by UART_FLOW_CONTROL_MODE. If set, Rx ready is true.
6	UART_DMA_EN	R/W	0x0	Enables the DMA interface mode. If set, then Tx and Rx FIFO access through UART transmit and receive (FIFO) is disabled. Instead, these FIFOs are connected to the internal DMA interface, if available.
5:4	UART_FLOW_ CONTROL_MODE	R/W	0x0	Selects which hardware flow control to enable: 0x0 — None — Disable hardware flow control. Serial Tx and Rx ready are controlled by UART_RX_READY_ OVERRIDE and UART_TX_READY_OVERRIDE. 0x2 — Hardware — Enable standard RTS/CTS flow control to control UART_SERIAL_TX_READY and UART_SERIAL_ RX_READY. 0x3 — Inverted — Enable inverted RTS/CTS flow control to control serial Tx ready and serial Rx ready.
3:2	UART_INTERFACE_ MODE	R/W	0x0	Selects which serial port interface to enable: 0x0 — None — Disable serial port. 0x2 — DTE — Configure the serial port for data terminal equipment operation. Tx on TD, Rx on RD, flow control out on RTS, flow control in on CTS. 0x3 — DCE — Configure serial port for data communication for data communication equipment operation. Tx on RD, Rx on TD, flow control out on CTS, flow control in on RTS.
1:0	UART_PARITY_ MODE	R/W	0x0	Selects the parity mode for transmit and receive data: 0x0 — None — Parity is not transmitted nor received. 0x2 — Odd — Odd parity transmitted and checked on receive. 0x3 — Even — Even parity transmitted and checked on receive.

4.4.3 UART clock (UART_CLOCK)

Address: **UART**: 0x0000C008
UART2: 0x00054C08
Access: See the field description
Reset Value: 0x00000000

This register sets the scaling factors use by the serial clock interpolator to create the transmit bit clock and receive sample clock.

Bits	Name	Access	Reset	Description
31:24	RES	RO	0x00	Reserved
23:16	UART_CLOCK_SCALE	R/W	0x0	Serial clock divisor used to create a scaled SERIAL_CLOCK; brings the serial clock into a range that can be interpolated by UART_CLOCK_STEP. The actual divisor is (1 + UART_CLOCK_SCALE). Use the formula: UART_CLOCK_SCALE = truncate((1310*SERIAL_CLOCK_FREQ)/(131072*BAUD_CLOCK_FREQ))
15:0	UART_CLOCK_STEP	R/W	0x0000	The ratio of the scaled serial clock to the baud clock, as expressed by a 17-bit fraction. This value should range between 1310 - 13107 to maintain a better than ± 5% accuracy. Smaller is generally better, because the interpolation error that a small value causes is usually far less than the quantization error that a large value causes. Use the formula: UART_CLOCK_STEP = round((131072*BAUD_CLOCK_FREQ)/(SERIAL_CLOCK_FREQ/(UART_CLOCK_SCALE+1))

4.4.4 UART interrupt control/status (UART_INT)

Address: **UART**: 0x0000C00C
UART2: 0x00054C0C
Access: See the field description
Reset Value: 0x00000000

A read of this register returns the current interrupt status; unless otherwise stated:

- Setting a bit clears the individual interrupt
- Clearing a bit has no effect

Bits	Name	Access	Description
31:10	RES	RO	Reserved
9	UART_TX_EMPTY_INT	R/W1CLR	This bit is set high while the transmit FIFO is almost empty; interrupt, sticky (individual bits)
8	UART_RX_FULL_INT	R/W1CLR	This bit is set high while the receive FIFO is almost full, and triggers hardware flow control if enabled; interrupt, sticky (individual bits)
7	UART_RX_BREAK_OFF_INT	R/W1CLR	This bit is set high while a break is not received; interrupt, sticky (individual bits)
6	UART_RX_BREAK_ON_INT	R/W1CLR	This bit is set high while a break is received; interrupt, sticky (individual bits)
5	UART_RX_PARITY_ERR_INT	R/W1CLR	This bit is set high if receive parity checking is enabled and the receive parity does not match the value configured by UART_PARITY_EVEN; interrupt, sticky (individual bits)
4	UART_TX_OFLOW_ERR_INT	R/W1CLR	This bit is set high if the transmit FIFO overflowed; interrupt, sticky (individual bits)
3	UART_RX_OFLOW_ERR_INT	R/W1CLR	This bit is set high if the receive FIFO overflowed; interrupt, sticky (individual bits)
2	UART_RX_FRAMING_ERR_INT	R/W1CLR	This bit is set high if a receive framing error was detected; interrupt, sticky (individual bits)
1	UART_TX_READY_INT	R/W1CLR	This bit is set high if there is room for more data in the transmit FIFO. Setting this bit clears this interrupt if there is room for more data in the transmit FIFO; interrupt, sticky (individual bits).
0	UART_RX_VALID_INT	R/W1CLR	This bit is set high while there is data in the receive FIFO. Setting this bit clears this interrupt if there is no more data in the receive FIFO; interrupt, sticky (individual bits).

4.4.5 UART interrupt enable (UART_INT_EN)

Address: **UART**: 0x0000C010
UART2: 0x00054C10
Access: See the field description
Reset Value: 0x00000000

This register enables interrupts in UART interrupt control/status (UART_INT).

Bits	Name	Access	Reset	Description
31:10	RES	RO	0x000000	Reserved
9	UART_TX_EMPTY_INT_EN	R/W	0x0	Enables UART_TX_EMPTY_INT
8	UART_RX_FULL_INT_EN	R/W	0x0	Enables UART_RX_FULL_INT
7	UART_RX_BREAK_OFF_INT_EN	R/W	0x0	Enables UART_RX_BREAK_OFF_INT
6	UART_RX_BREAK_ON_INT_EN	R/W	0x0	Enables UART_RX_BREAK_ON_INT
5	UART_RX_PARITY_ERR_INT_EN	R/W	0x0	Enables UART_RX_PARITY_ERR_INT
4	UART_TX_OFLOW_ERR_INT_EN	R/W	0x0	Enables UART_TX_OFLOW_ERR_INT
3	UART_RX_OFLOW_ERR_INT_EN	R/W	0x0	Enables UART_RX_OFLOW_ERR_INT
2	UART_RX_FRAMING_ERR_INT_EN	R/W	0x0	Enables UART_RX_FRAMING_ERR_INT
1	UART_TX_READY_INT_EN	R/W	0x0	Enables UART_TX_READY_INT
0	UART_RX_VALID_INT_EN	R/W	0x0	Enables UART_RX_VALID_INT

4.5 Serial interface registers

Table 4-7 summarizes the QCA9882 serial interface (I^2C or SPI) registers.

Table 4-7 Serial interface register summary

Address	Name	Description	Page
0x00010000	SI_CONFIG	Serial Interface Configuration (I^2C or SPI)	page 55
0x00010004	SI_CS	Serial Interface Control and Status	page 56
0x00010008	SI_TX_DATA0	Serial Interface Transmit Data 0 (low-order)	page 57
0x0001000C	SI_TX_DATA1	Serial Interface Transmit Data 1 (high-order)	page 57
0x00010010	SI_RX_DATA0	Serial Interface Receive Data 0 (low-order)	page 58
0x00010014	SI_RX_DATA1	Serial Interface Receive Data 1 (high-order)	page 58

4.5.1 Serial interface configuration (SI_CONFIG)

Address: 0x00010000
Access: See the field description
Reset Value: 0x000500B0

When this register is written to, the serial interface clock has 1/divider of period of the bus clock. This register also determines which clock edge data is driven on and sampled, as well as serial interface properties, such as whether the data port has an external pull-up (and thus behaves like a pseudo-open drain) and whether the interface is I^2C or SPI.

Bits	Name	Access	Reset	Description	
31:20	RES	RO	0x000	Reserved	
19	ERR_INT	R/W	0x0	Determines if DONE_ERR triggers an interrupt	
18	BIDIR_OD_DATA	R/W	0x1	(I^2C interface only) Determines if the bi-directional data pin SI_SI is pseudo-open drain. If it is, it is only driven low when data is low and not driven when data is high.	
				0	Data out pin is not pseudo-open drain
				1	Data out pin is pseudo-open drain
17	RES	RO	0x0	Reserved	
16	I2C	R/W	0x1	Determines whether the serial interface is I^2C or SPI	
				0	SPI
				1	I^2C
15:8	RES	RO	0x00	Reserved	
7	POS_SAMPLE	R/W	0x1	Determines whether data is sampled on the positive edge of the serial interface clock	
				0	Sample on negative edge
				1	Sample on positive edge
6	POS_DRIVE	R/W	0x0	Determines if data is driven on the negative edge of I^2C clock	
				0	Drive on negative edge
				1	Drive on positive edge
5	INACTIVE_DATA	R/W	0x1	Determines the value of inactive data out	
				0	Inactive data is deasserted
				1	Inactive data is asserted
4	INACTIVE_CLK	R/W	0x1	Determines the value of inactive clock	
				0	Inactive clock is deasserted
				1	Inactive clock is asserted
3:0	DIVIDER	R/W	0x0	Determines the value of the clock divider for SI_CK. The core clock to be divided is 38.4 MHz.	
				0	Divide by 2
				1	Divide by 4
				2	Divide by 8
				3	Divide by 16
				4	Divide by 32
				5	Divide by 64
				6	Divide by 128
				7	Divide by 256
				8	Divide by 512
				9	Divide by 1024

4.5.2 Serial interface control/status (SI_CS)

Address: 0x00010004
Access: See the field description
Reset Value: 0x00000000

This register is used to control the serial interface and to keep the serial interface status.

Bits	Name	Access	Reset	Description
31:14	RES	RO	0x00000	Reserved
13:11	BIT_CNT_IN_ LAST_BYTE	R/W	0x0	Determines the number of bits (from 1 to 8) to send or to receive on the serial interface for the last byte
				0 — 8 bits
				1 — 1 bit
				2 — 2 bits
				... — ...
				7 — 7 bits
10	DONE_ERR	RO	0x0	Set by the serial interface logic when the current entire sequence (Tx and Rx) completes an error. This bit is cleared when the START bit is set in this register.
9	DONE_INT	R/W	0x0	Set by the serial interface logic when the entire current sequence (Tx and Rx) has completed. This bit is cleared when 1 is written to this field or when the START bit is set in this register This bit being set triggers an interrupt if the interrupt enable bit for the serial interface in the interrupt control register is asserted. When this bit is polled, clear the interrupt enable so no interrupt is generated.
8	START	R/W	0x0	Setting this bit starts a Tx/Rx sequence on the serial interface. TX_CNT bytes are transmitted on the interface then RX_CNT bytes are received. This bit is cleared right after it is set.
7:4	RX_CNT	R/W	0x0	These bits determine the number of bytes (from 0 to 8) to receive on the serial interface. Receive is started whenever the START bit is set. The chip select stays asserted and the clock continues running to receive from 0 to 8 bytes of data. The first byte is loaded into bits [7:0] of the Serial interface transmit data 0 (SI_TX_DATA0) register and the eighth byte (if needed) is loaded into bits [31:24] of the Serial interface receive data 1 (SI_RX_DATA1) register. No data is transmitted during the receive phase.
3:0	TX_CNT	R/W	0x0	These bits determine the number of bytes (from 0 to 8) to send on the serial interface. Data, starting with the DATA0 field of the SI_TX_DATA0 register and ending with the DATA7 field of the SI_ TX_DATA1 register, is sent out whenever the START bit is set. The chip select signal is asserted and the clock is running for the entire transmit. No data is received during the transmit.

4.5.3 Serial interface transmit data 0 (SI_TX_DATA0)

Address: 0x00010008
Access: See the field description
Reset Value: 0x00000000

This register, combined with Serial interface transmit data 1 (SI_TX_DATA1), contains the data bits sent out on the serial interface. Data is sent, starting with bits [7:0] of this register and ending with bits [31:24] of SI_TX_DATA1, when the START bit is set in the Serial interface control/status (SI_CS) register.The bits in each byte are sent out serially with the most significant bit being sent first.

Bits	Name	Access	Reset	Description
31:24	DATA3	R/W	0x00	Fourth byte transferred. Sent if the TX_CNT field of the SI_CS register is greater than 3.
23:16	DATA2	R/W	0x00	Third byte transferred. Sent if the TX_CNT field of the SI_CS register is greater than 2.
15:8	DATA1	R/W	0x00	Second byte transferred. Sent if the TX_CNT field of the SI_CS register is greater than 1.
7:0	DATA0	R/W	0x00	First byte transferred. Sent if the TX_CNT field of the SI_CS register is greater than 0.

4.5.4 Serial interface transmit data 1 (SI_TX_DATA1)

Address: 0x0001000C
Access: See the field description
Reset Value: 0x00000000

This register, combined with Serial interface transmit data 0 (SI_TX_DATA0), contains the data bits sent out on the serial interface. Data is sent, starting with bits [7:0] of the SI_TX_DATA0 register and ending with bits [31:24] of this register, when the START bit is set in the Serial interface control/status (SI_CS) register. The bits in each byte are sent out serially with the most significant bit being sent first.

Bits	Name	Access	Reset	Description
31:24	DATA7	R/W	0x00	Eighth byte transferred. Sent if the TX_CNT field of the SI_CS register is greater than 7.
23:16	DATA6	R/W	0x00	Seventh byte transferred. Sent if the TX_CNT field of the SI_CS register is greater than 6.
15:8	DATA5	R/W	0x00	Sixth byte transferred. Sent if the TX_CNT field of the SI_CS register is greater than 5.
7:0	DATA4	R/W	0x00	Fifth byte transferred. Sent if the TX_CNT field of the SI_CS register is greater than 4.

4.5.5 Serial interface receive data 0 (SI_RX_DATA0)

Address: 0x00010010
Access: See the field description
Reset Value: 0x00000000

This register, combined with Serial interface receive data 1 (SI_RX_DATA1), captures data bits from the serial interface after the transmit has completed. The first byte of data is placed in bits [7:0] of this register and the last byte of data is placed in bits [31:24] of the SI_RX_DATA1 register. The bits in each byte are captured serially with the most significant bit being captured first.

Bits	Name	Access	Reset	Description
31:24	DATA3	RO	0x00	Fourth byte received. Loaded if the RX_CNT field of the SI_CS register is greater than 3.
23:16	DATA2	RO	0x00	Third byte received. Loaded if the RX_CNT field of the SI_CS register is greater than 2.
15:8	DATA1	RO	0x00	Second byte received. Loaded if the RX_CNT field of the SI_CS register is greater than 1.
7:0	DATA0	RO	0x00	First byte received. Loaded if the RX_CNT field of the SI_CS register is greater than 0.

4.5.6 Serial interface receive data 1 (SI_RX_DATA1)

Address: 0x00010014
Access: See the field description
Reset Value: 0x00000000

This register, combined with Serial interface receive data 0 (SI_RX_DATA0), captures data bits from the interface after the transmit has completed. The first byte of data is placed in bits [7:0] of the SI_RX_DATA0 register and the last byte of data is placed in bits [31:24] of this register. The bits in each byte are captured serially with the most significant bit being captured first.

Bits	Name	Access	Reset	Description
31:24	DATA7	RO	0x00	Eighth byte received. Loaded if the RX_CNT field of the SI_CS register is greater than 7.
23:16	DATA6	RO	0x00	Seventh byte received. Loaded if the RX_CNT field of the SI_CS register is greater than 6.
15:8	DATA5	RO	0x00	Sixth byte received. Loaded if the RX_CNT field of the SI_CS register is greater than 5.
7:0	DATA4	RO	0x00	Fifth byte received. Loaded if the RX_CNT field of the SI_CS register is greater than 4.

4.6 WLAN GPIO registers

Table 4-8 summarizes the QCA9882 WLAN GPIO registers. The address column refers to the offset from the base address configured by the host. The host accesses these registers' WLAN GPIO. At reset, an on-chip OTP initializes some registers, while the host or the QCA9882 hardware must program the others.

Table 4-8 WLAN GPIO register summary

Address	Name	Description	Page
0x00014000	WLAN_GPIO_OUT	GPIO Output	page 60
0x00014004	WLAN_GPIO_OUT_W1TS	GPIO Output Set Selected Bits	page 60
0x00014008	WLAN_GPIO_OUT_W1TC	GPIO Output Clear Selected Bits	page 60
0x0001400C	WLAN_GPIO_ENABLE	GPIO Enable	page 61
0x00014010	WLAN_GPIO_ENABLE_W1TS	GPIO Enable Set Selected Bits	page 61
0x00014014	WLAN_GPIO_ENABLE_W1TC	GPIO Enable Clear Selected Bits	page 61
0x00014018	WLAN_GPIO_IN	GPIO Input	page 62
0x0001401C	WLAN_GPIO_STATUS	GPIO Interrupt Status	page 62
0x00014020	WLAN_GPIO_STATUS_W1TS	GPIO Interrupt Status Set Selected Bits	page 62
0x00014024	WLAN_GPIO_STATUS_W1TC	GPIO Interrupt Status Clear Selected Bits	page 62
0x00014028	WLAN_GPIO_PIN0	Configures the Pin Type and Interrupt Behavior	page 63
0x0001402C	WLAN_GPIO_PIN1		page 64
0x00014030	WLAN_GPIO_PIN2		page 65
0x00014034	WLAN_GPIO_PIN3		page 66
0x00014038	WLAN_GPIO_PIN4		page 67
0x0001403C	WLAN_GPIO_PIN5		page 68
0x00014040	WLAN_GPIO_PIN6		page 69
0x00014044	WLAN_GPIO_PIN7		page 70
0x00014048	WLAN_GPIO_PIN8		page 71
0x0001404C	WLAN_GPIO_PIN9		page 72
0x00014050	WLAN_GPIO_PIN10		page 73
0x00014054	WLAN_GPIO_PIN11		page 74
0x00014058	WLAN_GPIO_PIN12		page 75
0x0001405C	WLAN_GPIO_PIN13		page 76
0x00014060	WLAN_GPIO_PIN14		page 77
0x00014064	WLAN_GPIO_PIN15		page 78
0x00014068	WLAN_GPIO_PIN16		page 79
0x0001406C	WLAN_GPIO_PIN17		page 80
0x00014074	WLAN_GPIO_PIN19		page 81
0x00014078	WLAN_GPIO_PIN20		page 82
0x0001407C	WLAN_GPIO_PIN21		page 83
0x00014080	WLAN_GPIO_PIN22		page 84
0x00014084	WLAN_GPIO_PIN23		page 85
0x000140B0	PINS_CONTROL	Controls the Override of Pins from the WLAN Side	page 86

4.6.1 GPIO output (WLAN_GPIO_OUT)

Address: 0x00014000
Access: See the field description
Reset Value: 0x00000000

When software writes this register, the write data is driven out for the pins that are enabled by the GPIO enable (WLAN_GPIO_ENABLE) register.

Bits	Name	Access	Reset	Description	
31:0	DATA	R/W	0x00000000	WLAN_GPIO pin data output:	
				0	Drive the pin low
				1	Drive the pin high

4.6.2 GPIO output W1TS (WLAN_GPIO_OUT_W1TS)

Address: 0x00014004
Access: See the field description
Reset Value: 0x00000000

This register is an alias of the GPIO output (WLAN_GPIO_OUT) register, which allows software to set selected bits without changing the value of other bits. For example, a write of 0x5 to this register sets bits [0] and [2] in WLAN_GPIO_OUT, but other bits remain unchanged.

Bits	Name	Access	Reset	Description	
31:0	DATA	W	0x00000000	For each bit position in the data word:	
				0	Do not change the bit
				1	Set the bit to 1

4.6.3 GPIO output W1TC (WLAN_GPIO_OUT_W1TC)

Address: 0x00014008
Access: See the field description
Reset Value: 0x00000000

This register is an alias of GPIO output (WLAN_GPIO_OUT), which allows software to clear selected bits without changing the value of other bits. For example, a write of 0x5 to this register clears bits [0] and [2] in WLAN_GPIO_OUT, but other bits remain unchanged.

Bits	Name	Access	Reset	Description	
31:0	DATA	W	0x00000000	For each bit position in the data word:	
				0	Do not change the bit
				1	Clear the bit to 0

4.6.4 GPIO enable (WLAN_GPIO_ENABLE)

Address: 0x0001400C
Access: See the field description
Reset Value: 0x00000000

When software writes this register, bits set to 1 enable the WLAN GPIO output driver for the corresponding GPIO pin. When the output driver is enabled, the corresponding GPIO_DATA_OUT bit or selected Sigma Delta PWM is driven to the pin. When the output driver is not enabled, no value is driven to the pin.

Bits	Name	Access	Reset	Description	
31:0	DATA	R/W	0x00000000	WLAN_GPIO pin data output enable.	
				0	The driver is not enabled for the corresponding pin
				1	The driver is enabled for the corresponding pin

4.6.5 GPIO enable W1TS (WLAN_GPIO_ENABLE_W1TS)

Address: 0x00014010
Access: See the field description
Reset Value: 0x00000000

This register is an alias of GPIO enable (WLAN_GPIO_ENABLE), which allows software to set selected bits without changing the value of other bits. For example, a write of 0x5 to this register sets bits [0] and [2] in WLAN_GPIO_ENABLE; all other bits remain unchanged.

Bits	Name	Access	Reset	Description	
31:0	DATA	W	0x00000000	For each bit position in the data word.	
				0	Do not change the bit
				1	Set the bit to 1

4.6.6 GPIO enable W1TC (WLAN_GPIO_ENABLE_W1TC)

Address: 0x00014014
Access: See the field description
Reset Value: 0x00000000

This register is an alias of GPIO enable (WLAN_GPIO_ENABLE) which allows software to clear selected bits without changing the value of other bits. For example, a write of 0x5 to this register clears bits [0] and [2] in WLAN_GPIO_ENABLE; all other bits remain unchanged.

Bits	Name	Access	Reset	Description	
31:0	DATA	W	0x00000000	For each bit position in the data word.	
				0	Do not change the bit
				1	Set the bit to 1

4.6.7 GPIO input (WLAN_GPIO_IN)

Address: 0x00014018
Access: See the field description
Reset Value: 0x00000000

Having software read this register returns data values at GPIO input (WLAN_GPIO_IN).

Bits	Name	Access	Reset	Description
31:0	DATA	RO	0x00000000	WLAN_GPIO pin data input.

4.6.8 GPIO status (WLAN_GPIO_STATUS)

Address: 0x0001401C
Access: See the field description
Reset Value: 0x00000000

WLAN_GPIO pin transitions can cause interrupts to be set in this register. The type of transition which cause interrupt are set in the WLAN_GPIO_PIN*x* registers.

Bits	Name	Access	Reset	Description	
31:0	INTERRUPT	R/W	0x00000000	WLAN_GPIO pin Interrupt pending.	
				0	Interrupt not pending
				1	Interrupt pending; remains set until software clears this bit

4.6.9 GPIO status W1TX (WLAN_GPIO_STATUS_W1TS)

Address: 0x00014020
Access: See the field description
Reset Value: 0x00000000

This register is an alias of GPIO status (WLAN_GPIO_STATUS), which allows software to set selected bits without changing the value of other bits. For example, a write of 0x5 to this register sets bits [0] and [2] in WLAN_GPIO_STATUS; other bits are unchanged.

Bits	Name	Access	Reset	Description	
31:0	INTERRUPT	W	0x00000000	For each bit position in the data word.	
				0	Do not change the bit
				1	Set the bit to 1

4.6.10 GPIO status W1TC (WLAN_GPIO_STATUS_W1TC)

Address: 0x00014024
Access: See the field description
Reset Value: 0x00000000

This register is an alias of GPIO status (WLAN_GPIO_STATUS), which allows software to clear selected bits without changing the value of other bits. For example, a write of 0x5 to this register clears bits [0] and [2] in WLAN_GPIO_STATUS; other bits are unchanged.

Bits	Name	Access	Reset	Description	
31:0	INTERRUPT	W	0x00000000	For each bit position in the data word.	
				0	Do not change the bit
				1	Clear the bit to 0

4.6.11 GPIO pin 0 (WLAN_GPIO_PIN0)

Address: 0x00014028
Access: See the field description
Reset Value: 0x00000008

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details.	
				1:0	GPIO
				2	Reserved
				3	RFSILENT_BB_L = 1 (Enable)
				4	RFSILENT_BB_L = 0 (Disable)
				5	RFSILENT_BB_L = From GPIO active low
				6	RFSILENT_BB_L = From GPIO active high
				8:7	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin causes SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 0:	
				0	Interrupt disabled for WLAN_GPIO 0
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 0
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 0
				3	Interrupt on any edge of WLAN_GPIO pin 0
				4	Interrupt on level 0 of WLAN_GPIO pin 0
				5	Interrupt on level 1 of WLAN_GPIO pin 0
				7:6	Reserved
6:5	PAD_PULL	R/W	0x0	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	Pin drive strength	
				0	22 mA driver
				1	45 mA driver
				2	68 mA driver
				3	90 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 0 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 0	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.12 GPIO pin 1 (WLAN_GPIO_PIN1)

Address: 0x0001402C
Access: See the field description
Reset Value: 0x00000028

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details.	
				0	GPIO
				1	LED_OUT
				5:2	GPIO
				8:6	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin causes SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 1:	
				0	Interrupt on 0->1 edge of WLAN_GPIO pin 1
				1	Interrupt on 1->0 edge of WLAN_GPIO pin 1
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 1
				3	Interrupt on any edge of WLAN_GPIO pin 1
				4	Interrupt on level 0 of WLAN_GPIO pin 1
				5	Interrupt on level 1 of WLAN_GPIO pin 1
				7:6	Reserved
6:5	PAD_PULL	R/W	0x1	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	Pin drive strength	
				0	4 mA driver
				1	8 mA driver
				2	12 mA driver
				3	24 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 1 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 1	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.13 GPIO pin 2 (WLAN_GPIO_PIN2)

Address: 0x00014030
Access: See the field description
Reset Value: 0x00000008

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details.	
				0	GPIO
				1	BT_ACTIVE (input for Bluetooth coexistence)
				2	Reserved
				3	I^2C data
				4	SPI_MASTER SPI_MISO
				5	Smart antenna bit [0]
				8:6	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also be to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin causes SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 2:	
				0	Interrupt disabled for WLAN_GPIO 2
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 2
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 2
				3	Interrupt on any edge of WLAN_GPIO pin 2
				4	Interrupt on level 0 of WLAN_GPIO pin 2
				5	Interrupt on level 1 of WLAN_GPIO pin 2
				7:6	Reserved
6:5	PAD_PULL	R/W	0x0	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	Pin drive strength.	
				0	4 mA driver
				1	8 mA driver
				2	12 mA driver
				3	24 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 2 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 2	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.14 GPIO pin 3 (WLAN_GPIO_PIN3)

Address: 0x00014034
Access: See the field description
Reset Value: 0x00000008

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details.	
				0	GPIO
				1	BT Priority (input for Bluetooth coexistence)
				2	Reserved
				3	GPIO
				4	SPI_MASTER SPI_CS_L
				5	Smart antenna bit [1]
				8:6	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin causes SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 3:	
				0	Interrupt disabled for WLAN_GPIO 3
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 3
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 3
				3	Interrupt on any edge of WLAN_GPIO pin 3
				4	Interrupt on level 0 of WLAN_GPIO pin 3
				5	Interrupt on level 1 of WLAN_GPIO pin 3
				7:6	Reserved
6:5	PAD_PULL	R/W	0x0	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	Pin drive strength	
				0	4 mA driver
				1	8 mA driver
				2	12 mA driver
				3	24 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 3 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 3	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.15 GPIO pin 4 (WLAN_GPIO_PIN4)

Address: 0x00014038
Access: See the field description
Reset Value: 0x00000048

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details.	
				0	GPIO
				1	WL_ACTIVE (output for Bluetooth coexistence)
				3:2	GPIO
				4	SPI master/I^{2}C clock
				5	Smart antenna bit [2]
				8:6	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 4:	
				0	Interrupt disabled for WLAN_GPIO 4
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 4
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 4
				3	Interrupt on any edge of WLAN_GPIO pin 4
				4	Interrupt on level 0 of WLAN_GPIO pin 4
				5	Interrupt on level 1 of WLAN_GPIO pin 4
				7:6	Reserved
6:5	PAD_PULL	R/W	0x2	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	Pin drive strength	
				0	4 mA driver
				1	8 mA driver
				2	12 mA driver
				3	24 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 4 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 4	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.16 GPIO pin 5 (WLAN_GPIO_PIN5)

Address: 0x0001403C
Access: See the field description
Reset Value: 0x00000008

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details.	
				0	GPIO
				1	BT Frequency (input for Bluetooth coexistence)
				2	Reserved
				3	GPIO
				4	SPI MASTER SPI_MOSI
				5	GPIO
				8:6	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also be sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 5:	
				0	Interrupt disabled for WLAN_GPIO 5
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 5
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 5
				3	Interrupt on any edge of WLAN_GPIO pin 5
				4	Interrupt on level 0 of WLAN_GPIO pin 5
				5	Interrupt on level 1 of WLAN_GPIO pin 5
				7:6	Reserved
6:5	PAD_PULL	R/W	0x0	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 5 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 5	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.17 GPIO pin 6 (WLAN_GPIO_PIN6)

Address: 0x00014040
Access: See the field description
Reset Value: 0x00000008

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details. Only applicable if PINS_CONTROL is set.	
				0	GPIO
				1	UART_RXD
				2	Reserved
				6:3	GPIO
				8:7	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 6:	
				0	Interrupt disabled for WLAN_GPIO 6
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 6
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 6
				3	Interrupt on any edge of WLAN_GPIO pin 6
				4	Interrupt on level 0 of WLAN_GPIO pin 6
				5	Interrupt on level 1 of WLAN_GPIO pin 6
				7:6	Reserved
6:5	PAD_PULL	R/W	0x0	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 6 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 6	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.18 GPIO pin 7 (WLAN_GPIO_PIN7)

Address: 0x00014044
Access: See the field description
Reset Value: 0x0000002A

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details. Only applicable if PINS_CONTROL is set.	
				0	GPIO
				1	UART_TXD
				6:2	GPIO
				8:7	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 7:	
				0	Interrupt disabled for WLAN_GPIO 7
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 7
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 7
				3	Interrupt on any edge of WLAN_GPIO pin 7
				4	Interrupt on level 0 of WLAN_GPIO pin 7
				5	Interrupt on level 1 of WLAN_GPIO pin 7
				7:6	Reserved
6:5	PAD_PULL	R/W	0x1	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 7 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 7	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.19 GPIO pin 8 (WLAN_GPIO_PIN8)

Address: 0x00014048
Access: See the field description
Reset Value: 0x00000028

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details. Only applicable if PINS_CONTROL is set.	
				0	GPIO
				1	UART2_TXD
				6:2	GPIO
				8:7	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 8:	
				0	Interrupt disabled for WLAN_GPIO 8
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 8
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 8
				3	Interrupt on any edge of WLAN_GPIO pin 8
				4	Interrupt on level 0 of WLAN_GPIO pin 8
				5	Interrupt on level 1 of WLAN_GPIO pin 8
				7:6	Reserved
6:5	PAD_PULL	R/W	0x1	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 8 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 8	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.20 GPIO pin 9 (WLAN_GPIO_PIN9)

Address: 0x0001404C
Access: See the field description
Reset Value: 0x00000028

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details. Only applicable if PINS_CONTROL is set.	
				0	GPIO
				1	UART2_RTS
				6:2	GPIO
				8:7	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 9:	
				0	Interrupt disabled for WLAN_GPIO 9
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 9
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 9
				3	Interrupt on any edge of WLAN_GPIO pin 9
				4	Interrupt on level 0 of WLAN_GPIO pin 9
				5	Interrupt on level 1 of WLAN_GPIO pin 9
				7:6	Reserved
6:5	PAD_PULL	R/W	0x1	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 9 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 9	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.21 GPIO pin 10 (WLAN_GPIO_PIN10)

Address: 0x00014050
Access: See the field description
Reset Value: 0x00000008

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details. Only applicable if PINS_CONTROL is set.	
				0	GPIO
				1	UART2_RXD
				6:2	GPIO
				8:7	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 10:	
				0	Interrupt disabled for WLAN_GPIO 10
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 10
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 10
				3	Interrupt on any edge of WLAN_GPIO pin 10
				4	Interrupt on level 0 of WLAN_GPIO pin 10
				5	Interrupt on level 1 of WLAN_GPIO pin 10
				7:6	Reserved
6:5	PAD_PULL	R/W	0x0	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 10 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 10	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.22 GPIO pin 11 (WLAN_GPIO_PIN11)

Address: 0x00014054
Access: See the field description
Reset Value: 0x00000008

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details. Only applicable if PINS_CONTROL is set.	
				0	GPIO
				1	UART2_CTS
				2	Reserved
				6:3	GPIO
				8:7	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 11:	
				0	Interrupt disabled for WLAN_GPIO 11
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 11
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 11
				3	Interrupt on any edge of WLAN_GPIO pin 11
				4	Interrupt on level 0 of WLAN_GPIO pin 11
				5	Interrupt on level 1 of WLAN_GPIO pin 11
				7:6	Reserved
6:5	PAD_PULL	R/W	0x0	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 11 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 11	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.23 GPIO pin 12 (WLAN_GPIO_PIN12)

Address: 0x00014058
Access: See the field description
Reset Value: 0x00000008

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details. Only applicable in WLAN EJTAG Mode or if PINS_CONTROL is set.	
				0	JTAG TMS
				4:1	GPIO
				5	Smart antenna bit [0]
				6	GPIO
				8:7	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 12:	
				0	Interrupt disabled for WLAN_GPIO 12
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 12
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 12
				3	Interrupt on any edge of WLAN_GPIO pin 12
				4	Interrupt on level 0 of WLAN_GPIO pin 12
				5	Interrupt on level 1 of WLAN_GPIO pin 12
				7:6	Reserved
6:5	PAD_PULL	R/W	0x0	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 12 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 12	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.24 GPIO pin 13 (WLAN_GPIO_PIN13)

Address: 0x0001405C
Access: See the field description
Reset Value: 0x00000028

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details. Only applicable in WLAN EJTAG Mode or if PINS_CONTROL is set.	
				0	JTAG TCK
				4:1	GPIO
				5	Smart antenna bit [1]
				6	GPIO
				8:7	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 13:	
				0	Interrupt disabled for WLAN_GPIO 13
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 13
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 13
				3	Interrupt on any edge of WLAN_GPIO pin 13
				4	Interrupt on level 0 of WLAN_GPIO pin 13
				5	Interrupt on level 1 of WLAN_GPIO pin 13
				7:6	Reserved
6:5	PAD_PULL	R/W	0x1	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 13 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 13	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.25 GPIO pin 14 (WLAN_GPIO_PIN14)

Address: 0x00014060
Access: See the field description
Reset Value: 0x00000028

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details. Only applicable in WLAN EJTAG Mode or if PINS_CONTROL is set.	
				0	JTAG TDI
				4:1	GPIO
				5	Smart antenna bit [2]
				6	GPIO
				8:7	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 14:	
				0	Interrupt disabled for WLAN_GPIO 14
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 14
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 14
				3	Interrupt on any edge of WLAN_GPIO pin 14
				4	Interrupt on level 0 of WLAN_GPIO pin 14
				5	Interrupt on level 1 of WLAN_GPIO pin 14
				7:6	Reserved
6:5	PAD_PULL	R/W	0x1	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 14 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 14	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.26 GPIO pin 15 (WLAN_GPIO_PIN15)

Address: 0x00014064
Access: See the field description
Reset Value: 0x00000028

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details. Only applicable in WLAN EJTAG Mode or if PINS_CONTROL is set.	
				0	JTAG TDO
				6:1	GPIO
				8:7	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 15:	
				0	Interrupt disabled for WLAN_GPIO 15
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 15
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 15
				3	Interrupt on any edge of WLAN_GPIO pin 15
				4	Interrupt on level 0 of WLAN_GPIO pin 15
				5	Interrupt on level 1 of WLAN_GPIO pin 15
				7:6	Reserved
6:5	PAD_PULL	R/W	0x1	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 15 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 15	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.27 GPIO pin 16 (WLAN_GPIO_PIN16)

Address: 0x00014068
Access: See the field description
Reset Value: 0x0000000A

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details. Only applicable in WLAN EJTAG Mode or if PINS_CONTROL is set.	
				0	EJTAG warm reset
				5:1	GPIO
				8:6	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 16:	
				0	Interrupt disabled for WLAN_GPIO 16
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 16
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 16
				3	Interrupt on any edge of WLAN_GPIO pin 16
				4	Interrupt on level 0 of WLAN_GPIO pin 16
				5	Interrupt on level 1 of WLAN_GPIO pin 16
				7:6	Reserved
6:5	PAD_PULL	R/W	0x0	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 16 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 16	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.28 GPIO pin 17 (WLAN_GPIO_PIN17)

Address: 0x0001406C
Access: See the field description
Reset Value: 0x0000002A

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details. Only applicable in WLAN EJTAG Mode or if PINS_CONTROL is set.	
				5:0	GPIO
				8:6	Reserved
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WBT_PINS_OVERRIDE_HIGHLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 17:	
				0	Interrupt disabled for WLAN_GPIO 17
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 17
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 17
				3	Interrupt on any edge of WLAN_GPIO pin 17
				4	Interrupt on level 0 of WLAN_GPIO pin 17
				5	Interrupt on level 1 of WLAN_GPIO pin 17
				7:6	Reserved
6:5	PAD_PULL	R/W	0x1	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 17 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0		Reserved
0	SOURCE	R/W	0x0	Output source for GPIO pin 17	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.29 GPIO pin 19 (WLAN_GPIO_PIN19)

Address: 0x00014074
Access: See the field description
Reset Value: 0x00000048

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details.	
				0	Antenna A
				15:1	GPIO
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 19:	
				0	Interrupt disabled for WLAN_GPIO 19
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 19
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 19
				3	Interrupt on any edge of WLAN_GPIO pin 19
				4	Interrupt on level 0 of WLAN_GPIO pin 19
				5	Interrupt on level 1 of WLAN_GPIO pin 19
				7:6	Reserved
6:5	PAD_PULL	R/W	0x2	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 19 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 19	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.30 GPIO pin 20 (WLAN_GPIO_PIN20)

Address: 0x00014078
Access: See the field description
Reset Value: 0x00000048

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details.	
				0	Antenna B
				15:1	GPIO
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 20:	
				0	Interrupt disabled for WLAN_GPIO 20
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 20
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 20
				3	Interrupt on any edge of WLAN_GPIO pin 20
				4	Interrupt on level 0 of WLAN_GPIO pin 20
				5	Interrupt on level 1 of WLAN_GPIO pin 20
				7:6	Reserved
6:5	PAD_PULL	R/W	0x2	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 20 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 20	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.31 GPIO pin 21 (WLAN_GPIO_PIN21)

Address: 0x0001407C
Access: See the field description
Reset Value: 0x00000048

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details.	
				0	Antenna C
				15:1	GPIO
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 21:	
				0	Interrupt disabled for WLAN_GPIO 21
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 21
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 21
				3	Interrupt on any edge of WLAN_GPIO pin 21
				4	Interrupt on level 0 of WLAN_GPIO pin 21
				5	Interrupt on level 1 of WLAN_GPIO pin 21
				7:6	Reserved
6:5	PAD_PULL	R/W	0x2	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 21 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 21	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.32 GPIO pin 22 (WLAN_GPIO_PIN22)

Address: 0x00014080
Access: See the field description
Reset Value: 0x00000048

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details.	
				0	Antenna D
				15:1	GPIO
10	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 22:	
				0	Interrupt disabled for WLAN_GPIO 22
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 22
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 22
				3	Interrupt on any edge of WLAN_GPIO pin 22
				4	Interrupt on level 0 of WLAN_GPIO pin 22
				5	Interrupt on level 1 of WLAN_GPIO pin 22
				7:6	Reserved
6:5	PAD_PULL	R/W	0x2	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 22 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 22	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.33 GPIO pin 23 (WLAN_GPIO_PIN23)

Address: 0x00014084
Access: See the field description
Reset Value: 0x00000048

This register configures the pin type and interrupt behavior.

Bits	Name	Access	Reset	Description	
31:15	RES	RO	0x00000	Reserved	
14:11 10	CONFIG	R/W	0x0	Configures the function of the WLAN_GPIO pin. Pin functions are independently selected. See the pin list for function details.	
				0	Antenna E
				15:0	GPIO
	WAKEUP_ENABLE	R/W	0x0	When this bit is set, an interrupt caused by this WLAN_GPIO pin is also sent to the power control FSM, causing interrupt events on this pin to wake the chip if in SLEEP mode. Wakeup enable interrupt pulses must be at least 2 msec in width to ensure they are captured by the high speed clock after wakeup. Wakeup enable interrupts can only be level sensitive, not edge sensitive.	
				0	Interrupt on this pin does not cause SLEEP wakeup
				1	Interrupt on this pin cause SLEEP wakeup
9:7	INT_TYPE	R/W	0x0	An interrupt is set if the following occurs on WLAN_GPIO pin 23:	
				0	Interrupt disabled for WLAN_GPIO 23
				1	Interrupt on 0->1 edge of WLAN_GPIO pin 23
				2	Interrupt on 1->0 edge of WLAN_GPIO pin 23
				3	Interrupt on any edge of WLAN_GPIO pin 23
				4	Interrupt on level 0 of WLAN_GPIO pin 23
				5	Interrupt on level 1 of WLAN_GPIO pin 23
				7:6	Reserved
6:5	PAD_PULL	R/W	0x2	WLAN_GPIO pin pad pull	
				0	No pull
				1	Pull-up
				2	Pull-down
				3	Reserved
4:3	PAD_STRENGTH	R/W	0x1	WLAN_GPIO pin drive strength	
				0	1.2 mA driver
				1	3.6 mA driver
				2	4.8 mA driver
				3	7.2 mA driver
2	PAD_DRIVER	R/W	0x0	WLAN_GPIO pin 23 driver type	
				0	Push/pull driver
				1	Open drain driver
1	RES	RO	0x0	Reserved	
0	SOURCE	R/W	0x0	Output source for GPIO pin 23	
				0	GPIO output (WLAN_GPIO_OUT) register
				1	Reserved; must be 0

4.6.34 Pins control (PINS_CONTROL)

Address: 0x000140B0
Access: See the field description
Reset Value: 0x00000000

This register controls the override of pins from the WLAN side.

Bits	Name	Access	Reset	Description
31:3	RES	RO	0x00000000	Reserved
2	UART	R/W	0x0	Override for UART pins: GPIO6 and GPIO7
1	HIGH	R/W	0x0	Override for high pins: GPIO12 through GPIO17
0	LOW	R/W	0x0	Override for low pins: GPIO8 through GPIO11

4.7 Copy engine registers

Table 4-9 summarizes the QCA9882 copy engine (CE) registers. The eight copy engines offset the register address from these address bases:

0x57400	Copy Engine 0
0x57800	Copy Engine 1
0x57C00	Copy Engine 2
0x58000	Copy Engine 3
0x58400	Copy Engine 4
0x58800	Copy Engine 5
0x58C00	Copy Engine 6
0x59000	Copy Engine 7

Table 4-9 Copy engine register summary

Address Offset	Name	Description	Page
0x0	SR_BA	Source Ring Base Address	page 88
0x4	SR_SIZE	Source Ring Size	page 88
0x8	DR_BA	Destination Ring Base Address	page 88
0xC	DR_SIZE	Destination Ring and Destination Status Ring Size	page 88
0x10	CE_CTRL1	CE Control	page 89
0x14	CE_CTRL2	CE Control 2	page 89
0x18	CE_CMD	CE Command	page 89
0x1C	MSI_ADDR	Address for Message Signaled Interrupt/Write Generation	page 90
0x20	MSI_DATA	Data for Message Signaled Interrupt/Write Generation	page 90
0x24	TARGET_IE	Target CPU Line Interrupt Enable	page 90
0x28	TARGET_IS	Target CPU Line Interrupt Status	page 90
0x2C	HOST_IS	Host Line Interrupt Enable	page 91
0x30	HOST_IS	Host Line Interrupt Status	page 91
0x34	MISC_IE	Miscellaneous Interrupt Enable	page 92
0x38	MISC_IS	Miscellaneous Interrupt Enable	page 92
0x3C	SRC_RING_WR_IND	Source Ring Write Index	page 93
0x40	DST_RING_WR_INDEX	Destination Ring Write Index	page 93
0x44	CURRENT_SRRI	Value of Source Ring Read Index in CE	page 93
0x48	CURRENT_DRRI	Value of Destination Ring Read Index in CE	page 93
0x4C	SRC_WATERMARK	Source Ring Watermark	page 93
0x50	DST_WATERMARK	Destination Ring Watermark	page 93

4.7.1 Source ring base address (SR_BA)

Address Offset: 0x0
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:0	SR_BA	Source ring base address

4.7.2 Source ring size (SR_SIZE)

Address Offset: 0x4
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:16	RES	Reserved
15:0	SR_SIZE	Source ring size

4.7.3 Destination ring base address (DR_BA)

Address Offset: 0x8
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:0	DR_BA	Destination ring base address

4.7.4 Destination ring and destination status ring size (DR_SIZE)

Address Offset: 0xC
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:16	RES	Reserved
15:0	DR_SIZE	Destination ring and destination status ring size

4.7.5 CE control (CE_CTRL1)

Address Offset: 0x10
Access: Read/Write
Reset Value: See the field description

Bits	Name	Reset	Description
31:19	RES	0x0	Reserved
18	MSI_EN	0x0	Enable MSI writes
17	DST_RING_BYTE_SWAP_EN	0x0	Destination ring byte swap enable
16	SRC_RING_BYTE_SWAP_EN	0x0	Source ring byte swap enable
15:0	DMAX_LENGTH	0x80	Destination buffer max size

4.7.6 CE control 2 (CE_CTRL2)

Address Offset: 0x14
Access: Read/Write
Reset Value: See the field description

Bits	Name	Reset	Description	
31:30	RES	0x0	Reserved	
29:25	NUM_AXI_ OUTSTANDING_WRITES	0x8	Maximum number of outstanding write transactions on the AXI from the CE	
24:20	NUM_AXI_ OUTSTANDING_READS	0x18	Maximum number of outstanding read transactions on the AXI from the CE	
19:4	AXI_TIMEOUT	0x1F40	Timeout on AXI BUS (in µs)	
3:2	DEST_AXI_MAX_LEN	0x1	AXI read/write transactions maximum size on the destination side	
1:0	SRC_AXI_MAX_LEN	0x1	AXI read/write transactions maximum size on the source side	
			0	32
			1	64
			2	128
			3	256

4.7.7 CE command (CE_CMD)

Address Offset: 0x18
Access: See the field description
Reset Value: 0x0

Bits	Name	Access	Description
31:4	RES	RO	Reserved
3	HALT_STATUS	RO	Halt status
2	DST_FLUSH	R/W	Reset the destination index registers
1	SRC_FLUSH	R/W	Reset the source index registers
0	HALT	R/W	Halt the CE after the current copy is complete

4.7.8 Address for message signaled interrupt/write generation (MSI_ADDR)

Address Offset: 0x1C
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:0	MIS_ADDR	Address for message signaled interrupt/write generation

4.7.9 Data for message signaled interrupt/write generation (MSI_DATA)

Address Offset: 0x20
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:0	MSI_DATA	Data for message signaled interrupt/write generation

4.7.10 Target CPU line interrupt enable (TARGET_IE)

Address Offset: 0x24
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:5	RES	Reserved
4	DST_RING_LOW_WATERMARK	Destination ring low watermark interrupt enable
3	DST_RING_HIGH_WATERMARK	Destination ring high watermark interrupt enable
2	SRC_RING_LOW_WATERMARK	Source ring low watermark interrupt enable
1	SRC_RING_HIGH_WATERMARK	Source ring high watermark interrupt enable
0	COPY_COMPLETE	Copy complete enable

4.7.11 Target CPU line interrupt status (TARGET_IS)

Address Offset: 0x28
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:5	RES	Reserved
4	DST_RING_LOW_WATERMARK	Destination ring low watermark interrupt status
3	DST_RING_HIGH_WATERMARK	Destination ring high watermark interrupt status
2	SRC_RING_LOW_WATERMARK	Source ring low watermark interrupt status
1	SRC_RING_HIGH_WATERMARK	Source ring high watermark interrupt status
0	COPY_COMPLETE	Copy complete status

4.7.12 Host line interrupt enable (HOST_IE)

Address Offset: 0x2C
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:5	RES	Reserved
4	DST_RING_LOW_WATERMARK	Destination ring low watermark interrupt enable
3	DST_RING_HIGH_WATERMARK	Destination ring high watermark interrupt enable
2	SRC_RING_LOW_WATERMARK	Source ring low watermark interrupt enable
1	SRC_RING_HIGH_WATERMARK	Source ring high watermark interrupt enable
0	COPY_COMPLETE	Copy complete enable

4.7.13 Host line interrupt status (HOST_IS)

Address Offset: 0x30
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:5	RES	Reserved
4	DST_RING_LOW_WATERMARK	Destination ring low watermark interrupt status
3	DST_RING_HIGH_WATERMARK	Destination ring high watermark interrupt status
2	SRC_RING_LOW_WATERMARK	Source ring low watermark interrupt status
1	SRC_RING_HIGH_WATERMARK	Source ring high watermark interrupt status
0	COPY_COMPLETE	Copy complete status

4.7.14 Miscellaneous interrupt enable (MISC_IE)

Address Offset: 0x34
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:11	RES	Reserved
10	AXI_ERR	AXI timeout or AXI bus error interrupt enable
9	DST_ADDR_ERR	Destination misalignment error interrupt enable
8	SRC_LEN_ERR	Source zero length error interrupt enable
7	DST_MAX_LEN_VIO	Destination maximum length violated interrupt enable
6	DST_RING_OVERFLOW	Destination ring overflow interrupt enable
5	SRC_RING_OVERFLOW	Source ring overflow interrupt enable
4	DST_RING_LOW_WATERMARK	Destination ring low watermark interrupt status
3	DST_RING_HIGH_WATERMARK	Destination ring high watermark interrupt status
2	SRC_RING_LOW_WATERMARK	Source ring low watermark interrupt status
1	SRC_RING_HIGH_WATERMARK	Source ring high watermark interrupt status
0	COPY_COMPLETE	Copy complete status

4.7.15 Miscellaneous interrupt status (MISC_IS)

Address Offset: 0x38
Access: See the field description
Reset Value: 0x0

Bits	Name	Access	Description
31:11	RES	RO	Reserved
10	AXI_ERR	R/W1CLR	AXI timeout or AXI bus error interrupt status sticky (individual bits)
9	DST_ADDR_ERR	R/W1CLR	Destination misalignment error interrupt status sticky (individual bits)
8	SRC_LEN_ERR	R/W1CLR	Source zero length error interrupt status sticky (individual bits)
7	DST_MAX_LEN_VIO	R/W1CLR	Destination maximum length violated interrupt status sticky (individual bits)
6	DST_RING_OVERFLOW	R/W1CLR	Destination ring overflow interrupt status Sticky (individual bits)
5	SRC_RING_OVERFLOW	R/W1CLR	Source ring overflow interrupt status sticky (individual bits)
4	DST_RING_LOW_WATERMARK	R/W	Destination ring low watermark interrupt status
3	DST_RING_HIGH_WATERMARK	R/W	Destination ring high watermark interrupt status
2	SRC_RING_LOW_WATERMARK	R/W	Source ring low watermark interrupt status
1	SRC_RING_HIGH_WATERMARK	R/W	Source ring high watermark interrupt status
0	COPY_COMPLETE	R/W	Copy complete interrupt status sticky (individual bits)

4.7.16 Source ring write index (SRC_RING_WR_IND)

Address Offset: 0x3C
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:0	SRC_RING_WR_IND	Source ring write index

4.7.17 Destination ring write index (DST_RING_WR_INDEX)

Address Offset: 0x40
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31”0	DST_RING_WR_IND	Destination ring write index

4.7.18 Value of source ring read index in CE (CURRENT_SRRI)

Address Offset: 0x44
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:0	CURRENT_SRRI	Source ring read index

4.7.19 Value of destination ring read index in CE (CURRENT_DRRI)

Address Offset: 0x48
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:0	CURRENT_DRRI	Destination ring read index

4.7.20 Source Watermark (SRC_WATERMARK)

Address Offset: 0x4C
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:16	HIGH	Source ring high watermark
15:0	LOW	Source ring low watermark

4.7.21 Destination Watermark (DST_WATERMARK)

Address Offset: 0x50
Access: Read/Write
Reset Value: 0x0

Bits	Name	Description
31:16	HIGH	Destination ring high watermark
15:0	LOW	Destination ring low watermark

4.8 Copy engine wrapper registers

Table 4-9 summarizes the QCA9882 copy engine (CE) wrapper registers.

Table 4-10 Copy engine register summary

Address	Name	Description	Page
0x57000	CE_WRAPPER_ INTERRUPT_SUMMARY	CE Interrupt Status	page 94
0x57004	NUM_AXI_ OUTSTANDING	Maximum number of outstanding AXI transactions	page 94

4.8.1 CE interrupt status (CE_WRAPPER_INTERRUPT_SUMMARY)

Address: 0x57000
Access: Read-Only
Reset Value: 0x0

This register retrieves the status of the eight HOST_MSI and MISC interrupt lines.

Bits	Name	Description
31:16	RES	Reserved
15:8	HOST_MSI	Retrieves the status of the HOST_MSI interrupt
7:0	MISC	Retrieves the status of the miscellaneous interrupt

4.8.2 Maximum number of outstanding AXI transactions (NUM_AXI_ OUTSTANDING)

Address: 0x57004
Access: Read/Write
Reset Value: See the field description

Bits	Name	Reset	Description
31:10	RES	0x0	Reserved
9:5	WRITES	0x8	Maximum number of outstanding write transactions on AXI
4:0	READS	0x18	Maximum number of outstanding read transactions on AXI

4.9 PCIE configuration space register descriptions

Table 4-11 summarizes the QCA9882 PCIE configuration space registers. The offset column refers to the offset from the base address configured by the host. The host accesses these registers at boot time to detect the type of card present and to perform low-level configuration, such as assigning the base address to the card. At reset, an on-chip one-time programmable memory (OTP) is used to initialize some registers, while the host or the QCA9882 hardware must program the others. See version 1.0a of the PCIE standard for detailed information on these registers.

Table 4-11 PCIE configuration space register summary

Offset from Base Address Configured by the Host	Name	Description	Initialized By	Page
0x00	VENDOR_ID	Manufacturer Identification	OTP	page 96
0x02	DEVICE_ID	Device Type Identification	OTP	page 96
0x04	COMMAND	Device Accessibility Control	Host	page 96
0x06	STATUS	Device Functionality Status	QCA9882	page 97
0x08	REVISION_ID	Device Revision Identification	OTP	page 98
0x09	CLASS_CODE	Device Basic Function Identification	OTP	page 98
0x0C	CACHE_SZ	System Cache Line Size	Host	page 98
0x0D	LATENCY_TMR	Defines Minimum Time (in Bus Cycles) the Bus Master Can Retain Ownership of the Bus	Host	page 98
0x0E	HDR_TYPE	Device Configuration Header Format	OTP	page 99
0x10	BASE_ADDR	Base Address to Access WLAN Memory-Mapped Registers	Host	page 99
0x2C	SSYS_VEND_ID	Subsystem Manufacturer Identification	OTP	page 99
0x2E	SSYS_ID	Subsystem Device Type Identification	OTP	page 99
0x34	CAP_PTR	Device Capability List Pointer	QCA9882	page 100
0x3D	INT_PIN	Interrupt Message to the SOST (INTA)	OTP	page 100
0x40	Power Management Capability		OTP	page 101
0x44	Power Management Status/Control		Host	page 102
0x50	Message Capability ID		QCA9882	page 102
0x51	Message Capability Next Pointer		QCA9882	page 102
0x52	Message Control		OTP	page 103
0x54	Message Address		Host	page 104
0x58	Message Data		Host	page 104
0x70	PCIE Capabilities List		OTP	page 104
0x72	PCIE Capabilities		OTP	page 105
0x74	Device Capabilities		OTP	page 105
0x78	Device Control		Host	page 106
0x7A	Device Status		Host	page 106
0x7C	Link Capabilities		Host	page 107
0x80	Link Control		Host	page 107
0x82	Link Status		Host	page 108

4.9.1 Vendor ID (VENDOR_ID)

Offset: 0x00
Access: Read-Only
Size: 16 bits

This register contains the vendor identification number.

Bit	Name	Description
15:0	VENDOR_ID	Vendor identification

4.9.2 Device ID (DEVICE_ID)

Offset: 0x02
Access: Read-Only
Size: 16 bits

This register identifies the device type.

Bit	Name	Description
15:0	DEVICE_ID	Device identification

4.9.3 Command (COMMAND)

Offset: 0x04
Access: Read/Write
Size: 16 bits
Reset Value: Undefined

This register provides access control of the QCA9882 PCIE interface. The register is controlled by the host.

Bit	Name	Description	
15:9	RES	Reserved. Must be written with zero. On read, can contain any value.	
8	SERR_EN	System error enable	
		0	Disable (Default)
		1	Enable
7	RES	Reserved. Must be written with zero. On read, can contain any value.	
6	PAR_ERR_RESP	Parity error response	
		0	Disable (Default)
		1	Enable
5:3	RES	Reserved. Must be written with zero. On read, can contain any value.	
2	BUS_MSTR	Bus master	
		0	Disable
		1	Enable
1	MEM_SPACE	Memory space	
		0	Disable
		1	Enable
0	IO_SPACE	I/O space	
		0	Disable
		1	Enable (not used)

4.9.4 Status (STATUS)

Offset: 0x06
Access: See the field description
Size: 16 bits
Reset Value: 0x0290

This register provides status of the functionality provided by the QCA9882 PCIE interface. This register is mostly controlled by the QCA9882.

Bit	Name	Access	Description			
15	DETECT_PAR_ERR	R/W	Detected parity error			
			On Read:		*On Write:*	
			0	No error	0	Do not clear error bit
			1	Error	1	Clear error bit
14	SIG_SYS_ERR	R/W	Signaled system error			
			On Read:		*On Write:*	
			0	No error	0	Do not clear error bit
			1	Error	1	Clear error bit
13	RX_MAS_ABORT	R/W	Received master abort			
			On Read:		*On Write:*	
			0	No abort	0	Do not clear abort bit
			1	Abort	1	Clear abort bit
12	RX_TARG_ABORT	R/W	Received target abort			
			On Read:		*On Write:*	
			0	No abort	0	Do not clear abort bit
			1	Abort	1	Clear abort bit
11	SIG_TARG_ABORT	R/W	Signaled target abort			
			On Read:		*On Write:*	
			0	No abort	0	Do not clear abort bit
			1	Abort	1	Clear abort bit
10:9	RES	RO	Reserved			
8	MD_PAR_ERR	R/W	Master data parity error			
			On Read:		*On Write:*	
			0	No error	0	Do not clear error bit
			1	Error	1	Clear error bit
7:5	RES	RO	Reserved. Must be written with zero. On read, can contain any value.			
4	CAP_LIST	RO	Capabilities list. Hard-wired to 1.			
3	INT	RO	Interrupt status. Indicates outstanding interrupt request for that function. Note that this bit only associated with INTx messages, and has no meaning if the device is using message signaled interrupts.			
2:0	RES	RO	Reserved. Must be written with zero. On read, can contain any value.			

4.9.5 Revision ID (REVISION_ID)

Offset: 0x08
Access: Read/Write
Size: 8 bits
Reset Value: 0x01

Bit	Name	Description
7:0	REVISION_ID	Device revision ID.

4.9.6 Class code (CLASS_CODE)

Offset: 0x09
Access: Read-Only
Size: 24 bits
Reset Value: 0x020000

Bit	Name	Description
23:0	CLASS_CODE	Class code identification value that identifies the basic function of the device

4.9.7 Cache line size (CACHE_SZ)

Offset: 0x0C
Access: Read/Write
Size: 8 bits
Reset Value: 0x00

Bit	Name	Description
7:0	CACHE_SZ	Cache line size, in units of 32-bit words (4 bytes)

4.9.8 Latency timer (LATENCY_TMR)

Offset: 0x0D
Access: Read/Write
Size: 8 bits
Reset Value: 0x00

This register does not apply to PCIE.

Bit	Name	Description
7:0	LATENCY_TMR	Latency timer; hardwired to 0

4.9.9 Header type (HDR_TYPE)

Offset: 0x0E
Access: Read-Only
Size: 8 bits
Reset Value: 0x0

This register contains the header type information.

Bit	Name	Description
7:0	HDR_TYPE	Header type; non-bridge PCI device

4.9.10 Base address (BASE_ADDR)

Offset: 0x10
Access: Bits [15:0] are Read Only (always return 0)
Bits [31:16} are Read/Write
Reset Value: Undefined

Bit	Name	Description
31:0	BASE_ADDR	Base address for accessing the QCA9882 WLAN memory mapped registers

4.9.11 Subsystem vendor ID (SSYS_VEND_ID)

Offset: 0x2C
Access: Read-Only
Size: 16 bits
Reset Value: 0x0

Bit	Name	Description
15:0	SSYS_VEND_ID	Subsystem vendor identification number

4.9.12 Subsystem ID (SSYS_ID)

Offset: 0x2E
Access: Read-Only
Size: 16 bits
Reset Value: 0x0

Bit	Name	Description
15:0	SSYS_ID	Subsystem device identification number

4.9.13 Capabilities pointer (CAP_PTR)

Offset: 0x34
Access: Read-Only
Size: 8 bits
Reset Value: 0x40

Bit	Name	Description
7:0	CAP_PTR	Capabilities pointer value; Default value is provided by the QCA9882.

4.9.14 Interrupt line (INT_LINE)

Offset: 0x3C
Access: Read/Write
Size: 8 bits
Reset Value: 0x00

This host-controlled register contains the host interrupt controller's interrupt line value that the device's interrupt pin is connected to.

Bit	Name	Description
7:0	INT_LINE	Interrupt line value; default = 0

4.9.15 Interrupt pin (INT_PIN)

Offset: 0x3D
Access: Read-Only
Size: 8 bits
Reset Value: 0x1

This register defines which of the four PCIE interrupt request pins a PCIE function is connected to.

Bit	Name	Description
7:0	INT_PIN	Interrupt pin value; hardcoded to 1 (INTA only)

4.9.16 Power management capability

Offset: 0x40
Access: Read-Only
Reset Value: 0x0102_5001

The power management capability structure is required for all PCIE devices to support D0 and D3 device states to indicate PME message passing capability.

Bit	Name	Description	
31:27	PME Support	Indicates the power states in which the device can generate a PME; default = 0	
26	D2 Support	Always 0	
25	D1 Support	Always 0	
24:22	AUX Current	Reports the 3.3 V_{aux} current requirements for the function. It is encoded as:	
		Bit Value	**Max Current Required**
		111	375 mA
		110	320 mA
		101	270 mA
		100	220 mA (Default)
		011	160 mA
		010	100 mA
		001	55 mA
		000	0 mA
21	DSI	Device-specific initialization. Default = 0.	
20:19	RES	Reserved	
18:16	Version	Set to 0x2	
15:8	Next Capability Pointer	Offset to the next PCIE capability structure	
7:0	Capability ID	Must be set to 0x1	

4.9.17 Power management status/control

Offset: 0x44
Access: See the field description
Reset Value: 0x0000_0000

The power management capability structure is required for all PCIE devices to support D0 and D3 device states to indicate PME message passing capability.

Bit	Name	Access	Description	
31:24	Data	RO	Always 0	
23:16	PME Status	R/W	Devices that consume AUX power must preserve the value of this register when AUX power is available in such devices; this value is not modified by hot, warm, or cold reset.	
15:13	Data Scale	RO	Always 0	
12:8	PME Enable	R/W	Devices that consume AUX power must preserve the value of this register when AUX power is available in such devices; this register value is not modified by hot, warm, or cold reset.	
1:0	Power State	R/W	00	D0 (Default)
			01	D1
			10	D2
			11	D3

4.9.18 Message capability ID (CAP_ID)

Offset: 0x50
Access: Read-Only
Size: 8 bits
Reset Value: 0x05

Enumerates the PCIE capability structure in the PCIE configuration space capability list.

Bit	Name	Description
7:0	CAP_ID	Capability ID. Indicates the PCIE capability structure. This field must return a capability ID of 0x10 indicating that this is a PCIE capability structure.

4.9.19 Message capability next pointer (NXT_PTR)

Offset: 0x51
Access: Read-Only
Size: 8 bits
Reset Value: 0x60

This register contains the message capability next pointer.

Bit	Name	Description
7:0	NXT_PTR	Next capability pointer. Indicates the offset to the next PCIE capability structure or 0x00 if no other items exist in the linked list of capabilities.

4.9.20 Message control

Offset: 0x52
Access: See the field description
Size: 16 bits
Reset Value: 0x0000

This register provides system control over MSI. A device driver is not permitted to modify the register's read/write bits and fields.

Bit	Name	Access	Description	
15:8	RES	RO	Reserved	
7	64-bit Address Capable	R/W	0	The function is not capable of generating a 64-bit message address
			1	The function is capable of generating a 64-bit message address
6:4	Multiple Message Enable	R/W	System software writes to this field indicate the number of allocated messages (equal to or less than the number of requested messages). After reset, the field's state is 000. When MSI is enabled, a device is allocated at least one message, defined as:	
			Encoding	**Number of Allocated Messages**
			000	1
			001	2
			010	4
			011	8
			100	16
			101	32
			110	Reserved
			111	Reserved
3:1	Multiple Message Capable	RO	System software reads this field to determine the number of requested messages, defined as:	
			Encoding	**Number of Allocated Messages**
			000	1
			001	2
			010	4
			011	8
			100	16
			101	32
			110	Reserved
			111	Reserved
0	MSI Enable	R/W	0	The function is prohibited from using MSI to request service. The bit's state after reset is 0. After reset, MSI is disabled (bit 0 is cleared). System software can enable MSI by setting bit 0 and can modify the register's read/write bit fields.
			1	The function is permitted to use MSI to request service. System configuration software sets this bit to enable MSI. A device driver is prohibited to from writing this bit to mask a function's service request.

4.9.21 Message address

Offset: 0x54
Access: Read/Write
Reset Value: 0x00000000

Bit	Name	Description
31:2	Message Address	System-specified message address. If bit [0] of the Message control register is set, the contents specify the DWORD-aligned address for the MSI memory write.
1:0	RES	Reserved. Always returns to 0 on read.

4.9.22 Message data

Offset: 0x58
Access: Read/Write
Size: 16 bits
Reset Value: 0x0000

Bit	Name	Description
15:0	Message Data	System-specified message. Each MSI function is allocated up to 32 unique messages. System architecture specifies the number of unique messages supported by the system. If the message enable bit of the Message control register is set, the message data is driven onto the lower word of the memory write transaction's data phase.

4.9.23 PCIE capabilities list

Offset: 0x70
Access: Read-Only
Size: 16 bits
Reset Value: 0x9010

This register enumerates the PCIE capability structure in the PCIE configuration space capability list.

Bit	Name	Description
15:8	Next Capability Pointer	Indicates the offset to the next PCIE capability structure or 0x00 if no other items exist in the linked list of capabilities.
7:0	Capability ID	Indicates the PCIE capability structure. This field must return a capability ID of 0x10 indicating that this is a PCIE capability structure.

4.9.24 PCIE capabilities

Offset: 0x72
Access: Read-Only
Size: 16 bits
Reset Value: 0x0011

This register contains the PCIE capability values.

Bit	Name	Description	
15:14	RES	Reserved	
13:9	Interrupt Message Number	Required when the function is allocated more than one MSI interrupt number to contain the offset between the base message data and the MSI message generated when any status bit in either the slot status register or root port status register of the capability structure is set. Hardware must update this field so that it is correct if the MSI messages assigned to the device changes.	
8	Slot Implemented	Indicates that the PCIE link associated with this port connected to a slot. Hardwired to 0.	
7:4	Device Port Type	Indicates the PCIE logical device	
		0000	PCIE endpoint device
		All other encodings are reserved.	
3:0	Capability Version	Indicates the PCIE capability structure version number	

4.9.25 Device capabilities

Address: 0x74
Access: Read-Only
Reset Value: See the field description

Bits	Name	Reset	Description
31:28	RES	0x0	Reserved
27:26	SLOT_PWR_LIMIT_SCALE	0x0	Captured slot power limit scale; upstream port only
25:18	SLOT_PWR_LIMIT_VALUE	0x0	Captured slot power limit value; upstream port only
17:16	RES	0x0	Reserved
15	ERROR_REPORTING	0x1	Role-based error reporting
14:12	RES	0x0	Reserved
11:9	DEFAULT_EP_L1_LATENCY	0x0	Endpoint L1 acceptable latency, writeable via the DBI
8:6	DEFAULT_EP_L0S_LATENCY	0x0	Endpoint L0S acceptable latency, writeable via the DBI
5	EXTENDED_TAG	0x0	Extended tag field supported
4:3	PHANTOM	0x0	Phantom function supported
2:0	MAX_PAYLOAD_SIZE	0x0	MAX_PAYLOAD_SIZE supported

4.9.26 Device control

Address: 0x78
Access: See the field description
Reset Value: See the field description

Bits	Name	Access	Reset	Description
31:15	RES	RO	0x0	Reserved
14:12	MAX_READ_REQUEST_SIZE	RW	0x2	Maximum read request size
11	NO_SNOOP	RW	0x0	Enables the no snoop
10	AUX_POWER	RWS	0x0	Auxiliary power management enable
9	PHANTOM	RW	0x0	Phantom function enable
8	EXTENDED	RW	0x0	Extended tag field enable
7:5	MAX_PAYLOAD_SIZE	RW	0x0	Maximum payload size
4	RELAXED_ORDERING	RW	0x1	Enable relaxed ordering
3	UNSUPPORTED	RW	0x0	Unsupported request reporting enable
2	FATAL_ERROR	RW	0x0	Fatal error reporting enable
1	NON_FATAL	RW	0x0	Non-fatal reporting enable
0	CORRECTABLE	RW	0x0	Correctable error reporting enable

4.9.27 Device status

Address: 0x7A
Access: See the field description
Reset Value: 0x0

Bits	Name	Access	Description
31:6	RES	0x0	Reserved
5	TRANSACTION	RO	Transaction pending; set to 1 when non-posted requests are not completed, cleared when they are completed
4	AUX_POWER	RO	Auxiliary power detected
3	UNSUPPORTED	RW1C	Unsupported request detected; errors are logged in this register regardless of whether error reporting is enabled in the Device control register
2	FATAL	RW1C	Fatal error detected; errors are logged in this register regardless of whether error reporting is enabled in the Device control register
1	NON_FATAL	RW1C	Non-fatal error detected; errors are logged in this register regardless of whether error reporting is enabled in the Device control register
0	CORRECTABLE	RW1C	Correctable error detected; errors are logged in this register regardless of whether error reporting is enabled in the Device control register

4.9.28 Link capabilities

Address: 0x7C
Access: Read-Only
Reset Value: See the field description

Bits	Name	Reset	Description
31:24	PORT_NUM	0x0	Port number, writeable via the DBI
23:21	RES	0x0	Reserved
20	DATA_LINK	0x1	Data link layer active reporting capable, hardwired to 0x1
19	RES	0x0	Reserved
18	CLK_PM_CAP	0x0	Clock power management; the default is user-specified during hardware configuration; writeable via the DBI
17:15	L1_EXIT_LATENCY	0x0	L1 exit latency; the default is user-specified during hardware configuration; writeable via the DBI
14:12	L0S_EXIT_LATENCY	0x0	L0S exit latency; the default is user-specified during hardware configuration; writeable via the DBI
11:10	AS_LINK_PM_SPT	0x0	Active state link power management support; the default is user-specified during hardware configuration; writeable via the DBI
9:4	CX_NL	0x0	Maximum link width; the default is user-specified during hardware configuration; writeable via the DBI
3:0	MAXIMUM_LINK_ SPEED	0x1	Maximum link speed; 0x1 is the only supported value

4.9.29 Link control

Address: 0x80
Access: Read/Write
Reset Value: See the field description

Bits	Name	Reset	Description
31:9	RES	0x0	Reserved
8	CLOCK_PM	0x0	Enable clock power management; hardwired to 0 if clock power management is disabled in the Link capabilities register
7	EXTENDED_SYNCH	0x0	Extended synch
6	CLOCK_CFG	0x0	Common clock configuration
5	RETRAIN	0x0	Retrain link; hardwired to 0x0
4	LINK_DISABLE	0x0	Link disable; hardwired to 0
3	RCB	0x1	Read completion boundary
2	RES	0x0	Reserved
1:0	ACTIVE_STATE	0x0	Active state link power management control

4.9.30 Link status

Address: 0x82
Access: Read-Only
Reset Value: See the field description

Bits	Name	Reset	Description
31:14	RES	0x0	Reserved
13	DATA_LINK	0x0	Data link layer active
12	SLOT_CLK	0x0	Slot clock configuration; indicates that the component uses the same physical reference clock that the performance provides on the connector. The default is user set during hardware configuration and is writeable via the DBI.
11	LINK_TRAINING	0x0	Link training; hardwired to 0
10	RES	0x0	Reserved
9:4	NEGOTIATED	0x04	Negotiated link width; hardware set after link initialization
3:0	LINK_SPEED	0x1	The negotiated link speed (2.5 GBps)

5 Electrical Characteristics

5.1 Absolute maximum ratings

Table 5-1 summarizes the absolute maximum ratings and Table 5-2 lists the recommended operating conditions for the QCA9882.

Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document is not recommended.

Table 5-1 Absolute maximum ratings

Symbol	Parameter	Max Rating	Unit
V_{dd12}	Supply voltage	-0.3 to 1.8	V
V_{dd33}	Maximum I/O supply voltage	-0.3 to 3.6	V
RF_{in}	Maximum RF input (reference to 50 Ω)	+10	dBm
T_{store}	Storage temperature	-60 to 150	°C
T_j	Junction temperature	125	°C
ESD	Electrostatic discharge tolerance		
	RF5OUT_0, RF5OUT_1, RF5OUT_2	1500	V
	All other pins	2000	V

5.2 Recommended operating conditions

Table 5-2 Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AV_{dd12}	External regulator voltage	±3%	1.24	1.28	1.32	V
D_{VDD12}	Internal regulator voltage	—	—	1.28	—	V
V_{dd33}	I/O voltage	±5%	3.135	3.3	3.465	V
T_{case}	Case temperature	—	0	—	110	°C
Psi_{JT}	Junction-to-top-center of the package thermal resistance[1]	—	—	—	2.6	°C/W

1. For 12x12 mm LPCC package.

5.3 40-MHz clock characteristics

TCXO clock is not supported by the QCA9882; a 40 MHz crystal with no less than 12 pF loading must be used.

5.4 GPIO DC electrical characteristics

Table 5-3 lists the GPIO DC electrical characteristics, with:

T_{amb} = 25 °C

Table 5-3 General DC electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	0.7 * V_{DD33}	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	0.3 * V_{DD33}	V
V_{OH}	High Level Output Voltage	—	0.9 * V_{DD33}	—	—	V
V_{OL}	Low Level Output Voltage	—	0	—	0.1 * V_{DD33}	V

5.5 PCIE pin characteristics

Table 5-4 shows the QCA9882 PCIE interface pin characteristics.

Table 5-4 PCIE interface DC electrical characteristics

Signal Name	Pin	Type	Drive	PU/PD Resistance
RESET_L	15	IH	—	—
PCIE_RST_L	26	IL	—	150 KΩ
PCIE_WAKE_L	22	OD	90 mA	—
PCIE_CLKREQ_L	24	OD	90 mA	—
PCIE_REFCLK_N	29	IA	—	—
PCIE_REFCLK_P	30	IA	—	—
PCIE_TX_N	31	OA		—
PCIE_TX_P	32	OA	—	—
PCIE_RX_N	34	IA	—	—
PCIE_RX_P	33	IA	—	—
GPIO0	17	IO	90 mA	—
GPIO1	18	IO	27 mA	—
GPIO2	19	IO	90 mA	—
GPIO3	20	IO	90 mA	—
GPIO4	23	IO	27 mA	—
GPIO5	25	IO	90 mA	—
GPIO6	40	IO	90 mA	—
GPIO7	41	IO	27 mA	—
GPIO8	42	IO	27 mA	—
GPIO9	43	IO	27 mA	—
GPIO10	44	IO	90 mA	—
GPIO11	46	IO	90 mA	—
GPIO12	47	IO	90 mA	—
GPIO13	48	IO	27 mA	—
GPIO14	49	IO	27 mA	—
GPIO15	50	IO	27 mA	—
GPIO16	57	IO	90 mA	—
GPIO17	58	IO	27 mA	—
GPIO19	59	IO	27 mA	—
GPIO20	60	IO	27 mA	—
GPIO21	61	IO	27 mA	—
GPIO22	62	IO	27 mA	—
GPIO23	63	IO	27 mA	—

5.6 Power up sequencing

Figure 5-1 depicts the required reset sequence for the QCA9882 PCIE interface. Table 5-5 shows the QCA9882 PCIE interface timing parameters.

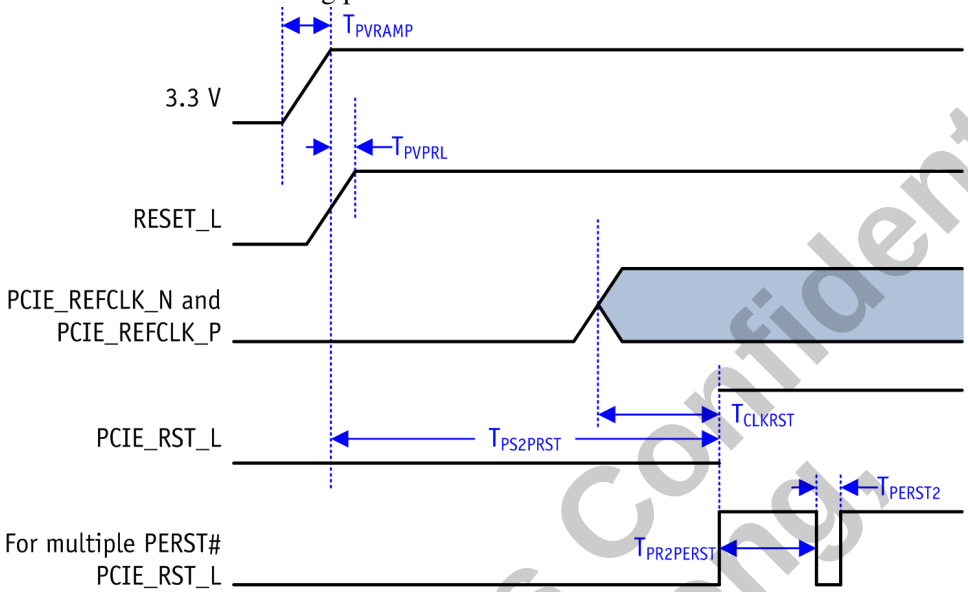

Figure 5-1 QCA9882 power up sequencing

Table 5-5 PCIE interface timing parameters

Symbol	Parameter	Min	Max	Unit
T_{PVRAMP}	Power supply ramp on 3.3 V	—	25	ms
T_{PVPRL}	Power valid to RESET_L asserted	0[1]	—	µs
T_{PRCLK}	RESET_L deasserted to PCIE_REFCLK_N and PCIE_REFCLK_P stable	100	—	µs
T_{CLKRST}	PCIE_REFCLK_N and PCIE_REFCLK_P stable to PCIE_RST_L deasserted	100[2]	—	µs
$T_{PS2PRST}$	Power supply stable to PCIE_RST_L deassert	10[3]	—	ms
$T_{PR2PERST}$	Initial PCIE_RST_L deassert to subsequent multiple PCIE_RST_L	40	—	ms
T_{PERST2}	Subsequent PCIE_RST_L asserted for multiple PCIE_RST_L	1	—	ms

1. It is recommended to leave the RST_L pin floating. At power up, internal power-on reset signal derived from 1.2 V and 3.3 V supply will ensure correct functionality.
2. This timing depends on hardware interface designs, such as Express Card, PCIE Mini Card, or PCIE desktop applications. The system must follow PCIE specifications, as well as TCLKRST.
3. $T_{PS2PRST}$ minimum timing must be observed.

5.7 Internal voltage regulators

Figure 5-2 depicts the voltages regulated by the QCA9882. Refer to the reference design schematics for details.

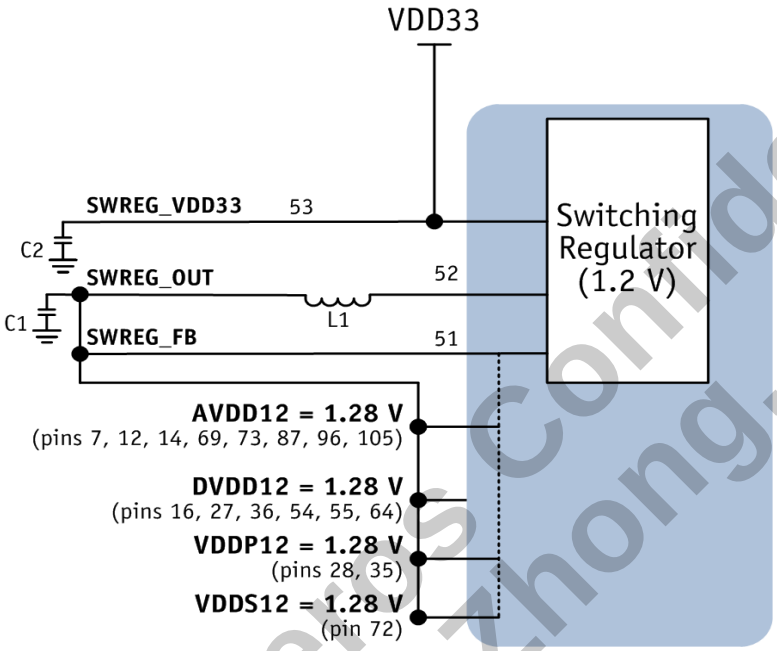

Figure 5-2 Output voltages regulated by the QCA9882

5.8 Radio characteristics

The following conditions apply to the typical per chain characteristics unless otherwise specified:

V_{DD12} = 1.2V
V_{DD33} = 3.3V, T_{amb} = 25 °C

5.8.1 Receiver characteristics

See these tables for the QCA9882 receiver characteristics:

Table	Receive Characteristics for:
Table 5-6	2.4 GHz Operation
Table 5-7	5 GHz Operation

Table 5-6 Rx characteristics for 2.4 GHz operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range	5 MHz center frequency	2.412	—	2.472	GHz
NF	Receive chain noise figure (max gain)	See Note 1	—	6.7	—	dB
S_{rf}	Sensitivity					
	CCK, 1 Mbps	See Note 2	-80	-96	—	dBm
	CCK, 11 Mbps		-76	-86	—	
	OFDM, 6 Mbps		-82	-92	—	
	OFDM, 54 Mbps		-65	-76	—	
	HT20, MCS0: 1 Stream, 2 Tx, 2 Rx	See Note 2	-82	-92	—	
	HT20, MCS7: 1 Stream, 2 Tx, 2 Rx		-64	-74	—	
	HT20, MCS8: 2 Stream, 2 Tx, 2 Rx		-82	-90	—	
	HT20, MCS15: 2 Stream, 2 Tx, 2 Rx		-64	-72	—	
	HT40, MCS0:1 Stream, 2 Tx, 2 Rx	See Note 2	-79	-90	—	
	HT40, MCS7: 1 Stream, 2 Tx, 2 Rx		-61	-72	—	
	HT40, MCS8: 2 Stream, 2 Tx, 2 Rx		-79	-88	—	
	HT40, MCS15: 2 Stream, 2 Tx, 2 Rx		-61	-68	—	
IIP1	Input 1 dB compression (min. gain)	—	—	-3.6	—	dBm
IIP3	Input third intercept point (min. gain)	—	—	6	—	dBm
Z_{RFin_input}	Recommended LNA differential drive impedance	Ch 0, Ch 1, Ch 2	—	50	—	Ω
R_{adj}	Adjacent channel rejection					
	CCK	See Note 3	—	41	—	dB
	OFDM, 6 Mbps		16	44	—	
	OFDM, 54 Mbps		-1	25	—	
	HT20, MCS0		16	26	—	
	HT20, MCS15		-2	10	—	
	HT40, MCS0		16	30	—	
	HT40, MCS15		-2	10	—	

1. For improved sensitivity performance, an external LNA may be used.
2. Sensitivity performance based on Qualcomm Atheros reference design, which includes Tx/Rx antenna switch and diplexer. Minimum values based on IEEE 802.11 specifications.
3. Typical values measured with reference design; minimum values are based on IEEE 802.11 specifications.

Table 5-7 Rx Characteristics for 5 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range	5 MHz center frequency	5.18	—	5.825	GHz
NF	Receive chain noise figure (max gain)	See Note 1	—	6.5	—	dB
S_{rf}	Sensitivity					
	OFDM, 6 Mbps	See Note 2	-82	-94	—	dBm
	OFDM, 54 Mbps	See Note 2	-65	-78	—	
	HT20, MCS0, 1 stream, 2 Tx, 2 Rx	See Note 2	-82	-94	—	
	HT20, MCS7, 1 stream, 2 Tx, 2 Rx		-64	-76	—	
	HT20, MCS8, 2 stream, 2 Tx, 2 Rx		-82	-94	—	
	HT20, MCS15, 2 stream, 2 Tx, 2 Rx		-64	-74	—	
	HT40, MCS0, 1 stream, 2 Tx, 2 Rx	See Note 2	-79	-92	—	
	HT40, MCS7, 1 stream, 2 Tx, 2 Rx		-61	-74	—	
	HT40, MCS8, 2 stream, 2 Tx, 2 Rx		-79	-90	—	
	HT40, MCS15, 2 stream, 2 Tx, 2 Rx		-61	-72	—	
	VHT20, MCS0, 1 stream, 2 Tx, 2 Rx	See Note 2	-82	-94	—	
	VHT20, MCS8, 2 stream, 2 Tx, 2 Rx		-59	-66	—	
	VHT40, MCS0, 1 stream, 2 Tx, 2 Rx	See Note 2	-79	-92	—	
	VHT40, MCS9, 2 stream, 2 Tx, 2 Rx		-54	-62	—	
	VHT80, MCS0, 1 stream, 2 Tx, 2 Rx	See Note 2	-76	-90	—	
	VHT80, MCS9, 2 stream, 2 Tx, 2 Rx		-51	-58	—	
IP1dB	Input 1 dB compression (min. gain)	—	—	-4	—	dBm
IIP3	Input third intercept point (min. gain)	—	—	7	—	dBm
Z_{RFin_input}	Recommended LNA single-ended drive impedance	Ch 0, Ch 1	—	50	—	Ω
R_{adj}	Adjacent channel rejection					
	11a OFDM, 6 Mbps	See Note 3	16	26	—	dB
	11a OFDM, 54 Mbps		-1	7	—	
	HT20, MCS0	See Note 3	16	20	—	dB
	HT20, MCS15		-2	0	—	
	HT40, MCS0	See Note 3	16	24	—	dB
	HT40, MCS15		-2	8	—	
	VHT20, MCS0, 1 stream	See Note 3	16	22	—	dB
	VHT20, MCS15, 2 stream		-9	-5	—	
	VHT40, MCS0, 1 stream	See Note 3	16	25	—	dB
	VHT40, MCS15, 2 stream		-9	0	—	
	VHT80, MCS0, 1 stream	See Note 3	16	20	—	dB
	VHT80, MCS9, 2 stream		-9	1	—	

1. For improved sensitivity performance, an external LNA may be used.
2. Sensitivity performance based on Qualcomm Atheros reference design, which includes Tx/Rx antenna switch, xLNA, and diplexer. Minimum values based on IEEE 802.11 specifications.
3. Typical values measured with reference design. Minimum values based on IEEE 802.11 specifications.

5.8.2 Transmitter characteristics

See these tables for the QCA9882 transmitter characteristics:

Table	Transmit Characteristics for:
Table 5-8	2.4 GHz Operation with Internal PA
Table 5-9	2.4 GHz Operation with External PA
Table 5-10	5 GHz Operation with Internal PA
Table 5-11	5 GHz Operation with External PA

Table 5-8 Tx Characteristics for 2.4 GHz Operation with Internal PA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	5 MHz center frequency	2.412	—	2.472	GHz
P_{out}	Mask compliant output power					
	1L	See Note 1	—	17	—	dBm
	6M		—	17	—	dBm
	HT20 MCS0		—	17	—	dBm
	HT40 MCS0		—	16	—	dBm
	EVM compliant output power:					
	54 Mbps	See Note 1	—	14	—	dBm
	HT20, MCS15		—	12	—	dBm
	HT40, MCS15		—	9	—	dBm
SP_{gain}	PA gain step	See Note 2	—	0.25	—	dB
A_{pl}	Accuracy of power leveling loop	See Note 3	—	±2	—	dB
Z_{RFout_load}	Recommended PA single-ended load impedance	See Note 4	—	50	—	Ω
RS	Synthesizer reference spur: 2/3 RF	—	—	-65	—	dBc

1. Measured with reference design including switch, filter, and diplexer.
2. Guaranteed by design.
3. Manufacturing calibration required.
4. See the impedance matching circuit in the Qualcomm Atheros reference design schematics. To achieve good RF performance, it is strongly recommended not to alter the RF portion of the Qualcomm Atheros reference design for different matching networks.

Table 5-9 Tx Characteristics for 2.4 GHz Operation with External PA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	5 MHz center frequency	2.412	—	2.472	GHz
P_{out}	Mask compliant output power					
	1 Mbps	See Note 1	—	7	—	dBm
	6 Mbps		—	5	—	dBm
	HT20, MCS0		—	5	—	dBm
	HT40, MCS0		—	4	—	dBm

Table 5-9 Tx Characteristics for 2.4 GHz Operation with External PA (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EVM		**Tx Power (dBm)[1]:**				
	802.11n, MCS15, HT20: 2 Tx Chain	-15	—	-37	—	dB
		-14	—	-38	—	
		-13	—	-38.5	—	
		-12	—	-41	—	
		-11	—	-40	—	
		-10	—	-38.5	—	
		-9	—	-37	—	
		-8	—	-38	—	
		-7	—	-38.5	—	
		-6	—	-36.5	—	
		-5	—	-34.5	—	
		-4	—	-32.5	—	
		-3	—	-31	—	
		-2	—	-29.5	—	
		-1	—	-28.5	—	
		0	—	-27	—	
	802.11n, MCS15, HT40: 2 Tx Chain	-15	—	-37.5	—	dB
		-14	—	-36	—	
		-13	—	-36.5	—	
		-12	—	-40	—	
		-11	—	-39	—	
		-10	—	-38.5	—	
		-9	—	-37	—	
		-8	—	-35.5	—	
		-7	—	-36	—	
		-6	—	-36	—	
		-5	—	-34.5	—	
		-4	—	-32.5	—	
		-3	—	-31	—	
		-2	—	-29.5	—	
		-1	—	-28.5	—	
		0	—	-27	—	
SP_{gain}	PA gain step	See Note 2	—	0.25	—	dB
A_{pl}	Accuracy of power leveling loop	See Note 3	—	±2	—	dB
Z_{RFout_load}	Recommended PA single-ended load impedance	See Note 4	—	50	—	Ω
RS	Synthesizer reference spur: 2/3 RF	—	—	-65	—	dBc

1. Measured at the chip output
2. Guaranteed by design.
3. Manufacturing calibration required.
4. See the impedance matching circuit in the Qualcomm Atheros reference design schematics. To achieve good RF performance, it is strongly recommended not to alter the RF portion of the Qualcomm Atheros reference design for different matching networks.

Table 5-10 Tx Characteristics for 5 GHz Operation with Internal PA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	20 MHz center frequency	5.18	—	5.825	GHz
P_{out}	Mask compliant output power					
	6M	See Note 1	—	15	—	dBm
	VHT20 MCS0		—	14	—	dBm
	VHT40 MCS0		—	14	—	dBm
	VHT80 MCS0		—	13	—	dBm
	EVM compliant output power					
	802.11a, 54 Mbps - single Tx chain	See Note 1	—	11	—	dBm
	802.11a, 54 Mbps - 2 Tx chain - CDD		—	11	—	
	802.11ac, MCS7, VHT20 - single Tx chain	See Note 1	—	11	—	dBm
	802.11ac, MCS7, VHT20 - 2 Tx chain		—	11	—	
	802.11ac, MCS7, VHT40 - single Tx chain		—	11	—	dBm
	802.11ac, MCS7, VHT40 - 2 Tx chain		—	11	—	
	802.11ac, MCS7, VHT80 - single Tx chain		—	11	—	dBm
	802.11ac, MCS7, VHT80 - 2 Tx chain		—	11	—	
	802.11ac, MCS8, VHT20 - single Tx chain	See Note 1	—	8	—	dBm
	802.11ac, MCS8, VHT20 - 2 Tx chain		—	8	—	
	802.11ac, MCS8, VHT40 - single Tx chain		—	7	—	dBm
	802.11ac, MCS8, VHT40 - 2 Tx chain		—	7	—	
	802.11ac, MCS8, VHT80 - single Tx chain		—	6	—	dBm
	802.11ac, MCS8, VHT80 - 2 Tx chain		—	6	—	
	802.11ac, MCS9, VHT40 - single Tx chain	See Note 1	—	7	—	dBm
	802.11ac, MCS9, VHT40 - 2 Tx chain		—	7	—	
	802.11ac, MCS9, VHT80 - single Tx chain		—	6	—	dBm
	802.11ac, MCS9, VHT80 - 2 Tx chain		—	6	—	
SP_{gain}	PA gain step	See Note 2	—	0.25	—	dB
A_{pl}	Accuracy of power leveling loop	See Note 3	—	±2	—	dB
Z_{RFout_load}	Output Impedance	See Note 4	—	50	—	Ω
SS	Sideband suppression	—	—	-40	—	dBc
LO_{leak}	LO leakage: at 2/3 of the RF output					
	@ RF=5.15-5.35 GHz (FCC)	—	—	-32	—	dBm
	@ RF=5.35-5.725 GHz (ETSI)			-36	—	dBm
	@ RF=5.725-5.825 GHz (FCC)			-30	—	dBm
RS	Synthesizer reference spur	—	—	-68	—	dBc

1. Measured with reference design including switch, filter, and diplexer.
2. Guaranteed by design.
3. Manufacturing calibration required.
4. See the sample impedance matching circuit in the Qualcomm Atheros reference design schematics. To achieve good RF performance, it is strongly recommended not to alter the RF portion of the Qualcomm Atheros reference design for different matching networks.

Table 5-11 Tx Characteristics for 5 GHz Operation with External PA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	20 MHz center frequency	5.18	—	5.825	GHz
P_{out}	Mask compliant output power					
	6 Mbps	See Note [1]	—	6	—	dBm
	VHT20, MCS0		—	6	—	
	VHT40, MCS0		—	5	—	
	VHT80, MCS0		—	5	—	
EVM		**Tx Power (dBm)[1]:**				
	802.11ac, MCS8, VHT20: 3 Tx Chain	-15	—	-40	—	dB
		-14	—	-40	—	
		-13	—	-39	—	
		-12	—	-40	—	
		-11	—	-40	—	
		-10	—	-39	—	
		-9	—	-39	—	
		-8	—	-38.5	—	
		-7	—	-37.5	—	
		-6	—	-37	—	
		-5	—	-35	—	
		-4	—	-33	—	
		-3	—	-31.5	—	
		-2	—	-29	—	
		-1	—	-27.5	—	
		0	—	-26.5	—	
	802.11ac, MCS9, VHT40: 3 Tx Chain	-15	—	-39.5	—	dB
		-14	—	-39	—	
		-13	—	-38	—	
		-12	—	-37.5	—	
		-11	—	-38.5	—	
		-10	—	-39	—	
		-9	—	-38.5	—	
		-8	—	-38	—	
		-7	—	-36.5	—	
		-6	—	-37	—	
		-5	—	-35.5	—	
		-4	—	-33.5	—	
		-3	—	-32.5	—	
		-2	—	-29.5	—	
		-1	—	-28	—	
		0	—	-26.5	—	

Table 5-11 Tx Characteristics for 5 GHz Operation with External PA (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EVM (cont.)	802.11ac, MCS9, VHT80: 3 Tx Chain	-15	—	-37.5	—	dB
		-14	—	-37	—	
		-13	—	-37	—	
		-12	—	-36	—	
		-11	—	-37	—	
		-10	—	-37	—	
		-9	—	-36.5	—	
		-8	—	-36	—	
		-7	—	-35	—	
		-6	—	-36	—	
		-5	—	-34.5	—	
		-4	—	-33	—	
		-3	—	-32	—	
		-2	—	-30	—	
		-1	—	-28	—	
		0	—	-26.5	—	
SP_{gain}	PA gain step	See Note 2	—	0.25	—	dB
A_{pl}	Accuracy of power leveling loop	See Note 3	—	±2	—	dB
Z_{RFout_load}	Output Impedance	See Note 4	—	50	—	Ω
SS	Sideband suppression	—	—	-40	—	dBc
LO_{leak}	LO leakage: at 2/3 of the RF output					
	@ RF=5.15-5.35 GHz (FCC)	—	—	-32	—	dBm
	@ RF=5.35-5.725 GHz (ETSI)			-36	—	
	@ RF=5.725-5.825 GHz (FCC)			-30	—	
RS	Synthesizer reference spur	—	—	-68	—	dBc

1. Measured at chip output.
2. Guaranteed by design.
3. Manufacturing calibration required.
4. See the sample impedance matching circuit in the Qualcomm Atheros reference design schematics. To achieve good RF performance, it is strongly recommended not to alter the RF portion of the Qualcomm Atheros reference design for different matching networks.

5.8.3 Synthesizer characteristics

Table 5-12 and Table 5-13 summarize the synthesizer characteristics for the QCA9882.

Table 5-12 Synthesizer Composite Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pn	Phase noise (at Tx_Out)					
	At 30 KHz offset	—	—	-103	—	dBc/Hz
	At 100 KHz offset		—	-103	—	
	At 500 KHz offset		—	-117	—	
	At 1 MHz offset		—	-124	—	
F_c	Center channel frequency	—	2.412	—	2.472	GHz
F_{ref}	Reference oscillator frequency	± 20 ppm[1]	—	40	—	MHz

1. Over temperature variation and aging.

Table 5-13 Synthesizer Composite Characteristics for 5 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pn	Phase noise (at Tx_Out)					
	At 30 KHz offset	—	—	-97	—	dBc/Hz
	At 100 KHz offset		—	-98	—	
	At 500 KHz offset		—	-103	—	
	At 1 MHz offset		—	-112	—	
F_c	Center channel frequency	Center frequency at 5 MHz spacing[1]	5.18	—	5.825	GHz
F_{ref}	Reference oscillator frequency	± 20 ppm[2]	—	40	—	MHz

1. Frequency is measured at the Tx output.
2. Over temperature variation and aging.

5.9 Power consumption parameters

These conditions apply to the typical characteristics unless otherwise specified:
V_{DD33} = 3.3V, T_{amb} = 25 °C

Table 5-14 through Table 5-19 show the typical power consumption as a function of the QCA9882's operating mode.

Table 5-14 Power consumption for 2.4 GHz operation (HT20)[1]

Operating Mode	AVDD33	DVDD33	AVDD12	DVDD12	Unit
Tx (Two-Chain[2]) with Internal PA	300	5	132	136	mA
Tx (Two-Chain[3]) with External PA	190	5	125	131	mA
Rx (Two-Chain)	79	5	191	197	mA

1. MCS15
2. Tx output power of 12 dBm
3. Tx output power of -10 dBm

Table 5-15 Power consumption for 2.4 GHz operation (HT40)[1]

Operating Mode	AVDD33	DVDD33	AVDD12	DVDD12	Unit
Tx (Two-Chain[2]) with Internal PA	300	5	130	162	mA
Tx (Two-Chain[3]) with External PA	190	5	128	156	mA
Rx (Two-Chain)	79	5	195	318	mA

1. MCS15
2. Tx output power of 12 dBm
3. Tx output power of -10 dBm

Table 5-16 Power consumption for 5 GHz operation (VHT20)[1]

Operating Mode	AVDD33	DVDD33	AVDD12	DVDD12	Unit
Tx (Two-Chain[2]) with Internal PA	330	5	125	126	mA
Tx (Two-Chain[3]) with External PA	157	5	125	119	mA
Rx (Two-Chain)	87	5	198	209	mA

1. MCS8
2. Tx output power of 8 dBm
3. Tx output power of -10 dBm

Table 5-17 Power consumption for 5 GHz operation (VHT40)[1]

Operating Mode	AVDD33	DVDD33	AVDD12	DVDD12	Unit
Tx (Two-Chain[2]) with Internal PA	326	5	125	163	mA
Tx (Two-Chain[3]) with External PA	157	5	125	157	mA
Rx (Two-Chain)	87	5	202	347	mA

1. MCS9
2. Tx output power of 7 dBm
3. Tx output power of -10 dBm

Table 5-18 Power consumption for 5 GHz operation (VHT80)[1]

Operating Mode	AVDD33	DVDD33	AVDD12	DVDD12	Unit
Tx (Two-Chain[2]) with Internal PA	317	5	140	205	mA
Tx (Two-Chain[3]) with External PA	158	5	140	214	mA
Rx (Two-Chain)	87	5	265	583	mA

1. MCS9
2. Tx output power of 6 dBm
3. Tx output power of -10 dBm

Table 5-19 Sleep power consumption

Operating Mode	AVDD33	DVDD33	AVDD12	DVDD12	Unit
Sleep Power Consumption	0	2	4	6	mA

6 Package Dimensions

The QCA9882 LPCC-108 package drawings and dimensions are provided in Figure 6-1 and Table 6-1.

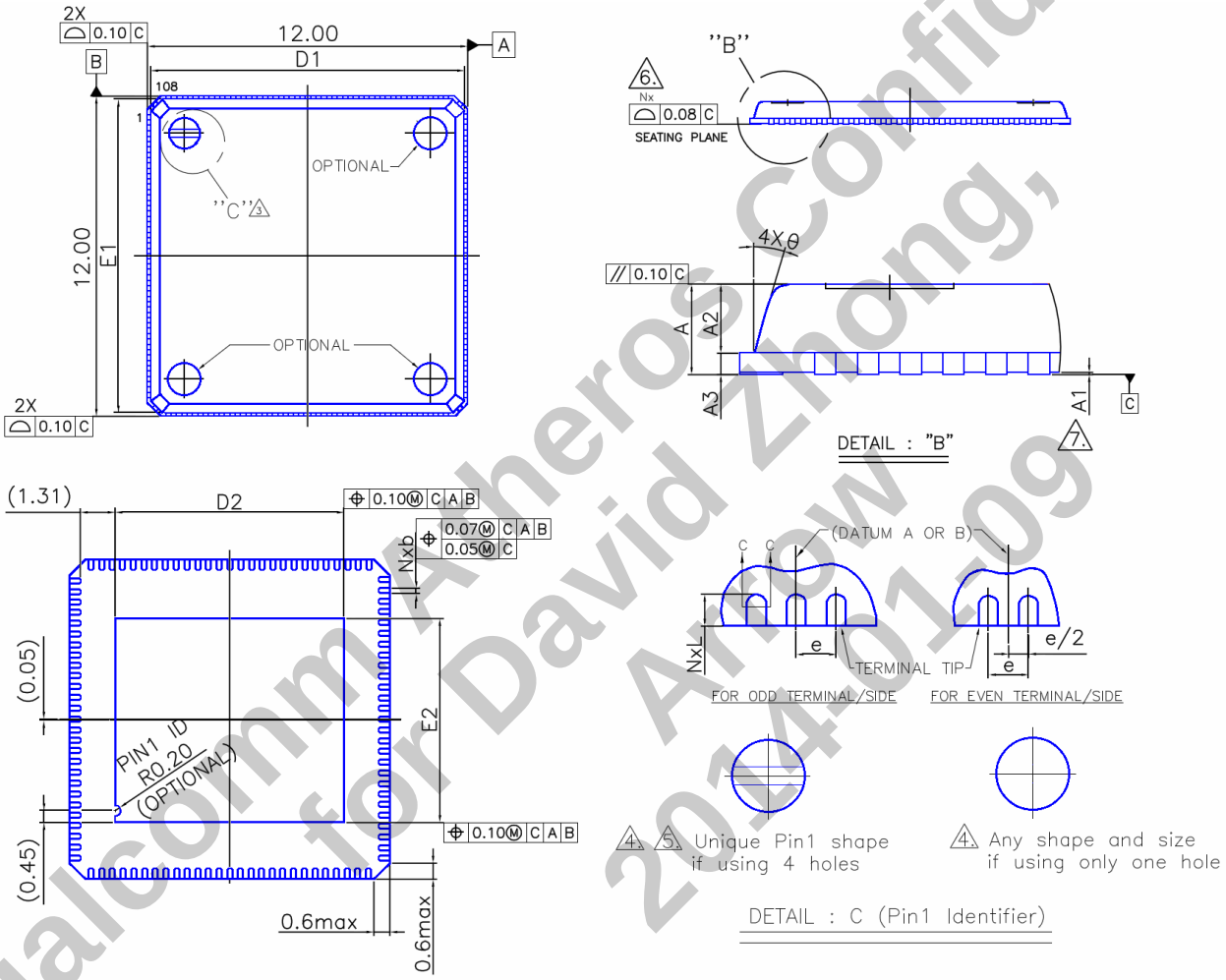

Figure 6-1 QCA9882 package details

Table 6-1 Package Dimensions

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	—	—	0.90	mm	—	—	0.035	inches
A1	0.00	0.02	0.05	mm	0.000	0.001	0.002	inches
A2	0.60	0.65	0.70	mm	0.024	0.026	0.028	inches
A3		0.20 REF		mm		0.008 REF		inches
b	0.15	0.20	0.25	mm	0.006	0.008	0.010	inches
D1/E1		11.75 BSC		mm		0.463 BSC		inches
D2	8.43	8.58	8.73	mm	0.332	0.338	0.344	inches
E2	7.50	7.65	7.80	mm	0.295	0.301	0.307	inches
e		0.40 BSC		mm		0.016 BSC		inches
L	0.30	0.40	0.50	mm	0.012	0.016	0.020	inches
θ	0°	—	14°	degrees	0°	—	14°	degrees

Controlling dimension: Millimeters
[1] N is the number of terminals = 108
[2] Dimensioning and tolerances confirm to ASME Y14.5M. - 2009
[3] The pin 1 identifier must exist on the top surface of the package by using the indentation mark or other feature of the package body
[4] Exact shape and size of this feature is optional
[5] Pin 1 identifier must be unique in shape if 4 holes are used
[6] Bilateral coplanarity zone applies to the exposed pad as well as the terminals
[7] Applied only to terminals

7 Ordering Information

The order number QCA9882-BR4A specifies a lead-free, halogen-free, standard-temperature version of the QCA9882. The order number QCA9882-BR4A-R specifies a tape-and-reel version of the QCA9882.