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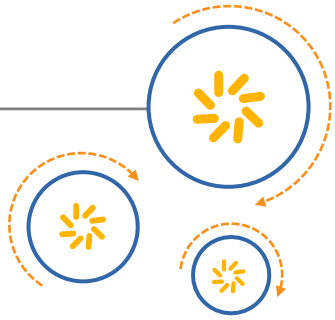

IPQ4018 Access Point SoC

Device Specification

80-Y9347-18 Rev. G

May 16, 2016

Qualcomm Atheros, Inc.
1700 Technology Drive
San Jose, CA 95110
U.S.A.

Revision history

Revision	Date	Description
A	May 2015	Initial release
B	July 2015	1. Section 3 “Electrical Specifications”: New. 2. Figure 4-3 and Table 4-2: Add Package B outline drawing. 3. Section 4.5 “Thermal Characteristics”: New
C	August 2015	1. Table 4-5 “Thermal Resistance”: Update qJB and qJC.
D	November 2015	**Introduction** ■ IPQ4018 general description: revised functional block diagram ■ IPQ4018 features: revised CPU clock, Flash memory, Network subsystem, High-speed interfaces **Pin Definitions** ■ DDR3L: revised DDR_DQ[x] and DDR_BA[x] functional description ■ Front-end: revised RBIAS functional description ■ PSGMII: added CLK25M_O voltage, revised PSGMII_SON, PSGMII_SOP, PSGMII_SIN, PSGMII_SIP functional description ■ GPIO interface: removed smart_ant0,smart_ant1, smart_ant2 and smart_ant3; revised GPIO52, GPIO63 type and functional description **Electrical Specifications** ■ Recommended operating conditions: updated operating temperature ■ Power sequencing: added power-on sequence ■ Digital characteristics: added digital I/O characteristics for 3.3 V IO and DDR3 PAD ■ Timing characteristics: added timing diagram conventions and rise and fall time specifications ■ Memory support: added DDR ■ Connectivity: added USB, UART, I2C, I2S, SPI (master), PSGMII ■ Radio characteristics: added Rx characteristics and Tx characteristics ■ Power consumption: added power consumption **Mechanical Information** ■ Device ordering information: updated ordering numbers ■ Thermal characteristics: updated thermal characteristics **Part reliability** ■ Reliability qualification summary: added silicon reliability results and package reliability results ■ Qualification sample description: added chip characteristics
E	December 2015	**Electrical Specifications** ■ Tx Characteristics: revised Tx characteristics ■ Power consumption: revised power consumption

Revision	Date	Description
F	May 2016	**Electrical Specifications** ■ Chapter 3.2.1 Crystal: updated crystal accuracy ■ Chapter 3.6.1 DDR: updated differential input cross point voltage ■ Table 3-6 Digital I/O characteristics for 3.3 V IO: added GPIO drive ■ strength **Mechanical Information** ■ Table 4-4 IPQ4018 order numbers: updated ordering numbers
G	May 2016	CPU frequency changed to 716.8 MHz DDR frequency changed to 537.6 MHz Chapter 4.2 Part marking: changed marking

Contents

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1 Introduction

1.1 IPQ4018 general description

The IPQ4018 is a highly integrated system-on-chip (SoC) designed for high-performance, power-efficient, and cost-effective 2×2, 802.11ac, dual-band concurrent access-point applications. The SoC incorporates a quad-core ARM Cortex A7 processor, two dual-band, concurrent 802.11ac Wave-2 Wi-Fi subsystems, and a five-port Gigabit Ethernet Layer2/3/4 multilayer switch supporting line rate network address translation (NAT). It supports one USB3.0 and one USB2.0. It also supports other miscellaneous interfaces, which can be configured as general purpose I/O pins. The block diagram in Figure 1-1 shows the major components of the SoC.

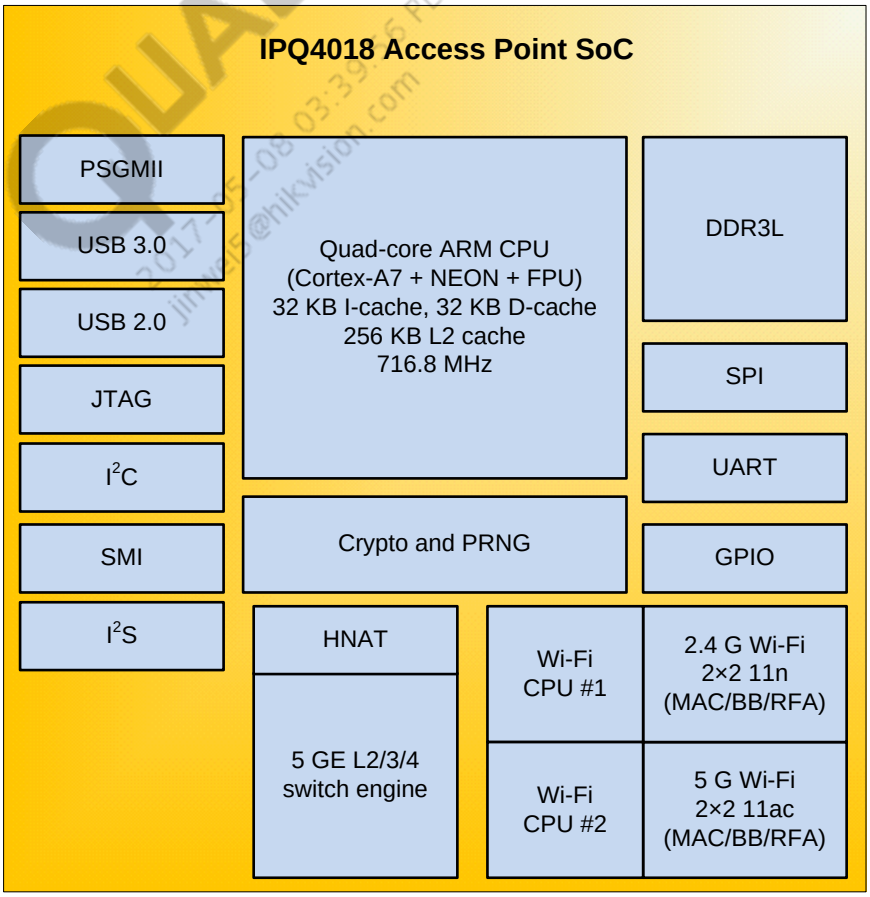


Figure 1-1 IPQ4018 functional block diagram

1.2 IPQ4018 features

- Quad-core ARM Cortex-A7 at 716.8 MHz
  - 32 KB instruction cache and 32 KB data cache per core
  - 256 KB L2 cache (shared)
  - Each core has NEON and FPU
  - Dynamic frequency scaling
  - Secure boot
- DRAM memory
  - JEDEC standard DDR3L SDRAM
  - Up to 256 MB
  - Supports 16-bit DDR interface
  - 537.6 MHz clock rate; 1075.2 MHz data rate
- Flash memory
  - SPI (x1b) flash
  - Supports SPI NOR
  - Supports SPI mode 0, 1, 2, 3
  - Cache and non-cache mode read channel
- Dual Wi-Fi subsystem with Qualcomm® VIVE™ technology
  - On-chip dual-band concurrent (DBDC) 2×2 2G 802.11n (256QAM) and 2×2 5G 802.11ac Wi-Fi, supporting MU-MIMO beamforming techniques.
  - Feature compatible with QCA99xx Wi-Fi chips
  - Two dedicated CPUs for Wi-Fi offloading and feature growth
  - Cooperates with QFE19x2 front-end chips or 3rd-party front-end chipsets
  - Smart antenna diversity
- Network subsystem
  - Integrated L2/3 multilayer switch/router
  - ACL (access control list) mask rules
  - Hardware network address translation (NAT) engine
  - Supports flow cookie
  - Traffic steering
  - Seamless integration with Linux network stack
  - Supports external gigabit Ethernet PHYs via PSGMII
- Security
  - Crypto engine

  - Encryption algorithms AES (128 and 256 bit key support) and DES/3DES
  - Authentication algorithms SHA1, SHA224 (the result of supporting SHA256), SHA256, and HMAC-SHA1 and HMAC-SHA2
  - XTS/CTR/CCM/CMAC mode for AES
  - CBC/ECB mode both for AES and DES/3DES.
- Trust Zone
- Pseudo-random number generator

- High-speed interfaces
  - 1× PSGMII
  - 1 × USB3.0
  - 1 × USB2.0
- Miscellaneous
  - I^2C
  - I^2S (single channel)
  - UART
  - JTAG
  - GPIO
- Package
  - 14 mm × 14 mm 180-pin Dual Row QFN package

1.3 Terms and abbreviations

Table 1-1 defines terms, abbreviations, and acronyms commonly used throughout this document.

Table 1-1 Terms and abbreviations

Term	Definition
ACL	Access control list
BB	Baseband
BLSP	BAM-enabled low-speed peripheral
DDR	Double data rate
GE	Gigabit Ethernet
LDO	Low drop-out (voltage regulator)
MII	Media-independent interface
NAT	Network address translation
PRNG	Pseudo-random number generator
PSGMII	Penta-SGMII

Table 1-1 Terms and abbreviations (cont.)

Term	Definition
SoC	System on a chip
SPI	Serial peripheral interface

1.4 Special marks

Table 1-2 defines special marks used in this document.

Table 1-2 Special marks

Mark	Definition
0x0000	Hexadecimal numbers are identified with an x in the number, for example, 0x0000. All numbers are decimal (base 10), unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number, for example, 0011 (binary).
|	A vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin Definitions

2.1 IPQ4018 pin map

Figure 2-1 shows a high-level view of the pin assignments.

The text within Figure 2-1 is difficult to read when viewing an 8½" by 11" hard copy. Other viewing options are available:

- Print that one page on an 11" by 17" sheet.
- View the graphic soft copy and zoom in.

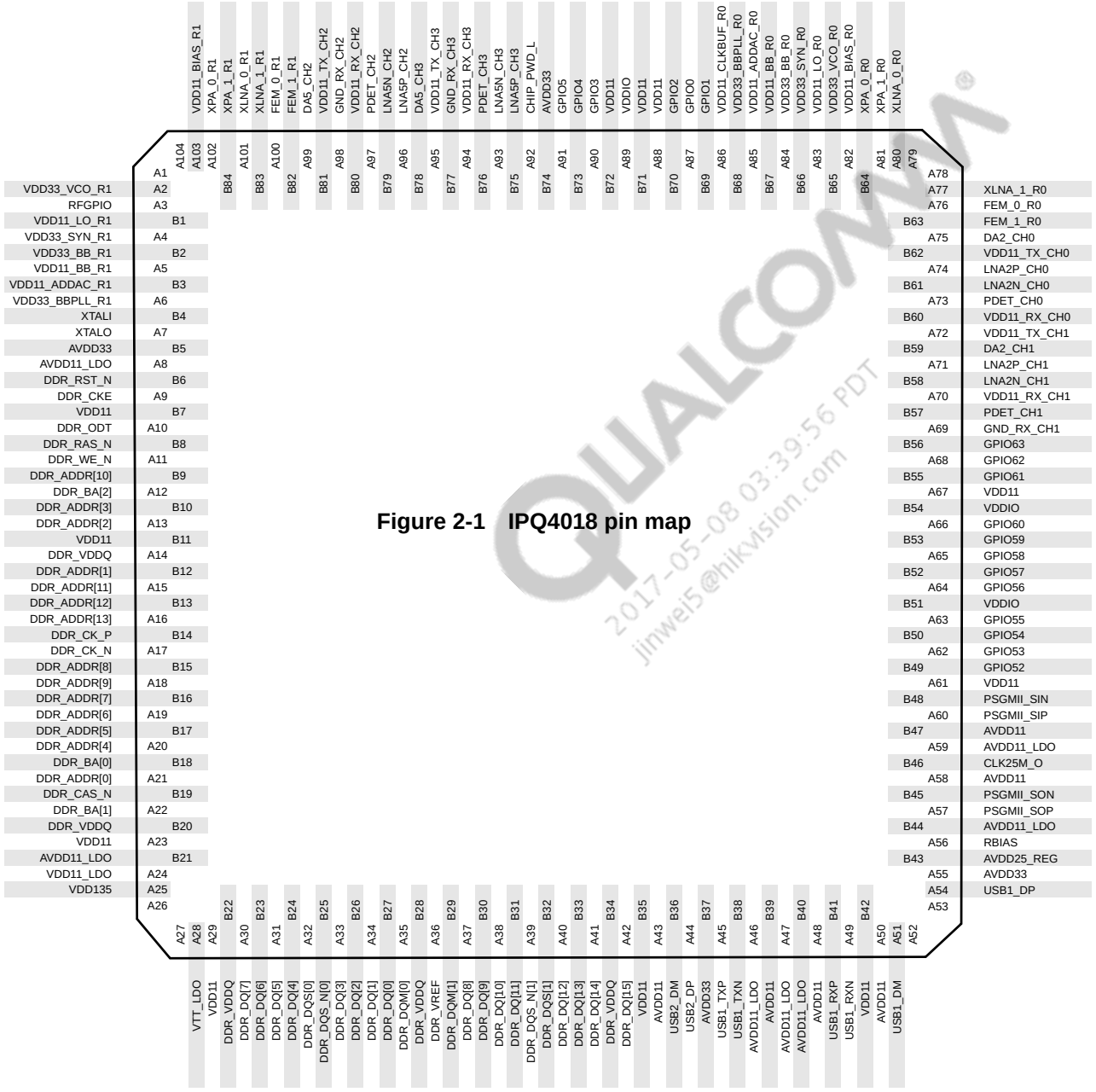


Figure 2-1 IPQ4018 pin map

2.2 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
AI	Analog input
AO	Analog output
GND	Ground
NC	Not connected; leave disconnected
RF IN	RF input
RF Out	RF output
I	Digital input signal
O	Digital output signal
IO	Digital bidirectional signal

2.3 Pin descriptions

Descriptions of pins are presented in the tables of this section. The pins are grouped by function.

2.3.1 Clock, power, and reset

Table 2-2 Clock, power, and reset

Pin ID	Pin name	Voltage	Type	Functional description
A43, A48, A50, A58, B39, B47	AVDD11	1.1	AI	1.1 V analog power
A8, A46, A47, A59, B21, B40, B44	AVDD11_LDO	1.1	AI	1.1 V analog power. Connect with pin A24 on board.
A55, B5, B37, B74	AVDD33	3.3	AI	3.3 V analog power
A23, A29, A61, A67, A88, B7, B11, B35, B42, B71, B72	VDD11	1.1	I	Digital power
A24	VDD11_LDO	1.1	O	1.1 V LDO output
A25	VDD135	1.35	I	Power input for VDD11_LDO and VTT_LDO. Route a dedicated wire from the 1.35 V switching regulator.
A89, B51, B54	VDDIO	3.3	I	Power for GPIO
A28	VTT_LDO	0.5 * VDD135	O	DDR termination voltage
B4	XTALI		I	Crystal oscillator input
A7	XTALO		O	Crystal oscillator output
A92	CHIP_PWD_L		I	Chip power-on reset.

2.3.2 5 GHz radio

In pin names and descriptions, “radio 1” or “R1” refers to the 5 GHz radio. “Channel 2”, “CH2”, “Channel 3”, and “CH3” are on the 5 GHz radio.

Table 2-3 5 GHz radio signals

Pin ID	Pin name	Voltage	Type	Functional description
B79 A96	LNA5N_CH2 LNA5P_CH2	1.1	IA	LNA differential input pair for chain 2
A93 B75	LNA5N_CH3 LNA5P_CH3	1.1	IA	LNA differential input pair for chain 3
A99	DA5_CH2	1.1	OA	DA single-ended output
B78	DA5_CH3			
A97	PDET_CH2	1.1	IA	PDET inputs
B76	PDET_CH3			
A102	XPA_0_R1		IO	External PA control
B84	XPA_1_R1			
A101	XLNA_0_R1		IO	External LNA control
B83	XLNA_1_R1			
A100	FEM_0_R1		IO	FEM control for CH0 of Radio 1
B82	FEM_1_R1			FEM control for CH1 of Radio 1

Table 2-4 5 GHz radio power and ground

Pin ID	Pin name	Voltage	Type	Functional description
A98	GND_RX_CH2		GND	
B77	GND_RX_CH3			
B3	VDD11_ADDAC_R1	1.1	I	1.1 V power supply for Radio 1
A5	VDD11_BB_R1			
A103	VDD11_BIAS_R1			
B1	VDD11_LO_R1			
B80	VDD11_RX_CH2			
A94	VDD11_RX_CH3			
B81	VDD11_TX_CH2			
A95	VDD11_TX_CH3			
A6	VDD33_BBPLL_R1	3.3	I	3.3 V power supply for Radio 1
B2	VDD33_BB_R1			
A4	VDD33_SYN_R1			
A2	VDD33_VCO_R1			

2.3.3 2 GHz radio

In pin names and descriptions, “radio 0” or “R0” refers to the 2 GHz radio. “Channel 0”, “CH0”, “Channel 1”, and “CH1” are on the 2 GHz radio.

Table 2-5 2 GHz radio signals

Pin ID	Pin name	Voltage	Type	Functional description
A74	LNA2P_CH0		IA	LNA differential input pair for chain 0
B61	LNA2N_CH0			
A71	LNA2P_CH1		IA	LNA differential input pair for chain 1
B58	LNA2N_CH1			
A75	DA2_CH0		OA	DA single-ended output
B59	DA2_CH1			
A73	PDET_CH0		IA	PDET inputs
B57	PDET_CH1			
B64	XPA_0_R0		OA	External PA control
A81	XPA_1_R0			
A80	XLNA_0_R0		O	External LNA control
A77	XLNA_1_R0			
A76	FEM_0_R0			FEM control for CH0 of Radio 0
B63	FEM_1_R0			FEM control for CH1 of Radio 0

Table 2-6 2 GHz radio power and ground

Pin ID	Pin name	Voltage	Type	Functional description
A69	GND_RX_CH1		GND	
A85	VDD11_ADDAC_R0	1.1	I	1.1 V power supply for Radio 0
B67	VDD11_BB_R0			
A82	VDD11_BIAS_R0			
A86	VDD11_CLKBUF_R0			
A83	VDD11_LO_R0			
B60	VDD11_RX_CH0			
A70	VDD11_RX_CH1			
B62	VDD11_TX_CH0			
A72	VDD11_TX_CH1			
B68	VDD33_BBPLL_R0	3.3	I	3.3 V power supply for Radio 0
A84	VDD33_BB_R0			
B66	VDD33_SYN_R0			
B65	VDD33_VCO_R0			

2.3.4 DDR3L

Table 2-7 16/8-bit DDR3L

Pin ID	Pin name	Voltage	Type	Functional description
A10	DDR_ODT			
B27	DDR_DQ[0]		I/O	DDR data[0:15]
A34	DDR_DQ[1]			
B26	DDR_DQ[2]			
A33	DDR_DQ[3]			
B24	DDR_DQ[4]			
A31	DDR_DQ[5]			
B23	DDR_DQ[6]			
A30	DDR_DQ[7]			
A37	DDR_DQ[8]			
B30	DDR_DQ[9]			
A38	DDR_DQ[10]			
B31	DDR_DQ[11]			
A40	DDR_DQ[12]			
B33	DDR_DQ[13]			
A41	DDR_DQ[14]			
A42	DDR_DQ[15]			
B14	DDR_CK_P		O	Differential clock (+)
A17	DDR_CK_N			Differential clock (-)
A9	DDR_CKE		O	Clock enable
B8	DDR_RAS_N			Chip select
B19	DDR_CAS_N			Chip select
A11	DDR_WE_N			Chip select
A35	DDR_DQM[0]			Data mask
B29	DDR_DQM[1]			
B18	DDR_BA[0]			Bank address
A22	DDR_BA[1]			
A12	DDR_BA[2]			

Table 2-7 16/8-bit DDR3L (cont.)

Pin ID	Pin name	Voltage	Type	Functional description
A21	DDR_ADDR[0]		O	DDR command/address[0:13]
B12	DDR_ADDR[1]			
A13	DDR_ADDR[2]			
B10	DDR_ADDR[3]			
A20	DDR_ADDR[4]			
B17	DDR_ADDR[5]			
A19	DDR_ADDR[6]			
B16	DDR_ADDR[7]			
B15	DDR_ADDR[8]			
A18	DDR_ADDR[9]			
B9	DDR_ADDR[10]			
A15	DDR_ADDR[11]			
B13	DDR_ADDR[12]			
A16	DDR_ADDR[13]			
A32	DDR_DQS[0]		I/O	Differential data strobe for byte 0 and 1 (+)
B32	DDR_DQS[1]			
B25	DDR_DQS_N[0]			Differential data strobe for byte 0 and 1 (-)
A39	DDR_DQS_N[1]			
B6	DDR_RST_N			Reset
A36	DDR_VREF	0.675	I	DDR Rx reference voltage input
A14, B20, B22, B28, B34	DDR_VDDQ	1.35	I	DDR I/O power

2.3.5 USB 3.0 and 2.0

Table 2-8 USB 3.0 signals

Pin ID	Pin name	Voltage	Type	Functional description
A54	USB1_DP		AI, AO	USB HS data positive
A51	USB1_DM		AI, AO	USB HS data negative
B41	USB1_RXP		AI	USB SS receive data positive
A49	USB1_RXN		AI	USB SS receive data negative
B38	USB1_TXN		AO	USB SS transmit data negative
A45	USB1_TXP		AO	USB SS transmit data positive

Table 2-9 USB 2.0 signals

Pin ID	Pin name	Voltage	Type	Functional description
A44	USB2_DP		AI, AO	USB HS data positive
B36	USB2_DM		AI, AO	USB HS data negative

2.3.6 Front-end

Table 2-10 Front-end

Pin ID	Pin name	Voltage	Type	Functional description
B43	AVDD25_REG	2.7	O	Power for pads and internal circuits
A56	RBIAS	1.175	O	Connect to an off-chip 5.9 K resistor to ground

2.3.7 PSGMII

Table 2-11 PSGMII

Pin ID	Pin name	Voltage	Type	Functional description
B46	CLK25M_O	1.1	O	Supply external PHY with 25 MHz clock
B45	PSGMII_SON	1.1	O	Differential negative output (6.25 Gbps in PSGMII mode)
A57	PSGMII_SOP	1.1	O	Differential positive output (6.25 Gbps in PSGMII mode)
B48	PSGMII_SIN	1.1	I	Differential negative input (6.25 Gbps in PSGMII mode)
A60	PSGMII_SIP	1.1	I	Differential positive input (6.25 Gbps in PSGMII mode)

2.3.8 GPIO interface

Individual GPIOs are configured by software using GPIO_CFGn registers corresponding to the GPIO number.

Table 2-12 GPIO

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
A87	GPIO0	0	GPIO	3.3		
		1	JTAG TDI[1]	3.3	I	JTAG test data in
		–				
B69	GPIO1	0	GPIO	3.3		
		1	JTAG TCK[1]	3.3	I	JTAG test clock
		–				
B70	GPIO2	0	GPIO	3.3		
		1	JTAG TMS[1]	3.3	IO	JTAG test mode state
		–				
A90	GPIO3	0	GPIO	3.3		
		1	JTAG TDO[1]	3.3	Z	JTAG test data out
			boot_config(0)	3.3	I	
B73	GPIO4	0	GPIO	3.3		
		1	JTAG RST_N[1]	3.3	I	JTAG reset for debug
A91	GPIO5	0	GPIO	3.3		
		1	JTAG TRST_N[1]	3.3	I	JTAG test reset
		–				
B49	GPIO52	0	GPIO	3.3		
		2	MDC	3.3	O	Management Data Clock
			boot_config(13)			
A62	GPIO53	0	GPIO	3.3		
		2	MDIO	3.3	I/O	Management Data I/O
B50	GPIO54	0	GPIO	3.3		
		2	blsp_spi0_ss0_n(1)	3.3	O	SPI0 chipselect 0
A63	GPIO55	0	GPIO	3.3		
		2	blsp_spi0_mosi(1)	3.3	O	SPI0 Master-out Slave-in data
			boot_config(9)	3.3	I	
A64	GPIO56	0	GPIO	3.3		
		2	blsp_spi0_sck(1)		O	SPI0 serial clock
			boot_config(10)	3.3	I	
B52	GPIO57	0	GPIO	3.3		

Table 2-12 GPIO (cont.)

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
		2	blsp_spi0_miso(1)		I	SPI0 Master-in Slave-out data
A65	GPIO58	0	GPIO	3.3		
		2	LED[2]	3.3	O	
		3	blsp_i2c0_sck(2)	3.3	IO	I^2C serial clock
		–				
		5	smart_ant6	3.3	IO	Smart antenna
B53	GPIO59	0	GPIO	3.3		
		2	blsp_i2c0_sda(2)	3.3	IO	I^2C serial data
		–				
		4	smart_ant7	3.3	IO	Smart antenna
A66	GPIO60	0	GPIO	3.3		
		2	blsp_uart0_rxd(1)	3.3	I	UART receive data
		–				
		4	smart_ant4	3.3	IO	Smart antenna
		5	LED[0]	3.3	O	
		6	audio_txbclk	3.3	IO	Audio transmit bit clock
		7	audio_rxbclk	3.3	IO	Audio receive bit clock
B55	GPIO61	0	GPIO	3.3		
		2	blsp_uart0_txd	3.3	O	UART transmit data
		–				
		4	smart_ant5	3.3	IO	Smart antenna
		5	audio_txfsync	3.3	IO	Audio transmit frame sync
		6	audio_rxfsync	3.3	IO	Audio receiver frame sync
		7	LED[1]	3.3	O	
			boot_config(14)	3.3	I	
A68	GPIO62	0	GPIO	3.3		
		2	Chip_rst_out	3.3	O	Chip reset signal
		3	Wifi0_uart_txd	3.3	O	Wifi0 UART transmit data
		4	Wifi1_uart_txd	3.3	O	Wifi1 UART transmit data
			boot_config(11)	3.3	I	

Table 2-12 GPIO (cont.)

Pin ID	Pin name	GPIO_CFG. FUNC_SEL	Configurable function	Voltage	Type	Functional description
B56	GPIO63	0	GPIO	3.3		
		2	Wifi0_uart_rxd	3.3	I	Wifi0 UART receive data
		3	Wifi1_uart_rxd	3.3	I	Wifi1 UART receive data
		4	Wifi1_uart_txd	3.3	O	Wifi1 UART transmit data
		5	Audio_txd[1]	3.3	O	Audio transmit data
		6	Audio_rxd	3.3	I	Audio receive data

1. Can also be activated by boot configuration.

2.3.9 Boot configuration

Several GPIO signals can be used to configure the secure boot feature and boot device. They are sampled only during power-on reset. Table 2-13 shows the boot configuration signals.

Table 2-13 Boot configuration

Pin #	Pin name BOOT_CONFIG[n]	Alternate function	Type	Functional description	
A64	10	GPIO56	I	Mode	
				0	Native mode
				1	Test mode
B49	13	GPIO52	I	Apps boot source	
				0	Boot from SPI NOR
				1	Boot from code RAM
A90	0	GPIO3	I	Apps authentication enable. Enables authentication for various AP code segments. Send to security control.	
				0	No authentication
				1	Enable authentication
A63	9	GPIO55	I	Force USB boot	
				0	Normal boot
				1	Force boot ROM USB interface. Send to security control.
A68	11	GPIO62	I	JTAG boot enable	
				0	GPIO0~GPIO5 are normal GPIOs; can be configured by the FUNC_SEL registers.
				1	GPIO0~GPIO5 are occupied by JTAG interface; cannot be changed by the FUNC_SEL registers.
B55	14	GPIO61	I	Watchdog disable. Only valid in native mode.	
				0	Watchdog enabled
				1	Watchdog disabled

3 Electrical Specifications

More specifications will be added in future revisions of this document as the data become available.

3.1 Absolute maximum ratings

Operating the IPQ4018 under conditions beyond its absolute maximum ratings (listed in Table 3-1) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, are not guaranteed or implied. Exposure may affect device reliability.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
T_J	Junction temperature	–	125	°C
T_{store}	Storage temperature	-45	135	°C

3.2 Recommended operating conditions

Operating conditions include parameters that are under the control of the user: power-supply voltage, ambient temperature, and case temperature. The IPQ4018 meets all performance specifications when used within the recommended operating conditions (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Recommended operating temperatures

Temperature	Description	Min	Typ	Max	Unit
T_{case}	Commercial case temperature	0	–	110	°C

Table 3-3 Recommended operating voltages

NOTE The maximum and minimum data are preliminary and are subject to change based on characterization results. Typical voltages are voltages at the pins of the package.

Pin	Description	Min	Typ[1]	Max	Unit
General					
AVDD11		1.05	1.1	1.15	V
VDD11		1.05	1.1	1.15	V
AVDD11_LDO		1.08	1.1	1.12	V
VDD135		1.28	1.35	1.42	V
DDR_VDDQ		1.28	1.35	1.42	V
AVDD33		3.13	3.3	3.46	V
VDDIO		3.13	3.3	3.46	V
VTT_LDO		0.5 * VDD135 ± 40			mV
DDR_Vref		0.5 * VDD135 ± 20			mV
5 GHz Radio					
VDD11_ADDAC_R1	1.1 V power supply for Radio 1	1.05	1.1	1.15	V
VDD11_BB_R1		1.05	1.1	1.15	V
VDD11_BIAS_R1		1.05	1.1	1.15	V
VDD11_LO_R1		1.05	1.1	1.15	V
VDD11_RX_CH2		1.05	1.1	1.15	V
VDD11_RX_CH3		1.05	1.1	1.15	V
VDD11_TX_CH2		1.05	1.1	1.15	V
VDD11_TX_CH3		1.05	1.1	1.15	V
VDD33_BBPLL_R1	3.3 V power supply for Radio 1	3.13	3.3	3.46	V
VDD33_BB_R1		3.13	3.3	3.46	V
VDD33_SYN_R1		3.13	3.3	3.46	V
VDD33_VCO_R1		3.13	3.3	3.46	V
2 GHz Radio					
VDD11_ADDAC_R0	1.1 V power supply for Radio 0	1.05	1.1	1.15	V
VDD11_BB_R0		1.05	1.1	1.15	V
VDD11_BIAS_R0		1.05	1.1	1.15	V
VDD11_CLKBUF_R0		1.05	1.1	1.15	V
VDD11_LO_R0		1.05	1.1	1.15	V
VDD11_RX_CH0		1.05	1.1	1.15	V
VDD11_RX_CH1		1.05	1.1	1.15	V
VDD11_TX_CH0		1.05	1.1	1.15	V
VDD11_TX_CH1		1.05	1.1	1.15	V

Table 3-3 Recommended operating voltages (cont.)

NOTE The maximum and minimum data are preliminary and are subject to change based on characterization results. Typical voltages are voltages at the pins of the package.

Pin	Description	Min	Typ[1]	Max	Unit
VDD33_BBPLL_R0	3.3 V power supply for Radio 0	3.13	3.3	3.46	V
VDD33_BB_R0		3.13	3.3	3.46	V
VDD33_SYN_R0		3.13	3.3	3.46	V
VDD33_VCO_R0		3.13	3.3	3.46	V

1. Typical voltages are voltages at the pins of the package.

3.2.1 Crystal

A 48-MHz crystal with accuracy of ±20 ppm may be used; for 5 MHz operation, ±10 ppm is required.

Table 3-4 Reference requirements for 48 MHz crystal

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	—	—	48	—	MHz
Frequency trimming	—	-10	—	10	PPM
Duty cycle of output signal	—	48	—	52	%
Voltage swing	—	0.8	—	1.5	Vpp
Settling time	—	—	—	1	ms
Output phase noise (48 MHz)	*f* = 1 KHz	—	-123.5	-121.5	dBc/Hz
	f = 10 KHz	—	-145.5	-143.5	dBc/Hz
	f = 100 KHz	—	-156.5	-154.5	dBc/Hz
	f = 1000 KHz	—	-157.5	-155.5	dBc/Hz
Output harmonic spur	—	—	—	-40	dBc
Mode of vibration	—	Fundamental			

3.3 Power sequencing

Power is supplied by external voltage regulators, which should be configured for the power-up sequence shown in Table 3-5. Any other supplies that are not critical to this power-up sequence, can be powered on by software after this sequence is completed.

Table 3-5 Power-on sequence

Step	Rails grouped by regulator	Voltage	Comments
1	AVDD33	3.3 V	3.3 V analog power
	VDDIO		Power for GPIO
	VDD33_BBPLL_R1, VDD33_BB_R1, VDD33_SYN_R1, VDD33_VCO_R1		3.3 V power supply for Radio 1
	VDD33_BBPLL_R0, VDD33_BB_R0, VDD33_SYN_R0, VDD33_VCO_R0		3.3 V power supply for Radio 0
2	VDD135	1.35 V	Power input for the VDD11 LDO and VTT LDO. Route a dedicated wire from the 1.35 V switching regulator.
	DDR_VDDQ		DDR I/O power
3	AVDD11	1.1 V	1.1 V analog power
	AVDD11_LDO		1.1 V analog power. Connect with pin A24 on board.
	VDD11		Digital power
	VDD11_LDO		1.1 V LDO output
	VDD11_ADDAC_R1, VDD11_BB_R1, VDD11_BIAS_R1, VDD11_LO_R1, VDD11_RX_CH2, VDD11_RX_CH3, VDD11_TX_CH2, VDD11_TX_CH3		1.1 V power supply for Radio 1
	VDD11_ADDAC_R0, VDD11_BB_R0, VDD11_BIAS_R0, VDD11_CLKBUF_R0, VDD11_LO_R0, VDD11_RX_CH0, VDD11_RX_CH1, VDD11_TX_CH0, VDD11_TX_CH1		1.1 V power supply for Radio 0

1. Within each step, no requirement for rail sequence.

3.4 Digital characteristics

Table 3-6 Digital I/O characteristics for 3.3 V IO

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage	CMOS/Schmitt	2	3.6	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.4	V
V_{SHYS}	Schmitt hysteresis voltage		–	–	mV
I_{IH}	Input high leakage current [1, 2]	No pulldown	–	1	µA
I_{IL}	Input low leakage current [1, 2]	No pullup	-1	–	µA
I_{IHPD}	Input high leakage current [1,3]	With pulldown	10	60	µA
I_{ILPU}	Input low leakage current [2, 3]	With pullup	-60	-10	µA
V_{OH}	High-level output voltage [4]	CMOS, at pin-rated drive strength	3.0	3.6	V
V_{OL}	Low-level output voltage [4]	CMOS, at pin-rated drive strength	-0.3	0.4	V
I_{OZH}	Tri-state leakage current [1]	Logic high output, no pulldown	–	1	µA
I_{OZL}	Tri-state leakage current [2]	Logic low output, no pullup	-1	–	µA
I_{OZHPD}	Tri-state leakage current [1, 3]	Logic high output with pulldown	10	60	µA
I_{OZLPU}	Tri-state leakage current [2, 3]	Logic low output with pullup	-60	-10	µA
C_{IN}	Input capacitance [5]		–	5	pF
I_{MAX}	GPIO drive strength [6]		2	5	mA

1. Pin voltage = VDDIO max. For keeper pins, pin voltage = VDDIO max - 0.45 V.
2. Pin voltage = GND and supply = VDDIO max. For keeper pins, pin voltage = 0.45 V and supply = VIO max.
3. Refer to Table 2-1 for pullup, pulldown, and keeper details.
4. Refer to Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable and depend on the associated supply voltage.
5. Input capacitance is guaranteed by design, but is not 100% tested.
6. GPIO drive strength can be configured by software.

Table 3-7 Digital I/O characteristics for DDR3 PAD

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage [1]	CMOS	1.05	1.65	V
V_{IL}	Low-level input voltage [1]	CMOS	-0.2	0.2	V
I_{IH}	Input high leakage current [2]	No pulldown	–	1	µA
I_{IL}	Input low leakage current [3]	No pullup	-1	–	µA
I_{IHPD}	Input high leakage current [2,4]	With pulldown	5	30	µA
I_{ILPU}	Input low leakage current [3, 4]	With pullup	-30	-5	µA
V_{OH}	High-level output voltage [5]	CMOS, at pin rated drive strength	1.2	1.5	V
V_{OL}	Low-level output voltage [5]	CMOS, at pin rated drive strength	-0.2	0.2	V
I_{OZH}	Tri-state leakage current	Logic high output	–	1	µA
I_{OZL}	Tri-state leakage current	Logic low output	-1	–	µA
C_{IN}	Input capacitance [6]		1	2	pF
$C_{I/O}$	I/O capacitance [6]	I/O, DQS, DQ, or clock pins	1.25	2.5	pF

1. V_{ref} = DDR_VDDQ.
2. Pin voltage = DDR_VDDQ. max.
3. Pin voltage = GND and supply = DDR_VDDQ. max.
4. Refer to Table 2-1 for pullup, pulldown, and keeper details.
5. Refer to Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable and depend on the associated supply voltage.
6. Input and I/O capacitances are guaranteed by design, but are not 100% tested.

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (see Figure 3-1) with respect to the drive current (see Table 2-1). They can be calculated using these relationships:

$$Vol[\max] = \frac{\%drive \times 450}{100} mV$$

$$Voh[\min] = Vdd\_px - \left(\frac{\%drive \times 450}{100}\right) mV$$

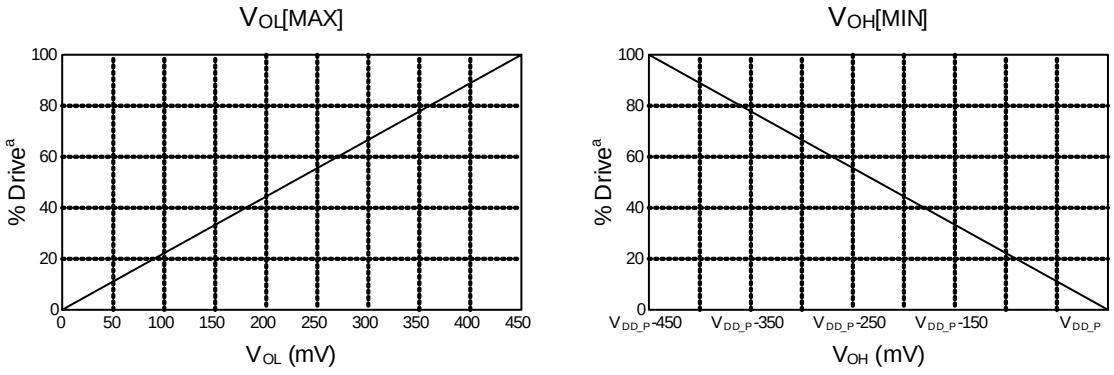


Figure 3-1 IV curve for V_{OL} and V_{OH} (valid for all V_{DD_PX})

3.5 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics are included here.

NOTE All IPQ4018 devices are characterized with actively terminated loads, so all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.5.2.

3.5.1 Timing diagram conventions

The conventions used throughout this document for timing diagrams are shown in Figure 3-2. For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown, the meaning depends on the signal.
- A single signal indicates *don't care*.
- In the case of bus activity, if both high and low levels are shown, this indicates that the processor or external interface is driving a value, but that this value may or may not be valid.

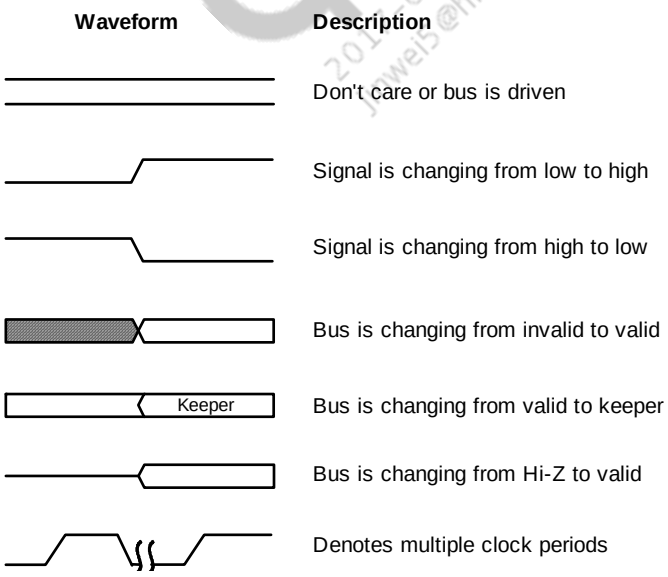


Figure 3-2 Timing diagram conventions

3.5.2 Rise and fall time specifications

The testers that characterize IPQ4018 have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions

have on rise and fall times is shown in Figure 3-3.

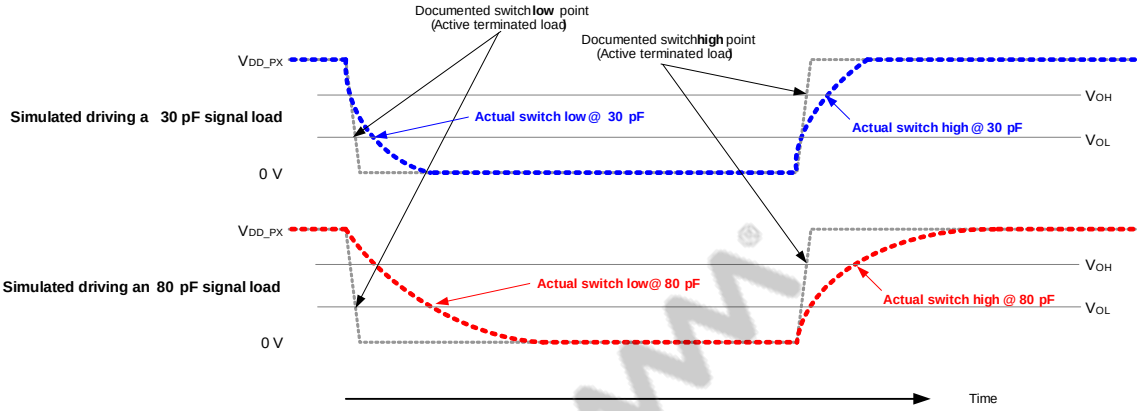


Figure 3-3 Rise and fall times under different load conditions

3.6 Memory support

3.6.1 DDR

All timing parameters in this document assume no bus loading. Rise/fall times must be factored into the numbers in this document. For example, setup times may get worse and hold times may get better.

Table 3-8 Summary of DDR support

Applicable standard	Feature exceptions	IPQ4018 variations
DDR3 SDRAM Specification JESD79-3A September 2007	None	None

3.6.1.1 Differential input cross point voltage

Make sure each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) meet the requirements in Table 3-9. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

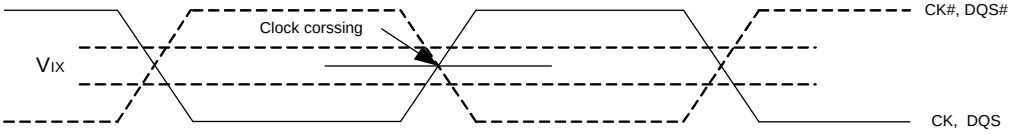


Figure 3-4 V_{IX} definition

Table 3-9 Cross point voltage for differential input signals (CK, DQS)

Parameter		Min	Typ	Max	Unit
1/t(ck)	PCDDR3L clock frequency	–	537.6	–	MHz
V_{IX}	Differential input cross-point voltage relative to VDD/2 for CK, CK#	-0.15		0.15	V

3.7 Connectivity

The connectivity functions supported by the IPQ4018 include:

- USB 3.0 and USB 2.0 ports
- Universal asynchronous receiver transmitter (UART) serial ports
- Inter-integrated circuit (I^2C) interfaces for peripheral devices
- Single channel I^2S interface for digital audio support
- Serial peripheral interface (SPI) ports
- Media-independent interface PSGMII

Pertinent specifications for these functions — where appropriate — are stated in the following subsections.

In addition to the following hardware specifications, consult the latest software release notes for software-based performance features or limitations.

3.7.1 USB interfaces

Table 3-10 Summary of USB support

Applicable standard	Feature exceptions	IPQ4018 variations
Universal Serial Bus Specification, Revision 3.0	None	None
Universal Serial Bus Specification, Revision 2.0	None	For operating voltages, system clock, and VBUS – see Table 3-3

3.7.2 High-speed UART interface

Table 3-11 Summary of UART support

Applicable standard	Feature exceptions	IPQ4018 variations
EIA RS232-C	None	None

3.7.3 I²C interface

Table 3-12 Summary of I²C support

Feature exceptions	IPQ4018 variations
■ High-speed mode (3.4 Mbps) is not supported. ■ 10-bit addressing is not supported. ■ Fast mode plus (1 Mbps) is not supported.	None

3.7.4 I²S interface

The IPQ4018 supports multichannel I²S. The I²Si interface meet the timing given in this section.

Table 3-13 Supported I²S standards and exceptions

Applicable standard	Feature exceptions	IPQ4018 variations
Philips Semiconductor, *I²S Bus Specification*, revised June 5, 1996		The IPQ4018 meets or exceeds this standard. The only exception is the IPQ4018 requires a 45/55 duty cycle when the SCK clock source is from an external source.

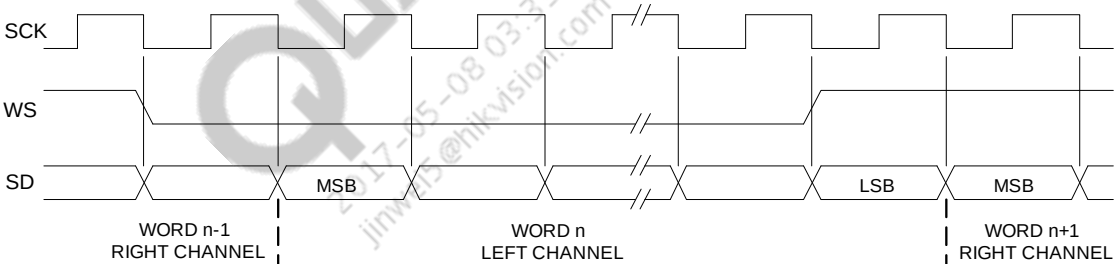


Figure 3-5 I²S interface basic timing

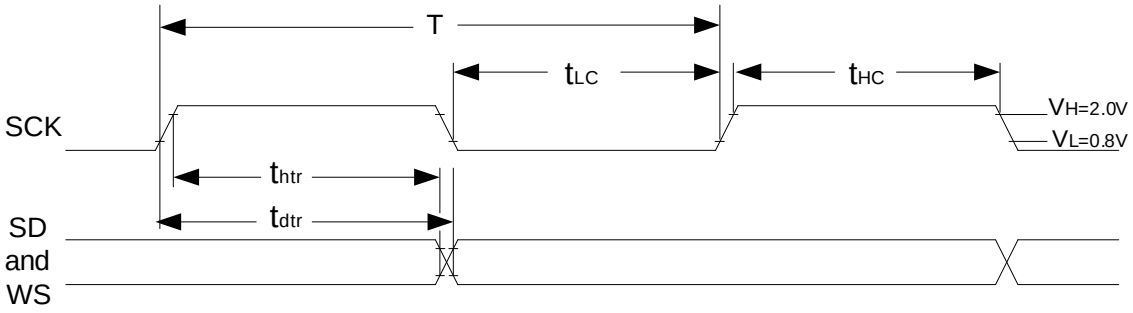


Figure 3-6 I²S interface transmitter timing

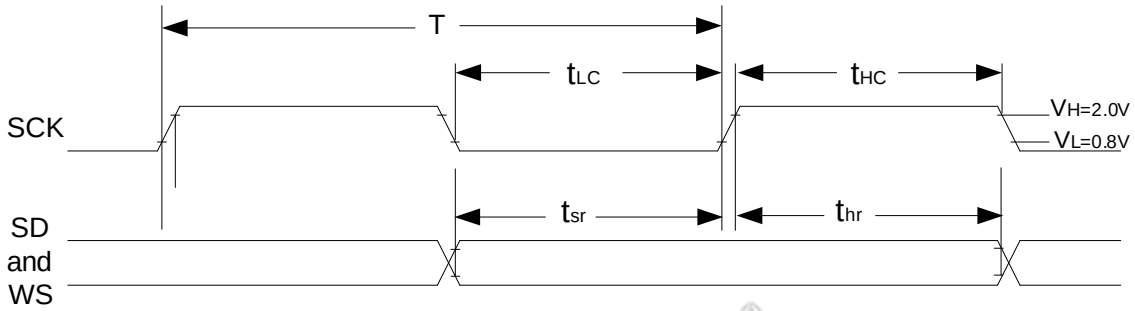


Figure 3-7 I²S interface receiver timing

Table 3-14 I²S interface timing using internal SCK clock

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Clock SCK						
Frequency	f	0		6.144	MHz	C_L = 10 pF
Clock period	T	0		162.76	ns	C_L = 10 pF
Clock high	t_{HC}	0.45T		0.55T	ns	C_L = 10 pF
Clock low	t_{LC}	0.45T		0.55T	ns	C_L = 10 pF
Inputs SD*, WS						
Setup time	t_{sr}	0.2T	–	–	ns	
Hold time	t_{hr}	0	–	–	ns	
Outputs SD*, WS						
Delay	t_{dtr}	–	–	0.8T	ns	C_L = 10 pF
Hold time	t_{htr}	0	–	–	ns	C_L = 10 pF

Table 3-15 I²S interface timing using external SCK clock

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Clock SCK						
Frequency	f	0		6.144	MHz	C_L = 10 pF
Clock period	T	0		162.76	ns	C_L = 10 pF
Clock high	t_{HC}	0.45T		0.55T	ns	C_L = 10 pF
Clock low	t_{LC}	0.45T		0.55T	ns	C_L = 10 pF
Inputs SD*, WS						
Setup time	t_{sr}	0.2T	–	–	ns	
Hold time	t_{hr}	0	–	–	ns	
Outputs SD*, WS						
Delay	t_{dtr}	–	–	0.8T	ns	C_L = 10 pF
Hold time	t_{htr}	0	–	–	ns	C_L = 10 pF

3.7.5 Serial peripheral interface (master only)

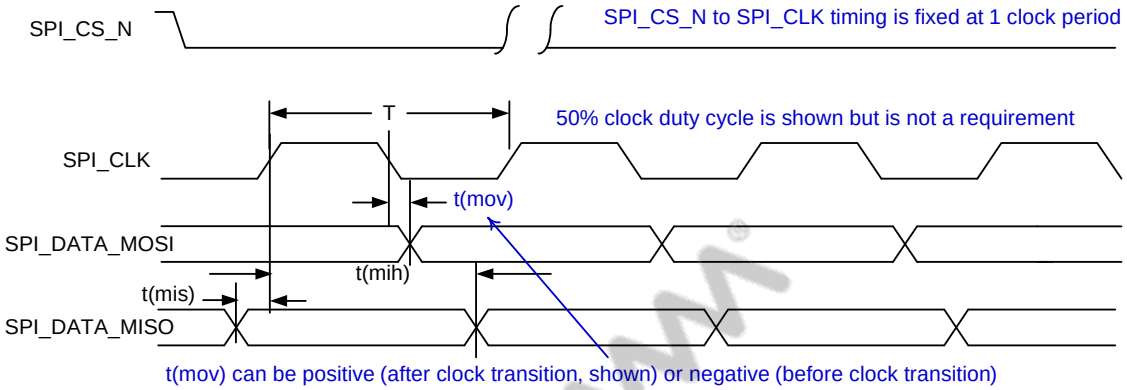


Figure 3-8 SPI master timing diagram

Table 3-16 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
SPI clock frequency		–	–	25	MHz
T (SPI clock period)		40	–	–	ns
t(ch)	Clock high	18	–	–	ns
t(cl)	Clock low	18	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

3.7.6 PSGMII Interface

Table 3-17 PSGMII transmit DC electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_BAUD	Transmit baud rate	–	6.250	–	Gbps
T_VDIFF[1]	Output differential voltage (into the load Rload=100Ω)	300	600	900	mVppd
T_Rs	Single-ended termination resistance	40	50	60	Ω
T_Vcm[2]	Output common mode voltage	0.6	0.8	1.05	V

1. The default value is 600 mVppd, and can be adjusted from 300 to 900 mVppd by register configuration.
2. The output common mode voltage changes accordingly if T_VDIFF is adjusted. It is also affected by supply voltage which is assumed 1.1 V+100mV/-50mV.

Table 3-18 PSGMII receive DC electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R_BAUD	Receive baud rate	–	6.250	–	Gbps
R_VDIFF	Input differential voltage	100	–	1600[2]	mVppd
R_Rs	Single-ended termination resistance	40	50	60	Ω
R_Vcm[1]	Input common mode voltage	1.05	1.1	1.2	V

1. The input common mode voltage is affected by supply voltage which is assumed 1.1 V+100mV/-50mV.
2. The maximum differential voltage the receiver can tolerate.

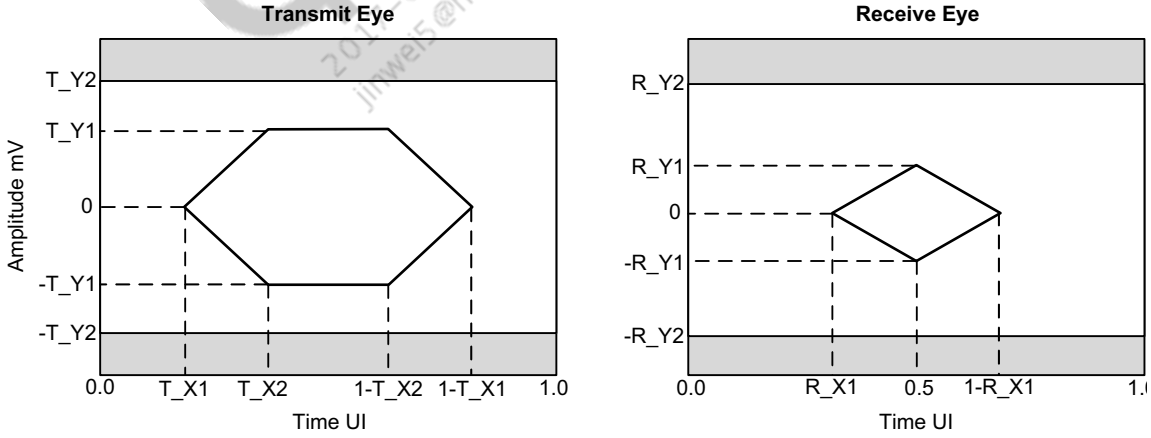


Figure 3-9 PSGMII jitter eye diagrams

Table 3-19 PSGMII transmit jitter specifications

Symbol	Parameter	Min	Typ	Max	Unit
T_UHPJ[1]	Uncorrelated high-probability jitter	–	–	0.15	UIpp
T_DCD	Duty cycle distortion	–	–	0.05	UIpp
T_Tj	Total jitter	–	–	0.30	UIpp
T_X1	Eye mask	–	–	0.15	UI
T_X2	Eye mask	–	–	0.40	UI
T_Y1	Eye mask	200	–	–	mV
T_Y2	Eye mask	–	–	450	mV

1. DJ component; no correlation to any signal level being transmitted.

Table 3-20 PSGMII receive jitter specifications

Symbol	Parameter	Min	Typ	Max	Unit
R_BHPJ[1]	Bounded high-probability jitter	–	–	0.45	UIpp
R_SJ_hf	Sinusoidal jitter, high frequency	–	–	0.05	UIpp
R_TJ	Total jitter (sinusoidal jitter not included)	–	–	0.60	UIpp
R_X1	Eye mask	–	–	0.30	UI
R_Y1	Eye mask	50	–	-	mV
R_Y2	Eye mask	–	–	450	mV

1. The sum of uncorrelated, bounded, high-probability jitter (UBHPJ, 0.15UI) and correlated, bounded, high-probability jitter (CBHPJ, 0.3UI). UBHPJ shows no correlation to any signal level being transmitted. CBHPJ shows a strong correlation to the signal level being transmitted, so can be considered equalizable.

3.8 Radio characteristics

These conditions apply to the typical per chain characteristics unless otherwise specified:

V_{DD11} = 1.1 V
V_{DD33} = 3.3 V, T_a = 25 °C

3.8.1 Rx characteristics

Table 3-21 Rx characteristics for 2.4 GHz operation

Symbol	Parameter			Min	Typ	Max	Unit	Conditions
Frx	Receive input frequency range			2.412	—	2.484	GHz	5 MHz center frequency
Sensitivity								
Srf (CCK)	CCK	1 Rx Chain	1 Mbps	—	-97	—	dBm	See Note 1
			11 Mbps	—	-95	—		
	CCK	2 Rx Chains	1 Mbps	—	-100	—	dBm	
			11 Mbps	—	-98	—		
Srf (OFDM)	OFDM	1 Rx Chain	6 Mbps	—	-92.5	—	dBm	See Note 1
			54 Mbps	—	-75	—		
	OFDM	2 Rx Chains	6 Mbps	—	-94.5	—	dBm	
			54 Mbps	—	-78	—		
Srf (802.11ac)	802.11ac VHT20	1 Stream (1x1)	MCS0	—	-92	—	dBm	—
			MCS8	—	-67	—		
	802.11ac VHT20	2 Streams (2x2)	MCS0	—	-91	—	dBm	
			MCS8	—	-66	—		
	802.11ac VHT40	1 Stream (1x1)	MCS0	—	-89.5	—	dBm	—
			MCS9	—	-65	—		
	802.11ac VHT40	2 Streams (2x2)	MCS0	—	-88.5	—	dBm	
			MCS9	—	-64	—		
Z_{RFin_input}	Recommended LNA differential drive impedance			—	2450 MHz Impedance 167-163j	—	Ω	Ch 0, Ch 1
Adjacent channel rejection								
R_{adj}	CCK			35	41.5	—	dB	See Note 2
	OFDM		6 Mbps	16	31	—		
			54 Mbps	-1	15	—		
	VHT20		1 Stream MCS0	16	28	—		
			2 Streams MCS8	-7	6	—		
	VHT40		1 Stream MCS0	16	24	—		
			2 Streams MCS9	-9	1	—		

1. VDD11 = A23, A29, A61, A67, A88, B7, B11, B35, B42, B71, B72
2. Measured with reference design AP.DK01 at RF input with NF = 5.0 dB. Minimum values based on IEEE 802.11 requirements. Tested with chain mask 3. Additional ±1.5 dB board-to-board variation must be accounted.

Table 3-22 Rx characteristics for 5 GHz operation

Symbol	Parameter			Min	Typ	Max	Unit	Conditions
Frx	Receive input frequency range			5.18	—	5.905	GHz	5 MHz center frequency
Sensitivity								
Srf (802.11a)	1 Stream (1x1)	1 Rx Chain	6 Mbps	—	-90	—	dBm	See Note 1
			54 Mbps	—	-75	—		
	2 Streams (2x2)	2 Rx Chains	6 Mbps	—	-93	—	dBm	
			54 Mbps	—	-78	—		
Srf (802.11ac)	802.11ac VHT20	1 Stream (1x1)	MCS0	—	-87	—	dBm	See Note 1
			MCS7	—	-70.5	—		
			MCS8	—	-67	—		
	802.11ac VHT40		MCS0	—	-85	—	dBm	
			MCS7	—	-68.5	—		
			MCS9	—	-61.5	—		
	802.11ac VHT80		MCS0	—	-82	—	dBm	
			MCS7	—	-65	—		
			MCS9	—	-58.5	—		
	802.11ac VHT20	2 Streams (2x2)	MCS0	—	-86	—	dBm	See Note 1
			MCS7	—	-69.5	—		
			MCS8	—	-66	—		
	802.11ac VHT40		MCS0	—	-84	—	dBm	
			MCS7	—	-67.5	—		
			MCS9	—	-60.5	—		
	802.11ac VHT80		MCS0	—	-81	—	dBm	
			MCS7	—	-64	—		
			MCS9	—	-57.5	—		
Z_{RFin_input}	Recommended LNA differential drive impedance			—	5500 MHz impedance 27 + 100j	—	Ω	Ch 0, Ch 1,
Adjacent channel rejection								
R_{adj}	802.11a OFDM (4x4)		6 Mbps	16	25	—	dB	See Note 1
			54 Mbps	-1	10	—		
	VHT20	1 Stream	MCS0	16	23	—	dB	See Note 1
		2 Streams	MCS8	-7	1	—		
	VHT40	1 Stream	MCS0	16	25	—	dB	See Note 1
		2 Streams	MCS9	-9	1	—		
	VHT80	1 Stream	MCS0	16	24	—	dB	See Note 1
		2 Streams	MCS9	-9	1	—		

Table 3-22 Rx characteristics for 5 GHz operation (cont.)

Symbol	Parameter			Min	Typ	Max	Unit	Conditions
Alternate channel rejection								
R_{alt}	802.11a OFDM		6 Mbps	32	36	—	dB	See Note 1
			54 Mbps	15	19	—		
	VHT20	1 Stream	MCS0	32	36	—	dB	See Note 1
		2 Streams	MCS8	9	13	—		
	VHT40	1 Stream	MCS0	32	32	—	dB	See Note 1
		2 Streams	MCS9	7	7	—		
	VHT80	1 Stream	MCS0	32	32	—	dB	See Note 1
		2 Streams	MCS9	7	10	—		

1. Simulated at chip input with an NF = 5.8 dB.Tested with chain mask 3. Additional ±1.5 dB board-to-board variation must be accounted.

3.8.2 Tx Characteristics

Table 3-23 Tx chain characteristics for 2.4 GHz operation at chip output with external PA

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
F_{tx}	Transmit output frequency range		2.421	—	2.484	GHz	5 MHz center freq
P_{out}	Mask compliant output power						
	1 Mbps		—	-3	—	dBm	See Note[1]
	6 Mbps		—	-3	—		
	HT20, MCS0		—	-3	—		
	HT40, MCS0		—	-3	—		
EVM (Header Only)			**Tx Power (dBm)[2]:**				
	802.11ac, VHT20 (Per Tx chain)	MCS8	—	-40	—	dB	Tx power < -6.5 dBm See Note[1]
	802.11ac, VHT40 (Per Tx chain)	MCS9	—	-39.5	—	dB	Tx power < -6.5 dBm See Note[1]
SP_{gain}	Tx gain step		—	0.5	—	dB	See Note[2]
A_{pl}	Accuracy of power control loop		—	±1.5	—	dB	See Note[3]
Z_{RFout_load}	Recommended PA single-ended load impedance		—	50	—	Ω	—

1. Simulated at the chip output
2. Guaranteed by design.
3. Manufacturing calibration required.

Table 3-24 Tx chain characteristics for 5 GHz operation at chip output with external PA

Symbol	Parameter			Min	Typ	Max	Unit	Conditions
F_{tx}	Transmit output frequency range			5.18	—	5.905	GHz	20 MHz center frequency
P_{out}	Mask compliant output power							
	6 Mbps			—	-1.6	—	dBm	See Note[1]
	VHT20, MCS0			—	-1.6	—		
	VHT40, MCS0			—	-1.6	—		
	VHT80, MCS0			—	-1.6	—		
EVM (Header Only) (Per Tx Chain)				**Tx Power (dBm)[2]:**				
	802.11ac	VHT20	MCS8	—	-39.5	—	dB	Tx power < -6.5 dBm See Note[1]
	802.11ac	VHT40	MCS9	—	-39.5	—	dB	Tx power < -9.5 dBm See Note[1]
	802.11ac	VHT80	MCS9	—	-39.5	—	dB	Tx power < -10.5 dBm See Note[1]
SP_{gain}	Tx gain step			—	0.5	—	dB	See Note[2]
A_{pl}	Accuracy of power control loop			—	±1.5	—	dB	See Note[3]
Z_{RFout_load}	Recommended PA single-ended load impedance			—	50	—	Ω	—
SS	Sideband suppression			—	-48	—	dBc	—

1. Simulated at the chip output
2. Guaranteed by design.
3. Manufacturing calibration required.

3.9 Power consumption

This section shows the typical power consumption with external PMU as a function of the IPQ4018's operating mode. See Note [1].

Table 3-25 802.11ac power consumption for 2.4 GHz (VHT20)

Mode	AVDD33 (mA)	AVDD11 (mA)	DVDD11 (mA)	VDDR1.35 (mA)	Power consumption (W)
Rx (two chains) MCS0	281	300	790	376	2.633
Rx (two chains) MCS8	279	325	819	412	2.735
Tx (two chains) MCS0	279	413	866	358	2.810
Tx (two chains) MCS8	280	398	842	380	2.801

Table 3-26 802.11ac power consumption for 2.4 GHz (VHT40)

Mode	AVDD33 (mA)	AVDD11 (mA)	DVDD11 (mA)	VDDR1.35 (mA)	Power consumption (W)
Rx (two chains) MCS0	280	309	830	360	2.662
Rx (two chains) MCS9	274	307	900	410	2.785
Tx (two chains) MCS0	279	440	905	357	2.882
Tx (two chains) MCS9	276	400	910	398	2.889

Table 3-27 802.11ac power consumption for 5 GHz (VHT20)

Mode	AVDD33 (mA)	AVDD11 (mA)	DVDD11 (mA)	VDDR1.35 (mA)	Power consumption (W)
Rx (two chains) MCS0	289	274	762	371	2.594
Rx (two chains) MCS 8	284	265	707	385	2.596
Tx (two chains) MCS0	280	365	860	357	2.753
Tx (two chains) MCS8	278	366	864	384	2.788

Table 3-28 802.11ac power consumption for 5 GHz (VHT40)

Mode	AVDD33 (mA)	AVDD11 (mA)	DVDD11 (mA)	VDDR1.35 (mA)	Power consumption (W)
Rx (two chains) MCS0	286	282	795	372	2.630
Rx (two chains) MCS9	286	267	875	410	2.753
Tx (two chains) MCS0	278	364	893	363	2.790
Tx (two chains) MCS9	280	357	896	402	2.845

1. 2.4 GHz and 5 GHz measured with AP.DK01 reference design.

Table 3-29 802.11ac power consumption for 5 GHz (VHT80)

Mode	AVDD33 (mA)	AVDD11 (mA)	DVDD11 (mA)	VDDR1.35 (mA)	Power consumption (W)
Rx (two chains) MCS0	279	303	870	373	2.714
Rx (two chains) MCS9	286	295	990	440	2.951
Tx (two chains) MCS0	274	356	990	430	2.965
Tx (two chains) MCS9	278	373	998	431	3.007

Table 3-30 802.11ac power consumption for 2.4 GHz (VHT40) + 5 GHz (VHT80)

Mode	AVDD33 (mA)	AVDD11 (mA)	DVDD11 (mA)	VDDR1.35 (mA)	Power consumption (W)
Rx (two chains) MCS0	307	315	920	380	2.884
Rx (two chains) MCS9	296	302	1060	480	3.123
Tx (two chains) MCS0	278	531	1070	370	3.178
Tx (two chains) MCS9	272	490	1139	459	3.309

4 Mechanical Information

The IPQ4018 uses 180-pin dual-row quad-flat no-leads (180DRQFN) package technology (see Figure 4-1).

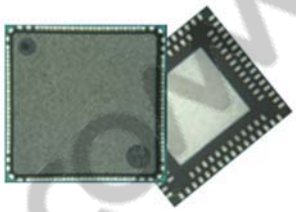


Figure 4-1 DRQFN package illustration

4.1 Device physical dimensions

Figure 4-2 shows the package drawing and Table 4-1 shows the dimensions for package A.
Figure 4-3 shows the package drawing and Table 4-2 shows the dimensions for package A.

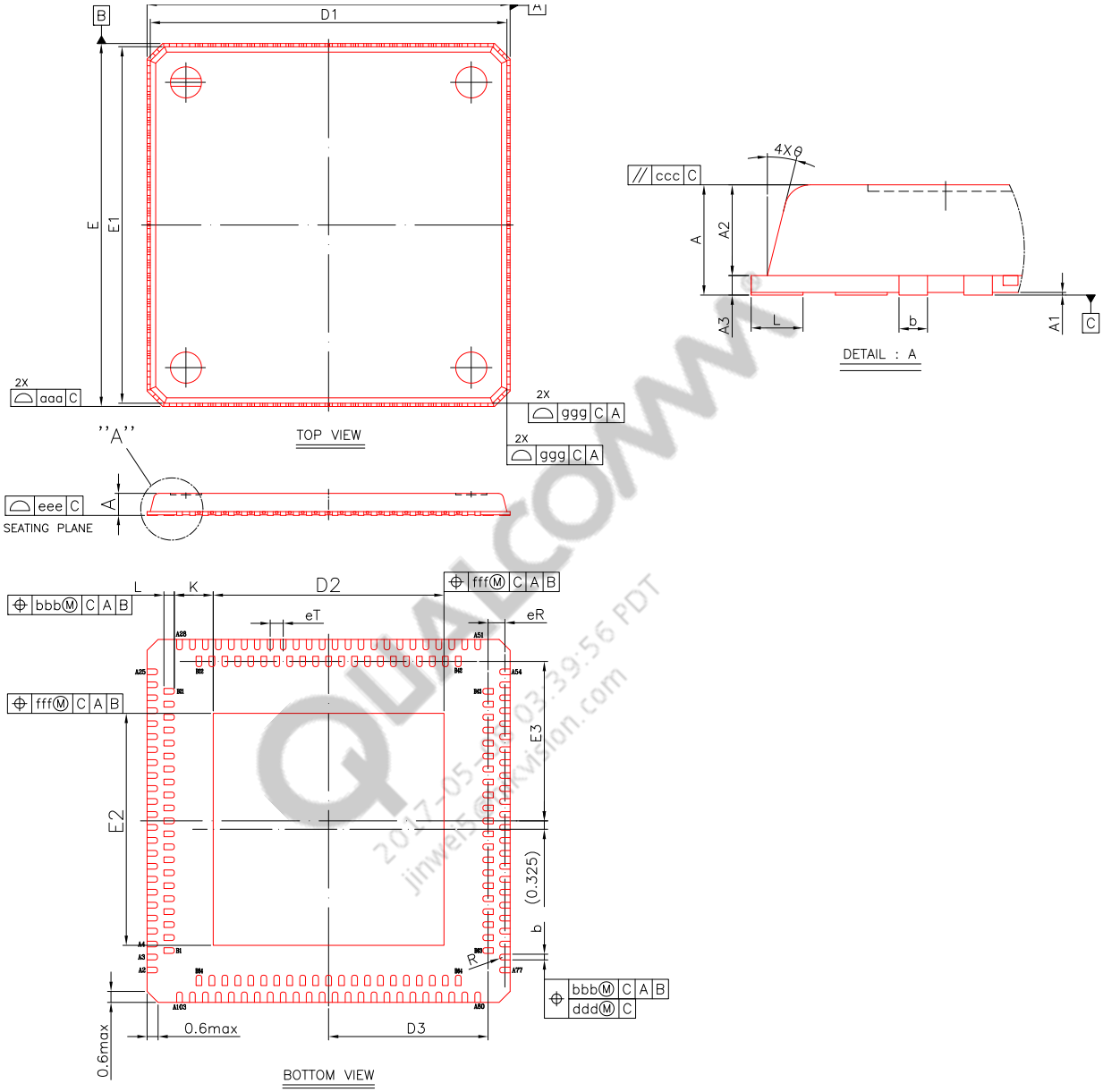


Figure 4-2 IPQ4018 180DRQFN package A details

Table 4-1 IPQ4018 180DRQFN package A dimensions

Dimension Label	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm
A1	0.00	0.02	0.05	mm
A2	0.65	0.70	0.75	mm
A3		0.15 REF		mm
b	0.18	0.22	0.30	mm
D/E	13.90	14.00	14.10	mm
D1/E1		13.75 BSC		mm
D2	8.80	8.90	9.00	mm
E2	8.85	8.95	9.05	mm
D3/E3		6.15 BSC		mm
eT		0.50 BSC		mm
eR		0.65 BSC		mm
L	0.30	0.40	0.50	mm
θ	5	---	15	°
K	0.20	---	---	mm
R	0.09	---		mm
aaa		0.10		mm
bbb		0.10		mm
ccc		0.10		mm
ddd		0.05		mm
eee		0.08		mm
fff		0.10		mm
ggg		0.20		mm

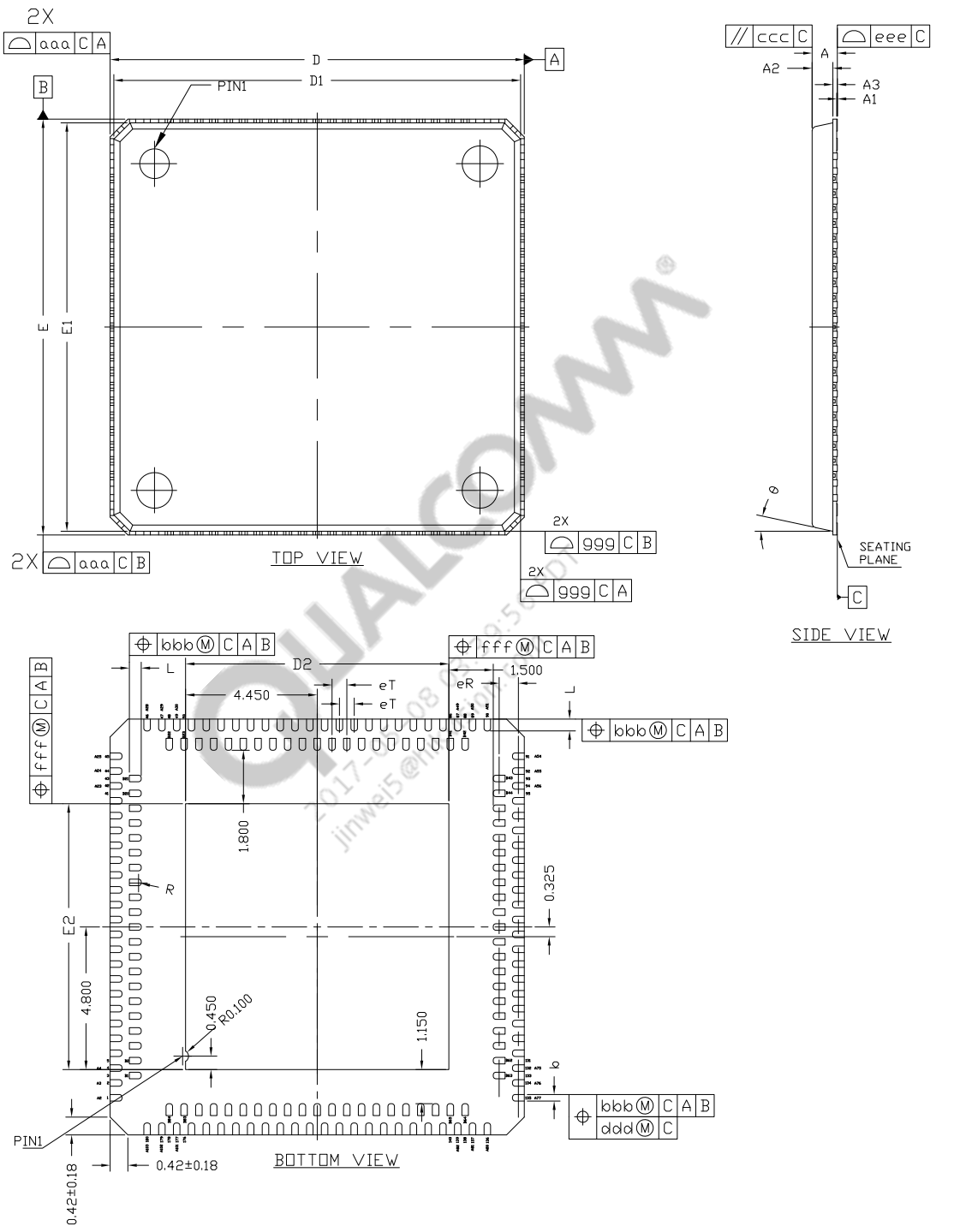


Figure 4-3 IPQ4018 180DRQFN package B details

Table 4-2 IPQ4018 180DRQFN package B dimensions

Dimension Label	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm
A1	0.00	0.02	0.05	mm
A2	0.65	0.70	0.75	mm
A3		0.15 REF		mm
b	0.18	0.22	0.30	mm
D/E	13.90	14.00	14.10	mm
D1/E1		13.75 BSC		mm
D2	8.80	8.90	9.00	mm
E2	8.85	8.95	9.05	mm
eT		0.50 BSC		mm
eR		0.65 BSC		mm
L	0.30	0.40	0.50	mm
θ	5	---	15	°
R	0.09	---		mm
aaa		0.10		mm
bbb		0.10		mm
ccc		0.10		mm
ddd		0.05		mm
eee		0.08		mm
fff		0.10		mm
ggg		0.20		mm

4.2 Part marking

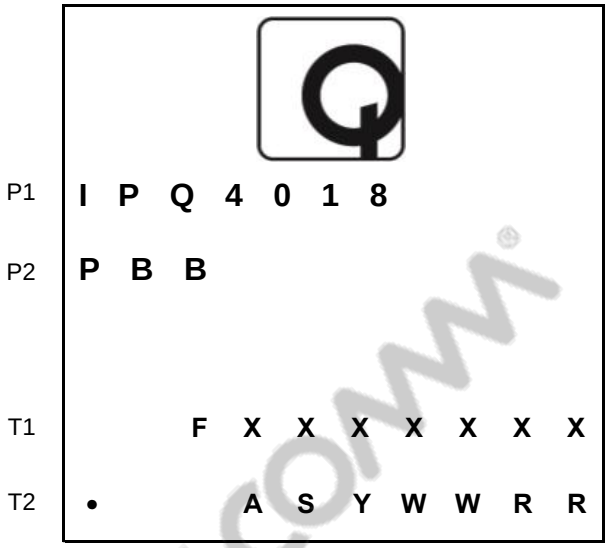


Figure 4-4 IPQ4018 marking (top view, not to scale)

Table 4-3 IPQ4018 marking line definitions

Line	Marking	Description
P1	IPQ4018	Product name
P2	PBB	P: product configuration code = 0 BB: feature code = VV
T1	FXXXXXXX	F: fab code XXXXXXX = lot number
T2	ASYWWRR	A: assembly site code S: assembly sequence number Y: single, last digit of year WW: work week (based on calendar year) RR: revision code

4.3 Device ordering information

Order numbers have the form shown in Figure 4-5.

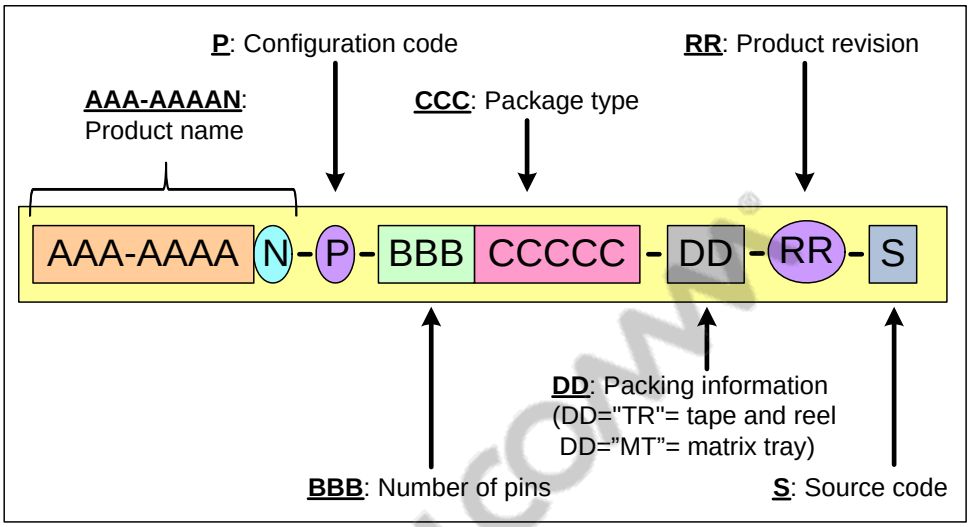


Figure 4-5 Device identification code

Table 4-4 shows the available order numbers.

Table 4-4 IPQ4018 order numbers

PRR	Order number	Description
000	IPQ-4018-0-180DRQFN-MT-00-0	RoHS & BrCl-free, C-Temp
000	IPQ-4018-0-180DRQFN-TR-00-0	RoHS & BrCl-free, C-Temp

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. Qualcomm follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. The IPQ4018 is classified as MSL3; the qualification temperature was 250ºC.

4.5 Thermal characteristics

Thermal data at 3.3 W; typical power is 2.7 W.

Table 4-5 Thermal resistance

Parameter		Comment	Typical	Unit
θ_{JA}	Junction-to-Ambient	■ Jedec JESD51-2A ■ Jedec JESD51-7	19.3	°C/W
θ_{JB}	Junction-to-Board	■ Jedec JESD51-7 ■ Jedec JESD51-8 ■ Cold plate ring maintained at 25°C at top and bottom of PCB	13.3	°C/W
θ_{JC}	Junction-to-Case	■ No thermal vias ■ Jedec JESD51-7 ■ Jedec JESD51-8 ■ Cu block at top of package maintained at 25°C	4.5	°C/W
Ψ_{JT}	Junction-to-Top	■ Jedec JESD51-2A ■ Jedec JESD51-7	0.18	°C/W

5 Carrier, Storage, and Handling

5.1 Carrier

5.1.1 Tape and reel information

The carrier tape system conforms to EIA-481 standards.

Simplified sketches of the IPQ4018 tape carrier are shown in Figure 5-1 and Figure 5-2, including the part orientation. Tape and reel details for the IPQ4018 are as follows:

- Reel diameter: 330 mm
- Hub size: 178 mm
- Tape width: 24 mm
- Tape pocket pitch: 20 mm
- Feed: Single
- Units per reel: 2000

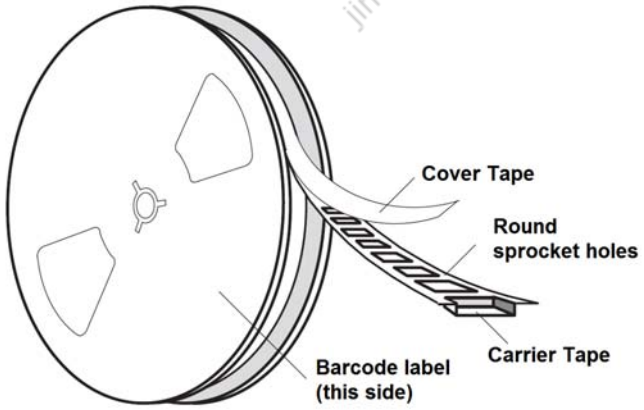


Figure 5-1 Tape orientation on reel

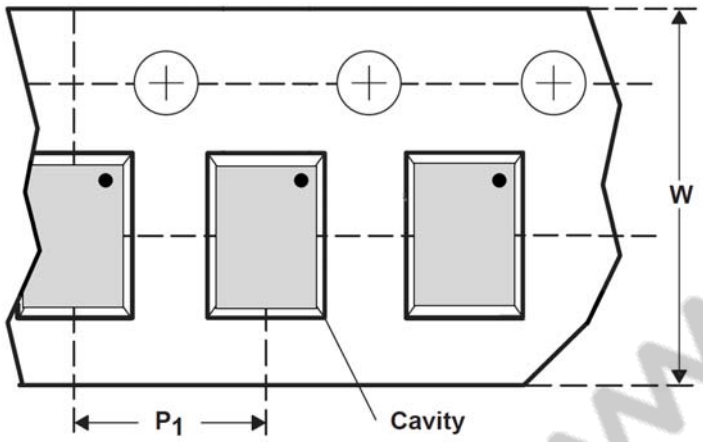
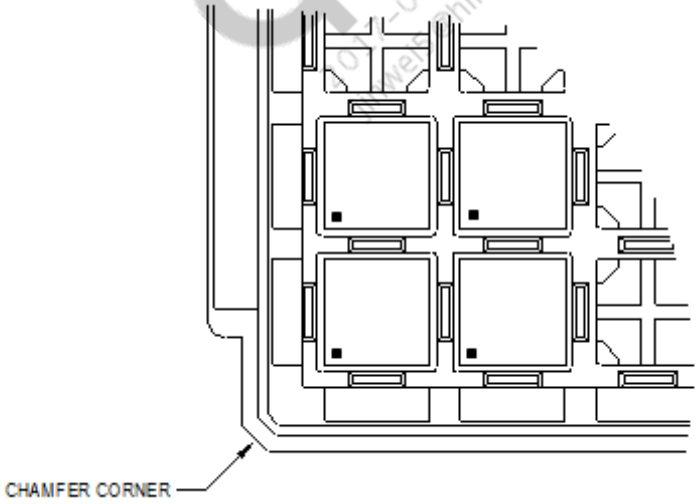


Figure 5-2 Part orientation in tape

5.1.2 Matrix tray information

Matrix tray carriers confirm to JEDEC standards. The device pin 1 is oriented to the chamfered corner of the matrix tray. Each tray of IPQ4018 contains up to 152 devices. See Figure 5-3 for matrix-tray key attributes and dimensions.



Key dimensions	
Array	8 × 19 = 152
M	10.55 mm
M1	10.80 mm
M2	16.30 mm
M3	16.40 mm

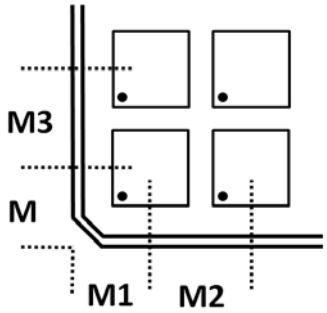


Figure 5-3 Matrix tray part orientation

5.2 Storage

5.2.1 Bagged storage conditions

IPQ4018 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling is described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

It is **not necessary** to bake the IPQ4018 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the IPQ4018 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see *ASIC Packing Methods and Materials Specification* (80-VK055-1) for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Barcode label and packing for shipment

Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

6 PCB Mounting Guidelines

Guidelines for mounting the IPQ4018 device onto a PCB are presented in this chapter, including land pad and stencil design details, surface mount technology (SMT) process characterization, and SMT process verification.

6.1 RoHS compliance

The IPQ4018 device is externally lead-free and RoHS-compliant. Qualcomm defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products.

6.2 SMT parameters

This section describes board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

Qualcomm recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil-pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability. Review the land pattern and stencil pattern design recommendations as a guide for characterization:

PCB Land and Stencil Design Guide (LS90-NG134-1).

6.2.2 Reflow profile

Reflow profile conditions typically used by Qualcomm for lead-free systems are listed in Table 6-1 and are shown in Figure 6-1.

Table 6-1 Typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Dry-out and flux activation	150 to 190°C	60 to 120sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C. This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

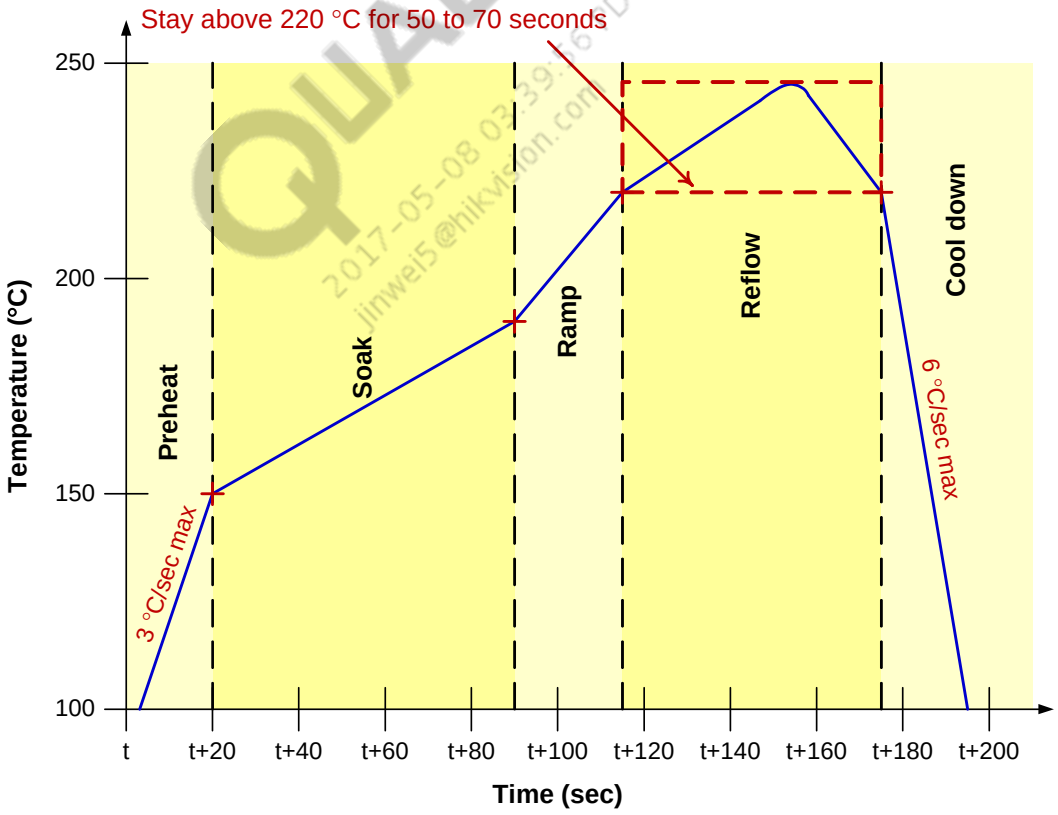


Figure 6-1 Typical SMT reflow profile

6.2.3 SMT peak package-body temperature

During a production board's reflow process, the temperature seen by the package must be controlled. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more). Although the solder-paste manufacturer's recommendations for optimum temperature and duration for solder reflow must be followed, the Qualcomm recommended limits must not be exceeded.

6.2.4 SMT process verification

Qualcomm recommends verification of the SMT process prior to high-volume board assembly, including:

- Electrical continuity
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume

6.3 Board-level reliability

Qualcomm conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

For board-level reliability data, refer to *Board-Level Reliability DRQFN/mQFN* (BR80-NT096-1).

7 Part Reliability

7.1 Reliability qualification summary

IPQ4018 reliability evaluation report.

Table 7-1 Silicon reliability results

Tests, Standards and Conditions	Lot/Sample	Result
Average failure rate (AFR) in FIT (λ) failure in billion device-hours HTOL: JESD22-A108-A Use condition: Temperature: 65 °C, core voltage: 1.2 V (Total samples from three different wafer lots)	3x77	0F/231 AFR=10.2
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from three different wafer lots)	3x77	97.7
ESD - Human-body model (HBM) rating JESD22-A114-F Target: 2000 V (Total samples from one wafer lot)	1x3	Pass
ESD - Charge-device model (CDM) rating JESD22-C101-D Target: 500 V (Total samples from one wafer lot)	1x3	Pass
Latch-up (I-test) EIA/JESD78A Trigger current: ±100 mA; temperature: 85 °C (Total samples from one wafer lot)	1x6	Pass
Latch-up (Vsupply overvoltage) EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × Vdd max per device specification; temperature: 85 °C (Total samples from one wafer lot)	1x6	Pass

Table 7-2 Package reliability results

Tests, Standards and Conditions	First assembly source sample size (lot/sample)	Second assembly source sample size (lot/sample)	Result
Moisture resistance test (MRT) MSL3; J-STD-020/JESD22-A113-F Reflow at 260 +0/-5 °C, Total samples from three different assembly lots	6x231	6x231	Pass
Temperature cycle JESD22-A104-D Temperature: -60°C to 150°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8-10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning** JESD22-A113-F MSL 3, reflow temperature: 260C+0/-5°C, Total samples from three different assembly lots	6x77	6x77	Pass
Unbiased highly accelerated stress test JESD22-A118 130C / 85% RH and 96 hrs duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260C+0/-5 °C, Total samples from three different assembly lots	6x77	6x77	Pass
Biased Highly Accelerated Stress test JESD22-A110 110C / 85% RH and 264 hrs duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260C+0/-5 °C, Total samples from three different assembly lots	3x77	3x77	Pass
High-Temperature Storage Life JESD22-A103-C Temperature 150 °C, 500, 1000 hours Total samples from three different assembly lots	6x77	6x77	Pass
Physical dimensions JESD22-B100-A	1x15	1x15	Pass
Die shear MIL-STD-883E, Method 2019 Total samples from three different assembly lots at each SAT	5x3	5x3	Pass

7.2 Qualification sample description

Device name:	IPQ4018
Package type:	180DRQFN
Package body size:	14.0 mm × 14.0 mm × 0.90 mm
Pin count:	180
Pin composition:	Matte tin
Pin pitch:	0.50 mm