QCA9563 802.11n 3x3 2.4 GHz Premium SOC for WLAN Platforms

Data Sheet

80-Y6999-3 Rev. E

July 2014

Confidential and Proprietary – Qualcomm Atheros Inc.

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Revision History

Revision	Date	Description
A	October 2013	Initial Release
B	January 2014	Added Registers, AC Specifications and electrical information
C	March 2014	Added Reliability chapter, tape and reel information, and chip makings information
D	April 2014	Added Reset Register 2 (RST_RESET2), GPIO MUX table
E	July 2014	Updated Power Consumption Information

Contents

1 General Description

The Qualcomm® XSPAN™ QCA9563 is a highly integrated and feature-rich IEEE 802.11n 3x3 2.4 GHz System-on-a-Chip (SoC) for advanced WLAN platforms.

It includes a MIPS 74Kc processor, an SGMII interface and an external memory interface for serial Flash, DDR1 or DDR2, UART, PCIe, two USB 2.0 Host controllers with built-in MAC/PHY and GPIOs that can be used for LED controls or other general purpose interface configurations.

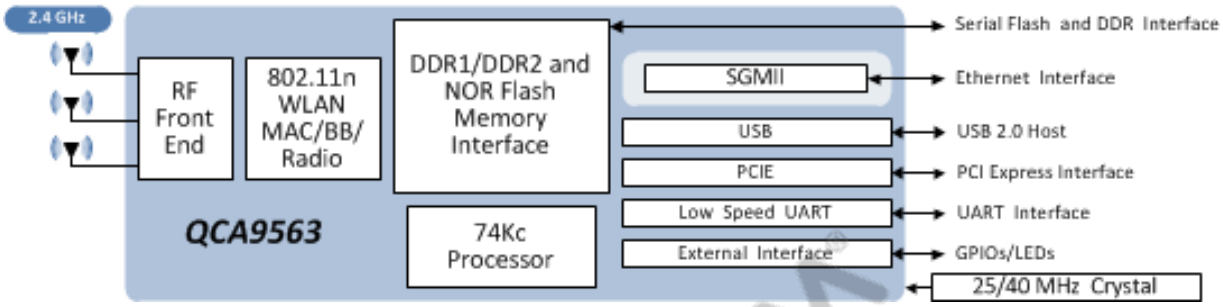
The QCA9563 supports 802.11n operations up to 216 Mbps for 20 MHz and 450 Mbps for 40 MHz, and 802.11b/g data rates. Additional features include Maximal Likelihood (ML) decoding, Low-Density Parity Check (encoding) and Maximal Ratio Combining (MRC).

The QCA9563 supports booting from NOR flash.

1.1 Features

- 74Kc MIPS processor with 64 KB I-Cache and 32 KB D-Cache, targeted to operate at 775 MHz
- External 16-bit DDR1, operating at up to 200 MHz, DDR2 operating at up to 333.5 MHz
- SPI NOR Flash memory support
- SGMII interface to connect to an external switch
- One low-speed UART (115 Kbps) and multiple GPIO pins for general purpose I/O
- Fully integrated RF Front-End including PAs and LNAs
- Optional external LNA/PA
- 25/40 MHz reference clock input
- 1.2 V switching regulator
- Advanced power management with dynamic clock switching for ultra-low power modes
- 164-pin 13 mm x 13 mm DRQFN package
- Two USB 2.0 Host controllers with built-in MAC/PHY
- PCIe Root Complex Interface

1.2 QCA9563 System Block Diagram



2 Pin Descriptions

This section contains both a package pinout and tabular listings of the signal descriptions.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
OD	An open-drain digital output signal
O	A digital output signal
P	A power or ground signal

Figure 2-1 shows the QCA9563 pinout.

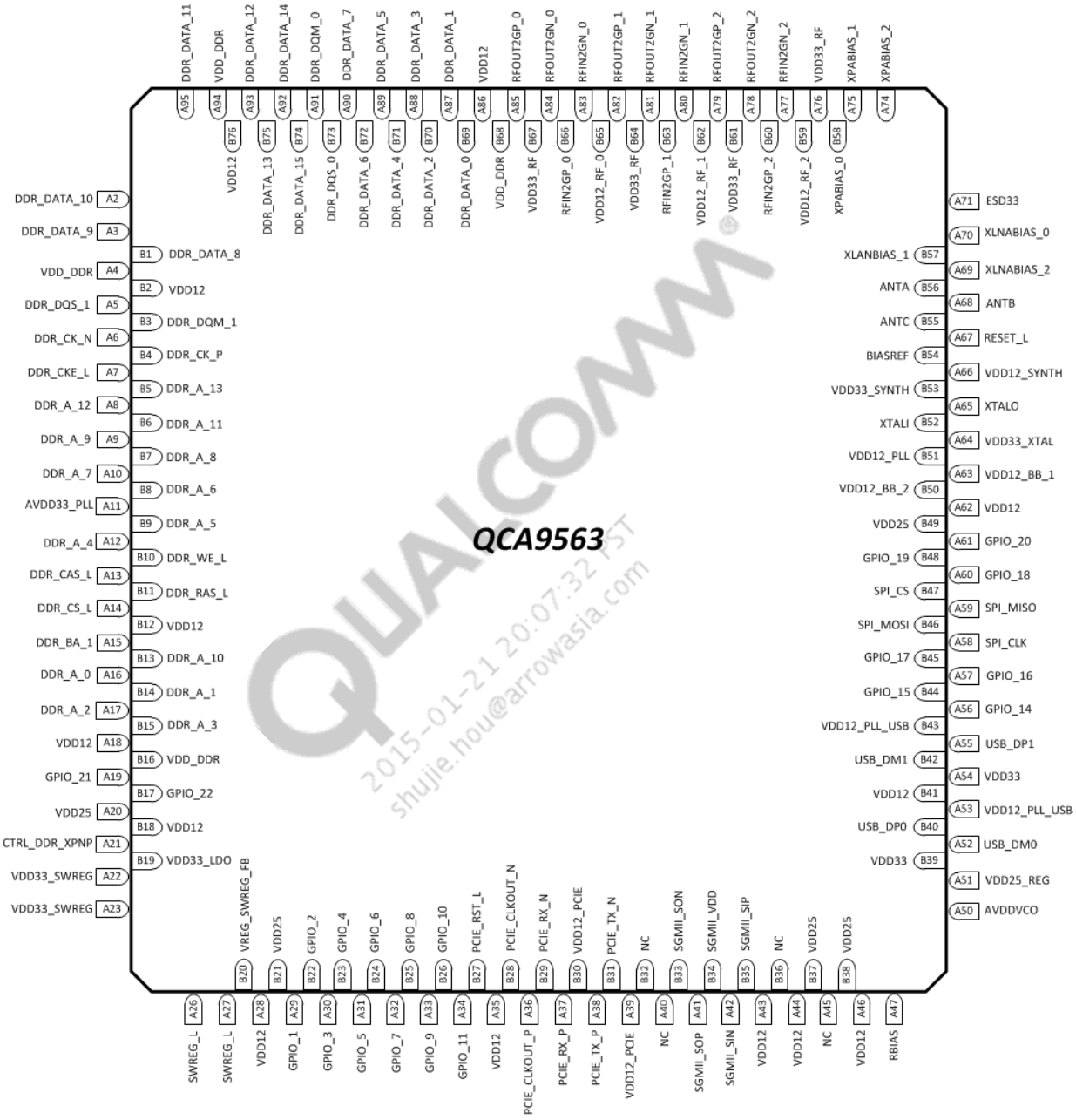


Figure 2-1 Package Pinout (See-Through Top View)

Table 2-1 provides the signal-to-pin relationship information for the QCA9563.

Table 2-1 Signal to Pin Relationships and Descriptions

Signal Name	Pins	Type	Description
General			
RESET_L	A67	IH	External power on reset with weak pull up. This signal is internally pulled up to 3.3 V. It is recommended to leave this signal floating if resetting the chip externally is not required. Otherwise the RESET_L input must be driven with 3.3 V logic.
XTALI	B52	I	25/40 MHz crystal When using an external clock (TCXO), the XTALI pin is grounded and the XTALO pin should be driven with a square wave clock. AC coupling is recommended for the clock signal to the XTALO pin. The internal circuit provides the DC bias of approximately 0.6 V. The peak-to-peak swing of the external clock can be between 0.3 V and 1.2 V. In general, larger swings and sharper edges reduce jitter, but introduce the potential of high frequency spurious tones. The phase noise of the oscillator should be lower than -145 dBc/Hz at 100 KHz carrier offset.
XTALO	A65	I/O	
PCIE			
PCIE_CLKOUT_N	B28	OA	Differential reference clock (100 MHz)
PCIE_CLKOUT_P	A36		
PCIE_RX_N	B29	IA	Differential receive
PCIE_RX_P	A37		
PCIE_TX_N	B31	OA	Differential transmit
PCIE_TX_P	A38		
PCIE_RST_L	B27	IL	PCI Express reset with weak pull-down
Radio			
RFIN2GN_0	A83	IA	Differential RF inputs for 2.4 GHz chain 0; Use one side for single-ended input
RFIN2GP_0	B66	IA	
RFOUT2GN_0	A84	OA	Differential RF outputs for 2.4 GHz chain 0
RFOUT2GP_0	A85	OA	
RFIN2GN_1	A80	IA	Differential RF inputs for 2.4 GHz chain 1; Use one side for single-ended input
RFIN2GP_1	B63	IA	
RFOUT2GN_1	A81	OA	Differential RF outputs for 2.4 GHz chain 1
RFOUT2GP_1	A82	OA	
RFIN2GN_2	A77	IA	Differential RF inputs for 2.4 GHz chain 2; Use one side for single-ended input
RFIN2GP_2	B60	IA	
RFOUT2GN_2	A78	OA	Differential RF outputs for 2.4 GHz chain 2
RFOUT2GP_2	A79	OA	

Table 2-1 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pins	Type	Description
Analog Interface			
BIASREF	B54	BIASREF voltage is 310 mV; must connect a 6.19 KΩ ± 1% resistor to ground	
RBIAS	A47	BIAS for Ethernet; connect a 2.43 KΩ ±1% resistor to ground. The resistor value is adjustable, depending on the PCB layout.	
XPABIAS_0	B58	Optional external power amplifier bias	
XPABIAS_1	A75		
XPABIAS_2	A74		
XLNABIAS_0	A70	Optional external LNA bias	
XLNABIAS_1	B57		
XLNABIAS_2	A69		
External Switch Control			
ANTA	B56	O	External RF switch control These output pins are in the V_{DD33} voltage domain.
ANTB	A68	O	
ANTC	B55	O	
External Memory Interface			
DDR_A_0	A16	O	14-bit external memory address bus
DDR_A_1	B14	O	
DDR_A_2	A17	O	
DDR_A_3	B15	O	
DDR_A_4	A12	O	
DDR_A_5	B9	O	
DDR_A_6	B8	O	
DDR_A_7	A10	O	
DDR_A_8	B7	O	
DDR_A_9	A9	O	
DDR_A_10	B13	O	
DDR_A_11	B6	O	
DDR_A_12	A8	O	
DDR_A_13	B5	O	
DDR_BA_0	B12	O	2-bit bank address to indicate which bank the chip is accessing
DDR_BA_1	A15	O	
DDR_CKE_L	A7	O	Deactivates the external memory clock when the signal is high
DDR_CK_N	A6	O	DDR_CK_P and DDR_CK_N are differential clock outputs. All address and control signals timing are related to the crossing of the positive edge of DDR_CK_P and the negative edge of DDR_CK_N.
DDR_CK_P	B4	O	

Table 2-1 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pins	Type	Description
DDR_CS_L	A14	O	External memory chip select signal, active low
DDR_CAS_L	A13	O	When this signal is asserted, it indicates the address is a column address. Active when the signal is low.
DDR_RAS_L	B11	O	When this signal is asserted, it indicates the address is a row address. Active when the signal is low.
DDR_DQM_0	A91	O	DDR data mask for data byte 0 and 1
DDR_DQM_1	B3	O	
DDR_DQS_0	B73	I/O	DDR data strobe for data byte 0 and 1
DDR_DQS_1	A5	I/O	
DDR_WE_L	B10	O	When this signal is asserted, it indicates that the following transaction is write. Active when the signal is low.
DDR_DATA_0	B69	I/O	16-bit external memory data bus
DDR_DATA_1	A87	I/O	
DDR_DATA_2	B70	I/O	
DDR_DATA_3	A88	I/O	
DDR_DATA_4	B71	I/O	
DDR_DATA_5	A89	I/O	
DDR_DATA_6	B72	I/O	
DDR_DATA_7	A90	I/O	
DDR_DATA_8	B1	I/O	
DDR_DATA_9	A3	I/O	
DDR_DATA_10	A2	I/O	
DDR_DATA_11	A95	I/O	
DDR_DATA_12	A93	I/O	
DDR_DATA_13	B75	I/O	
DDR_DATA_14	A92	I/O	
DDR_DATA_15	B74	I/O	

Table 2-1 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pins	Type	Description
GPIO			
GPIO_1	A29	I/O	General purpose I/O, programmable, can be used as JTAG, UARTs, LED control. Default input pins can be grounded, and default output pins can be left open if not used.
GPIO_2	B22	I/O	
GPIO_3	A30	I/O	
GPIO_4	B23	I/O	
GPIO_5	A31	I/O	
GPIO_6	B24	I/O	
GPIO_7	A32	I/O	
GPIO_8	B25	I/O	
GPIO_9	A33	I/O	
GPIO_10	B26	I/O	
GPIO_11	A34	I/O	
GPIO_14	A56	I/O	
GPIO_15	B44	I/O	
GPIO_16	A57	I/O	
GPIO_17	B45	I/O	
GPIO_18	A60	I/O	
GPIO_19	B48	I/O	
GPIO_20	A61	I/O	
GPIO_21	A19	I/O	
GPIO_22	B17	I/O	

Symbol	Pin	Type	Description
Regulator Control			
CTRL_DDR_XPNP	A21	OA	External PNP Control. Connect to the base of an external PNP: collector to VDD_DDR and emitter to V_{DD33}
SPI			
SPI_CS	B47	O	SPI chip select
SPI_MOSI	B46	O	Data transmission from the QCA9563 to an external device. On reset, SPIMOSI is output and can directly interface with a SPI device such as a serial flash.
SPI_MISO	A59	IL	Data transmission from an external device to the QCA9563. On reset,SPIMISO is input, which should be interfaced with an SPI device via a resistor divider for reliability.
SPI_CLK	A58	O	SPI serial interface clock
SGMII Interface			
SGMII_SIN	A42	I	Negative signal of the SGMII differential input
SGMII_SIP	B35	I	Positive signal of the SGMII differential input

Symbol	Pin	Type	Description
SGMII_SON	B33	O	Negative signal of the SGMII differential output
SGMII_SOP	A41	O	Positive signal of the SGMII differential output
USB			
USB_DM0	A52	IA/OA	USB D- signal; carries USB data to and from the USB 2.0 PHY
USB_DM1	B42	IA/OA	Second USB D- signal; carries USB data to and from the USB 2.0 PHY
USB_DP0	B40	IA/OA	USB D+ signal; carries USB data to and from the USB 2.0 PHY
USB_DP1	A55	IA/OA	Second USB D+ signal; carries USB data to and from the USB 2.0 PHY
Internal Voltage Regulator			
SWREG_L	A26, A27	1.2 V switching regulator output	
VDD33_SWREG	A22, A23	3.3 V input to the internal switching regulator	
VREG_SWREG_FB	B20	Feedback to the internal switching regulator	
Power			
AVDDVCO	A50	1.2 V input to the internal switching regulator	
AVDD33_PLL	A11	3.3 V power for CPU/DDR PLL	
ESD33	A71	Used to connect to VDD33 to improve ESD protection	
SGMII_VDD	B34	1.2 V power for SGMII	
VDD12	B2, A18, B18, A28, A35, A43, A44, A46, B41, A62, A86, B76	Digital 1.2 V supply	
VDD12_PLL	B51	Analog 1.2 V supply	
VDD12_SYNTH	A66		
VDD12_RF_0	B65		
VDD12_RF_1	B62		
VDD12_RF_2	B59		
VDD12_BB_1	A63		
VDD_12_BB_2	B50		
VDD12_PCIE	A39, B30	PCIE 1.2 V support	
VDD12_PLL_USB	B43, A53	1.2V supply for USB PLL	
VDD_DDR	A4, B16, B68, A94	DDR1/DDR2 supply 2.6 V and 1.8 V typical	
VDD25	A20, B21, B37, B38, B49	I/O 2.62 V Supply	
VDD25_REG	A51	VDD 2.5 V regulator	

Symbol	Pin	Type	Description
VDD33	B39, A54	Analog I/O, LDO regulator SWREG 3.3 V supplies	
VDD33_LDO	B19		
VDD33_SYNTH	B53		
VDD33_XTAL	A64		
VDD33_RF	A76, B61, B64, B67		
Ground Pad			
Exposed Ground Pad	—	Tied to GND; see “Package Dimensions” on page 354	
No Connect			
NC	B32, A40, B36, A45	No Connection	

3 Functional Description

3.1 Functional Block Diagram

Figure 3-1 illustrates the QCA9563 functional block diagram.

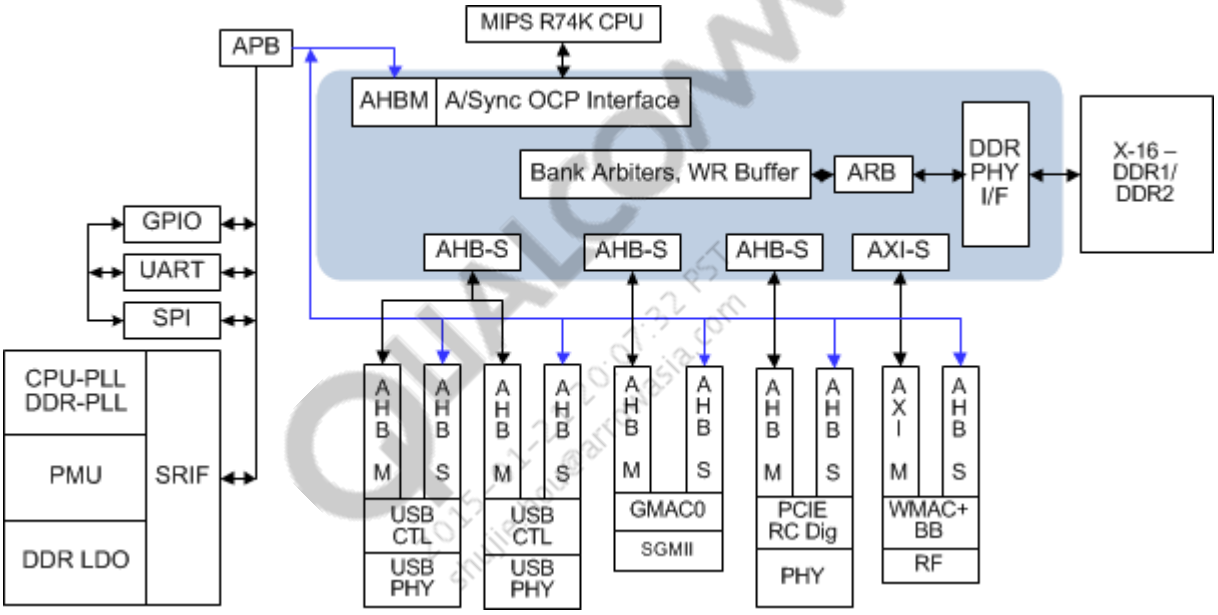


Figure 3-1 Functional Block Diagram

The QCA9563 is comprised of several internal functional blocks, as summarized in Table 3-1.

Table 3-1 Functional Blocks

Block	Description
CPU Core and Memory Controller	74Kc MIPS processor with 64 KB I-Cache and 32 KB D-Cache, targeted to operate at 775 MHz ■ The memory controller is targeted to run at a frequency of 333.5 MHz (667 M transfers/sec) ■ Supports DDR self refresh mode for low power consumption ■ Synchronous mode is also supported where the memory controller and CPU operate with a single phase align clock ■ Clock dithering for DDR/CPU clocks to reduce EMI interference ■ DDR Clock dithering effected immediately after refresh cycle
Clocking	Three internal PLLs: CPU, DDR and the WLAN PHY layer generate various internal clocks. The PLLs support a 25/40-MHz reference clock input. See PLL and Clock Control.
DDR Memory	■ DDR1 x16, DDR2 x16 See DDR Memory Controller.
SGMII	Serial Gigabit Media Interface (SGMII) used to connect to an external switch

Table 3-1 Functional Blocks (cont.)

Block	Description
PCI Express Interface	PCIE 1.1 interface Root Complex interface. See PCIE RC.
USB	Two USB 2.0 controllers with built-in SIE (Serial Interface Engine)/PHY supports Host mode. See USB 2.0 Interface.
WLAN	3 chain / 3 stream (3x3) IEEE 802.11n WLAN MAC, PHY, and internal radio that operates in 2.4 GHz
UART	Normal speed UART (16550 equivalent) at speeds up to 115.2 Kbps. See Low-Speed UART Interface.
GPIO	Contains 20 highly configurable GPIO pins; any multiplexed signal can be routed to any GPIO as output, and any multiplexed input can be routed from any GPIO pin to the internal logic. See GPIO.
Voltage Regulator and LDOs	Efficient 1.2 V switching regualtor for providing analog and digital core voltage of 1.2 V. LDOs are also provided to generate power to DDR1 (2.6 V), DDR2 (1.8 V) that can supply power to external memories and the DDR pads on the chip. GPIOs are powered by 2.62 V LDO.
Bootstrap Options	Several features of the QCA9563 can be configured or selected based on bootstrap pins whose state on power-on reset selects a given choice or configuration. See Bootstrap Options.

3.2 Bootstrap Options

Table 3-2 details the QCA9563 bootstrap options. The GPIO pins have internal pull-downs and the DDR pins have internal pull-ups.

Table 3-2 Bootstrap Options

Bit	Name	Pin	Description	
15:13	RES	Reserved	Reserved (Reset 0x0)	
12	SOFTWARE_OPTION_2	DDR_A_5	Can be used by software for any purpose	
11	SOFTWARE_OPTION_1	DDR_A_4	Can be used by software for any purpose	
10	RES	Reserved	Reserved (Reset 0x0). No pull down capable.	
9:4	RES	Reserved	Reserved (Reset 0x0)	
3	JTAG_MODE	GPIO19	0	EJTAG
			1	JTAG
2	REF_CLK	GPIO20	0	25 MHz reference clock
			1	40 MHz reference clock
1	RES	Reserved	Reserved (Reset 0x0)	
0	DDR_SELECT	GPIO17	0	Selects DDR 2 (Default)
			1	Selects DDR 1

3.3 Reset

Figure 3-2 shows the QCA9563 reset.

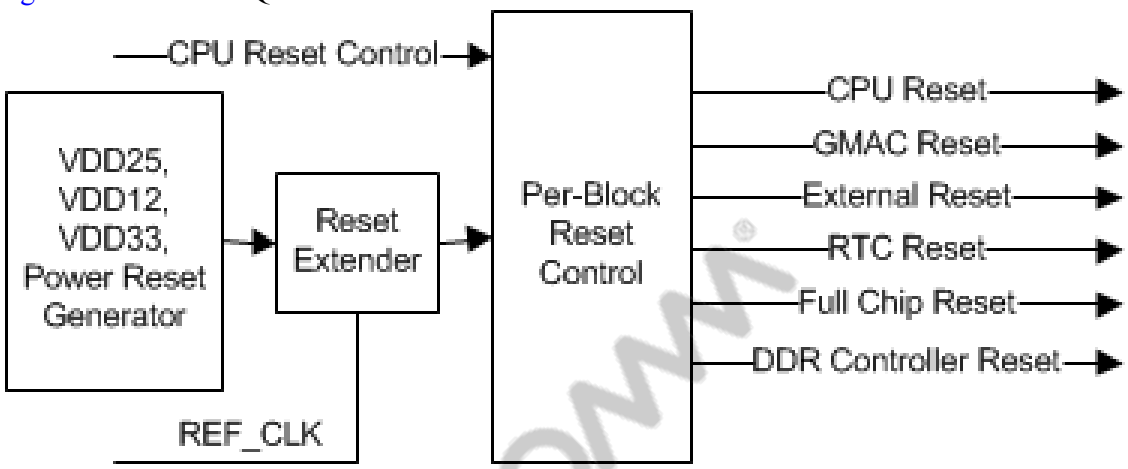


Figure 3-2 Reset

Each of the per- block resets can be issued by software by writing to the RST_RESET register. See Reset (RST_RESET) for the bit definitions for each per block reset.

3.4 PLL and Clock Control

3.4.1 Full Chip Clocking Structure

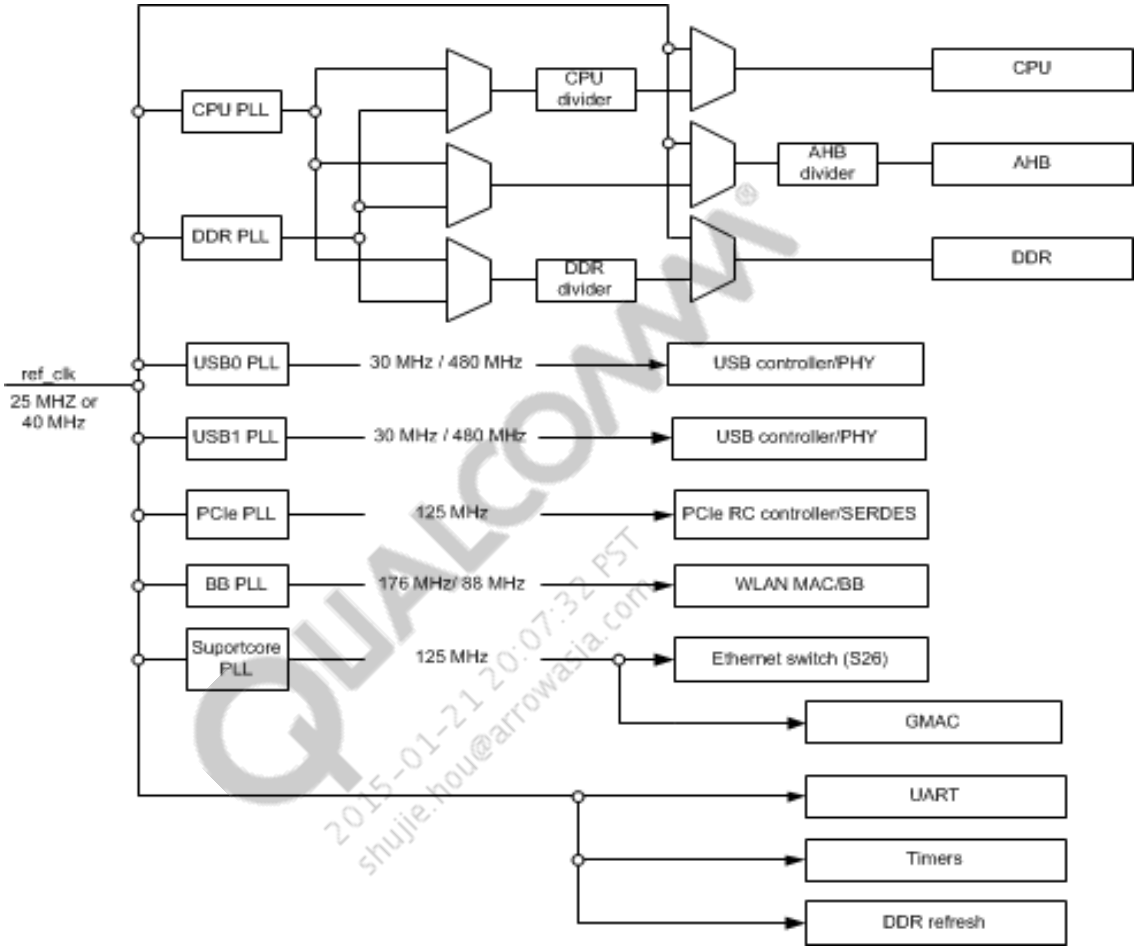


Figure 3-3 Full Chip Clocking Structure

The QCA9563 includes the BB, CPU, DDR, PCIE digital as well as the Ethernet and USB PLLs. See Table 3-3.

Table 3-3 QCA9563 PLLs

PLL	Description
BB PLL	By default, this PLL generates clocks for the radio, baseband, and WMAC.
CPU PLL	By default the source clock for the CPU_CLK, although it can also be derived from the DDR PLL.
DDR PLL	By default the source clock for DDR_CLK and AHB_CLK, though both can also be derived from the CPU PLL.
Ethernet PLL	Generates the clock for all Ethernet interfaces, MAC
USB PLL	Generates the USB 30 MHZ/480 MHz clock for the USB controller
PCIE PLL	Generates the 100 MHz reference clock for the PCIE RC. The final output frequency of the PCIE PLL is similarly configurable, like the CPU and DDR PLLs, although a fixed 100 MHz clock is required. OUTDIV should be set to 3, and N=14 for 100 MHz.

3.4.2 CPU PLL

The CPU PLL is configured with the registers CPU Phase Lock Loop Configuration (CPU_PLL_CONFIG), page 8-139, CPU Phase Lock Loop Configuration 1 (CPU_PLL_CONFIG1, page 8-140, and CPU DDR Clock Control (CPU_DDR_CLOCK_CONTROL), page 8-141. The clock can vary slightly by changing the divider's FRAC. The dithering is controlled through the CPU PLL Dither Parameter registers (CPU_PLL_DITHER1 and CPU_PLL_DITHER2). Note that if DDR_CLK is derived from the CPU PLL, it is better to turn off dithering.

The clock switcher and dynamic clock divider guarantee any change in inputs to this module is glitch-free; thus input to this block can change. Make sure when modifying the select to the clock switcher module that both clock inputs are present as switching from one clock to another depends on both clocks. Figure 3-4 details the derivation of the CPU_CLK that clocks the MIPS processor.

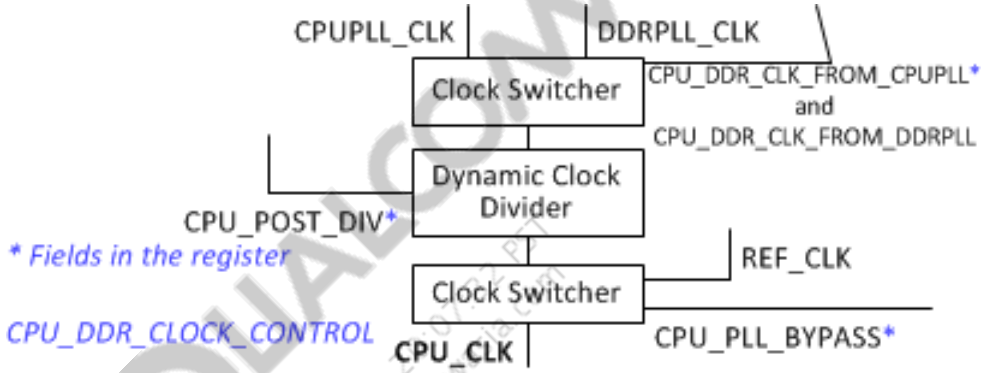


Figure 3-4 74Kc Processor CPU Clock

3.4.3 DDR PLL

The DDR PLL is configured with the registers CPU Phase Lock Loop Configuration (CPU_PLL_CONFIG), page 8-139, CPU Phase Lock Loop Configuration 1 (CPU_PLL_CONFIG1, page 8-140 and CPU DDR Clock Control (CPU_DDR_CLOCK_CONTROL), page 8-141. The clock can vary slightly by changing the divider's FRAC. The dithering is controlled through the DDR PLL Dither Parameter registers (DDR_PLL_DITHER1 and DDR_PLL_DITHER2). Figure 3-5 shows the DDR_CLK and AHB_CLK select signal change to clock switching logic, which should be made only if both clock inputs are preset.

The FRAC part of the PLL is dynamic, but the INT part of the divider requires the PWD to go high and then low. Thus, changing the PLL clocks dynamically would be possible only by:

1. Asserting the PLL_BYPASS mode bit.
2. Asserting the PWD for that PLL.
3. Reconfiguring divider INT/FRAC values.
4. Deasserting the PWD for the PLL
5. Waiting for the clock to become stable by polling the UPDATE bit.
6. Removing the PLL_BYPASS bit for this PLL.

The CPU can do this procedure any time for CPU_CLK/AHB_CLK, which is useful to enter low power states leading to minimal chip power consumption. Another way to change the CPU/AHB/DDR_POST_DIV is to shift down to lower clock for these clocks. An optimal DDR and CPU frequency can be dynamically chosen, and the PLL reprogrammed for optimal power. However, make sure no DDR transaction is pending or in progress before changing DDR_CLK frequency.

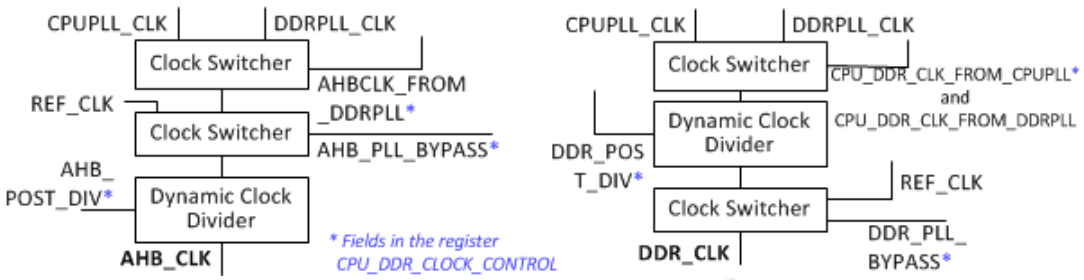


Figure 3-5 DDR_CLK and AHB_CLK

3.4.4 Ethernet PLL

The Ethernet PLL is controlled by the register Switch Clock Source Control (SWITCH_CLOCK_SPARE).

3.5 MIPS Processor

The QCA9563 integrates an embedded MIPS 74Kc processor.

Table 3-4 summarizes the configuration settings used by the QCA9563. Upon reset, the CPU puts out an address of 0xBFC00000 which is mapped to the flash address space. The QCA9563 has a 74Kc MIPS processor with 64 KB I-Cache and 32 KB D-Cache, targeted to operate at up to 775 MHz .

Table 3-4 Core Processor Configuration Settings

Setting	Description
Cache Size	The QCA9563 implements 64 KB 4-way set associative instruction cache and 32 KB 4-way set associative data cache. It supports single cycle multiply-accumulate, MIPS32 and MIPS16 instruction sets, and non-blocking cached reads.
Endian	The QCA9563 implements big Endian addressing.
Block Addressing	The QCA9563 implements sequential ordering.

3.6 Address Map

Figure 3-6 shows the address space allocation.

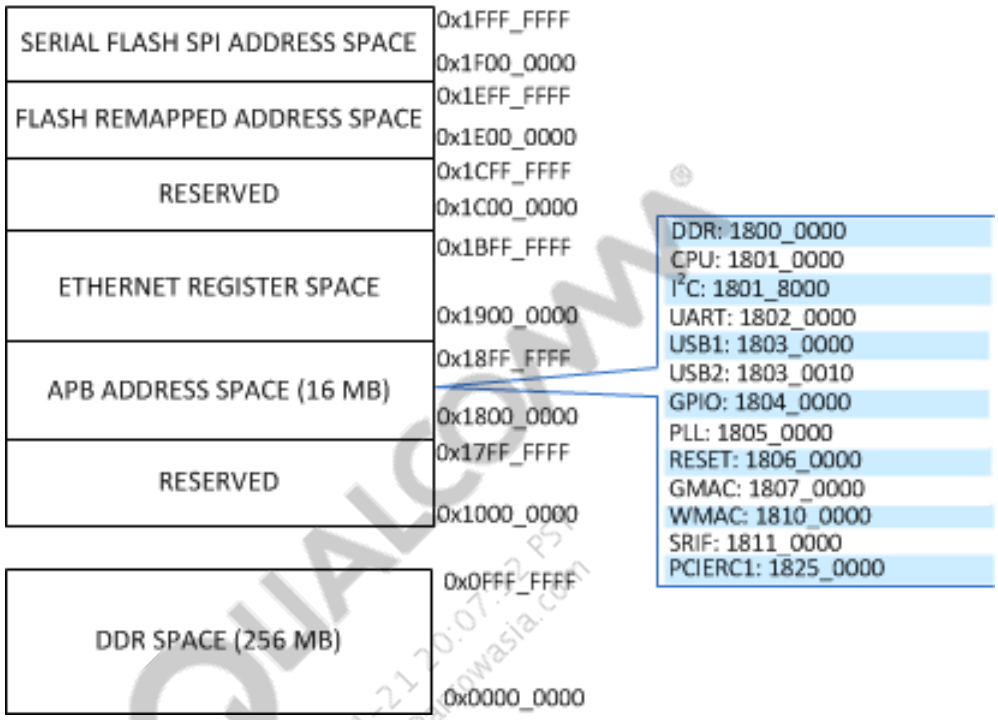


Figure 3-6 Address Space Allocation

3.7 DDR Memory Controller

The QCA9563 allows an external memory interface supporting 16-bit DDR1, or DDR2. The memory controller can enter DDR self refresh for low power modes. The DDR1 and DDR2 modes have small differences in read/write transactions. For a write transaction, DDR2 memory expects write data after a latency depending on CAS latency. DDR1 memory expects the first data immediately after the clock in which the write command is issued.

The controller uses the configurable parameter DDR2_TWL in the DDR2 Configuration (DDR_DDR2_CONFIG) register. The parameter is applicable for DDR1 and DDR2 modes: it should be set to one for DDR1 mode, and to (CAS – 1) * 2 – 1 for DDR2 mode.

Enabling DDR2 Mode

Set the bit MODE_EN in DDR Controller Configuration (DDR_CTL_CONFIG) to zero, and the bit ENABLE_DDR2 in the DDR2 Configuration (DDR_DDR2_CONFIG) register to one.

- If HALF_WIDTH is set, x16 mode is selected and requires the VEC field in the register DDR Read Data Capture Bit Mask (DDR_RD_DATA_THIS_CYCLE) to be set to 0xFFFF.
- Set the bit SEL_18 in the register DDR2 Configuration (DDR_DDR2_CONFIG) to one.

3.7.1 DDR Configurations

Table 3-5 shows the DDR configurations. See the reference design for details.

Table 3-5 DDR Configurations when DDR_CONFIG2_SWAP_A26_A27 = 0

Device on Board	Total Memory	Mode	DDR1	DDR2	Notes
512 Mbits x 16	64 MBytes	16 Bit	Yes	Yes	For both DDR1 and DDR2, CPU address A26, A27 unused
512 Mbits x 8 512 Mbits x 8	128 MBytes	16 Bit	Yes	Yes	In DDR1, CPU address A26 is A11 of COL, A27 used In DDR2, A26 is A13 of ROW, A27 unused
1 Gbits x 16	128 MBytes	16 Bit	Yes	Yes	In DDR1, CPU address A26 is A13 of ROW, A27 unused. In DDR2, CPU address A13 is BA_2, A27 unused.

Table 3-6 DDR Configurations when DDR_CONFIG2_SWAP_A26_A27 = 1

Device on Board	Total Memory	Mode	DDR1	DDR2	Notes
512 Mbits x 16	64 MBytes	16 Bit	Yes	Yes	For both DDR1 and DDR2, CPU address A26, A27 unused
512 Mbits x 8 512 Mbits x 8	128 MBytes	16 Bit	No	Yes	DDR1 is not supported In DDR2, A26 is A13 of ROW; A27 unused
1 Gbits x 16	128 MBytes	16 Bit	Yes	Yes	In DDR1, CPU address A26 is A13 of ROW, A27 unused. In DDR2, CPU address A26 is BA_2, A27 unused.

3.7.2 DDR Initialization Sequences

3.7.2.1 DDR1 Controller Initialization

NOTE It is extremely important to leave the reset values of many register fields untouched. Therefore software should always read a register and then modify only the required fields unless otherwise mentioned.

- Burst length (BL) should always be 8.
- Read Latency (RL) = Additive Latency (AL) + CAS Latency (CL)
- Write Latency (WL) = RL – 1
- tCK = CK_P CLK period

1. Program the register DDR Controller Configuration (DDR_CTL_CONFIG):

Bit	Bit Name	Setting	
1	HALF_WIDTH	0	Reserved
		1	For x16

This step must to be done before memory initialization; the other steps do not have this dependency.

2. Set a value in DDR Read Data Capture Bit Mask (DDR_RD_DATA_THIS_CYCLE):
   - 0xFFFF for x16
3. If $F_{DDR\_CLK} < 2 * F_{AHB\_CLK}$ (frequency of DDR_CLK and AHB_CLK), program the DDR FSM wait control with 0x00000A24.
4. Set the timing parameters in DDR DRAM Configuration (DDR_CONFIG). These numbers typically use the values from the specification, but greater values can also be used. Numbers are in terms of the number of controller clocks.

Bit	Bit Name	Description
26:23	TMRD	Load mode register command cycle time.
22:17	TRFC	Auto-refresh command period
16:13	TRRD	Active bank a to active bank delay
12:9	TRP	Precharge command period
8:5	TRCD	Active to read or write delay
4:0	TRAS	Active to precharge time = max(tRAS_min, tRCD + CL). A greater value can be programmed if tRTP is not satisfied.

5. Set timing parameters in DDR Controller Configuration (DDR_CTL_CONFIG). Bits [25:8] show minimum values; a greater value can also be programmed. Numbers are in terms of controller clock numbers.

Bit	Bit Name	Setting
29:26	GATE_OPEN_LATENCY	2 * CAS_LATENCY

25:21	TWTR	Write-to-read Command delay [1+BL/2 + tWTR/tCK] * 2 For example: tWTR=2 tCK; BL=8 TWTR=2 * [1+4+2]= 14
20:17	TRTP	Read-to-precharge command delay BL/2 + max(tRTP,2)-2
16:12	TRTW	Read-to-write command delay (CL + BL/2) * 2 For example: CL=3; BL=8; TRTW=7 * 2= 14
11:8	TWR	Write recovery time [BL/2+tWR/tCK] * 2 – 1 For example: BL=8; tWR= 15 ns; tCK=(1/200 MHz)= 5 ns TWR=[4+3] * 2-1= 13

6. Initialize DDR memory as shown in DDR Memory Initialization.
7. Set the register DDR Refresh Control and Configuration (DDR_REFRESH).
   E.g., for TREFI = 7.8 µs, set DDR_REFRESH[13:0] to 195 (REFCLK = 25 MHz).
8. Set the ENABLE bit.

3.7.2.2 DDR2 Controller Initialization

NOTE It is extremely important to leave the reset values of many register fields untouched. Therefore software should always read a register and then modify only the required fields unless otherwise mentioned.

- Burst length (BL) should always be 8.
- Read Latency (RL) = Additive Latency (AL) + CAS Latency (CL)
- Write Latency (WL) = RL – 1
- tCK = CK_P CLK period

1. Program the register DDR Extended Mode (DDR_EXTENDED_MODE_REGISTER):

Bit	Bit Name	Setting	
1	HALF_WIDTH	0	Reserved
		1	For x16

This step must to be done before memory initialization; the other steps do not have this dependency.

2. Set a value in DDR Read Data Capture Bit Mask (DDR_RD_DATA_THIS_CYCLE):
   - 0xFFFF for x16
3. If $F_{DDR\_CLK} < 2 * F_{AHB\_CLK}$ (frequency of DDR_CLK and AHB_CLK), program the DDR FSM wait control with 0x00000A24.
4. Set the timing parameters in DDR DRAM Configuration (DDR_CONFIG). These numbers typically use the values from the specification, but greater values can also be used. Numbers are in terms of the number of controller clocks.

Bit	Bit Name	Description
26:23	TMRD	Load mode register command cycle time.
22:17	TRFC	Auto-refresh command period
16:13	TRRD	Active bank a to active bank delay
12:9	TRP	Precharge command period
8:5	TRCD	Active to read or write delay
4:0	TRAS	Active to precharge time = max(tRAS_min, tRCD + CL). A greater value can be programmed if tRTP is not satisfied.

5. Set timing parameters in DDR DRAM Configuration 2 (DDR_CONFIG2). Bits [25:8] show minimum values; a greater value can also be programmed. Numbers are in terms of controller clock numbers.

Bit	Bit Name	Setting
29:26	GATE_OPEN_LATENCY	2 * CAS_LATENCY

25:21	TWTR	[WL+BL/2 + max(2, tWTR/tCK)] * 2
		For example:
		tWTR = 7.5 ns;
		tCK = (1/200 MHz) = 5 ns;
		BL = 8; CL = 4; AL = 0
		WL = AL+CL-1 = 0+4-1 = 3
		TWTR = [3+4+max(2, 7.5/5)] * 2 = [3+4+2] * 2 = 18

20:17	TRTP	16-bit [(AL+BL+max(tRTP/tCK,2))-2] * 2
		For example:
		tRTP = 7.5 ns;
		tCK= (1/200 MHz) = 5 ns;
		BL=8; AL=0
		TRTP = [(0+8+2)-2] * 2=16

16:12	TRTW	(RL+BL/2+1-WL) * 2 For example: CL = 4; BL = 8; AL = 0; WL=3; TRTW = [4+4+1-3]*2 = 12
11:8	TWR	(BL/2+tWR/tCK) * 2-1 For example: BL = 8; TWR = 15 ns; TCK = (1/200 MHz) = 5 ns TWR = [4+3] * 2-1 = 13

6. Initialize DDR memory as shown in DDR Memory Initialization.
7. Set the register DDR Refresh Control and Configuration (DDR_REFRESH).
   E.g., for TREFI = 7.8 µs, set DDR_REFRESH[13:0] to 195 (REFCLK = 25 MHz).
   a. Set the ENABLE bit.

3.7.3 DDR Memory Initialization

These steps are performed as step 6 under DDR1 Controller Initialization, and as step 7 under DDR2 Controller Initialization.

1. To initialize DDR memory, when:
   - CKE is set low
   - Clocks are stable

   Allow a 200 µs delay then send an NOP/DESELECT command.
2. Set the CKE bit of the register DDR DRAM Configuration 2 (DDR_CONFIG2).
3. Issue a precharge all commands by setting the PREA bit of the register DDR DRAM Configuration (DDR_CONFIG) twice with a interval of 200 clock cycles between them.
4. Write to the register DDR Extended Mode (DDR_EXTENDED_MODE_REGISTER) to enable the DLL. Refer to the DDR memory device datasheet for bit-definitions of this register.
5. Issue an EMRS command to DDR by setting the EMRS bit in the register DDR DRAM Configuration (DDR_CONFIG) to enable the DLL.
6. Write to the register DDR Mode Value (DDR_MODE_REGISTER) with the value 0x1*N*3 (the reset value) to reset the DLL, where *N* indicates to set the four fields appropriately per the CAS value. Refer to the DDR memory device datasheet for bit-definitions of this register.
7. Issue an MRS command to DDR by setting the MRS bit of the register DDR DRAM Configuration (DDR_CONFIG).
8. Re-issue two precharge all commands again by redoing step 3.
9. After a 200 CLK second delay, issue two refresh commands by setting REF (bit [2]) of the register DDR DRAM Configuration (DDR_CONFIG) twice with a interval of 200 clock cycles between them.
10. Write to the register DDR Mode Value (DDR_MODE_REGISTER) with the value 0x0*N*3 to bring DLL out of reset, where *N* indicates to set the four fields appropriately per the CAS.
11. Issue an MRS command to DDR by setting the MRS bit of the register DDR DRAM Configuration (DDR_CONFIG).

3.7.4 CPU DDR Address Mapping

Table 3-7 shows the correspondence of the internal CPU address, the DDR interface address, and the physical memory address.

Table 3-7 CPU Address: DDR Interface Address Mapping

DDR Interface Address	Column Address	Row Address[1]	Bank Address
DDR_A_0	0	CPU_ADDR[11]	—
DDR_A_1	CPU_ADDR[2]	CPU_ADDR[12]	—
DDR_A_2	CPU_ADDR[3]	CPU_ADDR[13]	—
DDR_A_3	CPU_ADDR[4]	CPU_ADDR[14]	—
DDR_A_4	CPU_ADDR[5]	CPU_ADDR[15]	—
DDR_A_5	CPU_ADDR[6]	CPU_ADDR[16]	—
DDR_A_6	CPU_ADDR[7]	CPU_ADDR[17]	—
DDR_A_7	CPU_ADDR[8]	CPU_ADDR[18]	—
DDR_A_8	CPU_ADDR[23]	CPU_ADDR[19]	—
DDR_A_9	CPU_ADDR[25]	CPU_ADDR[20]	—
DDR_A_10	0	CPU_ADDR[21]	—
DDR_A_11	CPU_ADDR[26]	CPU_ADDR[22]	—
DDR_A_12	CPU_ADDR[27]	CPU_ADDR[24]	—
DDR_A_13 / DDR_BA_2	—	CPU_ADDR[26][2 3]	CPU_ADDR[26][4]
DDR_BA_0	—	—	CPU_ADDR[9]
DDR_BA_1	—	—	CPU_ADDR[10]

1. Row address: DDR_A_0 through DDR_A_12, when the row is accessed.
2. CPU_ADDR[26] is DDR_A_13 in DDR1 1 GBit
3. CPU_ADDR[26] is DDR_BA_2 in DDR2 1 GBit
4. CPU_ADDR[26] and CPU_ADDR[27] can be swapped during column addressing, to support these on-board configurations: 2 x (DDR1 1 GBit x8), 2 x (DDR1/2 1 GBit x16)

3.7.5 Refresh

DDR memory must refresh periodically. The DDR controller has an automatic refresh command generation module that clocks with REF_CLK. Because DDR_CLK is dynamic, the auto REFRESH_PERIOD works on the fixed REF_CLK.

3.7.6 Self Refresh

The QCA9563 DDR controller supports a self refresh (SF) sequence; that is, it has hardware support to issue commands to place DDR memory into and to exit SF mode. The register Self Refresh Timer (SF_TIMER) controls basic SF behavior.

If EN_SELF_REFRESH is set and no valid DDR transactions are in progress, the DDR controller initiates an SF enter sequence. If DDR clients have transactions in progress, the controller waits until no DDR activity is occurring.

If EN_AUTO_SF_EXIT is set, the controller initiates an exit SF sequence upon detecting a DDR request from any DDR client. If this bit is not set, DDR is in SF, a DDR new request is seen, the controller generates a miscellaneous DDR_ACTIVITY_IN_SF interrupt (see the register Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS)). Software can alternatively force the controller to exit SF by setting EN_SELF_REFRESH to 0.

The controller can also generate an interrupt to the CPU while entering SF, exiting SF, and while in SF if DDR activity is detected. Immediately after exiting SF, read commands should not be issued until TXSR is met and non-read commands should not be issued until TXSNR is met. These timing parameters can be programmed via the TXSNR and TXSR fields of the DDR_SF_CTL registers. Note that these are in terms of DDR_CLK and not REF_CLK.

While in SF, DDR_CK_P and DDR_CK_N clocks can be gated, optionally using the EN_SF_CLK_GATING bit.

3.8 GPIO

GPIO pins can be configured as input/output by programming the appropriate bits in the GPIO function registers. On reset, GPIOs are configured with certain default signals

NOTE JTAG pins must use GPIO[17:14]. Apart from JTAG, all signals can use any GPIO .

3.8.1 GPIO Output

GPIO is structured to output one of 128 signal through any GPIO pin. See Figure 3-7.

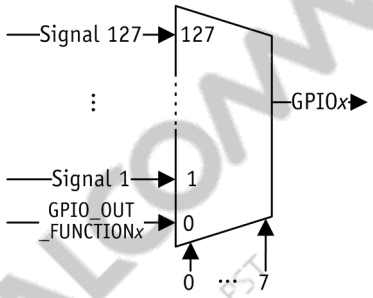


Figure 3-7 GPIO is Structured to Output 1 of 128 Signal Through Any GPIO

Each GPIO output is structured as 128:1 MUX. The MUX select is an 8-bit register that can be programmed with the values 0-127 to allow that particular input signal through the GPIO pin. The MUX selection values are displayed in Table 3-8.

Table 3-8 GPIO MUX Table

Signal Name	Mux Selection Value
Reserved	1 - 17
UART1 SOUT (TD)	18
UART1 RTS	19
UART1 SIN (RD)	20
UART1 CTS	21
UART1 SOUT	22
SRIF_SOUT	23
LED_SGMII_SPEED0	24
LED_SGMII_SPEED1	25
LED_SGMII_DUPLEX	26
LED_SGMII_LINK_UP	27
LED_SGMII_SPEED0 invert	28
LED_SGMII_SPEED1 invert	29
LED_SGMII_DUPLEX invert	30
LED_SGMII_LINK_UP invert	31
Reserved	32-36

Table 3-8 GPIO MUX Table

Signal Name	Mux Selection Value
SPI_CS1	37
SWCOM2	38
SWCOM3	39
SMART_ANY_CTL[2]	40
SMART_ANY_CTL[3]	41
ATT LED	42
PWR LED	43
TX FRAME	44
RX CLEAR EXTERNAL	45
LED NETWORK EN	46
LED POWER EN	47
Reserved	48 - 68
BT_ANT	69
RX CLEAR EXTENSION	70
Reserved	71-72
I2C_CLK	73
Reserved	74 - 76
I2C_SDA	77
CLK_REQ_N_RC	78
Reserved	79 - 88
SGMII_LCKDT	89
Reserved	90 -114
PCIE2_RESET_L_OUT	115
Reserved	90 -114116 - 127

The signal gets the source from the GPIO_OUT_FUNCTIONx registers. Each 32-bit register has select values for four GPIO pins (8 bits each). Those registers needed to control the GPIO pins are listed in Table 3-9.

Table 3-9 Corresponding Registers for GPIO Pins

Register	Selects values for these GPIO pins
GPIO Function 0 (GPIO_OUT_FUNCTION0)	GPIO pins 0, 1, 2, 3
GPIO Function 1 (GPIO_OUT_FUNCTION1)	GPIO pins 4, 5, 6, 7
GPIO Function 2 (GPIO_OUT_FUNCTION2)	GPIO pins 8, 9, 10, 11
GPIO Function 3 (GPIO_OUT_FUNCTION3)	GPIO pins 12, 13, 14, 15
GPIO Function 4 (GPIO_OUT_FUNCTION4)	GPIO pins 16, 17, 18, 19
GPIO Function 5 (GPIO_OUT_FUNCTION5)	GPIO pins 20, 21, 22

If set to zero, the CPU directly controls the GPIO through the GPIO Per Bit Set (GPIO_SET)/GPIO Per Bit Clear (GPIO_CLEAR) registers, or observes via the GPIO Input Value (GPIO_IN) register.

To output the signal through the GPIO pin, use this register programming:

1. If using a non-JTAG signal on GPIO[17:14], write the bit DISABLE_JTAG of the GPIO_OUT_FUNCTIONx register to 1.
2. Set the corresponding GPIO bit in GPIO Output Enable (GPIO_OE) to 0.
3. Write the particular GPIO field in GPIO_OUT_FUNCTIONx with the corresponding output signal value.

3.8.2 GPIO Input

GPIO inputs are structured so that any signal can source from any GPIO pin. See Figure 3-8.

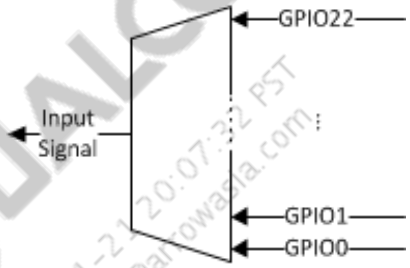


Figure 3-8 Any Signal Can Receive Input From Any GPIO

Each signal can receive its input from GPIOs. Each signal has an 8-bit register that can be programmed with the GPIO values 0-22; the signal gets its input for the corresponding GPIO pin programmed in the GPIO_IN_ENABLEx registers (GPIO Function 5 (GPIO_OUT_FUNCTION5).

To route the GPIO input to a particular signal, use this register programming:

1. If using a non-JTAG signal on GPIO[17:14], write the bit DISABLE_JTAG of the GPIO In Signals 3 (GPIO_IN_ENABLE3) register to 1.
2. Set the corresponding GPIO bit in the GPIO Output Enable (GPIO_OE) register to 1.
3. Write the particular 8-bit GPIO field in the register GPIO Function 5 (GPIO_OUT_FUNCTION5) with the corresponding output signal value.

   If a value greater than 22 is written, this signal is assigned a default value of 0.

3.9 Serial Flash SPI

The SPI controller supports two ways of programming the SPI device:

- The bit blasting method by which data, CLK, and the CS are programmed directly by CPU bit in the controller register SPI_IO_CNTRL_ADDR, which is shifted on to the interface signals.
- Direct programming of the data and the number of bits to shift. The controller takes care of shifting the specified number of bits.

The SPI controller has a dedicated chip select available to an external flash for booting, as well as two more configurable chip selects.

3.9.1 SPI Operations

Before performing any SPI operation, the FUNCTION_SELECT and REMAP_DISABLE bits of the register SPI Controller GPIO Mode Select (FUNCTION_SELECT_ADDR) are set to 1. Any page program or erase operations on the SPI device must enable the write enable latch (WEL).

3.9.2 Write Enable

1. Program the register SPI Controller GPIO Mode Select (FUNCTION_SELECT_ADDR) with the WREN CMD value.
2. Program SPI_SHIFT_CNT_ADDR:

SHIFT_CNT	8	Number of WREN command bits
TENATE	1	After shifting 8-bit deassert chip select
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

3.9.3 Page Program

- Send a **write enable** command before any page program or erase operations.
- Use the **send** command:
  a. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) with the PP CMD value.
  b. Program SPI Content to Shift Out or In (SPI_SHIFT_CNT_ADDR):

SHIFT_CNT	8	Number of command bits
TENATE	0	Do not deassert CS; CMD is followed by address/data
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

- Send the address:
  a. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) with the address to be programmed.
  b. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR):

SHIFT_CNT	24	Number of address command bits
TENATE	0	Do not deassert CS; CMD is followed by address/data
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

- Send the data:
  a. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) with the data to be programmed.
  b. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR):

SHIFT_CNT	32	Number of data bits
TENATE	1	Deassert chip select after programming the data
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

The command and address can be programmed together in SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) in the order: {8'CMD, 24'ADDR}. The SHIFT_CNT field in SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) is set to 32.

3.9.4 Page Read

- Send command and address:
  a. Program SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR) with the **read** command and address.
  b. Program SPI Content to Shift Out or In (SPI_SHIFT_CNT_ADDR):

SHIFT_CNT	32	Number of command and address bits
TERMINATE	0	Keep chip select asserted until the data is read
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

- Read the data by programming SPI Content to Shift Out or In (SPI_SHIFT_CNT_ADDR):

SHIFT_CNT	32	Number of bits to be read
TERMINATE	1	Deassert the chip select after the data is read
SHIFT_CLKOUT	0	Initial value of clk
SHIFT_CHNL	001	Enable chip select 0
SHIFT_EN	1	Enable shifting

3.10 Low-Speed UART Interface

The QCA9563 contains a 16550 equivalent UART controller/port for debug/console monitoring. The UART pins are multiplexed with GPIO pins. GPIO Output describes the multiplexed GPIO options. The UART controller can be programmed through a set of control registers. The UART supports programmable baud rates and can support up to 115.2 Kbps. This UART does not support hardware flow control.

3.11 PCIE RC

The QCA9563 has a PCIE root complex (RC) supporting a single-lane PCIE link at 2.5 Gbps. The RC core implements the PCIE protocol layers: transaction, data link, and physical.

The PCIE PHY module resides outside of the RC core, interfacing through the PIPE, which is the standard interface between the PHY and the RC core. The PHY is split across the PIPE so MAC functionality is in the RC core and PHY functionality is implemented in the PIPE-compliant PHY external to the RC.

It has a sideband interface referred to as data bus interface (DBI) controlled by the CPU via APB, which programs the RC core configuration space. The DBI delivers a read/write request from application logic to the internal registers of the core. The RC core configuration space contains these register maps:

- PCIE 3.0 compatible configuration space header

- PCIE capabilities structures
  (starts at offset 0x40)
- PCIE extended configuration space
  (starts at offset 0x100)
- Port logic (vendor-specific registers)
  (starts at offset 0x700)

The configuration and memory accesses to the two PCIE RC interfaces are mapped to the CPU AHB address space:

	Memory Slave	Configuration Slave
PCIE RC0	0x1000_0000 to 0x11FF_FFFF	0x1400_0000 to 0x5FF_FFFF

See Figure 3-9.

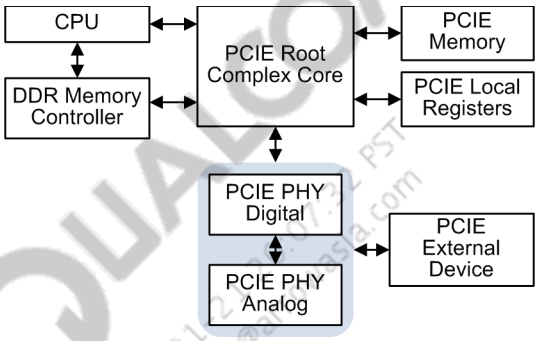


Figure 3-9 PCIE RC

3.11.1 Power Management

The PCIE RC supports L0s and L1 active state power management space. L0s is the low power standby state with lower entry/exit latencies. L1 saves more power, but with increased entry and exit latencies.

The PCIE RC includes the capacity to shut off the reference clocks going to the endpoint and powering down the RC PCIE PLL in L1 mode.

3.11.2 Interrupts

PCIE RC supports legacy INTx interrupts generated through PCIE message transactions. The application monitors the assertion and de-assertion messages for inbound INTx legacy interrupts (from the downstream component). It also supports MSI-based interrupt signalling through posted memory write transfers (only one of INTx or MSI can be enabled at any time).

3.11.3 Error Reporting Capability and Status Checking

PCIE RC support advanced error reporting (AER) and has the ability to capture correctable and uncorrectable (fatal and non-fatal) errors in transmit and receive. The provision to capture these error messages as interrupts also exists.

3.11.4 Byte-Swap Option

The PCIE RC AHB interface is configured as big-Endian. Depending on whether data is to be sent to the endpoint in little- or big-Endian format, PCIE RC software can add a byte-swap in slave data going into the PCIE core.

3.11.5 Request Sizes and Payloads

The PCIE RC supports:

- The maximum number of outstanding incoming non-posted requests is 32
- The maximum payload size is 128
- The maximum read the request size (AHB Master) is 128 bytes
- The burst size for master requests is 64 bytes (INCR)

3.12 USB 2.0 Interface

The USB controller supports a standard USB 2.0 host. In USB host mode, the QCA9563 can support the full number of devices/endpoints allowed in the USB 2.0 specification. It can be connected, either directly or through one or more hubs, at high-speed (480 Mbps) or full-speed (12 Mbps). The USB core acts as a master on the internal AHB bus, maximizing data transfer speeds with the system DDR memory. See Figure 3-10.

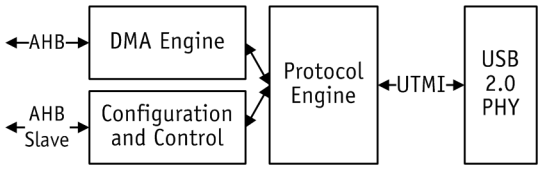


Figure 3-10 USB Interface

Table 3-10 describes the USB interface elements.

Table 3-10 USB Interface Elements

Name	Description
System Interface	The USB controller provides a AHB master interface for DMA transfer of descriptors and endpoint data between the System memory and the USB serial interface. QCA9563 CPU can control the USB controller operation through an AHB Slave interface. In Host Mode, the controller registers and data structures are compliant to Intel EHCI specifications. QCA9563 software must set the operation by writing into the CM bits of the USBMODE register.
Host Data Structure	The host data structures are used to communicate control, status, data and between software and the USB host controller. The data structure is compliant with EHCI specifications. A periodic frame list which is an array of pointers to a transfer list is used. There are asynchronous transfer lists for bulk and control data transfers and Isochronous Transfer list for Isochronous data transfers.
XCVR Interface	The USB Controller interfaces with an on-chip USB 2.0 PHY through the UTMI standard interface.

Table 3-11 shows the USB interface signals.

Table 3-11 USB Interface Elements

Name	Type	Description
USB_DP	IA/OA	USB D+ Signal
USB_DM	IA/OA	USB D– Signal

The QCA9563 has two USB 2.0 compliant host, that supports High-speed (480 Mbps), full speed (12Mbps) or Low speed (1.5 Mbps) clients. The USB core acts as a master on the internal AHB bus, thus maximizing data transfer speeds with the system DDR memory. The USB Host only interface supports all features of a compliant USB 2.0 host.

4 Radio Block

The transceiver of the QCA9563 solution consists of these major functional blocks:

- 3 x Receive chain

  Each chain = Radio + BB programmable gain filter
- 3 x Transmit chain

  Each chain = Radio + BB programmable gain filter
- Frequency synthesizer (SYNTH)
- Associated bias/control (BIAS)

See Figure 4-1.

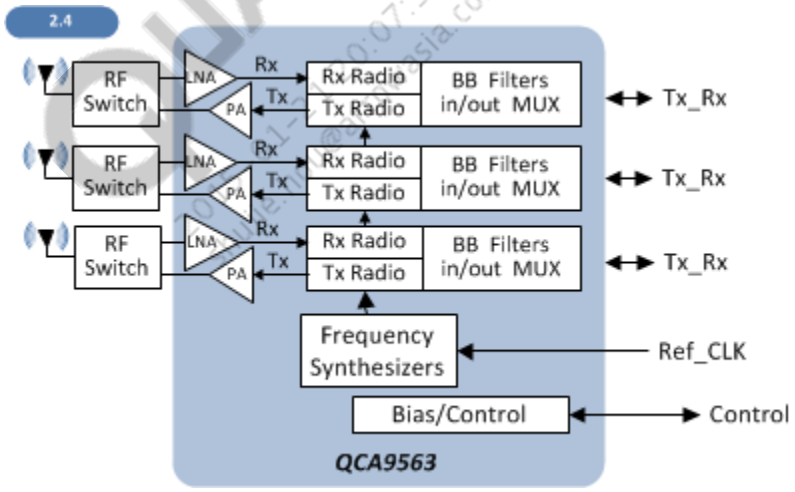


Figure 4-1 Radio Functional Block Diagram

4.1 Receiver (Rx) Block

The receiver converts an RF signal (with a 20 MHz or 40 MHz band) to baseband I and Q outputs. The dual band receiver operates in the 2.4 GHz band to support CCK and OFDM signals for 802.11b, 802.11g, and 802.11n.

The 2.4 GHz receiver implements a direct-conversion architecture and consists of a low noise amplifier (LNA), a pair of quadrature radio frequency (RF) mixers, and in-phase (I) and quadrature (Q) baseband programmable gain filter/amplifiers (PGA). The mixers convert the output of the on-chip LNA to baseband I and Q signals. The I and Q signals are low-pass filtered and amplified by a baseband programmable gain filter controlled by digital logic. The baseband signals are sent to the ADC within the MAC/Baseband processor.

The DC offset of the receive chain is reduced using multiple DACs controlled by the MAC/ Baseband processor. Additionally, the receive chain can be digitally powered down to conserve power.

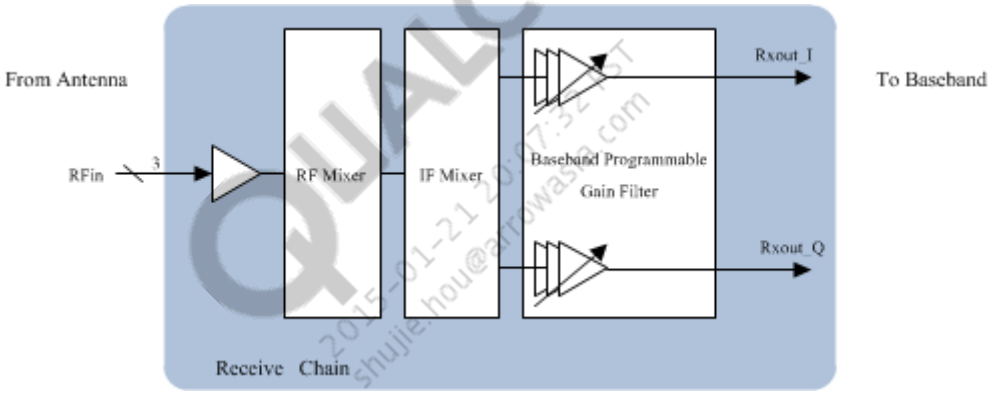


Figure 4-2 Radio Receive Chain Block Diagram

4.2 Transmitter (Tx) Block

The transmitter converts baseband I and Q inputs to 2.4 GHz RF outputs as shown in Figure 4-3. The inputs to the transmitter are current outputs of the I and Q DAC within the MAC/Baseband processor. These currents are low-pass filtered through an on-chip reconstruction filter to remove spectral images and out-of-band quantization noise.

The I and Q signals are converted to RF signals using an integrated up-conversion architecture.

For 2.4 GHz transmitter, the baseband I and Q signals are up-converted directly to RF using a pair of quadrature mixers. The up-converted RF signals are driven off-chip through a power amplifier.

The transmit chain can be digitally powered down to conserve power. To ensure that the FCC limits are observed and the output power stays close to the maximum allowed, the transmit output power is adjusted by a digitally programmed control loop at the start of each packet. The QCA9563 provides an open loop power control based on an on-chip temperature sensor.

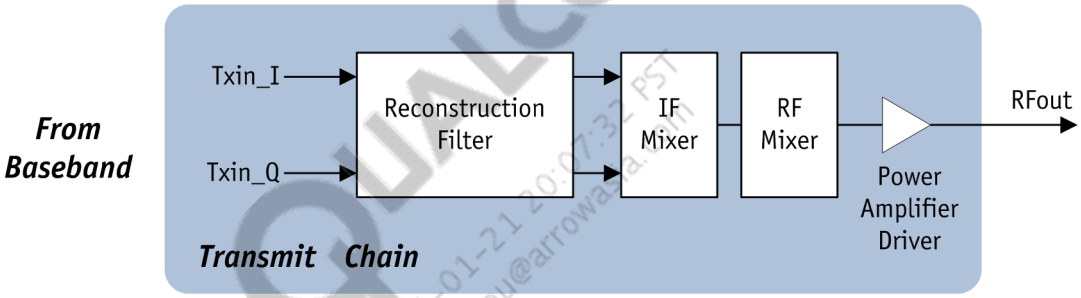


Figure 4-3 Radio Transmit Chain Block Diagram

4.3 Synthesizer (SYNTH) Block

The radio supports an on-chip synthesizer to generate local oscillator (LO) frequencies for the receiver and transmitter mixers. The synthesizer has the topology shown in Figure 4-4. The QCA9563 generates the reference input from a crystal for the synthesizer. An on-chip voltage controlled oscillator (VCO) provides the desired LO signal based on a phase locked loop.

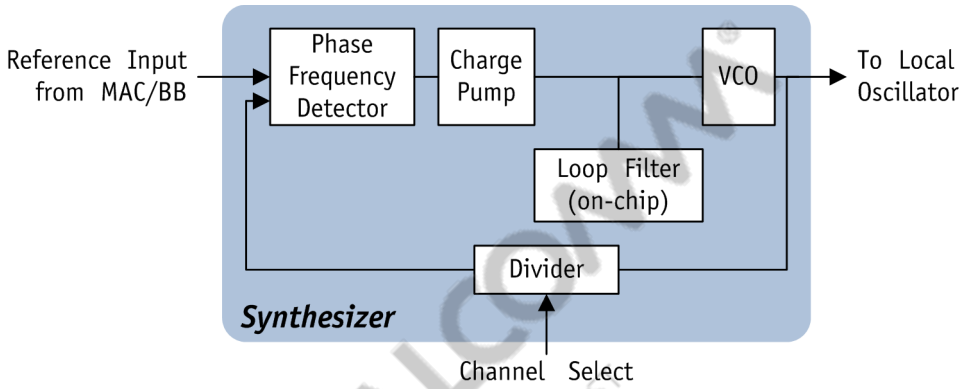


Figure 4-4 Radio Synthesizer Block Diagram

4.4 Bias/Control (BIAS) Block

The bias/control block provides the reference voltages and currents for all other circuit blocks (see Figure 4-5). An on-chip bandgap reference circuit provides the needed voltage and current references based on an external 6.19 KΩ ±1% resistor.

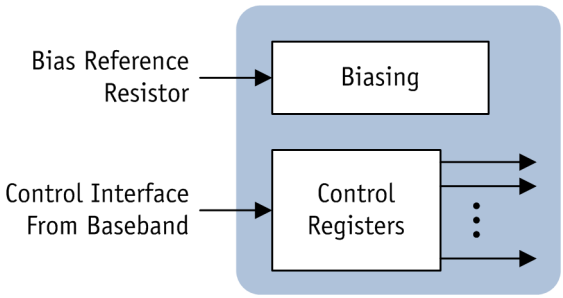


Figure 4-5 Bias/Control Block Diagram

5 WLAN Medium Access Control (MAC)

The WLAN MAC consists of the following major functional blocks: 10 queue control units (QCUs), 10 distributed coordination function (DCF) control units (DCUs), a single DMA Rx unit (DRU), and a single protocol control unit (PCU). See Figure 5-1.

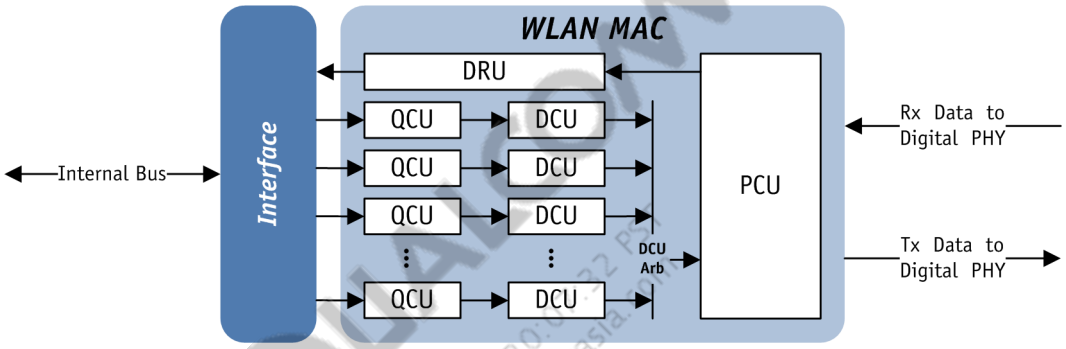


Figure 5-1 WLAN MAC Block Diagram

5.1 Overview

The WLAN MAC block supports full bus-mastering descriptor-based scatter/gather DMA. Frame transmission begins with the QCUs. QCUs manage the DMA of frame data and determines when a frame is available for transmission.

Each QCU targets exactly one DCU. Ready frames are passed from a QCU to its targeted DCU. The DCU manages the enhanced distributed coordination function (EDCF) channel access procedure on behalf of the QCUs associated with it.

Functionality of the WLAN MAC block includes:

- Tx frame data transfer from the DDR
- Rx frame data transfer the DDR
- Interrupt generation and reporting
- Sleep-mode sequencing
- Miscellaneous error and status reporting functions

Once the DCU gains access to the channel, it passes the frame to the PCU, which encrypts the frame and sends it to the baseband logic. The PCU handles both processing responses to the transmitted frame, and reporting the transmission attempt results to the DCU.

Frame reception begins in the PCU, which receives the incoming frame bitstream from the digital PHY. The PCU decrypts the frame and passes it to the DRU, which manages Rx descriptors and writes the incoming frame data and status.

5.2 Descriptor

The WLAN MAC is responsible for transferring frames between the DDR and the digital PHY. For all normal frame transmit/receive activity, the CPU provides a series of descriptors to the WLAN MAC, and the WLAN MAC then parses the descriptors and performs the required set of data transfers.

5.3 Descriptor Format

The transmit (Tx) descriptor format contains twenty-three 32-bit words and the receive (Rx) descriptor contains twelve 32-bit words.

A descriptor must be aligned on a 32-bit boundary in host memory, although best performance is achieved if the descriptor is aligned on a cache-line boundary. The MAC uses the final nine words of the Tx descriptor and the twelve words of the Rx descriptor to report status information back to the host.

See these tables for more information:

Table	Words	Description
Table 5-1	0–14	Tx descriptor format
Table 5-4	15–22	Tx descriptor format
Table 5-5	0–8	Tx descriptor status format
Table 5-6	0–11	Rx descriptor format

The Tx descriptor format is described in Table 5-1. With certain exceptions as noted, all Tx descriptor fields must be valid in the first descriptor of a non-aggregate frame. The fields for all following descriptors are ignored. For aggregate frames only the first descriptor of the first frame of the aggregate is valid. The fields for all following descriptors are ignored.

Table 5-1 Tx Descriptor Format: Words 0–14

Word	Bits	Name	Description
0	31:16	ATHEROS_ID	The unique Qualcomm Atheros identifier of 0x168C is used to visually identify the start of the descriptor.
	15	DESC_TX_RX	Indicates whether the descriptor is a transmit or receive descriptor. The value should be set to 1 indicating transmit.
	14	DESC_CTRL _STAT	Indicates whether the descriptor is a control or status descriptor. The value should be set to 1 indicating control descriptor.
	13:12	RES	Reserved
	11:8	TX_QCU_NUM	Tx QCU number Indicates which QCU this descriptor is part of.
	7:0	DESC_ LENGTH	Descriptor length Indicates the number of Dwords in this descriptor. The value should be set to 0x17 (23 Dwords).
1	31:0	LINK_PTR	Link pointer address Contains the 32-bit next descriptor pointer. Must be 32-bit aligned (bits [1:0] must be 0). A null value: (link_ptr= 0x0) is only allowed at the end of a non-aggregate or non-RIFS packet. If the packet is part of an aggregate or RIFS burst, a null is only allowed on the last descriptor of the last packet. A legal null value causes the QCU to stop. Must be valid for all descriptors.
2	31:0	BUF_PTR0	Data buffer pointer 0 Contains the 32-bits address of the first data buffer associated with this descriptor. A transmit data buffer may begin at any byte address. Must not be null (buf_ptr0 = 0x0) for all descriptors.
3	31:28	RES	Reserved

	27:16	BUF_LEN0	Data buffer length associated with data buffer pointer 0. Specifies the length, in bytes, of the data buffer associated with buf_ptr0. buf_len0 must not be 0. Note: This field must be valid for all descriptors.
			`case (header_length, qos packet) {`
			`  24, no : pad_length = 0;`
			`  24, yes: pad_length = 2;`
			`  30, no : pad_length = 2;`
			`  30, yes: pad_length = 0;`
			`}`
			`case (encrypt_type) {`
			`  wep  : icv_length = 4;`
			`  tkip nomic : icv_length = 4;`
			`  aes  : icv_length = 8;`
			`  tkip : icv_length = 12;`
			`  wapi : icv_length = 16;`
			`}`
			`fcs_length = 4;`
			`frame_length = buf_len0 + buf_len1 + buf_len2 + buf_len3 +`
			`  icv_length + fcs_length - pad_length`

	15:0	RES	Reserved
4	31:0	BUF_PTR1	Data buffer pointer 1 Contains the 32-bits address of the second data buffer associated with this descriptor. A transmit data buffer may begin at any byte address. Only valid if buf_ ptr0 is not null.

Table 5-1 Tx Descriptor Format: Words 0–14

Word	Bits	Name	Description
5	31:28	RES	Reserved
	27:16	BUF_LEN1	Data buffer length associated with data buffer pointer 1. buf_len1 can only be 0 if and only if buf_ptr1 is null. See buf_len0 for details.
	15:0	RES	Reserved
6	31:0	BUF_PTR2	Data buffer pointer 2 Contains the 32-bits address of the third data buffer associated with this descriptor. A transmit data buffer may begin at any byte address. Only valid if buf_ptr0 and buf_ptr1 are not null.
7	31:28	RES	Reserved
	27:16	BUF_LEN2	Data buffer length associated with data buffer pointer 2. buf_len2 can only be 0 if and only if buf_ptr2 is null. See buf_len0 for details.
	15:0	RES	Reserved
8	31:0	BUF_PTR3	Data buffer pointer 3 Contains the 32-bits address of the third data buffer associated with this descriptor. A Tx data buffer may begin at any byte address. Only valid if buf_ptr0, buf_ptr1, and buf_ptr2 are not null.
9	31:28	RES	Reserved
	27:16	BUF_LEN3	Data buffer length associated with data buffer pointer 2. buf_len2 can only be 0 if and only if buf_ptr3 is null. See buf_len0 for details.
	15:0	RES	Reserved
10	31:16	TX_DESC_ID	Tx descriptor sequence number Software will select a unique sequence number associated with this descriptor. This value is copied to the tx_desc_id in the transmit status.

	15:0	PTR_ CHECKSUM	Memory pointer checksum
			Verifies the integrity of the memory pointers/addresses in this descriptor. The equation looks like this:
			`checksum[31:0] = TXC[0]+TXC[1]+TXC[2]+TXC[3]+TXC[4]+`
			`TXC[5]+TXC[6]+TXC[7]+TXC[8]+TXC[9];`
			`ptr_checksum[15:0] = checksum[31:16] + checksum[15:0];`
			
			The carry bits above the MSB of the checksum or ptr_checksum will disappear.

Table 5-1 Tx Descriptor Format: Words 0–14

Word	Bits	Name	Description
11	31	CTS_ENABLE	Self-CTS enable Precedes the frame with CTS flag. If set, the PCU first sends a CTS before sending the frame described by the descriptor; used mainly for 802.11g frames to quiet legacy stations before sending a frame the legacy stations cannot interpret, even at the PHY level. At most only one of the rts_enable and cts_enable bits may be set; it is illegal to set both.
	30	DEST_INDEX _VALID	Destination index valid flag Specifies whether the contents of the DestIdx field are valid.
	29	INT_REQ	Interrupt request flag Set to one by the driver to request that the DMA engine generate an interrupt upon completion of the frame to which this descriptor belongs. Note: This field must be valid and identical for all descriptors of the frame. That is, all descriptors for the frame must have this flag set, or all descriptors for the frame must have this flag clear.
	28:25	RES	Reserved
	24	CLEAR_DEST _MASK	Clear destination mask bit flag If set, instructs the DCU to clear the destination mask bit at the index specified by the dest_index field.
	23	VEOL	Virtual end-of-list flag When set, indicates that the QCU should act (mostly) as if this descriptor had a null link_ptr, even though its link_ptr field may be non-null. Note: This field must be valid in the final descriptor of a frame and must be clear for all other descriptors of the frame.
	22	RTS_ENABLE	RTS enable If set, the PCU transmits the frame using the RTS/CTS protocol. If clear, the PCU transmits the frame without transmitting a RTS. At most only one of the rts_enable and cts_enable bits may be set; it is illegal to set both.
	21:16	TPC_0	TPC for Tx series 0. These bits pass unchanged to the baseband, where they control Tx power for the frame.
	15	CLEAR_ RETRY	Setting this bit disables the retry bit from being set in the Tx header on a frame retry; applies to both aggregate and non-aggregate frames.
11 (cont.)	14	LOW_RX_ CHAIN	When set to 1, indicates that switches the Rx chain mask to low power mode after transmitted this frame.
	13	FAST_ANT _MODE	Fast antenna mode If set to 0, this means that this Tx frame to use the omni antenna mechanism. if set to 1, then the opposite omni antenna should be used.
	12	VMF	Virtual more fragment If this bit is set, bursting is enabled for this frame. If there is no burst in progress, it will initiate a CTS protected burst if cts_enable is set. If there is a previous burst in progress, it ignores the cts_enable bit assuming that this burst is protected.
	11:0	FRAME_ LENGTH	Frame length Specifies the length, in bytes, of the entire MAC frame, including the FCS, IC, and ICV fields.

Table 5-1 Tx Descriptor Format: Words 0–14

<table>
<tr><th>Word</th><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="13">12</td><td>31</td><td>MORE_RIFS</td><td>More RIFS burst flag; When set, indicates that the current packet is not the last packet of an aggregate. All descriptors for all packets of a RIFS burst except the descriptors of the last packet must have this bit set. All descriptors of the last packet of a RIFS burst must have this bit clear.</td></tr>
<tr><td>30</td><td>IS_AGG</td><td>This packet is part of an aggregate flag. All descriptors of the all packets in an aggregate must have this bit set.</td></tr>
<tr><td>29</td><td>MORE_AGG</td><td>More aggregate flag; When set, indicates that the current packet is not the last packet of an aggregate. All descriptors for all packets of an aggregate except the descriptors of the last packet must have this bit set. All descriptors of the last packet of an aggregate must have this bit clear.</td></tr>
<tr><td>28</td><td>EXT_AND_ CTL</td><td>Extension and control channel enable
Only four combinations are allowed; otherwise desc_config_error asserts. When neither ext_only nor ext_and_ctl are set, the RTS/CTS and data frame is sent based on the bandwidth: HT20 when 20_40 is set to 0 and HT40 shared when 20_40 is set to 1 (RTS/CTS frames are sent at in HT40 duplicate mode if 20_40 is set to 1). When ext_and_ctl is set the RTS/CTS and data frame is sent at HT40 duplicate. When ext_only is set the RTS/CTS and data frame is sent out in HT20 extension channel mode.
<table>
<tr><th>ETX_AND_CTL</th><th>20_40</th><th>DATA</th><th>RTS/CTS</th></tr>
<tr><td>0</td><td>0</td><td>HT20 Control</td><td>HT20 Control</td></tr>
<tr><td>0</td><td>1</td><td>HT40 Shared</td><td>HT40 Duplicate</td></tr>
<tr><td>1</td><td>1</td><td>HT40 Duplicate</td><td>HT40 Duplicate</td></tr>
</table></td></tr>
<tr><td>27</td><td>RES</td><td>Reserved</td></tr>
<tr><td>26</td><td>CORRUPT_ FCS</td><td>Corrupt packet FCS; When set, the FCS of the packet will be inverted to guarantee the transmitted FCS is incorrect.</td></tr>
<tr><td>25</td><td>RES</td><td>Reserved</td></tr>
<tr><td>24</td><td>NO_ACK</td><td>No ACK flag; When set, indicates to the PCU that it should not expect to receive (and should not wait for) an ACK for the frame. Must be set for any frame that has the 802.11 NoACK bit set in the QoS field. Also must be set for all other frame types (such as beacons and other broadcast/multicast frames) that do not receive ACKs.</td></tr>
<tr><td>23:20</td><td>FRAME_TYPE</td><td>Frame type indication; indicates what type of frame is being sent:
<table>
<tr><td>15:5</td><td>Reserved</td></tr>
<tr><td>4</td><td>Probe response</td></tr>
<tr><td>3</td><td>Beacon</td></tr>
<tr><td>2</td><td>PS-Poll</td></tr>
<tr><td>1</td><td>ATIM</td></tr>
<tr><td>0</td><td>Frame type, other than the types listed in [15:1]</td></tr>
</table></td></tr>
<tr><td rowspan="4">12 (cont.)</td><td>19:13</td><td>DEST_INDEX</td><td>Destination table index
Specifies an index into an on-chip table of per-destination information. The PCU fetches the encryption key from the specified index in this table and uses this key to encrypt the frame. The DMA logic uses the index to maintain per-destination transmit filtering status and other related information.</td></tr>
<tr><td>12</td><td>MORE</td><td>More descriptors in this frame flag
Set to one by the driver to indicate that there are additional descriptors (that is, DMA fragments) in the current frame. The last descriptor of a packet must have this bit set to 0. Note: This field must be valid for all descriptors.</td></tr>
<tr><td>11:9</td><td>PA</td><td>Pre-distortion chain mask</td></tr>
<tr><td>8:0</td><td>RES</td><td>Reserved</td></tr>
</table>

Table 5-1 Tx Descriptor Format: Words 0–14

Word	Bits	Name	Description
13	31:28	TX_TRIES3	Number of frame data exchange attempts permitted for Tx series 3. A value of zero means skip this transmission series.
	27:24	TX_TRIES2	Number of frame data exchange attempts permitted for Tx series 2. A value of zero means skip this transmission series.
	23:20	TX_TRIES1	Number of frame data exchange attempts permitted for Tx series 1. A value of zero means skip this transmission series.
	19:16	TX_TRIES0	Number of frame data exchange attempts permitted for Tx series 0. A frame data exchange attempt means a transmission attempt in which the actual frame is sent on the air (in contrast to the case in which the frame has RTS enabled and the RTS fails to receive a CTS. In this case, the actual frame is not sent on the air, so this does not count as a frame data exchange attempt. Unlike TX_TRIES1...3, a value of zero is illegal for TX_TRIES0 field.
	15	DUR_ UPDATE_EN	Frame duration update control. If set, the MAC updates (overwrites) the duration field in the frame based on the current transmit rate. If clear, the MAC does not alter the contents of the frame duration field.
	14:0	BURST _DURATION	Burst duration value in usec. If this frame is not part of a burst or the last frame in a burst, this value should be zero. In a burst, this value is the amount of time to be reserved (via NAV) after the completion of the current transmit packet sequence (after the ACK if applicable).
14	31:24	TX_RATE3	Tx rate for transmission series 3; see Table 5-2 and Table 5-3
	23:16	TX_RATE2	Tx rate for transmission series 2; see Table 5-2 and Table 5-3
	15:8	TX_RATE1	Tx rate for transmission series 1; see Table 5-2 and Table 5-3
	7:0	TX_RATE0	Tx rate for transmission series 0; see Table 5-2 and Table 5-3

Table 5-2 MAC Rate Encodings

MAC Rate Encoding	Protocol
0x01	Reserved
0x02	
0x03	
0x06	
0x07	
0x8	OFDM_48Mb
0x9	OFDM_24Mb
0xA	OFDM_12Mb
0xB	OFDM_6Mb
0xC	OFDM_54Mb
0xD	OFDM_36Mb
0xE	OFDM_18Mb
0xF	OFDM_9Mb
0x18	CCK_11Mb_L
0x19	CCK_5_5Mb_L
0x1A	CCK_2Mb_L
0x1B	CCK_1Mb_L
0x1C	CCK_11Mb_S
0x1D	CCK_5_5Mb_S
0x1E	CCK_2Mb_S

Table 5-3 Tx Rates[1]

Rate	Desc	Stream	HT20; GI= 0 Mbps	HT20; GI = 1 Mbps	HT40; GI= 0 Mbps	HT40; GI= 1 Mbps
0x80	MCS 0	1	6.5	7.2	13.5	15
0x81	MCS 1	1	13	14.4	27	30
0x82	MCS 2	1	19.5	21.7	40.5	45
0x83	MCS 3	1	26	28.9	54	60
0x84	MCS 4	1	39	43.3	81	90
0x85	MCS 5	1	52	57.8	108	120
0x86	MCS 6	1	58.5	65.0	121.5	135
0x87	MCS 7	1	65	72.2	135	150
0x88	MCS 8	2	13	14.4	27	30
0x89	MCS 9	2	26	28.9	54	60
0x8A	MCS 10	2	39	43.3	81	90
0x8B	MCS 11	2	52	57.8	108	120
0x8C	MCS 12	2	78	86.7	162	180
0x8D	MCS 13	2	104	115.6	216	240
0x8E	MCS 14	2	117	130.0	243	270
0x8F	MCS 15	2	130	144.4	270	300
0x90	MCS 16	3	19.5	21.6	40.5	45
0x91	MCS 17	3	39	43.2	81	90
0x92	MCS 18	3	58.8	65.1	121.5	135
0x93	MCS 19	3	78	86.7	162	180
0x94	MCS 20	3	117	129.9	243	270
0x95	MCS 21	3	156	173.4	324	360
0x96	MCS 22	3	175.5	195	364.5	405
0x97	MCS 23	3	195	216.6	405	450

1. All rates not listed are reserved. Note that for short guard interval (GI=1), HT20 mode is allowed.

The Tx descriptor format for words 15 through 22 is described in Table 5-4.

Table 5-4 DMA Tx Descriptor Format for Words 15–22

Word	Bits	Name	Description	
15	31	RTS_CTS _QUAL1	Qualifies rts_enable or cts_enable in the Tx descriptor for Tx series 1	
			1	Default behavior with respect to rts_enable and cts_enable
	30:16	PACKET _DURATION1	Packet duration 1 (in μs); Duration of the actual Tx frame associated with TXRate1. This time does not include RTS, CTS, ACK, or any associated SIFS.	
	15	RTS_CTS _QUAL0	Qualifies rts_enable or cts_enable in the Tx descriptor for Tx series 0	
			1	Default behavior with respect to rts_enable and cts_enable
	14:0	PACKET _DURATION0	Packet duration 0 (in μs); Duration of the actual Tx frame associated with TXRate0. This time does not include RTS, CTS, ACK, or any associated SIFS.	
16	31	RTS_CTS _QUAL3	Qualifies rts_enable or cts_enable in the Tx descriptor for Tx series 3	
			1	Default behavior with respect to rts_enable and cts_enable
	30:16	PACKET _DURATION3	Packet duration 3 (in μs); Duration of the actual Tx frame associated with TXRate3. This time does not include RTS, CTS, ACK, or any associated SIFS.	
	15	RTS_CTS _QUAL2	Qualifies rts_enable or cts_enable in the Tx descriptor for Tx series 2	
			1	Default behavior with respect to rts_enable and cts_enable
	14:0	PACKET _DURATION2	Packet duration 2 (in μs); Duration of the actual Tx frame associated with TXRate2. This time does not include RTS, CTS, ACK, or any associated SIFS.	

Table 5-4 DMA Tx Descriptor Format for Words 15–22 (cont.)

Word	Bits	Name	Description	
17	31	RES	Reserved	
	30	CALIBRATING	Calibrating indication; causes the BB to apply the correct MCSD PPDU, which is used for radio calibration.	
	29	DC_AP _STA_SEL	Select for remaining the TBTT between TSF and TSF2, where 0 is from TSF and 1 is from TSF2. Should be used only when both ap_sta_enable and txop_tbtt_ limit_enable are enabled.	
	28:26	ENCRYPT_TYPE	Encryption type; DMA engine must add the number of necessary extra Dwords at the end of a packet to account for the encryption ICV generated by hardware. The encrypt type fields must be valid for all descriptors.	
			0	None; 0 pad bytes
			1	WEP or TKIP (no MIC); 4 pad bytes
			2	AES; 8 pad bytes
			3	TKIP; 12 pad bytes
			4	WAPI; 16 pad bytes
			7:5	Reserved
	25:18	PAD_DELIM	Pad delimiters; Between each packet of an A-MPDU aggregate the hardware will insert a start delimiter which includes the length of the next frame. Sometimes hardware on the transmitter or receiver requires some extra time between packets which can be satisfied by inserting zero length delimiters. This field indicates the number of extra zero length delimiters to add.	
	17:16	RES	Reserved	

	15:0	AGG_LENGTH	Aggregate (A-MPDU) length; the aggregate length is the number of bytes of the entire aggregate. This length should be computed as:
			`delimiters = start_delim + pad_delim;`
			`frame_pad = (frame_length % 4) ? (4 - (frame_ length % 4)) : 0`
			`agg_length = sum_of_all (frame_length + frame_pad + 4 * delimiters)`
			
			For the last packet of an aggregate the FRAME_PAD = 0 and delimiter= 0, frame_pad aligns to the next delimiter to be Dword aligned. Each delimiter is 4 bytes long. PAD_DELIM is the number of zero-length delimiters used to introduce an extra time gap between packets. START_DELIM is always 1 and includes the length of the next packet in the aggregate.	

Table 5-4 DMA Tx Descriptor Format for Words 15–22 (cont.)

Word	Bits	Name	Description	
18	31:28	STBC	STBC settings for all four series. If bit [0] is set, STBC is enabled for Tx series 0...3. Only supported for single stream rates, so only the lower bit is set.	
	27:20	RTS_CTS_RATE	RTS or self-CTS rate selection. Specifies the rate the RTS sends at if rts_enable is set, or self CTS sends at if cts_enable is set; see Table 5-3.	
	19:17	CHAIN_SEL_3	Chain select for Tx series 3. 1 and 3 are the only valid values.	
	16	GI_3	Guard interval control for Tx series 3	
			0	Normal guard interval
			1	Short guard interval
	15	20_40_3	20_40 control for Tx series 3	
			0	HT20 Tx packet
			1	HT40 Tx packet
	14:12	CHAIN_SEL_2	Chain select for Tx series 2. 1 and 3 are the only valid values.	
	11	GI_2	Guard interval control for Tx series 2	
	10	20_40_2	20_40 control for Tx series 2	
	9:7	CHAIN_SEL_1	Chain select for Tx series 1. 1 and 3 are the only valid values.	
	6	GI_1	Guard interval control for Tx series 1	
	5	20_40_1	20_40 control for Tx series 1	
	4:2	CHAIN_SEL_0	Chain select for Tx series 0. 1 and 3 are the only valid values.	
	1	GI_0	Guard interval control for Tx series 0	
	0	20_40_0	20_40 control for Tx series 0	

Table 5-4 DMA Tx Descriptor Format for Words 15–22 (cont.)

Word	Bits	Name	Description	
19	31:30	NESS_0	Number of Extension Spatial Streams (NESS) field of HT-SIG for Tx series 0. This setting is valid when the Tx rate is HT rate.	
			0	No Extension HTLTF is transmitting PPDU
			1	One Extension HTLTF is transmitting PPDU
	29	NOT _SOUNDING	Not sounding HT-SIG field; sends sounding PPDU in explicit feedback as BF. If rts_enable is set to 1, this field affects RTS only, not the next data frame.	
			0	The PPDU is a sounding PPDU
			1	The PPDU is not a sounding PPDU
	28	RTS_HTC_TRQ	Sounding request of RTS frame; available when rts_enable is set to 1.	
			0	The responder is not requested to transmit a sounding PPDU
			1	Request the responder to transmit a sounding PPDU
	27	RTS_HTC_MRQ	MCS request of RTS frame; available when rts_enable is set to 1	
			0	No MCS feedback is requested
			1	MCS feedback is requested
	26:24	RTS_HTC_MSI	MCS Request Sequence Identifier (MSI) of RTS frame	
			0	Reserved
			1	Contains a sequence number (0–6) to identify the specific request
	23:0	ANTENNA_0	Antenna switch for Tx series 0	
20	31:30	NESS_1	NESS field of HT-SIG for Tx series 1. This setting is valid when the transmission rate is HT rate.	
			0	No Extension HTLTF is transmitting PPDU
			1	One Extension HTLTF is transmitting PPDU
	29:24	TPC_1	TPC for Tx series 1. These bits pass unchanged to the baseband, where they control Tx power for the frame.	
	23:0	ANTENNA_1	Antenna switch for Tx series 1	
21	31:30	NESS_2	NESS field of HT-SIG for Tx series 2. This setting is valid when the transmission rate is HT rate.	
			0	No Extension HTLTF is transmitting PPDU
			1	One Extension HTLTF is transmitting PPDU
	29:24	TPC_2	TPC for Tx series 2. These bits pass unchanged to the baseband, where they control Tx power for the frame.	
	23:0	ANTENNA_2	Antenna switch for Tx series 2	
22	31:30	NESS_3	NESS field of HT-SIG for Tx series 3. This setting is valid when the transmission rate is HT rate.	
			0	No Extension HTLTF is transmitting PPDU
			1	One Extension HTLTF is transmitting PPDU
	29:24	TPC_3	TPC for Tx series 3. These bits pass unchanged to the baseband, where they control Tx power for the frame.	
	23:0	ANTENNA_3	Antenna switch for Tx series 3	

The Tx descriptor status format for words 0 through 8 is described in Table 5-5.

The words status is only considered valid when the done bit is set.

Table 5-5 Tx Descriptor Status Format: Words 0–8

Word	Bits	Name	Description
0	31:16	ATHEROS_ID	The unique Qualcomm Atheros identifier of 0x168C is used to visually identify the start of the descriptor.
	15	DESC_TX_RX	Indicates whether the descriptor is a transmit or receive descriptor. The value should be set to 1 indicating transmit.
	14	DESC_CTRL _STAT	Indicates whether the descriptor is a control or status descriptor. The value should be set to 0 indicating status descriptor.
	13:12	RES	Reserved
	11:8	TX_QCU_NUM	Tx QCU number Indicates which QCU this descriptor is part of.
	7:0	DESC_LENGTH	Descriptor length Indicates the number of Dwords in this descriptor. The value should be set to 0x9 (9 Dwords).
1	31:16	TX_DESC_ID	Tx descriptor sequence number Software will select a unique sequence number associated with this descriptor. This value is copied to the tx_desc_id in the Tx status.
	15:0	RES	Reserved
2	31	RES	Reserved
	30	BA_STATUS	Block ACK status If set, this bit indicates that the BA_BITMAP values are valid.
	29:16	RES	Reserved
	15:8	ACK_RSSI_ ANT01	Rx ACK signal strength indicator of control channel chain 1 A value of 0x80 (–128) indicates an invalid number.
	7:0	ACK_RSSI_ ANT00	Rx ACK signal strength indicator of control channel chain 0 A value of 0x80 (–128) indicates an invalid number.

Table 5-5 Tx Descriptor Status Format: Words 0–8

Word	Bits	Name	Description
3	31:20	RES	Reserved
	19	TX_TIMER _EXPIRED	Tx timer expired. This bit is set when the Tx frame is taking longer to send to the baseband than is allowed based on the TX_TIMER register. Some regulatory domains require that Tx packets may not exceed a certain amount of transmit time.
	18	RES	Reserved
	17	TX_DATA_ UNDERRUN_ERR	Tx data underrun error These error conditions occur on aggregate frames when the underrun condition happens while the MAC is sending the data portion of the frame or delimiters.
	16	TX_DELMTR _UNDERRUN_ ERR	Tx delimiter underrun error These error conditions occur on aggregate frames when the underrun conditions happens while the MAC is sending delimiters.
	15:12	VIRTUAL_ RETRY_CNT	Virtual collision count Reports the number of virtual collisions that occurred before transmission of the frame ended. The counter value saturates at 0xF. A virtual collision refers to the case, as described in the 802.11e QoS specification, in which two or more output queues are contending for a TXOP simultaneously. In such cases, all lower-priority output queues experience a virtual collision in which the frame is treated as if it had been sent on the air but failed to receive an ACK.
	11:8	DATA_FAIL_CNT	Data failure count Reports the number of times the actual frame (as opposed to the RTS) was sent but no ACK was received for the final transmission series (see the final_tx_index field).
	7:4	RTS_FAIL_CNT	RTS failure count Reports the number of times an RTS was sent but no CTS was received for the final transmission series (see the final_tx_index field). For frames that have the rts_enable bit clear, this count always will be zero. Note that this count is incremented only when the RTS/CTS exchange fails. In particular, this count is not incremented if the RTS/CTS exchange succeeds but the frame itself fails because no ACK was received.
	3	FILTERED	Frame transmission filter indication If set, indicates that the frame was not transmitted because the corresponding destination mask bit was set when the frame reached the PCU or if the frame violated TXOP on the first packet of a burst. Valid only if frm_xmit_ok is clear.
	2	FIFO_UNDERRUN	Tx FIFO underrun flag If set, transmission of the frame failed because the DMA engine was not able to supply the PCU with data as quickly as the baseband was requesting transmit data. Only valid for non-aggregate or non-RIFS underrun conditions unless the underrun occurred on the first packet of the aggregate or RIFS burst. See also the description for tx_delmtr_underrun_err and tx_data_underrun_err. Valid only if frm_xmit_ok is clear.
	1	EXCESSIVE _RETRIES	Excessive tries flag If set, transmission of the frame failed because the try limit was reached before the frame transmitted. Valid only if frm_xmit_ok is clear.
	0	frm_xmit_ok	Frame transmission success flag If set, the frame was transmitted successfully. If clear, no ACK or BA was received successfully.

Table 5-5 Tx Descriptor Status Format: Words 0–8

Word	Bits	Name	Description
4	31:0	SEND _TIMESTAMP	Timestamp at start of transmit A snapshot of the lower 32 bits of the PCU timestamp (TSF value). This field can be used to aid the software driver in implementing requirements associated with the aMaxTransmitMSDULifetime MAC attribute. The transmit timestamp is sampled on the rising of tx_frame signal which goes from the MAC to the baseband. This value corresponds to the last attempt at packet transmission not the first attempt.
5	31:0	BA_BITMAP_0-31	Block ACK bitmap 0 to 31 These bits are the values from the block ACK received after the successful transmission of an aggregate frame. If set, bit [0] represents the successful reception of the packet with the sequence number matching the seq_num value.
6	31:0	BA_BITMAP_32-63	Block ACK bitmap 32 to 63 These bits are the values from the block ACK received after the successful transmission of an aggregate frame. If set, bit [32] represents the successful reception of the packet with the sequence number matching the seq_num value + 32.
7	31:24	ACK_RSSI _COMBINED	Rx ACK signal strength indicator of combination of all active chains on the control and extension channels. The value of 0x80 (–128) is used to indicate an invalid number.
	23:16	RES	Reserved
	15:8	ACK_RSSI_ANT11	Rx ACK signal strength indicator of control channel chain 1 A value of 0x80 (–128) indicates an invalid number.
	7:0	ACK_RSSI_ ANT10	Rx ACK signal strength indicator of control channel chain 0 A value of 0x80 (–128) indicates an invalid number.
8	31:28	TID	Traffic Identifier (TID) of block ACK Indicates the TID of the response block ACK. This field is only valid on the last descriptor of the last packet of an aggregate.
	27:26	RES	Reserved
	25	PWR_MGMT	Power management state Indicates the value of the PwrMgt bit in the frame control field of the response ACK frame.
	24:23	RES	Reserved
	22:21	final_tx_index	Final transmission attempt series index Specifies the number of the Tx series that caused frame transmission to terminate.
	20:18	RES	Reserved
	17	TXOP_ EXCEEDED	TXOP has been exceeded Indicates that this transmit frame had to be filtered because the amount of time to transmit this packet sequence would exceeded the TXOP limit. This should only occur when software programs the TXOP limit improperly.
	16:13	RES	Reserved

Table 5-5 Tx Descriptor Status Format: Words 0–8

Word	Bits	Name	Description
8 (Cont.)	12:1	seq_num	The starting sequence number is the value of the Block ACK Starting Sequence Control field in the response Block ACK. Only consulted if the Tx frame was an aggregate.
	0	DONE	Descriptor completion flag Set to one by the DMA engine when it has finished processing the descriptor and has updated the status information. Valid only for the final descriptor of a non-aggregate frame, regardless of the state of the FrTxOK flag. For an aggregate frame it is valid for only the final descriptor of the final packet of an aggregate. The driver is responsible for tracking what descriptors are associated with a frame. When the DMA engine sets the done flag in the final descriptor of a frame, the driver must be able to determine what other descriptors belong to the same frame and thus also have been consumed.

Words 0, and 2 are valid for all descriptors. Words 0, 2, and 11 is valid for the last descriptor of each packets. Words 0–11 are valid for the last descriptor of an aggregate or last descriptor of a stand-alone packet. Additional validity qualifiers are described individually. See Table 5-6.

Table 5-6 DMA Rx Descriptor Format for Words 0–11

Word	Bits	Name	Description	
0	31:16	ATHEROS_ID	The unique Atheros identifier of 0x168C is used to visually identify the start of the descriptor.	
	15	DESC_TX_RX	Indicates whether the descriptor is a transmit or receive descriptor. The value should be set to 1 indicating transmit.	
	14	DESC_CTRL_ STAT	Indicates whether the descriptor is a control or status descriptor. The value should be set to 1 indicating status descriptor.	
	13:9	RES	Reserved	
	8	RX_PRIORITY	0	Low priority queue
			1	High priority queue
	7:0	DESC_LENGTH	Descriptor length Indicates the number of Dwords in this descriptor. The value should be set to 0x9 (9 Dwords).	
1	31:24	RX_RATE	Rx rate indication Indicates the rate at which this frame was transmitted from the source. Encodings match those used for the tx_rate*' field in word 5 of the Tx descriptor. Valid only if the frame_rx_ok flag is set or if the frame_rx_ok flag is clear and the phy_error flag is clear.	
	23:16	RES	Reserved	
	15:8	RSSI_ANT01	Received signal strength indicator of control channel chain 1 A value of 0x80 (–128) indicates an invalid number.	
	7:0	RSSI_ANT00	Received signal strength indicator of control channel chain 0 A value of 0x80 (–128) indicates an invalid number.	

Table 5-6 DMA Rx Descriptor Format for Words 0–11

Word	Bits	Name	Description
2	31:23	RES	Reserved
	22	HW_UPLOAD _DATA	The upload data is valid only when the field hw_upload_data_valid at RXS 4 bit [7] is set. See RXS 11 bit [26:25] hw_upload_data_type to know which data type is uploaded. Valid for all descriptors.
	21:14	NUM_DELIM	Number of zero length pad delimiters after current packet This field does not include the start delimiter which is required between each packet in an aggregate. This field is only valid for aggregate packets except for the last packet of an aggregate.
	13	RES	Reserved
	12	MORE	More descriptors in this frame flag If set, then this is not the final descriptor of the frame. If clear, then this descriptor is the final one of the frame. Valid for all descriptors.
	11:0	DATA_LEN	Received data length Specifies the length, in bytes, of the data actually received into the data buffer associated with this descriptor. The actual received data length will be between zero and the total size of the data buffer, as specified originally in this field (see the description for the buf_len field). Valid for all descriptors. See “Data Buffer Length (DATABUF)” on page 192.
3	31:0	RCV _TIMESTAMP	A snapshot of the PCU timestamp (TSF value), expressed in μs (that is, bits [31:0] of the PCU 64-bit TSF). Intended for packet logging and packet sniffing. The timestamp is sampled on the rising edge of rx_clear, which goes from the baseband to the MAC.
4	31:8	RES	Reserved
	7	HW_UPLOAD _DATA_VALID	Specifies whether the contents of the hardware upload data are valid
	6:5	NESS	Receive packet NESS field Shows the number of Rx extension spatial steams.
	4	NOT _SOUNDING	Rx packet not sounding flag If this value is clear, then the Rx frame is a sounding PPDU. If this value is set, the receive frame is not a sounding PPDU.
	3	STBC	Rx packet STBC indicator If this value is set then the baseband has received an STBC frames as indicated in the HT_PLCP.
	2	DUPLICATE	Rx packet duplicate indicator If this value is set, the baseband has determined that this packet is a duplicate packet.
	1	20_40	Rx packet 20 or 40 MHz bandwidth indicator If this value is clear, then the receive frame was a HT20 packet (20 MHz bandwidth). If this value is set, then the receive frame was a HT40 packet (40 MHz bandwidth).
	0	GI	Rx packet guard interval If this value is clear, then the Rx frame used a long guard interval. If this value is set, the Rx frame used a short guard interval.

Table 5-6 DMA Rx Descriptor Format for Words 0–11

Word	Bits	Name	Description			
5	31:24	RX_COMBINED	Receive signal strength indicator of combination of all active chains on the control and extension channels. The value of 0x80 (–128) is used to indicate an invalid number.			
	23:16	RES	Reserved			
	15:8	RSSI_ANT11	Received signal strength indicator of extension channel chain 1 A value of 0x80 (–128) indicates an invalid number.			
	7:0	RSSI_ANT10	Received signal strength indicator of extension channel chain 0 A value of 0x80 (–128) indicates an invalid number.			
6	31:0	EVM0	Rx packet error vector magnitude 0			
			Bits Mode	**HT20 Mode**	**HT40 Mode**	**Diagnostic**
			evm0[31:24]	pilot1_str0	pilot1_str0	legacy_plcp_byte_1
			evm0[23:16]	RES	RES	legacy_plcp_byte_2
			evm0[15:8]	pilot0_str1	pilot0_str1	legacy_plcp_byte_3
			evm0[7:0]	pilot0_str0	pilot0_str0	service_byte_1
7	31:0	EVM1	Rx packet error vector magnitude 1			
			Bits Mode	**HT20 Mode**	**HT40 Mode**	**Diagnostic**
			evm1[31:24]	pilot2_str1	pilot2_str1	service_byte_2
			evm1[23:16]	pilot2_str0	pilot2_str0	ht_plcp_byte_1
			evm1[15:8]	RES	RES	ht_plcp_byte_2
			evm1[7:0]	pilot1_str1	pilot1_str1	ht_plcp_byte_3
8	31:0	EVM2	Rx packet error vector magnitude 2			
			Bits Mode	**HT20 Mode**	**HT40 Mode**	**Diagnostic**
			evm2[31:24]	RES	RES	service_byte_4
			evm2[23:16]	pilot3_str1	pilot3_str1	ht_plcp_byte_5
			evm2[15:8]	pilot3_str0	pilot3_str0	ht_plcp_byte_6
			evm2[7:0]	RES	RES	0x0
9	31:0	EVM3	Rx packet error vector magnitude 3			
			Bits Mode	**HT20 Mode**	**HT40 Mode**	**Diagnostic**
			evm3[31:24]	0x80	pilot5_str0	0x0
			evm3[23:16]	0x80	RES	0x0
			evm3[15:8]	0x80	pilot4_str1	0x0
			evm3[7:0]	0x80	pilot4_str0	0x0
10	31:16	RES	Reserved			
	15:0	EVM4	Rx packet error vector magnitude 4			
			Bits Mode	**HT20 Mode**	**HT40 Mode**	**Diagnostic**
			evm4[15:8]	0x80	RES	0x0
			evm4[7:0]	0x80	pilot4_str1	0x0

Table 5-6 DMA Rx Descriptor Format for Words 0–11

<table>
<tr><th>Word</th><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td rowspan="15">11</td><td>31</td><td>KEY_MISS</td><td>Key cache miss indication
When set, indicates that the PCU could not locate a valid decryption key for the frame. Valid only if the frame_rx_ok flag is clear.</td></tr>
<tr><td>30</td><td>RES</td><td>Reserved</td></tr>
<tr><td>29</td><td>FIRST_AGG</td><td>First packet of aggregate
If set, indicates that this packet is the first packet of an aggregate.</td></tr>
<tr><td>28</td><td>HI_RX_CHAIN</td><td>If set indicates that the Rx chain control in high power mode.</td></tr>
<tr><td>27</td><td>RES</td><td>Reserved</td></tr>
<tr><td>26:25</td><td>HW_UPLOAD_
DATA_TYPE</td><td>Indicates the hardware upload data (H, V, or CV). The upload data is valid only when the field hw_upload_data_valid at RXS 4 bit [7] is set:
01 Upload is H
10 Upload is V
11 Upload is CV
Request report:
<table>
<tr><th>regs_config</th><th>Request CSI</th><th>Request V/CV</th></tr>
<tr><td>{0,0,x}</td><td>HW upload H</td><td>HW upload V/CV</td></tr>
<tr><td>{0,1,x}</td><td>HW upload H</td><td>HW upload H</td></tr>
</table>
If regs_config is {1,x,0}, it means hardware supports immediate response even if it does not need to respond to ACK. Hardware will upload H only when the request report is CSI.
If regs_config is {1,0,1}, it means HW support immediate response but hardware will upload H/V/CV base on request report for delay response if hardware does not need to respond to ACK.
Request Report:
<table>
<tr><th>regs_config</th><th>Request CSI</th><th>Request V/CV</th></tr>
<tr><td>{0,0,x}</td><td>HW upload H</td><td>HW upload V/CV</td></tr>
<tr><td>{0,1,x}</td><td>HW upload H</td><td>HW upload H</td></tr>
</table>
If regs_config is {1,1,1}, the hardware supports immediate response but hardware will only uploads H for a delay response if it does not need to respond to ACK.
For RTS, hardware only supports a delay response and will upload H, V, or CV to software.</td></tr>
<tr><td>24:19</td><td>RES</td><td>Reserved</td></tr>
<tr><td>18</td><td>POST_DELIM
_CRC_ERR</td><td>Delimiter CRC error is detected after this current frame
Only occurs when the start delimiter of the last frame in an aggregate is bad.</td></tr>
<tr><td>17</td><td>AGGREGATE</td><td>Aggregate flag
If set, indicates that this packet is part of an aggregate.</td></tr>
<tr><td>16</td><td>MORE_AGG</td><td>More aggregate flag
Set to 1 in all packets of an aggregate that have another packet of the current aggregate to follow. If clear, indicates that this packet is the last one of an aggregate.</td></tr>
</table>

Table 5-6 DMA Rx Descriptor Format for Words 0–11

Word	Bits	Name	Description
11 (Cont.)	15:9	key_idx	If the FrRxOK bit is set, then this field contains the decryption key table index. If KEY_IDX_VALID is set, then this field specifies the index at which the PCU located the frame's destination address in its on-chip decryption key table. If key_idx_VALID is clear, the value of this field is undefined. If the FrRxOK bit is clear and the PHYErr bit is set, then this field contains bits [7:1] of the PHY error code.
	8	KEY_IDX_VALID	If frame_rx_ok is set, this field contains the decryption key table index valid flag. If set, indicates that the PCU successfully located the frame's source address in its on-chip key table and that the key_idx field reflects the table index at which the destination address was found. If clear, indicates that PCU failed to locate the destination address in the key table and that the contents of key_idx field are undefined. If the frame_rx_ok bit is clear and the phy_error bit is set, then this field contains bit [0] of the PHY error code.
	7	ASPD_TRIG	Received APSD trigger frame The received frame matched the profile of an APSD trigger frame.
	6	PRE_DELIM_CRC_ERR	Delimiter CRC error detected before this current frame. May indicate that an entire packet may have been lost.
	5	MIC_ERROR	Michael integrity check error flag If set, then the frame TKIP Michael integrity check value did not verify correctly. Valid only when all of the following are true: ■ frame_rx_ok bit is set ■ The frame was decrypted using TKIP key type ■ The frame is not a fragment
	4	PHY_ERROR	PHY error flag If set, then reception of the frame failed because the PHY encountered an error. In this case, bits [15:8] of this word indicate the specific type of PHY error; see the baseband specification for details. Valid only if the frame_rx_ok flag is clear.
	3	DECRYPT_CRC_ERR	Decryption CRC failure flag If set, reception of the frame failed because the frame was marked as encrypted but the PCU was unable to decrypt the frame properly because the CRC check failed after the decryption process completed. Valid only if the frame_rx_ok flag is clear.
	2	CRC_ERROR	CRC error flag If set, reception of the frame failed because the PCU detected an incorrect CRC value. Valid only if the frame_rx_ok flag is clear.
	1	FRAME_RX_OK	Frame reception success flag. If set, the frame was received successfully. If clear, an error occurred during frame reception.
	0	DONE	Descriptor completion flag Set to one by the DMA engine when it has finished processing the descriptor and has updated the status information. Valid for all descriptors.

5.4 Queue Control Unit (QCU)

The queue control unit performs two tasks:

- Managing the Tx descriptor chain processing for frames pushed to the QCU from the CPU by traversing the linked list of Tx descriptors and transferring frame data from the host to the targeted DCU.
- Managing the queue transmission policy to determine when the frame at the head of the queue should be marked as available for transmission.

The MAC contains ten QCUs. Each QCU contains all the logic and state registers needed to manage a single queue (linked list) of Tx descriptors. A QCU is associated with exactly one DCU. When a QCU prepares a new frame, it signals ready to the DCU. When the DCU accepts the frame, the QCU responds by getting the frame data and passing it to the DCU for eventual transmission to the PCU and on to the air.

The host controls how the QCU performs these tasks by writing to various QCU configuration registers.

5.5 DCF Control Unit (DCU)

Collectively, the ten DCUs implement the EDCF channel access arbitration mechanism defined in the Task Group E (TGe) QoS extension to the 802.11 specification. Each DCU is associated with one of the eight EDCF priority levels and arbitrates with the other DCUs on behalf of all QCUs associated with it. A central DCU arbiter monitors the state of all DCUs and grants one the next access to the PCU (that is, access to the channel).

Because the EDCF standard defines eight priority levels, the first eight DCUs (DCUs 0–7) map directly to the eight EDCF priority levels. The two additional DCUs handle beacons and beacon-gated frames for a total of ten DCUs.

The mapping of physical DCUs to absolute channel access priorities is fixed and cannot be altered by software:

The highest-priority DCU is DCU 9. Typically, this DCU is the one associated with beacons.

The next highest priority DCU is DCU 8. Typically, this DCU is the one associated with beacon-gated frames.

The remaining eight DCUs priority levels are filled with DCUs 7 through 0. Among these 8 DCUs, DCU 7 has highest priority, DCU 6 the next highest priority, and so on through DCU 0, which has the lowest priority. Typically, these DCUs are associated with EDCF priorities seven through zero, respectively.

5.6 Protocol Control Unit (PCU)

The PCU is responsible for the details of sending a frame to the baseband logic for transmission, for receiving frames from the baseband logic and passing the frame data to the DRU, including:

- Buffering Tx and Rx frames
- Encrypting and decrypting
- Generating ACK, RTS, and CTS frames
- Maintaining the timing synchronization function (TSF)
- Forming aggregate

- Maintaining sequence state and generating Block ACK
- Inserting and verifying FCS
- Generating virtual clear channel assessment (CCA)
- Updating and parsing beacons
- The PCU is primarily responsible for buffering outgoing and incoming frames and conducting medium access compatible with the IEEE 802.11 DCF protocol

Figure 5-1 shows the PCU functional block diagram.

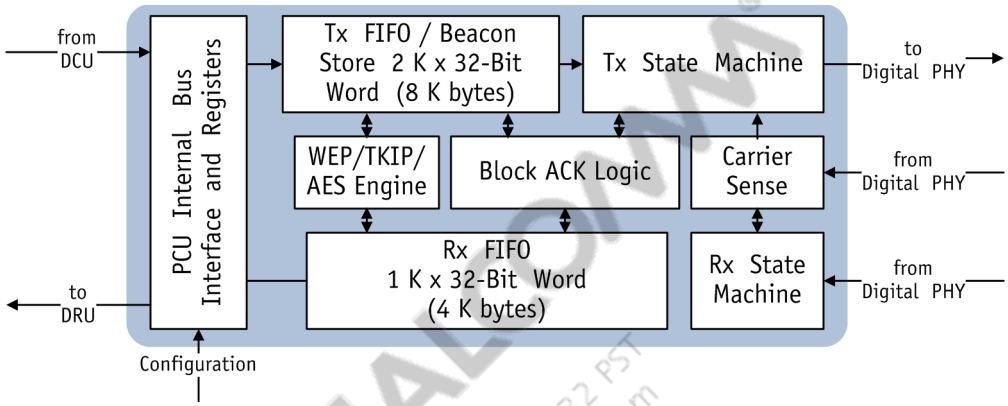


Figure 5-2 PCU Functional Block Diagram

5.7 Register Programming Details for Observing WMAC Interrupts

To configure the WMAC glue registers for observing WMAC interrupts:

1. Set bit [1] of these registers to observe MAC interrupts:
   - Synchronous Interrupt Enable (WMAC_GLUE_INTF_INTR_SYNC_ENABLE)
   - Synchronous Interrupt Cause (WMAC_GLUE_INTF_INTR_SYNC_CAUSE)
   - Interface Timeout (WMAC_GLUE_INTF_TIMEOUT)
   - Asynchronous Priority Interrupt Enable (WMAC_GLUE_INTF_INTR_PRIORITY_ ASYNC_ENABLE)
2. Write 0xFFFF_FFFF to the Synchronous Interrupt Cause (WMAC_GLUE_INTF_INTR_ SYNC_CAUSE) register to clear any pending interrupts.
3. Set bit [0] of the Global Interrupt Status (RST_GLOBAL_INTERRUPT_STATUS) register to enable MAC interrupts.
4. Enable primary MAC interrupts in the Primary Interrupt Mask (IMR_P) register (for example: bit [6] (TXOK), bit [1] (RXOK(LP)), and bit [0] (RXOK(HP)).
5. Enable secondary interrupts by writing to the IMR_S* registers: Secondary Interrupt Mask 0 (IMR_S0) through Secondary Interrupt Mask 5 (IMR_S5).
6. Read bits [3:0] of the register PCIE WMAC Interrupt Status (RST_PCIE _WMAC_ INTERRUPT_STATUS):

- Bit [0] = 1: Indicates a WMAC interrupt
- Bit [0] = 1, bit [1] = 1: Indicates a WMAC Tx interrupt
- Bit [0] = 1, bit [2] = 1: Indicates a WMAC Rx LP interrupt
- Bit [0] = 1, bit [3] = 1: Indicates a WMAC Rx HP interrupt

7. Read the Primary Interrupt Status (ISR_P) register to find the exact interrupt. Clear the interrupt by writing 1 to corresponding bit.

6 Digital PHY Block

The digital physical layer (PHY) block is described in 802.11n mode and 802.11 b/g legacy mode. Transmit and receive paths are provided and shown as block diagrams for 802.11n mode.

6.1 Overview

The digital PHY block is a half-duplex, OFDM, CCK, DSSS baseband processor compatible with IEEE 802.11n and 802.11b/g. The QCA9563 supports both 20- and 40-MHz channel modes and data rates up to 450 Mbps defined by the IEEE 802.11b/g/n standards. Modulation schemes include BPSK, QPSK, 16-QAM, 64-QAM and forward error correction coding with rates of 1/2, 2/3, 3/4, 5/6.

Two 802.11n advanced features, Space Time Block Code (STBC) and Low-Density Parity Check (Encoder) are supported in the QCA9563 chip. In addition, many new performance enhancing features are included, such as maximum likelihood (ML) MIMO receiver, and maximum ratio combining (MRC) for OFDM and 802.11b packet detection.

6.2 802.11n (MIMO) Mode

Frames beginning with training symbols are used for signal detection, automatic gain control, frequency offset estimation, symbol timing, and channel estimation. This process uses 56 sub-carriers for 20-MHz HT mode: 52 for data transmission and 4 for pilots. It uses 114 sub-carriers for 40-MHz HT mode: 108 for data transmission and 6 for pilots.

6.2.1 Transmitter (Tx)

Figure 6-1 shows the Tx path digital PHY 802.11n (MIMO mode) block diagram.

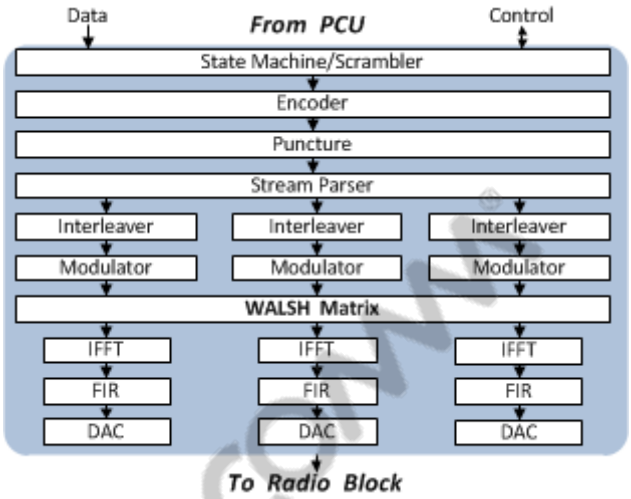


Figure 6-1 Digital PHY 802.11n Tx

The PCU block initiates transmission. The digital PHY powers on the digital to analog converter (DAC) and transmit the training symbol. The training symbols are a fixed waveform and are generated within the digital PHY in parallel with the PCU sending the Tx header (frame length, data rate, etc.). The PCU must send transmitted data quickly enough to prevent buffers in the digital PHY from becoming empty. The PCU is prevented from sending data too quickly by pauses generated within the digital PHY.

Figure 6-1 shows a 3x3 MIMO system with three spatial data streams. The spatial parser splits the coded data into multiple data streams by allocating the proper number of bits to each data stream so that the number of data symbols resulted in each stream is the same. Then it interleaves coded bits across different data subcarriers followed by the modulation. To achieve the maximum spatial diversity for one-stream and two-stream transmission, the Walsh matrix orthogonally spreads the modulated stream(s) into three Tx antennas before undergoing IFFT processing to produce time domain signals.

6.2.2 Receiver (Rx)

Figure 6-2 shows the Rx path digital PHY 802.11n (MIMO mode) block diagram.

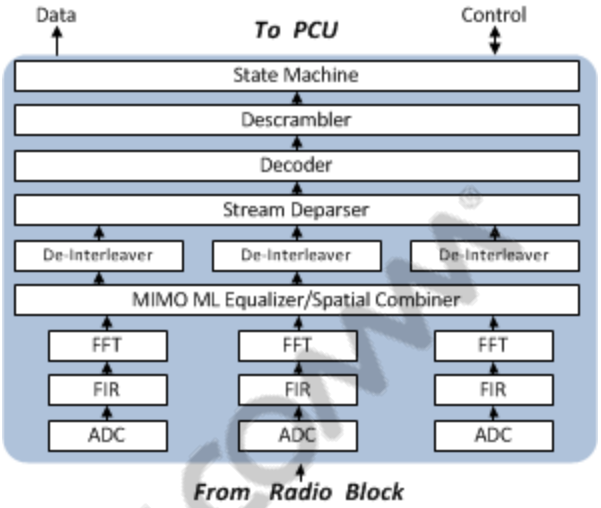


Figure 6-2 Digital PHY 802.11n Rx

The receiver inverts the transmitter's steps, performing a Fast Fourier Transform (FFT), extracting bits from received constellations, de-interleaving, accounting for puncturing, decoding, and descrambling. The Rx block shows 3x3 MIMO configuration. Figure 6-2 shows a frequency-domain Maximum Likelihood (ML) equalizer handling degradation due to multi-path.

6.3 802.11 b/g Legacy Mode

6.3.1 Transmitter

The QCA9563 digital PHY incorporates an OFDM and DSSS transceiver that supports all data rates defined by IEEE 802.11b/g. Legacy mode is detected on per-frame basis. PLCP frames are detected for legacy network information. The transmitter switches dynamically to generate legacy signals (802.11 b/g in 2.4 GHz).

6.3.2 Receiver

The receiver is capable of dynamically detecting legacy, HT 20 MHz or 40 MHz frames and will demodulate the frame according to the detected frame type. Maximum ratio combining (MRC) is used for OFDM and 802.11b packet detection.

7 Ethernet Subsystem

7.1 GMAC

The QCA9563 has a gigabit Ethernet MAC to connect to the SGMII interface.

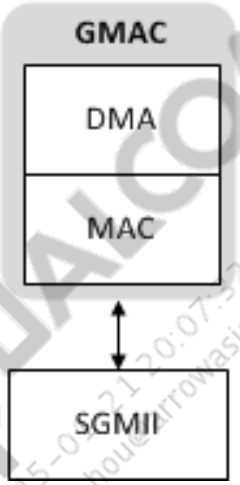


Figure 7-1 Ethernet Subsystem

7.1.1 SGMII Interface

The SGMII interface provides a high-speed serial interface that connects a GBit MAC and a 10/100/1000 PHY while requiring fewer signal pins. It can operate at ports speeds of 10, 100, and 1000 Mbps. GMAC0 can be connected to the SGMII physical interface of the QCA9563.

SGMII uses two data signals and two clock signals to convey frame data and link rate information between a 10/100/1000 PHY and an Ethernet MAC. The data signals operate at 1.25 GBaud and the clocks operate at 625 MHz (a DDR interface). Due to operating speed, each of these signals is realized as a differential pair, providing signal integrity while minimizing system noise.

The QCA9563 SGMII interface operates in a mode where the clock is recovered from the received data rather than being provided as a separate pin. SGMII interface pins include:

- SGMII_SIN
- SGMII_SIP
- SGMII_SOP
- SGMII_SON

SGMII supports these operating modes:

- SGMII MAC and PHY mode

  In this mode the MAC and PHY exchange capability information across the SGMII interface and set their speeds accordingly as 10, 100, or 1 GBps mode. GMAC0 can be connected to the SGMII physical interface of the QCA9563.

- Auto-negotiation

  In SGMII MAC and PHY mode, the PHY sends control information during auto-negotiation. While this exchange is labeled auto-negotiation, it is an information exchange where the PHY passes the copper side auto-negotiation results to the MAC. The MAC responds to the PHY with an acknowledgment.

  In BaseX mode, capabilities are advertised to a link partner and the MAC detects the corresponding capabilities advertised by the link partner. Auto-negotiation occurs in BaseX mode.

The MDIO interface is not directly supported through SGMII; use the GPIO-based MDIO master interface 1. See MDIO Master Interface.

7.2 GMAC Descriptor Structure: Rx

In the Rx descriptor, each descriptor comprises a sequence of three 32-bit memory locations:

Table 7-1 Rx Descriptors

Address	Name	Description	Page
0x0	PKT_START_ADDR	Start Address for Packet Data	page 85
0x4	PKT_SIZE	Packet Size and Flags	page 86
0x8	NEXT_DESCRIPTOR	Next Packet Descriptor Address	page 86

7.2.1 Start Address for Packet Data (PKT_START_ADDR)

Address Offset: 0x0
Access: Read/Write

Bit	Name	Description
31:0	PKT_START_ADDR	Packet start address. The built-in DMA controller reads this register to discover the location in host memory of the first byte of data. Note: The start addresses used in any sequence of descriptors must be spaced to add sufficient room in any location for a packet of the maximum size transferred.

7.2.2 Packet Size and Flags (PKT_SIZE)

Address Offset: 0x4
Access: See field descriptions

Bit	Name	Access	Description
31	EMPTY_FLAG	R/W	This bit indicates the availability of the specified location to store the received packet. Setting this flag validates the descriptor. This bit is also called the OWN (ownership) bit. Note: On successful completion of an Rx operation, the DMA controller writes 0 to this location to indicate that this location has been used to store the received packet. This action ensures that received data is not accidentally overwritten by a subsequent packet.
30	NAT_STATUS	RO	Set by the DMA controller indicating the NAT Status for the packet.
			0 NAT operation is not done. Valid only if Ingress NAT functionality is enabled.
			1 Successfully NAT edit.
29:28	RES	RO	Reserved
27:26	SW_STATUS	RO	Provides the software status bits loaded into the LUT for the connection that the packet belongs to.
25	NAT_ UNSUPPORTED	RO	Indicates an ERROR status for NAT because the packet is unsupported
			0 Supported packet type
			1 Unsupported packet type; valid only if NAT_STATUS is set to 0 and ingress NAT functionality is enabled
24	PER_PKT_ INTR_EN	R/W	When set to 1 by software, the DMA controller generates an interrupt to the CPU after successful completion of the packet DMA.
23	FRG	RO	Indicates whether this packet is fragmented
22:14	RES	RO	Reserved
13:0	PKT_SIZE	R/W	Updated by the hardware with the size of the actual packet received.

7.2.3 Next Packet Descriptor Address (NEXT_DESCRIPTOR)

Address Offset: 0x8
Access: Read/Write

Bit	Name	Description
31:2	DESCRIPTOR _ADDR	Top 30 bits of Packet the descriptor address. The built-in DMA controller reads this register to discover the location in host memory of the descriptor for the next packet in the sequence. The descriptors should form a closed linked list.
1:0	RES	Ignored by the DMA controller because it is a requirement of the system that all descriptors are 32-bit aligned in host memory. Default is 0.

7.3 GMAC Descriptor Structure: Tx

In the Tx descriptor, each descriptor comprises a sequence of three 32-bit memory locations:

Table 7-2 Tx Descriptors

Address Offset	Name	Description	Page
0x0	PKT_START_ADDR	Start Address for Packet Data	page 87
0x4	PKT_SIZE	Packet Size and Flags	page 87
0x8	NEXT_DESCRIPTOR	Next Packet Descriptor Address	page 88

7.3.1 Start Address for Packet Data (PKT_START_ADDR)

Address Offset: 0x0
Access: Read/Write

Bit	Name	Description
31:0	PKT_START_ADDR	Packet start address. The built-in DMA controller reads this register to discover the location in host memory of the first byte of data. Note: The start addresses used in any sequence of descriptors must be spaced to add sufficient room in any location for a packet of the maximum size transferred.

7.3.2 Packet Size and Flags (PKT_SIZE)

Address Offset: 0x4
Access: See fields descriptions

Bit	Name	Access	Description	
31	EMPTY_FLAG	R/W	This bit indicates the availability of the specified location to store the received packet. Setting this flag validates the descriptor. Note: On successful completion of an Rx operation, the DMA controller writes 0 to this location to indicate that this location has been used to store the received packet. This action ensures that received data is not accidentally overwritten by a subsequent packet.	
30	PER_PACKET_NAT_ENABLE	R/W	Used to control NAT function for Tx Packets on per-packet basis.	
			0	The Tx packet bypasses the egress NAT Engine. Valid only if egress NAT is enabled.
			1	The Tx packet goes through the egress NAT engine.
29	PER_PACKET_ACL_ENABLE	R/W	Used to control ACL function for Tx Packets on per-packet basis.	
			0	The Tx packet bypasses the egress ACL Engine. Valid only if egress ACL is enabled.
			1	The Tx packet goes through the egress NAT engine.
28	NAT_STATUS	RO	Set by the DMA controller indicating the NAT Status for the packet. '	
			0	NAT unsuccessful. Valid only if the egress NAT functionality is enabled and PER_PACKET_ACL_ENABLE is set.
			1	NAT successful.
27	ACL_STATUS	RO	Set by the DMA controller indicating the ACL Status for the packet.	
			0	ACL allow. Valid only if the egress ACL functionality is enabled and PER_PACKET_ACL_ENABLE is set.
			1	ACL drop
26	FRG	R/W	Indicates whether the current packet is fragmented.	

25	NAT_ UNSUPPORTED	RO	Indicates an ERROR status for NAT because the packet is unsupported	
			0	Supported packet type
			1	Unsupported packet type; valid only if NAT_STATUS is set to 0 and egress NAT functionality is enabled
24	MORE	R/W	Setting this bit indicates that the buffer is only part of the packet and does not contain the end of packet data. This bit should not be set if NAT/ACL are enabled.	
23:14	RES	WO	Reserved; must be set to 0.	
13:0	PKT_SIZE	R/W	Software writes the number of bytes to transmit into this field. The minimum value for this field is 5 bytes. If the MORE bit is set, then the value written should be a multiple of 4.	

7.3.3 Next Packet Descriptor Address (NEXT_DESCRIPTOR)

Address Offset: 0x8
Access: Read/Write

Bit	Name	Description
31:2	DESCRIPTOR _ADDR	Top 30 bits of Packet the descriptor address. The built-in DMA controller reads this register to discover the location in host memory of the descriptor for the next packet in the sequence. The descriptors should form a closed linked list.
1:0	RES	Ignored by the DMA controller because it is a requirement of the system that all descriptors are 32-bit aligned in host memory. Default is 0.

8 Register Descriptions

These sections describe the internal registers for the various QCA9563 blocks.

Table 8-1 summarizes the CPU mapped registers for the QCA9563.

Table 8-1 CPU Mapped Registers Summary

Address	Description	Page
0x18000000–0x18000128	DDR Registers	page 90
0x18018000-0x18018080	I^2C Registers	page 103
0x18020000–0x18020018	UART0 (Low-Speed) Registers	page 120
0x18030000–0x1803000C	USB Registers	page 128
0x18040000–0x1804006C	GPIO Registers	page 132
0x18050000–0x18050048	PLL Control Registers	page 139
0x18060000–0x180600AC	Reset Control Registers	page 150
0x18070000–0x18070064	GMAC Interface Registers	page 160
0x18250000–0x1825005C	PCIE RC Control Registers	page 173
0x18100008–0x1810012C	WLAN MAC Registers	page 185
0x18100800–0x18100A44	WLAN MAC Queue Control Unit Registers	page 205
0x18101000–0x18101F04	MAC Data Control Unit Registers	page 212
0x18104000–0x181040F0	WMAC Glue Registers	page 221
0x18107000–0x18107058	RTC Registers	page 229
0x18108000–0x18108800	WLAN MAC Protocol Control Unit Registers	page 239
0x18116180-0x181161C8	PLL SRIF Registers	page 280
0x18116CC0-0x18116CC4	PMU Registers	page 290
0x18116DC0–0x18116DC8	PCIE RC PHY Registers	page 291
0x19000000–0x190002E8	GMAC0 Registers	page 294
0x1F000000–0x1F000018	Serial Flash SPI Registers	page 340

8.1 DDR Registers

Table 8-1 summarizes the DDR registers for the QCA9563.

NOTE The memory controller core clock is twice the frequency of the DDR_CK_P clock.

Table 8-2 DDR Registers Summary

Address	Name	Description	Page
0x18000000	DDR_CONFIG	DDR DRAM Configuration	page 91
0x18000004	DDR_CONFIG2	DDR DRAM Configuration 2	page 92
0x18000008	DDR_MODE	DDR Mode Value	page 93
0x1800000C	DDR_EXTENDED_MODE_REGISTER	DDR Extended Mode Value	page 93
0x18000010	DDR_CONTROL	DDR Control	page 93
0x18000014	DDR_REFRESH	DDR Refresh Control and Configuration	page 94
0x18000018	DDR_RD_DATA_THIS_CYCLE	DDR Read Data Capture Bit Mask	page 94
0x1800001C	TAP_CONTROL_0	DQS Delay Tap Control for Byte 0	page 94
0x18000020	TAP_CONTROL_1	DQS Delay Tap Control for Byte 1	page 95
0x1800009C	DDR_WB_FLUSH_GE0	GE0 Interface Write Buffer Flush	page 95
0x180000A4	DDR_WB_FLUSH_USB	USB Interface Write Buffer Flush	page 95
0x180000A8	DDR_WB_FLUSH_PCIE	PCIE Interface Write Buffer Flush	page 96
0x180000AC	DDR_WB_FLUSH_WMAC	WMAC Interface Write Buffer Flush	page 96
0x180000B8	DDR_DDR2_CONFIG	DDR2 Configuration	page 96
0x180000BC	DDR_EMR2	DDR Extended Mode 2 Value	page 97
0x180000C0	DDR_EMR3	DDR Extended Mode 3 Value	page 97
0x180000C4	DDR_BURST	DDR bank arbiter per client burst size 1	page 97
0x180000C8	DDR_BURST2	DDR bank arbiter per client burst size 2	page 98
0x180000CC	AHB_MASTER_TIMEOUT_MAX	AHB Master Timeout Control	page 98
0x180000D0	AHB_MASTER_TIMEOUT_CURNT	AHB Timeout Current Count	page 98
0x180000D4	AHB_MASTER_TIMEOUT_SLAVE_ADDR	Timeout Slave Address	page 99
0x18000108	DDR_CTL_CONFIG	DDR Control Configuration	page 99
0x18000110	DDR_SF_CTL	DDR Self Refresh	page 101
0x18000114	SF_TIMER	DDR Self Refresh Timer	page 101
0x18000128	WMAC_FLUSH	WMAC Flush	page 102
0x1800015C	DDR3_CONFIG	DDR3 Configuration	page 102

8.1.1 DDR DRAM Configuration (DDR_CONFIG)

Address: 0x18000000
Access: Read/Write
Reset: See field description

This register is used to configure the DDR DRAM parameters.

Bit	Bit Name	Reset	Description
31	CAS_LATENCY_MSB	0x0	DRAM CAS latency parameter MSB rounded up in memory core clock cycles
30	RES	0x1	Reserved
29:27	CAS_LATENCY	0x6	DRAM CAS latency parameter (first 3 bits) rounded up in memory core clock cycles. CAS_LATENCY is used by the hardware to estimate the internal DDR clock latency of a read. It should be greater than or equal to GATE_OPEN_ LATENCY as specified in the DDR_CONFIG2 register. The value of this register should be memory cas_latency * 2 or cas_latency * 2+1/2/3.
26:23	TMRD	0xF	DRAM tMRD parameter rounded up in memory core clock cycles
22:17	TRFC	0x1F	DRAM tRFC parameter rounded up in memory core clock cycles
16:13	TRRD	0x4	DRAM tRRD parameter rounded up in memory core clock cycles
12:9	TRP	0x6	DRAM tRP parameter rounded up in memory core clock cycles
8:5	TRCD	0x6	DRAM tRCD parameter rounded up in memory core clock cycles
4:0	TRAS	0x10	DRAM tRAS parameter rounded up in memory core clock cycles

8.1.2 DDR DRAM Configuration 2 (DDR_CONFIG2)

Address: 0x18000004
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
31	HALF_WIDTH_LOW	—	This bit controls which part of the 32 bit DDR DQ bus is populated with DRAM in a 16 bit wide memory system.	
			0	31:16
			1	15:0
30	SWAP_A26_A27	0x0	This bit gives a choice to drive CPU address A26 and A27 on different column lines. This is needed to support different combinations of devices on board.	
			0	Drives CPU_ADDR[26] on A11 of COL if DDR_CONFIG_HALF_WIDTH==1 or on A9 of COL if DDR_CONFIG_HALF_WIDTH==0. In this case, CPU_ADDR[27] will be driven on A12 of COL if DDR_CONFIG_HALF_WIDTH==1 and A11 of COL if DDR_CONFIG_HALF_WIDTH==0.
			1	Drives CPU_ADDR[27] on A11 of COL if DDR_CONFIG_HALF_WIDTH==1 or on A9 of COL if DDR_CONFIG_HALF_WIDTH==0. In this case, CPU_ADDR[26] will be driven on A12 of COL if DDR_CONFIG_HALF_WIDTH==1 and A11 of COL if DDR_CONFIG_HALF_WIDTH==0.
29:26	GATE_OPEN_LATENCY	0x6	DRAM gate open latency parameter rounded up in memory core clock cycles	
25:21	TWTR	0xE	DRAM tWTR parameter rounded up in memory core clock cycles	
20:17	TRTP	0x8	DRAM read to precharge parameter rounded up in memory core clock cycles. The normal value is two clock cycles.	
16:12	TRTW	0x10	DRAM tRTW parameter rounded up in memory core clock cycles. The value should be calculated as CAS LATENCY + BURST LENGTH + BUS TURN AROUND TIME.	
11:8	TWR	0x6	DRAM tWR parameter rounded up in memory core clock cycles	
7	CKE	0x1	DRAM CKE bit	
6	PHASE_SELECT	0x0	Selects the output phase	
5	CNTL_OE_EN	0x1	Control bit to allow the memory controller to tri-state the address/control outputs	
4	BURST_TYPE	0x0	DRAM burst type	
			0	Sequential
			1	Interleaved
3:0	BURST_LENGTH	0x8	DRAM burst length setting. Only 8 is supported.	

8.1.3 DDR Mode Value (DDR_MODE_REGISTER)

Address: 0x18000008
Access: Read/Write
Reset: See field description

This register is used to set the DDR mode register value.

Bit	Bit Name	Reset	Description
31:14	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
13:0	VALUE	0x133	Mode register value. Reset to CAS 3, BL=8, sequential, DLL reset off.

8.1.4 DDR Extended Mode (DDR_EXTENDED_MODE_REGISTER)

Address: 0x1800000C
Access: Read/Write
Reset: See field description

This register is used to set the extended DDR mode register value.

Bit	Bit Name	Reset	Description
31:14	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
13:0	VALUE	0x2	Extended mode register value. Reset to weak driver, DLL on.

8.1.5 DDR Control (DDR_CONTROL)

Address: 0x18000010
Access: Read/Write
Reset: 0x0

This register is used to force update cycles in the DDR control.

Bit	Bit Name	Description
31:6	RES	Reserved
5	EMR3S	Forces an EMR3 update cycle
4	EMR2S	Forces an EMR2 update cycle
3	PREA	Forces a PRECHARGE ALL cycle
2	REF	Forces an AUTO REFRESH cycle
1	EMRS	Forces an EMRS update cycle
0	MRS	Forces an MRS update cycle

8.1.6 DDR Refresh Control and Configuration (DDR_REFRESH)

Address: 0x18000014
Access: Read/Write
Reset: See field description

This register is used to configure the settings to refresh the DDR.

Bit	Bit Name	Reset	Description
31:15	RES	0x0	Reserved
14	ENABLE	0x0	Setting this bit to one will enable a DDR refresh
13:0	PERIOD	0x12C	Sets the refresh period intervals with respect to the ref clock (25 MHz)

8.1.7 DDR Read Data Capture Bit Mask (DDR_RD_DATA_THIS_CYCLE)

Address: 0x18000018
Access: Read/Write
Reset: See field description

This register is used to set the parameters to read the DDR and capture bit masks.

Bit	Bit Name	Reset	Description
31:0	VEC	0xFF	DDR read and capture bit mask. Each bit represents a cycle of valid data. Set to 0xFFFF for 16-bit DDR memory systems.

8.1.8 DQS Delay Tap Control for Byte 0 (TAP_CONTROL_0)

Address: 0x1800001C
Access: Read/Write
Reset: See field description

This register is used along with DQ Lane 0, DQ[7:0], DQS_0.

Controls the delay in the DQS clock path. Used to position the DQS to the center of the EYE of DQ data signal.

Bit	Bit Name	Reset	Description
31:6	RES	0x0	Reserved
5:0	TAP	0x5	Tap setting for the delay chain of this lane. There are a total of 64 taps available, which may be set using these six bits.

8.1.9 DQS Delay Tap Control for Byte 1 (TAP_CONTROL_1)

Address: 0x18000020
Access: Read/Write
Reset: See field description

This register is used along with DQ Lane 1, DQ[15:8], DQS_1.

Controls the delay in the DQS clock path. Used to position the DQS to the center of the EYE of DQ data signal.

Bit	Bit Name	Reset	Description
31:6	RES	0x0	Reserved
5:0	TAP	0x5	Tap setting for the delay chain of this lane. There are a total of 64 taps available, which may be set using these six bits.

8.1.10 GE0 Interface Write Buffer Flush (DDR_WB_FLUSH_GE0)

Address: 0x1800009C
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the GE0 interface.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	Set this bit to 1 to flush the write buffer for the GE0 interface. This bit will reset to 0 when the flush is complete.

8.1.11 USB Interface Write Buffer Flush (DDR_WB_FLUSH_USB)

Address: 0x180000A4
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the USB interface.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the USB interface. This bit will reset to 0 when the flush is complete.

8.1.12 PCIE Interface Write Buffer Flush (DDR_WB_FLUSH_PCIE)

Address: 0x180000A8
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the PCIE interface.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the PCIE interface. This bit will reset to 0 when the flush is complete.

8.1.13 WMAC Interface Write Buffer Flush (DDR_WB_FLUSH_WMAC)

Address: 0x180000AC
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the WMAC interface.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the WMAC interface. This bit will reset to 0 when the flush is complete.

8.1.14 DDR2 Configuration (DDR_DDR2_CONFIG)

Address: 0x180000B8
Access: Read/Write
Reset: 0x0858

Bit	Bit Name	Type	RW	Description	
31:14	RES	RO	0x0	Reserved	
13:10	DDR2_TWL	RW	0x1	Delays driving the data signals for writing commands with respect to command issue by TWL DDR clocks	
9	DDR2_ODT	RW	0x1	This DDR2 setting enables a High output n the ODT signal	
8	RES	RO	0x0	Reserved	
7:2	DDR2_TFAW	RW	0x16	tFAW parameter in core DDR_CLK cycles	
1	RES	RW	0x0	Reserved	
0	ENABLE_DDR2	RW	0x0	0	DDR1
				1	DDR2

8.1.15 DDR EMR2 (DDR_EMR2)

Address: 0x180000BC
Access: Read/Write
Reset: 0x0

This register is used set the extended mode register 2 value.

Bit	Bit Name	Type	Reset	Description
31:14	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
13:0	VALUE	RW	0x0	Extended mode register 2 value, reset to weak driver, DLL on

8.1.16 DDR EMR3 (DDR_EMR3)

Address: 0x180000C0
Access: Read/Write
Reset: 0x0

This register is used set the extended mode register 3 value.

Bit	Bit Name	Type	Reset	Description
31:14	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
13:0	VALUE	RW	0x0	Extended mode register 3 value, reset to weak driver, DLL on

8.1.17 DDR Bank Arbiter Per Client Burst Size (DDR_BURST)

Address: 0x180000C4
Access: Read/Write
Reset: See field description

NOTE Changes to this register is not recommended.

Bit	Bit Name	Reset	Description
31	CPU_PRIORITY	0x0	Setting this bit causes the bank arbiters to break current burst and grant CPU
30	CPU_PRIORITY_BE	0x1	Setting this bit causes the bank arbiters to break only at current burst completion and grant CPU
29:28	ENABLE_RWP_MASK	0x3	Enables the Read/Write mask and the Precharge Mask
27:24	MAX_WRITE_BURST	0x0	Max Write Burst size. Reads are masked in the BANK_ARB.
23:20	MAX_READ_BURST	0x4	Max Read Burst size. Writes are masked in the BANK_ARB.
19:16	CPU_MAX_BL	0x0	CPU burst size
15:12	USB_MAX_BL	0x1	USB burst size
11:8	PCIE_MAX_BL	0x3	PCIE burst size
7:4	RES	0x4	Reserved
3:0	GE0_MAX_BL	0x4	Ethernet burst size

8.1.18 DDR Bank Arbiter Per Client Burst Size 2 (DDR_BURST2)

Address: 0x180000C8
Access: Read/Write
Reset: See field description

NOTE Changes to this register is not recommended.

Bit	Bit Name	Reset	Description
31:4	RES	0x0	Reserved
3:0	WMAC_MAX_BL	0x2	WNAC burst size

8.1.19 DDR AHB Master Timeout Control (DDR_AHB_MASTER_ TIMEOUT_MAX)

Address: 0x180000CC
Access: Read/Write
Reset: 0x0

This register specifies the maximum timeout value of the AHB master control.

Bit	Bit Name	Type	Reset	Description
31:20	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
19:0	VALUE	RW	0x8000	Maximum time out value

8.1.20 DDR AHB Timeout Current Count (DDR_AHB_MASTER_ TIMEOUT_CURNT)

Address: 0x180000D0
Access: Read/Write
Reset: 0x0

This register specifies the current AHB timeout value.

Bit	Bit Name	Type	Reset	Description
31:20	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
19:0	VALUE	RO	0x0	Current time out value

8.1.21 Timeout Slave Address (AHB_MASTER_TIMEOUT_SLV_ ADDR)

Address: 0x180000D4
Access: Read/Write
Reset: 0x0

This register specifies the maximum timeout value to access the slave address space.

Bit	Bit Name	Type	Reset	Description
31:0	ADDR	RO	0x0	Maximum time out value

8.1.22 DDR Controller Configuration (DDR_CTL_CONFIG)

Address: 0x18000108
Access: Read/Write
Reset: 0x0

This register specifies the control bits for the DDR.

Bit	Bit Name	Type	Reset	Description	
31:30	SRAM_TSEL	RW	0x1	Determines the TSEL value of the SRAM memory	
29:21	CLIENT_ACTIVITY	RO	0x0	Indicates if there is currently any activity in each of the AHB/AXI/OCP clients connected to the DDR	
20	GE0_SRAM_SYNC	RW	0x1	This bit is used to make sure that GE0 launches a SRAM write request only if all pending DDR write requests of GE0 have been completed. This is necessary to make sure that all data has been DMA'ed to the DDR memory before GE0 updates the descriptor status in the SRAM. Otherwise, there is a possibility that the CPU could poll for this status and read from the DDR memory before the data is actually DMA'ed to the DDR memory. In this case, the CPU receives the wrong data.	
				0	Disabled
				1	Enabled
19	RES	RW	0x1	Reserved	
18	USB_SRAM_SYNC	RW	0x1	This bit is used to make sure that USB launches a SRAM write request only if all pending DDR write requests of USB have been completed. This is necessary to make sure that all data has been DMA'ed to the DDR memory before GE1 updates the descriptor status in the SRAM. Otherwise, there is a possibility that the CPU could poll for this status and read from the DDR memory before the data is actually DMA'ed to the DDR memory. In this case, the CPU receives the wrong data.	
				0	Disabled
				1	Enabled

17	PCIE_SRAM_SYNC	RW	0x1	This bit is used to make sure that PCIE launches a SRAM write request only if all pending DDR write requests of PCIE have been completed. Otherwise, there is a possibility that the CPU could poll for this status and read from the DDR memory before the data is actually DMA'ed to the DDR memory. In this case, the CPU receives the wrong data.	
				0	Disabled
				1	Enabled
16	WMAC_SRAM_ SYNC	RW	0x1	This bit is used to make sure that WMAC launches a SRAM write request only if all pending DDR write requests of WMAC have been completed. This is necessary to make sure that all data has been DMA'ed to the DDR memory before WMAC updates the descriptor status in the SRAM. Otherwise, there is a possibility that the CPU could poll for this status and read from the DDR memory before the data is actually DMA'ed to the DDR memory. In this case, the CPU receives the wrong data.	
				0	Disabled
				1	Enabled
15:14	RES	R	0x0	Reserved	
6	PAD_DDR2_SEL	RW	0x0	Controls the SEL_18 of the DDR_PADS.	
				0	DDR1 mode
				1	DDR2 mode
5	RES	RW	0x0	Reserved	
4	GATE_SRAM_CLK	RW	0x0	SRAM gating enable	
				0	SRAM not gated
				1	SRAM gated
3	SRAM_REQ_ACK	RW	0x0	This bit is needed to make sure that two back-to-back requests from a AHB/AXI adapter are recognized as two requests in the CPU domain when the CPU is running at a slower clock compared to AHB_CLK. The synchronized request in CPU domain has to become 0 and get checked by the logic in AHB/AXI if it has become 0. Only then the adapter can launch the second request. Set this bit to 1 if the CPU_ CLK is slower than the AHB_CLK. Otherwise, there is no issue of back-to-back req synchronization.	
2	CPU_DDR_SYNC	RW	0x0	Set to 1 if the CPU and DDR clocks are needed to operate synchronously. By default, CPU and DDR clocks are asynchronous to each other.	
1	HALF_WIDTH	RW	0x1	Set to one for x16 DDR configurations	
0	RES	R	0x0	Reserved	

8.1.23 DDR Self Refresh Control (DDR_SF_CTL)

Address: 0x18000110
Access: Read/Write
Reset: 0x0

This register specifies the settings for the DDR self refresh mode.

Bit	Bit Name	Type	Reset	Description
31	EN_SELF_REFRESH	RW	0x0	Setting this bit will initiate entering self refresh mode. This bit can be cleared by S/W or H/W if the auto exit is enabled
30	EN_AUTO_SF_EXIT	RW	0x0	Setting this bit will initiate exiting self refresh mode upon request from any AHB/AXI master
29	CUR_SR_STATE	RO	0x0	Indicates if the DDR is currently in self refresh mode
28	CUR_CKE_STATE	RO	0x0	Indicates if the DDR CKE is high or low
27	EN_SF_CLK_ GATING	RW	0x0	Setting this bit gates CK_P and CK_N during self refresh mode
26:25	CKE_GATE_DLY_ SEL	RW	0x0	Determines the delay of the CKE assertion from CK_P and stops gating when exiting self refresh mode
24:21	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
20:18	NO_ACTIVITY_ CNTR	RO	0x0	Indicates the duration on no activity in the AHB/AXI clients of the DDR in terms of the DDR refresh period
17:8	TXSRD	RW	0x1C2	Indicates XSND parameter of the memory in the number of DDR_ CLKs
7:0	TXSNR	RW	0x3C	Indicates XSNR parameter of the memory in the number of DDR_ CLKs

8.1.24 Self Refresh Timer (SF_TIMER)

Address: 0x18000114
Access: Read/Write
Reset: 0x0

This register specifies the DDR refresh periods for self refresh mode.

Bit	Bit Name	Type	Reset	Description
31:16	RF_OUT_DPR_ COUNT	RO	0x0	Indicates the number of DDR_REFRESH_PERIODs for which HW remained out of the self refresh mode
15:0	IN_RF_DPR_ COUNT	RO	0x0	Indicates the number of DDR_REFRESH_PERIODs for which HW remained in self refresh mode

8.1.25 WMAC Flush (WMAC_FLUSH)

Address: 0x18000128
Access: Read/Write
Reset: 0x0

This register specifies the settings for the WMAC Flush.

Bit	Bit Name	Type	Reset	Description
31:10	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
9	DONE	RW	0x0	Set to 1 by HW after the flush is completed and the adapter is ready. SW clears it back to 0.
8:1	DDR_CLK_ CNTR	RW	0x28	Number of DDR clocks to count down after the last grant, ensuring all I/O reads are completed.
0	FORCE	RW	0x0	Set to 1 by software to start the AXI FLUSH. Hardware clears this field to 0.

8.1.26 DDR3 Configuration Register (DDR3_CONFIG)

Address: 0x1800015C
Access: Read/Write
Reset: 0x0

This register holds the configuration parameters for DDR timing.

Bit	Bit Name	Reset	Description
31:4	SPARE	0x0	Spare bits
3	TWR_MSB	0x0	MSB of TWR timing parameters expressed as an internal DDR clock
2	TRAS_MSB	0x0	MSB of TRAS timing parameters expressed as an internal DDR clock
1:0	TRFC_LSB	0x0	TRFC timing parameter. LSB two bits; in terms of the internal DDR clock.

8.2 I²C Configuration Registers

Table 8-4 summarizes the I²C configuration registers for the QCA9563.

Table 8-3 CPU Wrapper Registers Summary

Address	Name	Description	Page
0x18018000	IC_CON	I²C Configuration	page 104
0x18018004	IC_TAR	I²C Target Address	page 105
0x1801800C	IC_HS_MADDR	I²C HS Mode Master Code	page 105
0x18018010	IC_DATA_CMD	I²C Rx/Tx Data Buffer and Command	page 106
0x18018014	IC_SS_SCL_HCNT	Standard I²C Clock SCL High Count	page 106
0x18018018	IC_SS_SCL_LCNT	Standard I²C Clock SCL Low Count	page 107
0x1801801C	IC_FS_SCL_HCNT	Fast I²C Clock SCL High Count	page 107
0x18018020	IC_FS_SCL_LCNT	Fast I²C Clock SCL Low Count	page 108
0x18018024	IC_HS_SCL_HCNT	High Speed I²C Clock SCL High Count	page 108
0x18018028	IC_HS_SCL_LCNT	High Speed I²C Clock SCL Low Count	page 109
0x1801802C	IC_RAW_INTR_STAT	I²C Raw Interrupt Status	page 109
0x18018030	IC_INTR_MASK	I²C Interrupt Mask	page 111
0x18018034	IC_INTR_STAT	I²C Interrupt Status	page 111
0x18018038	IC_RX_TL	I²C Receive FIFO Threshold	page 113
0x1801803C	IC_TX_TL	I²C Transmit FIFO Threshold	page 113
0x18018040	IC_CLR_INTR	I²C Combined and Individual Interrupts Clear	page 113
0x18018044	IC_CLR_RX_UNDER	I²C Clear RX_UNDER Interrupts	page 114
0x18018048	IC_CLR_RX_OVER	I²C Clear RX_OVER Interrupts	page 114
0x1801804C	IC_CLR_TX_OVER	I²C Clear TX_OVER Interrupts	page 114
0x18018050	IC_CLR_RD_REQ	I²C Clear RD_REQ Interrupts	page 114
0x18018054	IC_CLR_TX_ABRT	I²C Clear TX_ABRT Interrupts	page 115
0x18018058	IC_CLR_RX_DONE	I²C Clear RX_DONE Interrupts	page 115
0x1801805C	IC_CLR_ACTIVITY	I²C Clear ACTIVITY Interrupts	page 115
0x18018060	IC_CLR_STOP_DET	I²C Clear STOP_DET Interrupts	page 116
0x18018064	IC_CLR_START_DET	I²C Clear START_DET Interrupts	page 116
0x18018068	IC_CLR_GEN_CALL	I²C Clear GEN_CALL Interrupts	page 116
0x1801806C	IC_ENABLE	I²C Enable	page 117
0x18018070	IC_STATUS	I²C Transfer and FIFO Status	page 117
0x18018074	IC_TXFLR	I²C Transmit FIFO Level	page 118
0x18018078	IC_RXFLR	I²C Receive FIFO Level	page 118
0x1801807C	IC_SRESET	I²C Soft Reset	page 118
0x18018080	IC_TX_ABRT_SOURCE	I²C TX Abort Source	page 119

8.2.1 I2C Configuration (IC_CON)

Address: 0x18018000
Access: Read-Write
Reset: See field description

This register can be written only when the DW_APB_I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Bit	Bit Name	Type	Reset	Description
31:6	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
5	IC_RESTART_EN	RW	0x1	Determines whether restart conditions may be sent when acting as a master. Some older slaves do not support handling restart conditions. Restart conditions are used in several DW_APB_I2C operations. Disabling a restart does not allow the master to perform these functions: 1. Send multiple bytes per transfer (split) 2. Change direction within a transfer (split) 3. Send a start byte 4. Perform any high-speed mode operation 5. Perform combined format transfers in 7- or 10-bit addressing modes (split for 7 bit) 6. Perform a read operation with a 10-bit address. Split operations are broken down into multiple DW_APB_I2C transfers with a stop and start condition in between. The other operations are not performed at all and result in setting TX_ABRT.
4	IC_10BITADDR_MASTER	RW	0x1	This bit controls whether the DW_APB_I2C starts its transfers in 10-bit addressing mode when acting as a master. 0 – 7-bit addressing 1 – 10-bit addressing
	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
2:1	SPEED	RW	0x3	Controls at which speed the DW_APB_I2C operates. If the DW_APB_I2C is configured for fast or standard mode (1 or 2) and a value of 2 or 3 is written, then IC_MAX_SPEED_MODE is stored. 0 – Illegal; writing a 0 results in setting SPEED to IC_MAX_SPEED_MODE 1 – Standard mode (100 KBps) 2 – Fast mode (400 KBps) 3 – High speed mode (3.4 MBps)
0	MASTER_MODE	RW	0x1	Controls whether the DW_APB_I2C master is enabled 0 – Master disabled 1 – Master enabled

8.2.2 I2C Target Address (IC_TAR)

Address: 0x18018004
Access: Read-Write
Reset: See field description

This register can be written only when the DW_APB_I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Bit	Bit Name	Type	Reset	Description	
31:12	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
11	SPECIAL	RW	0x0	This bit indicates whether software would like to perform a general call or start byte I2C command.	
				0	Ignore bit 10 GC_OR_START and use IC_TAR normally
				1	Perform special I2C command as specified in GC_OR_START bit
10	GC_OR_ START	RW	0x0	If bit 11 SPECIAL is set to 1, then this bit indicates whether a general call or start byte command is to be performed by the DW_APB_I2C.	
				0	General Call Address: After issuing a general call, only writes may be performed. Attempting to issue a read sets TX_ABRT. DW_APB_I2C remains in general call mode until the SPECIAL bit value is cleared.
				1	Start Byte
9:0	IC_TAR	RW	0x055	The target address for any master transactions. **The reset value of IC_TAR is equal to IC_DEFAULT_TAR_SLAVE_ADDR which indicates loopback mode.	

8.2.3 I2C HS Mode Master Code (IC_HS_MADDR)

Address: 0x1801800C
Access: Read-Write
Reset: See field description

This register holds the I2C HS master mode code address.

Bit	Bit Name	Type	Reset	Description
31:3	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
2:0	IC_HS_MADDR	RO/RW	0x1	IC_HS_MAR holds the value of the I2C HS mode master code. Valid values are from 0-7. This register goes away and becomes read-only returning 0 s if IC_MAX_SPEED_MODE = high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect

8.2.4 I2C Rx/Tx Data Buffer and Command (IC_DATA_CMD)

Address: 0x18018010
Access: Read-Write
Reset: See field description

This register contains the data buffer and commands for I2C Rx/Tx.

Bit	Bit Name	Type	Reset	Description
31:9	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
8	CMD	RW	0x0	This bit controls whether a read or a write is performed. For reads, the lower 8 (DAT) bits are ignored by the DW_APB_I2C. However, if the APB_DATA_WIDTH is 8, this dummy write is still required as there is coherency in this register. Reading this bit returns 0. Attempting to perform a read operation after a general call command has been sent results in TX_ABRT unless the SPECIAL bit in the IC_TAR register has been cleared. If this bit is written to a 1 after receiving RD_REQ, then a TX_ABRT occurs
				0 Write
				1 Read
7:0	DAT	RO	0x0	This register contains the data to be transmitted or received on the I2C bus. Read these bits to read out the data received on the I2C interface. Write these bits to send data out on the I2C interface.

8.2.5 Standard I2C Clock SCL High Count (IC_SS_SCL_HCNT)

Address: 0x18018014
Access: Read-Write
Reset: See field description

This register holds the standard speed I2C clock SCL high count.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:0	IC_SS_SCL_HCNT	RW	0x1D6	HCNT COUNT This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted, results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_APB_I2C. The lower byte must be programmed first, then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 6. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read-only.

8.2.6 Standard I2C Clock SCL Low Count (IC_SS_SCL_LCNT)

Address: 0x18018018
Access: Read-Write
Reset: See field description

This register holds the standard speed I2C clock SCL low count.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:0	IC_SS_SCL_ HCNT	RW	0x3C	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted, results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_ APB_I2C. The lower byte must be programmed first, then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 6. When the configuration parameter IC_HC_COUNT_ VALUES is set to 1, this register is read-only.

8.2.7 Fast I2C Clock SCL High Count (IC_FS_SCL_HCNT)

Address: 0x1801801C
Access: Read-Write
Reset: See field description

This register holds the fast speed I2C clock SCL high count.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:0	IC_FS_SCL_ HCNT	RW	0x82	This register must be set before any I2C bus transaction can take place to ensure proper I/ O timing. This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read only returning 0s if IC_MAX_ SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_APB_I2C. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 6. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

8.2.8 Fast I2C Clock SCL Low Count (IC_FS_SCL_LCNT)

Address: 0x18018020
Access: Read-Write
Reset: See field description

This register holds the fast speed I2C clock SCL low count.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:0	IC_FS_SCL_ LCNT	RW	0x190	This register must be set before any I2C bus transaction can take place to ensure proper I/ O timing. This register sets the SCL clock low-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. This register goes away and becomes read only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_ DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_APB_I2C. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 6. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

8.2.9 High Speed I2C Clock SCL High Count (IC_HS_SCL_HCNT)

Address: 0x18018024
Access: Read-Write
Reset: See field description

This register holds the high speed I2C clock SCL high count.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:0	IC_SS_SCL_ HCNT	RW	0x000C	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed. The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read only returning 0s if IC_MAX_SPEED_MODE = high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_ WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_APB_I2C. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 6. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

8.2.10 High Speed I2C Clock SCL Low Count (IC_HS_SCL_LCNT)

Address: 0x18018028
Access: Read-Write
Reset: See field description

This register holds the high speed I2C clock SCL low count.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:0	IC_SS_SCL_ HCNT	RW	0x0020	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. The SCL low time depends on the loading of the bus. For 100 pF loading, the SCL low time is 60ns; for 400pF loading, the SCL low time is 120 ns. This register goes away and becomes read only returning 0s if IC_MAX_SPEED_MODE = high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_ WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_APB_I2C. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 6. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.

8.2.11 I2C Raw Interrupt Status (IC_RAW_INTR_STAT)

Address: 0x1801802C
Access: Read-Write
Reset: See field description

This register holds the raw internal statistics of the I2C. Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the DW_APB_I2C.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
11	GEN_CALL	RW	0x0	Indicates that a general call request was received. The DW_APB_I2C stores the received data in the RX buffer.
10	START_DET	RW	0x0	Indicates whether a start condition has occurred on the I2C interface
9	STOP_DET	RW	0x0	Indicates whether a stop condition has occurred on the I2C interface
8	ACTIVITY	RW	0x0	This bit captures DW_APB_I2C activity and stays set until it is cleared, regardless of the DW_APB_I2C going idle.
7	RX_DONE	RW	0x0	When the DW_APB_I2C is acting as a slave transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.

6	TX_ABRT	RW	0x0	In general, this bit is set to 1 when the DW_APB_I2C acting as a master is unable to complete a command that the processor has sent. The conditions that set TX_ABRT are: 1. No slave acknowledges after the address is sent. 2. The addressed slave does not acknowledge a byte of data. 3. Arbitration is lost. 4. Attempting to send a master command when configured only to be a slave. 5. IC_RESTART_EN bit in the IC_CON register is set to 0 (restart condition disabled), and the processor attempts to issue an I^2C function that is impossible to perform without using restart conditions, and those conditions are: a. High-speed master code is acknowledge. b. Start byte is acknowledged. c. General call address is not acknowledged. d. When a read request interrupt occurs and the processor has previously placed data in the TX buffer that has not been transmitted yet. This data could have been intended to service a multi-byte RD_REQ that ended up having fewer numbers of bytes requested. Or, if IC_RESTART_EN is disabled and the I2C loses control of the bus between transfers and is then accessed as a slave-transmitter. e. If a read command is issued after a general call command has been issued. Disabling the I^2C reverts it back to normal operation. f. If the processor attempts to issue read command before a RD_ REQ is serviced. Anytime this bit is set, the contents of the transmit and receive buffers are flushed
5	RD_REQ	RW	0x0	This bit is set to 1 when the DW_APB_I2C is acting as slave and another I^2C master is attempting to read data from our module. The DW_APB_I2C holds the I^2C bus in waiting state (SCL=0) until this interrupt is serviced. The processor must acknowledge this interrupt and then write the requested data to the IC_DATA_CMD register.
4	TX_EMPTY	RW	0x0	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. It is automatically cleared by hardware when buffer level goes above the threshold.
3	TX_OVER	RW	0x0	Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_ DEPTH and the processor attempts to issue another I^2C command by writing to the IC_DATA_CMD register.
2	RX_FULL	RW	0x0	Set when the transmit buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold.
1	RX_OVER	RW	0x0	Set if the receive buffer was completely filled to IC_RX_BUFFER_DEPTH and more data arrived. That data is lost.
0	RX_UNDER	RW	0x0	Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

8.2.12 I2C Interrupt Mask (IC_INTR_MASK)

Address: 0x18018030
Access: Read-Write
Reset: See field description

This register's bits mask their corresponding interrupt status bits. They are active high; a value of 0 prevents a bit from generating an interrupt.

Bit	Bit Name	Type	Reset	Description
31:12	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
11	M_GEN_CALL	RW	0x0	Masks this bit in the I2C Interrupt Status (IC_INTR_STAT) register
10	M_START_DET	RW	0x0	Masks this bit in the IC_INTR_STAT register
9	M_STOP_DET	RW	0x0	Masks this bit in the IC_INTR_STAT register
8	M_ACTIVITY	RW	0x0	Masks this bit in the IC_INTR_STAT register
7	M_RX_DONE	RW	0x1	Masks this bit in the IC_INTR_STAT register
6	M_TX_ABRT	RW	0x1	Masks this bit in the IC_INTR_STAT register
5	M_RD_REQ	RW	0x1	Masks this bit in the IC_INTR_STAT register
4	M_TX_EMPTY	RW	0x1	Masks this bit in the IC_INTR_STAT register
3	M_TX_OVER	RW	0x1	Masks this bit in the IC_INTR_STAT register
2	M_RX_FULL	RW	0x1	Masks this bit in the IC_INTR_STAT register
1	M_RX_OVER	RW	0x1	Masks this bit in the IC_INTR_STAT register
0	M_RX_UNDER	RW	0x1	Masks this bit in the IC_INTR_STAT register

8.2.13 I2C Interrupt Status (IC_INTR_STAT)

Address: 0x18018034
Access: Read-Write
Reset: See field description

This register denotes the interrupt status of the I2C.

Bit	Bit Name	Type	Reset	Description
31:12	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
11	R_GEN_CALL	RW	0x0	Indicates that a general call request was received. The DW_APB_I2C stores the received data in the RX buffer
10	R_START_DET	RW	0x0	Indicates whether a start condition has occurred on the I2C interface
9	R_STOP_DET	RW	0x0	Indicates whether a stop condition has occurred on the I2C interface
8	R_ACTIVITY	RW	0x0	This bit captures DW_APB_I2C activity and stays set until it is cleared, regardless of the DW_APB_I2C going idle.
7	R_RX_DONE	RW	0x0	When the DW_APB_I2C is acting as a slave transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.

6	R_TX_ABRT	RW	0x0	In general, this bit is set to 1 when the DW_APB_I2C acting as a master is unable to complete a command that the processor has sent. The conditions that set TX_ABRT are: 1. No slave acknowledges after the address is sent. 2. The addressed slave does not acknowledge a byte of data. 3. Arbitration is lost. 4. Attempting to send a master command when configured only to be a slave. 5. IC_RESTART_EN bit in the I2C Configuration (IC_CON) register is set to 0 (restart condition disabled), and the processor attempts to issue an I^2C function that is impossible to perform without using restart conditions, and those conditions are: a. high-speed master code is acknowledge. b. start byte is acknowledged. c. general call address is not acknowledged. d. when a read request interrupt occurs and the processor has previously placed data in the Tx buffer that has not been transmitted yet. This data could have been intended to service a multi-byte RD_REQ that ended up having fewer numbers of bytes requested. Or, if IC_RESTART_EN is disabled and the I^2C loses control of the bus between transfers and is then accessed as a slave-transmitter. e. if a read command is issued after a general call command has been issued. Disabling the I^2C reverts it back to normal operation. f. if the processor attempts to issue read command before a RD_REQ is serviced. Anytime this bit is set, the contents of the transmit and receive buffers are flushed.
5	R_RD_REQ	RW	0x0	This bit is set to 1 when the DW_APB_I2C is acting as slave and another I^2C master is attempting to read data from our module. The DW_APB_I2C holds the I^2C bus in waiting state (SCL=0) until this interrupt is serviced. The processor must acknowledge this interrupt and then write the requested data to the I2C Rx/Tx Data Buffer and Command (IC_DATA_CMD) register.
4	R_TX_EMPTY	RW	0x0	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the I2C Transmit FIFO Threshold (IC_TX_TL) register. It is automatically cleared by hardware when buffer level goes above the threshold.
3	R_TX_OVER	RW	0x0	Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I^2C command by writing to the I2C Rx/Tx Data Buffer and Command (IC_DATA_CMD) register.
2	R_RX_FULL	RW	0x0	Set when the transmit buffer reaches or goes above the RX_TL threshold in the I2C Receive FIFO Threshold (IC_RX_TL) register. It is automatically cleared by hardware when buffer level goes below the threshold.
1	R_RX_OVER	RW	0x0	Set if the receive buffer was completely filled to IC_RX_BUFFER_DEPTH and more data arrived. That data is lost.
0	R_RX_UNDER	RW	0x0	Set if the processor attempts to read the receive buffer when it is empty by reading from the I2C Rx/Tx Data Buffer and Command (IC_DATA_CMD) register.

8.2.14 I2C Receive FIFO Threshold (IC_RX_TL)

Address: 0x18018038
Access: Read-Write
Reset: See field description

This register contains the threshold settings for the I2C receive FIFO.

Bit	Bit Name	Type	Reset	Description
31:8	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	RX_TL	RW	0x0	The receive FIFO Threshold Level controls the level of entries (or above) that triggers the RX_FULL interrupt. The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries. The core, in our case, is configured to use only 0-63

8.2.15 I2C Transmit FIFO Threshold (IC_TX_TL)

Address: 0x18018000
Access: Read-Write
Reset: See field description

This register contains the threshold settings for the I2C transmit FIFO.

Bit	Bit Name	Type	Reset	Description
31:8	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	TX_TL	RW	0x0	Transmit FIFO Threshold Level Controls the level of entries (or below) that trigger the TX_EMPTY interrupt. The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries. The core, in our case, is configured to use only 0-15

8.2.16 I2C Combined and Individual Interrupts Clear (IC_CLR_INTR)

Address: 0x18018040
Access: Read-Write
Reset: See field description

This register clears the combined and individual I2C interrupts.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_INTR	RW	0x0	Read this register to clear the combined interrupt, all individual interrupts, and the I2C TX Abort Source (IC_TX_ABRT_SOURCE) register.

8.2.17 I2C Clear RX_UNDER Interrupts (IC_CLR_RX_UNDER)

Address: 0x18018044
Access: Read-Only
Reset: See field description

This register clears the RX_UNDER interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_RX_UNDER	RO	0x0	Read this register to clear the RX_UNDER interrupt.

8.2.18 I2C Clear RX_OVER Interrupts (IC_CLR_RX_OVER)

Address: 0x18018048
Access: Read-Only
Reset: See field description

This register clears the RX_OVER interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_RX_OVER	RO	0x0	Read this register to clear the RX_OVER interrupt.

8.2.19 I2C Clear TX_OVER Interrupts (IC_CLR_TX_OVER)

Address: 0x1801804C
Access: Read-Only
Reset: See field description

This register clears the TX_OVER interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_TX_OVER	RO	0x0	Read this register to clear the TX_OVER interrupt.

8.2.20 I2C Clear RD_REQ Interrupts (IC_CLR_RD_REQ)

Address: 0x18018050
Access: Read-Only
Reset: See field description

This register clears the RD_REQ interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_RD_REQ	RO	0x0	Read this register to clear the RD_REQ interrupt.

8.2.21 I2C Clear TX_ABRT Interrupts (IC_CLR_TX_ABRT)

Address: 0x18018054
Access: Read-Only
Reset: See field description

This register clears the TX_ABRT interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_TX_ABRT	RO	0x0	Read this register to clear the TX_ABRT interrupt and IC_TX_ABRT_SOURCE.

8.2.22 I2C Clear RX_DONE Interrupts (IC_CLR_RX_DONE)

Address: 0x18018058
Access: Read-Only
Reset: See field description

This register clears the RX_DONE interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_RX_DONE	RO	0x0	Read this register to clear the RX_DONE interrupt

8.2.23 I2C Clear ACTIVITY Interrupts (IC_CLR_ACTIVITY)

Address: 0x1801805C
Access: Read-Only
Reset: See field description

This register clears the ACTIVITY status interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_ACTIVITY	RO	0x0	Read this register to get the status of the ACTIVITY interrupt. This bit is automatically cleared by hardware

8.2.24 I2C Clear STOP_DET Interrupts (IC_CLR_STOP_DET)

Address: 0x18018060
Access: Read-Only
Reset: See field description

This register clears the STOP_DET interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_STOP_DET	RO	0x0	Read this register to clear the STOP_DET interrupt

8.2.25 I2C Clear START_DET Interrupts (IC_CLR_START_DET)

Address: 0x18018064
Access: Read-Only
Reset: See field description

This register clears the START_DET interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_START_DET	RO	0x0	Read this register to clear the START_DET interrupt

8.2.26 I2C Clear GEN_CALL Interrupts (IC_CLR_GEN_CALL)

Address: 0x18018068
Access: Read-Only
Reset: See field description

This register clears the GEN_CALL interrupts register.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	CLR_GEN_CALL	RO	0x0	Read this register to clear the GEN_CALL interrupt

8.2.27 I2C Enable (IC_ENABLE)

Address: 0x1801806C
Access: Read-Write
Reset: See field description

This registers enables I2C.

Bit	Bit Name	Type	Reset	Description
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	ENABLE	RW	0x0	Controls whether the DW_APB_I2C is enabled. Writing a 1 enables the DW_APB_I2C, and writing a 0 disables it. Software should not disable the DW_APB_I2C while it is active. The ACTIVITY bit can be polled to determine if the DW_APB_I2C is active. If the module was transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module was receiving, the DW_APB_I2C stops the current transfer at the end of the current byte and does not acknowledge the transfer. In systems with asynchronous PCLK and IC_CLK (IC_CLK_TYPE = 1), there is a two IC_CLK delay when enabling or disabling the DW_APB_I2C.

8.2.28 I2C Transfer and FIFO Status (IC_STATUS)

Address: 0x18018070
Access: Read-Write
Reset: See field description

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt.

Bit	Bit Name	Type	Reset	Description	
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
4	REF	RW	0x0	Receive FIFO completely Empty. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty locations, this bit is cleared.	
				0	Receive FIFO is not full
				1	Receive FIFO is full
3	RFNE	RW	0x0	Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. This bit can be polled by software to completely empty the receive FIFO.	
				0	Receive FIFO is empty
				1	Receive FIFO is not empty
2	TFE	RW	0x1	Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.	
				0	Transmit FIFO is not empty
				1	Transmit FIFO is empty
1	TFNF	RW	0x1	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.	
				0	Transmit FIFO is full
				1	Transmit FIFO is not full
0	ACTIVITY	RW	0x0	I2C activity status	

8.2.29 I2C Transmit FIFO Level (IC_TXFLR)

Address: 0x18018074
Access: Read-Only
Reset: See field description

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared when the I2C is disabled, whenever there is a transmit abort, or whenever the Slave Bulk Transfer mode is aborted. It increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

Bit	Bit Name	Type	Reset	Description
31:4	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
3:0	TX_FLR	RW	0x0	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

8.2.30 I2C Receive FIFO Level (IC_RXFLR)

Address: 0x18018078
Access: Read-Only
Reset: See field description

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared when the I2C is disabled, whenever there is a transmit abort, or whenever the Slave Bulk Transfer mode is aborted. It increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

Bit	Bit Name	Type	Reset	Description
31:4	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
3:0	RX_FLR	RW	0x0	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO

8.2.31 I2C Soft Reset (IC_SRESET)

Address: 0x1801807C
Access: Read-Write
Reset: See field description

This register is used to issue a soft reset to the master and/or the slave state machines. Reading this register does not clear it; it is automatically cleared by hardware.

Bit	Bit Name	Type	Reset	Description
31:3	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
2	IC_SLAVE_SRST	RW	0x0	Issues a soft reset to the slave state machines. 1 = perform the reset
1	IC_MASTER_SRST	RW	0x0	Issues a soft reset to the master state machines. 1 = perform the reset
0	IC_SRST	RW	0x0	Issues a soft reset to the master and slave state machines.

8.2.32 I2C TX Abort Source (IC_TX_ABRT_SOURCE)

Address: 0x18018080
Access: Read-Write
Reset: See field description

This register has 16 bits that indicate the source of the TX_ABRT signal, This register is cleared whenever the processor reads it or when the processor issues a clear signal to all interrupts.

Bit	Bit Name	Type	Reset	Description
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
15	ABRT_SLVRD_ INTX	RW	0x0	Writing a 1 to this bit denotes a slave requesting data to TX and the user writing a read command into the TX_FIFO (9th bit is a 1)
14	ABRT_SLV_ ARBLOST	RW	0x0	Writing a 1 to this bit denotes a slave lost the bus while transmitting data to a remote master. IC_TX_ABRT[12] will be set at the same time
13	ABRT_ SLVFLUSH_ TXFIFO	RW	0x0	Writing a 1 to this bit denotes a slave has received a read command and some data exists in the TX_FIFO so the slave issues a TX_ABRT to flush old data in TX_FIFO.
12	ARB_LOST	RW	0x0	Writing a 1 to this bit denotes a Master has lost arbitration, or if TX_ ABRT_SRC[12] is also set, then the slave transmitter has lost arbitration
11	ARB_MASTER_ DIS	RW	0x0	Writing a 1 to this bit denotes a user attempted to use a disabled Master
10	ABRT_10B_RD_ NORSTRT	RW	0x0	Writing a 1 to this bit disables the restart (IC_RESTART_EN bit (ic_ con[5]) = 0) and the Master sends a read command in 10-bit addressing mode.
9	ABRT_SBYTE_ NORSTRT	RW	0x0	Writing a 1 to this bit disables the restart (IC_RESTART_EN bit (ic_ con[5]) = 0) and the user is trying to send a Start Byte.
8	ABRT_HS_ NORSTRT	RW	0x0	Writing a 1 to this bit disables the restart (IC_RESTART_EN bit (ic_ con[5]) = 0) and the user is trying to use the master to send data in High Speed mode.
7	ABRT_SBYTE_ ACKDET	RW	0x0	Writing a 1 to this bit denotes a Master has sent a Start Byte and the Start Byte was acknowledged (wrong behavior)
6	ABRT_HS_ ACKDET	RW	0x0	Writing a 1 to this bit denotes a Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior)
5	ABRT_GCALL_ READ	RW	0x0	Writing a 1 to this bit denotes a Master sent a general call but the user programmed the byte following the G.CALL to be a read from the bus (9th bit is set to 1)
4	ABRT_GCALL_ NOACK	RW	0x0	Writing a 1 to this bit denotes a Master sent a general call and no slave on the bus responded with an acknowledgement
3	ABRT_TX_DATA_ NOACK	RW	0x0	Writing a 1 to this bit denotes a Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	ABRT_10ADDR2_ NOACK	RW	0x0	Writing a 1 to this bit denotes a Master is in 10-bit address mode and the 2nd address byte of the 10-bit address was not acknowledged by any slave.
1	ABRT_10ADDR1_ NOACK	RW	0x0	Writing a 1 to this bit denotes a Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave
0	ABRT_7B_ADDR_ NOACK	RW	0x0	Writing a 1 to this bit denotes a Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

8.3 UART0 (Low-Speed) Registers

Table 8-4 summarizes the UART0 registers for the QCA9563.

Table 8-4 UART0 (Low-Speed) Registers Summary

Address	Name	Description	Page
0x18020000	RBR	Receive Buffer	page 120
0x18020000	THR	Transmit Holding	page 121
0x18020000	DLL	Divisor Latch Low	page 121
0x18020004	DLH	Divisor Latch High	page 122
0x18020004	IER	Interrupt Enable	page 122
0x18020008	IIR	Interrupt Identity	page 123
0x18020008	FCR	FIFO Control	page 124
0x1802000C	LCR	Line Control	page 125
0x18020010	MCR	Modem Control	page 126
0x18020014	LSR	Line Status	page 126
0x18020018	MSR	Modem Status	page 127

8.3.1 Receive Buffer (RBR)

Address: 0x18020000
Access: Read-Only
Reset: 0x0

This read-only register contains the data byte received on the serial input port (SIN). The data in this register is only valid if the Data Ready (DR) bit in the Line Status Register (LSR) is set. In the non-FIFO mode (FIFO_MODE = 0), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. In FIFO mode (FIFO_MODE = 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already residing in the FIFO is full and this register will be preserved but any incoming data will be lost. An overrun error will also occur

Bit	Bit Name	Description
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.
7:0	RBR	The receive buffer register value

8.3.2 Transmit Holding (THR)

Address: 0x18020004
Access: Write-Only
Reset: 0x0

This write-only register contains data to be transmitted on the serial port (s_{OUT}). Data can be written to the THR any time the THR Empty (THRE) bit of the Line Status Register is set. If FIFOs are not enabled and the THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFOs are enabled and the THRE is set, up to sixteen characters of data may be written to the THR before the FIFO is full. Attempting to write data when the FIFO is full results in the write data being lost.

Bit	Bit Name	Description
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.
7:0	THR	The transmit buffer value

8.3.3 Divisor Latch Low (DLL)

Address: 0x18020008
Access: Read/Write
Reset: 0x0

This register, in conjunction with the Divisor Latch High (DLH), page 8-122 register forms a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART0. It is accessed by first setting the DLAB bit (bit [7]) in the Line Control (LCR), page 8-125 register. The output baud rate is equal to the input clock frequency divided by sixteen times (*16) the value of the baud rate divisor:

baud = (clock freq)/ (16 * divisor)

Bit	Bit Name	Type	Reset	Description
31:8	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	DLL	RW	0x0	Divisor latch low

8.3.4 Divisor Latch High (DLH)

Address: 0x1802000C
Access: Read/Write
Reset: 0x0

This register, in conjunction with the Divisor Latch Low (DLL), page 8-121 register forms a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART0. It is accessed by first setting the DLAB bit (bit [7]) in the Line Control (LCR), page 8-125 register. The output baud rate is equal to the input clock frequency divided by sixteen times (*16) the value of the baud rate divisor:

baud = (clock freq)/ (16 * divisor)

Bit	Bit Name	Description
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.
7:0	DLH	Divisor latch high

8.3.5 Interrupt Enable (IER)

Address: 0x18020010
Access: Read/Write
Reset: 0x0

This register contains four bits that enable the generation of interrupts.

Bit	Bit Name	Description
31:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3	EDDSI	Enable modem status interrupt
2	ELSI	Enable receiver line status interrupt
1	ETBEI	Enable register empty interrupt
0	ERBFI	Enable received data available interrupt

8.3.6 Interrupt Identity (IIR)

Address: 0x18020014
Access: Read-Only
Reset: 0x0

This register identifies the source of an interrupt. The two upper bits of the register are FIFO-enabled bits.

Bit	Bit Name	Description	
31:8	RES	Reserved	
7:6	FIFO_STATUS	FIFO enable status bits	
		00	FIFO disabled
		11	FIFO enabled
5:4	RES	Reserved. Must be written with zero. Contains zeros when read.	
3:0	IID	Used to identify the source of the interrupt	
		0000	Modem status changed
		0001	No interrupt pending
		0010	THR empty
		0100	Received data available
		0110	Receiver status
		1100	Character time out

8.3.7 FIFO Control (FCR)

Address: 0x18020018
Access: Write-Only
Reset: 0x0

This register sets the parameters for FIFO control. This register will also return current time values.

If FIFO mode is 0, this register has no effect. If FIFO mode is 1, this register will control the read and write data FIFO operation and the mode of operation for the DMA signals TXRDY_N and RXRDY_N.

If FIFO mode is enabled (FIFO mode = 1 and bit [0] is set to 1), bit [3], bit [6], and bit [7] are active.

Bit	Bit Name	Description	
31:8	RES	Reserved	
7:6	RCVR_TRIG	Sets the trigger level in the receiver FIFO for both the RXRDY_N signal and the Enable received data available interrupt (ERBFI)	
		00	1 byte in FIFO
		01	4 bytes in FIFO
		10	8 bytes in FIFO
		11	14 bytes in FIFO
5:4	RES	Reserved	
3	DMA_MODE	This bit determines the DMA signalling mode for TXRDY_N and RXRDY_N output signals	
2	XMIT_FIFO_RST	Writing this bit resets and flushes data in the transmit FIFO	
1	RCVR_FIFO_RST	Writing this bit resets and flushes data in the receive FIFO	
0	FIFO_EN	Setting this bit enables the transmit and receive FIFOs. The FIFOs are also reset any time this bit changes its value.	

8.3.8 Line Control (LCR)

Address: 0x1802001C
Access: Read/Write
Reset: 0x0

This register controls the format of the data that is transmitted and received by the UART0 controller.

Bit	Bit Name	Description	
31:8	RES	Reserved	
7	DLAB	The divisor latch address bit. Setting this bit enables reading and writing of the Divisor Latch Low (DLL), page 8-121 and Divisor Latch High (DLH), page 8-122 registers to set the baud rate of the UART0. This bit must be cleared after the initial baud rate setup in order to access the other registers.	
6	BREAK	Setting this bit sends a break signal by holding the SOUT line low (when not in loopback mode, as determined by Modem Control (MCR), page 8-126 register bit [4]), until the BREAK bit is cleared. When in loopback mode, the break condition is internally looped back to the receiver.	
5	RES	Reserved	
4	EPS	Used to set the even/odd parity. If parity is enabled, this bit selects between even and odd parity. If this bit is a logic 1, an even number of logic 1s are transmitted or checked. If this bit is a logic 0, an odd number of logic 1s are transmitted or checked.	
3	PEN	Used to enable parity when set	
2	STOP	Used to control the number of stop bits transmitted. If this bit is a logic 0, one-stop bit is transmitted in the serial data. If this bit is a logic 1 and the data bits are set to 5, one and a half stop bits are generated. Otherwise, two stop bits are generated and transmitted in the serial data out.	
1:0	CLS	Used to control the number of bits per character	
		00	5 bits
		01	6 bits
		10	7 bits
		11	8 bits

8.3.9 Modem Control (MCR)

Address: 0x18020020
Access: Read/Write
Reset: See field description

This register controls the interface with the modem.

Bit	Bit Name	Reset	Description
31:6	RES	0x0	Reserved
5	LOOPBACK	0x1	When set, the data on the SOUT line is held HIGH, while the serial data output is looped back to the SIN line, internally. In this mode, all the interrupts are fully functional. This feature is also used for diagnostic purposes. The modem control inputs (DSR_L, CTS_L, RI_L, DCD_L) are disconnected and the four modem control outputs (DTR_L, RTS_L, OUT1_L, OUT1_L) are looped back to the inputs, internally.
4	RES	0x0	Reserved
3	OUT2	0x1	Used to drive the UART0 output UART0_OUT2_L
2	OUT1	0x1	Used to drive the UART0 output UART0_OUT1_L
1	RTS	0x1	Used to drive the UART0 output RTS_L
0	DTR	0x1	Used to drive the UART0 output DTR_L. Not supported.

8.3.10 Line Status (LSR)

Address: 0x18020024
Access: Read/Write
Reset: 0x0

This register contains the status of the receiver and transmitter data transfers. This status may be read by the user at any time.

Bit	Bit Name	Description
31:8	RES	Reserved
7	FERR	The error in receiver FIFO bit. This bit is only active when the FIFOs are enabled. This bit is set when there is at least one parity error, framing error or break in the FIFO. This bit is cleared when the LSR is read AND the character with the error is at the top of the receiver FIFO AND there are no subsequent errors in the FIFO.
6	TEMT	The transmitter empty bit. This bit is set in FIFO mode whenever the Transmitter Shift Register and the FIFO are both empty. In non-FIFO mode, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	THRE	The transmitter holding register empty bit. When set, indicates the UART0 controller can accept a new character for transmission. This bit is set whenever data is transferred from the THR to the transmit shift register and no new data has been written to the THR. This also causes a THRE Interrupt to occur, if enabled.

4	BI	The break interrupt bit. This bit is set whenever the serial input (SIN) is held in a logic zero state for longer than the sum of (start time + data bits + parity + stop bits). A break condition on SIN causes one, and only one character, consisting of all zeros which will be received by the UART0. In FIFO mode, the character associated with the break condition is carried through FIFO and revealed when the character reaches the top of FIFO. Reading the LSR clears the BI bit. In non-FIFO mode, the BI direction occurs immediately and continues until the LSR has been read.
3	FE	The framing error bit. This bit is set whenever there is a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In FIFO mode, the framing error associated with the character received will come to the top of FIFO so it can be noticed. The OE, PE and FE bits are reset when a read of the LSR is performed.
2	PE	The parity error bit. This bit is set whenever there is a parity bit error in the receiver if the Parity Enable (PEN) bit in the LCR is set. In FIFO mode, the parity error associated with the character received will come to the top of FIFO so it can be noticed.
1	OE	The overrun error bit. When set, indicates an overrun error occurred because a new data character was received before the previous data was read. In non-FIFO mode, it is set when a new character arrives in the receiver before the previous character has been read from the RBR. In FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives in the receiver. The data in FIFO is retained and the data in the receive shift register is lost.
0	DR	The data ready bit. When set, indicates that the receiver contains at least one character in the RBR or the receiver FIFO. This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty when in FIFO mode.

8.3.11 Modem Status (MSR)

Address: 0x18020028
Access: Read/Write
Reset: 0x0

This register contains the current status of the modem control input lines and notes whether they have changed.

Bit	Bit Name	Description
31:8	RES	Reserved
7	DCD	Contains information on the current state of the modem control lines; complement of DCD_L
6	RI	Contains information on the current state of the modem control lines; complement of RI_L
5	DSR	Contains information on the current state of the modem control lines; complement of DSR_L
4	CTS	Contains information on the current state of the modem control lines; complement of CTS_L
3	DDCD	Notes whether modem control line DCD_L changed since the last time the CPU read the MSR
2	TERI	Indicates whether RI_L changed from an active low to inactive high since the last time MSR was read
1	DDSR	Notes whether DSR_L has changed since the last time the CPU read the MSR
0	DCTS	Notes whether CTS_L has changed since the last time the CPU read the MSR

8.4 USB Registers

Table 8-5 summarizes the USB registers for the QCA9563.

Table 8-5 USB Registers Summary

Address	Name	Description	Page
0x18030000	USB_PWRCTL	USB Power Control	page 128
0x18030004	USB_CONFIG	USB Configuration Control	page 129
0x18030008	USB_DEV_SUSPEND_CTRL	USB Device Suspend Control	page 129
0x1803000C	SUSPEND_RESUME_CNTR	USB Suspend Resume Counters	page 130
0x18030010	USB2_PWRCTL	USB2 Power Control	page 130
0x18030014	USB2_CONFIG	USB2 Configuration Control	page 131
0x1803001C	ARBITER_CONFIG	Arbiter Configuration	page 131

8.4.1 USB Power Control (USB_PWRCTL)

Address: 0x18030000
Access: Read/Write
Reset: 0x0

This register contains status and control bits for USB power control.

Bit	Bit Name	Description
31:7	RES	Reserved
6	WAKEUP_STATUS	Final wakeup status that wakes up the USB core
5	USR_WAKEUP	User wakeup signal. Input that clears suspend output. All suspend outputs are synchronized to the appropriate clock and this input will not propagate to the suspend outputs until the related clock begins running. Thus it must remain asserted until the related suspend output transitions to zero.
4	WAKE_OVRCURR_EN	Wakeup status because of power fault
3	WAKE_DSCNNT_EN	Wakeup status because of a disconnect event
2	WAKE_CNNT_EN	Wakeup status because of connect event
1	SUSPEND_CLR	Output to notify of software commanded wake up; this bit is not synchronized and remains set until the SUSPEND bit (bit [0]) of this register is cleared.
0	SUSPEND	Suspend output synchronized to the XCVR_CLK.

8.4.2 USB Configuration Control (USB_CONFIG)

Address: 0x18030004
Access: Read/Write
Reset: 0x1E

This register controls the basic configuration for the USB controller.

Bit	Bit Name	Description	
31:5	RES	Reserved	
4	HOST_OR_DEVICE	0	Reserved
		1	Indicates operation in host mode
3	AHB_HRDATA_SWAP	Swaps the read data on AHB bus	
2	AHB_HWDATA_SWAP	Swaps the write data on the AHB bus	
1	HS_MODE_EN	Enables high speed mode	
0	UTMI_PHY_EN	Asserted when selecting the UTMI mode	

8.4.3 USB Device Suspend Control (USB_DEV_SUSPEND_CTRL)

Address: 0x18030008
Access: Read/Write
Reset: 0x0

This register contains the bits to control the suspend related parameters and enables SUSPEND operation.

Bit	Bit Name	Description	
31:3	RES	Reserved	
2	GPIO_SUSP_POLARITY	Control to determine the polarity of the suspend signal coming on GPIO.	
		0	Suspend is active low
		1	Suspend is active high
1	RESET_ON_RESUME	If set to 1 before USB suspend, then the USB host triggers a FULL_CHIP_ RESET on a RESUME signal	
0	MASTER_SUSP_EN	Master enable for suspend that puts the entire chip in power down mode. The CPU must set this bit as the last operation before moving to suspend/power-down state	

8.4.4 USB Suspend Resume Counters (SUSPEND_RESUME_CNTR)

Address: 0x1803000C
Access: Read/Write
Reset: 0x1F00EA60

This register contains counters that set up timings for suspend entry and exit.

Bit	Bit Name	Description
31:24	SUSP_ENTER_CNTR	Countdown timer. Forces device entry to suspend once the counter reaches zero.
23:18	RES	Reserved
17:0	SUSP_EXIT_CNTR	Countdown timer for suspend exit. Waits until it reaches zero before resume event is signalled to CPU.

8.4.5 USB2 Power Control (USB2_PWRCTL)

Address: 0x18030010

Access: Read/Write

Reset: 0x0

This register contains status and control bits for USB2 power control

Bit	Bit Name	Description
31:7	RES	Reserved
6	WAKEUP_STATUS	Final wakeup status that wakes up the USB2 core
5	USR_WAKEUP	User wakeup signal. Input that clears suspend output. All suspend outputs are synchronized to the appropriate clock and this input will not propagate to the suspend outputs until the related clock begins running. Thus it must remain asserted until the related suspend output transitions to zero.
4	WAKE_OVRCURR_EN	Wakeup status because of power fault
3	WAKE_DSCNNT_EN	Wakeup status because of a disconnect event
2	WAKE_CNNT_EN	Wakeup status because of connect event
1	SUSPEND_CLR	Output to notify of software commanded wake up; this bit is not synchronized and remains set until the SUSPEND bit (bit [0]) of this register is cleared.
0	SUSPEND	Suspend output synchronized to the XCVR_CLK.

8.4.6 USB2 Configuration Control (USB2_CONFIG)

Address: 0x18030014

Access: Read/Write

Reset: 0x0

This register controls the basic configuration for the USB2 controller.

Bit	Bit Name	Reset	Description	
31:5	RES	0x1	Reserved	
4	HOST_OR_DEVICE	0x1	0	Indicates operation in device mode
			1	Indicates operation in host mode
3	AHB_HRDATA_SWAP	0x1	Swaps the read data on AHB bus	
2	AHB_HWDATA_SWAP	0x1	Swaps the write data on the AHB bus	
1	HS_MODE_EN	0x1	Enables high speed mode	
0	UTMI_PHY_EN	0x0	Asserted when selecting the UTMI mode	

8.4.7 Arbiter Configuration (ARBITER_CONFIG)

Address: 0x1803001C
Access: Read/Write
Reset: 0x48

This register contains counters that set up timings for suspend entry and exit.

Bit	Bit Name	Description
31:11	RES	Reserved
10	DISABLE_BURST_CNT	Disables the switching grant feature if the max burst count is crossed
9:0	MAX_BURST_CNT	Indicates the max burst count for one requestor.

8.5 GPIO Registers

Table 8-6 summarizes the GPIO registers for the QCA9563.

Table 8-6 General Purpose I/O (GPIO) Registers Summary

Address	Name	Description	Page
0x18040000	GPIO_OE	GPIO Output Enable	page 132
0x18040004	GPIO_IN	GPIO Input Value	page 133
0x18040008	GPIO_OUT	GPIO Output Value	page 133
0x1804000C	GPIO_SET	GPIO Per Bit Set	page 133
0x18040010	GPIO_CLEAR	GPIO Per Bit Clear	page 133
0x18040014	GPIO_INT	GPIO Interrupt Enable	page 134
0x18040018	GPIO_INT_TYPE	GPIO Interrupt Type	page 134
0x1804001C	GPIO_INT_POLARITY	GPIO Interrupt Polarity	page 134
0x18040020	GPIO_INT_PENDING	GPIO Interrupt Pending	page 134
0x18040024	GPIO_INT_MASK	GPIO Interrupt Mask	page 135
0x1804002C	GPIO_OUT_FUNCTION0	GPIO pins 0, 1, 2, 3 Output Multiplexing	page 135
0x18040030	GPIO_OUT_FUNCTION1	GPIO pins 4, 5, 6, 7 Output Multiplexing	page 135
0x18040034	GPIO_OUT_FUNCTION2	GPIO pins 8, 9, 10, 11 Output Multiplexing	page 136
0x18040038	GPIO_OUT_FUNCTION3	GPIO pins 12, 13, 14, 15 Output Multiplexing	page 136
0x1804003C	GPIO_OUT_FUNCTION4	GPIO pins 16, 17, 18, 19 Output Multiplexing	page 136
0x18040040	GPIO_OUT_FUNCTION5	GPIO pins 20, 21, 22 Output Multiplexing	page 137
0x18040044	GPIO_IN_ENABLE0	UART0_SIN Multiplexing	page 137
0x18040050	GPIO_IN_ENABLE3	MDIO Muxing	page 137
0x1804006C	GPIO_FUNCTION	Controls JTAG in GPIO	page 138
0x18040070	GPIO_IN_ETH_SWITCH_LED	GPIO Ethernet LED Routing Select	page 138

8.5.1 GPIO Output Enable (GPIO_OE)

Address: 0x18040000
Access: Read/Write
Reset: 0x3F30B

Bit	Bit Name	Description	
31:0	OE	Per bit output enable, where bit [22] sets GPIO22, bit [21] sets GPIO21, bit [20] sets GPIO20, and so on.	
		0	The bit is used as output
		1	Enables the bit as input

8.5.2 GPIO Input Value (GPIO_IN)

Address: 0x18040004
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	IN	Current values of each of the GPIO pins, where bit[22] sets GPIO22, bit [21] sets GPIO21, bit [20] sets GPIO20, and so on.

8.5.3 GPIO Output Value (GPIO_OUT)

Address: 0x18040008
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	OUT	Driver output value. If the corresponding bit in the GPIO_OE register is set to 0, the GPIO pin will drive the value in the corresponding bit of this register.

8.5.4 GPIO Per Bit Set (GPIO_SET)

Address: 0x1804000C
Access: Write-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	SET	On a write, any bit that is set causes the corresponding GPIO bit to be set; any bit that is not set will have no effect.

8.5.5 GPIO Per Bit Clear (GPIO_CLEAR)

Address: 0x18040010
Access: Write-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	CLEAR	On a write, any bit that is set causes the corresponding GPIO bit to be cleared; any bit that is not set will have no effect.

8.5.6 GPIO Interrupt Enable (GPIO_INT)

Address: 0x18040014
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	INT	Each bit that is set is considered an interrupt ORd into the GPIO interrupt line.

8.5.7 GPIO Interrupt Type (GPIO_INT_TYPE)

Address: 0x18040018
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:0	TYPE	Interrupt type	
		0	Indicates the bit is a edge-sensitive interrupt
		1	Indicates the bit is an level-sensitive interrupt

8.5.8 GPIO Interrupt Polarity (GPIO_INT_POLARITY)

Address: 0x1804001C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:0	POLARITY	Interrupt polarity	
		0	Indicates that the interrupt is active low (level) or falling edge (edge)
		1	Indicates that the interrupt is active high (level) or rising edge (edge)

8.5.9 GPIO Interrupt Pending (GPIO_INT_PENDING)

Address: 0x18040020
Access: Read/Write (See field description)
Reset: 0x0

Bit	Bit Name	Description
31:0	PENDING	For each bit, indicates that an interrupt is currently pending for the particular GPIO; for edge-sensitive interrupts, this register is read-with-clear.

8.5.10 GPIO Interrupt Mask (GPIO_INT_MASK)

Address: 0x18040024
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	MASK	For each bit that is set, the corresponding interrupt in the register GPIO Interrupt Pending (GPIO_INT_PENDING), page 8-134 is passed on to the central interrupt controller.

8.5.11 GPIO Function 0 (GPIO_OUT_FUNCTION0)

Address: 0x1804002C
Access: Read/Write
Reset: 0x0

MUX values for GPIO[3:0].
Note that JTAG pins are available only in GPIO[3:0].

Bit	Bit Name	GPIO	Default Function	Description
31:24	ENABLE_GPIO_3	GPIO3	Reserved	Selected programmed value is available in GPIO3
23:16	ENABLE_GPIO_2	GPIO2	Reserved	Selected programmed value is available in GPIO2
15:8	ENABLE_GPIO_1	GPIO1	Reserved	Selected programmed value is available in GPIO1
7:0	ENABLE_GPIO_0	GPIO0	Reserved	Selected programmed value is available in GPIO0

8.5.12 GPIO Function 1 (GPIO_OUT_FUNCTION1)

Address: 0x18040030
Access: Read/Write
Reset: 0x0

MUX values for GPIO[7:4].

Bit	Bit Name	GPIO	Default Function	Description
31:24	ENABLE_GPIO_7	GPIO7	Reserved	Selected programmed value is available in GPIO7
23:16	ENABLE_GPIO_6	GPIO6	Reserved	Selected programmed value is available in GPIO6
15:8	ENABLE_GPIO_5	GPIO5	Reserved	Selected programmed value is available in GPIO5
7:0	ENABLE_GPIO_4	GPIO4	CLK_OBS5	Selected programmed value is available in GPIO4

8.5.13 GPIO Function 2 (GPIO_OUT_FUNCTION2)

Address: 0x18040034
Access: Read/Write
Reset: 0x0

MUX values for GPIO[11:8].

Bit	Bit Name	GPIO	Default Function	Description
31:24	ENABLE_GPIO_11	GPIO11	Reserved	Selected programmed value is available in GPIO11
23:16	ENABLE_GPIO_10	GPIO10	Reserved	Selected programmed value is available in GPIO10
15:8	ENABLE_GPIO_9	GPIO9	Reserved	Selected programmed value is available in GPIO9
7:0	ENABLE_GPIO_8	GPIO8	Reserved	Selected programmed value is available in GPIO8

8.5.14 GPIO Function 3 (GPIO_OUT_FUNCTION3)

Address: 0x18040038
Access: Read/Write
Reset: 0x0

MUX values for GPIO[15:12].

Bit	Bit Name	GPIO	Default Function	Description
31:24	ENABLE_GPIO_15	GPIO15	Reserved	Selected programmed value is available in GPIO15
23:16	ENABLE_GPIO_14	GPIO14	Reserved	Selected programmed value is available in GPIO14
15:8	ENABLE_GPIO_13	GPIO13	Reserved	Selected programmed value is available in GPIO13
7:0	ENABLE_GPIO_12	GPIO12	Reserved	Selected programmed value is available in GPIO12

8.5.15 GPIO Function 4 (GPIO_OUT_FUNCTION4)

Address: 0x1804003C
Access: Read/Write
Reset: 0x0

MUX values for GPIO[19:16].

Bit	Bit Name	GPIO	Default Function	Description
31:24	ENABLE_GPIO_19	GPIO19	Reserved	Selected programmed value is available in GPIO19
23:16	ENABLE_GPIO_18	GPIO18	Reserved	Selected programmed value is available in GPIO18
15:8	ENABLE_GPIO_17	GPIO17	Reserved	Selected programmed value is available in GPIO17
7:0	ENABLE_GPIO_16	GPIO16	Reserved	Selected programmed value is available in GPIO16

8.5.16 GPIO Function 5 (GPIO_OUT_FUNCTION5)

Address: 0x18040040
Access: Read/Write
Reset: 0x0

MUX values for GPIO[22:20].

Bit	Bit Name	GPIO	Default Function	Description
31:24	RES	RES	Reserved	Reserved
23:16	ENABLE_GPIO_22	GPIO22	Reserved	Selected programmed value is available in GPIO22
15:8	ENABLE_GPIO_21	GPIO21	Reserved	Selected programmed value is available in GPIO21
7:0	ENABLE_GPIO_20	GPIO20	Reserved	Selected programmed value is available in GPIO20

8.5.17 GPIO In Signals 0 (GPIO_IN_ENABLE0)

Address: 0x18040044
Access: Read/Write
Reset: See field description

Program the GPIO pin number through which these signals are input. Legal values for this register are 0–22 for GPIO0 to GPIO22.

Bit	Bit Name	Reset	Description
31:16	RES	0x0	Reserved
15:8	UART0_SIN	0x9	Programmed value indicates the GPIO that inputs UART0_SIN
7:0	RES	0x0	Reserved

8.5.18 GPIO In Signals 3 (GPIO_IN_ENABLE3)

Address: 0x18040050
Access: Read/Write
Reset: See field description

Program the GPIO pin number through which these signals are input. Legal values for this register are 0–22 for GPIO0 to GPIO22.

Bit	Bit Name	Reset	Description
31:24	RES	0x0	Reserved
23:16	MII_GE0_MDI	0x9	Programmed value indicates the GPIO through whichever MDIO signal of GE0 MDIO is available
15:0	RES	0x0	Reserved

8.5.19 GPIO Function (GPIO_FUNCTION)

Address: 0x1804006C
Access: Read/Write
Reset: See field description

This register indicates through which GPIO pins the particular input signal is available. Program the GPIO pin number through which these signals are input. If this bit is set enables or disables that specific function.

Bit	Bit Name	Reset	Description
31:9	RES	0x0	Reserved
11	CLK_OBS9_ENABLE	0x0	Enables observation of the USB clock for the second USB instance
10:9	RES	0x0	Reserved
8	CLK_OBS6_ENABLE	0x0	Enables observation of USB_CLK for the first instance
7	CLK_OBS5_ENABLE	0x0	Enables observation of CPU_CLK/4
6	CLK_OBS4_ENABLE	0x1	Enables observation of AHB_CLK/2
5	RES	0x0	Reserved
4	CLK_OBS2_ENABLE	0x0	Enables observation of 125 MHz CLK
3	CLK_OBS1_ENABLE	0x0	Enables observation of PCIE RC CLK
2	CLK_OBS0_ENABLE	0x0	Enables observation of the SGMII clock
1	DISABLE_JTAG	0x0	Disables JTAG port functionality to enable GPIO functionality
0	RES	0x0	Reserved

8.5.20 GPIO Ethernet LED Routing Select (GPIO_IN_ETH_SWITCH_LED)

Address: 0x18040070
Access: Read-Only
Reset: 0x0

Selects routing of the signal indication groups to the LED signals: activity, collision, link, or duplex.

Bit	Bit Name	Description
31:20	RES	Reserved
19:15	LINK	The current value of LED_LINK100*n*_O and LED_LINK10*n*_O
14:10	DUPL	The current value of LED_DUPLEX*n*_O
9:5	COLL	The current value of LED_COLN*n*_O
4:0	ACTV	The current value of LED_ACT*n*_O

8.6 PLL Control Registers

Table 8-7 summarizes the QCA9563 PLL control registers.

Table 8-7 PLL Control Registers Summary

Address	Name	Description	Page
0x18050000	CPU_PLL_CONFIG	CPU PLL Configuration	page 139
0x18050004	CPU_PLL_CONFIG1	CPU PLL Configuration 1	page 140
0x18050008	DDR_PLL_CONFIG	DDR PLL Configuration	page 140
0x1805000C	DDR_PLL_CONFIG1	DDR PLL Configuration 1	page 141
0x18050010	CPU_DDR_CLOCK_CONTROL	CPU DDR Clock Control	page 141
0x18050014	PCIE_PLL_CONFIG	PCIE PLL Configuration Register	page 142
0x18050018	PCIE_PLL_DITHER_DIV_MAX	PCIE Clock Jitter Control Maximum Register	page 143
0x1805001C	PCIE_PLL_DITHER_DIV_MIN	PCIE Clock Jitter Control Minimum Register	page 143
0x18050020	PCIE_PLL_DITHER_STEP	PCIE Clock Jitter Control Step Register	page 144
0x18050024	LDO_POWER_CONTROL	LDO Power Control Register	page 144
0x18050028	SWITCH_CLOCK_CONTROL	Switch Clock Source Control	page 145
0x1805002C	CURRENT_PCIE_PLL_DITHER	Current Dither Logic Output	page 146
0x18050030	ETH_XMII	Ethernet XMII Configuration Register	page 146
0x18050034	BB_PLL CONFIG	Baseband PLL Configuration Register	page 146
0x18050038	DDR_PLL_DITHER	DDR PLL Dither Parameter	page 147
0x1805003C	DDR_PLL_DITHER2	DDR PLL Dither Parameter 2	page 147
0x18050040	CPU_DLL_DITHER	CPU PLL Dither Parameter Register	page 148
0x18050044	CPU_DLL_DITHER2	CPU PLL Dither Parameter Register 2	page 148
0x18050048	ETH_SGMII	Ethernet SGMII	page 148
0x1805004C	ETH_SGMII_SERDES	Ethernet SGMII SERDES	page 149

8.6.1 CPU Phase Lock Loop Configuration (CPU_PLL_CONFIG)

Address: 0x18050000
Access: Read/Write
Reset: See field description

This register configures the CPU PLL.

$$Fvco = \frac{fREF}{REFDIV} \times \left(NINT + \frac{(NFRAC\{Bit(17 \cdot 5)\})}{2^{13}} + \frac{NFRAC\{Bit(4 \cdot 0)\}}{(25*2^{13})} \right)$$

Bit	Bit Name	Type	Reset	Description
31	UPDATING	RO	0x1	Poll for this bit to become 0 to ensure PLL had settled
30	PLLPWD	RW	0x1	Write 0 to this bit to power up the PLL
29:22	SPARE	RW	0x0	The spare bits in the CPU_PLL_CONFIG register is accessible only when the PLL is in BYPASS mode
21:19	OUTDIV	RW	0x0	Define the ratio between VCO output and PLL output. OUTDIV > 4 is unsupported.

18:17	RES	R	0x0	Reserved
16:12	REFDIV	RW	0x2	Reference clock divider
11:0	RES	R	0x0	Reserved

8.6.2 CPU Phase Lock Loop Configuration 1 (CPU_PLL_CONFIG1

Address: 0x18050004
Access: Read / Write
Reset: See field description

This register is used to configure the CPU PLL.

$$Fvco = \frac{fREF}{REFDIV} \times \left(NINT + \frac{(NFRAC\{Bit(17 \cdot 5)\})}{2^{13}} + \frac{NFRAC\{Bit(4 \cdot 0)\}}{(25*2^{13})} \right)$$

Bit	Bit Name	Type	Reset	Description
31:27	RES	R	0x0	Reserved
26:18	NINT	RW	0x14	The integer part of the CPU PLL
17:0	NFRAC	R	0x10000	Reflects the current NFrac. Use CPU PLL Dither Parameter (CPU_PLL_DITHER), page 8-148 and CPU PLL Dither 2 (CPU_PLL_DITHER2), page 8-148 to set.

8.6.3 DDR PLL Configuration (DDR_PLL_CONFIG)

Address: 0x18050008
Access: Read / Write
Reset: See field description

This register is used to configure the DDR PLL.

$$Fvco = \frac{fREF}{REFDIV} \times \left(NINT + \frac{(NFRAC\{Bit(17 \cdot 5)\})}{2^{13}} + \frac{NFRAC\{Bit(4 \cdot 0)\}}{(25*2^{13})} \right)$$

Bit	Bit Name	Type	Reset	Description
31	UPDATING	RO	0x1	This bit is set during the PLL update process. After the software configures CPU PLL, it takes about 32 µsec for the update to be finished. Software may poll this bit to see if the update has completed.
30	PLLPWD	RW	0x1	Power up control for the PLL, write zero to this bit to power up the PLL.
29:26	RES	RW	0x0	Reserved
25:23	OUTDIV	RW	0x0	Define the ratio between VCO output and PLL output. OUTDIV > 4 is unsupported.
22:21	RES	R	0x0	Reserved
20:16	REFDIV	RW	0x2	Reference clock divider
15:0	RES	R	0x0	Reserved

8.6.4 DDR PLL Configuration 1 (DDR_PLL_CONFIG1)

Address: 0x1805000C
Access: Read / Write
Reset: See field description

This register is used to configure the DDR PLL.

Bit	Bit Name	Type	Reset	Description
31:27	RES	R	0x0	Reserved
26:18	NINT	RW	0x14	The integer part of the DDR PLL
17:0	NFRAC	R	0x20000	Reflects the current NFrac. Use DDR PLL Dither Parameter (DDR_PLL_DITHER), page 8-147 and DDR PLL Dither 2 (DDR_PLL_DITHER2), page 8-147 to set.

8.6.5 CPU DDR Clock Control (CPU_DDR_CLOCK_CONTROL)

Address: 0x18050010
Access: Read / Write
Reset: See field description

This register is used to set the CPU and DDR clocks. Any field in this register can be dynamically modified.

Bit	Bit Name	Type	Reset	Description
31:25	RES	RW	0x0	Reserved
24	AHBCLK_FROM_DDRPLL	RW	0x1	AHB_CLK setting 0 AHB_CLK is derived from the CPU_PLL 1 AHB_CLK is derived from the DDR_PLL
23	CPU_RESET_EN_BP_DEASRT	RW	0x0	Enables reset to the CPU when the CPU_PLL bypass bit is reset
22	CPU_RESET_EN_BP_ASRT	RW	0x0	Enables reset to the CPU when the CPU_PLL bypass bit is set
21	CPU_DDR_CLK_FROM_CPUPLL	RW	0x0	These two bits work in conjuction with each other based on these factors: ■ When both bits are set to 0, CPU_CLK is derived from CPU_PLL and DDR_CLK is derived from DDR_PLL ■ When Bit 21 is set to 1 and bit 20 is set to 0, both the CPU_CLK and DDR_CLK are derived from CPU_PLL ■ When Bit 21 is set to 0 and bit 20 is set to 1, both the CPU_CLK and the DDR_CLK are derived from the DDR_PLL ■ Both bits can not be set to 1 at the same time
20	CPU_DDR_CLK_FROM_DDRPLL	RW	0x0	
19:15	AHB_POST_DIV	RW	0x0	Division of the AHB clock: <AHB frequency> = <PLL or REFCLK frequency> / (AHB_POST_DIV+1)
14:10	DDR_POST_DIV	RW	0x0	Division of the DDR PLL clock: <DDR frequency> = <PLL frequency> / (DDR_POST_DIV+1) or <REFCLK frequency>

9:5	CPU_POST_DIV	RW	0x0	Division of the CPU PLL clock: <CPU frequency> = <PLL frequency> / (CPU_POST_DIV+1) or <REFCLK frequency>
4	AHB_PLL_ BYPASS	RW	0x1	Enables bypassing of the AHB PLL path
3	DDR_PLL_ BYPASS	RW	0x1	Enables bypassing of the DDR PLL
2	CPU_PLL_ BYPASS	RW	0x1	Enables bypassing of the CPU PLL
1	RESET_SWITCH	RW	0x0	Reset during clock switch trigger
0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

8.6.6 PCIE PLL Configuration Register (PCIE_PLL_CONFIG)

Address: 0x18050014
Access: Read/Write
Reset: See field description

This register is the PCIE RC Phase Lock Loop configuration register:

$$PLL\_FREQ = \frac{\frac{REFCLK\_FREQ}{REFDIV} \times \left(NINT + \frac{(NFRAC[Bit13.1])}{2^{13}} + \frac{NFRAC[Bit0]}{25 \times 2^{8}} \right)}{6}$$

Use PCIE_PLL_DITHER_DIV_MAX/MIN to set DIV_INT and DIV_FRAC.

Bit	Bit Name	Reset	Description
31	UPDATING	0x0	Poll for this bit to become zero to ensure PLL has settled.
30	PLLPWD	0x1	Write zero to this bit to power up the PLL.
29:17	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
16	BYPASS	0x1	Enables bypassing of the PCIE PLL
15	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
14:10	REFDIV	0x1	Reference clock divider
9:0	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

8.6.7 PCIE Clock Jitter Control Maximum Register (PCIE_PLL_ DITHER_DIV_MAX)

Address: 0x18050018
Access: Read/Write
Reset: See field description

This register is the PCIE Clock Jitter Control Maximum Value Register which controls the Jitter behavior of the PCIE PLL.

Bit	Bit Name	Reset	Description
31	EN_DITHER	0x1	Enable dither logic
30	USE_MAX	0x1	Uses DIV_MAX values when dither logic is disabled
29:21	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
20:15	DIV_MAX_INT	0x13	Maximum limit integer part of the divider
14:1	DIV_MAX_FRAC	0x3FFF	Maximum limit fractional part of the divider

8.6.8 PCIE Clock Jitter Control Minimum Register (PCIE_PLL_ DITHER_DIV_MIN)

Address: 0x1805001C
Access: Read/Write
Reset: See field description

This register is the PCIE Clock Jitter Control Minimum Value Register which controls the Jitter behavior of the PCIE PLL.

Bit	Bit Name	Reset	Description
31:21	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
20:15	DIV_MIN_INT	0x13	Minimum limit integer part of the divider
14:1	DIV_MIN_FRAC	0x399D	Minimum limit fractional part of the divider
0	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

8.6.9 PCIE Clock Jitter Control Step Register (PCIE_PLL_DITHER_STEP)

Address: 0x18050020
Access: Read/Write
Reset: See field description

This register is the PCIE Clock Jitter Control Step Register which controls the Jitter behavior of the PCIE PLL.

Bit	Bit Name	Reset	Description
31:28	UPDATE_CNT	0x0	Count update frequency. and entry of 0 updates every clock
27:25	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
24:15	STEP_INT	0x0	Integer Part of the Step value of the divider
14:1	STEP_FRAC	0xA	Fractional Part of the Step value of the divider
0	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

8.6.10 LDO Power Control Register (LDO_POWER_CONTROL)

Address: 0x18050024
Access: Read/Write
Reset: See the field description

This register reflects/controls the Analog LDO control bits Controls the LDO.

Bit	Bit Name	Reset	Description
31:5	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
4	PWDLDO_CPU	0x0	1.2 V signal to power down DDR regulator
3	PWDLDO_DDR	0x0	1.2 V signal to power down DDR regulator
2:1	CPU_REFSEL	0x3	Selects CPU regulator output voltage
0	SELECT_DDR	0x0	Reflects the input in PC_DDR_SEL pin

8.6.11 Switch Clock Source Control (SWITCH_CLOCK_CONTROL)

Address: 0x18050028
Access: Read / Write
Reset: See field description

This register controls the clock sources to the various blocks.

Bit	Bit Name	Type	Reset	Description
31:20	RES	RW	0x0	Reserved
19	SWITCH_CLK_SEL	RW	0x1	Ethernet switch PLL reference clock section
				0 40 MHz reference clock
				1 25 MHz reference clock
18	OEN_CLK125M_SEL	RW	0x1	Enable for the PLL CLK 125M from the Ethernet PHY. Active low.
17	RES	RW	0x0	Reserved
16	SWITCH_FUNC_TST_MODE	RW	0x0	Enables Ethernet switch functional test mode
15:14	RES	RW	0x0	Reserved
13	MDIO_CLK_SEL0_2	RW	0x0	MDIO master operational clock selection for GMAC0. Used with MDIO_CLK_SEL0_1
				0 Reference clock, or 100 MHz clock
				1 50 MHz clock
12	EN_PLL_TOP	RW	0x1	Enables the Ethernet PHY PLL
11:8	USB_REFCLK_FREQ_SEL	RW	0x5	Used to select the REFCLK input of 25-MHz to the USB PLL
7	UART_CLK_SEL	RW	0x0	UART clock
				0 From the reference clock
				1 From the 100 MHz clock
6	MDIO_CLK_SEL0_1	RW	0x0	MDIO master operational clock selection for GMAC0. Used with MDIO_CLK_SEL0_2
				0 From the reference clock
				1 From the 100 MHz clock
5:0	RES	RW	0x0	Reserved

8.6.12 PCIE PLL Dither (CURRENT_PCIE_PLL_DITHER)

Address: 0x1805002C
Access: Read/ Write
Reset: See field description

This register sets the integer and fractional parts of the dither logic.

Bit	Bit Name	Type	Reset	Description
31:21	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
20:15	INT	RW	0x0	The integer part of the divider
14	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
13:0	FRAC	RW	0x3FFF	The fractional part of the divider

8.6.13 Ethernet XMII (ETH_XMII)

Address: 0x18050030
Access: Read/ Write
Reset: See field description

This controls the Tx and Rx clock for GMAC. It should only be changed when GE0 is in reset.

Bit	Bit Name	Type	Reset	Description
31	TX_INVERT	RW	0x0	To invert or not invert the GTx clock after the delay line
30	GIGE_QUAD	RW	0x0	Add 2ns delay for GTx clock. Only effective when bit 25 is set
29:28	RX_DELAY	RW	0x0	Delay line setting for Rx clock
27:26	TX_DELAY	RW	0x0	Delay line setting for GTx clock
25	GIGE	RW	0x0	Set only when there is a 1000 Mbps connection
24	OFFSET_PHASE	RW	0x0	Offset delay start from the positive or negative edge
23:8	OFFSET_COUNT	RW	0x0	Count value of GTx phase delay
15:8	PHASE1_COUNT	RW	0x1	Number of clk100 cycles in the negative cycle of XMII Tx/Rx clock
7:0	PHASE0_COUNT	RW	0x1	Number of clk100 cycles in the positive cycle of XMII Tx/Rx clock

8.6.14 Baseband PLL Configuration Register (BB_PLL_CONFIG)

Address: 0x18050034
Access: Read/Write
Reset: See field description

This register is the Baseband Phase Loop Lock configuration register.

Bit	Bit Name	Reset	Description
31	UPDATING	0x1	Poll for this bit to become 0 to ensure PLL has settled
30	PLLPWD	0x1	Write 0 to this bit to power up the PLL
29	SPARE	0x0	Spare bits
28:24	REFDIV	0x1	Reference clock divider
23:22	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
21:16	NINT	0x02	The integer part of the DIV to DDR PLL
15:14	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
13:0	NFRAC	14hccc	Reflects the current fraction of the PLL divider

8.6.15 DDR PLL Dither Parameter (DDR_PLL_DITHER)

Address: 0x18050038
Access: Read/Write
Reset: See field description

Controls the FRAC of the DDR_PLL. Should be enabled only if the DDR_CLK is from the DDR_ PLL.

Bit	Bit Name	Type	Reset	Description
31	DITHER_ EN	RW	0x0	The step value which increments every refresh period
30:27	UPDATE_ COUNT	RW	0xF	The number of refresh periods between two updates
26:20	NFRAC_ STEP	RW	0x1	7-bit LSB step value which increments every refresh period
19:18	RES	R	0x0	Reserved
17:0	NFRAC_ MIN	RW	0x0	The minimum NFRAC fractional value

8.6.16 DDR PLL Dither 2 (DDR_PLL_DITHER2)

Address: 0x1805003C
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description
31:18	RES	R	0x0	Reserved
17:0	NFRAC_MAX	RW	0x3E800	The maximum NFRAC fractional value

8.6.17 CPU PLL Dither Parameter (CPU_PLL_DITHER)

Address: 0x18050040
Access: Read/Write
Reset: 0x0

Sets the parameters for the CPU PLL dither.

Bit	Bit Name	Description
31	DITHER_ EN	The step value which increments every refresh period
30:27	UPDATE_ COUNT	The number of 512 CPU clocks between two updates in NFRAC
26:18	NFRAC_ STEP	The step value increment
17:0	NFRAC_ MIN	Minimum NFRAC value. If DITHER_EN is set to 0, the min would be used. Default value is 0x3000.

8.6.18 CPU PLL Dither 2 (CPU_PLL_DITHER2)

Address: 0x18050044
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description
31:18	RES	R	0x0	Reserved
17:0	NFRAC_MAX	RW	0x3C00	The maximum NFRAC fractional value

8.6.19 Ethernet SGMII (ETH_SGMII)

Address: 0x18050048
Access: Read/Write
Reset: See field description

Controls the Tx and Rx clocks for the GMAC and SGMII SERDES digital.

Bit	Bit Name	Type	Reset	Description	
31	TX_INVERT	RW	0x0	Chooses whether to invert the GTX clock after the delay line	
30	GIGE_QUAD	RW	0x0	Chooses whether to give a 2 ns shift (clock in the middle of data) to the GTX clock, effective only when Bit 25 is set	
29:28	RX_DELAY	RW	0x0	Delay buffers in Rx clock path to adjust against edge/middle -aligned RGMII inputs	
27:26	TX_DELAY	RW	0x0	Delay line setting for the GTX clock that goes out along with the data	
				00	Minimum
				01	Maximum
25	CLK_SEL	RW	0x1	Set to select between CLK100 / CLK125 for SGMII Source clock.	
				0	CLK100
				1	CLK125
24	GIGE	RW	0x1	Set this Bit if the GMAC connected to SGMII is in GIGE Mode	
23:16	RES	R	0x0	Reserved	

15:8	PHASE1_ COUNT	RW	0x1	Number of (clk100/clk125 + 1) cycles in the negative cycle of the SGMII Tx/Rx clock
7:0	PHASE0_ COUNT	RW	0x1	Number of (clk100/clk125 + 1) cycles in the positive cycle of the SGMII Tx/Rx clock

8.6.20 Ethernet SGMII SERDES (ETH_SGMII_SERDES)

Address: 0x1805004C
Access: Read/Write
Reset: See field description

Bit	Bit Name	Type	Reset	Description
31:3	RES	R	0x0	Reserved
2	EN_LOCK_ DETECT	RW	0x0	SGMII VCO control voltage detector
				0 Lock detector disabled
				1 Lock detector enabled
1	PLL_REFCLK_ SEL	RW	0x0	Select PLL reference clock
				0 PLL reference CLK is 25 MHz
				1 PLL reference CLK is 40 MHz
0	PLL_EN	RW	0x1	Enable SGMII PLL
				0 SGMII PLL disabled
				1 SGMII PLL enabled

8.7 Reset Registers

Table 8-8 summarizes the reset registers for the QCA9563.

Table 8-8 Reset Registers Summary

Address	Name	Description	Page
0x18060000	RST_GENERAL_TIMER	General Purpose Timer	page 151
0x18060004	RST_GENERAL_TIMER_RELOADx	General Purpose Timer Reload	page 151
0x18060008	RST_WATCHDOG_TIMER_CONTROL	Watchdog Timer Control	page 152
0x1806000C	RST_WATCHDOG_TIMER	Watchdog Timer	page 152
0x18060010	RST_MISC_INTERUPT_STATUS	Misc Interrupt Status	page 153
0x18060014	RST_MISC_INTERUPT_MASK	Misc Interrupt Mask	page 154
0x18060018	RST_GLOBAL_INTERUPT_STATUS	Global Interrupt Status	page 155
0x1806001C	RST_RESET	Reset	page 155
0x18060090	RST_REVISION_ID	Chip Revision ID	page 156
0x18060094	RST_GENERAL_TIMER2	General Purpose Timer 2	page 151
0x18060098	RST_GENERAL_TIMER2_RELOAD	General Purpose Timer2 Reload	page 151
0x1806009C	RST_GENERAL_TIMER3	General Purpose Timer 3	page 151
0x180600A0	RST_GENERAL_TIMER3_RELOAD	General Purpose Timer3 Reload	page 151
0x180600A4	RST_GENERAL_TIMER4	General Purpose Timer 4	page 151
0x180600A8	RST_GENERAL_TIMER4_RELOAD	General Purpose Timer4 Reload	page 151
0x180600AC	PCIE_WMAC_INTERRUPT_STATUS	PCIE WMAC Interrupt Status	page 156
0x180600B0	RST_BOOTSTRAP	Reset Bootstrap	page 157
0x180600B8	SPARE_STKY_REG[0:0]	Sticky Register Value	page 158
0x180600BC	RST_MISC2	Miscellaneous CPU Control Bits	page 158
0x180600C0	RST_RESET2	Reset Register 2	page 158
0x180600C8	RST_CLKGAT_EN	AHB Clock Gating Reset Register	page 158

8.7.1 General Purpose Timers (RST_GENERAL_TIMERx)

Timer1 Address: 0x18060000
Timer2 Address: 0x18060094
Timer3 Address: 0x1806009C
Timer4 Address: 0x180600A4
Access: Read/Write
Reset: 0x0

This timer counts down to zero, sets, interrupts, and then reloads from the register General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx), page 8-151. The timer operates with REF_CLK as reference input.

This definition holds true for timer1, timer2, timer3, and timer4.

Bit	Bit Name	Description
31:0	TIMER	Timer value

8.7.2 General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx)

Timer1 Reload Address: 0x18060004
Timer2 Reload Address: 0x18060098
Timer3 Reload Address: 0x180600A0
Timer4 Reload Address: 0x180600A8
Access: Read/Write
Reset: 0x0

This register contains the value that will be loaded into the register General Purpose Timers (RST_GENERAL_TIMERx), page 8-151 when it decrements to zero.

The timer operates with REF_CLK as reference input.

This definition holds true for timer1, timer2, timer3, and timer4.

Bit	Bit Name	Description
31:0	RELOAD_VALUE	Timer reload value

8.7.3 Watchdog Timer Control (RST_WATCHDOG_TIMER_CONTROL)

Address: 0x18060008
Access: See field description
Reset: 0x0

Sets the action to take when the watchdog timer reaches zero. The options are reset, non-maskable interrupt and general purpose interrupt after reaching zero.

The timer operates with REF_CLK as reference input.

Bit	Bit Name	Type	Description	
31	LAST	RO	Indicates if the last reset was due to a watchdog timeout	
30:2	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
1:0	ACTION	RW	The action to be taken after the timer reaches zero	
			00	No action
			01	General purpose interrupt
			10	Non-maskable interrupt
			11	Full chip reset, same as power-on reset

8.7.4 Watchdog Timer (RST_WATCHDOG_TIMER)

Address: 0x1806000C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	TIMER	Counts down to zero and stays at zero until the software sets this timer to another value. The timer operates with REF_CLK as reference input. These bits should be set to a non-zero value before updating the RST_WATCHDOG_ TIMER_CONTROL register to a non-zero number.

8.7.5 Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_ STATUS)

Address: 0x18060010
Access: Read/Write-to-Clear
Reset: 0x0

Sets the current state of the interrupt lines that are combined to form the MiscInterupt to the processor. All bits of this register need a write to clear.

Bit	Bit Name	Description	
31:28	RES	Reserved. Must be written with zero. Contains zeros when read.	
27	ETH_MAC_INT	Interrupt generated by Ethenet switch	
26	USB2_PLL_LOCK	USB2 PLL lock detection off interrupt	
25	USB1_PLL_LOCK	USB1 PLL lock detection off interrupt	
		0	Disabled
		1	Enabled
24:21	RES	Reserved	
20	WOW_INTR	Interrupt generated when the MAC detects a WOW event. Cleared on write of this register	
19	RES	Reserved	
18	DDR_ACTIVITY_ IN_SF	This interrupt is generated when the memory controller detects a DDR request when in self-refresh.	
17	DDR_SF_EXIT	This interrupt is generated by the memory controller upon entering self-refresh	
16	DDR_SF_ENTRY	This interrupt is generated by the memory controller upon entering self-refresh	
15:13	RES	Reserved	
12	SGMII_MAC_INT	Interupt generated form SGMII. Cleared on write of this register	
11	RES	Reserved	
10	TIMER4_INT	The interrupt corresponding to General Purpose Timer4. This bit is cleared after being read. The timer has been immediately reloaded from the General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx), page 8-151 register.	
9	TIMER3_INT	The interrupt corresponding to General Purpose Timer3. This bit has been cleared after being read. The timer will be immediately reloaded from the General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx), page 8-151 register.	
8	TIMER2_INT	The interrupt corresponding to General Purpose Timer2. This bit has been cleared after being read. The timer will be immediately reloaded from the General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx), page 8-151 register.	
7:6	RES	Reserved	
5	PC_INT	CPU performance counter interrupt. Generated whenever either of the internal CPU performance counters have bit [31] set. The relevant performance counter must be reset to clear this interrupt.	
4	WATCHDOG_ INT	The watchdog timer interrupt. This interrupt is generated when the watchdog timer reaches zero and the watchdog configuration register is configured to generate a general-purpose interrupt.	
3	UART_INT	The UART interrupt. UART0 interrupt registers must be read before this interrupt can be cleared.	
2	GPIO_INT	The GPIO interrupt. Individual lines must be masked before this interrupt can be cleared.	
1	ERROR_INT	The error interrupt.	
0	TIMER_INT	Interrupt occurring in correspondence to the general purpose timer0. This bit is cleared after being read. The timer has already been reloaded from the General Purpose Timers Reload (RST_GENERAL_TIMER_RELOADx), page 8-151 register.	

8.7.6 Miscellaneous Interrupt Mask (RST_MISC_INTERRUPT_MASK)

Address: 0x18060014
Access: Read/Write
Reset: 0x0

Enables or disables a propagation of interrupts in the Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS) register.

Bit	Bit Name	Description	
31:29	RES	Reserved. Must be written with zero. Contains zeros when read.	
28	MIPS_SI_TIMERINT_MASK	Enables MIPS Count/Compare Timer Interrupt. The register bit default mask CPU.SI_Int[5]. Software need to enable it before using CPU timer.	
27	ETH_MAC_INT_MASK	Enables the interrupt generated by Ethenet switch	
26	USB2_PLL_LOCK_MASK	USB2 PLL Lock detection off interrupt mask.	
		0	Interrupt disabled
		1	Interrupt enabled
25	USB_PLL_LOCK_MASK	USB1 PLL lock detection off an interrupt	
24	RES	Reserved	
23	USB_PLL_LOCK_MSK	Enables the USB PLL lock detection off an interrupt	
22:21	RES	Reserved	
20	WOW_INTR_MASK	Enables the USB PLL lock detection off an interrupt	
19	RES	Reserved	
18	DDR_ACTIVITY_IN_SF_MASK	Enables the interrupt generated when the memory controller detects a DDR request when in self-refresh	
17	DDR_SF_EXIT_MASK	Enables the interrupt generated when the memory controller enters self-refresh	
16	DDR_SF_ENTRY_MASK	Enables the interrupt generated when the memory controller enters self-refresh	
15:13	RES	Reserved	
12	SGMII_MAC_INT_MASK	Enables SGMII interrupt if this bit is set to 1	
11	RES	Reserved	
10	TIMER4_MASK	When set, enables Timer3 interrupt	
9	TIMER3_MASK	When set, enables Timer2 interrupt	
8	TIMER2_MASK	When set, enables Timer1 interrupt	
7:6	RES	Reserved	
5	PC_MASK	When set, enables CPU performance counter interrupt	
4	WATCHDOG_ MASK	When set, enables watchdog interrupt	
3	UART_MASK	When set, enables the UART interrupt	
2	GPIO_MASK	When set, enables GPIO interrupt	
1	ERROR_MASK	When set, enables the error interrupt	
0	TIMER_MASK	When set, enables timer interrupt	

8.7.7 Global Interrupt Status (RST_GLOBAL_INTERRUPT_STATUS)

Address: 0x18060018
Access: Read-Only
Reset: 0x0

This register indicates the cause of an interrupt to the CPU from various sources.

Bit	Bit Name	Description
31:10	RES	Reserved. Must be written with zero. Contains zeros when read.
9	WMAC_INT	WLAN MAC interrupt
8	RES	Reserved. Must be written with zero. Contains zeros when read.
7	USB2_INT	USB2 interrupt. Information available in the USB register space
6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	TIMER_INT	Internal MIPS Count/Compare Timer Interrupt
4	MISC_INT	Miscellaneous interrupt; source of the interrupt available on the Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS), page 8-153 register
3	RES	Reserved. Must be written with zero. Contains zeros when read.
2	GE0_INT	Ethernet0 interrupt; information available in the Ethernet0 register space
1	USB1_INT	USB1 interrupt. Information available in the USB register space.
0	PCIE_WMAC_INT	PCIE RC/WMAC interrupt

8.7.8 Reset (RST_RESET)

Address: 0x1806001C
Access: Read/Write
Reset: See field description

This register individually controls the reset to each of the chip's submodules.

Bit	Bit Name	Reset	Type	Description
31:29	RES	0x0	RO	Reserved
28	EXTERNAL_RESET	0x0	RW	Commands an external reset (SYS_RST_L pin) immediately; inverted before being sent to the pin.
27	RTC_RESET	0x1	RW	The RTC reset
26:25	RES	0x0	RO	Reserved. Must be written with 0. Contains zeroes when read.
24	FULL_CHIP_RESET	0x0	RW	Used to command a full chip reset. This is the software equivalent of pulling the reset pin. The system will reboot with PLL disabled. Always zero when read.
23	RES	0x1	RW	Reseved. Should be set to 1.
22	RESET_GE0_MDIO	0x1	RW	Resets the Ethernet 0 MDIO
21	CPU_NMI	0x0	RW	Used to send an NMI to the CPU. Always zero when read. The watchdog timer can also be used to generate NMI/full chip reset.
20	CPU_COLD_RESET	0x0	RW	Used to cold reset the entire CPU. This bit will be cleared automatically immediately after the reset. Always zero when read.
19:17	RES	0x0	RO	Reserved. Must be written with 0. Contains zeroes when read.
16	DDR_RESET	0x0	RW	Resets the DDR controller. Self-cleared to 0 by hardware
15	USB_PHY_PLL_PWD_EXT	0x0	RW	Used to power down the USB PHY PLL
14	RES	0x0	RO	Reserved. Must be written with 0. Contains zeroes when read.

13	RES	0x1	RW	Reserved. Should be set to 1.
12	ETH_SGMII_ARESET	0x1	RW	Reset the SGMII SERDES analog
11	USB_PHY_ARESET	0x1	RW	Resets the USB PHY's analog
10	RES	0x0	RO	Reserved. Must be written with 0. Contains zeroes when read.
9	GE0_MAC_RESET	0x1	RW	Used to reset the GE0 MAC
8	ETH_SGMII_RESET	0x1	RW	SGMII SERDES reset
7	PCIE_PHY_RESET	0x1	RW	Resets the PCIE PHY
6	PCIE_RESET	0x1	RW	Resets the PCIE host controller
5	USB_HOST_RESET	0x1	RW	Used to reset the USB Host Controller
4	USB_PHY_RESET	0x1	RW	Used to reset the USB PHYs
3	USB_PHY_SUSPEND_ OVERRIDE	0x0	RW	Used to set the USB suspend state
				0 Used to put the USB PHY in suspend state
				1 Delegates the Core to control the USB PHY suspend state
2	RES	0x1	RW	Reserved. Should be set to 1
1	RES	0x0	RO	Reserved. Must be written with 0. Contains zeroes when read.
0	RES	0x1	RW	Reserved. Should be set to 1.

8.7.9 Chip Revision ID (RST_REVISION_ID)

Address: 0x18060090
Access: Read-Only
Reset: See field description

This register is the revision ID for the chip.

Bit	Bit Name	Reset	Description
31:0	VALUE	0x1150	Revision ID value

8.7.10 PCIE WMAC Interrupt Status (RST_PCIE _WMAC_ INTERRUPT_STATUS)

Address: 0x180600AC
Access: Read-Only
Reset: 0x0

This register is used to read the interrupt statuses for PCIE RC and WMAC interrupts.

Bit	Bit Name	Description
31:29	RES	Reserved. Must be written with zero. Contains zeros when read.
28	USB2_INT	USB2 interrupt. Information available in the USB register space.
27:25	RES	Reserved
24	USB1_INT	USB1 interrupt
23:22	RES	Reserved
21	PCIE_HOST_IF_ INT	PCIe host interface interrupt

20	PCIE_HOSTDMA_INT	PCIe host DMA interupt
19:17	RES	Reserved
16	PCIE_RC_INT3	PCIe RC multi-MSI interrupt (vector3) / INTA interupt status
15	PCIE_RC_INT2	PCIe RC multi-MSI interrupt (vector2) / INTA interupt status
14	PCIE_RC_INT1	PCIe RC multi-MSI interrupt (vector1) / INTA interupt status
13	PCIE_RC_INT0	PCIe RC multi-MSI interrupt (vector0) / INTA interupt status
12	PCIE_RC_IN	Master PCIe RC interrupt
11:4	RES	Reserved
3	WMAC_RXHP_INT	Interrupt corresponding to the WMAC high priority receive queue
2	WMAC_RXLP_INT	Interrupt corresponding to the WMAC low priority receive queue
1	WMAC_TX_INT	Interrupt corresponding to the WMAC transmission
0	WMAC_MISC_INT	Interrupt corresponding to the WMAC

8.7.11 Reset Bootstrap (RST_BOOTSTRAP)

Address: 0x180600B0
Access: Read-Only
Reset: See field descriptions

This register contains the bootstrap values latched during reset.

Bit	Bit Name	Reset		Description
31:13	RES	0x0	Reserved	
12	SW_OPTION2	0x0	Software option 2	
11	SW_OPTION1	0x0	Software option 1	
10:5	RES	0x0	Reserved	
4	RES	0x1	Reserved	
3	JTAG_MODE	0x1	0	Selects EJTAG mode
			1	Selects JTAG mode
2	REF_CLK	0x0	0	Selects REF_CLK_25MHz
			1	Reserved
1	RES	0x1	Reserved. Should be tied to 1.	
0	DDR_SELECT	0x0	0	Selects DDR2
			1	Selects DDR1 (default)

8.7.12 Sticky Register Value (SPARE_STKY_REG[0:0])

Address: 0x180600B4
Access: Read/Write
Reset: 0x0

This register is a generic register only affected by power-cycling. This register can be used by the CPU to save and restore critical state bits during a suspend/resume event for example.

Bit	Bit Name	Description
31:0	VALUE	Sticky register value. This value is reset only with power on reset (not on any other reset).

8.7.13 Miscellaneous CPU Control Bits (RST_MISC2)

Address: 0x180600B8
Access: Read/Write
Reset: See field description

This register contains miscellaneous CPU controllable bits.

Bit	Bit Name	Reset	Description
31:29	SPARE	0x0	Spare bits
28	PCIE_CLKOBS1_SEL	0x0	Select between different PCIE Common PHY clocks for observation
27:14	RES	0x0	Reserved
13	PERSTN_RCPHY	0x1	Bit for controlling perstn of PCIE RC PHY
12:0	RES	0x0	Reserved

8.7.14 Reset Register 2 (RST_RESET2)

Address: 0x180600C0
Access: Read/Write
Reset: See field description

This register is the reset register 2 and individually controls the reset to the submodules of the chip.

Bit	Bit Name	Type	Reset	Description	
31:19	SPARE	RO	0x0	Spare bits	
18	EP_MODE	RW	0x0	Indicates if the EP is present	
				0	RC
				1	EP
17	USB2_EXT_PWR_SEQ	RW	0x1	External power REQ for second USB PHY	
16	USB1_EXT_PWR_SEQ	RW	0x1	External power REQ for USB PHY	
15	USB1_PHY2_PLL_EXT	RW	0x0	Used to power down the second USB PHY PLL	
14:12	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.	
11	USB_PHY2_ARESET	RW	0x1	Reset the analog of the second USB PHY	

10:8	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.	
7	PCIE_PHY_ RESET	RW	0x1	Reset the PCIE PHY	
6	PCIE_RESET	RW	0x1	Reset the PCIE host controller	
5	USB_HOST2_ RESET	RW	0x1	Reset the second USB host controller	
4	USB_PHY2_RESET	RW	0x1	Reset the second USB PHY	
3	USB_PHY2_ SUSPEND_ OVERRIDE	RW	0x0	0	Second USB PHY is in the uspend state
				1	Second USB PHY suspend is controlled from the core
2:1	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.	
0	USB2_MODE	RW	0x0	USB mode	
				0	Host mode
				1	Device Mode

8.7.15 AHB Clock Gating Reset Register (RST_CLKGAT_EN)

Address: 0x180600C8
Access: Read/Write
Reset: See field description

This register controls individual AHB clock gating for each interface.

Bit	Bit Name	Reset	Description
31:12	SPARE	0x0	Spare bits
11:10	RES	0x0	Reserved
9	WMAC	0x1	Enable AHB CLK to propagate for WMAC
8	USB2	0x1	Ebables AHB to propagate for USB2
7	USB1	0x1	Enable AHB CLK to propagate for USB1
6	RES	0x1	Reserved
5	GE0	0x1	Enable AHB CLK to propagate for GE0
4	RES	0x0	Reserved
3	CLK100_PCIE_RC	0x1	Enables the 100 MHz PCIE REFCLK for second PCIE RC
2	PCIE_RC	0x1	Enables the AHB clock to propagate for second PCIE RC
1:0	RES	0x0	Reserved

8.8 GMAC Interface Registers

Table 8-9 summarizes the GMAC interface registers for the QCA9563.

Table 8-9 GMAC Interface Registers Summary

Address	Name	Description	Page
0x18070000	ETH_CFG	Ethernet Configuration	page 160
0x18070014	SGMII_RESET	SGMII Reset	page 161
0x18070018	SGMII_SERDES	SERDES Control and Status Signals	page 161
0x1807001C	MR_AN_CONTROL	PHY Management Control	page 163
0x18070020	MR_AN_STATUS	PHY Management Status	page 164
0x18070024	AN_ADV_ABILITY	AN Adverse Ability	page 165
0x18070028	AN_LINK_PARTNER_ABILITY	AN Link Partner Ability	page 166
0x1807002C	AN_NP_TX	Auto Negotiation Next Page Transmission	page 167
0x18070030	AN_LP_NP_RX	Auto Negotiation Next Page Receive	page 167
0x18070034	SGMII_CONFIG	SGMII Configuration	page 168
0x18070038	SGMII_MAC_RX_CONFIG	SGMII PHY Link Partner Ability	page 169
0x1807003C	SGMII_PHY_TX_CONFIG	SGMII PHY Tx Configuration	page 170
0x18070040	SGMII_MDIO_TX	SGMII MDIO Transmit	page 171
0x18070044	SGMII_MDIO_RX	SGMII MDIO Receive	page 171
0x18070048	EEE	Energy Efficient Ethernet	page 171
0x18070054	SGMII_RESOLVE	SGMII Resolution	page 172
0x1807005C	SGMII_INTERRUPT	SGMII Interrupt	page 172
0x18070060	SGMII_INTERRUPT_MASK	SGMII Interupt Mask	page 172

8.8.1 Ethernet Configuration (ETH_CFG)

Address: 0x18070000
Access: Read/Write
Reset: 0x0

This register determines how GE0 is interfaced in the QCA9563. If SW_ONLY_MODE is set, then all five FE ports attach to the Ethernet switch (LAN ports).

Bit	Bit Name	Description	
31:22	ETH_SPARE	Spare register bits	
21:20	ETH_TXEN_DELAY	Specific selection of the delay line for Tx En	
19:18	ETH_TXD_ DELAY	Specific selection of the delay line for Tx Data	
17:16	ETH_RXDV_DELAY	Specific selection of the delay line for Rx DV	
15:14	ETH_RXD_DELAY	Specific selection of the delay line for Rx Data	
13:7	RES	Reserved	
6	GE0_SGMII	0	Reserved
		1	GMAC GE0 connects to SGMII
5:0	RES	Reserved	

8.8.2 SGMII Reset (SGMII_RESET)

Address: 0x18070014
Access: Read/Write
Reset: 0x0

This register sends resets to the SGMII MAC or PHY from the GMII interface.

Bit	Bit Name	Type	Description
31:5	RES	RO	Reserved. Must be written with zero. Contains zeros when read.
4	HW_RX_125M_N	RW	Hardware reset used in registering all control signals programmed through APB registers to the 125 MHz RX_CLK domain
3	TX_125M_N	RW	Reset bit that resets the whole of the Tx 125 MHz domain
2	RX_125M_N	RW	Reset bit that resets the whole of the Rx 125 MHz domain
1	TX_CLK_N	RW	Reset bit for the TX_CLK domain (2.5, 25, 125 MHz)
0	RX_CLK_N	RW	Reset bit for the RX_CLK domain (2.5, 25, 125 MHz)

8.8.3 SERDES Control and Status Signals (SGMII_SERDES)

Address: 0x18070018
Access: Read/Write
Reset: See field description

This register comprises of all control/status signals to and from the SERDES.

Bit	Bit Name	Type	Reset		Description
31	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
30:27	VCO_REG	RW	0x3	VCO speed increase	
				00	VCO increase speed by 10%
				01	VCO increased by 5%
				10	
				11	Default setting
26:23	RES_ CALIBRATION	RW	0x0	Resistor calibration from the PHY analog	
22	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
21:20	FIBER_MODE	RW	0x0	Indicates the fiber mode	
				00	Not in fiber mode
				01	100 Base-Tx mode and 1-bit recovered data
				10	Forbidden
				11	1000 Base-Tx mode
19:18	THRESHOLD_ CTRL	RW	0x0	Signal detection threshold setting control	
				00, 01	-2 dB
				10, 11	+2 dB

17	FIBER_SDO	RW	0x0	Fiber signal detection output indicating whether there is any data through the fiber	
				0	Valid data through the fiber
				1	No data through fiber
16	EN_SIGNAL_ DETECT	RW	0x1	SGMII signal detection	
				0	Disabled
				1	Enabled
15	LOCK_DETECT_ STATUS	RW	0x0	SGMII PLL lock status. For testing only.	
				0	PLL lock
				1	PLL not locked
14:9	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
8	PLL_BW	RW	0x1	SGMII PLL bandwidth	
				0	Low bandwidth
				1	High bandwidth
7	TX_IMPEDANCE	RW	0x0	Rx output single-ended termination	
				0	50 Ω termination
				1	75 Ω termination
6:4	TX_DR_CTRL	RW	0x1	Driver output VDIFF	
				000	500 mV
				001	600 mV
				010	700 mV
				011	800 mV
				100	900 mV
				101	1 V
				110	1.1 V
				111	1.2 V
3	HALF_TX	RW	0x0	Tx driver amplitude	
				0	Tx driver amplitude normal
				1	Tx driver amplitude is half
2:1	CDR_BW	RW	0x3	CDR digital accumulator length control	
				00	± 0
				01	± 2
				10	± 4
				11	± 8
0	RX_IMPEDANCE	RW	0x0	Rx input single-ended termination	
				0	50 Ω termination
				1	75 Ω termination

8.8.4 PHY Management Control (MR_AN_CONTROL)

Address: 0x1807001C
Access: Read/Write
Reset: See field description

This register contains bits to control the PHY operation.

Bit	Bit Name	Type	Reset	Description	
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
15	PHY_RESET	RW	0x0	0	Normal operation
				1	PHY reset
14	LOOPBACK	RW	0x0	0	Disable loopback mode
				1	Enable loopback mode
13	SPEED_SEL0	RW	0x0	LSB bit speed selection	
				00	10 Mb/s
				01	100 Mb/s
				10	1000 Mb/s
				11	Reserved
12	AN_ENABLE	RW	0x1	0	Disable auto-negotiation process
				1	Enable auto-negotiation process
11	POWER_DOWN	RW	0x0	Resets the whole PCS logic	
				0	Normal operation
				1	Power down
10	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
9	RESTART_AN	RW	0x0	0	Normal operation
				1	Restart auto-negotiation process
8	DUPLEX_MODE	RW	0x1	0	Half duplex
				1	Full duplex
7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
6	SPEED_SEL1	RW	0x1	MSB bit of speed selection	
				00	10 Mb/s
				01	100 Mb/s
				10	1000 Mb/s
				11	Reserved
5:0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	

8.8.5 PHY Management Status (MR_AN_STATUS)

Address: 0x18070020
Access: Read/Write
Reset: See field description

This register is for the auto-negotiation status.

Bit	Bit Name	Type	Reset	Description	
31:8	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
7	BASE_PAGE	RW	0x0	Indicates that the base page during auto-negotiation has been transmitted	
6	NO_PREAMBLE	RW	0x1	0	Indicates that PHY will not accept management frames with preamble pattern suppressed
				1	Indicates that PHY will accept management frames with preamble pattern suppressed
5	AN_COMPLETE	RW	0x0	0	Auto-negotiation incomplete
				1	Auto-negotiation complete
4	REMOTE_FAULT	RW	0x0	0	No remote fault condition detected
				1	Remote fault condition detected
3	AN_ABILITY	RW	0x1	Indicates that the SGMII PHY is capable to perform auto-negotiation	
2	LINK_UP	RW	0x0	0	Link down
				1	Link up
1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
0	EXT_CAPABILITY	RW	0x1	0	Basic register set capabilities only
				1	Indicates that SGMII PHY provides extended register capabilities

8.8.6 AN Adverse Ability (AN_ADV_ABILITY)

Address: 0x18070024
Access: Read/Write
Reset: See field description

This register indicates the adverse ability of the local device in BASEX mode. Should be utilized when the MODE_CTRL bits in the SGMII Configuration (SGMII_CONFIG) register is set.

Bit	Bit Name	Type	Reset	Description	
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
15	NEXT_PAGE	RW	0x0	0	Next page not avialable
				1	Request to transmit Next Page
14	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
13:12	REMOTE_FAULT	RW	0x0	Provides simple fault and error information	
				00	No error
				01	Link OK
				10	Offline
				11	AN error
11:9	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
8	ASYM_PAUSE	RW	0x0	Indicates device is capable of provideing symmetric pause functions.	
				00	No Pause
				01	Symmetric pause
				10	Asymmetric pause toward link partner.
				11	Both symmetric and asymmetric pause toward local device
7	PAUSE	RW	0x0	Indicates device is capable of provideing symmetric pause functions.	
				00	No Pause
				01	Symmetric pause
				10	Asymmetric pause toward link partner.
				11	Both symmetric and asymmetric pause toward local device
6	HALF_DUPLEX	RW	0x1	Half duplex mode	
5	FULL_DUPLEX	RW	0x1	Full duplex mode	
4:0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	

8.8.7 AN Link Partner Ability (AN_LINK_PARTNER_ABILITY)

Address: 0x18070028
Access: Read/Write
Reset: Read Only

Indicates the ability of link partner device in the BASEX mode. This register is valid only when the MODE_CTRL bits in SGMII Configuration (SGMII_CONFIG) register is set.

Bit	Bit Name	Type	Reset	Description	
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
15	NEXT_PAGE	RO	0x0	0	Next page not avialable
				1	Request to transmit Next Page
14	ACK	RO	0x0	Acknowledge is used by the AN funciton to indicate that a device has succesfully received its link partner's base or next page	
				0	Page not recieved
				1	Page successfully received
13:12	REMOTE_FAULT	RO	0x0	Provides simple fault and error information	
				00	No error
				01	Link OK
				10	Offline
				11	AN error
11:9	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
8	ASYM_PAUSE	RO	0x0	Indicates device is capable of provideing symmetric pause functions.	
				00	No Pause
				01	Symmetric pause
				10	Asymmetric pause toward link partner.
				11	Both symmetric and asymmetric pause toward local device
7	PAUSE	RO	0x0	Indicates device is capable of provideing symmetric pause functions.	
				00	No Pause
				01	Symmetric pause
				10	Asymmetric pause toward link partner.
				11	Both symmetric and asymmetric pause toward local device
6	HALF_DUPLEX	RO	0x1	Half duplex mode	
5	FULL_DUPLEX	RO	0x1	Full duplex mode	
4:0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	

8.8.8 Auto Negotiation Next Page Transmission (AN_NP_TX)

Address: 0x1807002C
Access: Read/Write
Reset: See field description

This register contains the next page link code word to be transmitted when next page ability is supported.

Bit	Bit Name	Type	Reset	Description	
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
15	NEXT_PAGE	RW	0x0	0	Next page not available
				1	Request to transmit next page
14	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
13	MESSAGE_PAGE	RW	0x0	Differentiates a message page from an unformatted page	
				0	Unformatted page
				1	Message page
12	ACK2	RW	0x0	Acknowledge 2 is used by the NP function to indicate that a device can comply with the message	
				0	Cannot comply with message
				1	Will comply with message
11	TOGGLE	RW	0x0	Used by the arbitration function to synchronize with the link partner during next page exchange	
				0	Previous value of transmitted link code word equalled logic one
				1	previous value of transmitted link code word equalled logic zero
10:0	MSG_UNFORM_ CODE	RW	0x0	Depends on bit [13] of this register. Message code field is an 11 bit wide field, encoding 2048 possible messages	

8.8.9 Auto Negotiation Next Page Receive (AN_LP_NP_RX)

Address: 0x18070030
Access: Read/Write
Reset: See field description

This register contains the next page link code word to be transmitted when next page ability is supported.

Bit	Bit Name	Type	Reset	Description	
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
15	NEXT_PAGE	RW	0x0	0	Next page not available
				1	Request to transmit next page
14	ACK	RW	0x0	Acknowledge is used by the NP function to indicate that a device can comply with the message	
				0	Cannot comply with message
				1	Will comply with message
13	MESSAGE_PAGE	RW	0x0	Differentiates a message page from an unformatted page	
				0	Unformatted page
				1	Message page

12	ACK2	RW	0x0	Acknowledge 2 is used by the NP function to indicate that a device can comply with the message	
				0	Cannot comply with message
				1	Will comply with message
11	TOGGLE	RW	0x0	Used by the arbitration function to synchronize with the link partner during next page exchange	
				0	Previous value of transmitted link code word equalled logic one
				1	Previous value of transmitted link code word equalled logic zero
10:0	MSG_UNFORM_ CODE	RW	0x0	Depends on bit [13] of this register. The message code field is an 11-bit wide field, encoding 2048 possible messages.	

8.8.10 SGMII Configuration (SGMII_CONFIG)

Address: 0x18070034
Access: Read/Write
Reset: See field description

This register contains configuration bits to enable SGMII mode of operation, PRBS, and MDIO.

Bit	Bit Name	Type	Reset		Description
31:15	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
14	PRBS_BERT_ ENABLE	RW	0x0	Enables the bit error rate feature	
13	PRBS_ENABLE	RW	0x0	Enables the PRBS feature in SGMII	
12	MDIO_ COMPLETE	RW	0x0	Indicates that the MDIO command is completely received	
11	MDIO_PULSE	RW	0x0	Pulse signal to indicate that an MDIO command is ready for transmitting	
10	MDIO_ENABLE	RW	0x0	Enables SGMII-MDIO function	
9	NEXT_PAGE_ LOADED	RW	0x0	0	Next page not loaded
				1	Indicates the next page is loaded for transmitting during auto-negotiation
8	REMOTE_PHY_ LOOPBACK	RW	0x0	0	No remote PHY loopback
				1	Indicates the remote PHY loopback is enabled
7:6	SPEED	RW	0x0	Forces the speed to be a certain level; only valid when bit [5] is set	
				0	10 MBps
				1	100 MBps
				2	1000 MBps
5	FORCE_SPEED	RW	0x0	Indicates the speed selection is forced by CPU, when forced auto-negotiation is disabled	
4	RES	RO	0x0	Reserved	
3	ENABLE_SGMII_ TX_PAUSE	RW	0x0	Enable transmitting pause in the base page when in SGMII PHY mode	
2:0	MODE_CTRL	RW	0x0	SGMII mode control	
				0	BASEX
				1	SGMII_PHY
				2	SGMII_MAC

8.8.11 SGMII PHY Link Partner Ability (SGMII_MAC_RX_CONFIG)

Address: 0x18070038
Access: Read/Write
Reset: See field description

This register indicates the SGMII PHY link partners abilities to the SGMII MAC. This register is valid only when the MODE_CTRL bits in SGMII Configuration (SGMII_CONFIG) register is set to 3'h2. This register is read-only.

Bit	Bit Name	Type	Reset	Description	
31:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
15	LINK	RO	0x0	0	Link down
				1	Link up
14	ACK	RO	0x0	Acknowledge is used to indicate that a PHY has also successfully received MAC's configuration information	
				0	Page not received
				1	Page received
13	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
12	DUPLEX_MODE	RO	0x0	Indicates the duplex mode of the LP	
				0	Half duplex
				1	Full duplex
11:10	SPEED_MODE	RO	0x0	The speed of the LP	
				00	10 MBps
				01	100 MBps
				10	1000 MBps
				11	Reserved
9	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
8	AYSM_PAUSE	RO	0x0	Indicates device is capable of providing symmetric pause functions.	
7	PAUSE	RO	0x0	Indicates device is capable of providing symmetric pause functions.	
6:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
0	RES	RO	0x1	Reserved. Should be set to 1.	

8.8.12 SGMII PHY Tx Configuration (SGMII_PHY_TX_CONFIG)

Address: 0x1807003C
Access: Read/Write
Reset: See field description

This is the PHY capabilities register which is transmitted to the SGMII MAC to advertise the PHY abilities. This register should be programmed when the MODE_CTRL bits in SGMII Configuration (SGMII_CONFIG) register is set to 3'h2. This register is read-only.

Bit	Bit Name	Type	Reset	Description	
31:6	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
5	ASYM_PAUSE	RO	0x0	Indicates device is capable of provideing symmetric pause functions.	
				00	No Pause
				01	Symmetric pause
				10	Asymmetric pause toward link partner.
				11	Both symmetric and asymmetric pause toward local device
4	PAUSE	RO	0x0	Indicates device is capable of provideing symmetric pause functions.	
				00	No Pause
				01	Symmetric pause
				10	Asymmetric pause toward link partner.
				11	Both symmetric and asymmetric pause toward local device
3	LINK	RO	0x0	0	Link down
				1	Link up
2	DUPLEX_MODE	RO	0x0	Indicates the duplex mode of the LP	
				0	Half duplex
				1	Full duplex
1:0	SPEED_MODE	RO	0x0	The speed of the LP	
				00	10 MBps
				01	100 MBps
				10	1000 MBps
				11	Reserved

8.8.13 SGMII MDIO Transmit (SGMII_MDIO_TX)

Address: 0x18070040
Access: Read/Write
Reset: See field description

SGMII MDIO register which transmits the command in MDIO mode

Bit	Bit Name	Type	Reset	Description
31:0	REG_VAL	RW	0x0	MDIO command for transmitting

8.8.14 SGMII MDIO Receive (SGMII_MDIO_RX)

Address: 0x18070044
Access: Read/Write
Reset: See field description

SGMII MDIO register which contains the command received

Bit	Bit Name	Type	Reset	Description
31:0	REG_VAL	RW	0x0	MDIO command received

8.8.15 Energey Efficient Ethernet (EEE)

Address: 0x18070048
Access: Read/Write
Reset: See field description

These register bits enable the LPI mode of operation and indicates the LPI status

Bit	Bit Name	Type	Reset	Description
31:22	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
21:6	WAKE_ERR_CNT	RO	0x0	Count value for wake period error
5	DISABLE_AUTO_LPI	RW	0x1	Disable the auto-detect link partner's az ability. Valid when bit 0 is zero.
4	RX_LPI_ACTIVE	R	0x0	This signal indicates that the receiver is in LPI mode
3	RX_QUIET	R	0x0	This signal indicates the receiver has been switched off
2	TX_QUIET	R	0x0	This signal indicates the transmitterhas been switched off
1	AUTO_LPI_EN	R	0x0	Automatic detection of LPI mode supported by the receiver. When bit 4 is asserted once, this bit will latch that value to indicate that the link partner has the ability of LPI. Is valid when both bit 0 and bit 5 are zero.
0	BASEX_AZ_EN	RW	0x0	Enables AZ funciton to let the Tx and Rx be queit when in LPI mode

8.8.16 SGMII Resolution (SGMII_RESOLVE)

Address: 0x18070054
Access: Read/Write
Reset: See field description

This register indicates the status of the priority resolution for duplex modes, pause capabilities, etc.

Bit	Bit Name	Type	Reset	Description
31:7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
6	LINK_FAIL_CFGO	RW	0x0	Indicates a link failure during configuration
5	SYNC_STATUS	RW	0x0	Indicates a sync status
4	AN_SYNC_STATUS	RW	0x0	Indicates a sync status during auto-negotiation
3	RECEIVE_PAUSE_ ENABLE	RW	0x0	Receive pause capability enabled
2	TRANSMIT_PAUSE	RW	0x0	Transmit pause capability enabled
1	DUPLEX_ERROR	RW	0x0	Duplex mode between device and LP does not match
0	DUPLEX_MODE	RW	0x0	Device and LP resolved duplex mode as full duplex

8.8.17 SGMII Interrupt (SGMII_INTERRUPT)

Address: 0x1807005C
Access: Read/Write
Reset: See field description

This register causes an interrupt when there is a change in the link or in duplex modes.

Bit	Bit Name	Type	Reset	Description
31:7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:0	INTR	RW	0x0	SGMII interrupt

8.8.18 SGMII Interrupt Mask (SGMII_INTERRUPT_MASK)

Address: 0x18070060
Access: Read/Write
Reset: See field description

This register is the mask to enable or disable SGMII interrupts.

Bit	Bit Name	Type	Reset	Description	
31:7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
6:0	MASK	RW	0x0	0	Interrupt masked
				1	Interrupt enabled

8.9 PCIE RC Control Registers

Table 8-10 summarizes the PCIE RC control registers for the QCA9563.

Table 8-10 PCIE RC Control Registers

Address	Name	Description	Page
0x18250000	PCIE_APP	PCIE Application Control	page 174
0x18250004	PCIE_AER	PCIE Interrupt and Error	page 174
0x18250008	PCIE_PWR_MGMT	PCIE Power Management	page 175
0x1825000C	PCIE_ELEC	PCIE Electromechanical	page 175
0x18250010	PCIE_CFG	PCIE Configuration	page 176
0x18250014	PCIE_RX_CNTL	PCIE Receive Completion	page 177
0x18250018	PCIE_RESET	PCIE Reset	page 177
0x1825001C	PCIE_DEBUG	PCIE Debug and Control	page 178
0x18250024	PCIE_PHY_RW_DATA	PCIE PHY Read/Write Data	page 178
0x18250028	PCIE_PHY_TRG_RD_LOAD	PCIE PHY Serial Interface Load/Read Trigger	page 179
0x1825002C	PCIE_PHY_CFG_DATA	PCIE PHY Configuration Data	page 179
0x18250030	PCIE_MAC_PHY	PCIE MAC-PHY Interface Signals	page 179
0x18250034	PCIE_PHY_MAC	PCIE PHY-MAC Interface Signals	page 180
0x18250038	PCIE_SIDEBAND1	PCIE Sideband Bus1	page 180
0x1825003C	PCIE_SIDEBAND2	PCIE Sideband Bus2	page 180
0x18250040	PCIE_SPARE	PCIE Spare	page 181
0x18250044	PCIE_MSI_ADDR	PCIE MSI Lower Address	page 181
0x18250048	PCIE_MSI_DATA	PCIE MSI Data Value	page 181
0x1825004C	PCIE_INT_STATUS	PCIE Interrupt Status	page 181
0x18250050	PCIE_INT_MASK	PCIE Interrupt Mask	page 183
0x18250054	PCIE_ERR_CNT	PCIE Error Counter	page 184
0x18250058	PCIE_REQ_LATENCY_W_INT	PCIE AHB Latency Interrupt Counter	page 184
0x1825005C	PCIE_MISC	Miscellaneous PCIE Bits	page 184

8.9.1 PCIE Application Control (PCIE_APP)

Address: 0x18250000
Access: Read/Write
Reset: See field description

This register provides various control and status bits to configure the PCIE RC core from the application side.

Bit	Bit Name	Reset	Description
31:22	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
21:20	CFG_TYPE	0x0	0 Sending a configuration transaction to the immediate downstream component (switch, endpoint) (Default) 1 Sending a type 1 configuration transaction to multiple endpoints via a switch.
19:16	PCIE_BAR_MSN	0x1	Most significant nibble of the register PCIE Interrupt and Error (PCIE_AER).
15:12	CFG_BE	0xF	Used as the byte enable of the next configuration request sent out on the PCIE interface.
11:6	SLV_RESP_ ERR_MAP	0x3F	AHB slave response for a previous PCIE transaction. The response bits are mapped as: 6 bits == {completion_tlp_abort, completion_ecrc, completion_ep, completion_crs, completion_ca, completion_ur}, where: 0 SLVERR 1 DECERR
5:4	MSTR_RESP_ ERR_MAP	0x0	AHB master response error map. This signal allows the application to select a master response error report mechanism received from an AHB response channel to the CPL status of native PCIE core transmissions. MSB is not currently used. ■ When the LSB is set to 0, it will set an AHB response error to a CA of a PCIE completion: 2 bits == {decerr, slverr} ■ When the LSB is set to 1, it will set an AHB response error to a UR of a PCIE completion.
3	INIT_RST	0x0	Application request to initiate a training reset
2	PM_XMT_ TURNOFF	0x0	Application signal to generate PM turnoff messages for power management
1	UNLOCK_MSG	0x0	Wakeup status because of power fault
0	LTSSM_ENABLE	0x0	Application signal to enable the LTSSM. If set to zero, it indicates that the application is not ready.

8.9.2 PCIE Interrupt and Error (PCIE_AER)

Address: 0x18250004
Access: Read-Only
Reset: 0x0

This register contains common transmit and receive advanced error (AER) counters, such as bad DLLP, BAD TLP, NAKS, REPLAY TIMEOUTS, and so on.

Bit	Bit Name	Description
31:24	ERR_CNT4	Counter for replay timeouts/replay rollover
23:16	ERR_CNT3	Counter for receive errors (coding and disparity errors)

15:8	ERR_CNT2	Counter for transmit NAKs
7:0	ERR_CNT1	Counter for bad TLP and DLLP errors

8.9.3 PCIE Power Management (PCIE_PWR_MGMT)

Address: 0x18250008
Access: Read/Write
Reset: 0x0

This register controls application control and status signals needed for power management.

Bit	Bit Name	Description
31:9	RES	Reserved
8	PME_INT	Interrupt caused by PME
6	RADM_PM_TO_ACK	Receipt of a PME turnoff acknowledgement message (the signal that indicates that the RC received a PME_TO_ACK message)
5	RADM_PM_PME	Receipt of a PME message (the signal that indicates that the RC received a PM_PME message)
4	AUX_PM_EN	AUX power PM enable; enable device to draw auxiliary power independent of PME AUX power
3	READY_ENTR_L23	Indication from the application that it is ready to enter the L2/L3 state
2	REQ_EXIT_L1	Request from the application to exit ASPM state L1, only effective if L1 is enabled
1	REQ_ENTRY_L1	Capability for applications to request PM state to enter L1; only effective if ASPM of L1 is enabled
0	AUX_PWR_DET	Auxiliary power detected; indicates that auxiliary power (VAUX) is present

8.9.4 PCIE Electromechanical (PCIE_ELEC)

Address: 0x1825000C
Access: See field description
Reset: 0x0

Bit	Bit Name	Access	Description	
31:3	RES	RW	Reserved	
2	SYS_ATTEN_ BUTTON_PRESSED	RW	Attention button pressed. Indicates that the system attention button was pressed, sets the attention button pressed bit in the Slot Status register	
1	CLK_REQ_N	RO	Clock enable Allows the application clock generation module to turn off CORE_CLK based on the current power management state:	
			0	CORE_CLK must be active for the current power state
			1	Current power state allows CORE_CLK to be shut down
0	WAKE_N	RO	Wake up from power management unit. PCIE RC core generates WAKE_L to request the system to restore power and clock when a beacon has been detected. Assertion of WAKE_L could be a clock or multiple clock cycles.	

8.9.5 PCIE Configuration (PCIE_CFG)

Address: 0x18250010
Access: Read/Write
Reset: 0x0

This registers controls application control and status signals to configure core behavior.

Bit	Bit Name	Description
31	RES	Reserved. Must be written with zero. Contains zeros when read.
30:26	INT_MSG_NUM	Advanced error interrupt message number Used when MSI or MSI-X is enabled. Assertion of CFG_AER_RC_ERR_MSI along with a value on CFG_AER_INT_MSG_NUM is equivalent to the RC core receiving an MSI with the CFG_AER_INT_MSG_NUM value as the MSI vector.
25	EML_CONTROL	Electromechanical interlock control; this bit denotes the state of the electromechanical interlock control bit in PCIE Electromechanical (PCIE_ELEC) register.
24	PWR_CTRLER_ CTRL	Power controller control; this bit controls the system power controller (from bit [10] of the PCIE Receive Completion (PCIE_RX_CNTL) register).
23:22	ATTEN_IND	Attention indicator control; these bits control the system attention indicator) from bits [7:6] of the PCIE Receive Completion (PCIE_RX_CNTL) register).
21:17	PBUS_DEV_NUM	Configured device number; denotes the device number assigned to the device.
16:9	PBUS_NUM	The configured primary bus number. These bits denote the primary bus number assigned to the device.
8	RCB	The read completion boundary (RCB). This bit denotes the value of the RCB bit in the Link Control register in the PCIE RC.
7:5	MAX_PAYLOAD_ SIZE	The maximum payload size. This bit denotes the value of the MAX_PAYLOAD_SIZE field in the Device Control register in the PCIE RC.
4:2	MAX_RDREQ_ SIZE	The maximum read request size. This bit denotes the value of the MAX_READ_ REQUEST_SIZE field in the Device Control register in the PCIE RC.
1	MEM_SPACE_EN	Memory space enable; this bit denotes the state of the Memory Space Enable bit in the PCI-compatible Command register in the PCIE RC.
0	BUS_MASTER_ EN	Bus master enable; this bit denotes the state of the Bus Master Enable bit in the PCI-compatible Command register in the PCIE RC.

8.9.6 PCIE Receive Completion (PCIE_RX_CNTL)

Address: 0x18250014
Access: Read-Only
Reset: 0x0

This register is used to denote the field values related to the completion timeout of the PCIE.

Bit	Bit Name	Description
31:29	RES	Reserved. Must be written with zero. Contains zeros when read.
28:21	TIMEOUT_CPL_ TAG	The tag field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted
20:9	TIMEOUT_CPL_ LEN	The length field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted.
8:7	TIMEOUT_CPL _ATTR	The attributes field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted.
6:4	TIMEOUT_CPL_ TC	The traffic class of the timed out completion. This bit is valid when the PCIE core Rx timeout signal is asserted.
3:1	TIMEOUT_FN_ NUM	The function number of the timed out completion. This bit is valid when the PCIE core Rx timeout signal is asserted.
0	CPL_TIMEOUT	The completion timeout. This bit indicates that the completion TLP for a request has not been received within the expected time window.

8.9.7 PCIE Reset (PCIE_RESET)

Address: 0x18250018
Access: Read/Write
Reset: See field description

This register is used to set the bits for the PCIE reset.

Bit	Bit Name	Reset	Description	
31:3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
2	EP_RESET_L	0x1	The reset bit for indicating an endpoint reset through the PCIE PHY	
1	LINK_REQ_ RESET	0x0	The reset request due to a link down status. A high-to-low transition indicates that the RC Core is requesting external logic to reset the RC Core because the PHY link is down.	
0	LINK_UP	0x0	Indicates if the PHY link is up or down	
			0	Link is down
			1	Link is up

8.9.8 PCIE Debug and Control (PCIE_DEBUG)

Address: 0x1825001C
Access: Read/Write
Reset: See field description

This register controls application and status signals for additional debug and configuration of the core behavior.

Bit	Bit Name	Reset	Description	
31:18	RES	0x0	Reserved	
17	AHB_MSTR_DATA_SWAP_EN	0x0	AHB master: byte swap configuration option	
16	PCIE_PHY_READY	0x0	PCIE PHy's ready signal	
15	RXVALID_EXT_ENABLE	0x0	Enable bit for extending rxvalid from PHY by three clocks	
14	BYTESWAP	0x1	AHB slave: byte swap configuration option	
13	PM_STATUS	0x0	Power management status: PME status bit from the PMCSR	
12	PM_PME_EN	0x0	Power management event (PME) enable: PME enable bit in the PMCSR	
11:9	PM_DSTATE	0x0	Current power management D-state of the function	
8:4	XMLH_LTSSM_STATE	0x0	Current LTSSM state	
3:1	PM_CURNT_STATE	0x0	Current power state	
0	RDLH_LINK_UP	0x0	DATA link layer up/down indicator This status from the flow control initialization state machine indicates that flow control has been initiated and the data link Layer is ready to transmit and receive packets.	
			0	Link is down
			1	Link is up

8.9.9 PCIE PHY Read/Write Data (PCIE_PHY_RW_DATA)

Address: 0x18250024
Access: Read/Write
Reset: 0x0

This register would trigger a read and a write to the PCIE PHY Serial Interface.

Bit	Bit Name	Description
31:0	PHY_DATA	PCIE PHY data read/write

8.9.10 PCIE PHY Serial Interface Load/Read Trigger (PCIE_PHY_TRG_RD_LOAD)

Address: 0x18250028
Access: Read-Only
Reset: 0x0

This register triggers a read or a load for the PCIE PHY serial interface.

Bit	Bit Name	Description	
31:0	PARALLEL_LOAD_OP_DONE	Bit 0	Parallel Load: Trigger a Parallel Load to the PCIE PHY - Would be cleared on Operation Complete
		Bit 31	OP_DONE: Indicates that the previous Operation is completed. Read / Write - Gets cleared on read/write to PCIE_PHY_RW_DATA register

8.9.11 PCIE PHY Configuration Data (PCIE_PHY_CFG_DATA)

Address: 0x1825002C
Access: Read-Only
Reset: 0x0 (32'd5)

Bit	Bit Name	Description
31:0	PHY_CFG_DATA	PCIE PHY configuration data

8.9.12 PCIE MAC-PHY Interface Signals (PCIE_MAC_PHY)

Address: 0x18250030
Access: Read-Only
Reset: See field description

This register is used to denote the interface signals for the MAC-PHY interface.

Bit	Bit Name	Description	
31:24	RES	Reserved	
23:22	PWRDOWN	The power control. Power control bits to the PHY. The MAC_PHY_POWERDOWN is a 2-bit signal that is shared by all Lanes.	
		00	P0 (normal operation)
		01	P0s (Low power, small latency for recovery)
		10	P1 (Much lower power but longer latency for recovery)
		11	P2 (Lowest power state)
21	RXPOLARITY	Inverted polarity on receive	
20	TXCOMPLIANCE	MAC_PHY_TX compliance status	
19	TXELECIDLE	Transmit electrical idle status	
18	TXDETRX_LOOPBACK	Status of MAC_PHY_TXDETECTRX from RC	
17:16	TXDATAK	Data/control indication for transmit data symbols. When set to 1, indicates a "K" or control symbol.	
15:0	TXDATA	PCIE RC transmit data from MAC to PHY	

8.9.13 PCIE PHY-MAC Interface Signals (PCIE_PHY_MAC)

Address: 0x18250034
Access: Read-Only
Reset: 0x0

This register is used to denote the interface signals for the PHY-MAC interface.

Bit	Bit Name	Description
31:26	RES	Reserved. Must be written with zero. Contains zeros when read.
25	RXDETECT_DONE	Indicated a successful receiver detection
24	PHYSTATUS_ASSERTED	Indicates that PHYSTATUS (bit [22])has been asserted
23	RXVALID	Indicates PIPE Rx data valid
22	PHYSTATUS	Indicates PIPE PHY status
21:19	RXSTATUS	Indicates PIPE Rx status
18	RXELECIDLE	Indicates PIPE electrical idle
17:16	RXDATAK	Data/control for the receive data symbols
15:0	RXDATA	PIPE receive data

8.9.14 PCIE Sideband Bus1 (PCIE_SIDEBAND1)

Address: 0x18250038
Access: Read-Only
Reset: 0x0

This register is used to control additional PHY purposes.

Bit	Bit Name	Description
31:0	CFG_PHY_CONTROL	The output bus that can be used for additional PHY control purposes. The CFG_ PHY_CONTROL bus maps to the PHY control register.

8.9.15 PCIE Sideband Bus2 (PCIE_SIDEBAND2)

Address: 0x1825003C
Access: Read-Only
Reset: 0x0

This register is used to control additional PHY purposes.

Bit	Bit Name	Description
31:0	CFG_PHY_CONTROL	The output bus that can be used for additional PHY control purposes. The CFG_ PHY_CONTROL bus maps to the PHY control register.

8.9.16 PCIE Spare (PCIE_SPARE)

Address: 0x18250040
Access: Read-Only
Reset: 0x0

This register is contains spare bits for the PCIE.

Bit	Bit Name	Description
31:0	BITS	Spare bits for the PCIE

8.9.17 PCIE MSI Lower Address (PCIE_MSI_ADDR)

Address: 0x18250044
Access: Read/Write
Reset: 0x0

This register holds the lower address for the MSI.

Bit	Bit Name	Description
31:0	LADDR	The lower address register for the MSI

8.9.18 PCIE MSI Data Value (PCIE_MSI_DATA)

Address: 0x18250048
Access: Read/Write
Reset: 0x0

This register is used to hold the data for the MSI including vector.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	VALUE	These bits hold the data for the MSI including vector [4:0]. The pattern assigned by the system software.

8.9.19 PCIE Interrupt Status (PCIE_INT_STATUS)

Address: 0x1825004C
Access: Read/Write
Reset: 0x0

This register reflects the status of currently active interrupts. A 1 in a bit position indicates the corresponding interrupt is active.

Bit	Bit Name	Description
31:28	RES	Reserved. Must be written with zero. Contains zeros when read.
27	LINK_DOWN	XMLH link down interrupt
26	LINK_REQ_RST	Request for reset from the PCIE RC core to the application.
25:22	MSI_VEC	Indicates which MSI interrupt has happened

21	CPU_INTD	The status bit to indicate that an INTD assertion has occurred and the client needs to send a deassert interrupt
20	CPU_INTC	The status bit to indicate that an INTC assertion has occurred and the client needs to send a deassert interrupt
19	CPU_INTB	The status bit to indicate that an INTB assertion has occurred and the client needs to send a deassert interrupt
18	CPU_INTA	The status bit to indicate that an INTA assertion has occurred and the client needs to send a deassert interrupt
17	INTDL	PCI 3.0 compatible, level triggered INTD virtual wire interrupt. This interrupt is ON on reception of INTD assertion message and stays on till the corresponding deassertion message is received.
16	INTCL	PCI 3.0 compatible, level triggered INTC virtual wire interrupt. This interrupt is ON on reception of INTC assertion message and stays on till the corresponding deassertion message is received.
15	INTBL	PCI 3.0 compatible, level triggered INTB virtual wire interrupt. This interrupt is ON on reception of INTB assertion message and stays on till the corresponding deassertion message is received.
14	INTAL	PCI 3.0 compatible, level triggered INTA virtual wire interrupt. This interrupt is ON on reception of INTA assertion message and stays on till the corresponding deassertion message is received.
13	SYS_ERR	A system error. The RC Core asserts CFG_SYS_ERR_RC if any device in the hierarchy reports any of the following errors and the associated enable bit is set in the Root Control register: ERR_COR, ERR_FATAL, ERR_NONFATAL.
12	AER_MSI	Advanced error MSI or MSI-X indication; CFG_AER_RC_ERR_MSI is set when: ■ MSI or MSI-X is enabled ■ A reported error condition causes a bit to be set in the Root Error Status register. ■ The associated error message reporting enable bit is set in the Root Error Command register.
11	AER_INT	Advanced error reporting interrupt; This interrupt is set when an internally generated error message is to be propagated to the software by PCIE root complex.
10	MSI_ERR	Error MSI interrupt Interrupt is set whenever an MSI error message is received by the PCIE root complex.
9	MSI	The interrupt caused by the MSI
8	INTD	PCI 3.0 compatible, edge triggered INTD virtual wire interrupt This interrupt is set on reception of INTD assertion message; software must explicitly write a 0 to this bit to clear the interrupt condition.
7	INTC	PCI 3.0 compatible, edge triggered INTC virtual wire interrupt This interrupt is set on reception of INTC assertion message; software must explicitly write a 0 to this bit to clear the interrupt condition.
6	INTB	PCI 3.0 compatible, edge triggered INTB virtual wire interrupt This interrupt is set on reception of INTB assertion message; software must explicitly write a 0 to this bit to clear the interrupt condition.
5	INTA	PCI 3.0 compatible, edge triggered INTA virtual wire interrupt This interrupt is set on reception of INTA assertion message; software must explicitly write a 0 to this bit to clear the interrupt condition.
4	RADMX_COMP_ LOOKUP_ERR	The RADMX response composer TAG lookup error. This is a fatal error condition.
3	GM_COMP_ LOOKUP_ERR	GM response composer TAG lookup error. This is a fatal error condition.
2	FATAL_ERR	The received fatal error message. One clock cycle pulse that indicates that the RC core received an ERR_FATAL message
1	NONFATAL_ERR	The received non-fatal error message. One clock cycle pulse that indicates that the RC core received an ERR_NONFATAL message
0	CORR_ERR	The received correctable error message. One clock cycle pulse that indicates that the RC core received an ERR_COR message.

8.9.20 PCIE Interrupt Mask (PCIE_INT_MASK)

Address: 0x18250050
Access: Read/Write
Reset: 0x0

Selectively enables or disables propagation of interrupts. A "1" in a bit position enables the corresponding interrupt being asserted. A "0" in a bit position disables the corresponding interrupt being asserted.

Bit	Bit Name	Description
31:28	RES	Reserved. Must be written with zero. Contains zeros when read.
27	LINK_DOWN	XMLH link down interrupt mask
26	LINK_REQ_RST	PCIE RC link reset link request int mask
25:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17	INTDL	Mask for the assertion+deassertion of the INTD virtual wire level-triggered interrupt.
16	INTCL	Mask for the assertion+deassertion of the INTC virtual wire level-triggered interrupt.
15	INTBL	Mask for the assertion+deassertion of the INTB virtual wire level-triggered interrupt.
14	INTAL	Mask for the assertion+deassertion of the INTA virtual wire level-triggered interrupt.
13	SYS_ERR	System error interrupt mask
12	AER_MSI	Mask for advanced error (AER) MSI or MSI-X indication interrupt
11	AER_INT	AER interrupt mask
10	MSI_ERR	MSI error interrupt
9	MSI	Interrupt caused by the MSI
8	INTD	INTD virtual wire edge triggered interrupt mask
7	INTC	INTC virtual wire edge triggered interrupt mask
6	INTB	INTB virtual wire edge triggered interrupt mask
5	INTA	INTA virtual wire edge triggered interrupt mask
4	RADMX_COMP_ LOOKUP_ERR	RADMX response composer TAG lookup error mask
3	GM_COMP_ LOOKUP_ERR	GM response composer TAG lookup error mask
2	FATAL_ERR	Received fatal error message interrupt (RADM_FATAL_ERR) mask
1	NONFATAL_ERR	Received non-fatal error message (RADM_NONFATAL_ERR) mask
0	CORR_ERR	Received correctable error message interrupt (RADM_CORRECTABLE_ERR) mask

8.9.21 PCIE Error Counter (PCIE_ERR_CNT)

Address: 0x18250054
Access: Read/Write
Reset: 0x0

This register keeps a count of the number of errors related to PCIE RC.

Bit	Bit Name	Description
31:0	VALUE	Indicates the number of errors related to PCIE RC; can include: bad DLLP, bad TLP, NAKS, REPLAY TIMEOUTS, and so on.

8.9.22 PCIE AHB Latency Interrupt Counter (PCIE_REQ_LATENCY_W_INT)

Address: 0x18250058
Access: Read/Write
Reset: 0x0

This register is a counter to indicate the AHB Request to AHB Ready Latency of PCIE when an interrupt is asserted.

Bit	Bit Name	Description
31	ENABLE	Counter enable
30:0	VALUE	Indicates the latency

8.9.23 Miscellaneous PCIE Bits (PCIE_MISC)

Address: 0x1825005C
Access: Read/Write
Reset: 0x0

This register contains miscellaneous spare CPU writable bits.

Bit	Bit Name	Description
31:0	BITS	Spare bits for the PCIE

8.10 WLAN MAC Registers

Table 8-11 shows the mapping of the general DMA and Rx-related (WLAN MAC interface) registers.

Table 8-11 WDMA Registers

Offset	Name	Description	Page
0x18100008	CR	Command	page 186
0x18100014	CFG	Configuration and Status	page 186
0x18100018	RXBUFPTR_THRESH	Rx DMA Data Buffer Pointer Threshold	page 187
0x1810001C	TXDPPTR_THRESH	Tx DMA Descriptor Pointer Threshold	page 187
0x18100020	MIRT	Maximum Interrupt Rate Threshold	page 188
0x18100024	IER	Interrupt Global Enable	page 188
0x18100028	TIMT	Tx Interrupt Mitigation Thresholds	page 189
0x1810002C	RIMT	Rx Interrupt Mitigation Thresholds	page 189
0x18100030	TXCFG	Transmit Configuration	page 189
0x18100034	RXCFG	Receive Configuration	page 191
0x18100040	MIBC	MIB Control	page 191
0x18100060	DATABUF	Data Buffer Length	page 192
0x18100064	GTT	Global Transmit Timeout	page 192
0x18100068	GTTM	Global Transmit Timeout Mode	page 192
0x1810006C	CST	Carrier Sense Timeout	page 193
0x18100070	RXDP_SIZE	Size of High and Low Priority	page 193
0x18100074	RX_QUEUE_HP_RXDP	Lower 32 bits of MAC Rx High Priority Queue RXDP Pointer	page 193
0x18100078	RX_QUEUE_LP_RXDP	Lower 32 bits of MAC Rx Low Priority Queue RXDP Pointer	page 193
0x18100080	ISR_P	Primary Interrupt Status	page 194
0x18100084	ISR_S0	Secondary Interrupt Status 0	page 195
0x18100088	ISR_S1	Secondary Interrupt Status 1	page 196
0x1810008C	ISR_S2	Secondary Interrupt Status 2	page 196
0x18100090	ISR_S3	Secondary Interrupt Status 3	page 197
0x18100094	ISR_S4	Secondary Interrupt Status 4	page 197
0x18100098	ISR_S5	Secondary Interrupt Status 5	page 198
0x181000A0	IMR_P	Primary Interrupt Mask	page 199
0x181000A4	IMR_S0	Secondary Interrupt Mask 0	page 200
0x181000A8	IMR_S1	Secondary Interrupt Mask 1	page 200
0x181000AC	IMR_S2	Secondary Interrupt Mask 2	page 201
0x181000B0	IMR_S3	Secondary Interrupt Mask 3	page 201
0x181000B4	IMR_S4	Secondary Interrupt Mask 4	page 202
0x181000B8	IMR_S5	Secondary Interrupt Mask 5	page 202
0x181000C0	ISR_P_RAC	Primary Interrupt Status Read-and-Clear	page 203
0x181000C4	ISR_S0_S	Secondary Interrupt Status 0 (Shadow Copy)	page 203
0x181000C8	ISR_S1_S	Secondary Interrupt Status 1 (Shadow Copy)	page 203
0x181000D0	ISR_S2_S	Secondary Interrupt Status 2 (Shadow Copy)	page 203
0x181000D4	ISR_S3_S	Secondary Interrupt Status 3 (Shadow Copy)	page 204

Table 8-11 WDMA Registers (cont.)

Offset	Name	Description	Page
0x181000D8	ISR_S4_S	Secondary Interrupt Status 4 (Shadow Copy)	page 204
0x181000DC	ISR_S5_S	Secondary Interrupt Status 5 (Shadow Copy)	page 204

8.10.1 Command (CR)

Offset: 0x18100008
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:11	RES	Reserved
10:7	SPARE	Spare bits
6	SWI	Software interrupt; this bit is one-shot/auto-cleared, so it always reads as 0
5	RXD	Rx disabled
4	RES	Reserved
3	RXE_HP	Receive enabled; this read-only bit indicates RxDMA status for HP frames. Set when SW writes to the RxBP register and cleared when RxDMA runs out of RxBP or RxD is asserted.
2	RXE_LP	Receive enabled; this read-only bit indicates RxDMA status for LP frames. Set when software writes to RXBUFPTR_THRESH register and cleared when RxDMA runs out of RXBUFPTR_THRESH or when RxD is asserted.
1:0	RES	Reserved

8.10.2 Configuration and Status (CFG)

Offset: 0x18100014
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset		Description
31:19	RES	0x0	Reserved	
18:17	FULL_THRESHOLD	0x0	PCIE core master request queue full threshold	
			0	Use default value of 4
			3:1	Use indicated value
16:13	RES	0x0	Reserved	
12	CFG_HALT_ACK	0x0	DMA halt status	
			0	DMA has not yet halted
			1	DMA has halted
11	CFG_HALT_REQ	0x0	DMA halt in preparation for reset request	
			0	DMA logic operates normally
			1	Request DMA logic to stop so software can reset the MAC; Bit [12] indicates when the halt has taken effect; the DMA halt is not recoverable; once software sets bit [11] to request a DMA halt, software must wait for bit [12] to be set and reset the MAC.
10	CFG_CLKGATE_DIS	0x0	0	Allow clock gating in all DMA blocks to operate normally
			1	Disable clock gating in all DMA blocks (for debug use)
9:6	RES	0x0	Reserved	

Bit	Bit Name	Reset	Description	
5	REG_CFG_ADHOC	0x0	0	AP mode: MAC is operating either as an AP or as a STA in a BSS
			1	Ad hoc mode: MAC is operating as a STA in an IBSS
4	MODE_MMR	0x0	Byteswap register access (MMR) data words	
3	MODE_RCV_DATA	0x0	Byteswap Rx data buffer words	
2	MODE_RCV_DESC	0x0	Byteswap Rx descriptor words	
1	MODE_XMIT_DATA	0x0	Byteswap Tx data buffer words	
0	MODE_XMIT_DESC	0x0	Byteswap Tx descriptor words	

8.10.3 Rx DMA Data Buffer Pointer Threshold (RXBUFPTR_THRESH)

Offset: 0x18100018
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:15	RES	Reserved
14:8	LP_DATA	Indicates the Rx DMA data buffer pointer threshold. An interrupt will be asserted (if enabled) if the number of available data buffer pointers is less than this threshold. There is a separate threshold for high and low priority buffers.
7:4	RES	Reserved
3:0	HP_DATA	Indicates the Rx DMA data buffer pointer threshold. An interrupt will be asserted (if enabled) if the number of available data buffer pointers is less than this threshold. The high and low priority buffers have separate thresholds.

8.10.4 Tx DMA Descriptor Pointer Threshold (TXDPPTR_THRESH)

Offset: 0x1810001C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:4	RES	Reserved
3:0	DATA	Indicates the Tx DMA descriptor pointer threshold. An interrupt will be asserted (if enabled) if the number of available descriptor pointers for any of the 10 queues is less than this threshold.

8.10.5 Maximum Interrupt Rate Threshold (MIRT)

Offset: 0x18100020
Access: Read/Write
Reset: 0x0

This register is described in ms up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The maximum interrupt rate timer is started when either the TXINTM or RXIMTM status bits are set. TXMINTR or RXMINTR are asserted at this time. No future TXINTM or RXINTM events can cause the TXMINTR or TXMINTR to be asserted until this timer has expired. If both the TXINTM and RXINTM status bits are set while the timer is expired then the TXMINTR and RXMINTR will round robin between the two.

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	INTR_RATE_THRESH	Maximum interrupt rate threshold

8.10.6 Interrupt Global Enable (IER)

Offset: 0x18100024
Access: Read/Write
Reset: 0x0

Enables hardware signalling of interrupts.

Bit	Bit Name	Description
31:1	RES	Reserved
0	ENABLE	Writing a 0 enables hardware signaling of interrupts

8.10.7 Tx Interrupt Mitigation Thresholds (TIMT)

Offset: 0x18100028
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:16	TX_FIRST_ PKT_THRESH	Tx first packet threshold This register is in μs up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The Tx first packet timer starts counting after any Tx completion. If the timer is still counting when the next Tx completion occurs, it resets and starts over. The first Tx packet timer expires when either the last Tx packet threshold equals the last Tx packet timer count or the first Tx packet threshold equals the first Tx packet timer count.
15:0	TX_LAST_ PKT_THRESH	Tx last packet threshold This register is in μs up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The Tx last packet timer starts counting after any Tx completion. If the timer is still counting when the next Tx completion occurs, it resets and starts over. The last Tx packet timer expires when either the last Tx packet threshold equals the last Tx packet timer count or the first Tx packet threshold equals the first Tx packet timer count.

8.10.8 Rx Interrupt Mitigation Thresholds (RIMT)

Offset: 0x1810002C
Access: Read/Write
Reset: Undefined

This register is in ms up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The Rx last packet timer starts counting after any receive completion. If the timer is still counting when the next receive completion occurs, it resets and starts over. The last receive packet timer expires when either the last receive packet threshold equals the last receive packet timer count or the first receive packet threshold equals the first receive packet timer count.

Bit	Bit Name	Description
31:16	RX_FIRST_PKT_THRESH	Receive first packet threshold
15:0	RX_LAST_PKT_THRESH	Receive last packet threshold

8.10.9 Tx Configuration (TXCFG)

Offset: 0x18100030
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
31:18	RES	0x0	Reserved	
17	DIS_RETRY _UNDERRUN	0x1	Disable retry of underrun packets	
			0	Underrun packets will retry indefinitely
			1	Underrun packets will quit after first underrun attempt and write status indicating underrun

Bit	Bit Name	Reset	Description
16:15	RES	0x0	Reserved
14	RTCI_DIS	0x0	ReadyTime/CBR disable for QCUs 8-9. When the MAC is running at a clock rate ≤ 32 MHz, this bit must be set and only the ASAP frame scheduling policy may be selected for QCUs 8-9. QCUs 0-7 may continue to use any frame scheduling policy. Since in normal operation the MAC clock rate is at least 40 MHz, this is meant as a debugging mode only. Resets to 0x0.
		0	MAC clock rate at least 33 MHz; enable all frame scheduling policies for all QCUs.
		1	MAC clock rate is ≤ 32 MHz. Disable non-ASAP FSP for QCUs 8-9 so that CBR and ReadyTime logic will continue to operate correctly for QCUs 0-7.
13	RES	0x0	Reserved
12	ATIM_DEFER_DIS	0x0	Fragment burst vs. ATIM window defer disable. Note: PCU does not currently support ATIM
		0	In ad hoc mode only, if the ATIM window starts in the middle of a fragment burst, halt the burst and allow frames from other DCUs (e.g., DCUs generating beacon and CAB traffic) to proceed. Resume fragment burst after the ATIM window ends and after following normal DCF channel access procedures.
		1	Pause the fragment burst for the duration of the ATIM window, but do not allow frames from other DCUs to appear on the air; meant for debugging mode or if a problem is suspected with the fragment burst deferral logic.
11	BCN_PAST_ATIM_DIS	0x0	Ad hoc beacon ATIM window transmission policy. Note: PCU does not currently support ATIM.
		0	If the ATIM window ends before the station can send its beacon, the station cancels its beacon transmission.
		1	The station continues to attempt to send its beacon until it is able to do so, regardless of the status of the ATIM window.
10	RES	0x0	Reserved
9:4	TXCFG_TRIGLVL	0x1	Frame trigger level; Specifies the minimum number (in units of 64 bytes) to DMA into the PCU TXFIFO before the PCU initiates sending the frame on the air. Resets to 0x1 (meaning 64 Bytes or a full frame, whichever occurs first).
3	RES	0x0	Reserved
2:0	TXCFG_DMA_SIZE	0x5	Maximum DMA request size for master reads
		0	4 B
		1	8 B
		2	16 B
		3	32 B
		4	64 B
		5	128 B
		6	256 B
		7	Reserved

8.10.10 Rx Configuration (RXCFG)

Offset: 0x18100034
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:8	RES	0x0	Reserved
7	SLEEP_RX_ PEND_EN	0x0	Sleep entry policy when frames are pending in the PCU RX FIFO.
		0	The DMA receive logic requires all frames to be drained from the PCU RX FIFO before allowing the chip to sleep (the desired and default setting)
		1	The DMA receive logic will allow the chip to sleep even when frames are pending in the PCU Rx FIFO. This setting should not be needed in normal use and is meant primarily as a debugging mode or if a bug is suspected in the DMA tracking of the PCU RX FIFO frame count.
6	JUMBO_ WRAP_EN	0x0	Jumbo descriptor wrap mode.
		0	After reaching end of the jumbo descriptor's data buffer, go to next descriptor
		1	After reaching end of the jumbo descriptor's data buffer, retransfer into the same descriptor's data buffer again. This means the descriptor's data buffer will be overwritten with data from the PCU repeatedly in an infinite loop.
5	RES	0x0	Reserved
4:3	ZERO_LEN_ DMA_EN	0x0	Zero-length frame DMA enable
		0	Disable DMA of all zero-length frames. In this mode, the DMA logic suppresses all zero-length frames. Reception of zero-length frames is invisible to the host (they neither appear in host memory nor consume a Rx descriptor).
		1	Reserved
		2	Enable DMA of all zero-length frames. In this mode, all zero-length frames (chirps, double-chirps, and non-chirps) are DMAed into host memory just like normal (non-zero-length) frames.
		3	Reserved
2:0	DMA_SIZE	0x4	Maximum DMA size for master writes; (See the encodings for the register “Tx Configuration (TXCFG)” on page 189)

8.10.11 MIB Control (MIBC)

Offset: 0x18100040
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description
31:4	RES	0x0	Reserved
3	STROBE	0x0	MIB counter strobe. This bit is a one-shot and always reads as zero. For writes:
		0	No effect
		1	Causes every MIB counter to increment by one
2	CLEAR	0x1	Clear all counters
1	FREEZE	0x1	Freeze all counters
0	RES	0x0	Reserved

8.10.12 Data Buffer Length (DATABUF)

Offset: 0x18100060
Access: Read/Write
Reset: 0xFFF

Bit	Name	Description
31:12	RES	Reserved
11:0	BUF_LEN	Data buffer length; specifies the maximum size of the frame (4 KBytes) that can be written to this buffer (in bytes). The first 48 bytes of the 4 KBytes are for Rx status, the rest are for payload.

8.10.13 Global Tx Timeout (GTT)

Offset: 0x18100064
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:16	LIMIT	Timeout limit (in TU: 1024 μs); on reset, this value is set to 25 TU.
15:0	COUNT	Timeout counter (in TU: 1024 μs). The current value of the timeout counter that is reset on every transmit. If no Tx frame is queued up and ready to transmit, the timeout counter stays at 0 or else the counter increments every 1024 μs. If the timeout counter is equal to or greater than the timeout limit, the global transmit timeout interrupt is set in the ISR. This mechanism can be used to detect whether a Tx frame is ready and is unable to be transmitted.

8.10.14 Global Tx Timeout Mode (GTTM)

Offset: 0x18100068
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:5	RES	Reserved
4	DISABLE_QCU_FR_ ACTIVE_GTT	Before the GTT logic was using the PCI_TX_QCU_STATUS signal for GTT. It didn't seem to cover all the cases such as retry. If this bit is set then the original functionality will be enabled. If this bit is clear then QCU_FR_ACTIVE is used instead.
3	CST_USEC_STROBE	CST μs strobe; if this bit is set, then the CST timer will not use the TU based strobe but rather use the μs strobe to increment the timeout counter.
2	RESET_ON_CHAN_IDLE	Reset count on chan idle low. Reset count every time channel idle is low.
1	IGNORE_CHAN_IDLE	Ignore channel idle; if this bit is set then the GTT timer does not increment if the channel idle indicates the air is busy or NAV is still counting down.
0	USEC_STROBE	μs strobe; if this bit is set then the GTT timer will not use the TU based strobe but rather use a μs strobe to increment the timeout counter.

8.10.15 Carrier Sense Timeout (CST)

Offset: 0x1810006C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:16	LIMIT	Timeout limit (in TU: 1024 μs). On reset, this value is set to 0 TU.
15:0	COUNT	Timeout counter (in TU: 1024 μs). The current value of the timeout counter that is reset on every transmit. If no Tx frame is queued up and ready to transmit, the timeout counter stays at 0 or the counter increments every 1024 μs. If the timeout counter is equal to or greater than the timeout limit then carrier sense timeout (CST) interrupt is set in the ISR. This counter starts counting if any queues are ready for Tx. It continues counting when RX_CLEAR is low, which is useful to determine whether the transmit is stuck because RX_CLEAR is low for a long time.

8.10.16 Size of High and Low Priority (RXDP_SIZE)

Offset: 0x18100070
Access: Read-Only
Reset: 0x0Indicates the size of high and low priority RXDP FIFOs.

Bit	Bit Name	Description
31:12	RES	Reserved
12:8	HP	Indicates the size of high priority RXDP FIFO
7:0	LP	Indicates the size of low priority RXDP FIFO

8.10.17 MAC Rx High Priority Queue RXDP Pointer (RX_QUEUE_HP_RXDP)

Offset: 0x18100074
Access: Read/Write
Reset: 0x0

Lower 32 bits of the MAC Rx high priority queue RXDP pointer.

Bit	Bit Name	Description
31:0	ADDR	MAC Rx high priority queue RXDP pointer

8.10.18 MAC Rx Low Priority Queue RXDP Pointer (RX_QUEUE_LP_RXDP)

Offset: 0x18100078
Access: Read/Write
Reset: 0x0

Lower 32 bits of MAC Rx Low Priority Queue RXDP pointer.

Bit	Bit Name	Description
31:0	ADDR	MAC Rx low priority queue RXDP pointer for the lower 32 bits

8.10.19 Primary Interrupt Status (ISR_P)

Offset: 0x18100080
Access: Read/Write-One-to-Clear
Reset: 0x0

NOTE

- The bits that are logical ORs of bits in the secondary ISRs are generated by logically ORing the secondary ISR bits after the secondary ISR bits have been masked with the appropriate bits from the corresponding secondary interrupt mask register.
- A write of one to a bit that is a logical OR of bits in a secondary ISR clears the secondary ISR bits from which the primary ISR bit is generated. E.g.: A write of a one to TXOK (bit [6]) in ISR_P clears all 10 TXOK bits in ISR_S0 (bits [9:0] of Secondary Interrupt Status 0 (ISR_S0), page 8-195).
- Only the bits in this register (ISR_P) and the primary interrupt mask register (Primary Interrupt Mask (IMR_P), page 8-199) control whether the MAC's interrupt output is asserted. The bits in the several secondary interrupt status/mask registers control what bits are set in the primary interrupt status register; however, the IMR_S* registers do not determine whether an interrupt is asserted. That is, an interrupt is asserted only when the logical AND of ISR_P and IMR_P is non-zero. The secondary interrupt mask/status registers affect which bits are set in ISR_P, but do not directly affect whether an interrupt is asserted.

Bit	Bit Name	Description
31	RXINTM	Rx completion interrupt after mitigation; either the first Rx packet or last Rx packet interrupt mitigation count has reached its threshold (see the register "Rx Interrupt Mitigation Thresholds (RIMT)" on page 189)
30	TXINTM	Tx completion interrupt after mitigation; either the first Tx packet or last Tx packet interrupt mitigation count has reached its threshold (see the register "Tx Interrupt Mitigation Thresholds (TIMT)" on page 189)
29	RES	Reserved
28	GENTMR	Logical OR of all GENERIC TIMER bits in the secondary ISR 5 which include the GENERIC_TIMER_TRIGGER[7:0], GENERIC_TIMER_THRESH[7:0], GENERIC_TIMER_OVERFLOW
27	QTRIG	Logical OR of all QTRIG bits in secondary ISR 4; indicates that at least one QCU's frame scheduling trigger event has occurred
26	QCBRURN	Logical OR of all QCBRURN bits in secondary ISR 3; indicates that at least one QCU's frame scheduling trigger event occurred when no frames were present on the queue
25	QCBROVF	Logical OR of all QCBROVF bits in secondary ISR 3; indicates that at least one QCU's CBR expired counter has reached the value of the QCU's CBR_OVR_THRESH parameter (see CBR Configuration (Q_CBRCFG), page 8-207 register bits [31:24])
24	RXMINTR	RXMINTR maximum receive interrupt rate; same as RXINTM with the added requirement that maximum interrupt rate count has reached its threshold; this interrupt alternates with TXMINTR.
23	BCNMISC	Miscellaneous beacon-related interrupts This bit is the Logical OR of the CST, GTT, TIM, CABEND, DTIMSYNC, BCNTO, CABTO, TSFOOR, DTIM, and TBTT_TIME bits in secondary ISR 2.
22:21	RES	Reserved
20	BNR	Beacon not ready Indicates that the QCU marked as being used for beacons received a DMA beacon alert when the queue contained no frames.

Bit	Bit Name	Description
19	TXMINTR	TXMINTR maximum Tx interrupt rate
18	BMISS	The PCU indicates that is has not received a beacon during the previous *N* (*N* is programmable) beacon periods
17	BRSSI	The PCU indicates that the RSSI of a beacon it has received has fallen below a programmable threshold
16	SWBA	The PCU has signalled a software beacon alert
15	RXKCM	Key cache miss; a frame was received with a set key cache miss Rx status bit
14	RXPHY	The PHY signalled an error on a received frame
13	SWI	Software interrupt signalled; see the register “Command (CR)” on page 186
12	MIB	One of the MIB regs has reached its threshold
11	TXURN	Logical OR of all TXURN bits in secondary ISR 2. Indicates that the PCU reported a txfifo underrun for at least one QCU’s frame
10	TXEOL	Logical OR of all TXEOL bits in secondary ISR 1; indicates that at least one Tx desc fetch state machine has no more Tx descs available
9	RES	Reserved
8	TXERR	Logical OR of all TXERR bits in secondary ISR 1; indicates that at least one frame was completed with an error, regardless of whether the InterReq bit was set
7	RES	Reserved
6	TXOK	Logical OR of all TXOK bits in secondary ISR 0; indicates that at least one frame was completed with no errors and at the requested rate, regardless of whether the InterReq bit was set.
5	RXORN	RxFIFO overrrun
4	RXEOL	Rx descriptor fetch logic has no more Rx descs available
3	RXNOFR	No frame was received for RXNOFR timeout clocks
2	RXERR	The frame was received with errors
1	RXOK_LP	Low priority frame was received with no errors
0	RXOK_HP	High priority frame was received with no errors

8.10.20 Secondary Interrupt Status 0 (ISR_S0)

Offset: 0x18100084
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31:10	RES	Reserved
9	TXOK[9]	TXOK for QCU 9
...	...	...
1	TXOK[1]	TXOK for QCU 1
0	TXOK[0]	TXOK for QCU 0

8.10.21 Secondary Interrupt Status 1 (ISR_S1)

Offset: 0x18100088
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25	TXEOL[9]	TXEOL for QCU 9
...	...	...
17	TXEOL]1]	TXEOL for QCU 1
16	TXEOL[0]	TXEOL for QCU 0
15:10	RES	Reserved
9	TXERR[9]	TXERR for QCU 9
...	...	...
1	TXERR[1]	TXERR for QCU 1
0	TXERR[0]	TXERR for QCU 0

8.10.22 Secondary Interrupt Status 2 (ISR_S2)

Offset: 0x1810008C
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31	TBTT_TIME	TBTT-referenced timer interrupt; indicates the PCU's TBTT-referenced timer has elapsed.
30	TSFOOR	TSF out of range; indicates that the corrected TSF received from a beacon differs from the PCU's internal TSF by more than a (programmable) threshold
29	DTIM	A beacon was received with the DTIM bit set and a DTIM count value of zero. Beacons with a set DTIM bit but a non-zero DTIM count do not generate it.
28	CABTO	CAB timeout; a beacon was received that indicated that the STA should expect to receive CAB traffic. However, the PCU's CAB timeout expired either because the STA received no CAB traffic, or because the STA received some CAB traffic but never received a CAB frame with the more data bit clear in the frame control field (which would indicate the final CAB frame).
27	BCNTO	Beacon timeout; a TBTT occurred and the STA began waiting to receive a beacon, but no beacon was received before the PCU's beacon timeout expired
26	DTIMSYNC	DTIM synchronization lost; a beacon was received that was expected to be a DTIM but was not, or a beacon was received that was not expected to be a DTIM but was
25	CABEND	End of CAB traffic; a CAB frame was received with the more data bit clear in the frame control field
24	TIM	A beacon was received with the local STA's bit set in the TIM element
23	GTT	Global Tx timeout; indicates the GTT count ≥ than the GTT limit
22	CST	Carrier sense timeout; indicates the CST count ≥ than the CST limit
21:10	RES	Reserved
9	TXURN[9]	TXURN for QCU 9
...	...	...
1	TXURN[1]	TXURN for QCU 1
0	TXURN[0]	TXURN for QCU 0

8.10.23 Secondary Interrupt Status 3 (ISR_S3)

Offset: 0x18100090
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25	QCBRURN[9]	QCBRURN for QCU 9
...	...	...
17	QCBRURN[1]	QCBRURN for QCU 1
16	QCBRURN[0]	QCBRURN for QCU 0
15:10	RES	Reserved
9	QCBROVF[9]	QCBROVF for QCU 9
1	QCBROVF[1]	QCBROVF for QCU 1
...	...	...
0	QCBROVF[0]	QCBROVF for QCU 0

8.10.24 Secondary Interrupt Status 4 (ISR_S4)

Offset: 0x18100094
Access: Read/Write-One-to-Clear
Reset: 0x0

Bit	Bit Name	Description
31:10	RES	Reserved
9	QTRIG[9]	QTRIG for QCU 9
...	...	...
1	QTRIG[1]	QTRIG for QCU 1
0	QTRIG[0]	QTRIG for QCU 0

8.10.25 Secondary Interrupt Status 5 (ISR_S5)

Offset: 0x18100098
Access: Read/Write-One-to-Clear
Reset: 0x0

NOTE The trigger indicates that the TSF matched or exceeded the timer. The threshold is set when the TSF exceeds the timer by the GENERIC_TIMER_THRESH value. The GENERIC_TIMER overflow occurs when the TSF exceeds the timer by such a large amount that TSF ≥ Timer + Period, indicating incorrect software programming. The GENERIC_TIMER 0 threshold was removed because timer 0 is special and does not generate threshold event.

Bit	Bit Name	Description
31	GENERIC_TIMER[15]	GENERIC_TIMER 15 threshold
...	...	...
17	GENERIC_TIMER[11]	GENERIC_TIMER 1 threshold
16	GENERIC_TIMER_OVERFLOW	GENERIC_TIMER overflow
15	GENERIC_TIMER_TRIGGER[15]	GENERIC_TIMER 15 trigger
...	...	...
1	GENERIC_TIMER_TRIGGER[1]	GENERIC_TIMER 1 trigger
0	GENERIC_TIMER_TRIGGER[0]	GENERIC_TIMER 0 trigger

8.10.26 Primary Interrupt Mask (IMR_P)

Offset: 0x181000A0
Access: Read/Write
Reset: 0x0

NOTE Only the bits in this register control whether the MAC's interrupt outputs are asserted. The bits in the secondary interrupt mask registers control what bits are set in the Primary Interrupt Mask (IMR_P), page 8-199 register; however, the IMR_S* registers do not determine whether an interrupt is asserted.

Bit	Bit Name	Description
31	RXINTM	RXINTM interrupt enable
30	TXINTM	TXINTM interrupt enable
29	RES	Reserved
28	GENTMR	GENTMR interrupt enable
27	QTRIG	QTRIG interrupt enable
26	QCBRURN	QCBRURN interrupt enable
25	QCBROVF	QCBROVF interrupt enable
24	RXMINTR	RXMINTR interrupt enable
23	BCNMISC	BCNMISC interrupt enable
22:21	RES	Reserved
20	BNR	BNR interrupt enable
19	TXMINTR	TXMINTR interrupt enable
18	BMISS	BMISS interrupt enable
17	BRSSI	BRSSI interrupt enable
16	SWBA	SWBA interrupt enable
15	RXKCM	RXKCM interrupt enable
14	RXPHY	RXPHY interrupt enable
13	SWI	SWI interrupt enable
12	MIB	MIB interrupt enable
11	TXURN	TXURN interrupt enable
10	TXEOL	TXEOL interrupt enable
9	TXNOFR	TXNOFR interrupt enable
8	TXERR	TXERR interrupt enable
7	RES	Reserved
6	TXOK	TXOK interrupt enable
5	RXORN	RXORN interrupt enable
4	RXEOL	RXEOL interrupt enable
3	RXNOFR	RXNOFR interrupt enable
2	RXERR	RXERR interrupt enable
1	RXOK_LP	RXOK_LP interrupt enable
0	RXOK_HP	RXOK_HP interrupt enable

8.10.27 Secondary Interrupt Mask 0 (IMR_S0)

Offset: 0x181000A4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:10	RES	Reserved
9	TXOK[9]	TXOK for QCU 9 interrupt enable
...	...	...
1	TXOK[1]	TXOK for QCU 1 interrupt enable
0	TXOK[0]	TXOK for QCU 0 interrupt enable

8.10.28 Secondary Interrupt Mask 1 (IMR_S1)

Offset: 0x181000A8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25	TXEOL[9]	TXEOL for QCU 9 interrupt enable
...	...	...
17	TXEOL[1]	TXEOL for QCU 1 interrupt enable
16	TXEOL[0]	TXEOL for QCU 0 interrupt enable
15:10	RES	Reserved
9	TXERR[9]	TXERR for QCU 9 interrupt enable
...	...	...
1	TXERR[1]	TXERR for QCU 1 interrupt enable
0	TXERR[0]	TXERR for QCU 0 interrupt enable

8.10.29 Secondary Interrupt Mask 2 (IMR_S2)

Offset: 0x181000AC
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31	TBTT_TIME	TBTT_TIME interrupt enable
30	TSFOOR	TSFOOR interrupt enable
29	DTIM	DTIM interrupt enable
28	CABTO	CABTO interrupt enable
27	BCNTO	BCNTO interrupt enable
26	DTIMSYNC	DTIMSYNC interrupt enable
25	CABEND	CABEND interrupt enable
24	TIM	TIM interrupt enable
23	GTT	GTT interrupt enable
22	CST	CST interrupt enable
21:10	RES	Reserved
9	TXURN[9]	TXURN for QCU 9 interrupt enable
...	...	...
1	TXURN[1]	TXURN for QCU 1 interrupt enable
0	TXURN[0]	TXURN for QCU 0 interrupt enable

8.10.30 Secondary Interrupt Mask 3 (IMR_S3)

Offset: 0x181000B0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25	QCBRURN[9]	QCBRURN for QCU 9 interrupt enable
...	...	...
17	QCBRURN[1]	QCBRURN for QCU 1 interrupt enable
16	QCBRURN[0]	QCBRURN for QCU 0 interrupt enable
15:10	RES	Reserved
9	QCBROVF[9]	QCBROVF for QCU 9 interrupt enable
...	...	...
1	QCBROVF[1]	QCBROVF for QCU 1 interrupt enable
0	QCBROVF[0]	QCBROVF for QCU 0 interrupt enable

8.10.31 Secondary Interrupt Mask 4 (IMR_S4)

Offset: 0x181000B4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:10	RES	Reserved
9	QTRIG[9]	QTRIG for QCU 9 interrupt enable
...	...	...
1	QTRIG[1]	QTRIG for QCU 1 interrupt enable
0	QTRIG[0]	QTRIG for QCU 0 interrupt enable

8.10.32 Secondary Interrupt Mask 5 (IMR_S5)

Offset: 0x181000B8
Access: Read/Write-One-to-Clear
Reset: 0x0

NOTE The trigger indicates the TSF matched or exceeded the timer; threshold is set when the TSF exceeds the timer by the GENERIC_TIMER_THRESH value. The GENERIC_TIMER overflow occurs when the TSF exceeds the timer by such a large amount that TSF ≥ Timer + Period, indicating incorrect software programming. The threshold GENERIC_TIMER 0 was removed because timer 0 is special and does not generate a threshold event.

Bit	Bit Name	Description
31	GENERIC_TIMER_THRESHOLD[15]	GENERIC_TIMER_THRESHOLD 15
30	GENERIC_TIMER_THRESHOLD[14]	GENERIC_TIMER_THRESHOLD 14
...	...	...
18	GENERIC_TIMER_THRESHOLD[2]	GENERIC_TIMER_THRESHOLD 2
17	GENERIC_TIMER_THRESHOLD[1]	GENERIC_TIMER_THRESHOLD 1
16	GENERIC_TIMER_OVERFLOW	GENERIC_TIMER overflow enable
15	GENERIC_TIMER_TRIGGER[15]	GENERIC_TIMER 15 trigger enable
...	...	...
1	GENERIC_TIMER_TRIGGER[1]	GENERIC_TIMER 1 trigger enable
0	GENERIC_TIMER_TRIGGER[0]	GENERIC_TIMER 0 trigger enable

8.10.33 Primary Interrupt Status Read and Clear (ISR_P_RAC)

Offset: 0x181000C0
Access: Read-and-Clear (No Write Access)
Reset: 0x0

NOTE A read from this location atomically:

- Copies all secondary ISRs into the corresponding secondary ISR shadow registers (ISR_S0 is copied to ISR_S0_S, etc.)
- Clears all bits of the primary ISR (ISR_P) and all bits of all secondary ISRs (ISR_S0–ISR_S4)
- Returns the contents of the primary ISR (ISR_P)

Bit	Bit Name	Description
31:0	ISR_P	Same format as Primary Interrupt Status (ISR_P)

8.10.34 Secondary Interrupt Status 0 (ISR_S0_S)

Offset: 0x181000C4
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 0 (ISR_S0)

8.10.35 Secondary Interrupt Status 1 (ISR_S1_S)

Offset: 0x181000C8
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 1 (ISR_S1)

8.10.36 Secondary Interrupt Status 2 (ISR_S2_S)

Offset: 0x181000D0
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 2 (ISR_S2)

8.10.37 Secondary Interrupt Status 3 (ISR_S3_S)

Offset: 0x181000D4
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 3 (ISR_S3)

8.10.38 Secondary Interrupt Status 4 (ISR_S4_S)

Offset: 0x181000D8
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 4 (ISR_S4)

8.10.39 Secondary Interrupt Status 5 (ISR_S5_S)

Offset: 0x181000DC
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:0	ISR_S0	Same format as Secondary Interrupt Status 5 (ISR_S5)

8.11 WLAN MAC Queue Control Unit Registers

The WLAN MAC Queue Control Unit registers occupy the offset range 0x18100800-0x18100A40 in the QCA9563 address space. The QCA9563 has ten QCUs, numbered from 0 to 9.

Table 8-12 WLAN MAC Queue Control Unit Registers

Offset	Name	Description	Page
0x18100800 + (Q << 2)[1]	Q_TXDP	Tx Queue Descriptor Pointer	page 205
0x18100830	Q_STATUS_RING_START	QCU_STATUS_RING_START_ ADDRESS Lower 32 bits of Address	page 206
0x18100834	Q_STATUS_RING_END	QCU_STATUS_RING_END_ADDR Lower 32 Bits of Address	page 206
0x18100838	Q_STATUS_RING_CURRENT	QCU_STATUS_RING_CURRENT Address	page 206
0x18100840	Q_TXE	Tx Queue Enable	page 206
0x18100880	Q_TXD	Tx Queue Disable	page 207
0x181008C0 + (Q << 2)[1]	Q_CBRCFG	CBR Configuration	page 207
0x18100900 + (Q << 2)[1]	Q_RDYTIMECFG	ReadyTime Configuration	page 207
0x18100940	Q_ONESHOTARM_SC	OneShotArm Set Control	page 208
0x18100980	Q_ONESHOTARM_CC	OneShotArm Clear Control	page 208
0x181009C0 + (Q << 2)[1]	Q_MISC	Miscellaneous QCU Settings	page 209
0x18100A00 + (Q << 2)[1]	Q_STS	Miscellaneous QCU Status	page 210
0x18100A40	Q_RDYTIMESHDN	ReadyTimeShutdown Status	page 211
0x18100A44	Q_MAC_QCU_DESC_CRC_ CHK	Descriptor CRC Check	page 211

1. The variable Q in the register addresses refers to the QCU number.

8.11.1 Tx Queue Descriptor (Q_TXDP)

Offset: 0x18100800 + (*Q* < 2)
Access: Read/Write
Cold Reset: Undefined
Warm Reset: Unaffected

Bit	Bit Name	Description
31:2	TXDP	Tx descriptor pointer
1:0	RES	Reserved

8.11.2 QCU_STATUS_RING_START_ADDRESS Lower 32 bits of Address (Q_STATUS_RING_START)

Offset: 0x18100830
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	ADDR	Lower 32 bits of QCU_STATUS_RING_START_ADDR

8.11.3 QCU_STATUS_RING_END_ADDR Lower 32 Bits of Address (Q_STATUS_RING_END)

Offset: 0x18100834
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	ADDR	Lower 32 bits of QCU_STATUS_RING_END_ADDR

8.11.4 QCU_STATUS_RING_CURRENT Address (Q_STATUS_RING_CURRENT)

Offset: 0x18100838
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	ADDR	MAC_QCU_STATUS_RING_CURRENT_ADDRESS

8.11.5 Tx Queue Enable (Q_TXE)

Offset: 0x18100840
Access: Read/Write
Reset: 0x0

NOTE Writing a 1 in bit position *N* sets the TXE bit for QCU *N*. Writing a 0 in bit position *N* has no effect; in particular, it does not clear the TXE bit for the QCU.

Bit	Bit Name	Description
31:10	RES	Reserved
9	QCU_EN[9]	Enable QCU 9
...	...	...
1	QCU_EN[1]	Enable QCU 1
0	QCU_EN[0]	Enable QCU 0

8.11.6 Tx Queue Disable (Q_TXD)

Offset: 0x18100880
Access: Read/Write
Reset: 0x0

NOTE To stop transmission for QCU *Q*:

1. Write a 1 to QCU Q's TXD bit
2. Poll the Tx Queue Enable (Q_TXE), page 8-206 register until QCU *Q*'s TXE bit is clear
3. Poll QCU *Q*'s Misc. QCU Status (Q_STS), page 8-210 register until its pending frame count (Q_STS bits [1:0]) is zero
4. Write a 0 to QCU *Q*'s TXD bit

NOTE At this point, QCU *Q* has shut down and has no frames pending in its associated DCU.

NOTE Software must not write a 1 to a QCU's TXE bit when that QCU's TXD bit is set; an undefined operation will result. Software must ensure that it sets a QCU's TXE bit only when the QCU's TXD bit is clear. It is fine to write a 0 to TXE when TXD is set, but this has no effect on the QCU.

Bit	Bit Name	Description
31:10	RES	Reserved
9	QCU_DIS[9]	Disable QCU 9
...	...	...
1	QCU_DIS[1]	Disable QCU 1
0	QCU_DIS[0]	Disable QCU 0

8.11.7 CBR Configuration (Q_CBRCFG)

Offset: 0x181008C0 + (*Q* < 2)
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:24	CBR_OVF_THRESH	CBR overflow threshold
23:0	CBR_INTV	CBR interval in μs

8.11.8 ReadyTime Configuration (Q_RDYTIMECFG)

Offset: 0x18100900 + (*Q* < 2)
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:25	RES	Reserved	
24	RDYTIME_EN	ReadyTime enable	
		0	Disable ReadyTime use
		1	Enable ReadyTime use
23:0	RDYTIME_DUR	ReadyTime duration in μs	

8.11.9 OneShotArm Set Control (Q_ONESHOTARM_SC)

Offset: 0x18100940
Access: Read/Write
Reset: 0x0

NOTE A read to this register returns the current state of all OneShotArm bits (QCU *Q*'s OneShotArm bit is returned in bit position *Q*).

Bit	Bit Name	Description	
31:10	RES	Reserved	
9	ONESHOTARM[9]	0	No effect
		1	Set OneShot arm bit for QCU 9
...	...	...	
1	ONESHOTARM[1]	0	No effect
		1	Set OneShot arm bit for QCU 1
0	ONESHOTARM[0]	0	No effect
		1	Set OneShot arm bit for QCU 0

8.11.10 OneShotArm Clear Control (Q_ONESHOTARM_CC)

Offset: 0x18100980
Access: Read/Write
Reset: 0x0

NOTE A read to this register returns the current state of all OneShotArm bits (QCU *Q*'s OneShotArm bit is returned in bit position *Q*).

Bit	Bit Name	Description	
31:10	RES	Reserved	
9	ONESHOT_CLEAR[9]	0	No effect
		1	Clear OneShot arm bit for QCU 9
...	...	...	
1	ONESHOT_CLEAR[1]	0	No effect
		1	Clear OneShot arm bit for QCU 1
0	ONESHOT_CLEAR[0]	0	No effect
		1	Clear OneShot arm bit for QCU 0

8.11.11 Misc. QCU Settings (Q_MISC)

Offset: 0x181009C0 + (*Q* < 2)
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
31:12	RES	0x0	Reserved	
11	QCU_FR_ABORT_REQ_EN	0x1	DCU frame early termination request control	
			0	Never request early frame termination. Once a frame enters the DCU, it will remain active until its normal retry count has been reached or the frame succeeds.
			1	Allow this QCU to request early frame termination. When requested, the DCU attempts to complete processing the frame more quickly than it normally would.
10	CBR_EXP_CNT_CLR_EN	0x0	CBR expired counter force-clear control. Write-only (always reads as zero). Write of:	
			0	No effect
			1	Resets the CBR expired counter to zero
9	TXE_CLR_ON_CBR_END	0x0	ReadyTime expiration and VEOL handling policy	
			0	On expiration of ReadyTime or on VEOL, the TXE bit is not cleared. Only reaching the physical end-of-queue (that is, a NULL LinkPtr) will clear TXE
			1	The TXE bit is cleared on expiration of ReadyTime, on VEOL, and on reaching the physical end-of-queue
8	CBR_EXP_INC_LIMIT	0x0	CBR expired counter limit enable	
			0	The maximum CBR expired counter value is 255, but a CBROVF interrupt is generated when the counter reaches the value set in the CBR overflow threshold field of the CBR Configuration (Q_CBRCFG) register.
			1	The maximum CBR expired counter is limited to the value of the CBR overflow threshold field of the CBR Configuration (Q_CBRCFG) register. Note that in addition to limiting the maximum CBR expired counter to this value, a CBROVF interrupt is also generated when the CBR expired counter reaches the CBR overflow threshold.
7	QCU_IS_BCN	0x0	Beacon use indication. Indicates whether the QCU is being used for beacons	
			0	QCU is being used for non-beacon frames only
			1	QCU is being used for beacon frames (and possibly for non-beacon frames)
6	CBR_EXP_INC_DIS_NOBCNFR	0x0	Disable the CBR expired counter increment if the frame scheduling trigger occurs and the QCU marked as being used for beacon transmission (i.e., the QCU that has bit [7] set in its Misc. QCU Settings (Q_MISC) register) contains no frames	
			0	Increment the CBR expired counter each time the frame scheduling trigger occurs, regardless of whether the beacon queue contains frames
			1	Increment the CBR expired counter only when both the frame scheduling trigger occurs and the beacon queue is valid (the beacon queue is valid whenever its TXE is asserted)
5	CBR_EXP_INC_DIS_NOFR	0x0	Disable the CBR expired counter increment if the frame scheduling trigger occurs and the queue contains no frames	
			0	Increment the CBR expired counter each time the frame scheduling trigger occurs, regardless of whether the queue contains frames
			1	Increment the CBR expired counter only when both the frame scheduling trigger occurs and the queue is valid (the queue is valid whenever TXE is asserted)

Bit	Bit Name	Reset	Description	
4	ONESHOT_EN	0x0	OneShot enable	
			0	Disable OneShot function
			1	Enable OneShot function - Note that OneShot must not be enabled when the QCU is set to an ASAP frame scheduling policy.
3:0	FSP	0x0	Frame scheduling policy setting	
			0	ASAP- The QCU is enabled continuously.
			1	CBR - The QCU is enabled under control of the settings in the CBR Configuration (Q_CBRCFG) register.
			2	DBA-gated; the QCU is enabled at each occurrence of a DMA beacon alert.
			3	TIM-gated - The QCU will be enabled whenever: ■ In STA mode, the PCU indicates that a beacon frame has been received with the local STA's bit set in the TIM element ■ In IBSS mode, the PCU indicates that an ATIM frame has been received
			4	Beacon-sent-gated - The QCU will be enabled when the DCU that is marked as being used for beacon transmission (see bit [16] of the Misc. DCU-Specific Settings (D_MISC) register) indicates that it has sent the beacon frame on the air
			5	Beacon-received-gated - The QCU will be enabled when the PCU indicates that it has received a beacon.
			6	HCF Poll gated - The QCU will be enabled whenever the Rx HCF poll event occurs; the signals come from the PCU when a directed HCF poll frame type is received with valid FCS.
			15:7	Reserved

8.11.12 Misc. QCU Status (Q_STS)

Offset: 0x18100A00 + ($Q < 2$)
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
31:16	RES	Reserved
15:8	CBR_EXP	Current value of the CBR expired counter
7:2	RES	Reserved
1:0	FC	Pending frame count; Indicates the number of frames this QCU presently has pending in its associated DCU.

8.11.13 ReadyTimeShutdown Status (Q_RDYTIMESHDN)

Offset: 0x18100A40
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:10	RES	Reserved	
9	READYTIME_SHUTDOWN[9]	ReadyTimeShutdown status for QCU 9	
...	...	...	
1	READYTIME_SHUTDOWN[1]	ReadyTimeShutdown status for QCU 1	
0	READYTIME_SHUTDOWN[0]	ReadyTimeShutdown status for QCU 0 On read, returns ReadyTimeShutdown indication. Write of:	
		0	No effect
		1	Set OneShot arm bit for QCU 0

8.11.14 Descriptor CRC Check (MAC_QCU_DESC_CRC_CHK)

Offset: 0x18100A44
Access: Read/Write
Reset: 0x1

Bit	Bit Name	Description	
31:1	RES	Reserved	
0	EN	QCU frame descriptor CRC check	
		0	Disable CRC check on the descriptor fetched from HOST
		1	Enable CRC check on the descriptor fetched from HOST

8.12 MAC Control Data Unit Registers

The MAC Control Data Unit registers occupy the offset range 0x18101000-0x181012F0 in the QCA9563 address space. The QCA9563 has ten DCUs, numbered from 0 to 9.

Table 8-13 MAC Control Data Unit Registers

Offset	Name	Description	Page
0x18101000 + (*D* << 2)[1]	D_QCUMASK	QCU Mask	page 212
0x18101030	D_GBL_IFS_SIFS	DCU-Global SIFS	page 213
0x18101040 + (*D* << 2)[1]	D_LCL_IFS	DCU-Specific IFS Settings	page 213
0x18101070	D_GBL_IFS_SLOT	DCU-Global IFS Settings: Slot Duration	page 213
0x18101080 + (*D* << 2)[1]	D_RETRY_LIMIT	Retry Limits	page 214
0x181010B0	D_GBL_IFS_EIFS	DCU-Global IFS Settings: EIFS Duration	page 214
0x181010C0 + (*D* << 2)[1]	D_CHNTIME	ChannelTime Settings	page 214
0x181010F0	D_GBL_IFS_MISC	QCU Global IFS Miscellaneous	page 215
0x18101100 + (*D* << 2)[1]	D_MISC	Miscellaneous DCU-Specific Settings	page 216
0x18101140	D_SEQ	DCU Sequence	page 218
0x18101270	D_PAUSE	DCU Pause	page 219
0x181012F0	D_TXSLOTMASK	DCU Transmission Slot Mask	page 219
0x18101F00	SLEEP_STATUS	MAC Sleep Status	page 220
0x18101F04	LED_CONFIG	MAC LED Configuration	page 220

1. The variable *D* in the register addresses refers to the DCU number.

8.12.1 QCU Mask (D_QCUMASK)

Offset: 0x18101000 + (*D* < 2)
Access: Read/Write
Cold Reset: 0x0
Warm Reset: Unaffected

NOTE To achieve lowest power consumption, software should set this register to 0x0 for all DCUs that are not in use. The hardware detects that the QCU mask is set to zero and shuts down certain logic in response, helping to save power.

Bit	Bit Name	Description
31:10	RES	Reserved
9:0	QCU_MASK	Setting bit *Q* means that QCU *Q* is associated with (i.e., feeds into) this DCU. These register have reset values which corresponding to a 1 to 1 mapping between QCUs and DCUs. A register offset of 0x1000 maps to 0x1, 0x1004 maps to 0x2, 0x1008 maps to 0x4, etc.

8.12.2 DCU-Global SIFS (D_GBL_IFS_SIFS)

Offset: 0x18101030
Access: Read/Write
Reset: 0x640

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	DURATION	SIFS duration in core clocks (40 MHz in non turbo mode, 80 MHz in turbo mode

8.12.3 DCU-Specific IFS Settings (D_LCL_IFS)

Offset: 0x18101040 + (*D* < 2)
Access: Read/Write
Cold Reset: See field description
Warm Reset: Unaffected

Bit	Bit Name	Reset	Description
When Long AIFS is 0:			
31:28	RES	0x0	Reserved
27:20	DATA_AIFS_D[7:0]	0x2	AIFS value, in slots beyond SIFS; e.g., a setting of 2 (the reset value) means AIFS is equal to DIFS. **NOTE** This field is 17 bits wide (including the 9 MSBs accessed using the AIFS field), but the maximum supported AIFS value is 0x1FFFC. Setting AIFS to 0x1FFFD, 0x1FFFE, or 0x1FFFF causes the DCU to hang.
19:10	DATA_CW_MAX	0x3FF	CW_MAX value; must be equal to a power of 2, minus 1
9:0	DATA_CW_MIN	0xF	CW_MIN value; must be equal to a power of 2, minus 1
When Long AIFS is 1:			
31:29	RES	0x0	Reserved
28	LONG_AIFS [DCU_IDX_D]	0x0	Long AIFS bit; used to read or write to the nine MSBs of the AIFS value
27:9	RES	0x0	Reserved
8:0	DATA_AIFS_D[16:8]	0x2	Upper nine bits of the AIFS value (see bits [27:20] listed in this register)

8.12.4 QCU Global IFS Slots (D_GBL_IFS_SLOT)

Offset: 0x18101070
Access: Read/Write
Reset: 0x360

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	DURATION	Slot duration in core clocks (40 MHz in non turbo mode, 80 MHz in turbo mode)

8.12.5 Retry Limits (D_RETRY_LIMIT)

Offset: 0x18101080 + (*D* < 2)
Access: Read/Write
Cold Reset: See field description
Warm Reset: Unaffected

Bit	Bit Name	Reset	Description
31:20	RES	0x20	Reserved
19:14	SDFL	0x20	STA data failure limit: Specifies the number of times a frame's data exchange may fail before CW is reset to CW_MIN. Note: A value of 0x0 is unsupported.
13:8	SRFL	0x20	STA RTS failure limit: Specifies the number of times a frame's RTS exchange may fail before the CW is reset to CW_MIN. Note: A value of 0x0 is unsupported.
7:4	RES	0x0	Reserved
3:0	FRFL	0x4	Frame RTS failure limit: Specifies the number of times a frame's RTS exchange may fail before the current transmission series is terminated. A frame's RTS exchange fails if RTS is enabled for the frame, but when the MAC sends the RTS on the air, no CTS is received. Note: A value of 0x0 is unsupported.

8.12.6 QCU Global IFS EIFS (D_GBL_IFS_EIFS)

Offset: 0x18101070
Access: Read/Write
Reset: 0x3480

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	DURATION	EIFS duration in core clocks (40 MHz in non turbo mode, 80 MHz in turbo mode)

8.12.7 ChannelTime Settings (D_CHNTIME)

Offset: 0x181010C0 + (*D* < 2)
Access: Read/Write
Cold Reset: 0x0
Warm Reset: Unaffected

Bit	Bit Name	Description
31:21	RES	Reserved
20	CHANNEL_TIME_EN	ChannelTime enable
19:0	DATA_CT_MMR	ChannelTime duration in μs

8.12.8 QCU Global IFS Miscellaneous (D_GBL_IFS_MISC)

Offset: 0x181010F0
Access: Read/Write
Reset: See field description

Determines which slice of the internal LFSR will be used to generate the random sequence used to determine backoff counts in the DCUs and scrambler seeds in the PCU. The intent is to have different stations have different LFSR slice values (perhaps by using some bits from the MAC address) to minimize the random sequence correlations among stations in the same BSS IBSS.

NOTE This field affects the MAC only when LFSR_SLICE_RANDOM_DIS (bit [24] of this register) is set. When random LFSR slice selection is enabled (default), it is ignored.

Bit	Bit Name	Reset	Description
31:30	RES	0x0	Reserved
29	SLOT_COUNT_ RST_UNCOND	0x0	Slot count reset policy. If set, slot count gets reset as soon as channel gets busy. If clear, slot count gets reset only after transmitting or receiving frame. Setting this bit will be helpful if performance is degraded by spur.
28	IGNORE_ BACKOFF	0x0	Ignore Back Off. Setting this bit will allow the DCU to ignore any backoff as well as EIFS. This should be set during fast channel change to guarantee low latency to flush the transmit pipe.
27	CHAN_SLOT_ ALWAYS	0x0	Force transmission always on slot boundaries. When bits [26:25] of this register are non-zero, the MAC will transmit on slot boundaries when the 802.11 spec requires it to do so. When bits [26:25] are not equal to 0x0 and this bit is non-zero, then the MAC will attempt to transmit on slot boundaries all the time, not just when the spec requires. This mainly affects the case in which a frame becomes available when the channel has been idle for an AIFS. If this bit is clear in this case, then the MAC will transmit immediately. If this bit is set, then the MAC will wait for the next slot boundary before transmitting. Note that the setting of this bit has no effect unless bits [26:25] are non-zero.
26:25	CHAN_SLOT_ WIN_DUR	0x0	Slot transmission window length. Under certain corner cases (most related to very slow PCI DMA), the MAC could send a frame not on a slot boundary, thus deslotting the network. The value in this field specifies the number of core clocks after a slot boundary during which the MAC is permitted to send a frame. Specified in units of 8 core clocks; if set to 0x0 (the reset value), the MAC is permitted to send at any point in the slot.
24	LFSR_SLICE_ RANDOM_DIS	0x0	Random LFSR slice selection disable. 0 Allow the IFS logic to randomly generate the LFSR slice select value (see bits [2:0] of this register). The random selection method is meant to ensure independence of the LFSR output values both for nodes on different PCI busses but on the same network as well as for multiple nodes connected to the same physical PCI bus. 1 Disable random LFSR slice selection. Instead, the value programmed into LFSR_SLICE_SEL (bits [2:0] of this register) will be used.
23:10	RES	0x0	Reserved
9:4	SIFS_DUR_ USEC	0x10	SIFS duration in Microseconds

Bit	Bit Name	Reset	Description
3	TURBO_MODE	0x0	Turbo mode indication. Software is required to keep this register consistent with the turbo non-turbo state of the overall system. In other words, this IS NOT a status bit generated by the MAC. Rather it is a control bit that must be maintained by software so that certain parts of the MAC that are sensitive to whether the system is in turbo mode will operate correctly.
			0 Station is operating in non-turbo mode
			1 Station is operating in turbo mode
2:0	LFSR_SLICE_SEL	0x0	LFSR slice select. Determines which slice of the internal LFSR generates the random sequence used to determine backoff counts in the DCUs and scrambler seeds in the PCU. The intent is to have different stations have different LFSR slice values (perhaps by using some bits from the MAC address) to minimize the random sequence correlations among stations in the same BSS IBSS. **NOTE** This field affects the MAC only when LFSR_SLICE_RANDOM_DIS (bit [24] of this register) is set. When random LFSR slice selection is enabled (the default), this field is ignored.

8.12.9 Misc. DCU-Specific Settings (D_MISC)

Offset: 0x18101100 + ($D < 2$)
Access: Read/Write
Cold Reset: See field description
Warm Reset: Unaffected

Bit	Bit Name	Reset	Description
31:25	RES	0x0	Reserved
24	SIFS_BURST_CHAN_BUSY_IGNORE	0x1	SIFS burst medium sense policy.
			0 MAC obeys medium busy during SIFS burst
			1 MAC ignore medium busy during SIFS burst
23	RETRY_ON_BLOWN_IFS_EN	0x0	Blown IFS handling policy. This setting controls how the DCU handles the case in which the DMA of a frame takes so long that the IFS spacing is met before the frame trigger level is reached.
			0 Send the frame on the air anyway (ignore the IFS violation); causes the frame to be sent on the air at a time that is later than called for in the 802.11 spec
			1 Do not send the frame on the air. Instead, act as if the frame had been sent on the air but failed and initiate the retry procedure. A retry will be charged against the frame. If more retries are permitted, the frame will be retried. If the retry limit has been reached, the frame will fail.
22	VIRT_COLL_CW_INC_EN	0x0	Post-frame backoff disable.
			0 DCU performs a backoff after each frame finishes, as required by the 802.11 spec
			1 DCU skips the post-frame backoff (or, equivalently, acts as if it always selects a post-frame backoff count of zero)
21	POST_BKOFF_SKIP	0x0	Post-frame backoff disable.
			0 DCU performs a backoff after each frame finishes, as required by the 802.11 spec
			1 DCU skips the post-frame backoff (or, equivalently, acts as if it always selects a post-frame backoff count of zero)

Bit	Bit Name	Reset	Description	
20	SEQNUM_ FREEZE	0x0	Sequence number increment disable.	
			0	Allow the DCU to use a normal sequence number progression (the DCU increments the sequence number for each new frame)
			1	Force the sequence number to be frozen at its current value
19	LOCKOUT_ IGNORE	0x0	DCU arbiter lockout ignore control.	
			0	Obey DCU arbiter lockouts from higher-priority DCUs
			1	Ignore DCU arbiter lockouts from higher-priority DCUs (that is, allow the current DCU to arbitrate for access to the PCU even if one or more higher-priority DCUs is asserting a DCU arbiter lockout)
18	LOCKOUT_ GBL_EN	0x0	DCU arbiter lockout control	
			0	No lockout. Allows lower-priority DCUs to arbitrate for access to the PCU concurrently with this DCU.
			1	Intra-frame lockout only. Forces all lower-priority DCUs to defer arbitrating for access to the PCU while the current DCU arbitrates for access to the PCU or doing an intra-frame backoff.
			2	Global lockout. Forces all lower-priority DCUs to defer arbitration for access to the PCU when: ■ At least one QCU feeding to the current DCU has a frame ready ■ The DCU is actively processing a frame, including arbitrating for PCU access, performing intra- or post-frame backoff, DMAing frame data to the PCU, or waiting for the PCU to complete the frame.
			3	Reserved
17	ARB_ LOCKOUT_IF_ EN	0x0	DCU arbiter lockout control	
16	DCU_IS_BRN	0x0	Beacon use indication. Indicates whether the DCU is being used for beacons.	
			0	DCU is being used for non-beacon frames only
			1	DCU is being used for beacon frames only
15:14	VIRT_COL_ POLICY	0x0	Virtual collision handling policy. Resets to 0x0. 0 - 1 - 2 - Reserved 3 - Reserved	
			3:2	Reserved
			1	Ignore. Virtual collisions are ignored (i.e., the DCU immediately re-arbitrates for access to the PCU without doing a backoff and without incrementing the retry count)
			0	Default handling. A virtual collision is processed like a collision on the air except that the retry count for the frame is not incremented (that is, just do the backoff)
13	RES	0x0	Reserved	
12	BKOFF_PF	0x0	Backoff persistence factor setting.	
			0	New CW equals old CW
			1	Use binary-exponential CW progression
11	HCF_POLL_EN	0x0	HCF poll enable.	
			0	DCU operates in VDCF mode
			1	DCU operates in HCF mode
10	RES	0x0	Reserved	

Bit	Bit Name	Reset	Description	
9	FRAG_ BURST_ BKOFF_EN	0x0	Fragment burst backoff policy. This bit controls whether the DCU performs a backoff after each transmission of a fragment (that is, a frame with the MoreFrag bit set in the frame control field).	
			0	The DCU handles fragment bursts normally -- no backoff is performed after a successful transmission, and the next fragment is sent at SIFS.
			1	Modified handling. The DCU performs a backoff after all fragments, even those transmitted successfully. In addition, after the backoff count reaches zero, the DCU then follows the normal channel access procedure and sends at AIFS rather than at SIFS. This setting is intended to ease the use of fragment bursts in XR mode see bug 4454 for more details.
8	FRAG_ BURST_WAIT_ QCU_EN	0x0	Fragment burst frame starvation handling policy. This bit controls the DCU operation when the DCU is in the middle of a fragment burst and finds that the QCU sourcing the fragments does not have the next fragment available.	
			0	The DCU terminates the fragment burst. Note that when this occurs, the remaining fragments (when the QCU eventually has them available) will be sent as a separate fragment burst with a different sequence number
			1	The DCU waits for the QCU to have the next fragment available. While doing so, all other DCUs will be unable to transmit frames.
7	CW_RST_AT_ TS_END)DIS	0x0	End of transmission series CW reset policy. Note that this bit controls only whether the contention window is reset when transitioning from one transmission series to the next *within* a single frame. The CW is reset per the 802.11 spec when the entire frame attempt terminates (either because the frame was sent successfully or because all transmission series failed).	
			0	Reset the CW to CW_MIN at the end of each intraframe transmission series.
			1	Do not reset the CW at the end of each intraframe transmission series.
6	SFC_RST_AT_ TS_END_EN	0x0	End of transmission series station RTS data failure count reset policy. Note that this bit controls only whether the two station failure counts are reset when transitioning from one transmission series to the next *within* a single frame. The counts are reset per the 802.11 spec when the entire frame attempt terminates (either because the frame was sent successfully or because all transmission series failed).	
			0	Do not reset the station RTS failure count or the station data failure count at the end of each transmission series.
			1	Reset both the station RTS failure count and the station data failure count at the end of each transmission series
5:0	DATA_BKOFF _THRESH	0x2	Backoff threshold setting. Determines the backoff count at which the DCU will initiate arbitration for access to the PCU and commit to sending the frame.	

8.12.10 DCU Sequence (D_SEQ)

Offset: 0x18101140
Access: Read/Write
Reset: 0x0

MAC DCU sequence number register.

Bit	Bit Name	Description
31:12	RES	Reserved
11:0	NUM	Value of the sequence number to be inserted into the next frame. Shared across all DCUs.

8.12.11 DCU Pause (D_PAUSE)

Offset: 0x18101270
Access: Read/Write
Reset: See field description

MAC DCU pause register.

Bit	Bit Name	Reset	Description
31:21	RES	0x0	Reserved
20:17	SPARE	0x0	Spare bits
16	STATUS	0x1	Transmit pause status. Resets to 0x1. 0 - 1 -
			0 Transmit pause request has not yet taken effect. This means that some of the DCUs for which a transmission pause request has been issued via bits [9:0] of this register still are transmitting and have not yet paused.
			1 All DCUs for which a transmission pause request has been issued via bits [9:0] of this register, if any, have in fact paused their transmissions. Note that if no transmission pause request is pending (that is, bits [9:0] of this register are all set to 0), then this transmit pause status bit will be set to one.
15:10	RES	0x0	Reserved
9:0	REQUEST	0x0	Request that some subset of the DCUs pause transmission. For bit D of this field (9<=D<=0.
			0 Allow DCU D to continue to transmit normally
			1 Request that DCU D pause transmission as soon as it is able to do so.
11:0	NUM	Value of the sequence number to be inserted into the next frame. Shared across all DCUs.	

8.12.12 DCU Transmission Slot Mask (D_TXSLOTMASK)

Offset: 0x181012F0
Access: Read/Write
Cold Reset: 0x0
Warm Reset: Unaffected

Bit	Bit Name	Description
31:16	RES	Reserved
15	SLOT_TX[15]	Specifies whether transmission may start on slot numbers that are congruent to 15 (mod 16)
		0 Transmission may start on such slots
		1 Transmission may not start on such slots
...	...	...
1	SLOT_TX[1]	Specifies whether transmission may start on slot numbers that are congruent to 1 (mod 16)
		0 Transmission may start on such slots
		1 Transmission may not start on such slots
0	SLOT_TX[0]	Specifies whether transmission may start on slot numbers that are congruent to 0 (mod 16)
		0 Transmission may start on such slots
		1 Transmission may not start on such slots

8.12.13 MAC Sleep Status (SLEEP_STATUS)

Offset: 0x18101F00
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Sleep status

8.12.14 MAC LED Configuration (LED_CONFIG)

Offset: 0x18101F04
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	LED Configuration

8.13 WMAC Glue Registers

Table 8-14 summarizes the WMAC glue control registers.

Table 8-14 WMAC Glue Registers

Offset	Name	Description	Page
0x18104000	WMAC_GLUE_INTF_RESET_CONTROL	Interface Reset Control	page 222
0x18104008	WMAC_GLUE_INTF_INTR_SYNC_ENABLE	Synchronous Interrupt Enable	page 222
0x18104018	WMAC_GLUE_INTF_TIMEOUT	Interface Timeout	page 222
0x18104028	WMAC_GLUE_INTF_INTR_SYNC_CAUSE	Synchronous Interrupt Cause	page 222
0x1810402C	WMAC_GLUE_INTF_INTR_SYNC_ENABLE	Synchronous Interrupt Enable	page 223
0x18104030	WMAC_GLUE_INTF_INTR_ASYNC_MASK	Asynchronous Interrupt Mask	page 223
0x18104034	WMAC_GLUE_INTF_INTR_SYNC_MASK	Synchronous Interrupt Mask	page 223
0x18104038	WMAC_GLUE_INTF_INTR_ASYNC_ CAUSE	Asynchronous Interrupt Cause	page 223
0x1810403C	WMAC_GLUE_INTF_INTR_ASYNC_ ENABLE	Asynchronous Interrupt Enable	page 224
0x18104048	WMAC_GLUE_INTF_GPIO_IN	GPIO Input	page 224
0x1810404C	WMAC_GLUE_INTF_GPIO_INPUT_VALUE	WMAC Glue GPIO Input Value	page 224
0x18104050	WMAC_GLUE_INTF_SWCOM_GPIO_ FUNC_ENABLE	GPIO SWCOM Enable Function	page 224
0x1810405C	WMAC_GLUE_INTF_GPIO_INPUT_VALUE	WMAC Glue GPIO Input Value	page 225
0x18104074	WMAC_GLUE_INTF_GPIO_INPUT_STATE	Output Values from MAC to GPIO Pins	page 225
0x181040A0	WMAC_GLUE_INTF_MISC	WMAC Glue Miscellaneous	page 226
0x181040B4	WMAC_GLUE_INTF_MAC_TXAPSYNC	Synchronous AP Transmit	page 226
0x181040B8	WMAC_GLUE_INTF_MAC_TXSYNC_ INITIAL_SYNC_TMR	Synchronous Initial Timer	page 226
0x181040BC	WMAC_GLUE_INTF_INTR _PRIORITY_SYNC_CAUSE	Synchronous Priority Interrupt Cause	page 226
0x181040C0	WMAC_GLUE_INTF_INTR _PRIORITY_SYNC_ENABLE	Synchronous Priority Interrupt Enable	page 227
0x181040C4	WMAC_GLUE_INTF_INTR _PRIORITY_ASYNC_MASK	Asynchronous Priority Interrupt Mask	page 227
0x181040C8	WMAC_GLUE_INTF_INTR _PRIORITY_SYNC_MASK	Synchronous Priority Interrupt Mask	page 227
0x181040CC	WMAC_GLUE_INTF_INTR _PRIORITY_ASYNC_CAUSE	Asynchronous Priority Interrupt Cause	page 228
0x181040D4	WMAC_GLUE_INTF_INTR _PRIORITY_ASYNC_ENABLE	Asynchronous Priority Interrupt Enable	page 228
0x181040F0	WMAC_GLUE_INTF_AXI_BYTE_SWAP	AXI to MAC and MAC to AXI Byte Swap Enable	page 228

8.13.1 Interface Reset Control (WMAC_GLUE_INTF_RESET_ CONTROL)

Offset: 0x18104000
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:2	RES	Reserved	
1	APB_RESET	0	Normal operation of the MAC APB interface
		1	Hold the MAC APB interface in reset
0	RES	Reserved	

8.13.2 Synchronous Interrupt Enable (WMAC_GLUE_INTF_INTR_ SYNC_ENABLE)

Offset: 0x18104008
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Writing a 1 to any bit in this register will allow the corresponding interrupt signal to set its corresponding bit in the synchronous interrupt cause register.

8.13.3 Interface Timeout (WMAC_GLUE_INTF_TIMEOUT)

Offset: 0x18104018
Access: Read/Write
Reset: 0x0

APB and AXI timeout counter.

Bit	Bit Name	Description
31:16	AXI_TIMEOUT_ VAL	AXI timeout counter for DMA success
15:0	RES	Reserved

8.13.4 Synchronous Interrupt Cause (WMAC_GLUE_INTF_INTR_ SYNC_CAUSE)

Offset: 0x18104028
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Any bit set to 1 in this register indicates that the corresponding interrupt has been triggered in the synchronous mode. In order for any bit to be set in this register, the corresponding bit in the synchronous interrupt enable register must also be set.

8.13.5 Synchronous Interrupt Enable (WMAC_GLUE_INTF_INTR_SYNC_ENABLE)

Offset: 0x1810402C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Any bit set to 1 in this register allows the corresponding interrupt signal to set its corresponding bit in the synchronous interrupt cause register.

8.13.6 Asynchronous Interrupt Mask (WMAC_GLUE_INTF_INTR_ASYNC_MASK)

Offset: 0x18104030
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	A bit set to 1 in this register allows the corresponding interrupt signal to trigger a PCI/PCIE interrupt provided that the corresponding Async Interrupt cause register bit is set. Note that for the Async Interrupt Cause register bit to be set, the corresponding Async Interrupt Enable register bit must also be set by the software

8.13.7 Synchronous Interrupt Mask (WMAC_GLUE_INTF_INTR_SYNC_MASK)

Offset: 0x18104034
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	A bit set to 1 in this register allows the corresponding interrupt signal to trigger a PCI/PCIE interrupt provided that the corresponding Sync Interrupt cause register bit is set. Note that for the Sync Interrupt Cause register bit to be set, the corresponding Sync Interrupt Enable register bit must also be set by the software

8.13.8 Asynchronous Interrupt Cause (WMAC_GLUE_INTF_INTR_ASYNC_CAUSE)

Offset: 0x18104038
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Any bit set to 1 in this register indicates that the corresponding interrupt has been triggered in the asynchronous mode. In order for any bit to be set in this register, the corresponding bit in the asynchronous interrupt enable register must also be set.

8.13.9 Asynchronous Interrupt Enable (WMAC_GLUE_INTF_INTR_ASYNC_ENABLE)

Offset: 0x1810403C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	DATA	Any bit set to 1 in this register allows the corresponding interrupt signal to set its corresponding bit in the asynchronous interrupt cause register.

8.13.10 GPIO Output (WMAC_GLUE_INTF_GPIO_OUT)

Offset: 0x18104048
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:4	RES	Reserved
3:0	OUT	Output value of each GPIO. This value is only used if the corresponding GPIO enable bits and GPIO output MUX registers are set correctly.

8.13.11 GPIO Input (WMAC_GLUE_INTF_GPIO_IN)

Offset: 0x1810404C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:11	RES	Reserved
10:0	IN	Input value of each GPIO. This value is only used if the corresponding GPIO enable bits and GPIO output MUX registers are set correctly.

8.13.12 GPIO SWCOM Enable Function (WMAC_GLUE_INTF_SWCOM_GPIO_FUNC_ENABLE)

Offset: 0x18104050
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:4	RES	Reserved
3:0	OUT	Enables GPIO output signals on SWCOM pins

8.13.13 WMAC Glue GPIO Input Value (WMAC_GLUE_INTF_GPIO_INPUT_VALUE)

Offset: 0x1810405C
Access: Read/Write
Reset: 0x0

WMAC Glue GPIO input value

Bit	Bit Name	Description	
31:17	RES	Reserved	
16	RTC_RESET_OVRD_ENABLE	0	RTC reset is entirely controlled by software
		1	RTC reset is controlled by GPIO input as well as software
15	RFSILENT_BB_L_ENABLE	0	Set RFSILENT_BB_L to default value
		1	Connect RFSILENT_BB_L to GPIO input
14	CLK25_ENABLE	0	Set CLK25 to default value
		1	Connect CLK25 to GPIO input
13:9	RES	Reserved	
8	GPIO_RST_TSF_ENABLE	0	Set RST_TSF to default value
		1	Connect RST_TSF to GPIO input
7	RFSILENT_BB_L_VAL	Default value of RFSILENT_BB_L input	
6	CLK25_VAL	Default value of CLK25 input	
5:0	RES	Reserved	

8.13.14 Output Values from MAC to GPIO Pins (WMAC_GLUE_INTF_GPIO_INPUT_STATE)

Offset: 0x18104074
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:7	RES	Reserved
6	TX_FRAME	Tx frame
5	RX_CLEAR_EXTERNAL	Rx clear external
4	LED_POWER_EN	LED power
3	LED_NETWORK_EN	LED network
2	RES	Reserved
1	PWR_LED	LED power
0	ATT_LED	ATT LED

8.13.15 WMAC Glue Miscellaneous (WMAC_GLUE_INTF_MISC)

Offset: 0x181040A0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved
0	AT_SPEED_EN	WMAC glue miscellaneous

8.13.16 Synchronous AP Transmit (WMAC_GLUE_INTF_MAC_ TXAPSYNC)

Offset: 0x181040B8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved
0	DATA	

8.13.17 Synchronous Initial Timer (WMAC_GLUE_INTF_MAC_ TXSYNC_INITIAL_SYNC_TMR)

Offset: 0x181040BC
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	DATA	

8.13.18 Synchronous Priority Interrupt Cause (WMAC_GLUE_INTF_ INTR_PRIORITY_SYNC_CAUSE)

Offset: 0x181040C0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	Any bit set to 1 in this register indicates that the corresponding interrupt has been triggered in synchronous mode. For any bit to be set in this register, the corresponding bit in the synchronous priority interrupt enable register must also be set by software:	
		Bit[0]	Tx interrupt triggered
		Bit[1]	Rx low priority interrupt triggered
		Bit[2]	Rx high priority interrupt triggered

8.13.19 Synchronous Priority Interrupt Enable (WMAC_GLUE_INTF_INTR_PRIORITY_SYNC_ENABLE)

Offset: 0x181040C4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	Any bit set to 1 in this register allows the corresponding interrupt signal to set its corresponding bit in the asynchronous priority interrupt cause register:	
		Bit[0]	Tx interrupt enable
		Bit[1]	Rx low priority interrupt enable
		Bit[2]	Rx high priority interrupt enable

8.13.20 Asynchronous Priority Interrupt Mask (WMAC_GLUE_INTF_INTR_PRIORITY_ASYNC_MASK)

Offset: 0x181040C8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	A bit set to 1 in this register allows the corresponding interrupt signal to trigger a CPU interrupt provided that the corresponding synchronous priority interrupt cause register bit is set. For the priority asynchronous interrupt cause register bit to be set, the corresponding asynchronous priority interrupt enable register bit must also be set by software:	
		Bit[0]	Tx interrupt mask
		Bit[1]	Rx low priority interrupt mask
		Bit[2]	Rx high priority interrupt mask

8.13.21 Synchronous Priority Interrupt Mask (WMAC_GLUE_INTF_INTR_PRIORITY_SYNC_MASK)

Offset: 0x181040CC
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	A bit set to 1 in this register allows the corresponding interrupt signal to trigger a CPU interrupt provided that the corresponding synchronous priority interrupt cause register bit is set. For the priority asynchronous interrupt cause register bit to be set, the corresponding asynchronous priority interrupt enable register bit must also be set by software:	
		Bit[0]	Tx interrupt mask
		Bit[1]	Rx low priority interrupt mask
		Bit[2]	Rx high priority interrupt mask

8.13.22 Asynchronous Priority Interrupt Cause (WMAC_GLUE_INTF_INTR_PRIORITY_ASYNC_CAUSE)

Offset: 0x181040D0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	Any bit set to 1 in this register indicates that the corresponding interrupt has been triggered in asynchronous mode. For any bit to be set in this register, the corresponding bit in the asynchronous priority interrupt enable register must also be set by software:	
		Bit[0]	Tx interrupt triggered
		Bit[1]	Rx low priority interrupt triggered
		Bit[2]	Rx high priority interrupt triggered

8.13.23 Asynchronous Priority Interrupt Enable (WMAC_GLUE_INTF_INTR_PRIORITY_ASYNC_ENABLE)

Offset: 0x181040D4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:3	RES	Reserved	
2:0	DATA	Any bit set to 1 in this register allows the corresponding interrupt signal to set its corresponding bit in the asynchronous priority interrupt cause register:	
		Bit[0]	Tx interrupt enable
		Bit[1]	Rx low priority interrupt enable
		Bit[2]	Rx high priority interrupt enable

8.13.24 AXI to MAC and MAC to AXI Byte Swap Enable (WMAC_GLUE_INTF_AXI_BYTE_SWAP)

Offset: 0x181040F0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:1	RES	Reserved	
0	ENABLE	0	Do not swap data bytes of a 32-bit word, transferred between Memory and MAC (Default)
		1	Swap data bytes of a 32-bit word, transferred between Memory and MAC

8.14 RTC Registers

RTC registers occupy the offset range 0x18107000-0x18107FFC in the QCA9563 address space. Within this address range, the 0x18107040-0x18107058 registers are always on and available for software access regardless of whether the RTC is asleep. Table 8-15 summarizes the RTC registers for the QCA9563.

Table 8-15 RTC Summary

Address	Name	Description	Page
0x18107000	RESET_CONTROL	Reset Control	page 229
0x18107004	XTAL_CONTROL	XTAL Control	page 230
0x18107014	WLAN_PLL_CONTROL	WLAN PLL Control Settings	page 231
0x18107018	PLL_SETTLE	PLL Settling Time	page 232
0x1810701C	XTAL_SETTLE	Crystal Settling Time	page 232
0x18107020	CLOCK_OUT	Pin Clock Speed Control	page 233
0x18107028	RESET_CAUSE	Reset Cause	page 234
0x1810702C	SYSTEM_SLEEP	System Sleep Status	page 234
0x18107034	KEEP_AWAKE	Keep Awake Timer	page 235
0x18107038	DERIVED_RTC_CLK	Derived RTC Clock	page 235
0x1810703C	PLL_CONTROL2	PLL Control	page 236
0x18107040	RTC_SYNC_REGISTER	RTC Sync Reset	page 236
0x18107044	RTC_SYNC_STATUS	RTC Sync Status	page 236
0x18107048	RTC_SYNC_DERIVED	RTC Derived	page 237
0x1810704C	RTC_SYNC_FORCE_WAKE	RTC Force Wake	page 237
0x18107050	RTC_SYNC_INTR_CAUSE	RTC Interrupt Cause	page 237
0x18107054	RTC_SYNC_INTR_ENABLE	RTC Interrupt Enable	page 238
0x18107058	RTC_SYNC_INTR_MASK	RTC Interrupt Mask	page 238

8.14.1 Reset Control (RESET_CONTROL)

Address: 0x18107000
Access: Read/Write
Reset: 0x0

This register is used to control individual reset pulses to functional blocks. Software can hold any target block in reset by writing a 1 to the corresponding bit in this register. Reset will be held asserted to the target block as long as the corresponding bit is set. Multiple blocks may be held in reset simultaneously.

Bit	Bit Name	Description
31:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3	COLD_RST	Cold reset
2	WARM_ RESET	Warm reset
1	MAC_COLD_RST	Holds MAC block in cold reset, including BB and Radio. To clear this reset, SW must write a 0 and poll (for 62-92 µsecs) till this bit returns a 0.
0	MAC_WARM_RST	Holds MAC block in warm reset, including BB and radio

8.14.2 XTAL Control (XTAL_CONTROL)

Address: 0x18107004
Access: Read/Write
Reset: See field description

This register controls the analog crystal interface, the regulator and the clock source selection between an TCXO and a crystal.

Bit	Bit Name	Reset	Description	
31:1	RES	0x0	Reserved	
0	TXCO	0x0	When a TCXO device is used, software should set this field to 1 **WARNING** If this field is set to 1 when a crystal is being used, the high speed clock will stop and the chip will hang.	
			0	The chip is being driven by a crystal.
			1	The chip is being driven by a TCXO device

8.14.3 Switching Regulator Control Bits 0 (REG_CONTROL0)

Address: 0x18107008
Access: Read/Write
Reset: See field description

This register contains the regulator control bits for switching.

Bit	Bit Name	Reset	Description
31:0	SWREG_BITS	0x0	Switching regulator control bits

8.14.4 WLAN PLL Control Settings (WLAN_PLL_CONTROL)

Address: 0x18107014
Access: Read/Write
Reset: See field description

Control settings for the PLL.: This register provides access to the PLL setup control signals. Any write to this register will freeze all high speed clocks for 61 µsec. The clock select lines and PLL control lines will change after 30.5 µsec, then another 30.5 µsec passes before enable to allow the clocks to settle.

PLL freq = (refclk/refdiv) * (div_int + div_frac*2^4/(2^18-1)) * (1/f(clk_sel)).

Before applying f(clk_sel) frequency range is 530 ~ 830 MHz.

NOTE This reset values of some fields in this register must be kept in sync with the corresponding fields in bb reg 31

Bit	Bit Name	Type	Reset	Description
31	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
30	MAC_ OVERRIDE	RW	0x0	When set, a MAC clock request will deassert PLLBYPASS even if the BYPASS field is set to 1. This can be set when its the preferable time to select the ON state to use the PLL, instead of the SOC_ON state.
29	NOPWD	RW	0x0	Prevents the PLL from being powered down when the PLLBYPASS is asserted or when in light sleep
28	UPDATING	RO	0x0	This bit is set during the PLL update process. After software writes to the PLL_CONTROL, it takes about 45 secs for the update to occur. Software may poll this bit to see if the update has taken place.
				0 PLL update is complete
				1 PLL update is pending
27	BYPASS	RW	0x00000001	Bypass PLL. This defaults to 1 for test purposes. Software must enable the PLL for normal operation.
26:25	CLK_SEL	RW	0x0	Controls the final PLL select.
				00 1
				01 2
				10 4
				11 Bypass
24:20	REFDIV	RW	0x00000005	Reference clock divider
19:6	DIV_FRAC	RW	0x0	Primary multiplier
5:0	DIV_INT	RW	0x2C	Primary multiplier

8.14.5 PLL Settling Time (PLL_SETTLE)

Address: 0x18107018
Access: Read/Write
Reset: See field description

This register sets the PLL settling time. The PLL requires some time to settle once it is powered up or reprogrammed. Each time the PLL parameters change due to a write to the PLL register or a system event which changes the PLL control, hardware will gate off the clocks for PLL_SETTLE time while the PLL stabilizes. Units are in REFCLK periods.

NOTE The reset values of this register must be kept in sync with the corresponding field in the baseband register 31.

Bit	Bit Name	Reset	Description
31:11	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
10:0	TIME	0x00000400	Time required for the PLL to settle. Units are in REFCLK periods, so the default value of 1024 will result in a 25.6 μsec settling time. This register should never be set less than 100.

8.14.6 Crystal Settling Time (XTAL_SETTLE)

Address: 0x1810701C
Access: Read/Write
Reset: See field description

This register sets the crystal settling time. The external crystal requires some time to settle once it is powered up. The power occurs as chip passes through the WAKEUP state, between OFF and ON or between SLEEP an ON. This exact time will vary and must be characterized, so this register is provided to allow the XTAL power up FSM to transition in the minimal correct time. The default value of 63 will always allow the XTAL to be fully settled before clocks are enabled, but this value can be set to a smaller value if hardware characterization approves. The timer will expire in (XTAL_SETTLE + 1) clocks. Unlike most registers, XTAL_SETTLE will retain its programmed value in the RTC block during reset. The value programmed in this register should be matched to the MAC register Sleep Clock 32 KHz Wake, field 'SLEEP32_WAKE_XTL_TIME'. Note that the MAC register value is in microseconds.

Bit	Bit Name	Reset	Description
31:7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:0	TIME	0x00000001	Time required for the XTAL to settle. Units are in 30 μsecs, so the default value of 66 will result in 2.0 msec settling time. this register should never be set to 0.

8.14.7 Pin Clock Speed Control (CLOCK_OUT)

Address: 0x18107020
Access: Read/Write
Reset: See field description

This register controls the CLK_OUT pin clock speed. The output clock can be used for testing or to drive external components.

Bit	Bit Name	Reset	Description	
31:7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
6:4	DELAY	0x00000000	Controls the tap selection point for CLK_OUT on a delay line when SELECT[2] is set. 000 corresponds to the least delay while 111 corresponds to the maximum display (100 to 180 degree delay).	
3:0	SELECT	0x00000000	Controls the CLK_OUT speed. The binary MUX select decode is as follows:	
			0000	Low
			0001	CLKOBSOUT (from the PCIE PHY)
			0010	CLK80_ADC
			0011	CLK160_DAC
			0100	LCL20A (delayed as specified by the DELAY field)
			0101	LCL40A (delayed as specified by the DELAY field)
			0110	LCL80A (delayed as specified by the DELAY field)
			0111	LCL160A (delayed as specified by the DELAY field)
			1000	CLK128
			1001	XTLCLK
			1010	CLK80_ADC
			1011	CLK160_DAC
			1100	RTC_CLK_W (delayed as specified by the DELAY field)
			1101	REFCLK_W (delayed as specified by the DELAY field)
			1110	PCI_CLK_W (delayed as specified by the DELAY field)
			1111	PCIE_CORE_CLK_W (delayed as specified by the DELAY field)

8.14.8 Reset Cause (RESET_CAUSE)

Address: 0x18107028
Access: Read/Write
Reset: See field description

This register holds the cause of the last reset event.

Bit	Bit Name	Reset	Description	
31:2	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
1:0	LAST	0x00000000	The value of this register holds the cause of the last reset, as stated:	
			0	Hard reset of the RTC
			1	Software wrote to the RTC_CONTOL_COLD_RST register
			2	Software wrote to the RTC_CONTOL_WARM_RST register
			3	Reserved

8.14.9 System Sleep Status (SYSTEM_SLEEP)

Address: 0x1810702C
Access: Read/Write
Reset: See field description

This register contains the system sleep status bits. System sleep state is entered when all high frequency clocks are gated and the high frequency crystal is shut down. This register is used to indicate the status of each sleep control interface. If any bit in this control register is 0, sleep is not permitted. If all bits are 1, sleep is permitted. The system will enter sleep as soon as the CPU executes a WAIT instruction. The LIGHT field will gate clocks off in SLEEP, but will keep the crystal running for faster wakeup. The DISABLE field will prevent the chip from entering SLEEP.

Bit	Bit Name	Reset	Description	
31:3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
2	MAC_IF	0x00000001	THE MAC block sleep state	
			0	The MAC block will not allow a sleep state
			1	The MAC block has enabled the sleep state
1	LIGHT	0x00000000	Controls whether or not the crystal is turned off during SLEEP. If the crystal is turned off, power consumption is lowered during sleep but the wakeup time is controlled by XTAL_SETTLE. If the crystal remains on, power consumption is higher but the wakeup time is about 45 μs.	
			0	System sleep is DEEP, resulting in minimal power consumption
			1	System sleep will be LIGHT
0	DISABLE	0x0000000	Enables or disables the system sleep	
			0	System sleep is enabled
			1	System sleep is disabled

8.14.10 Keep Awake Timer (KEEP_AWAKE)

Address: 0x18107034
Access: Read/Write
Reset: See field description

This register ensures that the chip does not enter the SLEEP state until at least the COUNT cycles have passed from the time of the last CLK_REQ event.

Bit	Bit Name	Reset	Description
31:8	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	COUNT	0x00000000	The keep awake timer measured in 32 KHz (30.5 μsecs) cycles

8.14.11 Derived RTC Clock (DERIVED_RTC_CLK)

Address: 0x18107038
Access: Read/Write
Reset: See field description

This register creates a 32 KHz clock, derived from the HF. This register controls a scaled output clock which can be used to generate lower frequency clocks based on the reference clock. For example, a 32.768 KHz clock can be generated by setting the divisor of the high speed clock accordingly. The accuracy will depend on how the divisors align with this integer count. RTC will start up normally using the derived RTC_CLK, and will switch to the LF_XTAL if it detects an LF_XTAL (this behavior can be modified using the fields in the RTC_SYNC_DERIVED register) since the external LF_XTAL is mostly unsupported.

Bit	Bit Name	Type	Reset	Description	
31:19	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
18	EXTERNAL_DETECT	RO	0x0	Detects external 32 KHz XTALs; if a LF XTAL is detected and RTC_SYNC_DERIVED clear, the RTC automatically uses the external XTAL.	
				0	No XTAL is detected
				1	LFXTAL not detected
17:16	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
15:1	PERIOD	RW	0x262	The period of the derived clock is 2 * (PERIOD + 1). The reset value creates a 30.55 sec clock if the REFCLK is 40 MHz. The 30.5 μs value is closer to 32.768 KHz. To set it to 30.5 μs, the PERIOD value should be 0x261. To set to 30.48 μs, the PERIOD should be 0x17C. HALF_CLK_LATENCY and TSF_INC fields in MAC PCU should also be set appropriately.	
0	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	

8.14.12 PLL Control (PLL_CONTROL2)

Address: 0x1810703C
Access: Read/Write
Reset: See field description

This register provides access to the PLL setup control signals for the additional bits required for the PLL.

Bit	Bit Name	Type	Reset	Description
31:7	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:3	DIV_FRAC	RW	0x0	Additional fractional bits
2:0	DIV_INT	RW	0x0	Additional int bits

8.14.13 RTC Sync Reset (RTC_SYNC_RESET)

Address: 0x18107040
Access: Read/Write
Reset: See field description

This register sets the RTC reset, force sleep and force wakeup.

Bit	Bit Name	Type	Reset	Description	
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
0	RESET	RW	0x0	Active low signal setting	
				0	RTC is currently resetting
				1	RTC is not currently resetting

8.14.14 RTC Sync Status (RTC_SYNC_STATUS)

Address: 0x18107044
Access: Read-Only
Reset: 0x0

This register denotes the current use of RTC.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	PLL_ CHANGING	PLL_CHANGING signal from RTC
4	WRESET	Denotes the RTC was accessed while the MAC is asleep
3	WAKEUP_STATE	RTC is in the wakeup state
2	SLEEP_STATE	RTC is in the sleep state
1	ON_STATE	RTC is in the on state
0	SHUTDOWN_STATE	RTC is in the shutdown state

8.14.15 RTC Derived (RTC_SYNC_DERIVED)

Address: 0x18107048
Access: Read/Write
Reset: See field description

This register is for the Derived RTC.

Bit	Bit Name	Reset	Description
31:2	RSVD	0x0	Reserved
1	FORCE	0x0	Force Derived RTC
0	BYPASS	0x0	Bypass the Derived RTC

8.14.16 RTC Force Wake (RTC_SYNC_FORCE_WAKE)

Address: 0x1810704C
Access: Read/Write
Reset: See field description

This register enables a Force Wake to the MAC.

Bit	Bit Name	Reset	Description
31:2	RSVD	0x0	Reserved
1	INTR	0x1	Allows a MAC interrupt to assert a force wake enable
0	ESABLE	0x1	Enables a Force Wake to the MAC

8.14.17 RTC Interrupt Cause (RTC_SYNC_INTR_CAUSE)

Address: 0x18107050
Access: Read/Write
Reset: 0x0

This register is a controller that works the same way as the host interface interrupt controller. Each bit in the interrupt cause register pertains to an event as described here. A write of 1 to any bit in this register will clear that bit in the interrupt cause register until the corresponding event occurs again.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	PLL_CHANGING	PLL_CHANGING signal received from RTC
4	SLEEP_ACCESS	RTC accessed while MAC is asleep
3	WAKEUP_STATE	RTC is in wakeup state
2	SLEEP_STATE	RTC is in sleep state
1	ON_STATE	RTC is in on state
0	SHUTDOWN_STATE	RTC is in shutdown state

8.14.18 RTC Interrupt Enable (RTC_SYNC_INTR_ENABLE)

Address: 0x18107054
Access: Read/Write
Reset: 0x0

This register is used for the RTC interrupts. Writing a 1 to any bit in this register allows that bit in the interrupt cause register to be set when the corresponding event occurs. Writing a 0 to any bit in this register will automatically clear the corresponding bit in the interrupt cause register regardless of the corresponding event.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	PLL_CHANGING	PLL_CHANGING signal received from RTC
4	SLEEP_ACCESS	RTC accessed while MAC is asleep
3	WAKEUP_STATE	RTC is in wakeup state
2	SLEEP_STATE	RTC is in sleep state
1	ON_STATE	RTC is in on state
0	SHUTDOWN_STATE	RTC is in shutdown state

8.14.19 RTC Interrupt Mask (RTC_SYNC_INTR_MASK)

Address: 0x18107058
Access: Read/Write
Reset: 0x0

This register is the mask for RTC interrupts. Writing a 1 to any bit in this register will allow the corresponding event to generate an RTC Interrupt to the host interface, which can be programmed to generate a system interrupt. The corresponding bit in the RTC Interrupt Enable register must also be set.

Bit	Bit Name	Description
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	PLL_CHANGING	PLL_CHANGING signal received from RTC
4	SLEEP_ACCESS	RTC accessed while MAC is asleep
3	WAKEUP_STATE	RTC is in wakeup state
2	SLEEP_STATE	RTC is in sleep state
1	ON_STATE	RTC is in on state
0	SHUTDOWN_STATE	RTC is in shutdown state

8.15 WLAN MAC Protocol Control Unit Registers

Table 8-16 shows the mapping of the WLAN MAC Protocol Control Unit Registers.

Table 8-16 WLAN MAC Protocol Control Unit Registers

Address	Name	Description	Page
0x18108000	WMAC_PCU_STA_ADDR_L32	STA Address Lower 32 Bits	page 242
0x18108004	WMAC_PCU_STA_ADDR_U16	STA Address Upper 16 Bits	page 242
0x18108008	WMAC_PCU_BSSID_L32	BSSID Lower 32 Bits	page 243
0x1810800C	WMAC_PCU_BSSID_U16	BSSID Upper 16 Bits	page 243
0x18108010	WMAC_PCU_BCN_RSSI_AVE	Beacon RSSI Average	page 243
0x18108014	WMAC_PCU_ACK_CTS_TIMEOUT	ACK and CTS Timeout	page 244
0x18108018	WMAC_PCU_BCN_RSSI_CTL	Beacon RSSI Control	page 244
0x1810801C	WMAC_PCU_USEC_LATENCY	Millisecond Counter and Rx/Tx Latency	page 244
0x18108020	WMAC_PCU_RESET_TSF	Reset TSF	page 245
0x18108038	WMAC_PCU_MAX_CFP_DUR	Maximum CFP Duration	page 245
0x1810803C	WMAC_PCU_RX_FILTER	Rx Filter	page 246
0x18108040	WMAC_PCU_MCAST_FILTER_L32	Multicast Filter Mask Lower 32 Bits	page 247
0x18108044	WMAC_PCU_MCAST_FILTER_U32	Multicast Filter Mask Upper 32 Bits	page 247
0x18108048	WMAC_PCU_DIAG_SW	Diagnostic Switches	page 247
0x1810804C	WMAC_PCU_TSF_L32	TSF Lower 32 Bits	page 248
0x18108050	WMAC_PCU_TSF_U32	TSF Upper 32 Bits	page 249
0x1810805C	WMAC_PCU_AES_MUTE_MASK_0	AES Mute Mask 0	page 249
0x18108060	WMAC_PCU_AES_MUTE_MASK_1	AES Mute Mask 1	page 249
0x18108070	DYM_MIMO_PWR_SAVE	Dynamic MIMO Power Save	page 249
0x18108080	WMAC_PCU_LAST_BEACON_TSF	Last Receive Beacon TSF	page 250
0x18108084	WMAC_PCU_NAV	Current NAV	page 250
0x18108088	WMAC_PCU_RTS_SUCCESS_CNT	Successful RTS Count	page 250
0x1810808C	WMAC_PCU_RTS_FAIL_CNT	Failed RTS Count	page 250
0x18108090	WMAC_PCU_ACK_FAIL_CNT	FAIL ACK Count	page 251
0x18108094	WMAC_PCU_FCS_FAIL_CNT	Failed FCS Count	page 251
0x18108098	WMAC_PCU_BEACON_CNT	Beacon Count	page 251
0x181080D4	WMAC_PCU_SLP1	Sleep 1	page 252
0x181080D8	WMAC_PCU_SLP2	Sleep 2	page 252
0x181080E0	WMAC_PCU_ADDR1_MASK_L32	Address 1 Mask Lower 32 Bits	page 252
0x181080E4	WMAC_PCU_ADDR1_MASK_U16	Address 1 Mask Upper 16 Bits	page 253
0x181080E8	WMAC_PCU_TPC	Tx Power Control	page 253
0x181080EC	WMAC_PCU_TX_FRAME_CNT	Tx Frame Counter	page 253
0x181080F0	WMAC_PCU_RX_FRAME_CNT	Rx Frame Counter	page 254
0x181080F4	WMAC_PCU_RX_CLEAR_CNT	Rx Clear Counter	page 254

Table 8-16 WLAN MAC Protocol Control Unit Registers (cont.)

Address	Name	Description	Page
0x181080F8	WMAC_PCU_CYCLE_CNT	Cycle Counter	page 254
0x181080FC	WMAC_PCU_QUIET_TIME_1	Quiet Time 1	page 254
0x18108100	WMAC_PCU_QUIET_TIME_2	Quiet Time 2	page 255
0x18108108	WMAC_PCU_QOS_NO_ACK	QoS NoACK	page 255
0x1810810C	WMAC_PCU_PHY_ERROR_MASK	PHY Error Mask	page 256
0x18108114	WMAC_PCU_RXBUF	Rx Buffer	page 256
0x18108118	WMAC_PCU_MIC_QOS_CONTROL	QoS Control	page 257
0x1810811C	WMAC_PCU_MIC_QOS_SELECT	Michael QoS Select	page 257
0x18108120	WMAC_PCU_MISC_MODE	Miscellaneous Mode	page 258
0x18108124	WMAC_PCU_FILTER_OFDM_CNT	Filtered OFDM Counter	page 259
0x18108128	WMAC_PCU_FILTER_CCK_CNT	Filtered CCK Counter	page 259
0x1810812C	WMAC_PCU_PHY_ERR_CNT_1	PHY Error Counter 1	page 260
0x18108130	WMAC_PCU_PHY_ERR_CNT_1_MASK	PHY Error Counter 1 Mask	page 260
0x18108134	WMAC_PCU_PHY_ERR_CNT_2	PHY Error Counter 2	page 260
0x18108138	WMAC_PCU_PHY_ERR_CNT_2_MASK	PHY Error Counter 2 Mask	page 261
0x1810813C	WMAC_PCU_TSF_THRESHOLD	TSF Threshold	page 261
0x18108144	WMAC_PCU_PHY_ERROR_EIFS_MASK	PHY Error EIFS Mask	page 261
0x18108168	WMAC_PCU_PHY_ERR_CNT_3	PHY Error Counter 3	page 262
0x1810816C	WMAC_PCU_PHY_ERR_CNT_3_MASK	PHY Error Counter 3 Mask	page 262
0x18108180	WMAC_PCU_GENERIC_TIMERS2	MAC PCU Generic Timers 2	page 262
0x181081C0	WMAC_PCU_GENERIC_TIMERS2_MODE	MAC PCU Generic Timers Mode 2	page 262
0x181081D0	WMAC_PCU_TXSIFS	SIFS, Tx Latency and ACK Shift	page 263
0x181081EC	WMAC_PCU_TXOP_X	TXOP for Non-QoS Frames	page 263
0x181081F0	WMAC_PCU_TXOP_0_3	TXOP for TID 0 to 3	page 263
0x181081F4	WMAC_PCU_TXOP_4_7	TXOP for TID 4 to 7	page 264
0x181081F8	WMAC_PCU_TXOP_8_11	TXOP for TID 8 to 11	page 264
0x181081FC	WMAC_PCU_TXOP_12_15	TXOP for TID 0 to 3	page 264
0x18108200	WMAC_PCU_GENERIC_TIMERS[0:15]	Generic Timers	page 265
0x18108240	WMAC_PCU_GENERIC_TIMERS_MODE	Generic Timers Mode	page 265
0x18108244	WMAC_PCU_SLP32_MODE	32 KHz Sleep Mode	page 266
0x18108248	WMAC_PCU_SLP32_WAKE	32 KHz Sleep Wake	page 266
0x1810824C	WMAC_PCU_SLP32_INC	32 KHz Sleep Increment	page 267
0x18108250	WMAC_PCU_SLP_MIB1	Sleep MIB Sleep Count	page 267
0x18108254	WMAC_PCU_SLP_MIB2	Sleep MIB Cycle Count	page 267
0x18108258	WMAC_PCU_SLP_MIB3	Sleep MIB Control Status	page 268
0x18108284	1μS	1 μs Clocks	page 268

Table 8-16 WLAN MAC Protocol Control Unit Registers (cont.)

Address	Name	Description	Page
0x1810829C	PHY_ERR_CNT_MASK_CONT	PHY Error Counter Continued	page 268
0x18108318	WMAC_PCU_20_40_MODE	Global Mode	page 269
0x18108328	WMAC_PCU_RX_CLEAR_DIFF_CNT	Difference RX_CLEAR Counter	page 269
0x1810832C	SELF_GEN_ANTENNA_MASK	Self Generated Antenna Mask	page 271
0x18108330	WMAC_PCU_BA_BAR_CONTROL	Control Registers for Block BA Control Fields	page 271
0x18108334	WMAC_PCU_LEGACY_PLCP_SPOOF	Legacy PLCP Spoof	page 272
0x18108338	WMAC_PCU_PHY_ERROR_MASK_CONT	PHY Error Mask and EIFS Mask	page 272
0x1810833C	WMAC_PCU_TX_TIMER	Tx Timer	page 273
0x18108348	ALT_AES_MUTE_MASK	Alternate AES QoS Mute Mask	page 273
0x18108390	TSF2_L32	TSF 2 Lower 32	page 274
0x18108394	TSF2_U32	TSF 2 Upper 32	page 274
0x1810839C	BSSID2_U16	BSSID 2 Upper 16	page 274
0x181083A4	WMAC_PCU_TID_TO_AC	TID Value Access Category	page 274
0x181083A8	WMAC_PCU_HP_QUEUE	High Priority Queue Control	page 276
0x181083C8	WMAC_PCU_HW_BCN_PROC1	Hardware Beacon Processing 1	page 277
0x181083CC	WMAC_PCU_HW_BCN_PROC2	Hardware Beacon Processing 2	page 277
0x18108800	WMAC_PCU_KEY_CACHE[0:1023]	Key Cache	page 278

8.15.1 STA Address Lower 32 Bits (WMAC_PCU_STA_ADDR_L32)

Offset: 0x18108000

Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	ADDR_31_0	Lower 32 bits of STA MAC address (PCU_STA_ADDR[31:0])

8.15.2 STA Address Upper 16 Bits (WMAC_PCU_STA_ADDR_U16)

Offset: 0x18108004
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

This register contains the lower 32 bits of the STA address.

Bit	Name	Reset	Description
31	REG_ADHOC_MCAST_SEARCH	0x0	Enables the key cache search for ad hoc MCAST packets
30	PCU_CBCIV_ENDIAN	0x0	Endianess of IV in CBC nonce
29	REG_PRESERVE_SEQNUM	0x1	Stops PCU from replacing the sequence number
28	PCU_KSRCH_MODE	0x0	Search key cache first. If not, match use offset for IV = 0, 1, 2, 3. ■ If KSRCH_MODE = 0 then do not search ■ If IV = 1, 2, or 3, then search ■ If IV = 0, do not search
27	REG_CRPT_MIC_ENABLE	0x0	Enables the checking and insertion of MIC in TKIP
26	SECTOR_SELF_GEN	0x0	Use the default antenna for self-generated frames
25	PCU_BSRATE_11B	0x0	802.11b base rate 0 Use all rates 1 Use only 1–2 MBps
24	PCU_ACKCTS_6MB	0x0	Use 6 MBps rate for ACK and CTS
23	RTS_USE_DEF	0x0	Use the default antenna to send RTS
22	DEFANT_UPDATE	0x0	Update the default antenna with the Tx antenna
21	USE_DEFANT	0x0	When the descriptor chooses auto-select mode (0000), use the default antenna to transmit
20	PCU_PCF	0x0	Set if associated AP is PCF capable
19	KEYSRCH_DIS	0x0	Disable key search
18	PW_SAVE	0x0	Set if STA is in power-save mode
17	PCU_ADHOC	0x0	Set if STA is in an ad hoc network
16	PCU_AP	0x0	Set if STA is an AP
15:0	PCU_STA_ADDR[47:32]	0x0	Upper 16 bits of STA MAC address

8.15.3 BSSID Lower 32 Bits (WMAC_PCU_BSSID_L32)

Offset: 0x18108008
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

This register contains the lower 32 bits of the BSS identification information.

Bit	Name	Description
31:0	pcu_bssid[31:0]	Lower 32 bits of BSSID

8.15.4 BSSID Upper 16 Bits (WMAC_PCU_BSSID_U16)

Offset: 0x1810800C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0
This register contains the upper 32 bits of the BSS identification information.

Bit	Name	Description
31:17	RES	Reserved
26:16	PCU_AID	Association ID
15:0	PCU_BSSID[47:32]	Upper 16 bits of BSSID

8.15.5 Beacon RSSI Average (WMAC_PCU_BCN_RSSI_AVE)

Offset: 0x18108010
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x800
BCN_RSSI_AVE

Bit	Name	Description
31:12	RES	Reserved
11:0	REG_BCN_RSSI_AVE	Holds the average RSSI with 1/16 dB resolution. The RSSI is averaged over multiple beacons which matched our BSSID. AVE_VALUE is 12 bits with 4 bits below the normal 8 bits. These lowest 4 bits provide for a resolution of 1/16 dB. The averaging function is depends on the BCN_RSSI_WEIGHT; determines the ratio of weight given to the current RSSI value compared to the average accumulated value.

8.15.6 ACK and CTS Timeout (WMAC_PCU_ACK_CTS_TIMEOUT)

Offset: 0x18108014
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:30	RES	Reserved
29:16	PCU_CTS_TIMEOUT	Timeout while waiting for CTS (in cycles)
15:14	RES	Reserved
13:0	PCU_ACK_TIMEOUT	Timeout while waiting for ACK (in cycles)

8.15.7 Beacon RSSI Control (WMAC_PCU_BCN_RSSI_CTL)

Offset: 0x18108018
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:30	RES	Reserved
29	REG_BCN_RSSI_RST_ STROBE	The BCN_RSSI_RESET clears BCN_RSSI_AVE, page 8-243 to aid in changing channels
28:24	REG_BCN_RSSI_WEIGHT	Used to calculate BCN_RSSI_AVE, page 8-243
23:16	RES	Reserved
15:8	PCU_BCN_MISS_THR	Threshold at which the beacon miss interrupt asserts. Because the beacon miss counter increments at TBTT, it increments to 1 before the first beacon.
7:0	PCU_RSSI_THR	The threshold at which the beacon low RSSI interrupt is asserted when the average RSSI (BCN_RSSI_AVE, page 8-243) below this level

8.15.8 Ms Counter and Rx/Tx Latency (WMAC_PCU_USEC_ LATENCY)

Offset: 0x1810801C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Description
31:29	RES	Reserved
28:23	PCU_RXDELAY	Baseband Rx latency to start of SIGNAL (in μs)
22:14	PCU_TXDELAY	Baseband Tx latency to start of timestamp in beacon frame (in μs)
13:8	RES	Reserved
7:0	USEC	USEC defines the number of clock cycles minus 1 in 1 microsecond. For example, 40 cycles of a 40 MHz clock is 1 μsec, so this register would be programmed to be 39. If the clock frequency is 40 5/9 MHz, the fractional components need to be defined. In this case the numerator (register: MAC_PCU_MAX_CFP_DUR, field: USEC_FRAC_ NUMERATOR) should be set to 5 and the denominator (register: MAC_PCU_MAX_CFP_ DUR, field: USEC_FRAC_DENOMINATOR) should be set to 9. The USEC field would still be 39. Note that the D_GBL_IFS_MISC register, microsecond duration field in the DMA block has been removed and the function is now shared with the PCU logic.

8.15.9 Reset TSF (WMAC_PCU_RESET_TSF)

Offset: 0x18108020
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Controls beacon operation by the PCU.

Bit	Name	Description
31:26	RES	Reserved
25	ONE_SHOT2	Setting this bit causes the TSF2 to reset. This register clears immediately after reset.
24	ONE_SHOT	Setting this bit causes the TSF to reset. This register clears immediately after reset.
23:0	RES	Reserved

8.15.10 Maximum CFP Duration (WMAC_PCU_MAX_CFP_DUR)

Offset: 0x18108038
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Contains the maximum time for a contention free period.

Bit	Name	Description
31:28	RES	Reserved
27	USEC_FRAC _DENOMINATOR[27:24]	See description for USEC[7:0] in Ms Counter and Rx/Tx Latency (WMAC_ PCU_USEC_LATENCY)
23:20	RES	Reserved
16:16	USEC_FRAC _DENOMINATOR[19:16]	See description for USEC[7:0] in Ms Counter and Rx/Tx Latency (WMAC_ PCU_USEC_LATENCY)
15:0	VALUE[15:0]	Maximum contention free period duration (in µs)

8.15.11 Rx Filter (WMAC_PCU_RX_FILTER)

Offset: 0x1810803C|
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

This register determines Rx frame filtering.

NOTE If any bit is set, the corresponding packet types pass the filter and DMA. All filter conditions except the promiscuous setting rely on the no early PHY error and protocol version being checked to ensure it is version 0.

Bit	Name	Reset	Description
31:20	RES	0x0	Reserved
19	CONTROL_ WRAPPER	0x1	Enable receiving directed frames for control wrapper frames
18	MGMT_ACTION_ MCAST	0x0	Enable receive of multicast frames for management action frames
17	HW_BCN_PROC _ENABLE	0x0	If set, the beacon frame with matching BSSID is filtered per hardware beacon processing logic. See the HW_BCN_PROC register.
16	RST_DLMTR_CNT _DISABLE	0x0	Clearing this bit resets the ST_DLMTR_CNT to 0 when RXSM.STATE leaves the START_DELIMITER state.
15	MCAST_BCAST_ALL	0x0	Enables receipt of all multicast and broadcast frames
14	PS_POLL	0x0	Enables receipt of PS-POLL
13	ASSUME_RADAR	0x1	If set, a legacy PLCP rate of 0 indicates a radar packet that will not be filtered
12	UNCOMPRESSED_ BA_BAR	0x0	Uncompressed directed block ACK request or block ACK
11	COMPRESSED_BA	0x0	Compressed directed block ACK
10	COMPRESSED_BAR	0x0	Compressed directed block ACK request
9	MY_BEACON	0x0	Retrieves any beacon frame with matching SSID
8	RES	0x0	Reserved
7	PROBE_REQ	0x0	Probe request enable; enables reception of all probe request frames
6	XR_POLL	0x0	Any multicast or broadcast frame with a frame type matching the XR_POLL_ TYPE register
5	PROMISCUOUS	0x0	Promiscuous Rx enable; enables reception of all frames, including errors
4	BEACON	0x0	Beacon frame enable; enables reception of beacon frames.
3	CONTROL	0x0	Control frame enable; enables reception of control frames
2	BROADCAST	0x0	Broadcast frame enable; enables reception of non beacon broadcast frames that originate from the BSS whose ID matches BSSID
1	MULTICAST	0x0	Multicast frame enable; enables reception of multicast frames that match the multicast filter
0	UNICAST	0x0	Unicast frame enable; enables reception of unicast (directed) frames that match the STA address

8.15.12 Multicast Filter Mask Lower 32 Bits (WMAC_PCU_MCAST_FILTER_L32)

Offset: 0x18108040
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PCU_MCAST_MASK	Multicast filter mask low. Lower 32 bits of multicast filter mask.

8.15.13 Multicast Filter Mask Upper 32 Bits (WMAC_PCU_MCAST_FILTER_U32)

Offset: 0x18108044
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PCU_MCAST_MASK	Multicast filter mask high. Upper 32 bits of multicast filter mask.

8.15.14 Diagnostic Switches (WMAC_PCU_DIAG_SW)

Offset: 0x18108048
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Controls the operation of the PCU, including enabling/disabling acknowledgements, CTS, transmission, reception, encryption, loopback, FCS, channel information, and scrambler seeds.

Bit	Name	Description
31:30	RES	Reserved
29	RX_CLEAR_EXT_LOW	Force the RX_CLEAR_EXT signal to appear to the MAC as being low
28	RX_CLEAR_CTL_LOW	Force the RX_CLEAR_CTL signal to appear to the MAC as being low
27	OBS_SEL_2	Observation point select.
26	SATURATE_CYCLE_CNT	The saturate cycle count bit, if set, causes the Cycle Counter (WMAC_PCU_CYCLE_CNT) register to saturate instead of shifting to the right by 1 every time the count reaches 0xFFFFFFFF. This saturate condition also holds the RX_CLEAR, RX_FRAME, and TX_FRAME counts.
25	FORCE_RX_ABORT	Force Rx abort bit in conjunction with Rx block aids quick channel change to shut down Rx. The force Rx abort bit kills with the Rx_abort any frame currently transferring between the MAC and baseband. while the RX block bit prevents any new frames from getting started.

Bit	Name	Description
24	DUAL_CHAIN_CHAN_INFO	Dual chain channel information
23	PHYERR_ENABLE_EIFS_CTL	Used frame and WAIT_WEP in the PCU_RX_ERR logic if this bit is set to 0
22	CHAN_IDLE_HIGH	Force channel idle high
21	IGNORE_NAV	Ignore virtual carrier sense (NAV)
20	RX_CLEAR_HIGH	Force RX_CLEAR high
19:18	OBS_SEL_1	Observation point select
17	ACCEPT_NON_V0	Enable or disable protocol field
16:9	RES	Reserved
8	DUMP_CHAN_INFO	Dump channel information
7	CORRUPT_FCS	Corrupt FCS
6	LOOP_BACK	Enable or disable Tx data loopback
5	HALT_RX	Enable or disable reception
4	NO_DECRYPT	Enable or disable decryption
3	NO_ENCRYPT	Enable or disable encryption
2	NO_CTS	Enable or disable CTS generation
1	NO_ACK	Enable or disable acknowledgement generation for all frames
0	PCU_INVALKEY_NOACK	Enable or disable acknowledgement when a valid key is not found for the received frames in the key cache.

8.15.15 TSF Lower 32 Bits (WMAC_PCU_TSF_L32)

Offset: 0x1810804C

Access: Hardware = Read/Write

Software = Read/Write

Reset Value: 0xFFFFFFF

Bit	Name	Description
31:0	VALUE	The timestamp value in μs. Writes to this register do not cause the TSF to change. Rather, the value is held in a temporary staging area until this register is written, at which point both the lower and upper parts of the TSF are loaded. A read result of 0xFFFFFFFF indicates that the read occurred before TSF logic came out of sleep. It may take up to 45 μs after the chip is brought out of sleep for the TSF logic to wake.

8.15.16 TSF Upper 32 Bits (WMAC_PCU_TSF_U32)

Offset: 0x18108050
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0xFFFFFFF

Bit	Name	Description
31:0	VALUE	The timestamp value in μs

8.15.17 AES Mute Mask 0 (WMAC_PCU_AES_MUTE_MASK_0)

Offset: 0x1810805C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Reset	Description
31:16	QOS_MUTEMASK	0xFFFF	AES mute mask for TID field
15:0	FC_MUTEMASK	0x478F	AES mute mask for frame control field

8.15.18 AES Mute Mask 1 (WMAC_PCU_AES_MUTE_MASK_1)

Offset: 0x18108060
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Reset	Description
31:16	FC_MGMT	0xE7FF	AES mute mask for management frame control field
15:0	SEQ_MUTEMASK	0x000F	AES mute mask for sequence number field

8.15.19 Dynamic MIMO Power Save (DYM_MIMO_PWR_SAVE)

Address: 0x18108070
Access: Read/Write
Reset: See field description

This register is for the MAC PCU dynamic MIMO power save.

Bit	Bit Name	Reset	Description
31:11	RES	0x0	Reserved
10:8	HI_PWR_CHAIN_MASK	0x3	The high power setting of the Rx chain mask
7	RES	0x0	Reserved
6:4	LOW_PWR_CHAIN_MASK	0x1	The low power setting of the Rx chain mask
3	RES	0x0	Reserved
2	SW_CHAIN_MASK_SEL	0x0	The software selection of the dynamic MIMO power save

1	HW_CTRL_EN	0x0	Enable the hardware control of the dynamic MIMO power save
0	USE_MAC_CTRL	0x0	The Rx chain mask will be controlled by MAC

8.15.20 Last Receive Beacon TSF (MAC_PCU_LAST_BEACON_TSF)

Offset: 0x18108080
Access: Hardware = Write-only
Software = Read-Only
Reset Value: 0x0

This threshold register indicates the minimum amount of data required before initiating a transmission.

Bit	Name	Description
31:0	LAST_TSTP	Beacon timestamp. Lower 32 bits of timestamp of the last beacon received.

8.15.21 Current NAV (WMAC_PCU_NAV)

Offset: 0x18108084
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:26	RES	Reserved
25:0	CS_NAV	Current NAV value (in µs)

8.15.22 Successful RTS Count (WMAC_PCU_RTS_SUCCESS_CNT)

Offset: 0x18108088
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of successful RTS exchanges. The counter stops at 0xFFFF. After a read, automatically resets to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	RTS_OK	RTS/CTS exchange success counter

8.15.23 Failed RTS Count (WMAC_PCU_RTS_FAIL_CNT)

Offset: 0x1810808C
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of failed RTS exchanges. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	RTS_FAIL	RTS/CTS exchange failure counter

8.15.24 FAIL ACK Count (WMAC_PCU_ACK_FAIL_CNT)

Offset: 0x18108090
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of failed acknowledgements. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	ACK_FAIL	DATA/ACK failure counter

8.15.25 Failed FCS Count (WMAC_PCU_FCS_FAIL_CNT)

Offset: 0x18108094
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of failed frame check sequences. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	FCS_FAIL	FCS failure counter

8.15.26 Beacon Count (WMAC_PCU_BEACON_CNT)

Offset: 0x18108098
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of valid beacon frames received. The counter stops at 0xFFFF. After a read, automatically resets to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	BEACONCNT	Valid beacon counter

8.15.27 MAC PCU Sleep 1 (SLP1)

Offset: 0x181080D4
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

The Sleep 1 register in conjunction with the Sleep 2 (WMAC_PCU_SLP2) register, controls when the QCA9563 should wake when waiting for AP Rx traffic. Sleep registers are only used when the QCA9563 is in STA mode.

Bit	Name	Reset	Description
31:21	CAB_TIMEOUT	0x5	Time in 1/8 TU the PCU waits for CAB after receiving the beacon or the previous CAB; insures that if no CAB is received after the beacon or if a long gap occurs between CABs, CAB powersave state returns to idle.
20	RES	0x0	Reserved
19	ASSUME_DTIM	0x0	A mode bit which indicates whether to assume a beacon was missed when the SLP_BEACON_TIMEOUT occurs with no received beacons, in which case is assumes the DTIM was missed, and waits for CAB.
18:0	RES	0x0	Reserved

8.15.28 Sleep 2 (WMAC_PCU_SLP2)

Offset: 0x181080D8
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x2

Bit	Name	Description
31:21	BEACON_TIMEOUT	Time in 1/8 TU that the PCU waits for a beacon after waking up. If this time expires, the PCU woke due to SLP_NEXT_DTIM, and SLP_ASSUME_DTIM is active, then it assumes the beacon was missed and goes directly to watching for CAB. Otherwise when this time expires, the beacon powersave state returns to idle.
20:0	RES	Reserved

8.15.29 Address 1 Mask Lower 32 Bits (WMAC_PCU_ADDR1_MASK_L32)

Offset: 0x181080E0

Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0xFFFFFFFF

This STA register provides multiple BSSID support when the QCA9563 is in AP mode.

Bit	Name	Description
31:0	STA_MASK_L	STA address mask lower 32-bit register. Provides multiple BSSID support.

8.15.30 Address 1 Mask Upper 16 Bits (WMAC_PCU_ADDR1_MASK_U16)

Offset: 0x181080E4

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0xFFFF

This STA register provides multiple BSSID support when the QCA9563 is in AP mode.

Bit	Name	Description
31:16	RES	Reserved
15:0	STA_MASK_L	STA address mask upper 16-bit register. Provides multiple BSSID support.

8.15.31 Tx Power Control (WMAC_PCU_TPC)

Offset: 0x181080E8

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x3F

The 6-bit Tx power control sent from the MAC to the baseband is typically controlled using the Tx descriptor field. But self-generated response frames such as ACK, CTS, and chirp that do not have a Tx descriptor use the values in the Tx power control register instead.

Bit	Name	Description
31:30	RES	Reserved
29:24	RPT_PWR	Tx power control for self-generated action/NoACK frame
23:22	RES	Reserved
21:16	CHIRP_PWR	Tx power control for chirp
15:14	RES	Reserved
13:8	CTS_PWR	Tx power control for CTS
7:6	RES	Reserved
5:0	ACK_PWR	Tx power control for ACK

8.15.32 Tx Frame Counter (WMAC_PCU_TX_FRAME_CNT)

Offset: 0x181080EC

Access: Hardware = Read/Write
Software = Read/Write

Reset Value: 0x0

The Tx frame counter counts the number of cycles the TX_FRAME signal is active.

Bit	Name	Description
31:0	TX_FRAME_CNT	Counts the number of cycles the TX_FRAME signal is active

8.15.33 Rx Frame Counter (WMAC_PCU_RX_FRAME_CNT)

Offset: 0x181080F0

Access: Hardware = Read/Write
Software = Read/Write

Reset Value: 0x0

The receive frame counter counts the number of cycles the RX_FRAME signal is active.

Bit	Name	Description
31:0	RX_FRAME_CNT	Counts the number of cycles the RX_FRAME signal is active

8.15.34 Rx Clear Counter (WMAC_PCU_RX_CLEAR_CNT)

Offset: 0x181080F4

Access: Hardware = Read/Write
Software = Read/Write

Reset Value: 0x0

The receive clear counter counts the number of cycles the RX_CLEAR signal is not active.

Bit	Name	Description
31:0	RX_CLEAR_CNT	Counts the number of cycles the RX_CLEAR signal is low (not active)

8.15.35 Cycle Counter (WMAC_PCU_CYCLE_CNT)

Offset: 0x181080F8

Access: Hardware = Read/Write
Software = Read/Write

Reset Value: 0x0

The cycle counter counts the number of clock cycles.

Bit	Name	Description
31:0	CYCLE_CNT	Counts the number of clock cycles

8.15.36 Quiet Time 1 (WMAC_PCU_QUIET_TIME_1)

Offset: 0x181080FC

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: See field description

The Quiet Time registers implement the quiet time function specified in the proposed 802.11h extension supporting radar detection.

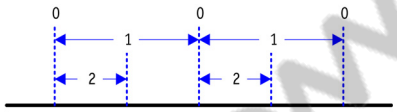
Bit	Name	Reset	Description
31:18	RES	0x0	Reserved
17	QUIET_ACK_CTS_ENABLE	0x1	If set, then the MAC sends an ACK or CTS in response to a received frame
16:0	RES	0x0	Reserved

8.15.37 Quiet Time 2 (WMAC_PCU_QUIET_TIME_2)

Offset: 0x18108100
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

The Quiet Time registers implement the quiet time function specified in the proposed 802.11h extension supporting radar detection.

NOTE QUIET_ENABLE is implemented as GENERIC_TIMER_ENABLE and NEXT_QUIET as GENERIC_TIMER_NEXT. QUIET_PERIOD is implemented as GENERIC_TIMER_PERIOD.



- 0 = NEXT_QUIET = TSF[31:0]
- 1 = QUIET_PERIOD
- 2 = QUIET_DURATION

(Chip remains awake during QUIET_DURATION)

Bit	Name	Description
31:16	QUIET_DURATION	The length of time in TUs (TU = 1024 µs) that the chip is required to be quiet
15:0	RES	Reserved

8.15.38 QoS NoACK (WMAC_PCU_QOS_NO_ACK)

Offset: 0x18108108
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x52

This register provides a mechanism to locate the NoACK information in the QoS field and determine which encoding means NoACK.

Bit	Name	Reset	Description	
31:9	RES	0x0	Reserved	
8:7	NOACK_BYTE_OFFSET	0x0	Number of bytes from the byte after end of the header of a data packet to the byte location where NoACK information is stored. (The end of the header is at byte offset 25 for 3-address packets and 31 for 4-address packets.)	
6:4	NOACK_BIT_OFFSET	0x5	Offsets from the byte where the NoACK information should be stored; offset can range from 0 to 6 only	
3:0	NOACK_2_BIT_VALUES	0x2	These values are of a two bit field that indicate NoACK	
			NOACK_2_BIT_VALUE	**Encoding Matching NoACK**
			xxx1	00
			xx1x	01
			x1xx	10
			1xxx	11

8.15.39 PHY Error Mask (WMAC_PCU_PHY_ERROR_MASK)

Offset: 0x1810810C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x2

NOTE Provides the ability to choose which PHY errors to filter from the BB; the number offsets into this register. If the mask value at the offset is 0, the error filters and does not show on the Rx queue.

Bit	Name	Description
31	ERROR CCK RESTART	CCK restart error
30	ERROR CCK SERVICE	CCK service error
29:28	RES	Reserved
27	ERROR CCK RATE_ILLEGAL	CCK illegal rate error
26	ERROR CCK HEADER_CRC	CCK CRC header error
25	ERROR CCK TIMING	False detection for CCK
24	RES	Reserved
23	ERROR OFDM RESTART	OFDM restart error
22	ERROR OFDM SERVICE	OFDM service error
21	ERROR OFDM POWER_DROP	OFDM power drop error
20	ERROR OFDM LENGTH_ILLEGAL	OFDM illegal length error
19	ERROR OFDM RATE_ILLEGAL	OFDM illegal rate error
18	ERROR OFDM SIGNAL_PARITY	OFDM signal parity error
17	ERROR OFDM TIMING	False detection for OFDM
16:8	RES	Reserved
7	ERROR TX_INTERRUPT_RX	Transmit interrupt
6	ERROR ABORT	Abort error
5	ERROR RADAR_DETECT	Radar detect error
4	ERROR PANIC	Panic error
3:1	RES	Reserved
0	ERROR TRANSMIT_UNDERRUN	Transmit underrun error

8.15.40 Rx Buffer (WMAC_PCU_RXBUF)

Offset: 0x18108114
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Reset	Description
31:12	RES	0x0	Reserved
11	REG_RD _ENABLE	0x0	When reading WMAC_PCU_BUF with this bit set, hardware returns the contents of the receive buffer.
10:0	HIGH_PRIORITY_ THRSHD	0x7FF	When number of valid entries in the receive buffer is larger than this threshold, the host interface logic gives the higher priority to receive side to prevent receive buffer overflow.

8.15.41 QoS Control (WMAC_PCU_MIC_QOS_CONTROL)

Offset: 0x18108118
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0xAA

Bit	Name	Description	
31:17	RES	Reserved	
16	MIC_QOS_ENABLE	Enable MIC QoS control	
		0	Disable hardware Michael
		1	Enable hardware Michael
15:14	MIC_QOS_CONTROL [7]	MIC QoS control [7]. See options for MIC_QOS_CONTROL [0], page 8-257.	
13:12	MIC_QOS_CONTROL [6]	MIC QoS control [6]. See options for MIC_QOS_CONTROL [0], page 8-257.	
11:10	MIC_QOS_CONTROL [5]	MIC QoS control [5]. See options for MIC_QOS_CONTROL [0], page 8-257.	
9:8	MIC_QOS_CONTROL [4]	MIC QoS control [4]. See options for MIC_QOS_CONTROL [0], page 8-257.	
7:6	MIC_QOS_CONTROL [3]	MIC QoS control [3]. See options for MIC_QOS_CONTROL [0], page 8-257.	
5:4	MIC_QOS_CONTROL [2]	MIC QoS control [2]. See options for MIC_QOS_CONTROL [0], page 8-257.	
3:2	MIC_QOS_CONTROL [1]	MIC QoS control [1]. See options for MIC_QOS_CONTROL [0], page 8-257.	
1:0	MIC_QOS_CONTROL [0]	MIC QoS control [0]	
		0	Use 0 when calculating Michael
		1	Use 1 when calculating Michael
		2	Use MIC_QOS_SELECT when calculating Michael
		3	Use inverse of MIC_QOS_SELECT when calculating Michael

8.15.42 Michael QoS Select (WMAC_PCU_MIC_QOS_SELECT)

Offset: 0x1810811C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x3210

Bit	Name	Description
31:28	MIC_QOS_SELECT [7]	MIC QoS select [7]. Select the OOS TID bit when calculating Michael.
27:24	MIC_QOS_SELECT [6]	MIC QoS select [6]. Select the OOS TID bit when calculating Michael.
23:20	MIC_QOS_SELECT [5]	MIC QoS select [5]. Select the OOS TID bit when calculating Michael.
19:16	MIC_QOS_SELECT [4]	MIC QoS select [4]. Select the OOS TID bit when calculating Michael.
15:12	MIC_QOS_SELECT [3]	MIC QoS select [3]. Select the OOS TID bit when calculating Michael.
11:8	MIC_QOS_SELECT [2]	MIC QoS select [2]. Select the OOS TID bit when calculating Michael.
7:4	MIC_QOS_SELECT [1]	MIC QoS select [1]. Select the OOS TID bit when calculating Michael.
3:0	MIC_QOS_SELECT [0]	MIC QoS select [0]. Select the OOS TID bit when calculating Michael.

8.15.43 Miscellaneous Mode (WMAC_PCU_MISC_MODE)

Offset: 0x18108120
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Reset	Description
31:30	RES	0x0	Reserved
29	USE_EOP_PTR_ FOR_DMA_WR	0x0	When this bit is set, use LAST_EOP_PTR as an indication for DMA write When this bit is clear, use RD_PTR_TO_DMA instead.
28	ALWAYS_ PERFORM_KEY_ SEARCH	0x0	If this bit is set, key search is performed for every frame in an aggregate. If this bit is cleared, key search is only performed for the first frame of an aggregate. Unless the transmitter address is different between the frames in an aggregate. This bit has no effect on non-aggregate frame packets.
27	SEL_EVM	0x1	If set, the EVM field of the Rx descriptor status contains the EVM data received from the BB. If cleared, the EVM field of the Rx descriptor status contains 3 bytes of Legacy PLCP, 2 service bytes, and 6 bytes of HP PLCP.
26	CLEAR_BA_VALID	0x0	If set, the state of the block ACK storage is invalidated.
25	CLEAR_FIRST_HCF	0x0	If the CLEAR_FIRST_HCF bit is set then the FIRST_HCF state will be cleared. This should be set to enter fast channel change mode and cleared once fast channel change is over.
24	CLEAR_VMF	0x0	If the CLEAR_VMF bit is set then the VMF mode in the transmit state machine will be cleared. This should be set to enter fast channel change mode and cleared once fast channel change is over.
23	RX_HCF_POLL_ ENABLE	0x1	If the RX_HCF_POLL_ENABLE bit is set then the MAC is enabled to receive directed HCF polls. If this bit is not set the receive state machine will not tell the rest of the MAC that it has received a directed HCF poll.
22	HCF_POLL_ CANCELS_NAV	0x1	If the HCF_POLL_CANCELS_NAV bit is set, when a directed HCF poll is received, the current NAV is cancelled and HCF data burst can proceed at SIFS.
21	TBTT_PROTECT	0x1	If set, then the time from TBTT to 20 μs after TBTT is protected from transmit. Turn this off in ad hoc mode or if this MAC is used in the AP.
20:19	RES	0x0	Reserved
18	FORCE_QUIET_ COLLISION	0x0	If set, the PCU thinks that it is in quiet collision period, kills any transmit frame in progress, and prevents any new frame from starting.
17:15	RES	0x0	Reserved
14	MISS_BEACON_IN_ SLEEP	0x1	If the MISS_BEACON_IN_SLEEP bit is set, the missed beacon logic will not clear the missed beacon count when the chip is in sleep.
13	RES	0x0	Reserved
12	TXOP_TBTT _LIMIT_ENABLE	0x0	If this limit is set, then logic to limit the value of the duration to fit the time remaining in TXOP and time remaining until TBTT is turned on. This logic will also filter frames, which will exceed TXOP.
11	KC_RX_ANT	0x1	If KC_RX_ANT_UPDATE bit is set, the transmit antenna information in the key cache is updated based on the receive antenna results from baseband. Updates only occur when the selected antenna does not match the requested antenna which only occurs when the receive diversity is turned on in the baseband. This bit is only used with the dual chain antenna feature. The DUAL_CHAIN_ANT_MODE needs to be set to enable the KC_RX_ANT_ UPDATE.
10:6	RES	0x0	Reserved

Bit	Name	Reset	Description
5	RXSM2SVD_PRE_RST	0x0	If set to high when packets are received, SVD is always reset.
4	CCK_SIFS_MODE	0x0	If set, the chip assumes that it is using 802.11g mode where SIFS is set to 10 μs and non-CCK frames must add 6 to SIFS to make it CCK frames. This bit is needed in duration calculation, as is the SIFS_TIME register.
3	TX_ADD_TSF	0x0	If the TX_ADD_TSF bit is set, the TSF in the transmit packet will be added to the internal TSF value for transmit beacons and prob_response frames.
2	MIC_NEW_LOCATION_ENABLE	0x0	If MIC_NEW_LOCATION_ENABLE is set, the Tx Michael Key is assumed to be co-located in the same entry where the Rx Michael key is.
1	RES	0x0	Reserved
0	BSSID_MATCH_FORCE	0x0	If the BSSID_MATCH_FORCE bit is set, all logic based on matching the BSSID thinks that the BSSID matches.

8.15.44 Filtered OFDM Counter (WMAC_PCU_FILTER_OFDM_CNT)

Offset: 0x18108124
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

The filtered OFDM counters use the MIB control signals.

Bit	Name	Description
31:24	RES	Reserved
23:0	FILTOFDM_CNT	Counts the OFDM frames that were filtered using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. PIB MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

8.15.45 Filtered CCK Counter (WMAC_PCU_FILTER_CCK_CNT)

Offset: 0x18108128
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	RES	Reserved
23:0	FILTCCK_CNT	Counts the CCK frames that were filtered using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. PIB MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

8.15.46 PHY Error Counter 1 (WMAC_PCU_PHY_ERR_CNT_1)

Offset: 0x1810812C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

The PHY error counters count any PHY error matching the respective mask. The bits of 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to provide flexibility in counting. For example, if setting the mask bits to 0xFF0000FF, then all PHY errors from 0-7 and 24-31 are counted.

Bit	Name	Description
31:24	RES	Reserved
23:0	PHY_ERROR_CNT1	Counts any PHY error1 using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. PIB MIB forces incrementation of all registers in each cycle. Counter saturates at the highest value and is writable. If the upper two counter bits are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

8.15.47 PHY Error Counter 1 Mask (WMAC_PCU_PHY_ERR_CNT_1_MASK)

Offset: 0x18108130
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PHY_ERROR_CNT_MASK1	Counts any error that matches the PHY error1 mask. The values of any 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to allow counting flexibility (e.g., setting the mask to 0xFF0000FF means all PHY errors from [7:0] and [31:24] are counted).

8.15.48 PHY Error Counter 2 (WMAC_PCU_PHY_ERR_CNT_2)

Offset: 0x18108134
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	RES	Reserved
23:0	PHY_ERROR_CNT	Counts any error that matches the PHY error2 mask. The values of any 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to allow counting flexibility (e.g., setting the mask to 0xFF0000FF means all PHY errors from 0:7 and 24:31 are counted).

8.15.49 PHY Error Counter 2 Mask (WMAC_PCU_PHY_ERR_CNT_2_MASK)

Offset: 0x18108138

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:0	PHY_ ERROR_ CNT_MASK2	Counts any PHY error2 using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all values of these registers. PIB MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted, generating an interrupt.

8.15.50 TSF Threshold (WMAC_PCU_TSF_THRESHOLD)

Offset: 0x1810813C

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0xFFFF

Bit	Name	Description
31:16	RES	Reserved
15:0	TSF_THRESHOLD	Asserts the PCU_TSF_OUT_OF_RANGE_INTER if the corrected receive TSF in a beacon is different from the internal TSF by more than this threshold.

8.15.51 PHY Error EIFS Mask (WMAC_PCU_PHY_ERROR_EIFS_MASK)

Offset: 0x18108144

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:0	VALUE	This mask provides the ability to choose which PHY errors from the baseband cause EIFS delay. The error number is used as an offset into this mask. If the mask value at the offset is 1, then this error will not cause EIFS delay.

8.15.52 PHY Error Counter 3 (WMAC_PCU_PHY_ERR_CNT_3)

Offset: 0x18108168

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:24	RES	Reserved
23:0	PHY_ERROR_CNT3	Count of PHY errors that pass the PHY_ERR_CNT_3_MASK filter

8.15.53 PHY Error Counter 3 Mask (WMAC_PCU_PHY_ERR_CNT_3_MASK)

Offset: 0x1810816C

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:0	PHY_ERROR_CNT_MASK3	Mask of the PHY error number allowed to be counted

8.15.54 MAC PCU Generic Timers 2 (WMAC_PCU_GENERIC_TIMERS2)

Offset: 0x18108180
Access: Read/Write
Reset Value: Undefined

Bit	Name	Description
31:0	DATA	WMAC_PCU_GENERIC_TIMERS

8.15.55 MAC PCU Generic Timers Mode 2 (WMAC_PCU_GENERIC_TIMERS2_MODE)

Offset: 0x181081C0
Access: See field description
Reset Value: Undefined

Bit	Name	Access	Description
31:11	RES	RO	Reserved
10:8	OVERFLOW_INDEX	RO	Overflow index
7:0	ENABLE	RW	Enable

8.15.56 SIFS, Tx Latency and ACK Shift (WMAC_PCU_TXSIFS)

Offset: 0x181081D0
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description	
31:15	RES	Reserved	
14:12	ACK_SHIFT	ACK_SHIFT is used to generate the ACK_TIME, which is used to generate the ACK_ SIFS_TIME. The ACK_TIME table in the hardware assumes a channel width of 2.5 MHz. This value should be 3 for CCK rates.	
		0	2.5 MHz
		1	5 MHz
		2	10 MHz (11j)
		3	20 MHz 802.11g
		4	40 MHz (turbo mode)
11:8	TX_LATENCY	TX_LATENCY is the latency in µs from TX_FRAME being asserted by the MAC to when the energy of the frame is on the air. This value is used to decrease the time to TBTT and time remaining in TXOP in the calculation to determine quiet collision.	
7:0	SIFS_TIME	SIFS_TIME is the number of µs in SIFS.	

8.15.57 TXOP for Non-QoS Frames (WMAC_PCU_TXOP_X)

Offset: 0x181081EC
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:8	RES	Reserved
7:0	SIFS_TIME	TXOP in units of 32 µs. A TXOP value exists for each QoS TID value. When a new burst starts, the TID is used to select one of the 16 TXOP values. This TXOP decrements until the end of the burst to make sure that the packets are not sent out by the time TXOP expires. This register is used for legacy non QoS frames.

8.15.58 TXOP for TID 0 to 3 (WMAC_PCU_TXOP_0_3)

Offset: 0x181081F0
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_3	Value in units of 32 µs
23:16	VALUE_2	Value in units of 32 µs
15:8	VALUE_1	Value in units of 32 µs
7:0	VALUE_0	Value in units of 32 µs

8.15.59 TXOP for TID 4 to 7 (WMAC_PCU_TXOP_4_7)

Offset: 0x181081F4
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_7	Value in units of 32 µs
23:16	VALUE_6	Value in units of 32 µs
15:8	VALUE_5	Value in units of 32 µs
7:0	VALUE_4	Value in units of 32 µs

8.15.60 TXOP for TID 8 to 11 (WMAC_PCU_TXOP_8_11)

Offset: 0x181081F8
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_11	Value in units of 32 µs
23:16	VALUE_10	Value in units of 32 µs
15:8	VALUE_9	Value in units of 32 µs
7:0	VALUE_8	Value in units of 32 µs

8.15.61 TXOP for TID 0 to 3 (WMAC_PCU_TXOP_12_15)

Offset: 0x181081FC
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_15	Value in units of 32 µs
23:16	VALUE_14	Value in units of 32 µs
15:8	VALUE_13	Value in units of 32 µs
7:0	VALUE_12	Value in units of 32 µs

8.15.62 Generic Timers (WMAC_PCU_GENERIC_TIMERS[0:15])

Offset: 0x18108200
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Address	Default	Description
0x8200–0x821C	0x0	GENERIC_TIMER_NEXT
0x8220–0x823C	0x0	GENERIC_TIMER_PERIOD

NOTE GENERIC _TIMER_0, unlike other generic timers, does not wake the MAC before timer expiration and its overflow mechanism does not generate an interrupt. Instead, it silently adds this period repeatedly until the next timer advances past the TSF. Thus when MAC wakes after sleeping for multiple TBTTs, the TGBTT does not assert repeatedly or cause the beacon miss count to jump.

Generic Timer	Function
0	TBTT
1	DMA beacon alert
2	SW beacon alert
3	Reserved
4	NEXT_TIM
5	NEXT_DTIM
6	Quiet time trigger
7	No dedicated function

8.15.63 Generic Timers Mode (WMAC_PCU_GENERIC_TIMERS_MODE)

Offset: 0x18108240
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: See Field Description

Bit	Name	Reset	Description
31:12	THRESH	0x100	Number of µs that generate a threshold interrupt if exceeded in TSF comparison
11	RES	0x0	Reserved
10:8	OVERFLOW_INDEX	UND	Indicates the last generic timer that overflowed
7:0	ENABLE	0x0	Timer enable

8.15.64 32 KHz Sleep Mode (WMAC_PCU_SLP32_MODE)

Offset: 0x18108244
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Reset	Description
31:25	RES	0x0	Reserved
24	TSF2_WRITE_ STATUS	0x1	This bit has the same function as TSF_WRITE_STATUS but this bit is the indication for TSF2.
23	FORCE_BIAS_ BLOCK_ON	0x0	When set, indicates that the Bias block is turned on and generating the reference current for PCIE PHY.
22	DISABLE_32KHZ	0x0	Indicates the 32 KHz clock is not used to control the TSF, but the MAC clock increments the TSF. Only used on AP class devices that do not go to sleep.
21	TSF_WRITE_STATUS	0x1	Since it takes such a long time to write the TSF, the effect of the TSF change may not occur until 10 μsec intervals after the write. Make sure that the write completes before the next read/write of the TSF is initiated. If the data is not stale, it may be read out. The SLEEP32_TSF_WRITE_STAT if set indicates that a configuration write or TSF reset (see register BEACON_PERIOD 0x8020) is in progress. Immediately after writing or resetting the TSF, this bit should be set between 15 to 45 μsec. If it does not get set, it may be because the TSF is being updated from a receive beacon and the writing or reset of the TSF will be lost. This is a read only register.
20	ENABLE	0x1	When set, indicates that the TSF should be allowed to increment on its own
19:0	HALF_CLK_LATENCY	0xF424	Defines the time in μsec from the detection of the falling edge of the 32 KHz clock to the rising edge of the 32 KHz clock. Whenever the TSF is updated by the configuration interface or by a receive beacon, the time in μsec is incremented until the falling edge of the 32 KHz clock then this time is added to the value of this register and is then is used to update the TSF. Since the 32 KHz clock is slow, if this modification is not done, the TSF will be off by 10s of μsecs. When there is no 32 KHz crystal the edges will be separated by 15.250 μsec which corresponds to the HALK_CLK_ LATENCY of 0xF400 for a 40 MHz reference clock.

8.15.65 32 KHz Sleep Wake (WMAC_PCU_SLP32_WAKE)

Offset: 0x18108248
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x800

Bit	Name	Description
31:16	RES	Reserved
15:0	XTL_TIME	Time in μs before a generic timer should expire that the wake signal asserts to the crystal wake logic. Add an extra 31 μs due to 32 KHz clock resolution.

8.15.66 32 KHz Sleep Increment (WMAC_PCU_SLP32_INC)

Offset: 0x1810824C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x1E848

Bit	Name	Description
31:20	RES	Reserved
19:0	TSF_INC	Time in $1/2^{12}$ of a µs the TSF increments on the rising edge of the 32 KHz clk (30.5176 µs period). The upper 8 bits are at µs resolution. The lower 12 bits are the fractional portion. 1 unit = X / 1/212 ms = 30.5176 ms Where *X* = 125000, or 0x1E848 is the default setting for 32.768 MHz clock. The TSF_INC value needs to be programmed differently if there is no 32.768 KHz crystal and the 32 KHz clock is approximated using the 40 MHz reference clock. This is actually a more common system configuration. The closest to 30.5176 µsec using a divider on a 40 MHz reference clock is 30.500 µsec which corresponds to TSF_INC of 0x1E800. The HALF_CLK_LATENCY will then be 15.250 µsec which corresponds to 0x0F400.

8.15.67 Sleep MIB Sleep Count (WMAC_PCU_SLP_MIB1)

Offset: 0x18108250
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	SLEEP_CNT	Counts the number of 32 KHz clock cycles that the MAC has been asleep

8.15.68 Sleep MIB Cycle Count (WMAC_PCU_SLP_MIB2)

Offset: 0x18108254
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

The SLEEP_CNT counts the number of 32 KHz clock cycles that the MAC has been asleep. The CYCLE_CNT counts the absolute number of 32 KHz clock cycles. When the CYCLE_CNT bit 31 is 1, the MIB interrupt will be asserted. The SLEEP_CNT and CYCLE_CNT are saturating counters when the value of CYCLE_CNT reaches 0xFFFF_FFFF both counters will stop incrementing. The CLR_CNT will clear both the SLEEP_CNT and CYCLE_CNT. During the time that the clearing of these register are pending the PENDING will be asserted. SLEEP_CNT, CYCLE_CNT, and CLR_CNT are writable for diagnostic purposes. Before every read/write, the PENDING bit should be polled to verify any pending write has cleared.

Bit	Name	Description
31:0	CYCLE_CNT	Counts the absolute number of 32KHz clock cycles. When CYCLE_CNT bit 31 is 1, the MIB interrupt will be asserted. SLEEP_CNT and CYCLE_CNT are saturating counters when the value of CYCLE_CNT reaches 0xFFFF_FFFF both counters will stop incrementing.

8.15.69 Sleep MIB Control Status (WMAC_PCU_SLP_MIB3)

Offset: 0x18108258
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0
See Sleep MIB Cycle Count (WMAC_PCU_SLP_MIB2).

Bit	Name	Description
31:2	RES	Reserved
1	PENDING	SLEEP_CNT, CYCLE_CNT, and CLR_CNT are writable for diagnostic purposes. Before every read/write, the pending bit should be polled to verify any pending write has cleared.
0	CLR_CNT	CLR_CNT clears both SLEEP_CNT and CYCLE_CNT. Pending is asserted while the clearing of these registers is pending.

8.15.70 1 µS Clocks (1µS)

Address: 0x18108284
Access: Read/Write
Reset: See field description

This register sets the number of clocks in one micro-second. See Sleep MIB Sleep Count (WMAC_PCU_SLP_MIB1) for more information.

Bit	Bit Name	Reset	Description
31:7	RES	0x0	Reserved
6:0	SCALER	0x2C	The number of MAC clocks in one µs

8.15.71 PHY Error Counter Continued (PHY_ERR_CNT_MASK_CONT)

Address: 0x1810829C
Access: Read/Write
Reset: 0x0

This register is the MAC PCU PHY error counter 1, 2, and 3 continued. See PHY Error Counter 1 (WMAC_PCU_PHY_ERR_CNT_1).

Bit	Bit Name	Description
31:24	RES	Reserved

23:16	MASK3	Mask for PHY error count #1 for PHY errors 35 to 32 which correspond to the MASK3 bits 39 to 32. PHY errors above 39 will not be counted.
15:8	MASK2	Mask for PHY error count #1 for PHY errors 39 to 32 which correspond to the MASK3 bits 39 to 32. PHY errors above 39 will not be counted.
17:0	MASK1	Mask for PHY error count #1 for PHY errors 39 to 32 which correspond to the MASK3 bits 39 to 32. PHY errors above 39 will not be counted.

8.15.72 Global Mode (WMAC_PCU_20_40_MODE)

Offset: 0x18108318

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

MAC PCU global mode register. There are only 4 allowable modes of operation:
A: Current HT2040 joined mode.
B: Current static HT20 mode.
C: Spec compliant mode.
D: Spec compliant but HT20 can Tx even when extension channel is busy mode.

Bit	Name	Description
31:16	RES	Reserved
15:4	PIFS_CYCLES	When EXT_PIFS_ENABLE is enabled, the PIFS_CYCLES register needs to be set to the appropriate value. In 11g mode PIFS is 10 μsec for SIFS and 9 μsec for slot. This register defines the number of clock cycles per PIFS. For HT2040 mode the number of cycles should be 1672 for 11g mode. For HT20 mode the number of cycles should be 836 for 11g mode.
3	SWAMPED_ FORCES_RX_ CLEAR_CTL_IDLE	Indicates that the baseband sees a strong signal on the extension channel and a weak signal on the control channel. This is likely caused by a transmitter on the extension channel that is so close that the spectral leakage onto the control channel is strong enough to cause RX_CLEAR on the control channel to indicate a busy signal.
2	TX_HT20_ON_ EXT_BUSY	When set, HT20 frames are permitted to be transmitted even when the extension channel has not been idle for PIFS. In fact it is permitted to transmit even if the extension channel is busy as long as the control channel is idle. The HT40 frames still depend on being idle for PIFS. This mode should only be enabled when capable of meeting the spectral mask requirement on the extension channel. To use this bit the JOINED_RX_CLEAR bit must be clear.
1	EXT_PIFS_ ENABLE	Enables the chips to be 802.11n compliant. The JOINED_RX_CLEAR must be clear to use this mode. When this bit is set, only the control channel RX_CLEAR is used to count down backoff. The only time that the extension channel is consulted is immediately prior to transmitting a frame. The PCU verifies that the extension channel has been clear for at least PIFS. See also PIFS_CYCLES register.
0	JOINED_RX_ CLEAR	Setting this bit causes the RX_CLEAR used in the MAC to be the AND of the control channel RX_CLEAR and the extension channel RX_CLEAR. If this bit is clear then the MAC will use only the control channel RX_CLEAR.

8.15.73 Difference RX_CLEAR Counter (WMAC_PCU_RX_CLEAR_ DIFF_CNT)

Offset: 0x18108328

Access: Hardware = Read-Only
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:0	RX_CLEAR_DIFF_ CNT	A cycle counter MIB register. On every cycle of the MAC clock, this counter increments every time the extension channel RX_CLEAR is low when the MAC is not actively transmitting or receiving. Due to a small lag between TX_FRAME and RX_CLEAR as well as between RX_CLEAR and RX_FRAME, the count may have some residual value even when no activity is on the extension channel.

8.15.74 Self Generated Antenna Mask (SELF_GEN_ANTENNA_ MASK)

Address: 0x1810832C
Access: Read/Write
Reset: See field description

The antenna mask normally comes from the transmit descriptor. For self generated frames, this register provides the antenna mask to the baseband via the MAC/baseband interface.

Bit	Bit Name	Reset	Description
31:5	RES	0x0	Reserved
4	FORCE_CHAIN	0x0	Forces the SELF_GEN frame to be sent by chain 0 when location mode is on
3	ONE_RESP_EN	0x1	Forces the SELF_GEN frame to be sent by only one antenna when location mode is on
2:0	VALUE	0x7	

8.15.75 Control Registers for Block BA Control Fields (WMAC_PCU_ BA_BAR_CONTROL)

Offset: 0x18108330
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

The MAC PCU control registers for block BA control fields. The antenna mask normally comes from the transmit descriptor. For self generated frames, this register will provide the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Reset	Description
31:13	RES	0x0	Reserved
12	UPDATE_BA_BITMAP _QOS_NULL	0x0	When set, it enables the update of BA_BITMAP on a QoS Null frame
11	TX_BA_CLEAR_BA _VALID	0x0	When set, enables the BA_VALID bits to be cleared upon transmit of the block ACK for an aggregate frame or on receiving a BAR
10	FORCE_NO_MATCH	0x0	Causes the BA logic to never find a match of previous saved bitmap in the memory
9	ACK_POLICY_VALUE	0x1	The value of the ACK policy bit
8	COMPRESSED_VALUE	0x1	The value of the compressed bit
7:4	ACK_POLICY_OFFSET	0x0	Indicates the bit offset in the block ACK or block ACK request control field which defines the location of the ACK policy bit.
3:0	COMPRESSED_ OFFSET	0x2	Indicates the bit offset in the block ACK or block ACK request control field which defines the location of the COMPRESSED bit.

8.15.76 Legacy PLCP Spoof (WMAC_PCU_LEGACY_PLCP_SPOOF)

Offset: 0x18108334
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

The MAC PCU legacy PLCP spoof. The antenna mask normally comes from the transmit descriptor. For self generated frames, this register will provide the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Reset	Description
31:13	RES	0x0	Reserved
12:8	MIN_LENGTH	0xE	Defines the minimum spoofed legacy PLCP length
7:0	EIFS_MINUS _DIFS	0x0	Defines the number of μs to be subtracted from the transmit packet duration to provide fairness for legacy devices as well as HT devices.

8.15.77 PHY Error Mask and EIFS Mask (WMAC_PCU_PHY_ERROR_ MASK_CONT)

Offset: 0x18108338
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

MAC PCU PHY error mask and EIFS mask continued. The antenna mask normally comes from the transmit descriptor. For self-generated frames, this register will provide the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Description
31:24	AIFS_VALUE	This is a continuation of register MAC_PCU_PHY_ERROR_AIFS_MASK_VALUE. Bits [31] to [24] correspond to PHY errors 39 to 32. All others PHY errors above 39 will cause AIFS delay. Currently the baseband does not generate PHY errors above 39
23:16	EIFS_VALUE	Continuation of PHY Error Counter 1 Mask (WMAC_PCU_PHY_ERR_CNT_1_MASK), page 8-260. Bits [2], [1], and [0] correspond to PHY errors 34, 33, and 32. All PHY errors above 39 cause EIFS delay.
15:8	RES	Reserved
7:0	MASK_VALUE	Continuation of PHY Error Counter 1 Mask (WMAC_PCU_PHY_ERR_CNT_1_MASK), page 8-260. Bits [2], [1], and [0] correspond to PHY errors 34, 33, and 32. All PHY errors above 39 are filtered.

8.15.78 Tx Timer (WMAC_PCU_TX_TIMER)

Offset: 0x1810833C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: See field description

The MAC PCU transmit timer. The antenna mask normally comes from the transmit descriptor. For self-generated frames, this register provides the antenna mask to the baseband via the MAC/baseband interface.

Bit	Name	Reset	Description
31:26	RES	0x0	Reserved
25	QUIET_TIMER_ ENABLE	0x1	The quiet timer is enabled when this bit is set to 1.
24:20	QUIET_TIMER	0x4	This timer is used to guarantee the transmit frame does not take less time than the values programmed in this timer in case a quiet collision occurs. The unit for this timer is μsecs.
19:16	RIFS_TIMER	0x0	This timer defines the RIFS interval in the unit of μsecs
15	TX_TIMER_ ENABLE	0x0	Enabled when this bit is set to 1
14:0	TX_TIMER	0x0	Guarantees the transmit frame does not take more time than the values programmed in this timer. The unit for this timer is in μsecs.

8.15.79 Alternate AES QoS Mute Mask (ALT_AES_MUTE_MASK)

Address: 0x18108348
Access: Read/Write
Reset: See field description

The antenna mask normally comes from the transmit descriptor. For self-generated frames, this register will provide the antenna mask to the baseband via the MAC/baseband interface.

Bit	Bit Name	Reset	Description
31:16	QOS	0x008F	Used to mask off sections of the MAC header for use in the AES algorithm. The QoS control fields are bytes 25 and 26 of the three-address frame and bytes 31 and 32 of the 4 address frame. This alternate QoS mute mask is needed to support changes in 802.11n related to the setting the mask of bit 7 of the QoS field. For APs, the client device must allow selection of the QoS mute mask. Some may support this new mute mask and others will not.
15:0	RES	0x0	Reserved

8.15.80 TSF 2 Lower 32 (TSF2_L32)

Address: 0x18108390
Access: Read/Write
Reset: See field description

This register holds the lower 32 bits of the MAC PCU TSF2.

Bit	Bit Name	Reset	Description
31:0	VALUE	0xFFFFFFF	Same function as TSF and added support for dual BSSID/TSF which is needed for DirectConnect or Mesh networking

8.15.81 TSF 2 Upper 32 (TSF2_U32)

Address: 0x18108394
Access: Read/Write
Reset: See field description

This register holds the upper32 bits of the MAC PCU TSF2.

Bit	Bit Name	Reset	Description
31:0	VALUE	0xFFFFFFF	The upper 32 bits of the local clock

8.15.82 BSSID 2 Upper 16 (BSSID2_U16)

Address: 0x1810839C
Access: Read/Write
Reset: 0x0

This register holds the upper 16 bits of the MAC PCU BSSID2.

Bit	Bit Name	Description
31:17	RES	Reserved
16	ENABLE	Enables BSSID2
15:0	ADDR	The upper 16 bits of BSSID2 (PCU_BSSID2[47:32])

8.15.83 TID Value Access Category (WMAC_PCU_TID_TO_AC)

Offset: 0x181083A4
Access: Read/Write
Reset Value: 0x0

Bit	Name	Description	
31:0	DATA	Maps the 16 user priority TID values to corresponding access category (AC). Two bits denote the AC for each TID. Bits [1:0] define the AC for TID 0 and next two bits are used for AC of TID 1, and finally bits [31:30] define the AC for TID 15. Default values are as specified in the 11e specification: TID 1 and 2 are BK, TID 0 and 3 are BK, TID 4 and 5 are VI, and TID 6 and 7 are V0. ACs:	
		00	BE
		01	BK
		10	VI
		11	VO

8.15.84 High Priority Queue Control (WMAC_PCU_HP_QUEUE)

Offset: 0x181083A8
Access: Read/Write
Reset Value: 0x0

Bit	Name	Reset	Description
31:23	RES	0x0	Reserved
22	NON_UAPSD_EN	0x1	If this bit is not set, only frames from UAPSD enabled devices having power management changes are placed into the HP QUEUE on power management change. Otherwise, all frames with power management changes are placed into the HP QUEUE. This bit is valid only if PM_ CHANGE bit is 1
21	PM_CHANGE	0x1	Place all frames which have power management state changes of a station into the HP QUEUE
20	UAPSD_EN	0x0	Enable detection and reporting in the Rx status of the UAPSD trigger frames and enable update of the PowerMgt bit in the key cache on error-free Rx-directed frames. If UAPSD enable is set for the AC of an error-free Rx directed QoS frame with the power management bit set, and the key cache entry of the sender has the PowerMgt bit set, it will be detected as a UAPSD trigger.
19:16	FRAME_SUBTYPE_ MASK0	0x0	Frame subtype mask for FRAME_SUBTYPE0, to be matched for the frame to be placed in high priority receive queue
15:12	FRAME_SUBTYPE0	0x0	Frame sub type to be matched for the frame to be placed in high priority receive queue
11:10	FRAME_TYPE_MASK0	0x3	Frame type mask for FRAME_TYPE0, to be matched for the frame to be placed in high priority receive queue
9:8	FRAME_TYPE0	0x0	Frame type to be matched for the frame to be placed in high priority receive queue
7	FRAME_BSSID_ MATCH0	0x0	If set to 1, frames with matching BSSID are only moved to high priority receive queue on a frame type match
6	FRAME_FILTER_ ENABLE0	0x0	Enables the mode where a frame is moved to high priority receive queue based on frame type
5	HPQON_UAPSD	0x0	Set to 1 if the Rx UAPSD trigger frame must be placed in the high priority Rx queue. Any frame that has a STA power management state change is also placed in the HP queue. HPQON_UAPSD = 1 with UAPSD_EN = 0 is not supported.
4	AC_MASK_VO	0x0	Set to 1 if BK traffic needs to be placed in high priority Rx queue
3	AC_MASK_VI	0x0	Set to 1 if VI traffic needs to be placed in high priority Rx queue
2	AC_MASK_BK	0x0	Set to 1 if BK traffic needs to be placed in high priority Rx queue
1	AC_MASK_BE	0x0	Set to 1 if BE traffic needs to be placed in high priority Rx queue
0	ENABLE	0x0	Enables high priority Rx queue

8.15.85 Hardware Beacon Processing 1 (HW_BCN_PROC1)

Address: 0x181083C8
Access: Read/Write
Reset: 0x0

This register is for Hardware Beacon Processing register 1.

Bit	Bit Name	Description
31:24	ELM2_ID	Element ID 2
23:16	ELM1_ID	Element ID 1
15:8	ELM0_ID	Element ID 0
7	EXCLUDE_ELM2	Exclude information with element ID ELM2 in CRC calculations
6	EXCLUDE_ELM1	Exclude information with element ID ELM1 in CRC calculations
5	EXCLUDE_ELM0	Exclude information with element ID ELM0 in CRC calculations
4	EXCLUDE_TIM_ELM	Exclude beacon TIME element in CRC calculations
3	EXCLUDE_CAP_INFO	Exclude beacon capability information in CRC calculations
2	EXCLUDE_BCN_INTVL	Exclude beacon intervals in CRC calculations
1	RESET_CRC	Reset the last beacon CRC calculated
0	CRC_ENABLE	Enables hardware beacon processing

8.15.86 Hardware Beacon Processing 2 (HW_BCN_PROC2)

Address: 0x181083CC
Access: Read/Write
Reset: See field description

This register is for Hardware Beacon Processing register 2.

Bit	Bit Name	Reset	Description
31:24	RES	0x0	Reserved
23:16	ELM3_ID	0x0	Element ID 3
15:8	FILTER_INTERVAL	0x2	Filter interval for beacons
7:3	RES	0x0	Reserved
2	EXCLUDE_ELM3	0x0	Exclude information with element ID ELM3 in CRC calculations
1	RESET_INTERVAL	0x0	Reset internal interval counter
0	FILTER_INTERVAL_ENABLE	0x0	Enable filtering beacons based on filter intervals

8.15.87 Key Cache (WMAC_PCU_KEY_CACHE[0:1023])

Offset: 0x18108800
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Table 8-17 Offset to First Dword of *N*th Key [1]

Intra Key	Offset Bits	Description	
8*N* + 00	31:0	Key[31:0]	
8*N* + 04	15:0	Key[47:32]	
8*N* + 08	31:0	Key[79:48]	
8*N* + 0C	15:0	Key[95:79]	
8*N* + 10	31:0	Key[127:96]	
8*N* + 14	14:3	Reserved	
	9	Power Mgt bit of last error-free directed Rx frame (only if UAPSD = 1)	
	8:5	UAPSD mask for the four ACs.	
		8	UAPSD enabled for BE
		7	UAPSD enabled for BK
		6	UAPSD enabled for VI
		5	UAPSD enabled for VO
	2:0	Key type:	
		0	40b
		1	104b
		2	TKIP without MIC
		3	128b
		4	TKIP
		5	Reserved
		6	AES_CCM
		7	Do nothing
8*N* + 18	31:0	Addr[32:1]	
8*N* + 1C	17:16	Key ID for multicast keys	
	15	Key valid	
		0	Entry has multi/broadcast key
		1	Entry has unicast key
	14:0	Addr[47:33]	

1. Key = (Address: 8800 + 20 * *N*)

When the key type is 4 (TKIP) and key is valid, this entry + 64 contains the Michael key. TKIP keys may not reside in the entries 64-127 because they require the Michael key. Entries 64-67 are always reserved for Michael.

Table 8-18 Offset to First Dword of *N*th Key (Continued)

Intra Key	Offset Bits	Description
8*N + 800	31:0	Rx Michael Key 0
8*N + 804	15:0	Tx Michael Key 0 [31:16]
8*N + 808	31:0	Rx Michael Key 1
8*N + 80C	15:0	Tx Michael Key 0 [15:0]
8*N + 810	31:0	Tx Michael Key 1
8*N + 814	RES	Reserved
8*N + 818	RES	Reserved
8*N + 81C	RES	Reserved
	15	Key Valid = 0

NOTE Internally the memory is 50 bits wide, thus writing a line of the memory requires two 32-bit writes. All writes to registers with an offset of 0x0 or 0x8 actually write to a temporary holding register. A write to registers with an offset of 0x4 or 0xC writes to memory.

8.16 PLL SRIF Registers

Table 8-19 summarizes the PLL SRIF registers.

Table 8-19 PLL SRIF Registers

Offset				Name	Page
Baseband	CPU	PCIE	DDR		
0x18116180	0x18116F00	0x18116C80	0x18116EC0	DPLL	page 280
0x18116184	0x18116F04	0x18116C84	0x18116EC4	DPLL2	page 280
0x18116188	0x18116F08	0x18116C88	0x18116EC8	DPLL3	page 281

8.16.1 DPLL

Address Offset:
Baseband: 0x18116180
CPU: 0x18116F00
DDR: 0x18116EC0
PCIE:0x18116C80
Access: Read/Write
Manaul control bits for DPLL

Bit	Bit Name	Description
31:27	REFDIV	Manual override PLL reference divider ratio
26:18	NINT	Manual override PLL feedback divide ratio
17:0	NFRAC	Manual override of PLL fractional value of PLL divide ratio

8.16.2 DPLL2

Address Offset:
Baseband: 0x18116184
CPU: 0x18116F04
DDR: 0x18116EC4
PCIE:0x18116C84
Access: Read/Write

Bit	Bit Name	Description	
31	LOCAL_PLL	Selects if we want to manually set PLL control bits through the SRIF space	
30:29	KI	Integral path gain of loop filter in DPLL	
28:25	KD	Proportional gain of loop filter in DPLL, this sets the loop bandwidth of the PLL	
24	EN_NEGTRIG	Enable negative triggered for digital engine of DPLL. Only use half-cycle for computation.	
23	SEL_1SDM	Sets order of SDM in DPLL	
		0	2nd order SDM
		1	1st order SDM

Bit	Bit Name	Description
22	PLL_PWD	Manual override for PLL power down; set to 1 to power down the PLL; a falling edge on this signal is needed to latch in the PLL values and initialize the PLL
21:19	OUTDIV	Manual override to divide output of VCO in DPLL by $2^{OUT\_DIV[2:0]}$
18:12	PHASE_SHIFT	Programmable phase shift for DPLL
11:0	RES	Reserved

8.16.3 DPLL3

Address Offset:
Baseband: 0x18116188
CPU: 0x18116F08
DDR: 0x18116EC8
PCIE:0x18116C88

Access: Read/Write

DPLL diagnostic bits and spares.

Bit	Bit Name	Description
31:3	RES	Reserved
2	LOCAL_PLL_PWD	Independant override control for PLL_PWD
1:0	RES	Reserved

8.17 PCIE Configuration Space Registers

Table 8-20 shows the PCI Express configuration space registers for the QCA9563.

Table 8-20 PCI Configuration Space Registers

Offset	Description	Page
0x180C0000	Vendor ID	page 282
0x180C0002	Device ID	page 283
0x180C0004	Command	page 283
0x180C0006	Status	page 284
0x180C0008	Revision ID	page 284
0x180C0009	Class Code	page 284
0x180C000C	Cache Line Size	page 285
0x180C000D	Master Latency Timer	page 285
0x180C000E	Header Type	page 285
0x180C0010	Base Address 0 (Read-Only)	page 285
0x180C0010	BAR0 Mask (Write-Only)	page 286
0x180C0018	Bus Number	page 286
0x180C001E	Secondary Status	page 287
0x180C0020	Memory Base	page 287
0x180C0022	Memory Limit	page 287
0x180C0024	Prefetchable Memory Base	page 288
0x180C0026	Prefetchable Memory Limit	page 288
0x180C0034	Capability Pointer	page 288
0x180C003C	Interrupt Line	page 288
0x180C003D	Interrupt Pin	page 289
0x180C003E	Bridge Control	page 289

8.17.1 Vendor ID

Address: 0x180C
Access: Read-Only

The default value is the hardware configuration parameter.

Bit	Bit Name	Description
15:0	CX_VENDOR_ID_0	Vendor ID

8.17.2 Device ID

Address: 0x180C0002
Access: Read-Only

The default value is the hardware configuration parameters.

Bit	Bit Name	Description
15:0	CX_DEVICE_ID_0	Device ID

8.17.3 Command

Address: 0x180C0004
Access: See field description
Reset: 0

Bit	Access	Description
15:11	RO	Reserved
10	R/W	INTx assertion disable
9	RO	Fast back-to-back enable. Not applicable for PCIE. Hard-wired to 0.
8	R/W	SERR# enable
7	RO	IDSEL stepping/wait cycle control. Not applicable for PCIE. Hard-wired to 0.
6	R/W	Parity error response
5	RO	VGA palette snoop. Not applicable for PCIE. Hard-wired to 0.
4	RO	Memory write and invalidate. Not applicable for PCIE. Hard-wired to 0.
3	RO	Special cycle enable. Not applicable for PCIE. Hard-wired to 0.
2	R/W	Bus master enable
1	R/W	Memory space enable
0	R/W	I/O space enable

8.17.4 Status

Address: 0x180C0006
Access: See field description
Reset: See field description

Bit	Access	Reset	Description
15	RW1C	0	Detected parity error
14	RW1C	0	Signalled system error
13	RW1C	0	Received master abort
12	RW1C	0	Received target abort
11	RW1C	0	Signalled target abort
10:9	RO	0x0	DEVSEL timing; not applicable for PCIE. Hard-wired to 0.
8	RW1C	0	Master data parity error
7	RO	0	Fast back-to-back capable; not applicable for PCIE. Hard-wired to 0.
6	RO	0	Reserved
5	RO	0	66 MHz capable; not applicable for PCIE. Hardwired to 0.
4	RO	1	Capabilities list. Indicates presence of an extended capability item. Hard-wired to 1.
3	RO	0	INTx status
2:0	RO	0x0	Reserved

8.17.5 Revision ID

Address: 0x180C0008
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
7:0	CX_REVISION_ID_0	Revision ID

8.17.6 Class Code

Address: 0x180C0009
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
23:16	BASE_CLASS_CODE_0	Base class code
15:8	SUB_CLASS_CODE_0	Sub class code
7:0	IF_CODE_0	Programming interface

8.17.7 Class Line Size

Address: 0x180C000C
Access: Read/Write
Reset: 0x0

Bit	Description
7:0	Cache line size This register is R/W for legacy compatibility purposes and is not applicable to PCI Express device functionality. Writing to the Cache Line Size register does not impact functionality of the RC.

8.17.8 Master Latency Timer

Address: 0x180C000D
Access: Read-Only
Reset: 0x0

Bit	Description
7:0	Master latency timer; not applicable to PCIE. Hardwired to 0.

8.17.9 Header Type

Address: 0x180C000E
Access: Read-Only
Reset: See field descriptions

Bit	Reset	Description
7	0x0	Multi-function device
6:0	0x01	Configuration header format. Hardwired to 0x01.

8.17.10 Base Address 0 (BAR0)

Address: 0x180C0010
Access: Read-Only
Reset: See field descriptions

The RC Core provides one 32-bit base address register.

Bit	Reset		Description
31:4	0x0000000		BAR0 base address bits. The BAR0 mask value determines which address bits are masked.
3	PREFETCHABLE0_0 for memory BAR		If BAR0 is a memory BAR, indicates if the memory region is prefetchable:
		0	Non-prefetchable
		1	Prefetchable
2:1	BAR0_TYPE_0 for memory BAR		If BAR 0 is a memory BAR, bits [2:1] determine the BAR type:
		00	32-bit BAR
		10	Unused
0	MEM0_SPACE_DECODER_0	0	BAR0 is a memory BAR
		1	Unused

8.17.11 BAR0 Mask

Address: 0x180C0010 (same as Base Address 0 (BAR0), page 8-285
Access: Write-Only
Reset: See field descriptions

Determines which bits in the BAR are non-writable by host software, which determines the size of the address space claimed by the BAR. This register only exists when the corresponding BAR*n*_MASK_WRITABLE_0 value is 1. Otherwise, the BAR*n*_MASK_0 value sets the BAR Mask value in hardware.

BAR Mask values indicate the range of low-order bits in each implemented BAR to not use for address matching. The BAR Mask value also indicates the range of low-order bits in the BAR that cannot be written from the host. The application can write to all BAR bits to set memory, I/O, and other BAR options. To disable a BAR, the application can write a 0 to bit [0] of the BAR Mask register. To change the BAR Mask value for a disabled BAR, the application must first enable the BAR by writing 1 to bit [0]. After enabling the BAR, the application can write a new value to the BAR Mask register. If the BAR Mask value for a BAR is less than that required for the BAR type, the RC Core uses the minimum BAR type value:

- BAR bits [11:0] are always masked for a memory BAR. The RC Core requires each memory BAR to claim at least 4 KB
- BAR bits [7:0] are always masked for an I/O BAR. The RC Core requires each I/O BAR to claim at least 256 bytes

Bit	Bit Name	Description	
31:1	BAR0 _MASK_0	Indicates which BAR0 bits to mask (make nonwritable) from host software, which in turn determines the size of the BAR. For example, writing 0xFFF to the BAR0 Mask register claims a 4096-byte BAR by masking bits 11:0 of the BAR from writing by host software. Application write access depends on the value of BAR0_MASK_WRITABLE_0: ■ If BAR0_MASK_WRITABLE_0 = 1, the BAR0 Mask register is writable ■ If BAR0_MASK_WRITABLE_0 = 0, BAR0 Mask is not writable	
0	BAR0 _ENABLED _0	BAR0 enable	
		0	BAR0 is disabled
		1	BAR0 is enabled
		Bit [0] is interpreted as BAR enable when writing to the BAR Mask register rather than as a mask bit because bit [0] of a BAR is always masked from writing by host software.	

8.17.12 Bus Number

Address: 0x180C0018
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
31:24	RO	Secondary latency timer; not applicable to PCI Express, hardwired to 0x00.
23:16	R/W	Subordinate bus number
15:8	R/W	Secondary bus number
7:0	R/W	Primary bus number

8.17.13 Secondary Status

Address: 0x180C001E
Access: See field descriptions
Reset: 0

Bit	Access	Description
15	RW1C	Detected parity error
14	RW1C	Received system error
13	RW1C	Received master abort
12	RW1C	Received target abort
11	RW1C	Signalled timer abort
10:9	RO	DEVSEL timing; not applicable to PCIE. Hardwired to 0.
8	RW1C	Master data parity error
7	RO	Fast back-to-back capable; not applicable to PCIE. Hardwired to 0.
6	RO	Reserved
5	RO	66 MHz; not applicable to PCIE. Hardwired to 0.
4:0	RO	Reserved

8.17.14 Memory Base

Address: 0x180C0020
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
15:4	R/W	Memory base address
3:0	RO	Reserved

8.17.15 Memory Limit

Address: 0x180C0022
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
15:5	R/W	Memory limit address
4:0	RO	Reserved

8.17.16 Prefetchable Memory Base

Address: 0x180C0024
Access: See field descriptions
Reset: See field descriptions

Bit	Access	Default	Description	
15:4	R/W	0x000	Upper 12 bits of 32-bit prefetchable memory start address	
3:1	RO	0x0	Reserved	
0	RO	MEM_DECODE_64_0	64-bit memory addressing	
			0	32-bit memory addressing
			1	Unused

8.17.17 Prefetchable Memory Limit

Address: 0x180C0026
Access: See field descriptions
Reset: See field descriptions

Bit	Access	Default	Description	
15:4	R/W	0x000	Upper 12 bits of 32-bit prefetchable memory end address	
3:1	RO	0x0	Reserved	
0	RO	MEM_DECODE_64_0	64-bit memory addressing	
			0	32-bit memory addressing
			1	Unused

8.17.18 Capability Pointer

Address: 0x180C0034
Access: Read-Only
Reset: 0x40

Bit	Description
7:0	First capability pointer. Points to power management capability structure by default.

8.17.19 Interrupt Line

Address: 0x180C003C
Access: Read/Write
Reset: 0xFF

Bit	Description
7:0	Interrupt line

8.17.20 Interrupt Pin

Address: 0x180C003D
Access: Read-Only
Reset: 0x1

Bit	Description	
7:0	Interrupt pin. Identifies the legacy interrupt Message that the device uses. Valid values are:	
	00	The device does not use legacy interrupt
	01	The device uses INTA

8.17.21 Bridge Control

Address: 0x180C003E
Access: See field descriptions
Reset: 0x0

Bit	Access	Description
15:12	RO	Reserved
11	RO	Discard timer SERR enable status; not applicable to PCIE. Hardwired to 0.
10	RO	Discard timer status; not applicable to PCIE. Hardwired to 0.
9	RO	Secondary discard timer; not applicable to PCIE. Hardwired to 0.
8	RO	Primary discard timer; not applicable to PCIE. Hardwired to 0.
7	RO	Fast back-to-back transactions enable; not applicable to PCIE. Hardwired to 0.
6	R/W	Secondary bus reset
5	RO	Master abort mode; not applicable to PCIE. Hardwired to 0.
4	R/W	VGA 16-bit decode
3	R/W	VGA enable
2	R/W	ISA enable
1	R/W	SERR enable
0	R/W	Parity error response enable

8.18 PMU Registers

Table 8-21 summarizes the PCIE RC PHY registers for the QCA9563.

Table 8-21 PCIE RC PHY Registers

Address	Name	Description	Page
0x18116CC0	PMU1	PMU Configuration	page 290
0x18116CC4	PMU2	PMU Configuration 2	page 290

8.18.1 PMU Configuration (PMU1)

Address: 0x18116CC0
Access: Read/Write
Reset: 0x633C8176

This register is for configuring PMU.

Bit	Bit Name	Description
31:0	SWREG	CTRL bits for SWREG

8.18.2 PMU Configuration 2 (PMU2)

Address: 0x18116CC4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:22	SWREGMSB	MSB CTRL bits for SWREG
21	PGM	PGM
20:19	LDO_TUNE	DDR LDO TUNE
18	PWDLDO_DDR	PWD DDR LDO
17	LPOPWD	PWD DDR LDO
16:0	SPARE	Spare bits

8.19 PCIE RC PHY Registers

Table 8-22 summarizes the PCIE RC PHY registers for the QCA9563.

Table 8-22 PCIE RC PHY Registers

Address	Name	Description	Page
0x18116E00	PCIE_PHY_REG_1	PCIE PHY 1	page 291
0x18116E04	PCIE_PHY_REG_2	PCIE PHY 2	page 292
0x18116E08	PCIE_PHY_REG_3	PCIE PHY 3	page 293

8.19.1 PCIE PHY 1 (PCIE_PHY_REG_1)

Address: 0x18116E00
Access: Read/Write
Reset: See field description

This register is the PCIE PHY long shift register.

Bit	Bit Name	Reset	Description	
31	SERDES_DIS_RXIMP	0x0	Disable the receiver impedance in SERDES	
30:29	SERDES_TXDR_CTRL	0x0	Transmit Amplitude control for the SERDES (used in conjunction with SERDES_HALFTXDR)	
28:27	PERSTDELAY	0x2	Controls delay of PERSTN_DIGITAL WRT PERSTN_SERDES	
			00	10 µs
			01	12 µs
			10	15 µs
			11	20 µs
26:25	CLKOBSSEL	0x0	Select different clocks for observation.	
			00	No clock
			01	CLK125M_TX
			10	CLK125M_RX
			11	CLK_PCIEREF
24	DATAOBSEN	0x0	Enables the receive Data Observe bus	
23	FUNCTEST_EN	0x0	Enables the low-speed functional test mode of the PCIE interface	
22	SERDES_DISABLE	0x0	Forces the SERDES into power down mode. Used during ATE testing of other interfaces	
21	RXCLKINV	0x1	Invert the CLK125M_RX before using for receive data latching	
20	FUNCTESTRXCLKINV	0x0	Invert the Functional Test Clock for receive latching	
19	FUNCTESTTXCLKINV	0x0	Invert the Functional Test Clock for Transmit latching	
18	ENABLECLKREQ	0x0	Enables assertion/deassertion of CLKREQ# pin upon L1-Entry/Exit	
17	FLORCELOOPBACK	0x0	Force PCIE PHY into looping back its Rx data back to Tx	
16:15	SEL_CLK	0x2	Overclock control	

14	SERDES_RX_EQ	0x0	Enables receiver equalization	
13	SERDES_EN_LCKDT	0x1	Enables the lock detect circuit	
12	SERDES_PLL_ DISABLE	0x0	When this bit is set the PLL is disabled in L1 state	
11	SERDES_POWER_ SAVE	0x0	When set, enables additional power saving of SERDES in L0s and L1 states	
10:9	SERDES_CDR_BW	0x3	CDR digital accumulator length control	
8:7	SERDES_TH_LOS	0x0	Threshold selection for RX loss-of-signal detection	
			00	Normal
			01	-2dB
			10, 11	+2dB
6	SERDESEN_DEEMP	0x1	Enable TX de-emphasis when high	
5	SERDES_HALFTXDR	0x0	Tx driver output amplitude is reduced to 500 mVppd when high	
4	SERDES_SEL_HSP	0x1	VCO frequency adjust	
3:0	SWITCH_CTRL	0xE	Resistor calibration switch control	

8.19.2 PCIE PHY 2 (PCIE_PHY_REG_2)

Address: 0x18116E04
Access: Read/Write
Reset: See field description

This register is the PCIE PHY long shift register.

Bit	Bit Name	Reset	Description
31:24	PRBS_ERROR_COUNT	0x0	PRBS error count
23	SDS_SDM_RXELECIDLE	0x0	SERDES Rx electrical idle status
22	SDS_SDM_RXDETECTED	0x0	SERDES receiver detect status
21	PRBS_SCRAMBLE	0x0	Scramble during PRBS pattern
20	PRBS_START	0x0	Start the PRBS testing
19:13	PRBS_TS_NUM	0x40	Number of TS preceding PRBS
12	TXDETRXOVREN	0x0	Enable bit for overriding and controlling the TxDetRx trigger
11	TXDETRXOVRVALUE	0x0	Override value for TxDetRx trigger
10	DATAOBSPRBSERR	0x0	Enables observation of PRBS Error Count of the 20-bit observation bus
9:6	CDRREADYTIMER	0x7	RX_CLOCK ready timer in units of 8*8ns. Triggered by an exit from RXELECIDLE
5:1	TXDETRXTARGETDELAY	0xC	Programmable timer that gets enabled after assertion of Tx Elecidle and MAC-PHY TxDetRx trigger . Receiver detection status is checked after the completion of this timer.
0	FORCEDETECT	0x0	Overrides the PHY_MAC_RXSTATUS to 0x3 (successful receiver detection) on occurence of PHY_MAC_PHYSTATUS pulse and mac_ PHY_XDETECTRX (receiver detection request). Overrides the originial receiver detection indication.

8.19.3 PCIE PHY 3 (PCIE_PHY_REG_3)

Address: 0x18116E08
Access: Read/Write
Reset: See field description

This register is the PCIE PHY long shift register.

Bit	Bit Name	Reset	Description
31:28	PRBS_COMMA_STATUS	0x0	PRBS Rx comma status
27:11	SPARE	0x00A0B	Spare bits
10	SEL_CLK100	0x0	Enable/disable for 100 MHz reference clock input to analog (used when serdes_disable is set)
9	EN_BEACONGEN	0x0	Enable SERDES beacon generation Controllability used in SRIF mode (pipe_mode = 0)
8	TXELECIDLE	0x0	Controllability for transmit electrical idle
7:6	SEL_CLK	0x0	Overclock control Controllability used in SRIF mode (pipe_mode = 0)
5	RX_DET_REQ	0x0	Receiver detection TxDetRx trigger - controllability used in SRIF mode (pipe_mode = 0)
4	MODE_OCLK_IN	0x0	Overclocking control 0 Non-overclocking 1 Overclocking
3	EN_PLL	0x0	Enable/disable SERDES PLL Controllability used in SRIF mode (pipe_mode = 0)
2	EN_LCKDT	0x1	Enable lock detect circuit Controllability used in SRIF mode (pipe_mode = 0)
1	EN_BUFS_RX	0x0	Enable SERDES Rx buffers Controllability used in SRIF mode (pipe_mode = 0)
0	EN	0x0	SERDES enable Controllability used in SRIF mode (pipe_mode = 0)

8.20 GMAC Registers

Table 8-23 summarizes the GMAC registers for the QCA9563.

Table 8-23 Ethernet Registers Summary

GMAC Address	Description		Page
0x19000000	MAC Configuration 1		page 297
0x19000004	MAC Configuration 2		page 298
0x19000008	IPG/IFG		page 299
0x1900000C	Half-Duplex		page 300
0x19000010	Maximum Frame Length		page 300
0x19000020	MII Configuration		page 301
0x19000024	MII Command		page 302
0x19000028	MII Address		page 302
0x1900002C	MII Control		page 302
0x19000030	MII Status		page 303
0x19000034	MII Indicators		page 303
0x19000038	Interface Control		page 304
0x1900003C	Interface Status		page 305
0x19000040	STA Address 1		page 306
0x19000044	STA Address 2		page 306
0x19000048	ETH Configuration 0		page 306
0x1900004C	ETH Configuration 1		page 307
0x19000050	ETH Configuration 2		page 308
0x19000054	ETH Configuration 3		page 308
0x19000058	ETH Configuration 4		page 309
0x1900005C	ETH Configuration 5		page 310
0x19000080	TR64	Tx/Rx 64 Byte Frame Counter	page 310
0x19000084	TR127	Tx/Rx 65-127 Byte Frame Counter	page 311
0x19000088	TR255	Tx/Rx 128-255 Byte Frame Counter	page 311
0x1900008C	TR511	Tx/Rx 256-511 Byte Frame Counter	page 311
0x19000090	TR1K	Tx/Rx 512-1023 Byte Frame Counter	page 312
0x19000094	TRMAX	Tx/Rx 1024-1518 Byte Frame Counter	page 312
0x19000098	TRMGV	Tx/Rx 1519-1522 Byte VLAN Frame Counter	page 312
0x1900009C	RBYT	Receive Byte Counter	page 313
0x190000A0	RPKT	Receive Packet Counter	page 313
0x190000A4	RFCS	Receive FCS Error Counter	page 313
0x190000A8	RMCA	Receive Multicast Packet Counter	page 314
0x190000AC	RBCA	Receive Broadcast Packet Counter	page 314
0x190000B0	RXCF	Receive Control Frame Packet Counter	page 314

Table 8-23 Ethernet Registers Summary (cont.)

GMAC Address	Description		Page
0x190000B4	RXPF	Receive Pause Frame Packet Counter	page 315
0x190000B8	RXUO	Receive Unknown OPCode Packet Counter	page 315
0x190000BC	RALN	Receive Alignment Error Counter	page 315
0x190000C0	RFLR	Receive Frame Length Error Counter	page 316
0x190000C4	RCDE	Receive Code Error Counter	page 316
0x190000C8	RCSE	Receive Carrier Sense Error Counter	page 316
0x190000CC	RUND	Receive Undersize Packet Counter	page 317
0x190000D0	ROVR	Receive Oversize Packet Counter	page 317
0x190000D4	RFRG	Receive Fragments Counter	page 317
0x190000D8	RJBR	Receive Jabber Counter	page 318
0x190000DC	RDRP	Receive Dropped Packet Counter	page 318
0x190000E0	TBYT	Transmit Byte Counter	page 318
0x190000E4	TPKT	Transmit Packet Counter	page 319
0x190000E8	TMCA	Transmit Multicast Packet Counter	page 319
0x190000EC	TBCA	Transmit Broadcast Packet Counter	page 319
0x190000F0	TXPF	Transmit Pause Control Frame Counter	page 320
0x190000F4	TDFR	Transmit Deferral Packet Counter	page 320
0x190000F8	TEDF	Transmit Excessive Deferral Packet Counter	page 320
0x190000FC	TSCL	Transmit Single Collision Packet Counter	page 321
0x19000100	TMCL	Transmit Multiple Collision Packet	page 321
0x19000104	TLCL	Transmit Late Collision Packet Counter	page 321
0x19000108	TXCL	Transmit Excessive Collision Packet Counter	page 322
0x1900010C	TNCL	Transmit Total Collision Counter	page 322
0x19000110	TPFH	Transmit Pause Frames Honored Counter	page 322
0x19000114	TDRP	Transmit Drop Frame Counter	page 323
0x19000118	TJBR	Transmit Jabber Frame Counter	page 323
0x1900011C	TFCS	Transmit FCS Error Counter	page 323
0x19000120	TXCF	Transmit Control Frame Counter	page 324
0x19000124	TOVR	Transmit Oversize Frame Counter	page 324
0x19000128	TUND	Transmit Undersize Frame Counter	page 324
0x1900012C	TFRG	Transmit Fragment Counter	page 324
0x19000130	CAR1	Carry Register 1	page 325
0x19000134	CAR2	Carry Register 2	page 326
0x19000138	CAM1	Carry Mask Register 1	page 327

Table 8-23 Ethernet Registers Summary (cont.)

GMAC Address	Description		Page
0x1900013C	CAM2	Carry Mask Register 2	page 328
0x19000180	DMATXCNTRL_Q0	DMA Transfer Control for Queue 0	page 328
0x19000184	DMATXDESCR_Q0	Descriptor Address for Queue 0 Tx	page 329
0x19000188	**DMA Tx Status**		page 329
0x1900018C	DMARXCTRL	Rx Control	page 330
0x19000190	DMARXDESCR	Pointer to Rx Descriptor	page 330
0x19000194	DMARXSTATUS	Rx Status	page 330
0x19000198	DMAINTRMASK	Interrupt Mask	page 331
0x1900019C	**Interrupts**		page 332
0x190001A0	ETH_TX_BURST	Ethernet Tx burst	page 333
0x190001A4	ETH_TXFIFO_TH	Ethernet Tx FIFO Max and Min Threshold	page 333
0x190001A8	ETH_XFIFO_DEPTH	Current Tx and Rx FIFO Depth	page 334
0x190001AC	ETH_RXFIFO_TH	Ethernet Rx FIFO	page 334
0x190001B8	ETH_FREE_TIMER	Ethernet Free Timer	page 334
0x190001C0	DMATXCNTRL_Q1	DMA Transfer Control for Queue 1	page 334
0x190001C4	DMATXDESCR_Q1	Descriptor Address for Queue 1 Tx	page 335
0x190001C8	DMATXCNTRL_Q2	DMA Transfer Control for Queue 2	page 335
0x190001CC	DMATXDESCR_Q2	Descriptor Address for Queue 2 Tx	page 335
0x190001D0	DMATXCNTRL_Q3	DMA Transfer Control for Queue 3	page 336
0x190001D4	DMATXDESCR_Q3	Descriptor Address for Queue 3 Tx	page 336
0x190001D8	DMATXARBCFG	DMA Tx Arbitration Configuration	page 336
0x190001E4	DMATXSTATUS_123	Tx Status and Packet Count for Queues 1 to 3	page 337
0x19000200	LCL_MAC_ADDR_DW0	Local MAC Address Dword0	page 337
0x19000204	LCL_MAC_ADDR_DW1	Local MAC Address Dword1	page 337
0x19000208	NXT_HOP_DST_ADDR_DW0	Next Hop Router MAC Address Dword0	page 338
0x1900020C	NXT_HOP_DST_ADDR_DW1	Next Hop Router MAC Destination Address Dword1	page 338
0x19000210	GLOBAL_IP_ADDR0	Local Global IP Address 0	page 338
0x19000214	GLOBAL_IP_ADDR1	Local Global IP Address 1	page 339
0x19000218	GLOBAL_IP_ADDR2	Local Global IP Address 2	page 339
0x1900021C	GLOBAL_IP_ADDR3	Local Global IP Address 3	page 339

8.20.1 MAC Configuration 1

GMAC Address: 0x19000000
Access: See field description
Reset: See field description

This register is used to set the actions for transmitting and receiving frames.

Bit	Bit Name	Type	Reset	Description
31	SOFT_RESET	RW	0x1	Setting this bit resets all modules except the host interface. The host interface is reset via HRST.
30	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
29:20	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
19	RESET_RX_MAC_ CONTROL	RW	0x0	Resets the receive (Rx) MAC control block
18	RESET_TX_MAC_ CONTROL	RW	0x0	Resets the transmit (Tx) MAC control
17	RESET_RX_ FUNCTION	RW	0x0	Resets the Rx function
16	RESET_TX_ FUNCTION	RW	0x0	Resets the Tx function
15:9	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
8	LOOP_BACK	RW	0x0	Setting this bit causes MAC Rx outputs to loop back to the MAC Rx inputs. Clearing this bit results in normal operation.
7:6	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
5	RX_FLOW _CONTROL	RW	0x0	Setting this bit causes the Rx MAC control to detect and act on pause flow control frames.
4	TX_FLOW_ CONTROL	RW	0x0	Setting this bit causes the Tx MAC control to send requested flow control frames. Clearing this bit prevents the MAC from sending flow control frames. The default is 0.
3	SYNCHRONIZED_RX	RO	0x0	Rx enable synchronized to the receive stream
2	RX_ENABLE	RW	0x0	Setting this bit will allow the MAC to receive frames from the PHY. Clearing this bit will prevent the reception of frames.
1	SYNCHRONIZED_TX	RO	0x0	Tx enable synchronized to the Tx stream
0	TX_ENABLE	RW	0x0	Allows the MAC to transmit frames from the system. Clearing this bit will prevent the transmission of frames.

8.20.2 MAC Configuration 2

GMAC Address: 0x19000004
Access: Read/Write
Reset: See field description

This register is used to set the parameters relating to the MAC, including duplex, CRC, and oversized frames.

Bit	Bit Name	Reset	Description
31:16	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:12	PREAMBLE_ LENGTH	0x7	Determines the length of the preamble field of the packet, in bytes.
11:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:8	RES	0x0	Reserved. Must be set to 0x01
7:6	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
5	HUGE_FRAME	0x0	Set this bit to allow frames longer than the MAXIMUM FRAME LENGTH to be transmitted and received. Clear this bit to have the MAC limit the length of frames at the MAXIMUM FRAME LENGTH value, which is contained in the Maximum Frame Length, page 8-300 register.
4	LENGTH_FIELD	0x0	Set this bit to cause the MAC to check the frame's length field to ensure it matches the data field length. Clear this bit for no length field checking.
3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
2	PAD/CRC ENABLE	0x0	Set this bit to have the MAC pad all short frames and append a CRC to every frame whether or not padding was required. Clear this bit if frames presented to the MAC have a valid length and contain a CRC.
1	CRC_ENABLE	0x0	Set this bit to have the MAC append a CRC to all frames. Clear this bit if frames presented to the MAC have a valid length and contain a valid CRC.
0	FULL_DUPLEX	0x0	Setting this bit configures the MAC to operate in full-duplex mode. Clearing this bit configures the MAC to operate in half-duplex mode only.

8.20.3 IPG/IFG

GMAC Address: 0x19000008
Access: Read/Write
Reset: See field description

This register is used to configure settings for the inter-packet gap and the inter-frame gap.

Bit	Bit Name	Reset	Description
31	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
30:24	NON_BACK_TO_BACK_INTER_PACKET_GAP1	0x40	Represents the carrier sense window. If a carrier is detected, MAC defers to the carrier. If the carrier becomes active, MAC continues timing and Tx, knowingly causing a collision to ensure fair access to the medium.
23	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
22:16	NON_BACK_TO_BACK_INTER_PACKET_GAP2	0x60	This programmable field represents the non-back-to-back inter-packet gap in bit times
15:8	MINIMUM_IFG_ENFORCEMENT	0x50	Represents the minimum IFG size to enforce between frames (expressed in bit times). Frames with a IFG of less than programmed are dropped.
7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
6:0	BACK_TO_BACK_INTER_PACKET_GAP	0x60	Represents the IPG between back-to-back packets (expressed in bit times). This IPG parameter is used in full- duplex mode when two Tx packets are sent back-to-back. Set this field to the desired number of bits.

8.20.4 Half-Duplex

GMAC Address: 0x1900000C
Access: Read/Write
Reset: See field description

This register is used to configure the settings for half-duplex, including back pressure, excessive defer and collisions.

Bit	Bit Name	Reset	Description
31:24	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
23:20	ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION	0xA	Used when bit [19] is set. The value programmed is substituted for the Ethernet standard value of ten.
19	ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE	0x0	Setting this bit configures the Tx MAC to use the setting of bits [23:20] instead of the tenth collision. Clearing this bit will cause the TX MAC to follow the standard binary exponential backoff rule, which specifies that any collision after the tenth uses 210-1 as the maximum backoff time.
18	BACKPRESSURE_ NO_BACKOFF	0x0	Setting this bit configures the Tx MAC to immediately retransmit following a collision during backpressure operation. Clearing this bit causes the Tx MAC to follow the binary exponential backoff rule.
17	NO_BACKOFF	0x0	Setting this bit configures the Tx MAC to immediately retransmit following a collision. Clearing this bit causes the Tx MAC to follow the binary exponential backoff rule.
16	EXCESSIVE_ DEFER	0x1	Setting this bit configures the Tx MAC to allow the transmission of a packet that has been excessively deferred. Clearing this bit will cause the Tx MAC to abort the transmission of a packet that has been excessively deferred.
15:12	RETRANSMISSION_ MAXIMUM	0xF	This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The maximum number of attempts is defined by 802.11 standards as 0xF.
11:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:0	COLLISION_ WINDOW	0x37	This programmable field represents the slot time or collision window during which collisions might occur in a properly configured network. Since the collision window starts at the beginning of a transmission, the preamble and SFD are included. The reset value (0x37) corresponds to the count of frame bytes at the end of the window. If the value is larger than 0x3F the TPST single will no longer work correctly.

8.20.5 Maximum Frame Length

GMAC0 Address: 0x19000010
Access: Read/Write
Reset: 0x600

This register is used to set the maximum allowable frame length.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	MAX_FRAME _LENGTH	This programmable field sets the maximum frame size in both the Tx and Rx directions

8.20.6 MII Configuration

GMAC Address: 0x19000020
Access: Read/Write
Reset: 0x0

This register is used to set the MII management parameters.

Bit	Bit Name	Description
31	RESET_MII_MGMT	Setting this bit resets the MII Management. Clearing this bit allows MII Management to perform management read/write cycles as requested by the Host interface.
30:6	RES	Reserved. Must be written with zero. Contains zeros when read.
5	SCAN_AUTO_INCREMENT	Setting this bit causes MII Management to continually read from a set of contiguous PHYs. The starting address of the PHY is specified by the PHY address field recorded in the MII Address register. The next PHY to be read will be PHY address + 1. The last PHY to be queried in this read sequence will be the one residing at address 0x31, after which the read sequence will return to the PHY specified by the PHY address field.
4	PREAMBLE_SUPRESSION	Setting this bit causes MII Management to suppress preamble generation and reduce the management cycle from 64 clocks to 32 clocks. Clearing this bit causes MII Management to perform Management read/write cycles with the 64 clocks of preamble.
3:0	MGMT_CLOCK_SELECT	This field determines the clock frequency of the management clock (MDC).

Management Clock Select	3	2	1	0
Source clock divided by 4	0	0	0	0
Source clock divided by 4	0	0	0	1
Source clock divided by 6	0	0	1	0
Source clock divided by 8	0	0	1	1
Source clock divided by 10	0	1	0	0
Source clock divided by 14	0	1	0	1
Source clock divided by 20	0	1	1	0
Source clock divided by 28	0	1	1	1
Source clock divided by 34	1	0	0	0
Source clock divided by 42	1	0	0	1
Source clock divided by 50	1	0	1	0
Source clock divided by 58	1	0	1	1
Source clock divided by 66	1	1	0	0
Source clock divided by 74	1	1	0	1
Source clock divided by 82	1	1	1	0
Source clock divided by 98	1	1	1	1

8.20.7 MII Command

GMAC Address: 0x19000024
Access: Read/Write
Reset: 0x0

This register is used to cause MII management to perform read cycles.

Bit	Bit Name	Description
31:2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	SCAN_CYCLE	Causes MII management to perform read cycles continuously (e.g. to monitor link fail).
0	READ_CYCLE	Causes MII management to perform a single read cycle.

8.20.8 MII Address

GMAC Address: 0x19000028
Access: Read/Write
Reset: 0x0

All MAC/PHY registers are accessed via the MII address and MII control registers of GMAC0 only. The details of the Ethernet MAC/PHY that are accessible through the MAC0 MII address.

Bit	Bit Name	Description
31:13	RES	Reserved. Must be written with zero. Contains zeros when read.
12:8	PHY_ADDRESS	Represents the five-bit PHY address field used in management cycles. Up to 31 PHYs can be addressed (0 is reserved).
7:5	RES	Reserved. Must be written with zero. Contains zeros when read.
4:0	REGISTER ADDRESS	Represents the five-bit register address field used in management cycles. Up to 32 registers can be accessed.

8.20.9 MII Control

GMAC Address: 0x1900002C
Access: Write-Only
Reset: 0x0

All MAC/PHY registers are accessed via the MII Address and MII Control registers.
This register is used to perform write cycles using the information in the MII Address register.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	MII_MGMT_ CONTROL	When written, an MII management write cycle is performed using the 16-bit data and the pre-configured PHY and register addresses from “MII Address, page 8-302” (0x0A).

8.20.10 MII Status

GMAC Address: 0x19000030
Access: Read-Only
Reset: 0x0

This register is used to read information following an MII management read cycle.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	MII_MGMT_ STATUS	After an MII management read cycle, 16-bit data can be read from this register.

8.20.11 MII Indicators

GMAC Address: 0x19000034
Access: Read-Only
Reset: 0x0

This register is used indicate various functions of the MII management are currently being performed.

Bit	Bit Name	Description
31:3	RES	Reserved. Must be written with zero. Contains zeros when read.
2	NOT_VALID	When a 1 is returned, this bit indicates that the MII management read cycle has not yet completed and that the read data is not yet valid
1	SCANNING	When a 1 is returned, this bit indicates that a scan operation (continuous MII management read cycles) is in progress
0	BUSY	When a 1 is returned, this bit indicates that the MII management block is currently performing an MII management read or write cycle

8.20.12 Interface Control

MAC 0 Address: 0x19000038
MAC 1 Address: 0x1A000038
Access: Read/Write
Reset: 0x0

This register is used to configure and set the interface modules

Bit	Bit Name	Description	
31	RESET_ INTERFACE_ MODULE	Setting this bit resets the interface module. Clearing this bit allows for normal operation. This bit can be used in place of bits [23], [15] and [7] when any interface module is connected.	
30:25	RES	Reserved. Must be written with zero. Contains zeros when read.	
24	PHY_MODE	Setting this bit configures the serial MII module to be in PHY Mode. Link characteristics are taken directly from the RX segments supplied by the PHY.	
23	RESET_PERMII	Setting this bit resets the PERMII module. Clearing this bit allows for normal operation.	
22:17	RES	Reserved. Must be written with zero. Contains zeros when read.	
16	SPEED	This bit configures the reduced MII module with the current operating speed.	
		0	Selects 10 Mbps mode
		1	Selects 100 Mbps mode
15	RESET_PE100X	This bit resets the PE100X module, which contains the 4B/5B symbol encipher/decipher code.	
14:11	RES	Reserved. Must be written with zero. Contains zeros when read.	
10	FORCE_QUIET	Affects PE100X module only.	
		0	Normal operation
		1	Tx data is quiet, allowing the contents of the cipher to be output
9	NO_CIPHER	Affects PE100X module only.	
		0	Normal ciphering occurs
		1	The raw transmit 5B symbols are transmitting without ciphering
8	DISABLE_LINK_ FAIL	Affects PE100X module only.	
		0	Normal Operation
		1	Disables the 330-ms link fail timer, allowing shorter simulations. Removes the 330-ms link-up time before stream reception is allowed.
7	RESET GPSI	This bit resets the PE10T module which converts MII nibble streams to the serial bit stream of ENDEC PHYs. Affects PE10T module only.	
6:1	RES	Reserved. Must be written with zero. Contains zeros when read.	
0	ENABLE_ JABBER_ PROTECTION	This bit enables the Jabber Protection logic within the PE10T in ENDEC mode. Jabber is the condition where a transmitter is on for longer than 50 ms preventing other stations from transmitting. Affects PE10T module only.	

8.20.13 Interface Status

GMAC Address: 0x1900003C
Access: Read-Only
Reset: 0x0

Identifies the interface statuses. The range of bits that are active are dependant upon the optional interfaces connected at the time.

Bit	Bit Name	Description	
31:10	RES	Reserved. Must be written with zero. Contains zeros when read.	
9	EXCESS_DEFER	This bit sets when the MAC excessively defers a transmission. It clears when read. This bit latches high.	
8	CLASH	Used to identify the serial MII module mode	
		0	In PHY mode or in a properly configured MAC to MAC mode
		1	MAC to MAC mode with the partner in 10 Mbps and/or half-duplex mode indicative of a configuration error
7	JABBER	Used to identify a jabber condition as detected by the serial MII PHY	
		0	No jabber condition detected
		1	Jabber condition detected
6	LINK_OK	Used to identify the validity of a serial MII PHY link	
		0	No valid link detected
		1	Valid link detected
5	FULL_DUPLEX	Used to identify the current duplex of the serial MII PHY	
		0	Half-duplex
		1	Full-duplex
4	SPEED	Used to identify the current running speed of the serial MII PHY	
		0	10 Mbps
		1	100 Mbps
3	LINK_FAIL	Used to read the PHY link fail register. For asynchronous host accesses, this bit must be read at least once every scan read cycle of the PHY.	
		0	The MII management module has read the PHY link fail register to be 0
		1	The MII management module has read the PHY link fail register to be 1
2	CARRIER_LOSS	Carrier status. This bit latches high.	
		0	No carrier loss detection
		1	Loss of carrier detection
1	SQE_ERROR	0	Has not detected an SQE error. Latches high.
		1	Has detected an SQE error.
0	JABBER	0	Has not detected a Jabber condition. Latches high.
		1	Has detected a Jabber condition

8.20.14 STA Address 1

GMAC Address: 0x19000040
Access: Read/Write
Reset: 0x0

This register holds the first four octets of the station address.

Bit	Bit Name	Description
31:24	STATION_ ADDRESS_1	This field holds the first octet of the station address
23:16	STATION_ ADDRESS_2	This field holds the second octet of the station address
15:8	STATION_ ADDRESS_3	This field holds the third octet of the station address
7:0	STATION_ ADDRESS_4	This field holds the fourth octet of the station address

8.20.15 STA Address 2

GMAC Address: 0x19000044
Access: Read/Write
Reset: 0x0

This register holds the last two octets of the station address.

Bit	Bit Name	Description
31:24	STATION_ ADDRESS_5	This field holds the fifth octet of the station address
23:16	STATION_ ADDRESS_6	This field holds the sixth octet of the station address
15:0	RES	Reserved

8.20.16 ETH_FIFO RAM Configuration 0

GMAC Address: 0x19000048
Access: See field description
Reset: 0x0

This register is used to assert and negate functions concerning the ETH module.

Bit	Bit Name	Access		Description
31:21	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
20	FTFENRPLY	RO	Asserted	The eth_fab module is enabled
			Negated	The eth_fab module is disabled
19	STFENRPLY	RO	Asserted	The eth_sys module is enabled
			Negated	The eth_sys module is disabled
18	FRFENRPLY	RO	Asserted	The eth_fab module is enabled
			Negated	The eth_fab module is disabled
17	SRFENRPLY	RO	Asserted	The eth_sys module is enabled
			Negated	The eth_sys module is disabled

16	WTMENRPLY	RO	Asserted	The eth_wtm module is enabled
			Negated	The eth_wtm module is disabled
15:13	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
12	FTFENREQ	RW	Asserted	Requests enabling of the eth_fab module
			Negated	Requests disabling of the eth_fab module
11	STFENREQ	RW	Asserted	Requests enabling of the eth_sys module
			Negated	Requests disabling of the eth_sys module
10	FRFENREQ	RW	Asserted	Requests enabling of the eth_fab module
			Negated	Requests disabling of the eth_fab module
9	SRFENREQ	RW	Asserted	Requests enabling of the eth_sys module
			Negated	Requests disabling of the eth_sys module
8	WTMENREQ	RW	Asserted	Requests enabling of the eth_wtm module
			Negated	Requests disabling of the eth_wtm module
7:5	RES	RW	Reserved. Must be written with zero. Contains zeros when read.	
4	HSTRSTFT	RW	When asserted, this bit places the eth_fab module in reset	
3	HSTRSTST	RW	When asserted, this bit places the eth_sys module in reset	
2	HSTRSTFR	RW	When asserted, this bit places the eth_fab module in reset	
1	HSTRSTSR	RW	When asserted, this bit places the eth_sys module in reset	
0	HSTRSTWT	RW	When asserted, this bit places the eth_wtm module in reset	

8.20.17 ETH Configuration 1

GMAC Address: 0x1900004C
Access: Read/Write
Reset: 0xFFFF

This register is used to configure the ETH storage area.

Bit	Bit Name	Description
31:28	RES	Reserved. Must be written with zero. Contains zeros when read.
27:16	CFGFRTH [11:0]	This hex value represents the minimum number of 4-byte locations to store simultaneously in the receive RAM, relative to the beginning of the frame being input, before FRRDY may be asserted. Note that FRRDY will be latent a certain amount of time due to fabric transmit clock to system transmit clock time domain crossing, and conditional on FRACPT assertion. When set to the maximum value, FRRD may be asserted only after the completion of the input frame. The value of this register must be greater than 18D when HSTDRPLT64 is asserted.
15:0	CFGXOFFRTX	This hexadecimal value represents the number of pause quanta (64-bit times) after an XOFF pause frame has been acknowledged until the ETH reasserts TCRQ if the ETH receive storage level has remained higher than the low watermark.

8.20.18 ETH Configuration 2

MAC 0 Address: 0x19000050
MAC 1 Address: 0x1A000050
Access: Read/Write
Reset: See field description

This register is used to number the minimum amount of 8-byte words in the Rx RAM before pause frames are transmitted.

Bit	Bit Name	Reset	Description
31:29	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
28:16	CFGHWM [12:0]	0xAAA	This hex value represents the maximum number of 8-byte words to store simultaneously in the Rx RAM before TCRQ and PSVAL facilitates an XOFF pause control frame.
15:13	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
12:0	CFGLWM [12:0]	0x555	This hex value represents the minimum number of 8-byte words to store simultaneously in Rx RAM before TCRQ and PSVAL facilitate an XON pause control frame in response to a transmitted XOFF pause control frame.

8.20.19 ETH Configuration 3

GMAC Address: 0x19000054
Access: Read/Write
Reset: See field description

This register is used denote the minimum number of 4-byte locations to simultaneously store in the Tx RAM before assertion.

Bit	Bit Name	Reset	Description
31:28	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
27:16	CFGHWMFT [11:0]	0x555	This hex value represents the maximum number of 4-byte locations to store simultaneously in Tx RAM before FTHWM is asserted. Note that FTHWM has two FTCLK clock periods of latency before assertion or negation, as should be considered when calculating required headroom for maximum size packets.
15:12	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
11:0	CFGFTTTH [11:0]	0xFFF	This hex value represents the minimum number of 4-byte locations to store simultaneously in the Tx RAM, relative to the beginning of the frame being input, before TPSF is asserted. Note that TPSF is latent for a certain amount of time due to fabric Tx clock system Tx clock time domain crossing. When set to the maximum value, TPSF asserts only after the completion of the input frame.

8.20.20 ETH Configuration 4

GMAC Address: 0x19000058
Access: Read/Write
Reset: 0x0

This register is used to signal drop frame conditions internal to the Ethernet.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
HSTFLTRFRM [17:0]: These configuration bits are used to signal the drop frame conditions. The setting of these bits along with their don't care values in the ETH Configuration 5, page 8-310 register (bits [17:0]), determines if the packet is dropped by the GMAC. Drop condition is (|((Pkt_extracted_field[17:0] ~^ eth_configuration_4[17:0]) & ~eth_configuration_5[17:0])) == 1) For example: ■ if it is desired to drop a frame that contains a FCS Error, HSTFLTRFRM[4] would be set and bit 4 in ETH Configuration 5, page 8-310 is not set. ■ if it is desired to drop a multicast frame, HSTFLTRFRM[8] would be set and bit 8 in ETH Configuration 5, page 8-310 is not set. ■ if it is desired to drop a broadcast frame, HSTFLTRFRM[9] would be set and bit 9 in ETH Configuration 5, page 8-310 is not set.		
17	Unicast MAC address match	Unicast Address Match. Destination MAC port matched the STA MAC address configured.
16	Truncated frame	Receive Frame Truncated. Frame length greater than Max frame configured.
15	Long event	Receive Long Event. rx_dv did not get asserted even after long time: 10 Mbps - 50,000 bit time, 100/1000 Mbps - 80,000 bit times.
14	VLAN tag detected	Receive VLAN Tag Detected. Frame's length/type field contained 0x8100 which is the VLAN Protocol Identifier
13	Unsupported op. code	Receive Unsupported Op-code. Current Frame was recognized as a Control frame by the PEMCS, but it contained an Unknown Op-code. Customer may wish to qualify with inverse of CRCERR (~RSV[20]), and with length (64 - 1518) to verify that the frame was a valid Control Frame.
12	Pause frame	Receive PAUSE Control Frame. Current frame was recognized as a Control frame containing a valid PAUSE Frame Op-code and a valid address. Customer may wish to qualify with inverse of CRCERR (~RSV[20]), and with length (64 - 1518) to verify that the frame was a valid Control Frame
11	Control frame	Receive Control Frame. Current Frame was recognized as a Control frame for having a valid Type-Length designation. Customer may wish to qualify with inverse of CRCERR (~RSV[20]), and with length (64 - 1518) to verify that the frame was a valid Control Frame.)
10	Dribble nibble	Receive Dribble Nibble. Indicates that after the end of the packet an additional 1 to 7 bits were received. A single nibble, called the dribble nibble, is formed but not sent to the system (10/100 Mbps only)
9	Broadcast	Receive Broadcast. Packet's destination address contained the broadcast address
8	Multicast	Receive Multicast. Packet's destination address contained a multicast address
7	OK	Receive OK. Frame contained a valid CRC and did not have a code error
6	Out of range	Receive Length Out of Range. Indicates that frame's Length was larger than 1518 bytes but smaller than the Host's Maximum Frame Length Value (Type Field)
5	Length mismatch	Receive Length Check Error. Indicates that frame length field value in the packet does not match the actual data byte length and is not a Type Field
4	CRC error	Receive CRC Error. The packet's CRC did not match the internally generated CRC

3	Code error	Receive Code Error. One or more nibbles were signaled as errors during the reception of the packet
2	False carrier	Receive False Carrier. Indicates that at some time since the last receive statistics vector, a false carrier was detected, noted and reported with this the next receive statistics. The false carrier is not associated with this packet. False carrier is activity on the receive channel that does not result in a packet receive attempt being made. Defined to be RX_ER = 1, RX_DV = 0, RXD[3:0] = 0xE (RXD[7:0] = 0x0E)
1	RX_DV event	Receive RX_DV Event. indicates that the last receive event seen was not long enough to be a valid packet
0	Drop event	Receive Previous Packet Dropped. indicates that since the last RSV a packet was dropped (i.e. IFG too small)

8.20.21 ETH Configuration 5

GMAC Address: 0x1900005C
Access: Read/Write
Reset: See field description

This register is used to control the drop behavior of the GMAC.

Bit	Bit Name	Reset	Description
31:20	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
19	BYTE/NIBBLE	0x0	This bit should be set to 1 for 1000 Mbps, else set to 0.
18	SHORT FRAME	0x0	If set to 1, all frames under 64 bytes are dropped.
17:0	RX FILTER[17:0]	0x3FFFF	HSTFLTRFRMDC [17:0]: These configuration bits indicate which are don't cares for frame drop circuitry. Clearing the bit will look for a matching level on the corresponding HSTFLTRFRM bit in ETH_Configuration 4. If a match is made then the frame is dropped. If a HSTFLTRFRMDC bit is set in this register, no frames are dropped for this condition.

8.20.22 Tx/Rx 64 Byte Frame Counter (TR64)

GMAC Address: 0x19000080
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were up to 64 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR64	The transmit and receive 64 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which is 64 bytes in length inclusive (excluding framing bits but including FCS bytes).

8.20.23 Tx/Rx 65-127 Byte Frame Counter (TR127)

GMAC Address: 0x19000084
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 65–127 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR127	The transmit and receive 65–127 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 65-127 bytes in length inclusive (excluding framing bits but including FCS bytes).

8.20.24 Tx/Rx 128-255 Byte Frame Counter (TR255)

GMAC Address: 0x19000088
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 128–255 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR255	The transmit and receive 128-255 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 128-255 bytes in length inclusive (excluding framing bits but including FCS bytes).

8.20.25 Tx/Rx 256-511 Byte Frame Counter (TR511)

GMAC Address: 0x1900008C
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 256–511 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR511	The transmit and receive 256–511 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 256–511 bytes in length inclusive (excluding framing bits but including FCS bytes).

8.20.26 Tx/Rx 512-1023 Byte Frame Counter (TR1K)

GMAC Address: 0x19000090
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 512–1023 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TR1K	The transmit and receive 512–1023 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 512–1023 bytes in length inclusive (excluding framing bits but including FCS bytes).

8.20.27 Tx/Rx 1024-1518 Byte Frame Counter (TRMAX)

GMAC Address: 0x19000094
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 1024–1518 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TRMAX	The transmit and receive 1024-1518 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 1024-1518 bytes in length inclusive (excluding framing bits but including FCS bytes).

8.20.28 Tx/Rx 1519-1522 Byte VLAN Frame Counter (TRMGV)

GMAC Address: 0x19000098
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 1519–1522 bytes in length.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TRMGV	The transmit and receive 1519–1522 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 1519–1522 bytes in length inclusive (excluding framing bits but including FCS bytes).

8.20.29 Receive Byte Counter (RXBT)

GMAC Address: 0x1900009C
Access: Read/Write
Reset: 0x0

This register is used to count incoming frames and then increment this register accordingly.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:0	RBYT	The receive byte counter. This statistic count register is incremented by the byte count of all frames received, including bad packets but excluding framing bits but including FCS bytes.

8.20.30 Receive Packet Counter (RPKT)

GMAC Address: 0x190000A0
Access: Read/Write
Reset: 0x0

This register is used to count packets received.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	RPKT	The receive packet counter. This register is incremented for each received packet (including bad packets, all Unicast, broadcast and Multicast packets).

8.20.31 Receive FCS Error Counter (RFCS)

GMAC Address: 0x190000A4
Access: Read/Write
Reset: 0x0

This register is used to count frames received between 64–1518 in length and has a FCS error.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RFCS	The received FCS error counter. This register is incremented for each frame received that has an integral 64–1518 length and contains a frame check sequence error.

8.20.32 Receive Multicast Packet Counter (RMCA)

GMAC Address: 0x190000A8
Access: Read/Write
Reset: 0x0

This register is used to count received good standard multicast packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	RMCA	The receive multicast packet counter. This register is incremented for each multicast good frame of lengths smaller than 1518 (non-VLAN) or 1522 (VLAN) excluding broadcast frames. This does not include range/length errors.

8.20.33 Receive Broadcast Packet Counter (RBCA)

GMAC Address: 0x190000AC
Access: Read/Write
Reset: 0x0

This register is used to count received good broadcast frames.

Bit	Bit Name	Description
31:22	RES	Reserved. Must be written with zero. Contains zeros when read.
21:0	RBCA	The receive broadcast packet counter. This register is incremented for each broadcast good frame of lengths smaller than 1518 (non-VLAN) or 1522 (VLAN) excluding multicast frames. This does not include range or length errors.

8.20.34 Receive Control Frame Packet Counter (RXCF)

GMAC Address: 0x190000B0
Access: Read/Write
Reset: 0x0

This register is used to count received MAC control frames.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	RXCF	The receive control frame packet counter. This register is incremented for each MAC control frame received (pause and unsupported).

8.20.35 Receive Pause Frame Packet Counter (RXPF)

GMAC Address: 0x190000B4
Access: Read/Write
Reset: 0x0

This register is used to count received pause frame packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RXPF	The receive pause frame packet counter. This register is incremented each time a valid pause MAC control frame is received.

8.20.36 Receive Unknown OPCode Packet Counter (RXUO)

GMAC Address: 0x190000B8
Access: Read/Write
Reset: 0x0

This register is used to count received MAC control frames that contain an opcode.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RXUO	The receive unknown OPcode counter. This bit is incremented each time a MAC control frame is received which contains an opcode other than a pause.

8.20.37 Receive Alignment Error Counter (RALN)

GMAC Address: 0x190000BC
Access: Read/Write
Reset: 0x0

This register is used to count received packets with an alignment error.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RALN	The receive alignment error counter. This register is incremented for each received frame from 64–1518 bytes that contains an invalid FCS and is not an integral number of bytes.

8.20.38 Receive Frame Length Error Counter (RFLR)

GMAC Address: 0x190000C0
Access: Read/Write
Reset: 0x0

This register is used to count received frames that have a length error.

Bit	Bit Name	Description
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.
15:0	RFLR	The received frame length error counter. this register is incremented for each received frame in which the 802.3 length field did not match the number of data bytes actually received (46–1500 bytes). The counter is not incremented if the length field is not a valid 802.3 length, such as an EtherType value.

8.20.39 Receive Code Error Counter (RCDE)

GMAC Address: 0x190000C4
Access: Read/Write
Reset: 0x0

This register is used to count the number of received frames that had a code error counter.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RCDE	The receive code error counter. This register is incremented each time a valid carrier was present and at least one invalid data symbol was detected.

8.20.40 Receive Carrier Sense Error Counter (RCSE)

GMAC Address: 0x190000C8
Access: Read/Write
Reset: 0x0

This register is used to count the number of frames received that had a false carrier.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RCSE	The receive false carrier counter. This register is incremented each time a false carrier is detected during idle, as defined by a 1 on RX_ER and an 0xE on RXD. This event is reported along with the statistics generated on the next received frame. Only one false carrier condition can be detected and logged between frames.

8.20.41 Receive Undersize Packet Counter (RUND)

GMAC Address: 0x190000CC
Access: Read/Write
Reset: 0x0

This register is used to count the number of received packets that were undersized.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RUND	The receive undersize packet counter. This register is incremented each time a frame is received which is less than 64 bytes in length and contains a valid FCS and were otherwise well formed. This does not include Range Length errors

8.20.42 Receive Oversize Packet Counter (ROVR)

GMAC Address: 0x190000D0
Access: Read/Write
Reset: 0x0

This register is used to count received packets that were oversized.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	ROVR	The receive oversize packet counter., This register is incremented each time a frame is received which exceeded 1518 (non-VLAN) or 1522 (VLAN) and contains a valid FCS and were otherwise well formed. This does not include Range Length errors.

8.20.43 Receive Fragments Counter (RFRG)

GMAC Address: 0x190000D4
Access: Read/Write
Reset: 0x0

This register is used to count received fragmented frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RFRG	The receive fragments counter. This register is incremented for each frame received which is less than 64 bytes in length and contains an invalid FCS. This includes integral and non-integral lengths.

8.20.44 Receive Jabber Counter (RJBR)

GMAC Address: 0x190000D8
Access: Read/Write
Reset: 0x0

This register is used to count received jabber frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RJBR	The received jabber counter. This register is incremented for frames which exceed 1518 (non-VLAN) or 1522 (VLAN) bytes and contains an invalid FCS, including alignment errors.

8.20.45 Receive Dropped Packet Counter (RDRP)

GMAC Address: 0x190000DC
Access: Read/Write
Reset: 0x0

This register is used to count received dropped packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	RDRP	The received dropped packets counter. this register is incremented for frames received which are streamed to the system but are later dropped due to a lack of system resources.

8.20.46 Transmit Byte Counter (TXBT)

GMAC Address: 0x190000E0
Access: Read/Write
Reset: 0x0

This register is used to count transmitted bytes.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:0	TXBT	The transmit byte counter. This register is incremented by the number of bytes that were put on the wire including fragments of frames that were involved with collisions. This count does not include preamble/SFD or jam bytes.

8.20.47 Transmit Packet Counter (TPKT)

GMAC Address: 0x190000E4
Access: Read/Write
Reset: 0x0

This register is used to count transmitted packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TPKT	The transmit packet counter. This register is incremented for each transmitted packet (including bad packets, excessive deferred packets, excessive collision packets, late collision packets, all Unicast, Broadcast and Multicast packets.

8.20.48 Transmit Multicast Packet Counter (TMCA)

GMAC Address: 0x190000E8
Access: Read/Write
Reset: 0x0

This register is used to count transmitted multicast packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TMCA	Transmit multicast packet counter. Incremented for each multicast valid frame transmitted (excluding broadcast frames).

8.20.49 Transmit Broadcast Packet Counter (TBCA)

GMAC Address: 0x190000EC
Access: Read/Write
Reset: 0x0

This register is used to count transmitted broadcast packets.

Bit	Bit Name	Description
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.
17:0	TBCA	Transmit broadcast packet counter. Incremented for each broadcast frame transmitted (excluding multicast frames).

8.20.50 Transmit Pause Control Frame Counter (TXPF)

GMAC Address: 0x190000F0
Access: Read/Write
Reset: 0x0

This register is used to count transmitted pause control frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TXPF	Transmit pause frame packet counter. Incremented each time a valid pause MAC control frame is transmitted.

8.20.51 Transmit Deferral Packet Counter (TDFR)

GMAC Address: 0x190000F4
Access: Read/Write
Reset: 0x0

This register is used to count transmitted deferral packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TDFR	Transmit deferral packet counter. Incremented for each frame that was deferred on its first transmission attempt. Does not include frames involved in collisions.

8.20.52 Transmit Excessive Deferral Packet Counter (TEDF)

GMAC Address: 0x190000F8
Access: Read/Write
Reset: 0x0

This register is used to count excessive transmitted deferral packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TEDF	Transmit excessive deferral packet counter. Incremented for frames aborted that were deferred for an excessive period of time (3036 byte times).

8.20.53 Transmit Single Collision Packet Counter (TSCL)

GMAC Address: 0x190000FC
Access: Read/Write
Reset: 0x0

This register is used to count transmitted single collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TSCL	Transmit single collision packet counter. Incremented for each frame transmitted that experienced exactly one collision during transmission.

8.20.54 Transmit Multiple Collision Packet (TMCL)

GMAC Address: 0x19000100
Access: Read/Write
Reset: 0x0

This register is used to count transmitted multiple collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TMCL	Transmit multiple collision packet counter. Incremented for each frame transmitted that experienced 2–15 collisions (including any late collisions) during transmission as defined using the RETRY[3:0] field of the Tx function control register.

8.20.55 Transmit Late Collision Packet Counter (TLCL)

GMAC Address: 0x19000104
Access: Read/Write
Reset: 0x0

This register is used to count transmitted late collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TLCL	Transmit late collision packet counter. Incremented for each frame transmitted that experienced a late collision during a transmission attempt. Late collisions are defined using the LCOL[5:0] field of the Tx function control register.

8.20.56 Transmit Excessive Collision Packet Counter (TXCL)

GMAC Address: 0x19000108
Access: Read/Write
Reset: 0x0

This register is used to count excessive transmitted collision packets.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TXCL	Transmit excessive collision packet counter. Incremented for each frame that experienced 16 collisions during transmission and was aborted.

8.20.57 Transmit Total Collision Counter (TNCL)

GMAC0 Address: 0x1900010C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted total collision packets.

Bit	Bit Name	Description
31:13	RES	Reserved. Must be written with zero. Contains zeros when read.
12:0	TNCL	Transmit total collision counter. Incremented by the number of collisions experienced during the transmission of a frame as defined as the simultaneous presence of signals on the DO and RD circuits (i.e., transmitting and receiving at the same time). Note, this register does not include collisions that result in an excessive collision condition).

8.20.58 Transmit Pause Frames Honored Counter (TPFH)

GMAC Address: 0x19000110
Access: Read/Write
Reset: 0x0

This register is used to count honored transmitted pause frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TPFH	Transmit pause frames honored counter. Incremented each time a valid pause MAC control frame is transmitted and honored.

8.20.59 Transmit Drop Frame Counter (TDRP)

GMAC Address: 0x19000114
Access: Read/Write
Reset: 0x0

This register is used to count transmitted drop frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TDRP	Transmit drop frame counter. Incremented each time input PFH is asserted.

8.20.60 Transmit Jabber Frame Counter (TJBR)

GMAC Address: 0x19000118
Access: Read/Write
Reset: 0x0

This register is used to count transmitted jabber frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TJBR	Transmit jabber frame counter. Incremented for each oversized transmitted frame with an incorrect FCS value.

8.20.61 Transmit FCS Error Counter (TFCS)

GMAC Address: 0x1900011C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted FCS errors.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TFCS	Transmit FCS error counter. Incremented for every valid sized packet with an incorrect FCS value.

8.20.62 Transmit Control Frame Counter (TXCF)

GMAC Address: 0x19000120
Access: Read/Write
Reset: 0x0

This register is used to count transmitted control frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TXCF	Transmit control frame counter. Incremented for every valid size frame with a type field signifying a control frame.

8.20.63 Transmit Oversize Frame Counter (TOVR)

GMAC Address: 0x19000124
Access: Read/Write
Reset: 0x0

This register is used to count transmitted oversize frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TOVR	Transmit oversize frame counter. Incremented for each oversized transmitted frame with an correct FCS value.

8.20.64 Transmit Undersize Frame Counter (TUND)

GMAC Address: 0x19000128
Access: Read/Write
Reset: 0x0

This register is used to count transmitted undersize frames.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TUND	Transmit undersize frame counter. Incremented for every frame less then 64 bytes, with a correct FCS value.

8.20.65 Transmit Fragment Counter (TFRG)

GMAC Address: 0x1900012C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted fragments.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11:0	TFRG	Transmit fragment counter. Incremented for every frame less then 64 bytes, with an incorrect FCS value.

8.20.66 Carry Register 1 (CAR1)

GMAC Address: 0x19000130
Access: Read-Only
Reset: 0x0

Carry register bits are cleared on carry register write while the respective bit is asserted.

Bit	Bit Name	Description
31	C1_64	Carry register 1 TR64 counter carry bit
30	C1_127	Carry register 1 TR127 counter carry bit
29	C1_255	Carry register 1 TR255 counter carry bit
28	C1_511	Carry register 1 TR511 counter carry bit
27	C1_1K	Carry register 1 TR1K counter carry bit
26	C1_MAX	Carry register 1 TRMAX counter carry bit
25	C1_MGV	Carry register 1 TRMGV counter carry bit
24:17	RES	Reserved. Must be written with zero. Contains zeros when read.
16	C1_RBY	Carry register 1 RBYT counter carry bit
15	C1_RPK	Carry register 1 RPKT counter carry bit
14	C1_RFC	Carry register 1 RFCS counter carry bit
13	C1_RMC	Carry register 1 RMCA counter carry bit
12	C1_RBC	Carry register 1 RBCA counter carry bit
11	C1_RXC	Carry register 1 RXCF counter carry bit
10	C1_RXP	Carry register 1 RXPF counter carry bit
9	C1_RXU	Carry register 1 RXUO counter carry bit
8	C1_RAL	Carry register 1 RALN counter carry bit
7	C1_RFL	Carry register 1 RFLR counter carry bit
6	C1_RCD	Carry register 1 RCDE counter carry bit
5	C1_RCS	Carry register 1 RCSE counter carry bit
4	C1_RUN	Carry register 1 RUND counter carry bit
3	C1_ROV	Carry register 1 ROVR counter carry bit
2	C1_RFR	Carry register 1 RFRG counter carry bit
1	C1_RJB	Carry register 1 RJBR counter carry bit
0	C1_RDR	Carry register 1 RDRP counter carry bit

8.20.67 Carry Register 2 (CAR2)

GMAC Address: 0x19000134
Access: Read-Only
Reset: 0x0

Carry register bits are cleared on carry register write while the respective bit is asserted.

Bit	Bit Name	Description
31:20	RES	Reserved. Must be written with zero. Contains zeros when read.
19	C2_TJB	Carry register 2 TJBR counter carry bit
18	C2_TFC	Carry register 2 TFCS counter carry bit
17	C2_TCF	Carry register 2 TXCF counter carry bit
16	C2_TOV	Carry register 2 TOVR counter carry bit
15	C2_TUN	Carry register 2 TUND counter carry bit
14	C2_TFG	Carry register 2 TFRG counter carry bit
13	C2_TBY	Carry register 2 TBYT counter carry bit
12	C2_TPK	Carry register 2 TPKT counter carry bit
11	C2_TMC	Carry register 2 TMCA counter carry bit
10	C2_TBC	Carry register 2 TBCA counter carry bit
9	C2_TPF	Carry register 2 TXPF counter carry bit
8	C2_TDF	Carry register 2 TDFR counter carry bit
7	C2_TED	Carry register 2 TEDF counter carry bit
6	C2_TSC	Carry register 2 TSCL counter carry bit
5	C2_TMA	Carry register 2 TMCL counter carry bit
4	C2_TLC	Carry register 2 TLCL counter carry bit
3	C2_TXC	Carry register 2 TXCL counter carry bit
2	C2_TNC	Carry register 2 TNCL counter carry bit
1	C2_TPH	Carry register 2 TPFH counter carry bit
0	C2_TDP	Carry register 2 TDRP counter carry bit

8.20.68 Carry Mask Register 1 (CAM1)

GMAC Address: 0x19000138
Access: Read/Write
Reset: 0x1

When one of these mask bits is set to zero, the corresponding interrupt bit is allowed to cause interrupt indications on output CARRY.

Bit	Bit NaM1e	Description
31	M1_64	Mask register 1 TR64 counter carry bit
30	M1_127	Mask register 1 TR127 counter carry bit
29	M1_255	Mask register 1 TR255 counter carry bit
28	M1_511	Mask register 1 TR511 counter carry bit
27	M1_1K	Mask register 1 TR1K counter carry bit
26	M1_MAX	Mask register 1 TRMAX counter carry bit
25	M1_MGV	Mask register 1 TRMGV counter carry bit
24:17	RES	Reserved. Must be written with zero. Contains zeros when read.
16	M1_RBY	Mask register 1 RBYT counter carry bit
15	M1_RPK	Mask register 1 RPKT counter carry bit
14	M1_RFC	Mask register 1 RFCS counter carry bit
13	M1_RMC	Mask register 1 RMCA counter carry bit
12	M1_RBC	Mask register 1 RBCA counter carry bit
11	M1_RXC	Mask register 1 RXCF counter carry bit
10	M1_RXP	Mask register 1 RXPF counter carry bit
9	M1_RXU	Mask register 1 RXUO counter carry bit
8	M1_RAL	Mask register 1 RALN counter carry bit
7	M1_RFL	Mask register 1 RFLR counter carry bit
6	M1_RCD	Mask register 1 RCDE counter carry bit
5	M1_RCS	Mask register 1 RCSE counter carry bit
4	M1_RUN	Mask register 1 RUND counter carry bit
3	M1_ROV	Mask register 1 ROVR counter carry bit
2	M1_RFR	Mask register 1 RFRG counter carry bit
1	M1_RJB	Mask register 1 RJBR counter carry bit
0	M1_RDR	Mask register 1 RDRP counter carry bit

8.20.69 Carry Mask Register 2 (CAM2)

GMAC Address: 0x1900013C
Access: Read/Write
Reset: 0x1

When one of these mask bits is set to zero, the corresponding interrupt bit is allowed to cause interrupt indications on output CARRY.

Bit	Bit Name	Description
31:20	RES	Reserved. Must be written with zero. Contains zeros when read.
19	M2_TJB	Mask register 2 TJBR counter carry bit
18	M2_TFC	Mask register 2 TFCS counter carry bit
17	M2_TCF	Mask register 2 TXCF counter carry bit
16	M2_TOV	Mask register 2 TOVR counter carry bit
15	M2_TUN	Mask register 2 TUND counter carry bit
14	M2_TFG	Mask register 2 TFRG counter carry bit
13	M2_TBY	Mask register 2 TBYT counter carry bit
12	M2_TPK	Mask register 2 TPKT counter carry bit
11	M2_TMC	Mask register 2 TMCA counter carry bit
10	M2_TBC	Mask register 2 TBCA counter carry bit
9	M2_TPF	Mask register 2 TXPF counter carry bit
8	M2_TDF	Mask register 2 TDFR counter carry bit
7	M2_TED	Mask register 2 TEDF counter carry bit
6	M2_TSC	Mask register 2 TSCL counter carry bit
5	M2_TMA	Mask register 2 TMCL counter carry bit
4	M2_TLC	Mask register 2 TLCL counter carry bit
3	M2_TXC	Mask register 2 TXCL counter carry bit
2	M2_TNC	Mask register 2 TNCL counter carry bit
1	M2_TPH	Mask register 2 TPFH counter carry bit
0	M2_TDP	Mask register 2 TDRP counter carry bit

8.20.70 DMA Transfer Control for Queue 0 (DMATXCNTRL_Q0)

GMAC Address: 0x19000180
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 0

8.20.71 Descriptor Address for Queue 0 Tx (DMATXDESCR_Q0)

GMAC Address: 0x19000184
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 0
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

8.20.72 Transmit Status (DMATXSTATUS)

GMAC Address: 0x19000188
Access: Read/Write
Reset: 0x0

This register is used to set the bits and flags regarding the DMA controller and its transferring status.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:16	TXPKTCOUNT	This 8-bit Tx packet counter increments when the DMA controller transfers a packet successfully, and decrements when the host writes a 1 to TXPKTSENT (bit [0]).
15:12	RES	Reserved.
11	TX_UNDERRUN_Q3	Indicates TXUNDERRUN_Q3 as an interrupt source
10	TX_UNDERRUN_Q2	Indicates TXUNDERRUN_Q2 as an interrupt source
9	TX_UNDERRUN_Q1	Indicates TXUNDERRUN_Q1 as an interrupt source
8:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3	BUS_ERROR	Indicates that the DMA controller received a host/slave split, error, or retry response
2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	TXUNDERRUN_Q0	This bit is set when the DMA controller reads a set (1) empty flag in the descriptor it is processing
0	TXPKTSENT	Indicates that one or more packets transferred successfully. This bit is cleared when TXPKTCOUNT (bits [23:16]) is zero. Writing a 1 to this bit reduces TXPKTCOUNT by one.

8.20.73 Receive Control (DMARXCTRL)

GMAC Address: 0x1900018C
Access: Read/Write
Reset: 0x0

This register is used to enable the DMA to receive packets.

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	RXENABLE	Allows the DMA to receive packet transfers. When set, the built-in DMA controller begins receiving packets as the FIFO indicates they are available (FRSOF asserted). The DMA controller clears this bit when it encounters an RX overflow or bus error state.

8.20.74 Pointer to Receive Descriptor (DMARXDESCR)

GMAC Address: 0x19000190
Access: Read/Write
Reset: 0x0

This register is used to find the location of the first TX packet descriptor in the memory.

Bit	Bit Name	Description
31:2	DESCRIPTOR_ ADDRESS	The descriptor address. When the RXENABLE (bit [0] of the Receive Control (DMARXCTRL), page 8-330 register) is set by the host, the DMA controller reads this register to find the host memory location of the first receive packet descriptor.
1:0	RES	Ignored by the DMA controller, because it is a requirement of the system that all descriptors are 32-bit aligned in the host memory.

8.20.75 Receive Status (DMARXSTATUS)

GMAC Address: 0x19000194
Access: Read/Write
Reset: 0x0

This register is used to set the bits and flags regarding the DMA controller and its receiving status.

Bit	Bit Name	Description
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.
23:16	RXPKTCOUNT	This 8-bit receive packet counter increments when the DMA controller transfers a packet successfully, and decrements when the host writes a 1 to RXPKTRECEIVED (bit [0]).
15:4	RES	Reserved. Must be written with zero. Contains zeros when read.
3	BUSERROR	Indicates that the DMA controller received a host/slave split, error, or retry response
2	RXOVERFLOW	This bit is set when the DMA controller reads a set empty flag in the descriptor it is processing
1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	RXPKT RECEIVED	Indicates that one or more packets were received successfully. This bit is cleared when the RXPKTCOUNT (bits [23:16]) is zero. Writing a 1 to this bit reduces RXPKTCOUNT by one.

8.20.76 Interrupt Mask (DMAINTRMASK)

GMAC Address: 0x19000198
Access: Read/Write
Reset: 0x0

This register is used to configure interrupt masks for the DMA. Setting a bit to 1 enables the corresponding status signal as an interrupt source. The register "DMA Interrupts" is the AND of DMA status bits with this register.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11	TX_UNDERRUN_Q3_MASK	Setting this bit 1 enables TXUNDERRUN_Q3(bit [11] in the Transmit Status (DMATXSTATUS), page 8-329 register) as an interrupt source
10	TX_UNDERRUN_Q2_MASK	Setting this bit 1 enables TXUNDERRUN_Q2 (bit [10] in the Transmit Status (DMATXSTATUS), page 8-329 register) as an interrupt source
9	TX_UNDERRUN_Q1_MASK	Setting this bit 1 enables TXUNDERRUN_Q1 (bit [9] in the Transmit Status (DMATXSTATUS), page 8-329 register) as an interrupt source
8	RES	Reserved. Must be written with zero. Contains zeros when read.
7	BUS_ERROR_MASK	Setting this bit to 1 enables BUSERROR (bit [3] in the Receive Status (DMARXSTATUS), page 8-330 register) as an interrupt source
6	RX_OVERFLOW_MASK	Setting this bit to 1 enables RXOVERFLOW (bit [1] in the Receive Status (DMARXSTATUS), page 8-330 register) as in interrupt source
5	RES	Reserved. Must be written with zero. Contains zeros when read.
4	RXPKTRECEIVED_MASK	Enables RXPKTRECEIVED (bit [0] in the Receive Status (DMARXSTATUS), page 8-330 register) as an interrupt source
3	BUSERROR_MASK	Setting this bit to 1 enables BUSERROR (bit [3] in the Transmit Status (DMATXSTATUS), page 8-329 register) as an interrupt source
2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	TX_UNDERRUN_Q0_MASK	Setting this bit 1 enables TXUNDERRUN_Q0 (bit [1] in the Transmit Status (DMATXSTATUS), page 8-329 register) as an interrupt source
0	TXPKTSENT_MASK	Setting this bit to 1 enables TXPKTSENT (bit [0] in the Transmit Status (DMATXSTATUS), page 8-329 register) as an interrupt source

8.20.77 Interrupts (DMAINTERRUPT)

GMAC Address: 0x1900019C
Access: Read/Write
Reset: 0x0

This register is used to configure interrupts for the DMA. Flags in this register clear when their corresponding Status bit is cleared.

Bit	Bit Name	Description
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.
11	TX_UNDERRUN_Q3	Setting this bit 1 enables TXUNDERRUN_Q3(bit [11] in the Transmit Status (DMATXSTATUS), page 8-329 register) as an interrupt source
10	TX_UNDERRUN_Q2	Setting this bit 1 enables TXUNDERRUN_Q2 (bit [10] in the Transmit Status (DMATXSTATUS), page 8-329 register) as an interrupt source
9	TX_UNDERRUN_Q1	Setting this bit 1 enables TXUNDERRUN_Q1 (bit [9] in the Transmit Status (DMATXSTATUS), page 8-329 register) as an interrupt source
8	RES	Reserved. Must be written with zero. Contains zeros when read.
7	BUS_ERROR_MASK	Setting this bit to 1 records an Rx bus error interrupt when BUS_ERROR (bit [3] in the Receive Status (DMARXSTATUS), page 8-330 register) and BUS_ERROR_MASK (bit [7] of the Interrupt Mask (DMAINTRMASK), page 8-331 register) are both set
6	RX_OVERFLOW_MASK	Setting this bit to 1 records an Rx overflow error interrupt when RX_OVERFLOW (bit [1] in the Receive Status (DMARXSTATUS), page 8-330 register) and RX_OVERFLOW_MASK (bit [6] of the Interrupt Mask (DMAINTRMASK), page 8-331 register) are both set
5	RES	Reserved. Must be written with zero. Contains zeros when read.
4	RXPKT_RECEIVED_MASK	Records a RX_PKT_RECEIVED error interrupt when RX_PKT_RECEIVED (bit [0] in the Receive Status (DMARXSTATUS), page 8-330 register) and RXPKT_RECEIVED_MASK (bit [4] of the Interrupt Mask (DMAINTRMASK), page 8-331 register) are both set
3	BUS_ERROR	Setting this bit to 1 enables BUSERROR (bit [3] in the Transmit Status (DMATXSTATUS), page 8-329 register) and BUSERROR_MASK (bit [3] of the Interrupt Mask (DMAINTRMASK), page 8-331 register) are both set
2	RES	Reserved. Must be written with zero. Contains zeros when read.
1	TX_UNDERRUN_Q0	Setting this bit to 1 enables TX_UNDERRUN (bit [1] in the Transmit Status (DMATXSTATUS), page 8-329 register) and TX_UNDERRUN_MASK (bit [1] of the Interrupt Mask (DMAINTRMASK), page 8-331 register) are both set
0	TXPKTSENT	Set this bit to 1 enables TXPKTSENT (bit [0] in the Transmit Status (DMATXSTATUS), page 8-329 register) and TXPKTSENT_MASK (bit [0] of the Interrupt Mask (DMAINTRMASK), page 8-331 register) are both set

8.20.78 Ethernet TX Burst (ETH_ARB_TX_BURST)

GMAC Address: 0x190001A0
Access: Read/Write
Reset: 0x48

Tx and Rx requests are arbitrated based on these parameters. These parameters ensure DDR bandwidth is available to both Tx and Rx until the specified number of DWs transfer. Note that this affects the bandwidth/latency of the data for transmit and receive.

Bit	Bit Name	Description
31:26	RES	Reserved
25:16	MAX_RCV_BURST	Maximum number of DWs to be continuously allowed for Rx
15:10	RES	Reserved
9:0	MAX_TX_BURST	Maximum number of DWs to be continuously allowed for Tx

8.20.79 Current Tx and Rx FIFO Depth (ETH_XFIFO_DEPTH)

GMAC Address: 0x190001A8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:26	RES	Reserved
25:16	CURRENT_RX_FIFO_DEPTH	Current Rx FIFO depth
15:10	RES	Reserved
9:0	CURRENT_TX_FIFO_DEPTH	Current Tx FIFO depth

8.20.80 Ethernet Transmit FIFO Throughput (ETH_TXFIFO_TH)

GMAC Address: 0x190001A4
Access: Read/Write
Reset: See field description

This Ethernet register has a 2 KB Tx FIFO. It is use to determine the minimum and maximum levels of the transfer FIFO and correspondingly keep the transmit levels within the range to keep a continuous data transfer flowing.

Bit	Bit Name	Reset	Description
31:26	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
25:16	TXFIFO_MAXTH	0x1D8	This bit represents the maximum number of double words in the Tx FIFO, and once this limit is surpassed, this bit should be de-asserted
15:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:0	TXFIFO_MINTH	0x160	This bit specifies the minimum number of double words in the Tx FIFO, and if it is less than this value, this bit needs to be asserted.

8.20.81 Ethernet Receive FIFO Threshold (ETH_RXFIFO_TH)

GMAC Address: 0x190001AC
Access: Read/Write
Reset: See field description

This Ethernet register has a 2 KB Rx FIFO. It is used to determine the minimum and maximum levels of the transfer FIFO and correspondingly keep the transmit levels within the range to keep a continuous data transfer flowing.

Bit	Bit Name	Reset	Description
31:10	SCRATCHREG_0	0x28	This bit is a pure scratch pad register that can be used by the CPU for any general purpose.
9:0	RCVFIFO_MINTH	0x0	The minimum number of double words in the receive FIFO. Once this number is reached, this bit needs to be asserted.

8.20.82 Ethernet Free Timer (ETH_FREE_TIMER)

GMAC Address: 0x190001B8
Access: Read/Write
Reset: See field description

This register updates the Ethernet descriptors with time stamps

Bit	Bit Name	Reset	Description	
31	TIMER_UPDATE	0x1	0	Timer update at the AHB_CLK
			1	Free timer at the AHB_CLK/4
30:21	SCRATCHREG_1	0x0	The pure general purpose register for use by the CPU	
20:0	FREE_TIMER	0x3FFFFF	Free timer	

8.20.83 DMA Transfer Control for Queue 1 (DMATXCNTRL_Q1)

GMAC0 Address: 0x190001C0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 1

8.20.84 Descriptor Address for Queue 1 Tx (DMATXDESCR_Q1)

GMAC Address: 0x190001C4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 1
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

8.20.85 DMA Transfer Control for Queue 2 (DMATXCNTRL_Q2)

GMAC Address: 0x190001C8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 2

8.20.86 Descriptor Address for Queue 2 Tx (DMATXDESCR_Q2)

GMAC Address: 0x190001CC
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 2
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

8.20.87 DMA Transfer Control for Queue 3 (DMATXCNTRL_Q3)

GMAC Address: 0x190001D0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.
0	TX_ENABLE	Enables queue 3

8.20.88 Descriptor Address for Queue 3 Tx (DMATXDESCR_Q3)

GMAC Address: 0x190001D4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 3
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.

8.20.89 DMA Transfer Arbitration Configuration (DMATXARBCFG)

GMAC Address: 0x190001D8
Access: Read/Write
Reset: See field description

This register is used to select the type of arbitration used for the QoS feature and the weight to be assigned to a particular queue. Note that a weight of zero is not permitted and causes the hardware to misbehave.

Bit	Bit Name	Reset	Description	
31:26	WGT3	0x1	The weight for Queue 3, if WRR has been selected	
25:20	WGT2	0x2	The weight for Queue 2, if WRR has been selected	
19:14	WGT1	0x4	The weight for Queue 1, if WRR has been selected	
13:8	WGT0	0x8	The weight for Queue 0, if WRR has been selected	
7:1	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
0	RRMODE	0x4	Round robin mode	
			0	Simple priority (Q0 highest priority)
			1	Weighted round robin (WRR)

8.20.90 Tx Status and Packet Count for Queues 1 to 3 (DMATXSTATUS_123)

GMAC0 Address: 0x190001E4
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:24	RES	Reserved
23:16	TXPKTCOUNT_CH3	8-bit Tx packet counter that increments when the built-in DMA controller successfully transfers a packet for queue 3, and decrements when the host writes a 1 to bit TXPKTSENT for chain 3 in the DMATXSTATUS register. Default is 0.
15:8	TXPKTCOUNT_CH2	8-bit Tx packet counter that increments when the built-in DMA controller successfully transfers a packet for queue 2, and decrements when the host writes a 1 to bit TXPKTSENT for chain 2 in the DMATXSTATUS register. Default is 0.
7:0	TXPKTCOUNT_CH1	8-bit Tx packet counter that increments when the built-in DMA controller successfully transfers a packet for queue 1, and decrements when the host writes a 1 to bit TXPKTSENT for chain 1 in the DMATXSTATUS register. Default is 0.

8.20.91 Local MAC Address Dword0 (LCL_MAC_ADDR_DW0)

GMAC0 Address: 0x19000200
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_MAC_ADDR_DW0	Bits [31:0] of the local L2 MAC address

8.20.92 Local MAC Address Dword1 (LCL_MAC_ADDR_DW1)

GMAC0 Address: 0x19000204
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	LOCAL_MAC_ADDR_DW1	Bits [47:32] of the local L2 MAC address

8.20.93 Next Hop Router MAC Address Dword0 (NXT_HOP_DST_ADDR_DW0)

GMAC0 Address: 0x19000208
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_MAC_DST_ADDR_DW0	Bits [31:0] of the next hop router's local L2 MAC address

8.20.94 Next Hop Router MAC Destination Address Dword1 (NXT_HOP_DST_ADDR_DW1)

GMAC0 Address: 0x1900020C
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:16	RES	Reserved
15:0	LOCAL_MAC_DST_ADDR_DW1	Bits [47:32] of the local L2 MAC address

8.20.95 Local Global IP Address 0 (GLOBAL_IP_ADDR0)

GMAC0 Address: 0x19000210
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_GLOBAL_IP_ADDR0	Local IP address 0 (up to 4 global IP addresses are supported)

8.20.96 Local Global IP Address 1 (GLOBAL_IP_ADDR1)

GMAC Address: 0x19000214
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_GLOBAL_IP_ADDR1	Local IP address 1 (up to 4 global IP addresses are supported)

8.20.97 Local Global IP Address 2 (GLOBAL_IP_ADDR2)

GMAC0 Address: 0x19000218
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_GLOBAL_IP_ADDR2	Local IP address 2 (up to 4 global IP addresses are supported)

8.20.98 Local Global IP Address 3 (GLOBAL_IP_ADDR3)

GMAC0 Address: 0x1900021C
Access: Read/Write
Reset: 0x0

NOTE This register is available only for GE0 MAC.

Bit	Bit Name	Description
31:0	LOCAL_GLOBAL_IP_ADDR3	Local IP address 3 (up to 4 global IP addresses are supported)

8.21 Serial Flash SPI Controller Registers

Table 8-24 summarizes the serial flash SPI controller registers for the QCA9563.

Table 8-24 Serial Flash SPI Controller Registers Summary

Address	Name	Description	Page
0x1F000000	FUNCTION_SELECT_ADDR	SPI Controller GPIO Mode Select	page 340
0x1F000004	SPI_CONTROL_ADDR	SPI Address Control	page 340
0x1F000008	SPI_IO_CONTROL_ADDR	SPI I/O Address Control	page 341
0x1F00000C	SPI_READ_DATA_ADDR	SPI Read Data Address	page 341
0x1F000010	SPI_SHIFT_DATAOUT_ADDR	SPI Data to Shift Out	page 341
0x1F000014	SPI_SHIFT_CNT_ADDR	SPI Content to Shift Out or In	page 342
0x1F000018	SPI_SHIFT_DATAIN_ADDR	SPI Data to Shift In	page 342

8.21.1 SPI Controller GPIO Mode Select (FUNCTION_SELECT_ADDR)

Address: 0x1F000000
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:1	RES	Reserved
0	FUNCTION_SELECT	Writing a non-zero value to this register selects the GPIO mode for the SPI controller.

8.21.2 SPI Address Control (SPI_CONTROL_ADDR)

Address: 0x1F000004
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:14	RES	Reserved
13:8	TSHSL_CNT	Minimum time for which CS has must be deasserted between two SPI transactions.
7	SPI_RELOCATE	When this bit is set, 16 MB of SPI space is mapped to 0x1E00_0000, else it is mapped to 0x1F00_0000.
6	REMAP_DISABLE	Disables the alias of the lower 4 MB of SPI space, enabling the ROM to boot from 0x1FC_0000 to alias to 0x1F0_0000 until software disables the aliasing.
5:0	CLOCK_DIVIDER	The clock divider is based on the AHB clock. The generated clock is AHBclock/((CLOCK_DIVIDER+1) * 2).

8.21.3 SPI I/O Address Control (SPI_IO_CONTROL_ADDR)

Address: 0x1F000008
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description	
31:19	RES	Reserved	
18	IO_CS2	Chip select 2. Active low signal.	
		0	Enable chip select 2
		1	Disable chip select 2
17	IO_CS1	Chip select 1. Active low signal.	
16	IO_CS0	Chip select 0. Active low signal.	
15:9	RES	Reserved	
8	IO_CLK	SPI clock	
7:1	RES	Reserved	
0	IO_DO	Data out	

8.21.4 SPI Read Data Address (SPI_READ_DATA_ADDR)

Address: 0x1F00000C
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	READ_DATA	The SPI read data is shifted in and sampled every cycle

8.21.5 SPI Data to Shift Out (SPI_SHIFT_DATAOUT_ADDR)

Address: 0x1F000010
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	SHIFT_DATAOUT	The data (either CMD, ADDR, or DATA) to be shifted out every clock cycle

8.21.6 SPI Content to Shift Out or In (SPI_SHIFT_CNT_ADDR)

Address: 0x1F000014
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31	SHIFT_EN	Enables shifting data out
30	SHIFT_CHNL	If set to 1, enables chip select 2
29		If set to 1, enables chip select 1
28		If set to 1, enables chip select 0
27	SHIFT_CLKOUT	Initial value of the clock signal
26	TERMINATE	When set to 1, deasserts the chip select
25:7	RES	Reserved
6:0	SHIFT_COUNT	The number of bits to be shifted out or shifted in on the data line

8.21.7 SPI Data to Shift In (SPI_SHIFT_DATAIN_ADDR)

Address: 0x1F000018
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
31:0	SHIFT_DATAIN	SPI read data

9 Electrical Characteristics

9.1 Absolute Maximum Ratings

Table 9-1 summarizes the absolute maximum ratings and Table 9-2 lists the recommended operating conditions for the QCA9563.

Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 9-1 Absolute Maximum Ratings

Symbol	Parameter	Max Rating	Unit
V_{DD33}	Supply Voltage	-0.3 to 3.6	V
V_{DD25}	Maximum I/O Supply Voltage	-0.3 to 2.75	V
V_{DD12}	Core Voltage	-0.3 to 1.29	V
T_{store}	Storage Temperature	-40 to 150	°C
T_j	Junction Temperature	125	°C
ESD	Electrostatic Discharge Tolerance	2000	V

9.2 Recommended Operating Conditions

Table 9-2 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD33}	Supply Voltage	±5%	3.15	3.3	3.46	V
V_{DD25}	I/O Supply Voltage[1]	±5%	2.49	2.62	2.75	V
V_{DD12}	Core Voltage[2]	±5%	1.17	1.23	1.29	V
A_{VDD12}	Analog Voltage[2]	±5%	1.17	1.23	1.29	V
V_{DD_DDR}	DDR1 I/O Voltage[1]	±5%	2.47	2.6	2.73	V
	DDR2 I/O Voltage[1]	±5%	1.71	1.8	1.89	V
T_{case}	Case Temperature	—	0	—	115	°C
Psi_{JT}	Thermal Parameter[3]	—	—	—	2.5	°C/W

1. Voltage regulated internally by the QCA9563
2. V_{DD12} and AV_{DD12} voltage values are tentative
3. 4.The thermal parameter is for the 13x13 mm DRQFN package.

9.3 25 MHz Clock Characteristics

When using an external clock (TCXO), the XTALI pin is grounded and the XTALO pin should be driven with a square wave clock.

AC coupling is recommended for the clock signal to the XTALO pin.

The internal circuit provides the DC bias of approximately 0.6 V. The peak to peak swing of the external clock can be between 0.3 V to 1.2 V. In general, larger swings and sharper edges will reduce jitter, but introduce the potential of high frequency spurious tones.

The phase noise of the oscillator should be lower than -145 dBc/Hz at 100 KHz carrier offset.

Table 9-3 Clock Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INMAX}	Input Voltage Maximum	—	—	—	1.4	V
V_{INMIN}	Input Voltage Minimum[1]	—	-0.2	—	—	V
T_{DCycle}	Duty Cycle	—	40	50	60	%
TRise	Clock Rise Time	—	—	—	2[2]	ns
TFall	Clock Fall Time	—	—	—	2[2]	ns

1. V_{INMAX} of -0.2 V is limited by the ESD protection diode. If V_{INMAX} is less than -0.2 V, the ESD diode turns on and protects the chip
2. The 2 ns rise/fall time specification is for TCXO input only, does not apply when using a XTAL.

9.4 Radio Characteristics

The following conditions apply to the typical characteristics unless otherwise specified:

VDD12 = 1.23 V

VDD33 = 3.3 V, T_{amb} = 25 °C

9.4.1 Radio Receiver Characteristics

Table 9-4 summarizes the QCA9531 receiver characteristics. These conditions apply to the typical characteristics unless otherwise specified: VDD12 = 1.2 V, VDD33 = 3.3 V, Tamb = 25°C.

Table 9-4 Radio Receiver Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receiver input frequency range	5 MHz center frequency	2.412	—	2.472	GHz
NF	Receive chain noise figure	See note[1]	—	5.5	—	dB
S_{rF}	Sensitivity					
	CCK, 1 Mbps	See note[2]	—	-97	—	dBm
	CCK, 11 Mbps		-76	-88	—	
	OFDM, 6 Mbps		-82	-91	—	
	OFDM, 54 Mbps		-65	-78	—	
	HT20, MCS0, 1 stream, 3 Tx, 3 Rx		-82	-90	—	
	HT20, MCS7, 1 stream, 3 Tx, 3 Rx		-64	-75	—	
	HT20, MCS8, 2 stream, 3 Tx, 3 Rx		-82	-90	—	
	HT20, MCS15, 2 stream, 3 Tx, 3 Rx		-64	-71	—	
	HT20, MCS16, 3 stream, 3 Tx, 3 Rx		-82	-90	—	
	HT20, MCS23, 3 stream, 3 Tx, 3 Rx		-64	-71	—	
	HT40, MCS0, 1 stream, 3 Tx, 3 Rx		-79	-89	—	
	HT40, MCS7, 1 stream, 3 Tx, 3 Rx		-61	73	—	
	HT40, MCS8, 2 stream, 3 Tx, 3 Rx		-79	-89	—	
	HT40, MCS15, 2 stream, 3 Tx, 3 Rx		-61	-69	—	
	HT40, MCS16, 3 stream, 3 Tx, 3 Rx		-79	-89	—	
	HT40, MCS23, 3 stream, 3 Tx, 3 Rx		-61	-69	—	
IP1	Input 1 dB compression (min. gain)	—	—	-0.5	—	dBm
IIP1	Input third intercept point (min. gain)	—	—	8	—	dBm
Z_{RFin_input}	Recommended LNA differential drive impedance	See note[3]	—	25.6-j1.2	—	^
ER_{phase}	I, Q phase error	See note[4]	—	TBD	—	°
ER_{amp}	I, Q amplitude error	—	—	TBD	—	°

Table 9-4 Radio Receiver Characteristics for 2.4 GHz Operation

Radj	Adjacent channel rejection					
	CCK, 2L	10 to 20 MHz[5]	35	39	—	dB
	OFDM, 6 Mbps		16	34	—	
	OFDM, 54 Mbps		-1	19	—	
	HT20, MCS0		16	34	—	
	HT40, MCS0		16	24	—	
TR_{powup}	Time for power up (from synthesizer)	—	—	1.5	—	µs

1. The noise figure computation includes the baseband gain stages along with LNA.
2. Sensitivity performance based on Qualcomm Atheros reference design, which includes a Tx/Rx antenna switch. Minimum values based on IEEE 802.11 specifications.
3. Estimated values
4. These are residual values after applying IQ calibration at chip level
5. Typical values measured with reference design. Minimum values based on IEEE 802.11 specifications.

9.4.2 Transmitter Characteristics

Table 9-5 summarizes the transmitter characteristics for the QCA9563.

Table 9-5 Transmitter Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	5 MHz center frequency	2.142	—	2.472	GHz
P_{out}	Mask compliant power					
	1 Mbps	See note[1]	—	—	—	dBm
	6 Mbps		—	19	—	
	HT20, MCS0		—	18	—	
	HT40, MCS0		—	17	—	
	EVM compliant power					
	54 Mbps	See note[1]	—	15	—	
	HT20, MCS23		—	13	—	
	HT40, MCS23		—	12	—	
SP_{gain}	PA gain step	See note[2]	—	0.5	—	dB
A_{pl}	Accuracy of power leveling loop	See note[3]	—	±2	—	dB
Z_{RFout_load}	Recommended PA differential load impedance	See note[4]	—	172+j147	—	^
OP1dB	Output P1dB (max. gain)	See note[5]	21.5	22.5	—	dBm
OIP3	Output third order intercept point (max. gain)	—	31	32	—	dBm
ER_{phase}	I, Q phase error	—	—	±/1	—	°
ERamp	I, Q amplitude error	—	—	±/-0.1	—	dB
RS	Synthesizer reference spur	—	< -45	-52	—	dBc
TT_{powup}	Time for power up	—	—	1.5	—	µs

1. Measures using the Internal PA recommended by Qualcomm Atheros under open-loop power control.
2. Guaranteed by design.
3. Manufacturing calibration required.
4. See the impedance matching circuit in the Qualcomm Atheros reference design schematics. To achieve good RF performance, it is strongly recommended not to alter the RF portion of the Qualcomm Atheros reference design for different matching networks.
5. Measured at the antenna connector port of the reference design, which includes Tx/Rx antenna switch.

9.4.3 Synthesizer Characteristics

Table 9-6 summarizes the synthesizer characteristics for the QCA9563.

Table 9-6 Synthesizer Composite Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_n	Phase noise (at Tx_Out)	—	2.142	—	2.472	GHz
	At 30 KHz offset	—	-90	-92		dBc/Hz
	At 100 KHz offset	—	-90	-94	—	
	At 500 KHz offset	—	-105	-111	—	
	At 1 MHz offset	—	-110	-117	—	
Fc	Center channel frequency	±20 ppm[1]	2.412		2.472	GHz
Fref	Reference oscillator frequency	—	—	25	—	MHz
TS_{powup}	Time for power up	—	—	200	—	µs

1. Manufacturing calibration is required; And is over temperature and aging.

9.5 Power Consumption

Table 9-7 Power Consumption for 2.4 GHz Operation (external PA)

Operating Mode[1]	Total 3.3 V Power Supply[2]				VDD12 (mA)[3]	VDD25 (mA)[3]
	VDD33 + VDD33_RF (mA)	QCA9563PA (mA)	VDD_DDR1.8V (mA)	AR8337NVDD33 _S17 (mA)		
Tx (three-chain at 22 dBm)	483	920	22	360	480	3.8
Rx (three-chain)	390	28	22.4	364	570	4

1. Internal 2.4 GHz radio, external PA, PCIE RC interface, USB and internal switch are all in maximum data transfer condition and the CPU in maximum utilization
2. The current consumption from 3.3 V includes analog, RF, USB and the 1.2 V power as the internal switching regulator is used
3. Current consumption of the VDD_DDR, VDD25, and VDD12 power rails from the QCA9563

10 AC Specifications

10.1 DDR Interface Timing

Figure 10-1 and Table 10-1 show the DDR Interface Timing requirements.

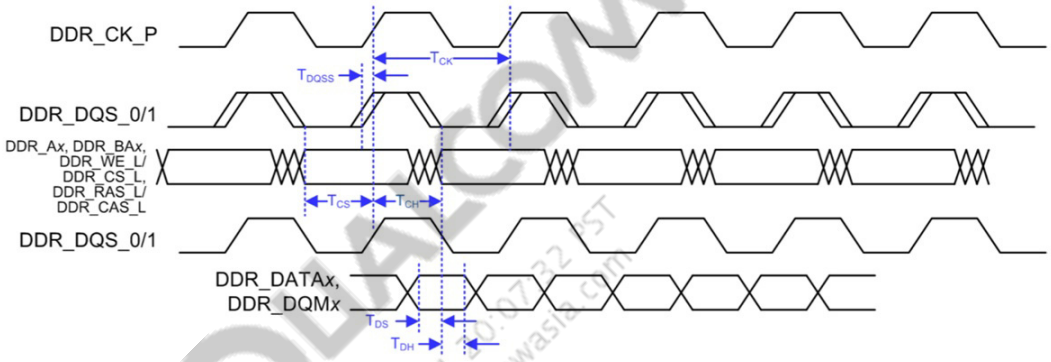


Figure 10-1 DDR Interface Timing

Table 10-1 DDR Interface Timing

Parameter	Reference Signal	Min	Max	Comments
T_{CK}	—	3.0 ns	—	Normal Period of CK_P clock output signal
T_{IS}	DDR_CK_P	1.3 ns	—	ADDR/CMD setup time before DDR_CK_P rising edge
T_{IH}	DDR_CK_P	1.3 ns	—	ADDR/CMD hold time after DDR_CK_P rising edge
T_{DQSS}	DDR_CK_P	—	0.2 ns	CLK_DQS skew
T_{DS}	DDR_DQS_0/1	0.55 ns	—	DQ setup time before DQS rising/falling edge
T_{DH}	DDR_DQS_0/1	0.55 ns	—	DQ hold time before DQS rising/famming edge

10.2 DDR Input Timing

Figure 10-2 illustrates the DDR input timing.

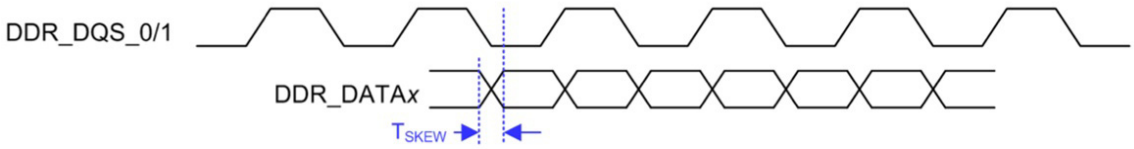


Figure 10-2 DDR Input Timing

Table 10-2 shows the values for DDR input timing.

Table 10-2 DDR input timing

Parameter	Reference Signal	Min	Max	Comments
T_{SKEW}	DDR_DQS_0/1	—	0.4 ns	Maximum skew from DQS to DQ stable from memory

10.3 SPI Timing

Figure 10-3 shows the timing for SPI .

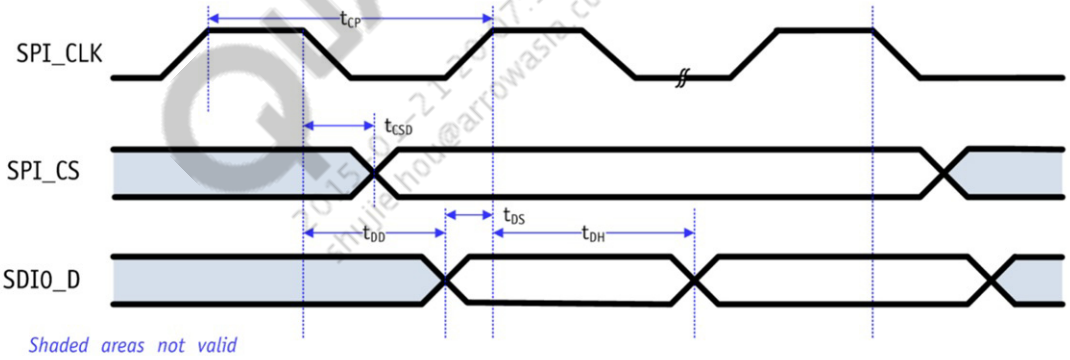


Figure 10-3 SPI timing

Table 10-3 shows the values for timing constraints for SPI .

Table 10-3 SPI Master Timing Constraints

Parameter	Reference Signal	Min	Max	Comments
t_{CP}	—	40 ns	—	SPI clock period
t_{CSD}	SPI_CLK	—	7 ns	Maximum CS delay from SPI_CLK falling edge
t_{DD}	SPI_CLK	—	6 ns	Maximum data delay from SPI_CLK falling edge
t_{DS}	SPI_CLK	7 ns	—	Maximum data setup time before SPI_CLK rising edge
t_{DH}	SPI_CLK	0 ns	—	Minimum data hold time after SPI_CLK rising edge

10.4 Power on Sequence

Figure 10-4 illustrates the power on sequence.

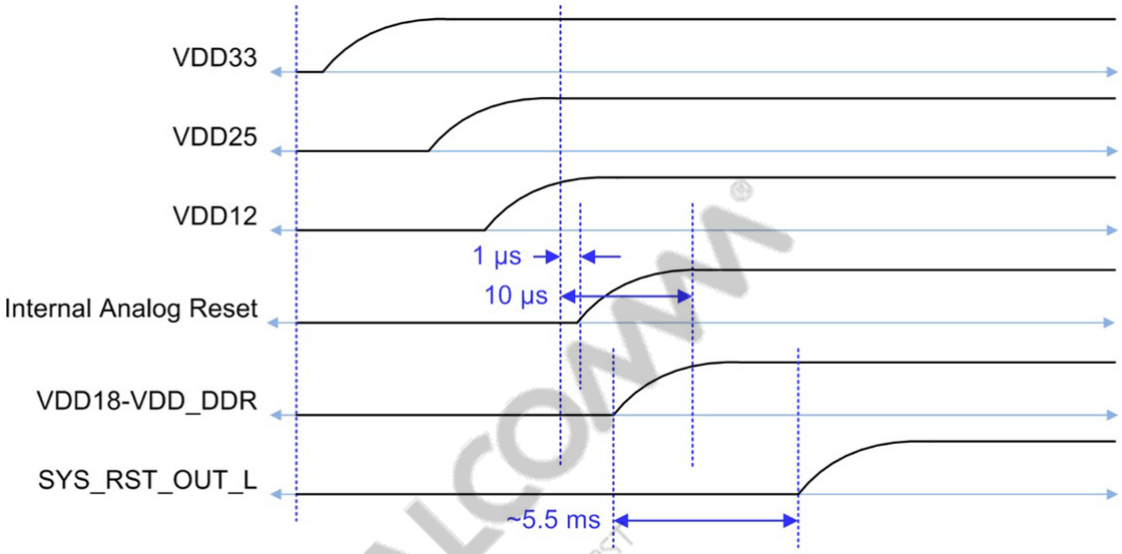


Figure 10-4 Power on sequence

11 Part Reliability

11.1 Reliability Qualifications Summary

Table 11-1 QCA9563 Reliability Evaluation

Reliability Tests, Standards and Conditions	Sample Size	Results
Average failure rate (AFR, λ) in FIT **Failure in billion device-hours** Functional HTOL: JESD22-A108	231	λ = 12.1 FIT
Mean time to failure (MTTF, million hours) t = 1/λ	231	82.3
ESD – (HBM) human body model rating JESD22-A114	3	Pass; ± 2000 V; all pins
ESD – (CDM) charge device model rating JESD22-C101-D	3	Pass; ± 500V; all pins
Latch-up (I-test): EIA/JESD78 Trigger current: ±100 mA; Temperature: 85°C	6	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78 Trigger voltage: 1.5x V; Temperature: 85°C	6	Pass
Moisture resistance test (MRT): MSL3; J-STD-020D,(30C/60%RH, 192 hrs,3xIR@260°C)	1078	Pass
Temperature cycle: JESD22-A104 Temperature: -60°C to +150°C Number of cycles: 1000 Min soak time at min/max temperature: 5 minutes Cycle rate: 2 cycles per hour (cph) **Preconditioning**: JESD22-A113 **MSL: 3;** (30C/60%RH, 192 hrs, 3xIR@260°C)	462	Pass
Biased highly accelerated stress test (BHAST) JESD22-A110 **Preconditioning**: JESD22-A113 **MSL: 3;** (30C/60%RH, 192 hrs,3xIR@260°C)	154	Pass
Unbiased highly accelerated stress test (UHAST) JESD22-A118 **Preconditioning**: JESD22-A113 **MSL: 3;** (30C/60%RH, 192 hrs,3xIR@260°C)	462	Pass
High temperature storage life: JESD22-A103 Temperature 150°C, 1000 hours	462	Pass
Physical dimensions: JESD22-B100 Package outline drawing: NT90-Y5244	30	Pass
Solder ball shear stress test: JESD22-B117	N/A	N/A

11.2 Qualification Sample Description

Table 11-2 QCA9563 Device Characteristics

Device name	QCA9563
Package type	DRFQN
Package body size	13 mm x 13 mm
Lead count	164
Lead composition	Matte Tin
Fab process	55 nm CMOS
Pin pitch	0.5 mm

12 Package Dimensions

The QCA9563 is packaged in a dual-row QFN package. The body size is 13 mm by 13 mm.

Moisture Sensitivity Level (MSL) for this device is L3 per JSTD020D-01.

The A-type package drawings and dimensions are provided in Figure 12-1 and Table 12-1.

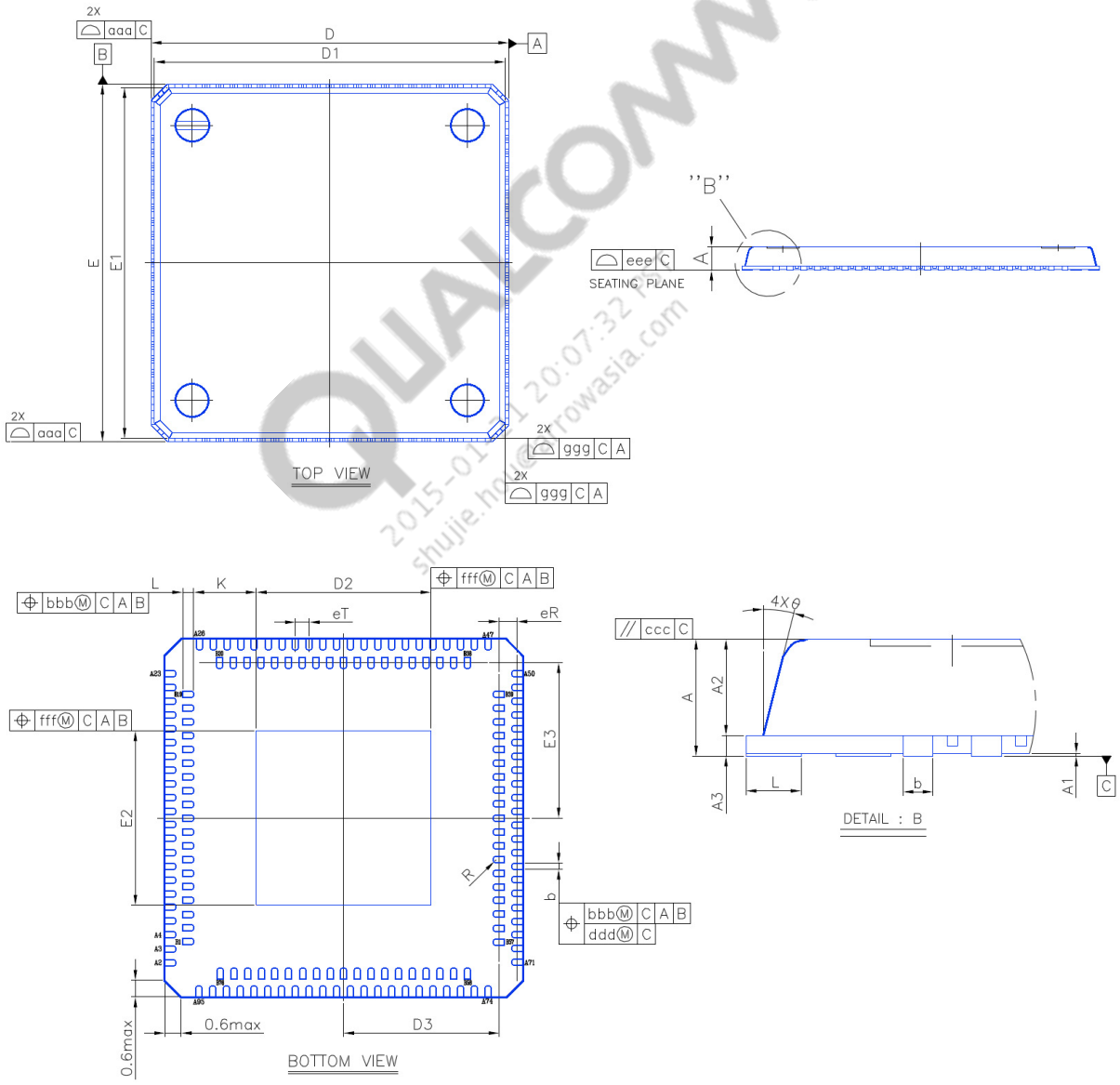


Figure 12-1 QCA9563 A-Type Package Drawing

Table 12-1 A-Type Package Dimensions

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm	0.031	0.033	0.035	inches
A1	0.00	0.02	0.05	mm	0.00	0.0008	0.002	inches
A2	0.65	0.70	0.75	mm	0.026	0.028	0.030	inches
A3		0.15 REF		mm		0.006 REF		inches
b	0.18	0.22	0.30	mm	0.007	0.009	0.012	inches
D/E	12.90	13.00	13.10	mm	0.508	0.512	0.516	inches
D1/E1		12.75 BSC		mm		0.502 BSC		inches
D2/E2	6.25	6.35	6.45	mm	0.246	0.250	0.254	inches
D3/E3		5.65 BSC		mm		0.222 BSC		inches
eR		0.65 BSC		mm		0.020 BSC		inches
eT		0.50 BSC		mm		0.026 BSC		inches
L	0.30	0.40	0.50	mm	0.012	0.016	0.020	inches
θ		5-15		°		5-15		°
K	0.20	—	—	mm	0.008	—	—	inches
R	0.09	—	0.14	mm	0.004	—	0.006	inches
aaa		0.10		mm		0.004		inches
bbb		0.10		mm		0.004		inches
ccc		0.10		mm		0.004		inches
ddd		0.05		mm		0.002		inches
eee		0.08		mm		0.003		inches
fff		0.10		mm		0.004		inches
ggg		0.20		mm		0.008		inches

Notes:

1. Controlling dimension: millimeter
2. Reference Document: NT90-Y7488-D2_A

12.1 Part Marking

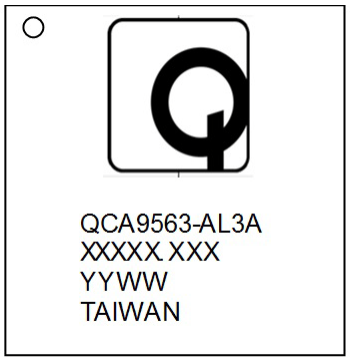


Figure 12-2 QCA9563 marking (top view, not to scale)

Table 12-2 QCA9563 marking line definitions

Line	Marking	Description
1	Qualcomm Atheros logo	Logo
2	QCA9563-AL3A	Part number
3	*XXXX.XXXX*	Assembly lot ID
4	*YYWW*	Year and week of production
5	*TAIWAN*	Manufacturing country
Additional lines may appear on the part marking for some samples; this is manufacturing information that is only relevant to Qualcomm and Qualcomm suppliers.		

12.2 Tape and Reel Information

Carrier tape system conforms to EIA-481 standards.

A simplified sketch of the QCA9563 tape carrier is shown in Figure 12-3, including the part orientation. Tape and reel details for the QCA9563 are as follows:

- Reel diameter: 330 mm
- Hub size: 178 mm
- Tape width: 24 mm
- Tape pocket pitch: 16 mm
- Feed: Single
- Orientation: Left (Q1)
- Units per reel: 2000

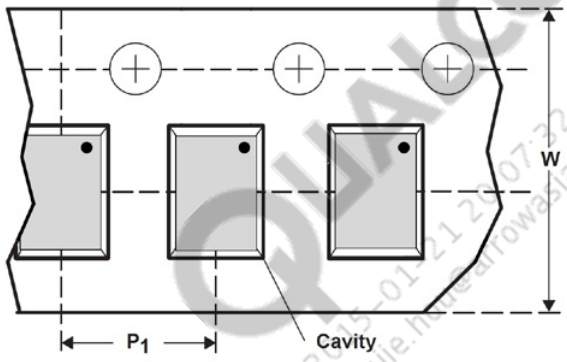


Figure 12-3 Carrier tape drawing with part orientation

13 Ordering Information

The order number QCA9563-AL3A specifies a lead-free standard-temperature version of the QCA9563.

The order number QCA9563-AL3A-R specifies a lead-free standard-temperature tape-and-reel version of the QCA9563.