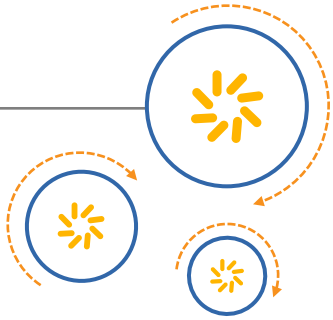
Qualcomm Technologies, Inc.



IPQ4018/IPQ4028/IPQ4019/IPQ4029 RF Test

User Guide

80-Y9700-3 Rev. L

March 7, 2017

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Revision history

Revision	Date	Description
A	July 2015	Initial release
B	September 2015	Chapter 1: Updated DK01 design kit and design packages
C	September 2015	Appendix A: Updated EEPROM structures.
D	October 2015	Revised EEPROM layout in Table A-1; added clpcFlag in Table A-2; added pre-calibration data in section 2A.7.
E	November 2015	Revised EEPROM layout ▪ Table A-2 Base header: clpc_error, paBiasSetting, refDesignIdForFilename and paprdShortCal ▪ Table A-3 EEP_FLAGS: flag3 ▪ Table A-4 Bimodal EEPROM header: minPwr4TPCErrCorr Table A-11 Thermal fields: configFlag
F	April 2016	Updated EEPROM layout ▪ Table A-3 EEP_FLAGS: updated flag3 Section A.8: added Misc section
G	June 2016	Updated flag1 definition in Table A-3 EEP_FLAGS. Updated reference board BDF in Table 1-3.
H	July 2016	Updated steps in 1.7 Setting up QSPR automation test Updated steps in 1.8 Setting up QCARCT manual test Added 1.9 AP.DK07 RF calibration setup Added new fields in Table A-2 Base header Added new fields in Table A-4 Bimodal EEPROM header
J	July 2016	Updated reference board BDF in Table 1-3.
K	September 2016	Updated reference board BDF in Table 1-3.
L	March 2017	Updated Table A-4 Bimodal EEPROM header.

NOTE: The following letters are not used to designate revisions: I, O, Q, S, X, and Z.

Contents

Figures

Tables

1 QDART-Connectivity Test Setup

QDART-Connectivity is a collection of software tools and resources designed to aid original equipment manufacturers with hardware development and production issues. The QDART-Connectivity collection includes several tools:

- Qualcomm Atheros Manufacturing Support Library (QCAMSL)
- Qualcomm Atheros Radio Control Tool (QCARCT)
- Qualcomm Sequence Profiling Resource (QSPR)
- QSPR subsystem test libraries and extensible test tree files (XTTs).

User credential is required to access CreatePoint site https://createpoint.qti.qualcomm.com/. Contact Qualcomm Technologies at support.cdmatech@qti.qualcomm.com if any questions or issues with the access.

1.1 Installing QDART-Connectivity

Before start, make sure older version has been uninstalled completely from the workstation.

1. Download QDART-Connectivity from CreatePoint.

   QDART-Connectivity release package can be downloaded at **CreatePoint** > **Tools** > **Qualcomm Development Acceleration Resource Toolkit – Connectivity**. Make sure the latest version is used for testing and calibration.

2. Make sure Microsoft .NET Framework 4 is installed on the Windows-based workstation.
3. Install QDART-Connectivity.
   a. Unzip the QDART-Connectivity package.
   b. Right click QDART-Connectivity<version>.exe and select Run as administrator.
   c. Click through to accept license agreement.
   d. Select **Complete** mode to install.

When the installation is complete, QDART-Connectivity utilities such as QCARCT, QMine, and QSPR are installed at `C:\Program Files (x86)\Qualcomm`. DLL files are located at `C:\Program Files (x86)\Qualcomm\bin`.

A folder structure is created at `C:\Qualcomm` containing the testing files, tester configurations, and reports/logs. Table 1-1 lists some of the folders and files that are configured or used during setup, testing, and calibration.

Table 1-1 QDART-Connectivity folders and files (C:\Qualcomm)

QMINE\Temp	Excel files generated when QMine creates plots from test logs
QSPR\Testlog	Log files of QSPR
WCN\ProdTests\BIN	DLL files
WCN\ProdTests\CLPC	External coupler testing files
WCN\ProdTests\QMineFormatDescriptors	QMine files
WCN\ProdTests\refDesigns\	Board data files referenced by the WlanLoadDut properties within each TestTree.xml file for loading DUT.
WCN\ProdTests\StationCal	Pathloss for specific test instrument referenced by InitializeWlanTester in TestTree.xml.
WCN\ProdTests\TesterConfig	QSPR tester configuration (including tester type and IP address) referenced by InitializeWlanTester in TestTree.xml.
WCN\ProdTests\Test Trees	The test trees (.xtt) files reference many of the above directories for information/files/data.

1.2 Installing tester software

Contact tester vendor for installation documents and support.

1.3 Setting up test environment

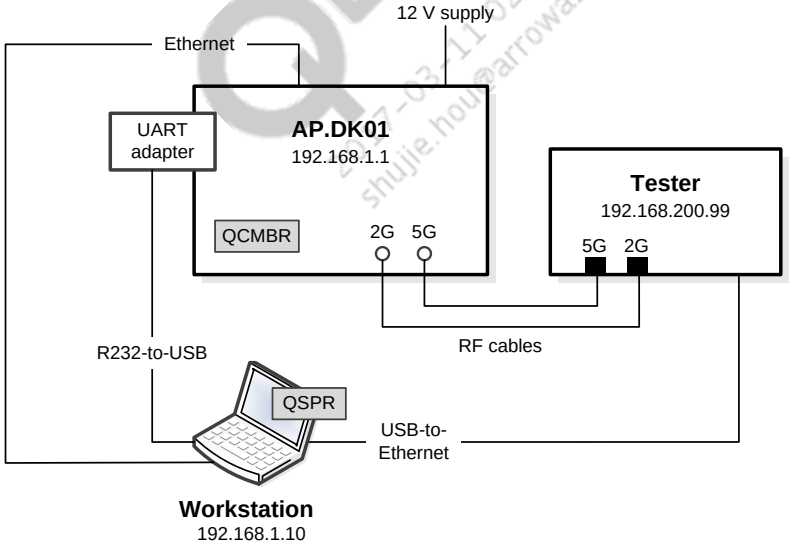


Figure 1-1 DK01 test setup example

Required hardware and equipment

- Hardware design kit that include DUT board, UART adapter, and power supply
- Workstation: Laptop with Intel i7 processor and 64-bit Windows 7 OS
- Tester: LitePoint IQxel

IP addresses

- Workstation QSPR Ethernet port IP: 192.168.1.10
- Workstation USB2Ethernet port IP: 192.168.200.100
- LitePoint IP: 192.168.200.99
- DK01 Ethernet IP: 192.168.1.1

DUT console ports

- Instance 0 (or device 0): 2390
- Instance 1 (or device 1): 2391

1.4 Setting up DUT

Following is an example to set up AP.DK01 with IPQ4019.

1. Boot the DUT to get QSDK up and running.
2. Show wireless status.
   ```
   uci show wireless
   ```
   If **wireless.wifi0.disabled** or **wireless.wifi1.disabled** is 1, set it to 0.
   ```
   uci set wireless.wifi0.disabled=0
   uci set wireless.wifi1.disabled=0
   ```
3. Set DUT IP address and commit the address. Make sure the DUT and the workstation are under the same subnet.
   ```
   uci set network.lan.ipaddr=192.168.1.1
   uci commit network
   ```
4. Turn off Wi-Fi.
   ```
   wifi down
   ```
5. Start QCMBR.
   ```
   /etc/init.d/qcmbr start
   ```
   This command run Dual Band Dual Concurrent (DBDC) on the DUT using the command:
   - 2 GHz only:
     ```
     /usr/sbin/Qcmbr -instance 0 -pcie 0
     ```
   - 2 GHz and 5 GHz:
     ```
     /usr/sbin/Qcmbr -instance 0, 1 -pcie 0, 1
     ```

Other useful commands

- Restart QCMBR
  ```
  /etc/init.d/qcmbr restart
  ```
- Run QCMBR with console prints:
  ```
  /lib/firmware/IPQ4019/hw.1# kill <pcie0 process ID>
  /lib/firmware/IPQ4019/hw.1# kill <pcie1 process ID>
  ps
  ```

```
/usr/sbin/Qcmbr -instance 0 –pcie 0 &
/usr/sbin/Qcmbr –instance 1 –pcie 1 &
```

1.5 Configuring test tree

Sample test tree is provided in the DP25 package. It is recommended to use QSPR GUI to edit test tree (*.xtt) and use Notepad++ to modify configuration files (*.xml). During the configuration, make sure correct file names and paths are provided in the test tree.

1. Download DP25 package from CreatePoint > Hardware Document > IPQ4018/IPQ4028/IPQ4019/IPQ4029.
2. Copy the sample test tree (*.xtt) to `WCN\ProdTests\Test Trees`.
3. Configure the test tree parameters in Table 1-2 accordingly.

Table 1-2 Test tree configurations

InitializeWlanTester Parameters	
testerConfigFileName	Reference to TesterConfigFile which contains the tester name.
stationCalFileName	Reference to StationCalFile which contains the pathloss information listed in TxStationCalPath.
TxStationCalPath	Names of the chains defined in the StationCalFile. Following is a naming example: BHx_device, where x = chain number, device = LP (LitePoint) or GLDN (Golden). For example: BH0_LP and BH1_LP
RxStationCalPath	
ConnectDutUsingUserTranspportDLL	
Type	1 QLIB_TARGET_TYPE_APQ
wlanID	4019
comport	192.168.1.1 (for Remote or Network port)
userTransPortDll	QMSL_WLAN_Transport.dll (Qmissle)
WlanLoadDut	
DevDLLName	ipq4019
refDesign	ipq4019
eepFname	C:\<configdir>\boardData\fakeBoardData_ipq4019.bin
iNVMemOption	5 DataFile
ssid	0x40

1.6 Reference board and BDF mapping

Before running the IPQ40xx reference boards in Mission mode, perform calibration for the boards first. If reference board is not calibrated, the Host driver in Mission mode cannot select the correct BDF automatically and always uses boarddata_0/1.bin. In this case, user must copy the correct BDF to boarddata_0/1.bin according to Table 1-3.

Table 1-3 Reference board and BDF mapping

MCN Number	Reference Board ID	Board Data File
AP.DK01		
Y9658 (DK01 ES)	0x10	boardData_1_0_IPQ4019_DK01_2G.bin
	0x11	boardData_1_0_IPQ4019_DK01_5G.bin
Y9803 (DK01 FC) YB021 (DK01 CS)	0x10	boardData_1_0_IPQ4019_Y9803_wifi0.bin
	0x11	boardData_1_0_IPQ4019_Y9803_wifi1.bin
AP.DK03		
Y9988 (DK03 ES/FC)	0x12	boardData_1_0_IPQ4019_DK03_wifi0.bin
	0x13	boardData_1_0_IPQ4019_DK03_wifi1.bin
YA131 (DK03 CS) YA541 (DK03 post-CS)	0x18	boardData_1_0_IPQ4019_YA131_wifi0.bin
	0x19	boardData_1_0_IPQ4019_YA131_wifi1.bin
AP.DK04		
Y9761 (DK04 CS)	0x14	boardData_1_0_IPQ4019_DK04_2G.bin
	0x15	boardData_1_0_IPQ4019_DK04_5G.bin
Y9761 (DK04 CS for Negative Power)	0x16	boardData_1_0_IPQ4019_DK04_2G_neg_pwr.bin
	0x17	boardData_1_0_IPQ4019_DK04_5G_neg_pwr.bin
AP.DK05		
Y9857 (DK05 ES)	0x1a	boardData_1_0_IPQ4019_DK05_2G.bin
	0x1b	boardData_1_0_IPQ4019_DK05_5G.bin
AP.DK06		
Y9828 (DK06 ES/CS)	0x1f	boardData_1_0_IPQ4019_DK06_2G.bin
	0x20	boardData_1_0_IPQ4019_DK06_5G.bin
AP.DK07		
YA246 (DK07 ES/CS)	0x1c	boardData_1_0_IPQ4019_DK07_wifi0_2G.bin
	0x1d	boardData_1_0_IPQ4019_DK07_wifi0_5G_HB.bin
	0x1e	boardData_1_0_IPQ4019_DK07_wifi1_5G_LB.bin

1.7 Setting up QSPR automation test

QSPR is an automated test tool to characterize RF radio and calibrate the board. The calibration results can be written to flash memory. QSPR test tree are organized in several loops which presented in QSPR GUI as folders. Each folder represents a series of tests where loop can be set up on it. For example:

- First loop for 2.4 GHz channels: Loop through variable “channels”
- Second loop for 802.11b long rates: Loop through variable “rate”

- Third loop for power: Loop through variable “powerLevel” where EVM, spectrum mask, and power are measured.

QSPR calibration requires the following bin files:

- **boarddata.bin**: Default board data information to be populated to the RAM data structure in the Tensilica processor. This file is loaded during bootup process.
- **otp.bin**: Downloaded from host driver to target RAM and executed in Tensilica processor. During bootup, this program reads some board data fields from EEPROM and overwrite the relevant fields in the RAM structure.
- **utf.bin**: Firmware program for universal firmware testing. After board data is loaded to Tensilica processor, this file is loaded from host driver to target, and remains in Tensilica processor until the board is power cycled or the driver is disabled.

  Communication between host and target are implemented using a set of commands for transmit, receive, calibrate, save calibration data, and so on. These commands are executed by the target firmware (UTF).

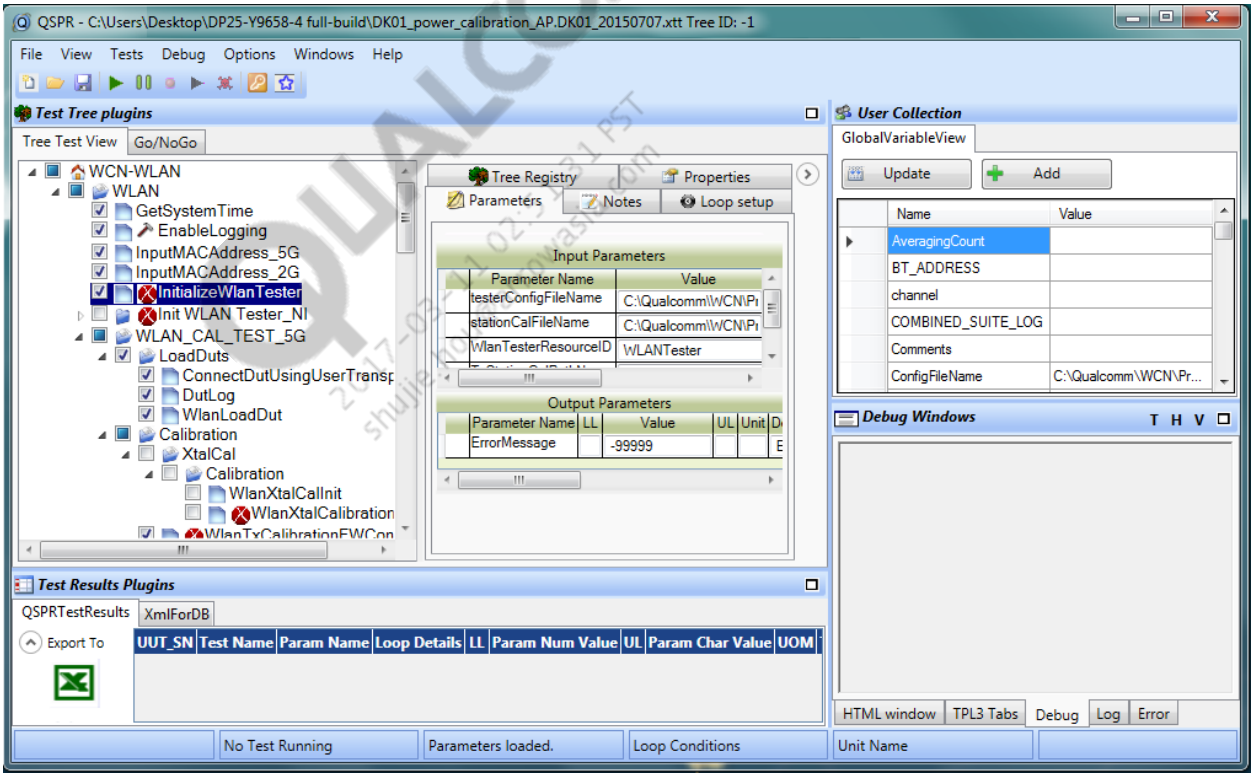


Figure 1-2 QSPR GUI

1. Start QSPR in administrator mode and open the test tree.
2. Set up the tester configuration file.
   a. Sample tester configuration files can be found under C:\Qualcomm\WCN\ProdTests\ConfigFiles\SCPI_Config_Files\.
   b. You can modify your tester configuration file according to (80-Y0306-1) *Wireless Connectivity Non-Signaling Tests User Guide*.

c. In QSPR test tree, select **WLAN > InitializeWlanTester**. Set **testerConfigFileName** to your tester configuration file.

3. Set up the cable loss configuration file.

   a. Sample cable loss config files are located at `C:\Qualcomm\WCN\ProdTests\StationCal\`.

   b. Modify WLAN cable loss in section **<PathName>** to match the **'TxStationCalPathName/RxStationCalPathName'** in 'InitializeWlanTester' test node.

   c. In QSPR test tree, select **WLAN > InitializeWlanTester**. Set **stationCalFileName** to your cable loss configuration file.

4. Set up DUT transport.

   a. Select WLAN_CAL_TEST_5G > ConnectDutUsingUserTransportDLL, configure the transport parameters:

   - **wlanID**: 4019
   - **comPort**: 198.168.1.1: 2391
   - **userTransPortDll**: C:\Program Files (x86)\Qualcomm\QDART\bin\QMSL_WLAN_Transport.dll

   b. Select WLAN_CAL_TEST_2G > ConnectDutUsingUserTransportDLL, configure the transport parameters:

   - **wlanID**: 4019
   - **comPort**: 198.168.1.1: 2390
   - **userTransPortDll**: C:\Program Files (x86)\Qualcomm\QDART\bin\QMSL_WLAN_Transport.dll

5. Set up board data.

   a. Use TFTP to copy **boarddata_0.bin** from DUT directory `/lib/firmware/IPQ4019/hw.1` to workstation folder `C:\Qualcomm\WCN\Prodtests\refDesigns`.

   b. On the workstation, copy boarddata_0.bin to fakeBoradData_ipq4019.bin.

   c. In QSPR, select **WLAN_CAL_TEST_5G > WlanLoadDut**, set **eepFName** to fakeBoardData_ipq4019.bin path.

   d. In QSPR, select **WLAN_CAL_TEST_2G > WlanLoadDut**, set **eepFName** to fakeBoardData_ipq4019.bin path.

6. Set up test result write option.

   Select **SaveCalMacData > Write MAC > WlanMemCommit**, set **iWriteOption** to **5 DataFile**.

7. Run test tree.

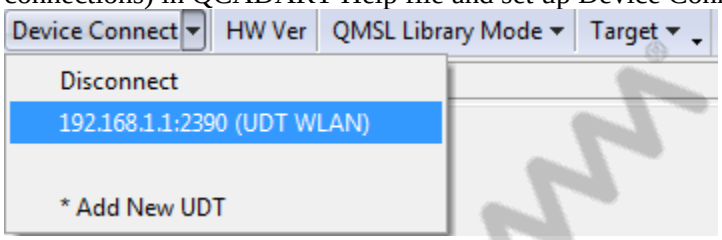
   a. Click the Play button  on the tool bar.

   b. In the pop-up window, enter test name or serial number in the **Unit ID** field. Click **OK**.

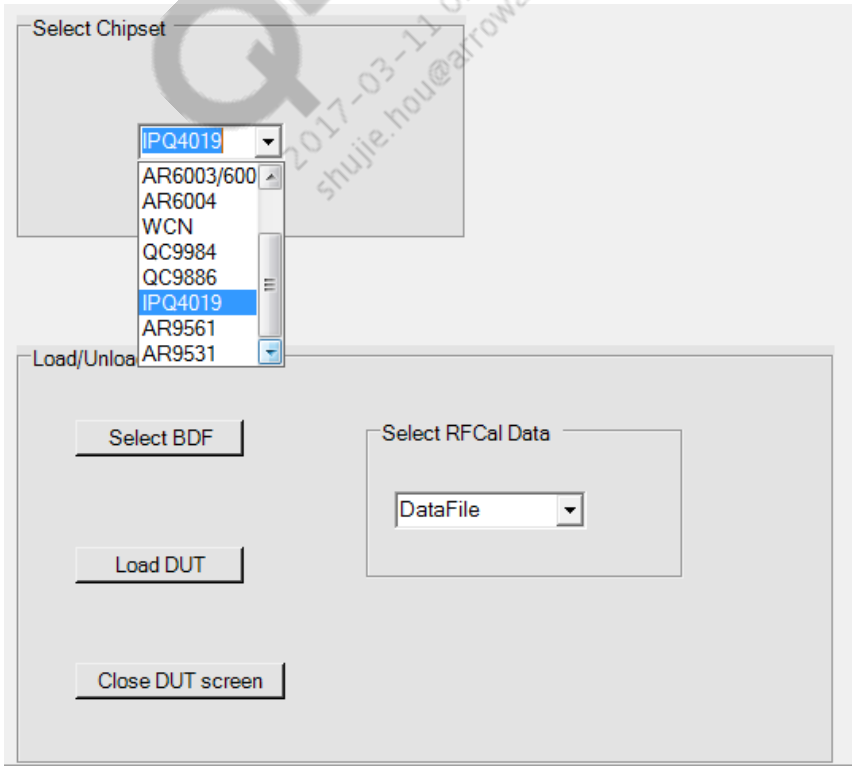
   c. Test results are printed to the **Test Result Plugin** window and saved to `C:\Qualcomm\QSPR\TestLog`.

1.8 Setting up QCARCT manual test

1. Set up transport.
   a. Start QCARCT in administrator mode.
   b. Select Tool > User Defined Transport.
   c. Refer to **QCARCT** > **Menu Structure** > **Device Connect** (User Defined Transport connections) in QCADART Help file and set up Device Connect.

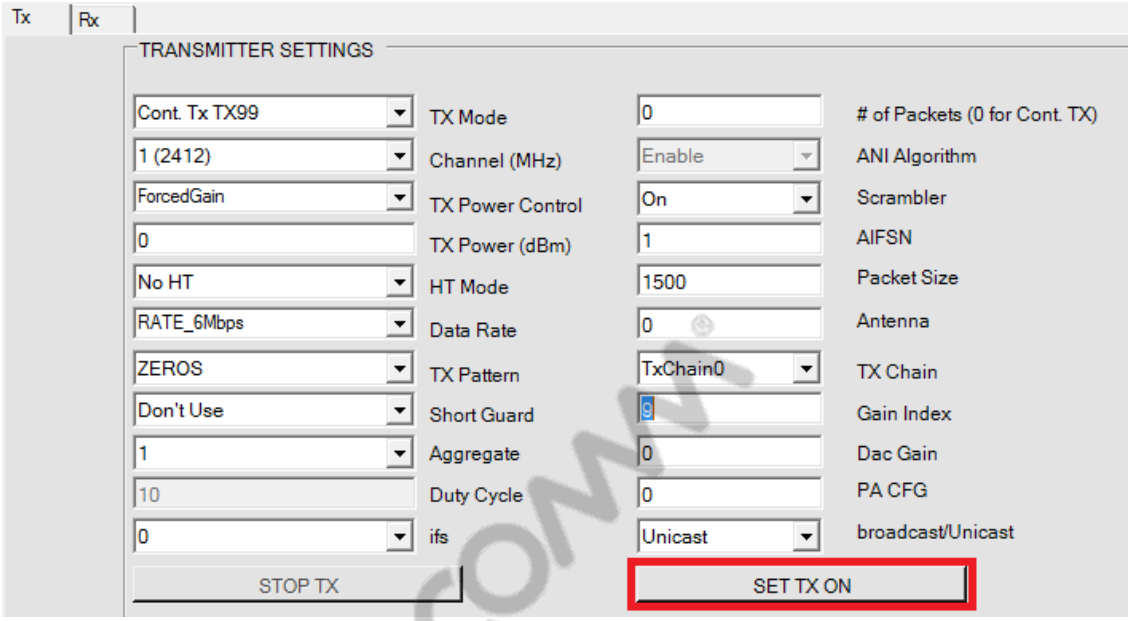


2. Initialize QCARCT.
   a. Select User Defined Transport > Connect.
   b. Select **FTM Command > WLAN**. In the **Select Chipset** drop-down list, select **IPQ4019**.
   c. Click Select BDF and navigate to the fakeBoardData_IPQ4019.bin file.
   d. Click **Load DUT**. The DUT is now ready for RF testing.

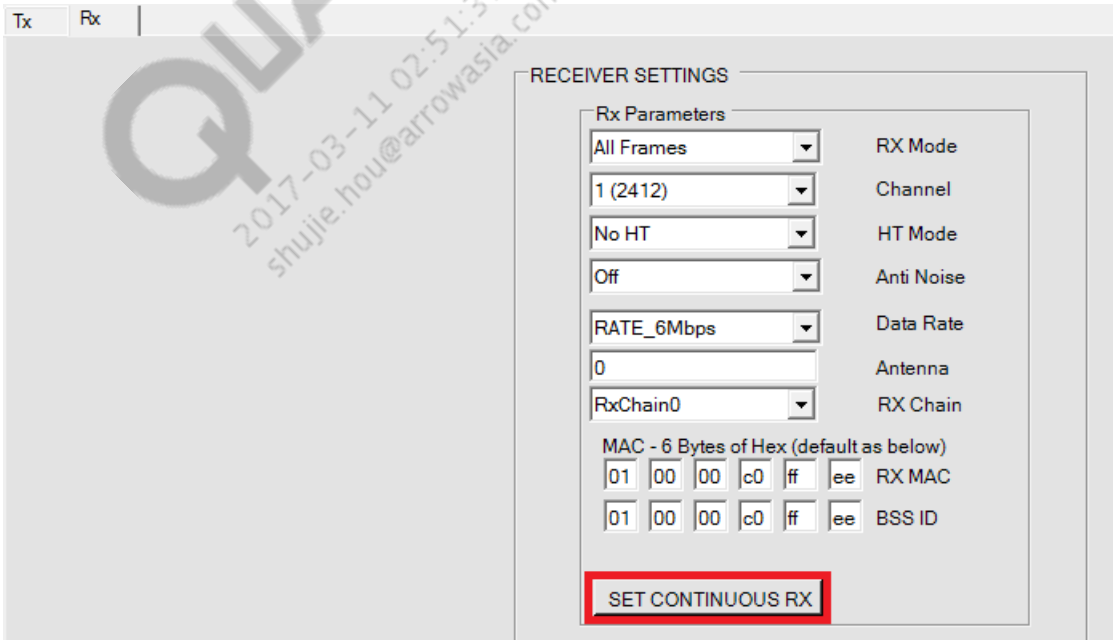


3. Start/Stop QCARCT WLAN Tx test.

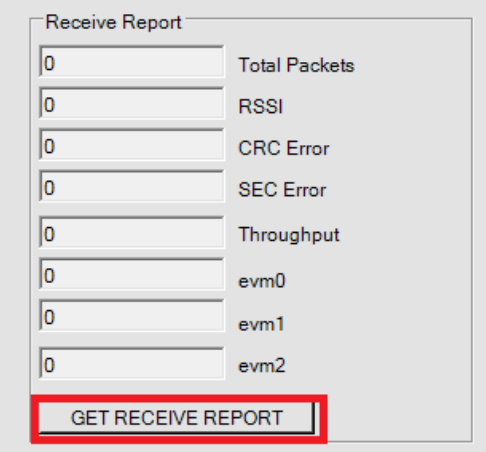
   Click **Tx > SET TX ON/STOP TX** to start/stop transmission. Use tester to analyze Tx signals.



4. Start/Stop QCARCT WLAN Rx test.
   a. Click **Rx > SET CONTINUOUS RX** to start receiving.



   b. Use tester to send packets.
   c. After the test is done, click **GET RECEIVE REPORT** to stop receiving and get the report.



1.9 AP.DK07 RF calibration setup

1.9.1 AP.DK07.1 + BSR02.1 (Three-radio SBS)

It's AP.DK07 (2.4 GHz wifi0 + 5G_LB wifi1) + QCA9886 (5G_HB wifi2).

1. Boot AP to kernel level and do following steps to modify the board data file corresponds to AP.DK07.
   a. cd /lib/firmware/IPQ4019/hw.1/
   b. rm boarddata_0.bin
   c. rm boarddata_1.bin
   d. cp boardData_1_0_IPQ4019_DK07_wifi0_2G.bin boarddata_0.bin
   e. cp boardData_1_0_IPQ4019_DK07_wifi1_5G_LB.bin boarddata_1.bin
   f. cd /lib/firmware/QCA9888/hw.2/
   g. cp boardData_2_0_QCA9888_5G_Y9690_SBS_HB.bin boarddata_2.bin
2. Start QCMBR
   a. /etc/init.d/qcmbr restart

NOTE: After UTF firmware is downloaded, the QCMBR application should be running for all the three devices. If it is not running, it is possible that the Wi-Fi profile was not created properly.

3. Launch QSPR tree to do calibration and WLAN Tx/Rx verification.
   a. A sample QCA9886 test tree of 'Besra_Ver3_QC98xx-30_Y9690_1_QDP_IQxel.xtt' can be found in DP25-YA105-100.
   b. Need to change the input parameter of 'comPort' to '192.168.1.1:**2392**' in 'ConnectDutUsingUserTransportDLL' test node of above QCA9886 test tree.
   c. A sample AP.DK07 test tree of 'AP.DK07_2G_5G_LB.xtt' can be found in DP25-YA246-100.

d. You can create a new test tree by combining above AP.DK07 test tree with QCA9886 test tree.

1.9.2 AP.DK07.1 + CUS240.5 (Three-radio SBS)

It's AP.DK07 (5G_HB wifi0 + 5G_LB wifi1) + QCA9884 (2.4 GHz wifi2).

1. Boot AP to kernel level and do following steps to modify the board data file corresponds to AP.DK07.
   a. cd /lib/firmware/IPQ4019/hw.1/
   b. rm boarddata_0.bin
   c. rm boarddata_1.bin
   d. cp boardData_1_0_IPQ4019_DK07_wifi0_5G_HB.bin boarddata_0.bin
   e. cp boardData_1_0_IPQ4019_DK07_wifi1_5G_LB.bin boarddata_1.bin
   f. cd /lib/firmware/QCA9984/hw.1/
   g. cp boardData_QCA9984_CUS240_2G_v1_004.bin boarddata_2.bin
2. Start QCMBR
   a. /etc/init.d/qcmbr restart

NOTE: After UTF firmware is downloaded, the QCMBR application should be running for all the three devices. If it is not running, it is possible that the Wi-Fi profile was not created properly.

3. Launch QSPR tree to do calibration and WLAN Tx/Rx verification.
   a. A sample QCA9984 2.4 GHz test tree of '23305_cs1_ver4_qc99xx-30_y8667_333_qdpcs1_150521.4_iqxel (cus240).xtt' can be found in DP25-Y8667-2.
   b. Need to change the input parameter of 'comPort' to '192.168.1.1:2392' in 'ConnectDutUsingUserTransportDLL' test node of above QCA9984 test tree.
   c. A sample AP.DK07 test tree of 'AP.DK07_5G0_5G1.xtt' can be found in DP25-YA246-100.
   d. You can create a new test tree by combining above AP.DK07 test tree with QCA9984 test tree.

1.9.3 AP.DK07.1 + CS.CAS01.3 (Three-radio SBS)

It's AP.DK07 (2.4 GHz wifi0 + 5G_LB wifi1) + QCA9984 (5G_HB wifi2).

1. Boot AP to kernel level and do following steps to modify the board data file corresponds to AP.DK07.
   a. cd /lib/firmware/IPQ4019/hw.1/
   b. rm boarddata_0.bin
   c. rm boarddata_1.bin
   d. cp boardData_1_0_IPQ4019_DK07_wifi0_2G.bin boarddata_0.bin
   e. cp boardData_1_0_IPQ4019_DK07_wifi1_5G_LB.bin boarddata_1.bin

f. cd /lib/firmware/QCA9984/hw.1/

g. cp boardData_QCA9984_CUS239_high_band_5G_v1_006.bin boarddata_2.bin

h. Start QCMBR

i. /etc/init.d/qcmbr restart

NOTE: After UTF firmware is downloaded, the QCMBR application should be running for all the three devices. If it is not running, it is possible that the Wi-Fi profile was not created properly.

2. Launch QSPR tree to do Calibration and WLAN Tx/Rx verification.

   a. A sample QCA9984 5 GHz test tree of 'ES_Cascade_Ver3_QC9984-30_YA026-232_IQxel (Cus239)_SBS_232.xtt' can be found in DP25-YA026-2320.

   b. Need to change the input parameter of 'comPort' to '192.168.1.1:2392' in 'ConnectDutUsingUserTransportDLL' test node of above QCA9984 test tree.

   c. A sample AP.DK07 test tree of 'AP.DK07_2G_5G_LB.xtt' can be found in DP25-YA246-100.

   d. You can create a new test tree by combining above AP.DK07 test tree with QCA9984 test tree.

2 References

- (80-Y9798-1) WLAN AP Test and Calibration User Guide
- (80-VB987-1) Qualcomm Sequence Profiling Resource (QSPR) User Guide

A EEPROM Structure

This chapter lists all the EEPROM fields and their values. Some fields cannot be changed or are reserved for future use.

A.1 EEPROM layout

Table A-1 EEPROM layout

Section	Size
Base EEPROM Header	220
BiModal Section(2G/5G)	240
Freq Modal	148
Spur Mit	136
heavyClip	104
Pre-calibration Data	320
Misc	958
2G power cal data and target power/CTL table	2658
5G power cal data and target power/CTL table	6400
Rx Gain Cal	192
Sticky Write table	508
chipCalData	36
ATE data	144
TOTAL SIZE	12064

A.2 Base header

Table A-2 Base header

Field Name	Bytes	Description	Bits	Bit Definition
length	2	Overall EEPROM file size Based on the selected .bin file.	[16:0]	Fixed value 12064.
checksum	2	EEPROM file checksum	[16:0]	Value
eeprom version	1	Version control	[7:0]	0x1 for IPQ40X8/40X9.
template version	1	Reserved. Template version control (some boards have special template defined fields)	[7:0]	Value
macAddr	6	WLAN MAC Address	[47:0]	WLAN MAC address
regDmn	4	Determines regulatory domain, country code.	[31:16]	Reserved
			[15]	COUNTRY_OR_DOMAIN_FLAG
			[14]	WORLD_WIDE_ROAMING_FLAG
			[11:0]	COUNTRY_OR_DOMAIN_CODE
opCapBrdFlags	16	Determines the operation mode of the device. (Detail in EEP_FLAGS page)	[95:0]	Refer to “EEP_FLAGS”
binBuildNumber	4	Includes 4 fields: ▪ RefDesignId ▪ customerId ▪ projectId ▪ boardDataRev	[31:24]	boardDataRev starting from 2 for IPQ40X8/40X9.
			[23:16]	Project ID
			[15:8]	Customer ID
			[7:0]	Reference design ID
txrxMask	1	Tx and Rx Mask bit to identify MIMO configuration	[7:4]	Rx Mask ▪ 0x1: RF Chain 0 ▪ 0x2: RF Chain 1 ▪ 0x3: RF Chain 0 & 1
			[3:0]	Tx Mask ▪ 0x1: RF Chain 0 ▪ 0x2: RF Chain 1 ▪ 0x3: RF Chain 0 & 1
rfSilent	1	Reserved for RF slient pin configuration	[7:0]	Reserved

Field Name	Bytes	Description	Bits	Bit Definition
wlanLedGpio	1	Reserved for LED pin configuration	[7:0]	Reserved
swreg	1	Reserved for control internal switching regulator register.	[7:0]	Reserved
deltaCck	1	Bandwidth Compensation value for CCK modulation. For example, setting to 4 increases Tx power by 0.5 dB, while setting to 0xFC decreases the power by 0.5 dB	[7:0]	Signed value in 1/8 dB resolution.
delta20	1	Bandwidth Compensation value for 20 MHz OFDM modulation.	[7:0]	Signed value in 1/8 dB resolution.
delta40	1	Bandwidth Compensation value for 40 MHz OFDM modulation.	[7:0]	Signed value in 1/8 dB resolution.
delta80	1	Bandwidth Compensation value for 80 MHz OFDM modulation.	[7:0]	Signed value in 1/8 dB resolution.
custData	20	Space for customer writing some information	[159:0]	–
param_for_tuning_caps	1	Value of XTAL_CAPOUTDAC	[7:0]	Value of XTAL_CAPOUTDAC. This field is valid when featureEnable[6]=1.
param_for_tuning_caps_1	1	Value of XTAL_CAPINDAC	[7:0]	Value of XTAL_CAPINDAC. This field is valid when featureEnable[6]=1.
tpc_flag	1	TPC flag for CLPC/OPLC	[3:0]	2G ▪ 0x3: CLPC_xPet (also for DC based CLPC) ▪ other values: CLPC (RF based CLPC)
			[7:4]	5G ▪ 0x3: CLPC_xPet (also for DC based CLPC) ▪ other values: CLPC (RF based CLPC)
dpdRfbMode	1	DPD configuration	[7:0]	Value
dpdTrainingSample	2	Reserved	[15:0]	Reserved
dpdHeavyClipEnable	2	Reserved	[15:0]	Reserved
dpdQuickDrop	1	Reserved	[7:0]	Reserved
dpdTargetLvlHi	1	DPD configuration	[7:0]	Value
dpdTargetLvlLow	1	DPD configuration	[7:0]	Value
dpdTargetLvlWeak	1	DPD configuration	[7:0]	Value
dpdPwrHi	1	DPD configuration	[7:0]	Value

Field Name	Bytes	Description	Bits	Bit Definition
dpdPwrLow	1	DPD configuration	[7:0]	Value
dpdPwrWeak	1	DPD configuration	[7:0]	Value
dpdEnable	1	1: Enable DPD 0: Disable DPD	[7:0]	Value
dpdSqLimit	1	DPD configuration Code logic. Distinguish if DPD training result is good or not. Compare this parameter with bestSQ.	[7:0]	Value
dpdSqBestLimit	1	DPD configuration Code logic. Distinguish if DPD training result is good or not. (SQ: Signal Quality) *if(bestSQ <= sqBestLimit) {* *timing_training_done = 1;* *}*	[7:0]	Value
dpdCorexRange	1	DPD configuration Code logic. It means MAX_COARSE_IDX. If this value is “0”, it will be set to “12”.	[7:0]	Value
dpdForceClock_TxRadioBW	1	Reserved	[7:0]	Reserved
dpdAm2AmMask	4	DPD configuration	[31:0]	Value
dpdAm2PmMask	4	DPD configuration	[31:0]	Value
dpdHt40Mask	4	DPD configuration	[31:0]	Value
dpdTrainingBW	1	DPD configuration	[7:0]	Value
dpdAgc2Settling	1	DPD configuration	[7:0]	Value
dpdDebugMode	1	Print DPD debug message	[7:0]	1: Enable; 0: Disable (default)
dpdXpaOn	1	DPD configuration	[7:0]	Value
baseFuture1	52	Reserved	[289:0]	Reserved
clpc_error	2	Change intial CLPC error value. This is valid if flag3[bit 4]=1 (0x10)	[15:0]	Value
clpcFlag	1	0x1 : disable 10*log10 (pdadc) while doing PLUT generation	[7:0]	value

Field Name	Bytes	Description	Bits	Bit Definition
tempSlopeCharacterized	1	Temp slope Valid only when chipCalData.configFlag[0]=1	[7:0]	0: Use default value (default value is 216)
xtal_cap_interval	4	Reserved	[31:0]	Reserved
xtal_cap_offset	4	Reserved	[31:0]	Reserved
pefFlag	1	Eanble / disable PEF	[7:0]	0 : Disable PEF 1 : Enable PEF
pefCalMax	1	Reserved	[7:0]	Reserved
pefCalMin	1	Reserved	[7:0]	Reserved
pefCalStep	1	Reserved	[7:0]	Reserved
pefMaxCalAtt	1	Reserved	[7:0]	Reserved
pefMaxCalBw	1	Reserved	[7:0]	Reserved
pefMagSel	1	Reserved	[7:0]	Reserved
pefLbSel	1	Reserved	[7:0]	Reserved
checkTrainingStatusDelay	2	DPD CAL settling time (in microseconds) to get training sequence status. If checkTrainingStatusDelay is “0”, it will be set to 400. This is a waiting delay to wait register BB_PAPRD_TRAINER_STAT1.PAPRD_TRAIN_DONE.	[15:0]	Value
dpdLNASETTING	4	Reserved	[31:0]	Reserved
nvMacFlag	1	NV MAC flag. otp.bin sets this field if OTP has MAC address. 0: Generate random MAC address 1: Use BDF or OTP MAC address	[7:0]	Value
mipiPowerMode	1	MIPI interface PW mode	[7:0]	Value
pefMask	4	DPD configuration	[31]	Reserved
			[30:0]	Value
sensitivityAdjustment	1	Adjust ANI function	[7:0]	Value
smartAntennaEnable	1	Enable smart Antenna	[7:0]	0: Disable 1: Enable
ccaThresh	1	Set CCA threshold	[7:0]	Value

Field Name	Bytes	Description	Bits	Bit Definition
packageType	1	Chip package type 0 = QFN, 1 = BGA	[7:0]	Value
paBiasSetting	4	PA Bias Setting for Edison	[31:0]	Value
refDesignIdForFilename	1	Reserved	[7:0]	Reserved
paprdShortCal	1	Enable DPD short calibration	[7:0]	Value
nonLinearTxFir	1	Reserved	[7:0]	Reserved
thermOffset	1	Reserved	[7:0]	Reserved
droopingFlag	1	Reserved	[7:0]	Reserved
droopingEnableTempThresh	1	Reserved	[7:0]	Reserved
droopingDisableTempThresh	1	Reserved	[7:0]	Reserved
hal_cal_version_major	1	Board calibration version. This value will be stored into FLASH while doing power calibration. Do not change this value.	[7:0]	Value
hal_cal_version_minor	1	Board calibration version. This value will be stored into FLASH while doing power calibration. Do not change this value.	[7:0]	value
baseFuture	34	Reserved	[271:0]	Reserved

A.3 EEPROM flags

Table A-3 EEP_FLAGS

Field Name	Bytes	Description	Bits	Bit Definition
opFlags	1	Determines the operation mode of the device.	[7:0]	WHAL_OPFLAGS_11A = 0x01 WHAL_OPFLAGS_11G = 0x02 WHAL_OPFLAGS_5G_HT40 = 0x04 WHAL_OPFLAGS_2G_HT40 = 0x08 WHAL_OPFLAGS_5G_HT20 = 0x10 WHAL_OPFLAGS_2G_HT20 = 0x20
featureEnable	1	Enable/disable some features	[7:0]	0x20 = Override heavy clip. Refer to HeavyClip table. 0x40 = tuning_caps. Use longshift to update CAPINDAC/CAPOUTDAC. 0x80 = Override heavy clip PERBW for BW40/80
miscConfiguration	1	Reserved	[7:0]	Reserved
flag1	1	Enable/disable some features	[0:0]	WHAL_FLAG1_RXDCCAL_SWITCH_TABLE_FROM_BDF = 0x1 Control xLAN on/off by BDF's antCtrlChain setting while doing RxDcoCal.
			[7:1]	Reserved

Field Name	Bytes	Description	Bits	Bit Definition
boardFlags	4	Boards flags to enable/disable features	[31:0]	WHAL_BOARD_SELLNA = 0x001 (not used) WHAL_BOARD_ZERO_DBM = 0x002 (work with negative power) WHAL_BOARD_TXGAIN_TBL = 0x008 (not used) WHAL_BOARD_ANTDIVERSITY = 0x010 (not used) WHAL_BOARD_TEMP_SENSOR = 0x020 (not used) WHAL_BOARD_USE_OTP_XTALCAPS = 0x040 (not used) WHAL_BOARD_SHARED_RX = 0x080 (not ready) WHAL_BOARD_BT_SIGNAL_PRESENT = 0x100 (not used) WHAL_BOARD_USE_XPA = 0x200 (not used) WHAL_BOARD_PMU_BYPASS_SW = 0x400 (not used) WHAL_BOARD_PMU_BYPASS_PA = 0x800 (not used) WHAL_BOARD_PAPRD_2G_DISABLE = 0x2000 (not used) WHAL_BOARD_PAPRD_5G_DISABLE = 0x4000 (not used) WHAL_BOARD_0CAL_ENABLED = 0x8000 (not used) WHAL_BOARD_TXGAINTBL_EEP_ENA = 0x10000 (not used) WHAL_BOARD_TXGAINTBL_SCHEME = 0x20000 (not used) WHAL_BOARD_ENABLE_XPA_BIAS_2G = 0x40000 (not used) WHAL_BOARD_ENABLE_XPA_BIAS_5G = 0x80000 (not used) WHAL_BOARD_ENABLE_FEM_VMODE_5G = 0x100000
opFlags2	1	Extend part of opFlags	[7:0]	WHAL_OPFLAGS2_5G_VHT20 = 0x01 WHAL_OPFLAGS2_2G_VHT20 = 0x02 WHAL_OPFLAGS2_5G_VHT40 = 0x04 WHAL_OPFLAGS2_2G_VHT40 = 0x08 WHAL_OPFLAGS2_5G_VHT80 = 0x10

Field Name	Bytes	Description	Bits	Bit Definition
flag2	1	Extend part of flag1 (No detail define in SW now)	[7:0]	WHAL_FLAG2_CTLS_VALID = 0x01 ▫ Only support new CTL format. Set if properly populated. WHAL_FLAG2_ALT_TGT_PWR_LAYOUT = 0x02 ▫ Set when using new stream based target power storage WHAL_FLAG2_MINCCA_THR_FROM_MODAL = 0x04 ▫ Set to apply minCCA from the fields in the modal structure WHAL_FLAG2_MINCCA_THR_FROM_RXGAIN = 0x08 ▫ Set to apply minCCA from rxGain Cal WHAL_FLAG2_IBF_CAL = 0x10 ▫ Set to IBF Cal WHAL_FLAG2_TPC_CAL_TGT_PWR_GUIDE = 0x20 ▫ Set to TPC target power array for 2G and 5G WHAL_FLAG2_OVERRIDE_PAPRD_BW = 0x40 WHAL_FLAG2_XTAL_TEMP_COMP_ENABLE = 0x80 ▫ Set Xtal temperature compensation table in boarddata file
flag3	1	feature enable	[7:0]	WHAL_FLAG3_PA_BIAS_OVERRIDE = 0x1 Set Edison PA Bias current via BDF (only for Beeliner) WHAL_FLAG3_ENABLE_160_TARGET_PWR = 0x2 Set when 160MHz target powers are properly populated in bdf WHAL_FLAG3_ENABLE_DPD_MASK_BANDEDGE = 0x4 Enable DPD mask in CTL band edge channels WHAL_FLAG3_OVERRIDE_CLPC_ERROR = 0x8 Set to override intial CLPC error value from BDF WHAL_FLAG3_DYNAMIC_CLPC_ERROR = 0x10 Set to change CLPC error value based on different temperature WHAL_FLAG3_TX_IQ_3GROUP = 0x80 Set to enable TxIQ Cal with 3 group (default is 2 group)
eep_flags_resvd	2	16 Bytes alignment	[15:0]	–
boardFlagsExt	4	Reserved for coex and future flags	[31:0]	–

A.4 Bimodal EEPROM header

Table A-4 Bimodal EEPROM header

Field Name	Bytes	Description	Bits	Bit Definition
voltSlope	4	Reserved	[31:0]	Reserved
biModal_resv1	2	Add for byte alignment	[15:0]	Reserved
xpaBiasLvl	1	Reserved for external PA bias level voltage level.	[7:0]	Reserved
antennaGainCh	1	Reserved for antenna gain calculation.	[7:0]	Reserved
antCtrlCommon	4	Sets switch_table during Tx states. Details in BB_SWITCH_TABLE_COM1. Antenna control settings common across chains. A low 2-bit setting controlling the output of PINs (SWCOM0 and SWCOM1) on IPQ40x8/IPQ40x9 is specified for six possible transmission states. Bits[5:2] are un-used on IPQ40x8/IPQ40x9. Pin name of antenna control on IPQ40x8/IPQ40x9: ▪ Radio0: ▫ FEM_0_R0: Bit 0 ▫ FEM_1_R0: Bit 1 ▪ Radio1: ▫ FEM_0_R1: Bit 0 ▫ FEM_1_R1: Bit 1	[31:0]	[31:28: WLAN Tx on 1 un-shared chain. [27:22]: Idle and OTP_SWCOM_IDLE_MODE is 1'b1 [21:16]: Bluetooth [15:12]: Tx ant2 [11:6]: Tx ant1 [5:0]: Idle and OTP_SWCOM_IDLE_MODE is 1'b0

Field Name	Bytes	Description	Bits	Bit Definition
antCtrlCommon2	4	Sets Ant switch_table during Rx states. Details in BB_SWITCH_TABLE_COM2. Antenna control settings common across chains. A low 2-bit setting controlling the output of PINs (SWCOM0 and SWCOM1) on IPQ40x8/IPQ40x9 is specified for five possible reception states. Bits[5:2] are un-used on IPQ40x8/IPQ40x9. Pin name of Antenna control on IPQ40x8/IPQ40x9: ▪ Radio0: ▫ FEM_0_R0: Bit 0 ▫ FEM_1_R0: Bit 1 ▪ Radio1: ▫ FEM_0_R1: Bit 0 ▫ FEM_1_R1: Bit 1	[31:0]	[21:18]: Rx ant1&2 + lna1&2 [17:14]: Rx ant2, lna2. [13:10]: Rx ant1, lna2. [9:6]: Rx ant2, lna1. [5:0]: Rx ant1, lna1.
antCtrlChain	8	Sets XLNA control lines during any state. Detail in BB_switch_table_chn_b0/BB_switch_table_chn_b1. Each word is comprised of a repeated 2-bit setting controlling the output of xLNA control pins and specified for seven possible transmission/reception states. Starting at the LSB of the register, these states include: ▪ Idle ▪ Transmit ▪ Receive ▪ Receive with the first attenuation ▪ Receive with the second attenuation addition ▪ Receive with both attenuation conditions ▪ BT coexistence state	[63:48]	Value of chain 3, reserved
			[47:32]	Value of chain 2, reserved
			[31:16]	Value of chain 1 [15:12]: Reserved [11:10]: switch_table_b_0 when Bluetooth [9:8]: switch_table_rx12_0 when Rx ant, xatten1&2 asserted [7:6]: switch_table_rx1_0 when Rx ant, xatten1 asserted [5:4]: R/W switch_table_r_0 when Rx ant [3:2]: R/W switch_table_t_0 when Tx ant [1:0]: R/W switch_table_idle_0 when idle

Field Name	Bytes	Description	Bits	Bit Definition
		Pin name of xLNA control on IPQ40x8/IPQ40x9: ▪ Radio0 (2G, bit 0 is un-used) ▫ RF chain 0: [15:0] ▫ XLNA_0_R0: Bit 1 ▫ RF chain1: [31:16] ▫ XLNA_1_R0: Bit 1 ▪ Radio0 (5G, bit 1 is un-used) ▫ RF chain 0: [15:0] ▫ XLNA_0_R0: Bit 0 ▫ RF chain1: [31:16] ▫ XLNA_1_R0: Bit 0 ▪ Radio1 (5G, bit 1 is un-used) ▫ RF chain 0: [15:0] ▫ XLNA_0_R1: Bit 0 ▫ RF chain1: [31:16] ▫ XLNA_1_R1: Bit 0	[15:0]	Value of chain 0 [15:12]: Reserved [11:10]: switch_table_b_0 when Bluetooth [9:8]: switch_table_rx12_0 when Rx ant, xatten1&2 asserted [7:6]: switch_table_rx1_0 when Rx ant, xatten1 asserted [5:4]: R/W switch_table_r_0 when Rx ant [3:2]: R/W switch_table_t_0 when Tx ant [1:0]: R/W switch_table_idle_0 when idle
fem_xpa_set	1	Reserved	[7:0]	Reserved
rxFilterCap	1	Reserved	[7:0]	Reserved
rxGainCap	1	Reserved	[7:0]	Reserved
txrxgain	1	Tx and Rx gain table index SW will fill the INI tables to use based on Tx and Rx gain index (in code arxxx_ini.c)	[7:4]	Tx gain table index Index 0 for XPA; Index 1 for IPA
			[3:0]	Rx gain table index Index 0 for XPA; Index 1 for IPA
dpdCtrl	2	Reserved	[15:0]	Reserved
dpdTxFirCoeffSel	1	Reserved	[7:0]	Reserved
dpdInitRxBbGain	1	Reserved	[7:0]	Reserved
dpdVht80Mask	4	DPD Configuration	[31:0]	Value
dpdInitRxBbGainLow	1	Reserved	[7:0]	Reserved
dpdInitRxBbGainHi	1	Reserved	[7:0]	Reserved
dpdMaxIndexRef	1	Reserved	[7:0]	Reserved
dpdTrainPwrInc_t7	1	Reserved	[7:0]	Reserved

Field Name	Bytes	Description	Bits	Bit Definition
dpdNoiseRatio	1	DPD configuration	[7:0]	Value
dpdStartCoarseIdx	1	DPD configuration	[7:0]	Value
unUsed	2	Reserved	[15:0]	Reserved
dpdTxFirCoeffMem	1	Reserved	[7:0]	Reserved
clpcAttenTargetPwrChain0	1	Not applied	[7:0]	Reserved
clpcAttenTargetPwrChain1	1	Not applied	[7:0]	Reserved
clpcPdetTiaGain	1	Not applied	[7:0]	Reserved
clpcSensitivePdadc	1	Not applied	[7:0]	Reserved
thermal_interval	1	Change thermal interval to select suitable alpha thermal slope.	[7:0]	Value 0 is using default value (40).
thermal_interval_lowTemp	1	Change thermal interval for low temperature.	[7:0]	Value 0 is using default value (45).
calPowerOffset	1	Not applied	[7:0]	Reserved
clpcLpfHighLowTiaHighGain	1	Not applied	[7:0]	Reserved
clpcSqGain	1	Not applied	[7:0]	Reserved
dpdTargetPwrMax	1	DPD configuration	[7:0]	Value
dpdTargetPwrMin	1	DPD configuration	[7:0]	Value
paprdAttenTable	20	DPD configurations: 6 DPD table * 3 frequency piers for low, middle, high frequency Set DPD attn value #define HALPHY_2G_LOW_FREQ 2412 #define HALPHY_2G_MID_FREQ 2442 #define HALPHY_2G_HIGH_FREQ 2484 #define HALPHY_5G_LOW_FREQ 4915 #define HALPHY_5G_MID_FREQ 5370 #define HALPHY_5G_HIGH_FREQ 5825	[159:151]	Reserved
			[23:16], [47:40], [71:64], [95:88], [119:112], [143:136]	Value for high frequency
			[15:8], [39:32], [63:56], [87:80], [111:104], [135:128]	Value for middle frequency

Field Name	Bytes	Description	Bits	Bit Definition
			[7:0], [31:24], [55:48], [79:72], [103:96], [127:120]	Value for low frequency
minCCAPwrThresh	2	Setup minCCA power threshold This field is valid if flag2[bit2] = 1	[15:0]	Value
TxIQMaxTxGain	1	Change Max Tx Gain index for Tx IQ CAL. 0: Use default value	[31:0]	Value
minPwr4TPCErrCorr	1	When TPC_LOWER_PERFORM was set in OTP and power is lower than this value, disable CLPC error correct.	[7:0]	Value. Unit is 1/2 dB
startChannel	1	Limit start channel (channel number. Ex 1, 36,..)	[7:0]	Value (0 means support all channels)
endChannel	1	Limit end channel (channel number. Ex 1, 36,..)	[7:0]	Value (0 means support all channels)
tempSlopeGLUTShift	1	Reserved	[7:0]	Reserved
futureBiModal	37	Reserved	[295:0]	Reserved

A.5 Frequency modal EEPROM header

Table A-5 Frequency modal EEPROM header

Field Name	Bytes	Description	Bits	Bit Definition
xatten1DB	16	2 chains' attenuation in dBs. The value is provided by switch (first stage of attenuation). Details in BB_ext_atten_switch_ctl_bx.	[127:64]	Reserved
			[63:56]	For chain1, value5GHigh frequencies: 5785-
			[55:48]	For chain1, value5GMid frequencies: 5500-5785
			[47:40]	For chain1, value5GLow frequencies: 5180-5500
			[39:32]	For chain1, value2G
			[31:24]	For chain0, value5GHigh frequencies: 5785-
			[23:16]	For chain0, value5GMid frequencies: 5500-5785
			[15:8]	For chain0, value5GLow frequencies: 5180-5500
			[7:0]	For chain0, value2G
xatten1Margin	16	2 chains, margin-to-max receiver gain in dBs before first stage of switch attenuation is activated. Details in BB_ext_atten_switch_ctl_bx.	[63:56]	For chain1, value5GHigh frequencies: 5785-
			[55:48]	For chain1, value5GMid frequencies: 5500-5785
			[47:40]	For chain1, value5GLow frequencies: 5180-5500
			[39:32]	For chain1, value2G
			[31:24]	For chain0, value5GHigh frequencies: 5785-
			[23:16]	For chain0, value5GMid frequencies: 5500-5785
			[15:8]	For chain0, value5GLow frequencies: 5180-5500
			[7:0]	For chain0, value2G
xatten1Hyst	16	Reserved 2 chains, Margin-to-max receiver gain in dB, before first stage of switch attenuation is activated. Detail in BB_gain_force_max_gains_bx	[63:56]	Reserved
			[55:48]	
			[47:40]	
			[39:32]	
			[31:24]	
			[23:16]	
			[15:8]	
			[7:0]	

Field Name	Bytes	Description	Bits	Bit Definition
xatten1HystHT40	16	Reserved 2 chains, Margin-to-max receiver gain in dB, before activing first stage of switch attenuation. Detail in BB_ext_atten_switch_ctl_bx	[63:56]	Reserved
			[55:48]	
			[47:40]	
			[39:32]	
			[31:24]	
			[23:16]	
			[15:8]	
			[7:0]	
xatten1HystHT80	16	Reserved 2 chains, Margin-to-max receiver gain in dB, before activing first stage of switch attenuation. Detail in BB_ext_atten_switch_ctl_bx	[63:56]	Reserved
			[55:48]	
			[47:40]	
			[39:32]	
			[31:24]	
			[23:16]	
			[15:8]	
			[7:0]	
xlnaGain	4	xlnaGain for 4 chains	[31:16]	Reserved
			[15:8]	xlnaGain for Chain 1
			[7:0]	xlnaGain for Chain 0
Reserved	64	Reserved for future use	[511:0]	Reserved

A.6 Spur mitigation

Table A-6 Spur mitigation

Field Name	Bytes	Description	Bits	Bit Definition
spurRssiThresh	1	RSSI threshold to enable spur	[7:0] Decimal value	The RSSI threshold to enable the spur mitigation. Spur mitigation is disabled above this RSSI threshold.
spurRssiThreshCCK	1	RSSI threshold to enable spur in CCK mode	[7:0] Decimal value	Barker RSSI threshold to disable CCK spur mitigation, signed number from -128 to 127.
spurMitFlag	1	Additional flag to control spur mitigation behavior	[7:4]	Reserved
			[3]	SKIP_STRENGTH Disable strength comparison. Spurs will be sorted only by their distance from the central frequency or primary channel.
			[2]	THRESHOLD_OVERRIDE
			[1]	MASK_OVERRIDE. Override mask settings.
			[0]	Reserved FILTER_TYPE_OVERRIDE. Override CCK spur filter setting.
spurMitFreqMax	1	FD spur configuration	[7:0]	Maximum concurrent in-band spurs to be mitigated. Value: 1-8 Setting to 0 will be treated as all allowed (=8).
spurChans_CCK	6	Reserved	[47:0]	Reserved
spurChans_2G	8	Spur channels in usual fbin coding format	[63:0]	Store 2G spur frequency. To save storage space, each spur takes one byte only: spur = 2300 + [offset] E.g. spur at 2464 MHz, store 164 to spurChans_2G []. Totally 6 spurs can be saved. Note: CCK & OFDM use the same spur channel settings.
spurStr_2G	8	Spur configuration	[63:0]	Store 2G spur strength. The order to input should follow the order of spurChans_2G.
spurChans_5G	64	Spur channels in usual fbin coding format	[4095:0]	Store 5G spur frequency. Each spur takes TWO bytes. E.g. spur at 5424 MHz, store 5424 to spurChans_5G []. Totally 24 spurs can be saved.

Field Name	Bytes	Description	Bits	Bit Definition
spurStr_5G	32	Spur configuration	[255:0]	Store 5G spur strength. The order to input should follow the order of spurChans_5G.
spur_config_reserve	3	Reserved	[23:0]	Reserved
spurThreshold	5	Spur configuration	[39:32]	SPUR_THRESHOLD_CCK: CCK spur mitigation Default value is -105. This field is available when spurMitFlag[2] = 1.
			[31:24]	SPUR_THRESHOLD_DATA_FD: frequency domain spur mitigation Default value is -106. This field is available when spurMitFlag[2] = 1.
			[23:16]	SPUR_THRESHOLD_DATA_TD: time domain spur mitigation. Default value is -95. This field is available when spurMitFlag[2] = 1.
			[15:8]	SPUR_THRESHOLD_SELFCOR: SelfCor spur mitigation. Default value is -98 if not overridden. This field is available when spurMitFlag[2] = 1.
			[7:0]	SPUR_THRESHOLD_AGC: AGC spur mitigation. Default value is -98 if not overridden. This field is available when spurMitFlag[2] = 1.
spurPuncMask	1	Spur configuration	[7:0]	Value to set register CF_PUNC_MASK. This field is available when spurMitFlag[1] = 1.
spurPilotMask	1	Spur configuration	[7:0]	Value to set register CF_PILOT_MASK. This field is available when spurMitFlag[1] = 1.
spurChanMask	1	Spur configuration	[7:0]	Value to set register CF_CHAN_MASK. This field is available when spurMitFlag[1] = 1.

A.7 Pre-calibration data

Table A-7 Pre-calibration data

Fieldname	Byte	Description	Example 5G values	Example 2G values
gainIdxForCal	1*32	Specify the gain indexes that should be used during calibration.	3 7 9 11 13 15 17 19 21 23 25 27 29 (255 = Not used)	5 7 9 11 13 15 17 19 21 23 25 27 29 (255 = Not used)
dacGainForCal	1*32	Specify the dac gain to use for each gain index specified above.	"-8 -8 -8 -8 -8 -8 -8 -8 -8 -8 -8 -8 -8" (Typically the same value is used for each.)	"-8 -8 -8 -8 -8 -8 -8 -8 -8 -8 -8 -8 -8" (Typically the same value is used for each.)
paConfigForCal	1*32	Only used for power calibration.	Reserved	Reserved
calPwrTargets	1*5	Specifies the desired powers for the 5 points of the gain look up table, in 8th of dBm (ie power value * 8).	176 144 104 64 24 (22, 18, 13, 8, 3 dBm)	160 132 104 72 40
calPdadcTargets	1*5	Specifies the desired values for the 5 points of the power to pdadc table.	200 125 80 50 30	200 125 80 50 30
pdetAttenProfile_32nddb	1*15	Reserve The size of the feedback signal back to chip is controlled by attenuation – 16 levels. This table specifies the amount of attenuation applied from each level. In 1/32th db (ie 32 = 1db). This table specifies the amount of attenuation applied from each level. In 1/32th db (ie 32 = 1db).But this entry is not applied for use.	Reserve	Reserve
pdetTiaGainProfile_8thdb	1	Reserve Gain can also be applied to the feedback signal (It is either on or off). Specifies the difference in gain between off and on. (in 1/8th db). But this entry is not applied for use.	Reserve	Reserve

Fieldname	Byte	Description	Example 5G values	Example 2G values
alutOffset	1	Reserved Specifies the amount of attenuation (index into pdetAttenProfile table) that should be applied during calibration. But this entry is not applied for use.	Reserve	Reserve
pdetRange_8thdb	1	Reserved Controls the power range over which the feedback path gain. The attenuator settings used during calibration can be used. (in 1/8th dB) This value is the amount to add to the minimum, and remove from the maximum power in the power to pdadc measurements stored in non-volatile memory. But this entry is not applied for use.	Reserve	Reserve
txPwrOffset	1	Used to offset the power table to accommodate negative powers. This field was used when vaild=1 and boardFlags[1]=1 (WHAL_BOARD_ZERO_DBM).	0	0
Valid	1	Set to 1 to use above values from board data file, otherwise the code defaults can be used.	1	1
unused	2	Reserved	Reserved	Reserved
calDataTgtPwr	32	This field was used when vaild=1 and flag2[5]=1. Change goal power of QSPR while power calibration. Please fill 255 if not use. The unit is 1/8 dBm.	0 0 0 0 18 32 50 65 84 96 114 124 135 143 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255	0 0 0 3 13 29 47 69 87 105 119 130 137 142 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255

A.8 Misc

Table A-8 Misc

Fieldname	Byte	Description	Bits	Bit Definition
pasetting_2g	72	Reserved		Reserved
pasetting_5g	64	Reserved		Reserved
pefsetting	12	Reserved		Reserved
noachsetting	8	Reserved		Reserved
DPDBWTable	36	Reserved		Reserved
pad31	2	Reserved		Reserved
PefCoefI	20	PEF configuration		Reserved
PefCoefQ	20	PEF configuration		Reserved
PefCoefI_HT40	20	PEF configuration		Reserved
PefCoefQ_HT40	20	PEF configuration		Reserved
PefCoefI_HT80	20	PEF configuration		Reserved
PefCoefQ_HT80	20	PEF configuration		Reserved
antCtrlCommon_vmode5G	4	Switch com setting for vmode for 5G only. boardFlags[20] = 1 to enable this feature	[31:0]	value
antCtrlCommon2_vmode5G	4		[31:0]	value
pad30	24	Reserved		Reserved
calData5G_PLUT_Future	92	Reserved		Reserved
powerOffset_HT20	10	mapping to MCS0~9 for BW20		value
powerOffset_HT40	10	mapping to MCS0~9 for BW40		value
powerOffset_HT80	10	mapping to MCS0~9 for BW80		value
powerOffset5G_reserved	226	Reserved		Reserved
dpdTargetAgc2LUT	24	If it is "0", halphy sets "-13" by default this is signed value (A_INT8)		
pad0	63	Reserved		Reserved
calData2G_PLUT_Future	44	Reserved		Reserved

Fieldname	Byte	Description	Bits	Bit Definition
pad1	5	Reserved		Reserved
powerOffset_HT20	10	mapping to MCS0~9 for BW20		value
powerOffset_HT40	10	mapping to MCS0~9 for BW40		value
powerOffset_HT80	10	mapping to MCS0~9 for BW80		value
txcalMappingDeltaTbl	64	change TxCalMappingDelta table		value
TxIQ2ndGroupStartTGI	1	start Tx Gain index of 2nd group		value (0~31)
TxIQ3rdGroupStartTGI	1	start Tx Gain index of 3rd group		value (0~31)
TxIQ1stGroupDA	1	DA value for 1st group		value (0~7)
TxIQ2ndGroupDA	1	DA value for 2nd group		value (0~7)
TxIQ3rdGroupDA	1	DA value for 3rd group		value (0~7)
txiq_pad	3	Reserved		Reserved
powerOffset2G_reserved	26	Reserved		Reserved

A.9 2.4 GHz calibration

Table A-9 2.4 GHz calibration

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/Field Description	Bits	Bit Definition
calFreqPier2G	calFreqPier2G	16	2 GHz channels that are calibrated. Ex: Decimal + 2300Hz = channel frequency	[127:0]	1 byte per channel (Max 16 channel)
	calFreqPier2G _ext	16	Extend for channel calibrated flag	[127:0]	–
calPierData2G (OLPC) = calibration data stored per point per channel per RF chain. (NumOfChain*10B (calPerPoint) + 4B(dacGain) + 5B(therm/vol)) * NumOfChannels (4*10+9)*14 = 686 Bytes	calPerPoint (per chain)	1	Tx gain index CAL point 1	[7:3]	Value of CAL gain index
			PA setting CAL point 1	[2:0]	Value of CAL PA setting
		1	meas_pwr CAL point 1	[7:0]	Value of measured power
		1	Tx gain index CAL point 2	[7:3]	Value of CAL gain index
			PA setting CAL point 2	[2:0]	Value of CAL PA setting
		1	meas_pwr CAL point 2	[7:0]	Value of measured power
		1	Tx gain index CAL point 3	[7:3]	Value of CAL gain index
			PA setting CAL point 3	[2:0]	Value of CAL PA setting
		1	meas_pwr CAL point 3	[7:0]	Value of measured power
		1	Tx gain index CAL point 4	[7:3]	Value of CAL gain index
			PA setting CAL point 4	[2:0]	Value of CAL PA setting
		1	meas_pwr CAL point 4	[7:0]	value of measured power
		1	Tx gain index CAL point 5	[7:3]	Value of CAL gain index
			PA setting CAL point 5	[2:0]	Value of CAL PA setting
		1	meas_pwr CAL point 5	[7:0]	Value of measured power
	dacGain (per chain)	1	dacGain of glut gain setting	[7:0]	Value
	thermCalVal (per chain)	1	therm_cal_value (not per chain)	[7:0]	Value
	voltCalVal	1	volt_cal_value (not per chain)	[7:0]	Value

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/Field Description	Bits	Bit Definition
pad0	pad0	63	Pad0	–	–
calData2G_PLUT_Future	calData2G_PLUT_Future	44	–	[351:0]	–
pad1	pad1	5	–	[39:0]	–
powerOffset2G	powerOffset2G	128	Reserved Can be used for power offset for CCK/OFDM 20/40/80 16 channels; 4 chains.	[1023:0]	Reserved
calPierData2G_CLPC (5points*2Byte*4Chains)*14 Piers = 560 Bytes	pdadc_read	1	PDADC value for each CAL point	[7:0]	PDADC value for each CAL point
	meas_pwr	1	Measured power value for each CAL point	[7:0]	Measured power value for each CAL point
calData2GFuture	calData2GFuture	560	Reserved	[4479:0]	Reserved
alutFuture2G	alutFuture2G	92	Reserved	[735:0]	Reserved
extTPow2xDelta2G	extTPow2xDelta2G	24	Extend target power delta from 4bit to 5bit. Here are all rates 5th bits.	[192:0]	5th bits of target power delta
Target powers for channels	calTargetFreqbinCck	2	802.11b target powers for the following channels. Ex: Decimal + 2300Hz = channel frequency	[15:0]	1 byte per channel (up to 2 channels)
	calTargetFreqbin2G	3	802.11g target powers for the following channels. Ex: Decimal + 2300Hz = channel frequency	[23:0]	1 byte per channel (up to 3 channels)
	pad11	3	Reserved space for byte alignment	[23:0]	Reserved
	targetFreqbin2GVHT20	4	HT20/VHT20 target powers for the following channels. Ex: Decimal + 2300Hz = channel frequency	[31:0]	1 byte per channel (up to 4 channels)

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/Field Description	Bits	Bit Definition
	targetFreqbin2GVHT40	4	HT40/VHT40 Target powers for the following channels Ex: Decimal + 2300Hz = channel frequency	[31:0]	1 byte per channel (up to 4 channels)
pad2	pad2	4	–	[31:0]	–
Target power for DSSS & HR/DSSS rates. 4 bytes per channel * 2 channels = 8 Bytes	targetPowerCCk	4	Target powers for 802.11b rates Ex: Decimal/2 = Power level [dBm]	[31:24]	11(S) Mbps
				[23:16]	11(L) Mbps
				[15:8]	5.5(S) Mbps
				[7:0]	1 Mbps -5.5(L) Mbps
Target power for 2 GHz HT20/VHT20 rates 20 bytes per channel * 4 channels = 80 bytes	targetPower2GVHT20	20	VHT20 MCS9	[159:152]	[MU]MCS9
			VHT20 MCS8	[151:144]	[MU]MCS8
			HT20/VHT20 MCS7	[143:136]	[MU]MCS7
			Legacy 54, HT20/VHT20 MCS6	[135:128]	[MU]MCS6
			Legacy 48, HT20/VHT20 MCS5	[127:120]	[MU]MCS5
			Legacy 36, HT20/VHT20 MCS4	[119:112]	[MU]MCS4
			Legacy 24, HT20/VHT20 MCS3	[111:104]	[MU]MCS3
			Legacy 18, HT20/VHT20 MCS2	[103:96]	[MU]MCS2
			Legacy 12, HT20/VHT20 MCS1	[95:88]	[MU]MCS1
			Legacy 6/9, HT20/VHT20 MCS0	[87:80]	[MU]MCS0
			VHT20 MCS9	[79:72]	[SU]MCS9
			VHT20 MCS8	[71:64]	[SU]MCS8
			HT20/VHT20 MCS7	[63:56]	[SU]MCS7
			Legacy 54, HT20/VHT20 MCS6	[55:48]	[SU]MCS6
			Legacy 48, HT20/VHT20 MCS5	[47:40]	[SU]MCS5
			Legacy 36, HT20/VHT20 MCS4	[39:32]	[SU]MCS4
			Legacy 24, HT20/VHT20 MCS3	[31:24]	[SU]MCS3
			Legacy 18, HT20/VHT20 MCS2	[23:16]	[SU]MCS2
			Legacy 12, HT20/VHT20 MCS1	[15:8]	[SU]MCS1
			Legacy 6/9, HT20/VHT20 MCS0	[7:0]	[SU]MCS0

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/Field Description	Bits	Bit Definition
Target power for 2 GHz HT40/VHT40 rates 20 bytes per channel * 4 channels = 80 bytes	targetPower2GVHT40	20	VHT40 MCS9	[159:152]	[MU]MCS9
			VHT40 MCS8	[151:144]	[MU]MCS8
			HT40/VHT40 MCS7	[143:136]	[MU]MCS7
			HT40/VHT40 MCS6	[135:128]	[MU]MCS6
			HT40/VHT40 MCS5	[127:120]	[MU]MCS5
			HT40/VHT40 MCS4	[119:112]	[MU]MCS4
			HT40/VHT40 MCS3	[111:104]	[MU]MCS3
			HT40/VHT40 MCS2	[103:96]	[MU]MCS2
			HT40/VHT40 MCS1	[95:88]	[MU]MCS1
			HT40/VHT40 MCS0	[87:80]	[MU]MCS0
			VHT40 MCS9	[79:72]	[SU]MCS9
			VHT40 MCS8	[71:64]	[SU]MCS8
			HT40/VHT40 MCS7	[63:56]	[SU]MCS7
			HT40/VHT40 MCS6	[55:48]	[SU]MCS6
			HT40/VHT40 MCS5	[47:40]	[SU]MCS5
			HT40/VHT40 MCS4	[39:32]	[SU]MCS4
			HT40/VHT40 MCS3	[31:24]	[SU]MCS3
			HT40/VHT40 MCS2	[23:16]	[SU]MCS2
			HT40/VHT40 MCS1	[15:8]	[SU]MCS1
			HT40/VHT40 MCS0	[7:0]	[SU]MCS0
Rate TPC PA BW	rateTpcPaGTX2GTable	40	Reserved	Reserved	Reserved

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/Field Description	Bits	Bit Definition
2G CTL 11b Index	ctlIndex2G_11b	12	6 indexes Each index includes 2 bytes 2 modes, 3 regulatory domains.	[15:12]	SS mask Specify which spatial stream the CTL applies for. 4 bit binary mask, with 1 bit for each of 4 stream combinations. More than 1 bit set means the CTL applies to each of the spatial stream rate groups which are set. 0001 = apply CTL power to 1 spatial stream rate 0010 = apply CTL power to 2 spatial stream rates. 0100 = apply CTL power to 3 spatial stream rates. 1000 = apply CTL power to 4 spatial stream rates.
				[11:8]	Chain mask stream Specify which chain operating modes the CTL applies for. 4 bit binary mask, with 1 bit for each chain operating mode. More than 1 bit set means the CTL applies to each of the chain operation modes which are set. 0001 = apply CTL power when 1 chain is transmitting. 0010 = apply CTL power when 2 chains are transmitting. 0100 = apply CTL power when 3 chains are transmitting. 1000 = apply CTL power when 4 chains are transmitting.
				[7:4]	REG DOMN
				[3]	BF
				[2:0]	MODE 11b = 0x1 Legacy (11a or 11g) = 0x0 (V)HT20 = 0x2 (V)HT40 = 0x3 VHT80 = 0x4
2G CTL 11b Frequency bin	ctlFreqbin2G_11b	27	(Frequency_in_MHz – 2300) 9 channels 3 domains (FCC, MKK, ETSI)	[3:0]	Frequency
Padding	–	1	–	–	–

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/Field Description	Bits	Bit Definition
2G CTL 11b data Bin	ctlData2G_11b	54	1 PWR VAL for frequency and mode 2 modes, 9 channels, 3 regulatory domains	[3:0]	dBm
2G CTL HT20/VHT20 index	ctlIndex2G_ HT20/VHT20	60	30 indexes Each index includes 2 bytes 10 modes, 3 regulatory domains.	[15:12]	SS mask Specify which spatial stream the CTL applies for. 4 bit binary mask, with 1 bit for each of 4 stream combinations. More than 1 bit set means the CTL applies to each of the spatial stream rate groups which are set. 0001 = apply CTL power to all 1 spatial stream rates. 0010 = apply CTL power to all 2 spatial stream rates. 0100 = apply CTL power to all 3 spatial stream rates. 1000 = apply CTL power to all 4 spatial stream rates.
				[11:8]	Chain mask stream Specify which chain operating modes the CTL applies for. 4 bit binary mask, with 1 bit for each chain operating mode. More than 1 bit set means the CTL applies to each of the chain operation modes which are set. 0001 = apply CTL power when only 1 chain is transmitting. 0010 = apply CTL power when 2 chains are transmitting. 0100 = apply CTL power when 3 chains are transmitting. 1000 = apply CTL power when 4 chains are transmitting.
				[7:4]	REG DOMN
				[3]	BF. Beamforming Set to 1 to specify with beamforming Set to 0 to specify without beamforming
				[2:0]	MODE 11b = 0x1 Legacy (11a or 11g) = 0x0 (V)HT20 = 0x2 (V)HT40 = 0x3 VHT80 = 0x4

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/Field Description	Bits	Bit Definition
2G CTL HT20/VHT20 Frequency Bin	ctlFreqbin2G_ HT20/VHT20	33	(Frequency_in_MHz – 2300) 11 channels 3 domains (FCC, MKK, ETSI)	[3:0]	Frequency
Padding	–	1	–	–	–
2G CTL HT20/VHT20 data Bin	ctlData2G_ HT20/VHT20	330	1 PWR VAL for frequency and mode 10 modes, 11 channels, 3 regulatory domains	[3:0]	dBm
2G CTL HT40/VHT40 index	ctlIndex2G_ HT40/VHT40	36	18 indexes Each index includes 2 bytes 6 modes, 3 regulatory domains (FCC, MKK, ETSI).	[15:12]	SS mask Specify which spatial stream the CTL applies for. 4 bit binary mask, with 1 bit for each of 4 stream combinations. More than 1 bit set means the CTL applies to each of the spatial stream rate groups which are set. 0001 = apply CTL power to all 1 spatial stream rates. 0010 = apply CTL power to all 2 spatial stream rates. 0100 = apply CTL power to all 3 spatial stream rates. 1000 = apply CTL power to all 4 spatial stream rates.
				[11:8]	Chain mask stream Specify which chain operating modes the CTL applies for. 4 bit binary mask, with 1 bit for each chain operating mode. More than 1 bit set means the CTL applies to each of the chain operation modes which are set. 0001 = apply CTL power when only 1 chain is transmitting. 0010 = apply CTL power when 2 chains are transmitting. 0100 = apply CTL power when 3 chains are transmitting. 1000 = apply CTL power when 4 chains are transmitting.
				[7:4]	REG DOMN
				[3]	BF

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/Field Description	Bits	Bit Definition
				[2:0]	MODE 11b = 0x1 Legacy (11a or 11g) = 0x0 (V)HT20 = 0x2 (V)HT40 = 0x3 VHT80 = 0x4
2G CTL HT40/VHT40 Frequency Bin	ctlFreqbin2G_ HT40/VHT40	18	(Frequency_in_MHz – 2300) 6 channels 3 domains (FCC, MKK, ETSI)	[3:0]	Frequency
2G CTL HT40/VHT40 data bin	ctlData2G_ HT40/VHT40	108	1 PWR VAL for frequency and mode 6 modes, 6 channels, 3 regulatory domains	[3:0]	dBm
2G CTL spare	–	4	–	–	–
Alpha thermal channel 4 bytes per chain * 4 RF chains = 16 Bytes	tempCompChans2G	4	Alpha thermal channel index Ex: Decimal + 2300Hz = Channel frequency	[31:0]	1 byte per channel (Max 4 channel)
Alpha thermal table 4 bytes per chain * 4 channels * 4 RF chains = 32 Bytes	tempComp2G	4	Alpha thermal table	[31:24]	85
				[23:16]	45
				[15:8]	-10
				[7:0]	-40

A.10 5 GHz calibration

Table A-10 5 GHz calibration, target and control power

Structure description	Structure name/field name	Bytes	Structure detail/field description	Bits	Bit definition
calFreqPier5G	calFreqPier5G	32	5GHz channels that are calibrated. Ex: (Decimal*5) + 4800Hz = channel frequency	[255:0]	1 byte per channel (Max 32 channel)
	calFreqPier5G _ext	32	Extend for channel calibrated flag	[255:0]	–
calPierData5G (OLPC) calibration data stored per point per channel per RF chain. (NumOfChain*11B + 4(therm)+1vol))* 32 channels = (4*11B+5B)*32 = 1568 Bytes	calPerPoint	1	Tx gain index CAL point 1	[7:3]	Value of CAL gain index
			PA setting CAL point 1	[2:0]	Value of CAL PA setting
		1	meas_pwr CAL point 1	[7:0]	Value of measured power
		1	Tx gain index CAL point 2	[7:3]	Value of CAL gain index
			PA setting CAL point 2	[2:0]	Value of CAL PA setting
		1	meas_pwr CAL point 2	[7:0]	Value of measured power
		1	Tx gain index CAL point 3	[7:3]	Value of CAL gain index
			PA setting CAL point 3	[2:0]	Value of CAL PA setting
		1	meas_pwr CAL point 3	[7:0]	Value of measured power
		1	Tx gain index CAL point 4	[7:3]	Value of CAL gain index
			PA setting CAL point 4	[2:0]	Value of CAL PA setting
		1	meas_pwr CAL point 4	[7:0]	Value of measured power
		1	Tx gain index CAL point 5	[7:3]	Value of CAL gain index
			PA setting CAL point 5	[2:0]	Value of CAL PA setting
		1	meas_pwr CAL point 5	[7:0]	Value of measured power
	dacGain (Per Chain)	1	dacGain of glut gain setting	[7:0]	Value
	thermCalVal (Per Chain)	1	Thermal CAL value	[7:0]	Value
	voltCalVal	1	Voltage CAL value	[7:0]	Value

Structure description	Structure name/field name	Bytes	Structure detail/field description	Bits	Bit definition
pad30	Padding	32	padding	[255:0]	–
calData5G_PLUT_Future	calData5G_PLUT_Future	92	calData5G_PLUT_Future	[735:0]	Reserved
Pad31	Padding	2	padding	[15:0]	–
powerOffset5G	powerOffset5G	256	Used for power offset for CCK/OFDM 20/40/80 32 channels; 4 chains	[2047:0]	Reserved
calPierData5G_CLPC (5points*2B*4Chains)* 32 Piers = 1280 bytes	pdadc_read	1	PDADC value for each CAL point	[7:0]	PDADC value for each CAL point
	meas_pwr	1	Measured power value for each CAL point	[7:0]	Measured power value for each CAL point
calData5G_plut_future	calData5G_plut_future	1280	Reserved space for store additional channels PLUT: 5point*2data*4chains*32channels = 1280	[10239:0]	Reserved
alutFuture	alutFuture	72	–	[375:0]	–
extTPow2xDelta5G	extTPow2xDelta5G	72	Extend target power delta from 4bit to 5bit. Here are the all rates 5th bits.	[375:0]	5th bits of target power delta
Target powers for channels	targetFreqbin5G	8	11a target powers for the following channels Ex: (Decimal*5) + 4800Hz = channel frequency	[47:0]	1 byte per channel (Max 6 channel)
	targetFreqbin5GVHT20	8	HT20/VHT20 target powers for the following channels Ex: (Decimal*5) + 4800Hz = channel frequency	[47:0]	1 byte per channel (Max 6 channel)
	targetFreqbin5GVHT40	8	HT40/VHT40 target powers for the following channels Ex: (Decimal*5) + 4800Hz = channel frequency	[47:0]	1 byte per channel (Max 6 channel)
	targetFreqbin5GVHT80	8	VHT80 target powers for the following channels Ex: (Decimal*5) + 4800Hz = channel frequency	[47:0]	1 byte per channel (Max 6 channel)

Structure description	Structure name/field name	Bytes	Structure detail/field description	Bits	Bit definition
Target power for 5 GHz HT20/VHT20 rates 20 bytes per channel * 4 channels = 80 bytes	targetPower5GVHT20	20	VHT20 MCS9	[159:152]	[MU]MCS9
			VHT20 MCS8	[151:144]	[MU]MCS8
			HT20/VHT20 MCS7	[143:136]	[MU]MCS7
			Legacy 54, HT20/VHT20 MCS6	[135:128]	[MU]MCS6
			Legacy 48, HT20/VHT20 MCS5	[127:120]	[MU]MCS5
			Legacy 36, HT20/VHT20 MCS4	[119:112]	[MU]MCS4
			Legacy 24, HT20/VHT20 MCS3	[111:104]	[MU]MCS3
			Legacy 18, HT20/VHT20 MCS2	[103:96]	[MU]MCS2
			Legacy 12, HT20/VHT20 MCS1	[95:88]	[MU]MCS1
			Legacy 6/9, HT20/VHT20 MCS0	[87:80]	[MU]MCS0
			VHT20 MCS9	[79:72]	[SU]MCS9
			VHT20 MCS8	[71:64]	[SU]MCS8
			HT20/VHT20 MCS7	[63:56]	[SU]MCS7
			Legacy 54, HT20/VHT20 MCS6	[55:48]	[SU]MCS6
			Legacy 48, HT20/VHT20 MCS5	[47:40]	[SU]MCS5
			Legacy 36, HT20/VHT20 MCS4	[39:32]	[SU]MCS4
			Legacy 24, HT20/VHT20 MCS3	[31:24]	[SU]MCS3
			Legacy 18, HT20/VHT20 MCS2	[23:16]	[SU]MCS2
			Legacy 12, HT20/VHT20 MCS1	[15:8]	[SU]MCS1
			Legacy 6/9, HT20/VHT20 MCS0	[7:0]	[SU]MCS0
Target power for 5 GHz HT40/VHT40 rates 20 bytes per channel * 4 channels = 80 bytes	targetPower5GVHT40	20	VHT40 MCS9	[159:152]	[MU]MCS9
			VHT40 MCS8	[151:144]	[MU]MCS8
			HT40/VHT40 MCS7	[143:136]	[MU]MCS7
			HT40/VHT40 MCS6	[135:128]	[MU]MCS6
			HT40/VHT40 MCS5	[127:120]	[MU]MCS5
			HT40/VHT40 MCS4	[119:112]	[MU]MCS4
			HT40/VHT40 MCS3	[111:104]	[MU]MCS3
			HT40/VHT40 MCS2	[103:96]	[MU]MCS2

Structure description	Structure name/field name	Bytes	Structure detail/field description	Bits	Bit definition
			HT40/VHT40 MCS1	[95:88]	[MU]MCS1
			HT40/VHT40 MCS0	[87:80]	[MU]MCS0
			VHT40 MCS9	[79:72]	[SU]MCS9
			VHT40 MCS8	[71:64]	[SU]MCS8
			HT40/VHT40 MCS7	[63:56]	[SU]MCS7
			HT40/VHT40 MCS6	[55:48]	[SU]MCS6
			HT40/VHT40 MCS5	[47:40]	[SU]MCS5
			HT40/VHT40 MCS4	[39:32]	[SU]MCS4
			HT40/VHT40 MCS3	[31:24]	[SU]MCS3
			HT40/VHT40 MCS2	[23:16]	[SU]MCS2
			HT40/VHT40 MCS1	[15:8]	[SU]MCS1
			HT40/VHT40 MCS0	[7:0]	[SU]MCS0
Target power for 5 GHz VHT80 rates 20 bytes per channel * 4 channels = 80 bytes	targetPower5 GVHT80	20	VHT80 MCS9	[159:152]	[MU]MCS9
			VHT80 MCS8	[151:144]	[MU]MCS8
			VHT80 MCS7	[143:136]	[MU]MCS7
			VHT80 MCS6	[135:128]	[MU]MCS6
			VHT80 MCS5	[127:120]	[MU]MCS5
			VHT80 MCS4	[119:112]	[MU]MCS4
			VHT80 MCS3	[111:104]	[MU]MCS3
			VHT80 MCS2	[103:96]	[MU]MCS2
			VHT80 MCS1	[95:88]	[MU]MCS1
			VHT80 MCS0	[87:80]	[MU]MCS0
			VHT80 MCS9	[79:72]	[SU]MCS9
			VHT80 MCS8	[71:64]	[SU]MCS8
			VHT80 MCS7	[63:56]	[SU]MCS7
			VHT80 MCS6	[55:48]	[SU]MCS6
			VHT80 MCS5	[47:40]	[SU]MCS5
			VHT80 MCS4	[39:32]	[SU]MCS4

Structure description	Structure name/field name	Bytes	Structure detail/field description	Bits	Bit definition
			VHT80 MCS3	[31:24]	[SU]MCS3
			VHT80 MCS2	[23:16]	[SU]MCS2
			VHT80 MCS1	[15:8]	[SU]MCS1
			VHT80 MCS0	[7:0]	[SU]MCS0
RATE_TPC_PA_BW	rateTpcPaGTX5GTable	60	Reserved	[479:0]	Reserved
	targetPower5GFuture	20	Reserved	[159:0]	Reserved
	configAddr	127	▪ 0x0111a428 0x0b34022c: Indicates to program reg 0x1a428 to 0x0b34022c after BB calibration. ▪ 0x0011a428 0x0b34022c: Indicates to program reg 0x1a428 to 0x0b34022c before BB calibration. ▪ 0x0111a428 0x11111111: Indicates reg 0x1a428 = 0x11111111 for both 2G and 5G. ▪ 0x0121a428 0x11111111 0x22222222: Indicates reg 0x1a428 =: ▫ 0x11111111 for 2G; ▫ 0x22222222 for 5G ▪ 0x0131a428 0x11111111 0x22222222 0x33333333 0x44444444 0x55555555: Indicates reg0x1a428 = ▫ 0x11111111 for 2G HT20 ▫ 0x22222222 for 2G HT40 ▫ 0x33333333 for 5G HT20 ▫ 0x44444444 for 5G HT40 ▫ 0x55555555: for 5G HT80	[1015:0]	Value
Rx Gain Cal	rxGainCaltbl	192	See section 0	–	–

Structure description	Structure name/field name	Bytes	Structure detail/field description	Bits	Bit definition
Alpha thermal channel 8 bytes per chain * 4 RF chains = 32 bytes	tempCompChans5G	8	Alpha thermal channel index Ex: (Decimal x 5) + 4900Hz = channel frequency	[63:0]	1 byte per channel (Max 8 channel)
Alpha thermal table 4 bytes per chain * 8 channels * 4 RF chains = 128 bytes	alphaThermTbl	4	Alpha thermal table	[31:24]	85
				[23:16]	45
				[15:8]	-10
				[7:0]	-40
5G CTL 11a Index	ctlIndex5G_11a	18	9 indexes Each index includes 2 bytes 3 modes, 3 regulatory domains.	[15:12]	SS mask Specify which spatial stream the CTL applies for. 4 bit binary mask, with 1 bit for each of 4 stream combinations. More than 1 bit set means the CTL applies to each of the spatial stream rate groups which are set. 0001 = apply CTL power to all 1 spatial stream rates. 0010 = apply CTL power to all 2 spatial stream rates. 0100 = apply CTL power to all 3 spatial stream rates. 1000 = apply CTL power to all 4 spatial stream rates.
				[11:8]	Chain mask stream Specify which chain operating modes the CTL applies for. 4 bit binary mask, with 1 bit for each chain operating mode. More than 1 bit set means the CTL applies to each of the chain operation modes which are set. 0001 = apply CTL power when only 1 chain is transmitting. 0010 = apply CTL power when 2 chains are transmitting. 0100 = apply CTL power when 3 chains are transmitting. 1000 = apply CTL power when 4 chains are transmitting.
				[7:4]	REG DOMN
				[3]	BF
				[2:0]	MODE 11b = 0x1 Legacy (11a or 11g) = 0x0 (V)HT20 = 0x2 (V)HT40 = 0x3 VHT80 = 0x4

Structure description	Structure name/field name	Bytes	Structure detail/field description	Bits	Bit definition
5G CTL 11a frequency bin	ctlFreqbin5G_11a	75	((Frequency_in_MHz – 4800)/5) 25 channels 3 domains (FCC, MKK, ETSI)	[3:0]	Frequency
Padding	–	1	–	–	–
5G CTL 11a data Bin	ctlData5G_11a	225	1 PWR VAL for frequency and mode 3 modes, 25 channels, 3 regulatory domains	[3:0]	dBm
Padding	–	1	–	–	–
5G CTL HT20/VHT20 index	ctlIndex5G_HT20/VHT20	48	8 indexes Each index includes 2 bytes 8 modes, 3 regulatory domains.	[15:12]	SS mask Specify which spatial stream the CTL applies for. 4 bit binary mask, with 1 bit for each of 4 stream combinations. More than 1 bit set means the CTL applies to each of the spatial stream rate groups which are set. 0001 = apply CTL power to all 1 spatial stream rates. 0010 = apply CTL power to all 2 spatial stream rates. 0100 = apply CTL power to all 3 spatial stream rates. 1000 = apply CTL power to all 4 spatial stream rates.
				[11:8]	Chain mask stream Specify which chain operating modes the CTL applies for. 4 bit binary mask, with 1 bit for each chain operating mode. More than 1 bit set means the CTL applies to each of the chain operation modes which are set. 0001 = apply CTL power when only 1 chain is transmitting. 0010 = apply CTL power when 2 chains are transmitting. 0100 = apply CTL power when 3 chains are transmitting. 1000 = apply CTL power when 4 chains are transmitting.
				[7:4]	REG DOMN
				[3]	BF

Structure description	Structure name/field name	Bytes	Structure detail/field description	Bits	Bit definition
				[2:0]	MODE 11b = 0x1 Legacy (11a or 11g) = 0x0 (V)HT20 = 0x2 (V)HT40 = 0x3 VHT80 = 0x4
5G CTL HT20/VHT20 frequency bin	ctlFreqbin5G_ HT20/VHT20	75	((Frequency_in_MHz – 4800)/5) 25 channels 3 domains (FCC, MKK, ETSI)	[3:0]	Frequency
Padding	–	1	–	–	–
5G CTL HT20/VHT20 data Bin	ctlData5G_ HT20/VHT20	600	1 PWR VAL for frequency and mode 8 modes, 25 channels, 3 regulatory domains	[3:0]	dBm
5G CTL HT40/VHT40 index	ctlIndex5G_ HT40/VHT40	36	18 indexes Each index includes 2 bytes 6 modes, 3 regulatory domains (FCC, MKK, ETSI).	[15:12]	SS mask Specify which spatial stream the CTL applies for. 4 bit binary mask, with 1 bit for each of 4 stream combinations. More than 1 bit set means the CTL applies to each of the spatial stream rate groups which are set. 0001 = apply CTL power to all 1 spatial stream rates. 0010 = apply CTL power to all 2 spatial stream rates. 0100 = apply CTL power to all 3 spatial stream rates. 1000 = apply CTL power to all 4 spatial stream rates.
				[11:8]	Chain mask stream Specify which chain operating modes the CTL applies for. 4 bit binary mask, with 1 bit for each chain operating mode. More than 1 bit set means the CTL applies to each of the chain operation modes which are set. 0001 = apply CTL power when only 1 chain is transmitting. 0010 = apply CTL power when 2 chains are transmitting. 0100 = apply CTL power when 3 chains are transmitting. 1000 = apply CTL power when 4 chains are transmitting.
				[7:4]	REG DOMN

Structure description	Structure name/field name	Bytes	Structure detail/field description	Bits	Bit definition
				[3]	BF
				[2:0]	MODE 11b = 0x1 Legacy (11a or 11g) = 0x0 (V)HT20 = 0x2 (V)HT40 = 0x3 VHT80 = 0x4
5G CTL HT40/VHT40 frequency bin	ctlFreqbin5G_ HT40/VHT40	36	((Frequency_in_MHz – 4800)/5) 12 channels 3 domains (FCC, MKK, ETSI)	[3:0]	Frequency
5G CTL HT40/VHT40 data bin	ctlData5G_ HT40/VHT40	216	1 PWR VAL for frequency and mode 6 modes, 12 channels, 3 regulatory domains	[3:0]	dBm
5G CTL HT80/VHT80 index	ctlIndex5G_HT 80/VHT80	36	18 indices Each index includes 2 bytes 6 modes, 3 regulatory domains (FCC, MKK, ETSI).	[15:12]	SS mask Specify which spatial stream the CTL applies for 4 bit binary mask, with 1 bit for each of 4 stream combinations. More than 1 bit set means the CTL applies to each of the spatial stream rate groups which are set. 0001 = apply CTL power to all 1 spatial stream rates. 0010 = apply CTL power to all 2 spatial stream rates. 0100 = apply CTL power to all 3 spatial stream rates. 1000 = apply CTL power to all 4 spatial stream rates.
				[11:8]	Chain mask stream Specify which chain operating modes the CTL applies for. 4 bit binary mask, with 1 bit for each chain operating mode. More than 1 bit set means the CTL applies to each of the chain operation modes which are set. 0001 = apply CTL power when only 1 chain is transmitting. 0010 = apply CTL power when 2 chains are transmitting. 0100 = apply CTL power when 3 chains are transmitting. 1000 = apply CTL power when 4 chains are transmitting.
				[7:4]	REG DOMN
				3	BF

Structure description	Structure name/field name	Bytes	Structure detail/field description	Bits	Bit definition
				[0:2]	MODE 11b = 0x1 Legacy (11a or 11g) = 0x0 (V)HT20 = 0x2 (V)HT40 = 0x3 VHT80 = 0x4
5G CTL HT80/VHT80 frequency bin	ctlFreqbin5G_HT80/VHT80	18	((Frequency_in_MHz – 4800)/5) 6 channels 3 domains (FCC, MKK, ETSI)	[3:0]	Frequency
5G CTL VHT80 data bin	ctlData5G_VHT80	108	1 PWR VAL for frequency and mode 6 modes, 6 channels, 3 regulatory domains	[3:0]	dBm
5G CTL spare	ctlSpare5G	42	Reserved	[335:0]	Reserved

A.11 Rx gain calibration

Table A-11 rxGainCalCfg – Configuration for Rx Gain CAL

Field name	Bytes	Description	Bits	Bit definition
bandMask	1	Mask for 2G/5G	[7:0]	Value = FF enabled
refISS	1	Reference signal from tester	[7:0]	dBm
rate	1	Rate used for CAL	[7:0]	The rate used
bandWidth	1	BW used for CAL	[7:0]	20, 40, 80
numChan	1	Number of channels	[7:0]	–
numChain	1	Number of chains	[7:0]	–
numPkts	2	Number of packets	[15:0]	Packets used
chans	1*4	List of channels to be calibrated	[31:0]	List channels. If number of channels is 2, then the two channels are listed here.
chainMasks	1*4	List of chains to be calibrated	[31:0]	Same for chain masks
rxNFCalPowerDBr	1*4 (chain)*4 (Rx CAL channel)	Result NF for each chain in dBr	–	–
rxNFCalPowerDBm	1*4 (chain)*4 (Rx CAL channel)	Result NF for each chain in dBm	–	–
rxTempMeas	1*4 (chain)*4 (Rx CAL channel)	Measured temp for each chain during CAL	–	–
rxNFThermCalSlope	1*4 (chain)*4 (Rx CAL channel)	NF CAL slope for each chain	–	–
minCcaThreshold	1*4 (chain)*4 (Rx CAL channel)	Min CCA threshold for each chain	–	–

A.12 Calibration data per chip

Table A-12 Thermal fields

Field Name	Bytes	Description	Bits	Bit Definition
thermAdcScaledGain	2	Thermometer ADC scaled gain correction factor (unsigned) for chain 0	[15:9]	Reserved
			[8:0]	ADC scaled gain correction
thermAdcOffset	1	Thermometer ADC offset correction factor (signed) for chain 0	[7:0]	ADC offset correction
rbias	1	Reserved for analog rbias register setting value	[8:0]	Reserved
thermAdcScaledGain1	2	Thermometer ADC scaled gain correction factor (unsigned) for chain 1	[15:9]	Reserved
			[8:0]	ADC scaled gain correction
thermAdcOffset1	1	Thermometer ADC offset correction factor (signed) for chain1	[7:0]	ADC offset correction
ate_reserved1	1	Reserved	[7:0]	Reserved
thermAdcScaledGain2	2	Thermometer ADC scaled gain correction factor (unsigned) for chain 2	[15:9]	Reserved
			[8:0]	ADC scaled gain correction
thermAdcOffset2	1	Thermometer ADC offset correction factor (signed) for chain2	[7:0]	ADC offset correction
ate_reserved2	1	Reserved	[7:0]	Reserved
thermAdcScaledGain3	2	Thermometer ADC scaled gain correction factor (unsigned) for chain 3	[15:9]	Reserved
			[8:0]	ADC scaled gain correction
thermAdcOffset3	1	Thermometer ADC offset correction factor (signed) for chain 3	[7:0]	ADC offset correction
ate_reserved3	1	Reserved	[7:0]	Reserved
configFlag	1	Feature enable flag	[7:2]	Reserved
			[1]	Do not use this bit. It will be updated by otp.bin.
			[0]	1: Enable thermal Compensation
ate_reserved4	3	Reserved	[23:0]	Reserved
ateCALTemp	4	All ATE temp values (ATE_CAL_TEMP, CODE0, Code1)	[31:0]	This filed is valid when configFlag[0] = 1 OTP ATE DATA for chain 0-1.
ateCALTemp1	4	All ATE temp values (ATE_CAL_TEMP, CODE2, Code3)	[31:0]	This filed is valid when configFlag[0] = 1 OTP ATE DATA for chain 2-3.
Reserve	14	Reserved for future use	[111:0]	Value

Table A-13 ATE fields

Structure description	Field name	Bytes	Description	Bits	Bit definition
TPC attenuator ATE CAL	tpc_attenuatior	120	5 bits (step size) for each calibration point, 15 CAL points, internal/external coupler, 2 frequency bands, 2 chains 5*15*2*2*2 = 600 bits = 75 bytes To facilitate save/store, use 15*2*2*2 = 120 bytes.	[959:0]	Value
Reserved	Reserved	24	–	[192:0]	Value