

ISSUE TITLE	Improve RGMII timing and Electrical Characteristics			
SDK VERSION	4.2.0.0	CHIP	MT7621	Date 2013/12/25
Description: We found TRGMII mode cannot work properly in some situations. Please MUST change Linux setting from Turbo RGMII mode to RGMII mode. In addition, we have new RGMII setting to improve timing and electrical characteristics. Please apply below patch as well.				
How to Fix: 1. Change Linux setting from TRGMII to RGMII. <pre> <#> Ralink GMAC Network BottomHalves (Tasklet) ---> [] SKB Recycling [] Ralink Special Tag (0x810x) [] Jumbo Frame up to 4K bytes [*] TCP/UDP/IP checksum offload [] When TX ring is full, inform kernel stop transmit and stop RX handler [] 32 bytes TX/RX description [*] LRO (Large Receive Offload) [] Transmit VLAN HW (DoubleVLAN is not supported) [] Receive VLAN HW (DoubleVLAN is not supported) [*] TSOV4 (Tcp Segmentaton Offload) [] TSOV6 (Tcp Segmentaton Offload) [*] Choose QDMA instead of DMA GMAC is connected to (RGMII_FORCE_1000 (GigaSW, CPU)) ---> -* Ralink Embedded Switch -* LAN/WAN Partition Switch Board Layout Type (LLLL/W) ---> [*] GMAC2 Support GMAC2 is connected to (Internal GigaPHY) ---> </pre>				

2. Modify RT288x_SDK/source/linux-2.6.36.x/drivers/net/raeth/raether.c

```
void setup_internal_gsw(void)
```

```
{
```

```
.....
```

```
#if defined (CONFIG_GE1_TRGMII_FORCE_1200) && defined (CONFIG_MT7621_ASIC)
```

```
    mii_mgr_write(0, 14, 0x3); /*TRGMII*/
```

```
#else
```

```
    mii_mgr_write(0, 14, 0x1); /*RGMII*/
```

```
    /* set MT7530 central align */
```

```
    mii_mgr_read(31, 0x7830, &regValue);
```

```
    regValue &= ~1;
```

```
    regValue |= 1<<1;
```

```
    mii_mgr_write(31, 0x7830, regValue);
```

```
    mii_mgr_read(31, 0x7a40, &regValue);
```

```
    regValue &= ~(1<<30);
```

```
    mii_mgr_write(31, 0x7a40, regValue);
```

```
    regValue = 0x855;
```

```
    mii_mgr_write(31, 0x7a78, regValue);
```

```
.....
```

```
}
```

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