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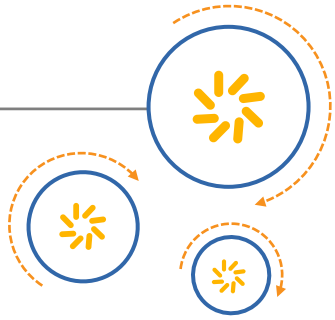

QCA9981 Single-Band 4x4 with 4 SS MIMO 802.11ac/bgn WLAN SoC

Device Specification

80-Y2314-3 Rev. A

March 2015

Qualcomm Atheros, Inc.
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San Jose, CA 95110
U.S.A.

Revision history

Revision	Date	Description
A	March 2015	Initial version

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1 Introduction

1.1 General description

The QCA9981 with Qualcomm® VIVE™ 802.11ac technology is a highly integrated wireless local area network (WLAN) system-on-chip (SoC) for 2.4 GHz 802.11ac or 2.4 GHz 802.11n WLAN applications. The QCA9981 includes a CPU and memory for WLAN media access layer (MAC) and physical layer (PHY) management and provides host offload of other high-level networking tasks. It enables high-performance 4x4 MIMO with four spatial streams for wireless applications demanding the highest robust link quality and maximum throughput and range. The QCA9981 integrates a multi-protocol MAC, PHY, analog-to-digital/digital-to-analog converters (ADC/DAC), 4x4 MIMO radio transceivers, and PCIE interface in an all-CMOS device for low power consumption and small form-factor applications.

The QCA9981 implements half-duplex OFDM, CCK, and DSSS PHY, supporting 800 Mbps for 802.11ac 40 MHz channel operation. It supports 802.11n up to 288.9 Mbps for 20 MHz and 600 Mbps for 40 MHz channel operations, and IEEE 802.11b/g/n/ac data rates. Additional features include 802.11ac explicit transmit beamforming (TxBF), 802.11 compatible implicit TxBF, multi-user MIMO (MU-MIMO), Maximal Likelihood (ML) decoding, Low-Density Parity Check (LDPC), Maximal Ratio Combining (MRC), Space Time Block Code (STBC), and On-Chip One-Time Programmable (OTP) memory to eliminate the need for an external flash and to further reduce the external component count and BOM cost with integrated power management. The QCA9981 supports 802.11 wireless MAC protocol, 802.11i security, Wi-Fi offload, error recovery, and 802.11e quality of service (QoS).

The QCA9981 supports up to four simultaneous spatial streams integrating four Tx and four Rx chains for high throughput and extended coverage. Tx chains combine PHY in-phase (I) and quadrature (Q) signals, convert them to the desired frequency, and drive the RF signal through external power amplifiers (PAs). Rx chains receive from antennas through external LNAs. The frequency synthesizer supports 1-MHz steps to match frequencies defined by IEEE 802.11b/g/n specifications. The QCA9981 supports frame data transfer to and from the host using a PCIE interface that supports interrupt generation and reporting and status reporting. Other external interfaces include EEPROM and GPIOs.

1.2 Features

General

- 4x4 SU-/MU-MIMO technology improves effective throughput and range over existing 802.11b/g products
- Support for up to four spatial streams
- Optional integrated voltage regulator
- Support for 48-MHz crystal
- 156-pin, 12 mm x 12 mm DRQFN package

WLAN

- Supports 20/40 MHz at 2.4 GHz
- Supports up to 256 QAM
- Data rates of up to 800 Mbps in 802.11ac 40 MHz channels using reduced (short) guard interval (GI)
- Data rates of up to 288.9 Mbps for 20 MHz channels and 600 Mbps for 40 MHz channels in 802.11n using short GI
- Multi-user MIMO (MU-MIMO) beamformer
- Explicit transmit beamforming (TxBF) and legacy implicit TxBF for both beamformer and beamformee
- TCP and UDP checksum offload
- Maximal likelihood (ML) decoding
- Supports spatial multiplexing, cyclic-delay diversity (CDD), low-density parity check (LDPC), maximal ratio combining (MRC), Space Time Block Code (STBC)
- AMSDU and AMPDU frame aggregation
- 802.11e-compatible bursting
- Digital predistortion
- Support for locationing (RSSI and RTT-based, 802.11REVmc compliant)

Supported Standards

- 802.11b/g/n
- Support for IEEE 802.11d, e, h, i, j, k, r, u, v time stamp, w, and z standards

CPU/Memory

- Integrated CPU for Wi-Fi offload with memory
- On-chip OTP memory

RF

- Support for external PA
- Support for external LNA

Security

- AES-CCMP at 128/256 bits
- AES-GCMP at 128/256 bits
- WEP, TKIP hardware encryption
- WAPI hardware encryption

Interfaces

- PCI Express 2.0 interface
- I^2C EEPROM support
- GPIOs
- JTAG for debugging and boundary scan
- MIPI RFFE

1.3 High-level system diagram

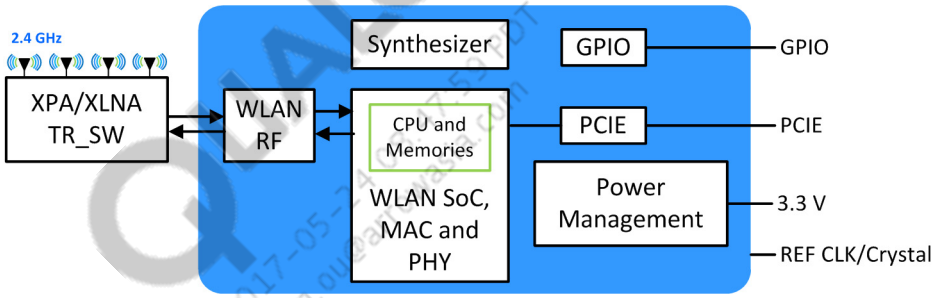


Figure 1-1 QCA9981 block diagram

1.4 Functional Specification

1.4.1 Functional block diagram

Figure 1-2 illustrates the QCA9981 functional block diagram.

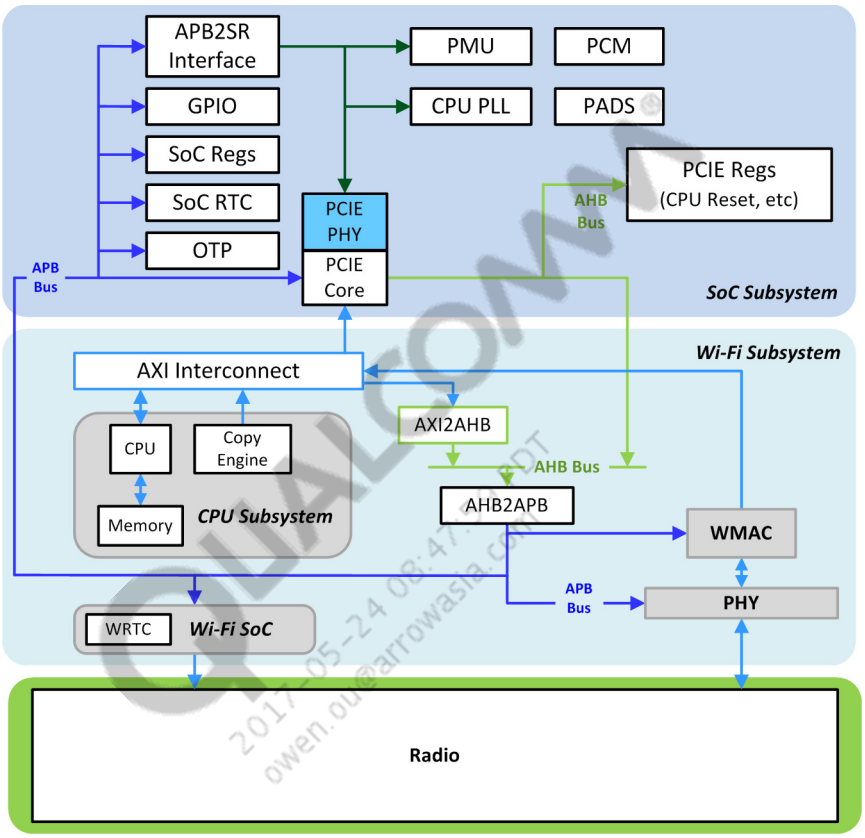


Figure 1-2 QCA9981 functional block diagram

The QCA9981 is comprised of several internal functional blocks, as summarized in Table 1-1.

Table 1-1 Functional blocks

Block	Description
GPIOs	All digital pins map to 35 GPIOs. These GPIOs are used for a variety of purposes such as UART, I^2C, SPI, JTAG. See GPIO.
OTP	WLAN one-time programmable (OTP) memory
WRTC	Controls the clocks and power going to other modules within the chip. Its inputs consist of sleep requests from these modules and its outputs consists of clock enable signals used to gate the clocks going to these modules. This block also manages resets going to other modules within the device.

Table 1-1 Functional blocks (cont.)

Block	Description
AXI Interconnect	The AXI bus is accessed simultaneously by multiple masters in the PCIE host memory, CPU memory, and all programmable registers. The WLAN portion of the AXI fabric supports split transactions to achieve higher utilization on the PCIE bus. All register access from the CPU route through the AXI fabric. A bridge converts AXI requests to AHB requests, and the AHB arbiter selects between PCIE register access requests and CPU register access requests on a round-robin basis. All register accesses for all modules including the MAC, CE, and blocks such as GPIOs, RTC, or OTP use the APB protocol. A bridge converts AHB requests into APB. It must be noted here that the entire AXI fabric, AHB, and APB interfaces all run synchronously on the SoC clock domain. See GPIO.
Copy Engine	The copy engine establishes a communication channel between firmware and the host. It performs a DMA copy from source memory to destination memory, and it can perform this DMA copy operation in a batch under software control. A copy involves a read operation from the source memory, followed by a write operation to the destination memory.
CPU Core and Memory Controller	The CPU is a Tensilica XTENSA 7.0 processor with a hardware abstraction layer (HAL) to support low level WLAN activity with minimal support from the PCIE host. The CPU is configured with a peripheral interface (PIF). The outbound PIF is used by the CPU for register access. The inbound PIF is used by the other AXI masters (MAC and CE) to access the data memory (DMEM) connected to the CPU.
WMAC/PHY/Radio	The integrated 2.4 GHz 802.11ac MAC/PHY/radio includes the features of maximal likelihood (ML) decoding, low-density parity check (LDPC), and maximal ratio combining (MRC). The MAC supports A-MSDU scatter and gather, L2 header encapsulation and decapsulation, IP/TCP/UDP checksum, and Rx classification.
PCIE Registers	The QCA9981 PCIE configuration space also maps to the host memory space. Most programmable registers can be accessed either by the host over PCIE or by the internal CPU over AHB. Some additional registers are accessible only by the host over PCIE. These registers run on the PCIE clock domain, allowing the PCIE host to determine the sleep status of the SoC and to wake up the SoC if needed.
PCIE Core/ PCIE PHY	All programmable registers can be accessed by either the PCIE host or by the internal CPU. The PCIE core provides a simple proprietary interface for register accesses.

1.4.2 GPIO

The QCA9981 provides 35 configurable bi-directional general purpose I/O ports and 3 configurable input-only ports. Each GPIO port can be configured independently as input or output using the GPIO control registers. The GPI/GPIOs are used for a variety of purposes such as UART, I^2C, SPI, JTAG, and so on.

Most GPIOs have normal mode functionality as well as test-mode functionality. GPIO mapping is shown in Table 1-2. On reset bootstrap values are sampled. Global test mode is on GPIO_30. If this pin is sampled high during initialization, the chip enters test mode.

Table 1-2 GPIO

Pin	Name	Functional Alternate	Description
B12	**GPIO_0**	SWCOM2	External antenna select
A14	**GPIO_1**	SWCOM3	External antenna select
A15	**GPIO_2**	SWCOM0	External Tx/Rx switch control
B14	**GPIO_3**	SWCOM1	External Tx/Rx switch control
A16	**GPIO_4**	SWCOM4	External antenna select
A17	**GPIO_5**	SWCOM5	External antenna select
B16	**GPIO_6**	GPIO	General purpose I/O
A18	**GPIO_7**	GPIO	
B17	**GPIO_8**	GPIO	
A19	**GPIO_9**	GPIO	
A20	**GPIO_10**	GPIO	
B34	**GPIO_11**	GPIO	
A39	**GPIO_12**	GPIO	
B35	**GPIO_13**	GPIO	
A40	**GPIO_14**	GPIO	
A41	**GPIO_15**	GPIO	
B37	**GPIO_16**	GPIO	
A42	**GPIO_17**	GPIO	
A47	**GPIO_19**	EEPROM_PROT	EEPROM protection
B40	**GPIO_20**	I2C_SDA	I2C data
A48	**GPIO_21**	GPIO	General purpose I/O
A49	**GPIO_22**	I2C_CLK	I2C clock
B42	**GPIO_23**	GPIO	General purpose I/O
A50	**GPIO_24**	GPIO	
B43	**GPIO_25**	GPIO	
A51	**GPIO_26**	GPIO	
B44	**GPIO_27**	GPIO	
A52	**GPIO_28**	GPIO	
B45	**GPIO_29**	GPIO	
A53	**GPIO_30**	GPIO	
B47	**GPIO_31**	GPIO	
A55	**GPIO_32**	GPIO	
A56	**GPIO_33**	GPIO	
B49	**GPIO_34**	GPIO	

2 Pin Descriptions

This section contains both a package pinout and tabular listings of the signal descriptions.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
IO	A digital bidirectional signal
OA	An analog output signal
OD	An open-drain digital output signal
O	A digital output signal
P	A power or ground signal

Figure 2-1 shows the QCA9981 4×4 pinout.

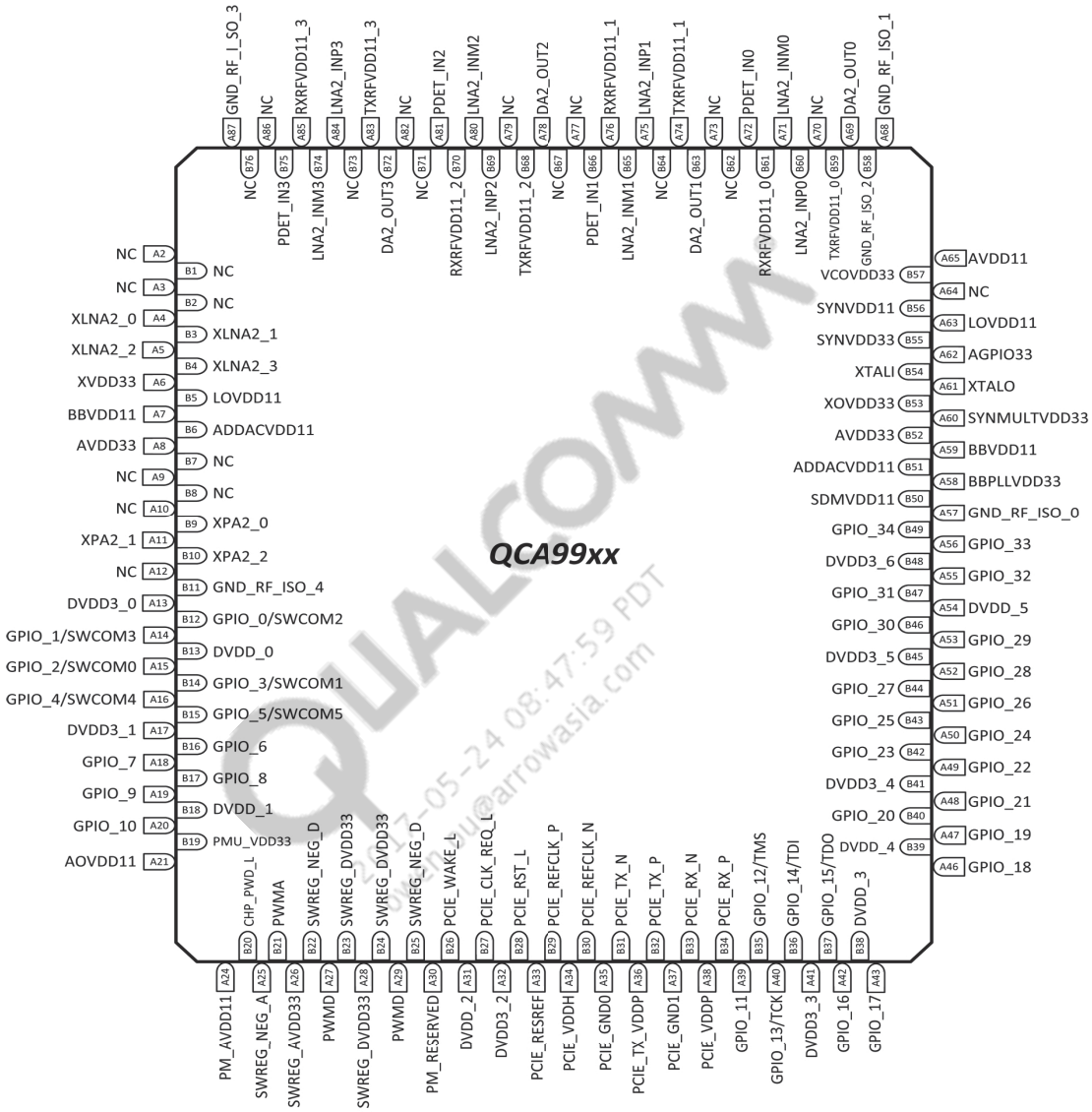


Figure 2-1 4×4 Package Pinout (See-Through Top View)

Table 2-1 provides the signal-to-pin relationship information for the QCA9981.

Table 2-1 Signal to Pin Relationships and Descriptions

Signal Name	Pins	Type	Description
Clock			
XTALI	B54	—	48 MHz crystal
XTALO	A61	—	
Radio			
LNA2_INM0	A71	IA	2 GHz LNA differential input pair for chain 0
LNA2_INP0	B60	IA	
LNA2_INM1	B65	IA	2 GHz LNA differential input pair for chain 1
LNA2_INP1	A75	IA	
LNA2_INM2	A80	IA	2 GHz LNA differential input pair for chain 2
LNA2_INP2	B69	IA	
LNA2_INM3	B74	IA	2 GHz LNA differential input pair for chain 3
LNA2_INP3	A84	IA	
DA2_OUT0	A69	OA	2 GHz DA single-ended output
DA2_OUT1	B63	OA	
DA2_OUT2	A78	OA	
DA2_OUT3	B72	OA	
PDET_IN0	A72	IA	PDET inputs for 2 GHz
PDET_IN1	B66	IA	
PDET_IN2	A81	IA	
PDET_IN3	B75	IA	
AGPIO33	A62	OA	3.3 V analog GPIO supply
Analog Interface			
XPA2_0	B9	OA	2.4 GHz external PA bias for 2.5 V to 3.3 V
XPA2_1	A11	OA	
XPA2_2	B10	OA	
XLNA2_0	A4	O	2.4 GHz external LNA control, 12 mA
XLNA2_1	B3	O	
XLNA2_2	A5	O	
PCI Express Endpoint			
PCIE_TX_N	B31	OA	Differential transmit
PCIE_TX_P	B32	OA	
PCIE_RX_N	B33	IA	Differential receive
PCIE_RX_P	B34	IA	
PCIE_REFCLK_N	B30	IA	Differential reference clock (100 MHz)
PCIE_REFCLK_P	B29	IA	
PCIE_RST_L	B28	I	PCIE reset
PCIE_RESREF	A33	—	PCIE reference resistor; attach a 200-Ω 1% 100-ppm/C precision resistor to ground on the board
PCIE_CLK_REQ_L	B27	OD	PCIE reference clock requests; open drain. An external pull up resistor to 3.3 V is required. Drive strength 16 mA.
PCIE_WAKE_L	B26	OD	PCIE request to service a function-initiated wake event; open drain. An external pull up resistor to 3.3 V is required. Drive strength 16 mA.

Table 2-2 External Switch Control/GPIO Pins

Signal Name	Pins	Type	Description
GPIO_0/SWCOM2	B12	IO	General purpose IO, programmable, can be used as JTAG, SPI, UARTs, LED control. ■ GPIO_0, GPIO_1, GPIO_2, GPIO_3, GPIO_4, and GPIO_5 are multiplexed pins that default to the antenna switch control (SWCOM) interface. ■ GPIO_0 through GPIO_5 use a 16 mA drive strength. ■ GPIO_6 through GPIO_34 use an 8 mA drive strength. Default input pins can be grounded, and default output pins can be left open if not used. See Table 1-2 on page 13.
GPIO_1/SWCOM3	A14	IO	
GPIO_2/SWCOM0	A15	IO	
GPIO_3/SWCOM1	B14	IO	
GPIO_4/SWCOM4	A16	IO	
GPIO_5/SWCOM5	B15	IO	
GPIO_6	B16	IO	
GPIO_7	A18	IO	
GPIO_8	B17	IO	
GPIO_9	A19	IO	
GPIO_10	A20	IO	
GPIO_11	A39	IO	
GPIO_12/TMS	B35	IO	
GPIO_13/TCK	A40	IO	
GPIO_14/TDI	B36	IO	
GPIO_15/TDO	B37	IO	
GPIO_16	A42	IO	
GPIO_17	A43	IO	
GPIO_18	A46	IO	
GPIO_19	A47	IO	
GPIO_20	B40	IO	
GPIO_21	A48	IO	
GPIO_22	A49	IO	
GPIO_23	B42	IO	
GPIO_24	A50	IO	
GPIO_25	B43	IO	
GPIO_26	A51	IO	
GPIO_27	B44	IO	
GPIO_28	A52	IO	
GPIO_29	A53	IO	
GPIO_30	B46	IO	
GPIO_31	B47	IO	
GPIO_32	A55	IO	
GPIO_33	A56	IO	
GPIO_34	B49	IO	

Table 2-3 Power and Ground Pins

Symbol	Pin	Description
Power		
DVDD_0	B13	1.1 V digital supply (from digital voltage regulator)[1]
DVDD_1	B18	
DVDD_2	A31	
DVDD_3	B38	
DVDD_4	B39	
DVDD_5	A54	
DVDD3_0	A13	3.3 V digital supply
DVDD3_1	A17	
DVDD3_2	A32	
DVDD3_3	A41	
DVDD3_4	B41	
DVDD3_5	B45	
DVDD3_6	B48	
NC	A64	No connect
PM_RESERVED	A30	Reserved. Leave floating.
RF Power		
AVDD11	A65	1.1 V analog supply (from analog voltage regulator)[1]
AVDD33	A8, B52	3.3 V analog supply
ADDACVDD11	B6, B51	1.1 V supply for ADC/DAC (from analog voltage regulator)
BBVDD11	A7, A59	1.1 V supply Tx/Rx BB FLTs (from analog voltage regulator)
BBPLLVDD33	A58	3.3 V supply for BB PLL
XVDD33	A6	3.3 V supply for xLNA and xPA
LOVDD11	A63, B5	1.1 V supply for LO (from analog voltage regulator)
RXRFVDD11_0	B61	1.1 V supply for Rx RF (from analog voltage regulator)
RXRFVDD11_1	A76	
RXRFVDD11_2	B70	
RXRFVDD11_3	A85	
TXRFVDD11_0	B59	1.1 V supply for Tx RF (from analog voltage regulator)
TXRFVDD11_1	A74	
TXRFVDD11_2	B68	
TXRFVDD11_3	A83	
SDMVDD11	B50	1.1 V supply for synth SDM (from analog voltage regulator)
SYNVDD11	B56	1.1 V supply for synth (from analog voltage regulator)
SYNMULTVDD33	A60	3.3 V supply for synth reference clock
SYNVDD33	B55	3.3 V supply for synth
VCOVDD33	B57	3.3 V VCO regulator
XOVDD33	B53	3.3 V supply for XO

Table 2-3 Power and Ground Pins (cont.)

Symbol	Pin	Description	
PCIE Power			
PCIE_TX_VDDP	A36	1.1 V supply for PCIE PHY Tx (from digital voltage regulator)	
PCIE_VDDP	A38	1.1 V supply for PCIE PHY (from digital voltage regulator)	
PCIE_VDDH	A34	3.3 V supply for PCIE PHY high voltage	
PCIE_GND0	A35	PCIE ground	
PCIE_GND1	A37		
Internal Voltage Regulators			
		When using internal regulator...[2]	**When using external regulator...**
CHP_PWD_L	B20	Chip power down control. Must be de-asserted after 3.3 V power becomes stable.	Must be de-asserted after both 3.3 V power and 1.1 V power become stable. See Section 3.7 for example circuit.
PMU_VDD33	B19	3.3 V supply for PMU.	
SWREG_AVDD33	A26	3.3 V power input to the analog voltage regulator	Should be connected to GND. Use firmware that disables the internal regulators.
SWREG_DVDD33	A28, B23, B24	3.3 V power input to the digital voltage regulator	
SWREG_NEG_A	A25	Analog voltage regulator ground	
SWREG_NEG_D	B22, B25	Digital voltage regulator ground	
AOVDD11	A21	Decoupling capacitor for internal LDO regulator.	
PM_AVDD11	A24	Feedback from the analog voltage regulator.	Connect to 1.1 V rail
PWMA	B21	Analog voltage regulator switching output.	Leave floating.
PWMD	A27, A29	Digital voltage regulator switching output.	Leave floating.
Ground Pad			
GND_RF_ISO_0	A57	GND pins, connected to the PCB ground	
GND_RF_ISO_1	A68		
GND_RF_ISO_2	B58		
GND_RF_ISO_3	A87		
GND_RF_ISO_4	B11		
Exposed Ground Pad	—	Tied to GND; see "Device Physical Dimensions" on page 27	
NC	A2, A3, A9, A10, A12, A70, A73, A77, A79, A82, A86, B1, B2, B7, B8, B62, B64, B67, B71, B73, B76	No connection	

1. When using an external regulator, both AVDD_n and DVDD11 must be powered from a single regulator. Minimum current rating of regulator is 3.5 A (2.5 A digital + 1 A analog). External regulator tolerance requirement is +5%/-3%.
2. The internal regulator is not supported in the QCA9981.

3 Electrical Characteristics

3.1 Absolute maximum ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the QCA9981.

Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document is not recommended.

Table 3-1 Absolute maximum ratings

Symbol	Parameter		Max Rating	Unit
DVDD_*,	Supply from external digital regulator voltage		-0.3 to 1.21	V
AVDD11, ADDACVDD11, BBVDD11, LOVDD11, RFRXVDD11_*, TXRFVDD11_*, SDMVDD11, SYNVDD11	Supply from external analog regulator voltage			
PCIE_TX_VDDP	PCIE PHY Tx supply			
PCIE_VDDP	PCIE PHY supply			
PMU_VDD33	Maximum supply for PMU		-0.3 to 3.63	V
DVDD3_*	Digital I/O voltage			
AVDD33, AGPIO33, BBPLLVDD33, SYNMULTIVDD33, SYNVDD33, XVDD33, XOVDD33, VCOVDD33	Analog I/O voltage			
PCIE_VDDH	PCIE PHY I/O			
RF_{in}	Maximum RF input (reference to 50 Ω)		0	dBm
T_{store}	Storage temperature		-45 to 135	°C
T_j	Junction temperature		125	°C
ESD	Electrostatic discharge tolerance	HBM	2000	V
		CDM	500	

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DVDD_*,	Supply from external digital regulator voltage	—	—	1.1	—	V
AVDD11, ADDACVDD11, BBVDD11, LOVDD11, RFRXVDD11_*, TXRFVDD11_*, SDMVDD11, SYNVDD11	Supply from external analog regulator voltage	+5/-3%	1.067	1.1	1.155	V
DVDD3_*	Digital I/O voltage	±5%	3.135	3.3	3.465	V
AVDD33, AGPIO33, BBPLLVDD33, SYNMULTIVDD33, SYNVDD33, XVDD33, XOVDD33, VCOVDD33	Analog I/O voltage	±5%	3.135	3.3	3.465	V
PCIE_VDDH	PCIE PHY I/O supply	±5%	3.135	3.3	3.465	V
PCIE_TX_VDDP	PCIE PHY Tx supply	+5/-3%	1.067	1.1	1.155	V
PCIE_VDDP	PCIE PHY supply	+5/-3%	1.067	1.1	1.155	V
T_{case}	Case temperature	—	0	—	110	°C

3.3 48-MHz clock characteristics

A 48-MHz crystal with accuracy ±20 ppm may be used; for 5 MHz operation, ±10 ppm is required.

Table 3-3 Reference requirements for 48 MHz crystal

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency	—	—	48	—	MHz
Frequency trimming	—	-10	—	10	PPM
Duty cycle of output signal	—	48	—	52	%
Voltage swing	—	0.8	—	1.5	Vpp
Settling time	—	—	—	1	ms
Output phase noise (48 MHz)	*f* = 1 KHz	—	-123.5	-121.5	dBc/Hz
	f = 10 KHz	—	-145.5	-143.5	dBc/Hz
	f = 100 KHz	—	-156.5	-154.5	dBc/Hz
	f = 1000 KHz	—	-157.5	-155.5	dBc/Hz
Output harmonic spur	—	—	—	-40	dBc
Mode of vibration	—	Fundamental			

3.4 GPIO DC electrical characteristics

Table 3-4 lists the GPIO DC electrical characteristics, with:

$T_a = 25$ °C

Table 3-4 GPIO DC electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	0.7 * V_{DD33}	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	0.3 * V_{DD33}	V
V_{OH}	High Level Output Voltage	—	0.9 * V_{DD33}	—	—	V
V_{OL}	Low Level Output Voltage	—	0	—	0.1 * V_{DD33}	V

3.5 Power up sequencing

Figure 3-1 depicts the required reset sequence for the QCA9981 PCIE interface. Table 3-5 shows the QCA9981 PCIE interface timing parameters.

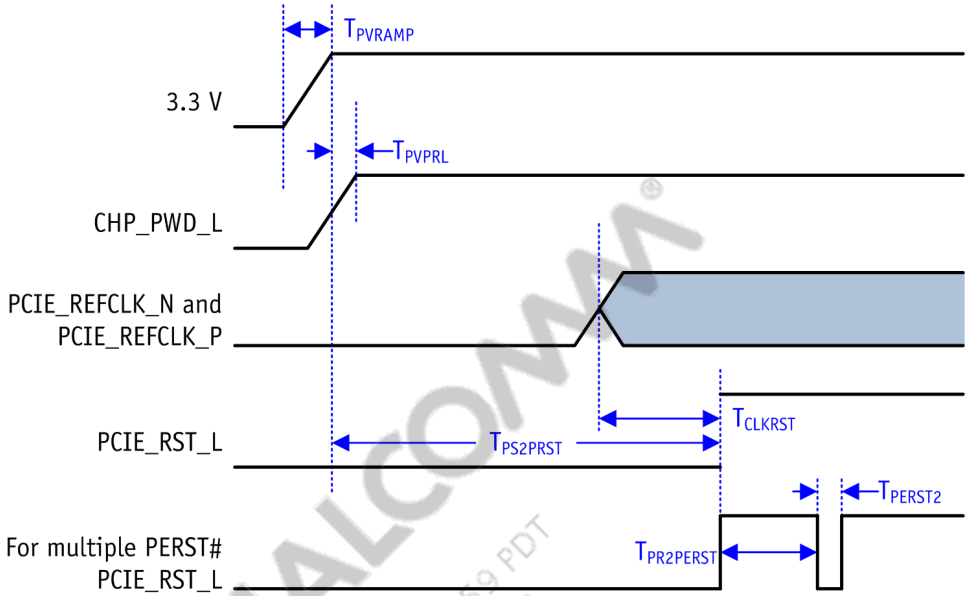


Figure 3-1 QCA9981 power up sequencing

Table 3-5 PCIE interface timing parameters

Symbol	Parameter	Min	Max	Unit
T_{PVRAMP}	Power supply ramp on 3.3 V	—	25	ms
T_{PVPRL}	Power valid to RESET_L asserted	0[1]	—	µs
T_{PRCLK}	RESET_L deasserted to PCIE_REFCLK_N and PCIE_REFCLK_P stable	100	—	µs
T_{CLKRST}	PCIE_REFCLK_N and PCIE_REFCLK_P stable to PCIE_RST_L deasserted	100[2]	—	µs
$T_{PS2PRST}$	Power supply stable to PCIE_RST_L deassert	10[3]	—	ms
$T_{PR2PERST}$	Initial PCIE_RST_L deassert to subsequent multiple PCIE_RST_L	40	—	ms
T_{PERST2}	Subsequent PCIE_RST_L asserted for multiple PCIE_RST_L	1	—	ms

1. When using an external voltage regulator, CHP_PWD_L must be de-asserted after both 3.3 V power and 1.1 V power have become stable. See Section 3.7 for an example RC circuit that controls the de-assertion of CHP_PWD_L.
2. This timing depends on hardware interface designs, such as Express Card, PCIE Mini Card, or PCIE desktop applications. The system must follow PCIE specifications, as well as TCLKRST.
3. $T_{PS2PRST}$ minimum timing must be observed.

3.6 Internal voltage regulators

NOTE The internal regulator (internal PMU) is not supported in the QCA9981.

Refer to the *QCA99xx Device Revision Guide* (80-Y8049-1) for additional information.

3.7 External voltage regulator

The 1.1 V power can be derived from the 3.3 V supply by an external regulator. Figure 3-2 shows circuitry for an external regulator. Refer to *QCA99xx Designs – External Regulator Application Note* (80-Y8050-26) for details.

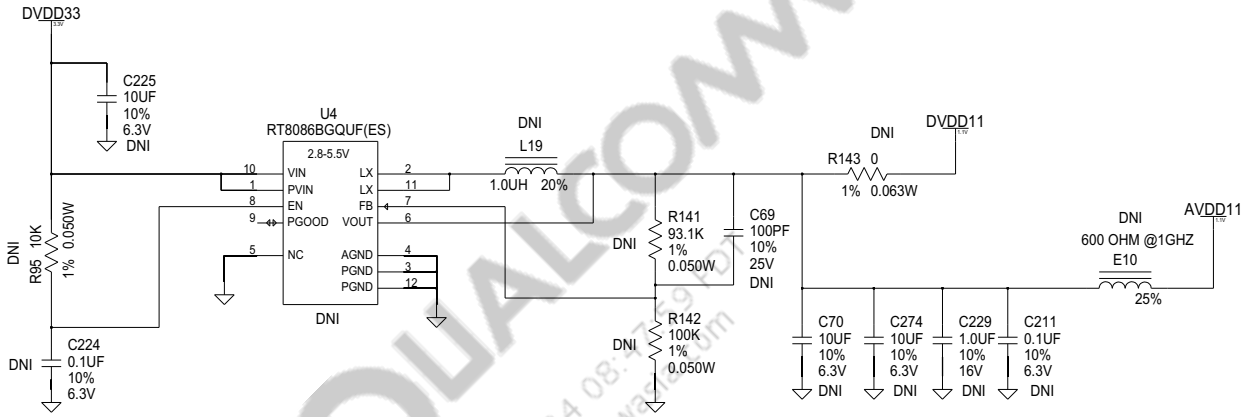


Figure 3-2 External 3.3 V to 1.1 V regulator

In addition to the external regulator, CHP_PWD_L should be de-asserted after 3.3 V power and 1.1 V power have become stable. Figure 3-3 shows an example RC circuit that could be used to control when CHP_PWD_L is de-asserted.

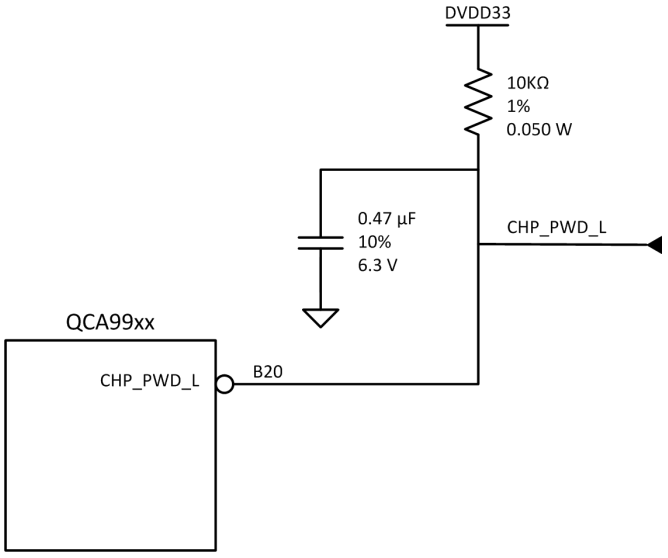


Figure 3-3 RC circuit on CHP_PWD_L

3.8 Radio characteristics

These conditions apply to the typical per chain characteristics unless otherwise specified:

RF V_{DD11} Group [1] = 1.1 V
V_{DD33} = 3.3 V, T_a = 25 °C

3.8.1 Rx characteristics

This section shows the QCA9981 receiver characteristics.

Table 3-6 Rx characteristics for 2.4 GHz operation

Symbol	Parameter			Min	Typ	Max	Unit	Conditions
Frx	Receive input frequency range			2.412	—	2.484	GHz	5 MHz center frequency
Sensitivity								
Srf (CCK)	CCK	1 Rx Chain	1 Mbps	—	-98	—	dBm	See Note 1
			11 Mbps	—	-83	—		
	CCK	3 Rx Chains	1 Mbps	—	-102	—	dBm	
			11 Mbps	—	-94	—		
Srf (OFDM)	OFDM	1 Rx Chain	6 Mbps	—	-92.5	—	dBm	See Note 1
			54 Mbps	—	-75	—		
	OFDM	3 Rx Chains	6 Mbps	—	-96.5	—	dBm	
			54 Mbps	—	-80.5	—		
Srf (802.11n)	802.11n HT20	1 Stream (1x1)	MCS0	—	-92	—	dBm	—
			MCS8	—	-73.5	—		
	802.11n HT20	3 Streams (3x3)	MCS0	—	-92	—	dBm	
			MCS8	—	-75	—		
	802.11n HT40	1 Stream (1x1)	MCS0	—	-89.5	—	dBm	—
			MCS7	—	-71	—		
	802.11n HT40	3 Streams (3x3)	MCS0	—	-92	—	dBm	
			MCS23	—	-75	—		
Z_{RFin_input}	Recommended LNA differential drive impedance			—	2450 MHz Impedance 167-163j	—	Ω	Ch 0, Ch 1, Ch 2, Ch 3
Adjacent channel rejection								
R_{adj}	CCK			35	41.5	—	dB	See Note 2
	OFDM		6 Mbps	16	32.5	—		
			54 Mbps	-1	27	—		
	HT20		MCS0	16	31	—		
			MCS23	-2	13	—		
	HT40		MCS0	16	25	—		
			MCS23	-2	2	—		

1. Measured with reference design CUS260 at RF input with NF = 5.0 dB.
2. Minimum values based on IEEE 802.11 requirements.
   Tested with chain mask 15.
   Additional ±1.5 dB board-to-board variation must be accounted.

1. RF VDD11 Group = Pins A7, A59, A63, A65, A74, A76, A83, A85, B5, B6, B50, B51, B55, B59, B61, B68, B70

3.8.2 Tx Characteristics

See Table 3-7 for the QCA9981 transmitter characteristics.

Table 3-7 Tx chain characteristics for 2.4 GHz operation at chip output with external PA

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
F_{tx}	Transmit output frequency range		2.412	—	2.484	GHz	5 MHz center freq
P_{out}	Mask compliant output power						
	1 Mbps		—	-3	—	dBm	See Note 2
	6 Mbps		—	-3	—		
	HT20, MCS0		—	-3	—		
	HT40, MCS0		—	-3	—		
EVM (Header Only)[1]			**Tx Power (dBm)[2]:**				
	802.11ac, HT20 (Per Tx chain)	MCS8	—	-39.2	—	dB	—
	802.11ac, HT40 (Per Tx chain)	MCS9	—	-38.9	—	dB	—
SP_{gain}	Tx gain step		—	0.5	—	dB	See Note 3
A_{pl}	Accuracy of power control loop		—	±1	—	dB	See Note 4
Z_{RFout_load}	Recommended PA single-ended load impedance		—	50	—	Ω	—

1. Measured with CUS260.
2. Simulated at the chip output
3. Guaranteed by design.
4. Manufacturing calibration required.

3.9 Power consumption

This section shows the typical power consumption with external PMU as a function of the QCA9981's operating mode.

Table 3-8 802.11ac Power Consumption for 2.4 GHz (HT20)[1]

Mode	DVDD33 (mA)	AVDD33 (mA)	AVDD11 (mA)	DVDD11 (mA)	Power Consumption (mW)
Rx (Four-Chain) MCS0	15	58	249	409	965
Rx (Four-Chain) MCS8	25	56	241	506	1089
Tx (Four-Chain) MCS0	15	89	562	372	1371

1. Measured with CUS260 reference design

Table 3-9 802.11ac Power Consumption for 2.4 GHz (HT40)[1]

Mode	DVDD33 (mA)	AVDD33 (mA)	AVDD11 (mA)	DVDD11 (mA)	Power Consumption (mW)
Rx (Four-Chain) MCS0	15	57	249	653	1230
Rx (Four-Chain) MCS9	34	58	254	776	1436
Tx (Four-Chain) MCS0	15	85	583	425	1439

1. Measured with CUS260 reference design

4 Mechanical Information

The QCA9981 uses a 156-pin, dual-row, quad flat, no-leads (DRQFN) package

4.1 Device Physical Dimensions

The QCA9981 DRQFN-156 package drawings and dimensions are provided in Figure 4-1 and Figure 4-2, and in Table 4-1 and Table 4-2.

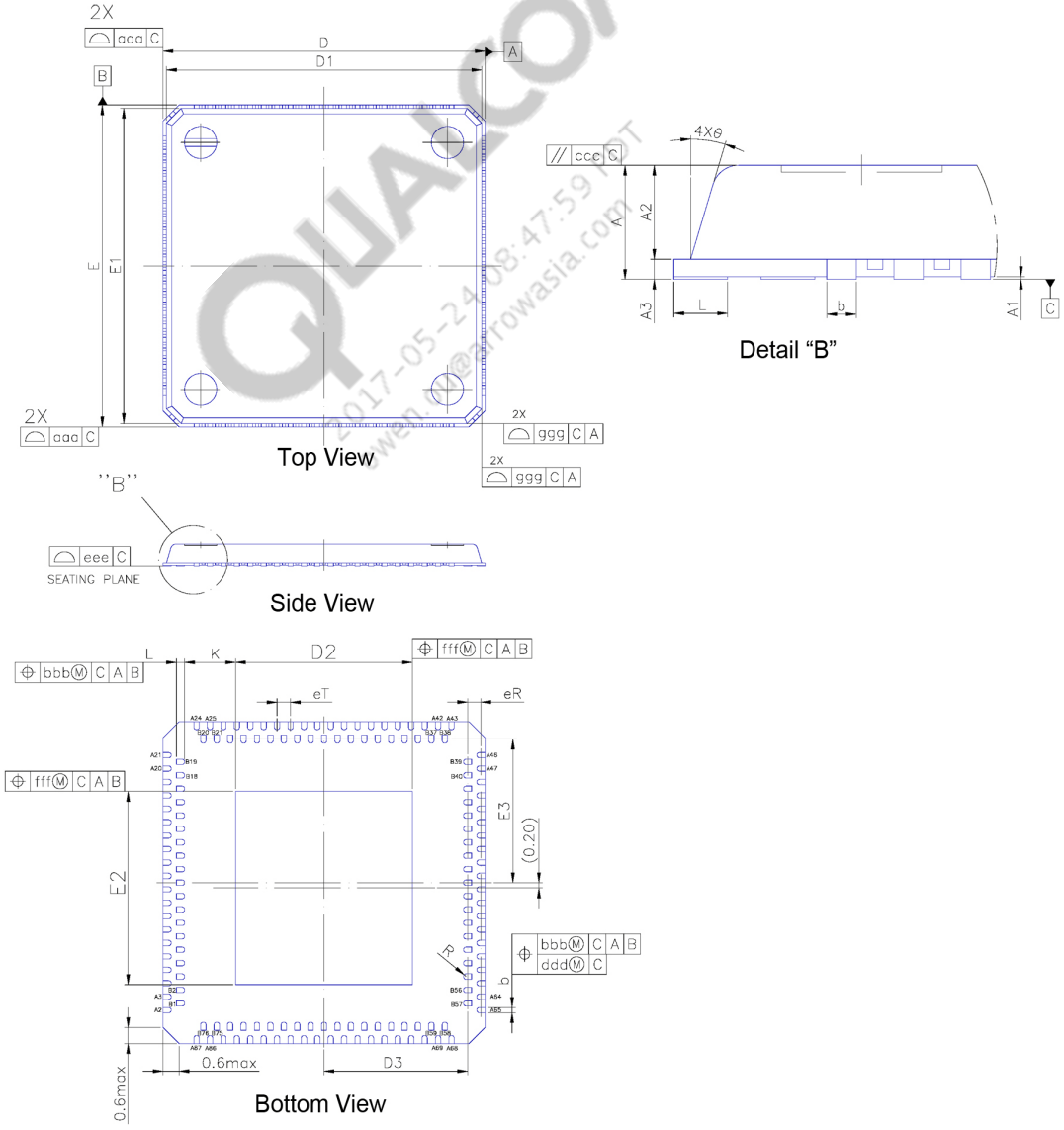


Figure 4-1 QCA9981 package A details

Table 4-1 Package A Dimensions

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm	0.031	0.033	0.035	inches
A1	0.00	0.02	0.05	mm	0.000	0.001	0.002	inches
A2	0.65	0.70	0.75	mm	0.026	0.028	0.030	inches
A3		0.15 REF		mm		0.006 REF		inches
b	0.15	0.20	0.25	mm	0.006	0.008	0.010	inches
D/E	11.90	12.00	12.10	mm	0.469	0.472	0.476	inches
D1/E1		11.75 BSC		mm		0.463 BSC		inches
D2	6.50	6.60	6.70	mm	0.256	0.260	0.264	inches
E2	7.10	7.20	7.30	mm	0.280	0.283	0.287	inches
D3/E3		5.35 BSC		mm		0.211 BSC		inches
eT		0.50 BSC		mm		0.020 BSC		inches
eR		0.50 BSC		mm		0.020 BSC		inches
L	0.20	0.30	0.40	mm	0.008	0.012	0.016	inches
θ	5°	—	15°	degrees	5°	—	15°	degrees
K	0.20	—	—	mm	0.008	—	—	inches
R	0.075	—	0.125	mm	0.003	—	0.005	inches
aaa		0.10		mm		0.004		inches
bbb		0.10		mm		0.004		inches
ccc		0.10		mm		0.004		inches
ddd		0.05		mm		0.002		inches
eee		0.08		mm		0.003		inches
fff		0.10		mm		0.004		inches
ggg		0.20		mm		0.008		inches
Controlling dimension: Millimeters								

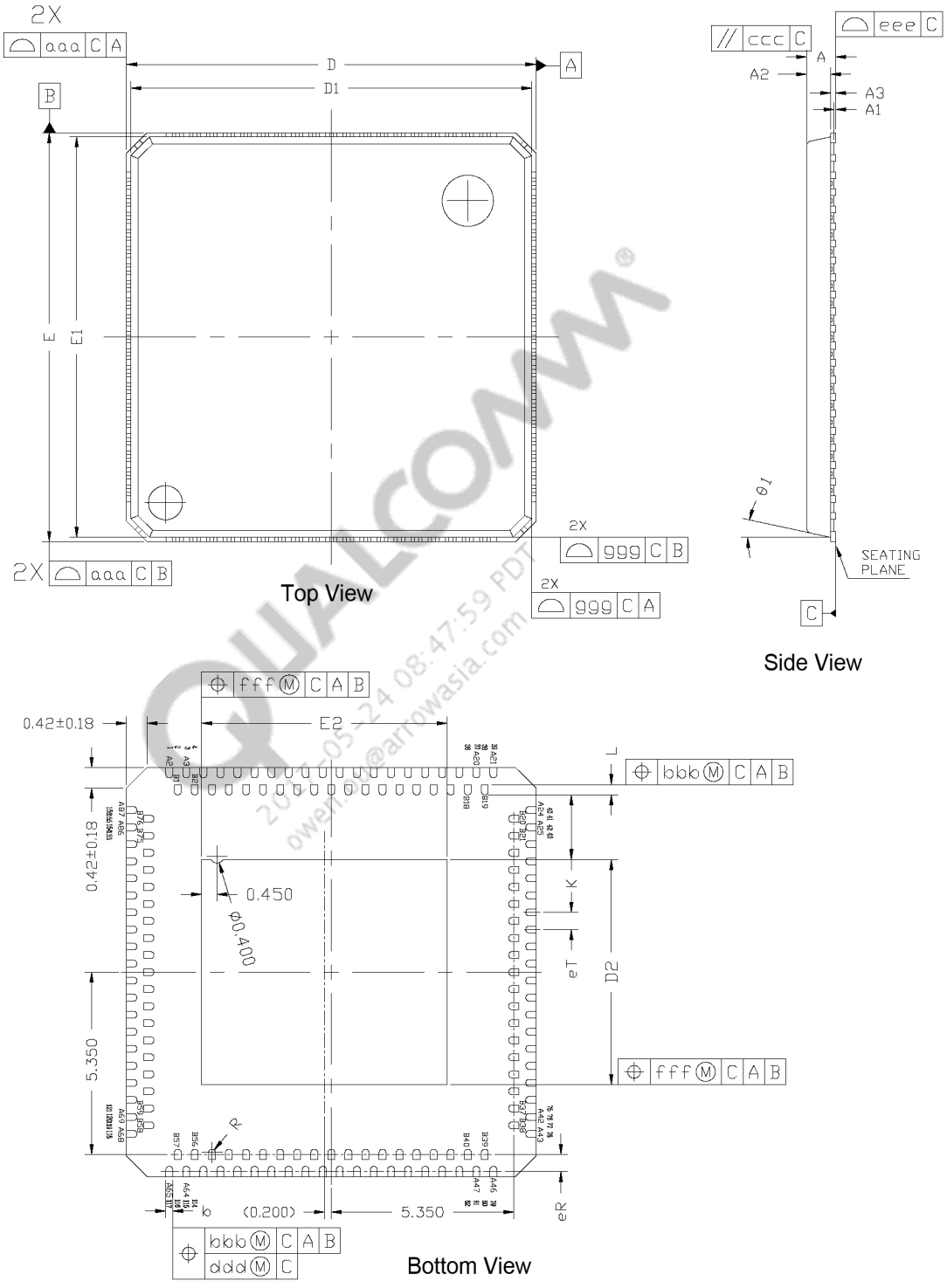


Figure 4-2 QCA9981 package B details

Table 4-2 Package B Dimensions

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm	0.031	0.033	0.035	inches
A1	0.00	0.02	0.05	mm	0.000	0.001	0.002	inches
A2	0.65	0.70	0.75	mm	0.026	0.028	0.030	inches
A3		0.15 REF		mm		0.006 REF		inches
b	0.15	0.20	0.25	mm	0.006	0.008	0.010	inches
D/E		12 BSC		mm		0.472 BSC		inches
D1/E1		11.75 BSC		mm		0.463 BSC		inches
D2	6.50	6.60	6.70	mm	0.256	0.260	0.264	inches
E2	7.10	7.20	7.30	mm	0.280	0.283	0.287	inches
eT		0.50 BSC		mm		0.020 BSC		inches
eR		0.50 BSC		mm		0.020 BSC		inches
L	0.20	0.30	0.40	mm	0.008	0.012	0.016	inches
θ	5°	—	15°	degrees	5°	—	15°	degrees
R	0.075	—	0.125	mm	0.003	—	0.005	inches
aaa		0.10		mm		0.004		inches
bbb		0.10		mm		0.004		inches
ccc		0.10		mm		0.004		inches
ddd		0.05		mm		0.002		inches
eee		0.08		mm		0.003		inches
fff		0.10		mm		0.004		inches
ggg		0.20		mm		0.008		inches
Controlling dimension: Millimeters								

4.2 Part marking

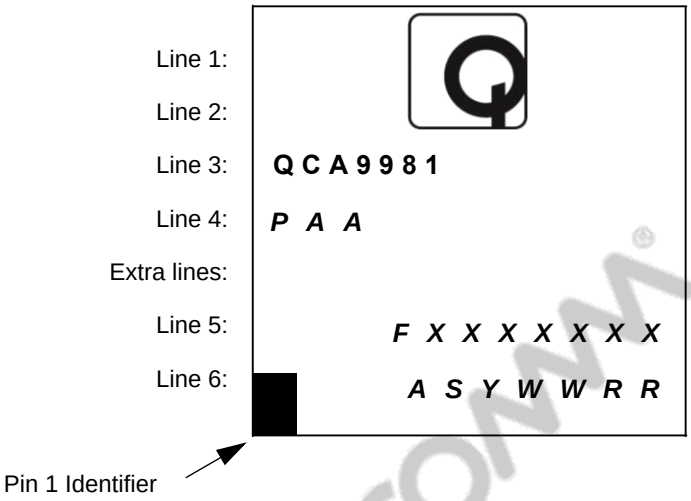


Figure 4-3 QCA9981 marking (top view, not to scale)

Table 4-3 QCA9981 marking line definitions

Line	Marking	Description
1 and 2	QUALCOMM	Qualcomm name or logo
3	QCA9981	Qualcomm product name
4	*PAA*	P = product configuration code AA = product feature code
5	*FXXXXXXX*	F = fab code XXXXXXX = wafer lot ID
6	*ASYWWRR*	A = assembly site code S = assembly sequence number Y = single, last digit of year WW = work week (based on calendar year) RR = product revision
Additional lines may appear on the part marking for some samples; this is manufacturing information that is only relevant to Qualcomm and Qualcomm suppliers.		

4.3 Device ordering information

Order numbers have the form shown in Figure 4-4.

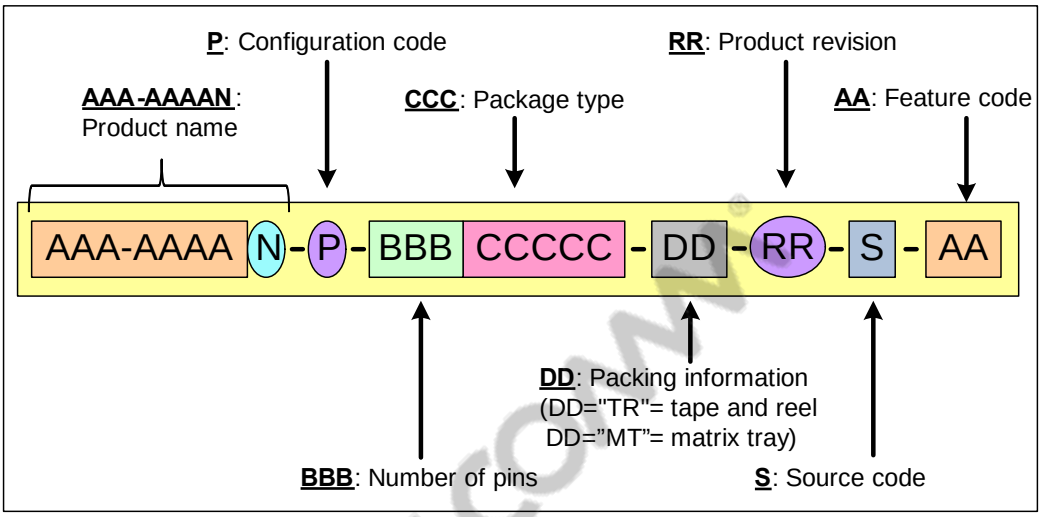


Figure 4-4 Device identification code

Table 4-4 shows the available order numbers.

Table 4-4 QCA9981 Order Numbers

Number	Descriptions
QCA-9981-0-156DRQFN-TR-01-0	RoHS & BrCl-free
QCA-9981-0-156DRQFN-MT-01-0	RoHS & BrCl-free

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. Qualcomm follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. The QCA9981 is classified as MSL3; the qualification temperature was 255ºC.

4.5 Thermal characteristics

Table 4-5 Thermal Resistance

Parameter		Comment	Typical	Unit
θ_{JA}	Junction-to-Ambient	■ With 30 thermal vias[1] ■ Jedec JESD51-2A ■ Jedec JESD51-5	22.95	°C/W
θ_{JB}	Junction-to-Board	■ Jedec JESD51-7 ■ Jedec JESD51-8	20.43	°C/W
θ_{JC}	Junction-to-Case	■ Jedec JESD51-7 ■ Jedec JESD51-8	6.86	°C/W
Ψ_{JT}	Junction-to-Top	■ Jedec JESD51-2A[2]	0.29	°C/W

1. Thermal array is required
2. Use Ψ_{JT} to calculate junction temperature from temperature measured at center of case top; Tj = Tc + (Ψ_{JT} * power)

5 Carrier, Storage, and Handling

5.1 Carrier

5.1.1 Tape and reel information

Carrier tape system conforms to EIA-481 standards.

Simplified sketches of the QCA9981 tape carrier is shown in Figure 5-1 and Figure 5-2, including the part orientation. Tape and reel details for the QCA9981 are as follows:

- Reel diameter: 330 mm
- Hub size: 102 mm
- Tape width: 24mm
- Tape pocket pitch: 16mm
- Feed: Single
- Units per reel: 2000

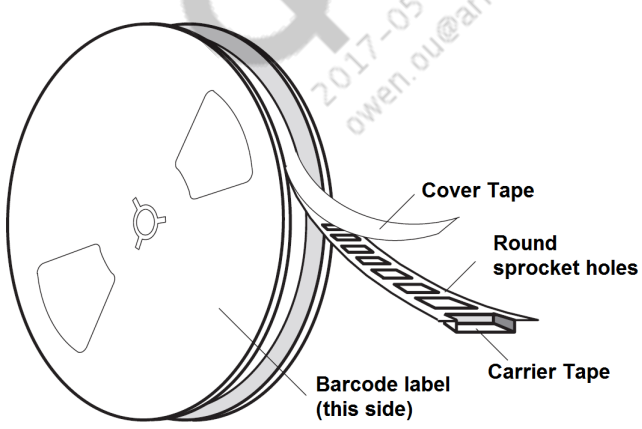


Figure 5-1 Tape orientation on reel

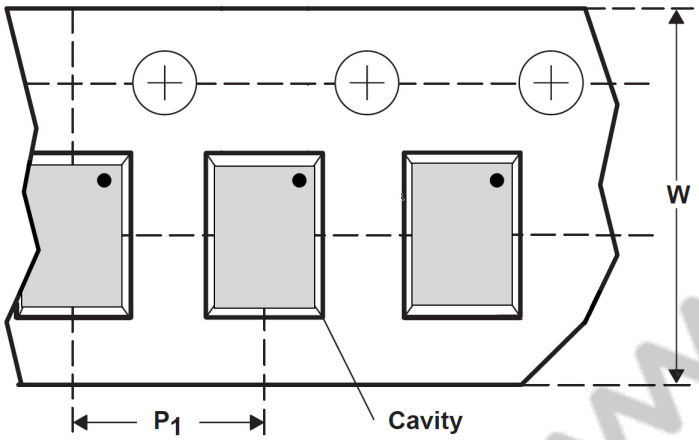
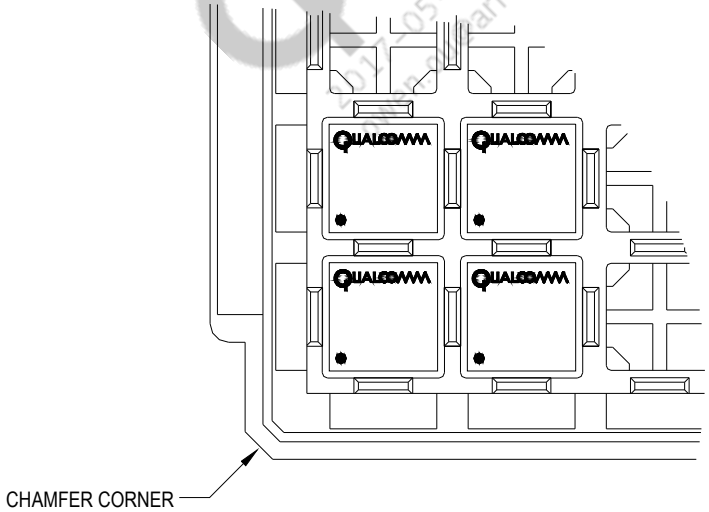


Figure 5-2 Part orientation in tape

5.1.2 Matrix tray information

All QTI matrix tray carriers confirm to JEDEC standards. The device pin 1 is oriented to the chamfered corner of the matrix tray. Each tray of the QCA9981 contains up to 152 devices. See Figure 5-3 for matrix-tray key attributes and dimensions.



Key dimensions	
Array	8 × 19 = 152
M	13.70 mm
M1	18.00 mm
M2	15.50 mm
M3	15.50 mm

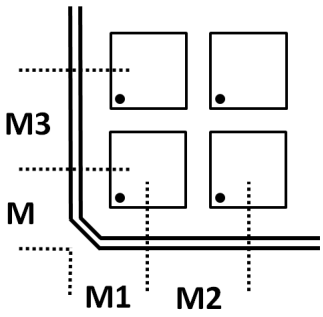


Figure 5-3 Matrix tray part orientation

5.2 Storage

5.2.1 Bagged storage conditions

QCA9981 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling is described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

It is **not necessary** to bake the QCA9981 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the QCA9981 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see *ASIC Packing Methods and Materials Specification* (80-VK055-1) for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

6 PCB Mounting Guidelines

Guidelines for mounting the QCA9981 device onto a PCB are presented in this chapter, including land pad and stencil design details, surface mount technology (SMT) process characterization, and SMT process verification.

6.1 RoHS compliance

The QCA9981 device is externally lead-free and RoHS-compliant. Qualcomm defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products.

6.2 SMT parameters

This section describes board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

Qualcomm recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil-pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability. Review the land pattern and stencil pattern design recommendations as a guide for characterization:

PCB Land and Stencil Design Guide (LS90-NG134-1).

6.2.2 Reflow profile

Reflow profile conditions typically used by Qualcomm for lead-free systems are listed in Table 6-1 and are shown in Figure 6-1.

Table 6-1 Typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Dry-out and flux activation	150 to 190°C	60 to 120sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C. This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

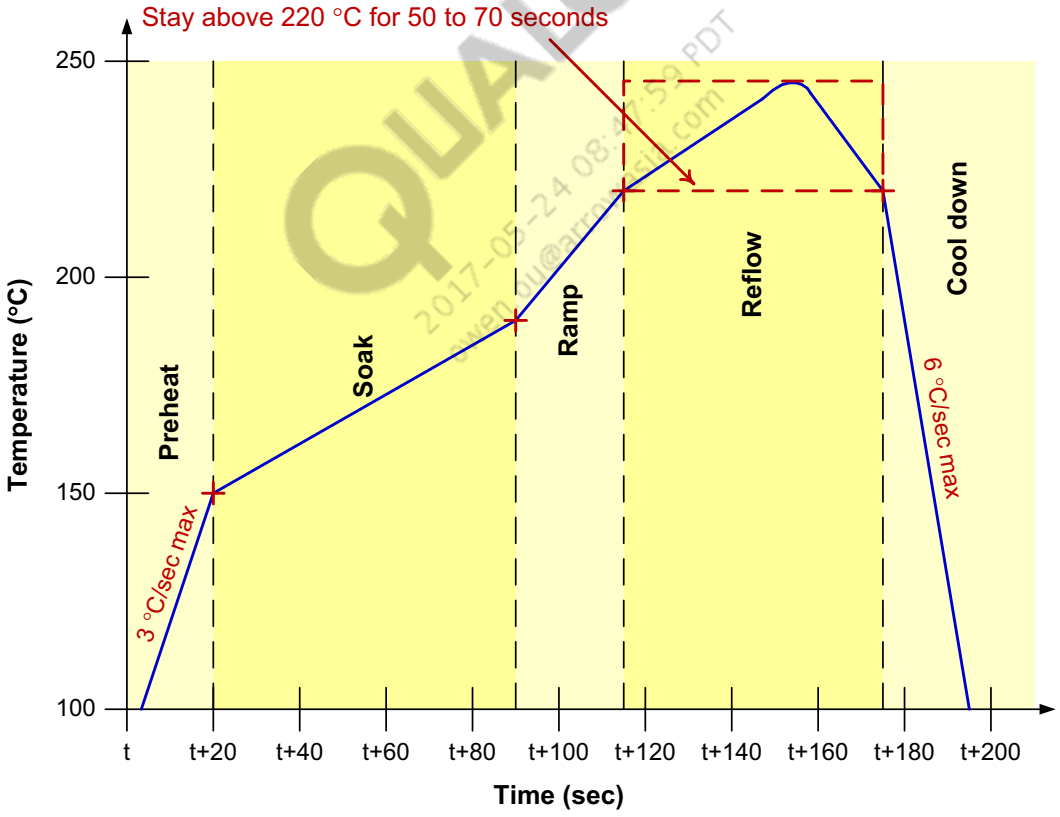


Figure 6-1 Typical SMT reflow profile

6.2.3 SMT peak package-body temperature

During a production board's reflow process, the temperature seen by the package must be controlled. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more). Although the solder-paste manufacturer's recommendations for optimum temperature and duration for solder reflow must be followed, the Qualcomm recommended limits must not be exceeded.

6.2.4 SMT process verification

Qualcomm recommends verification of the SMT process prior to high-volume board assembly, including:

- Electrical continuity
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume

6.3 Board-level reliability

Qualcomm conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

For board-level reliability data, refer to *Board-Level Reliability DRQFN/mQFN* (BR80-NT096-1).

7 Part Reliability

7.1 Reliability qualification summary

QCA9981 reliability evaluation report.

Table 7-1 Reliability Evaluation Results

Tests, standards, and conditions	Sample Size	Result
Average failure rate (AFR, λ) in FIT Failure in billion device-hours Functional HTOL: JESD22-A108-A	240	λ = 46 FIT PASS
Mean time to failure (MTTF, million hours) t = 1/λ	240	~10 yrs
ESD - Human-body model (HBM) rating JESD22-A114-B	3	PASS[1]
ESD - Charge-device model (CDM) rating JESD22-C101-D	3	PASS[2]
Latch-up (I-test): EIA/JESD78 Trigger current: ±100 mA; Temperature: 85°C	6	PASS
Latch-up (V-supply Overvoltage): EIA/JESD78 Trigger voltage: 1.5xVdd; Temperature: 85°C	6	PASS
Moisture resistance test (MRT): **MSL3**, J-STD-020 3 x Reflow Cycles @ 255C +5/-0 °C 100% CSAM Delamination Inspection	480	PASS
Temperature cycle: JESD22-A104 Temperature: -55C to +125C; Number of cycles: 1000 Soak time at min/max temperature: 20 minutes Cycle rate: 2 cycles per hour (cph) **Preconditioning: MSL3**; JESD22-A113 Reflow temperature: 255 °C +5/-0 °C	180	PASS
biased highly accelerated stress test (bHAST): JESD22-A110 **Preconditioning: MSL3;** JESD22-A113 Reflow temperature: 255 °C +5/-0 °C	720	PASS
High-Temperature Storage Life: JESD22-A103 Temperature 150°C, 1000 hours duration	480	PASS
Physical dimensions: JESD22-B100 Package outline drawing in Section 4.1	30	PASS

1. ±2000 V; all pins
2. ±500 V; all pins

7.2 Qualification sample description

Table 7-2 QCA9981 characteristics

Device name	QCA9981
Package type	0.5mm DRQFN
Package body size	12 x 12 x 0.9mm
Pin count	156
Pin composition	Sn
Process	40 nm