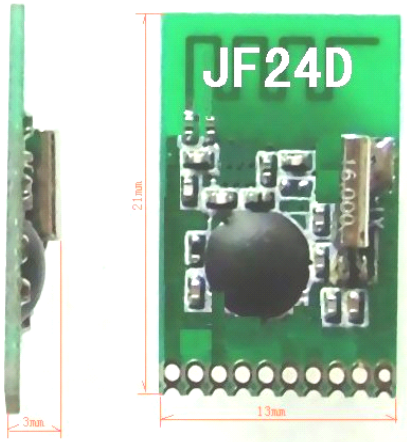
JF24D Functional Description



1.1 TDD RF Transceiver

JF24D operates in TDD mode, either as a transmitter or as a receiver.

The RF channel frequency determines the center of the channel used by JF24D. It can operate on frequencies from 2.397 GHz to 2.4835 GHz. The resolution of the RF channel frequency is 1 MHz.

The RF channel frequency is set by the RF_CH register in register bank 0 according to the following formula: F0= 2397 + RF_CH [MHz] (1 Mbps mode) or F0= 2398 + RF_CH [MHz] (2 Mbps mode). In following chapters, all registers are in register bank 0 except with explicit claim.

A transmitter and a receiver must be programmed with the same RF channel frequency to be able to communicate with each other.

The output power of JF24D is set by the RF_PWR bits in the RF_SETUP register.

1.2 FSK/GFSK MODEM

JF24D supports both FSK and GFSK modulation, which can be set by MODU_MOD register in register bank 1.

Demodulation is done with embedded data slicer and bit recovery logic. The air data rate can be programmed to 1 Mbps or 2 Mbps by RF_DR register. A transmitter and a receiver must be programmed with the same setting.

1.3 State control

1.3.1 State control diagram

JF24D has a built-in state machine that control the state transition between different modes. State transition is fully controlled by MCU when auto acknowledge feature is not enabled. Otherwise there is automatic state transition sometimes for auto acknowledge and auto re-transmission.

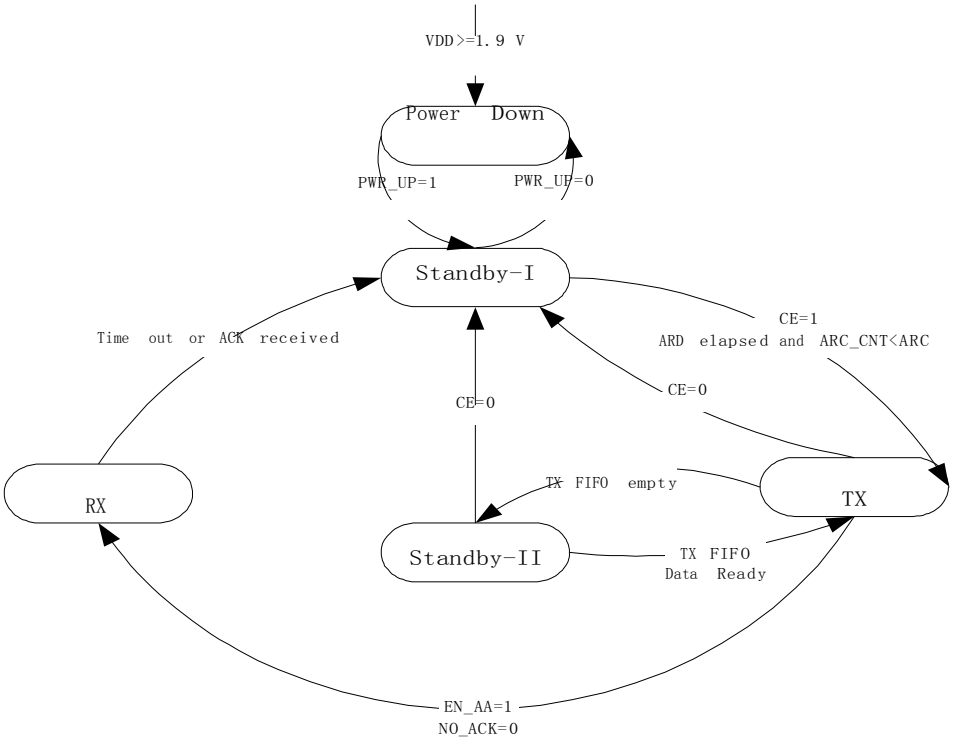


Figure 2 PTX (PRIM_RX=0) state control diagram

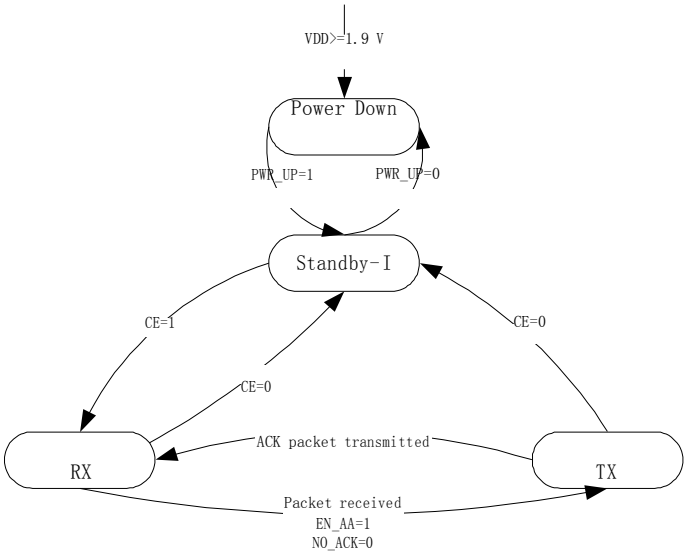


Figure 3 PRX (PRIM_RX=1) state control diagram

- Pin signal: VDD, CE
- SPI register: PWR_UP, PRIM_RX, EN_AA, NO_ACK, ARC, ARD
- System information: Time out, ACK received, ARD elapsed, ARC_CNT, TX FIFO empty, ACK packet transmitted, Packet received

1.3.2 Power Down mode

In power down mode JF24D is in sleep mode with minimal current consumption. SPI interface is still active in this mode. And, all register values are available by SPI. Power down mode is entered by setting the PWR_UP bit in the CONFIG register to low.

1.3.3 Standby-I mode

By setting the PWR_UP bit in the CONFIG register to 1 and de-asserting CE to 0, the device enters into standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start-up time. In this mode, part of the crystal oscillator is active. This is also the mode which the JF24D returns to from TX or RX mode when CE is set low.

1.3.4 Standby-II mode

In standby-II mode more clock buffers are active than in standby-I mode and much more current is used. Standby-II occurs when CE is held high on a PTX device with empty TX FIFO. If a new packet is uploaded to the TX FIFO in this mode, the device will automatically enter into TX mode and the packet is transmitted.

1.3.5 TX mode

- PTX device (PRIM_RX=0)

The TX mode is an active mode where the PTX device transmits a packet. To enter this mode from power down mode, the PTX device must have the PWR_UP bit set high, PRIM_RX bit set low, a payload in the TX FIFO and, a high pulse on the CE for more than 10μs.

The PTX device stays in TX mode until it finishes transmitting the current packet. If CE = 0 it returns to standby-I mode. If CE = 1, the next action is determined by the status of the TX FIFO. If the TX FIFO is not empty the PTX device remains in TX mode, transmitting the next packet. If the TX FIFO is empty the PTX device goes into standby-II mode.

If the auto retransmit is enabled (EN_AA=1) and auto acknowledge is required (NO_ACK=0), the PTX device will enter into TX mode from standby-I mode when ARD elapsed and number of retried is less than ARC.

- PRX device (PRIM_RX=1)

The PRX device will enter into TX mode from RX mode only when EN_AA=1 and NO_ACK=0 in received packet to transmit acknowledge packet with pending payload in TX FIFO.

1.3.6 RX mode

- PRX device (PRIM_RX=1)

The RX mode is an active mode where the JF24D radio is configured to be a receiver. To enter this mode from standby-I mode, the PRX device must have the PWR_UP bit set high, PRIM_RX bit set high and the CE pin set high. Or PRX device can enter this mode from TX mode after transmitting a acknowledge packet when EN_AA=1 and NO_ACK=0 in received packet.

In this mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the packet processing engine. The packet processing engine continuously searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFO. If the RX FIFO is full, the received packet is discarded.

The PRX device remains in RX mode until the MCU configures it to standby-I mode or power down mode.

In RX mode a carrier detection (CD) signal is available. The CD is set to high when a RF signal is detected inside the receiving frequency channel. The signal must be FSK/GFSK modulated for a secure detection. Other signals can also be detected. The CD is set high when an RF signal is detected in RX mode, otherwise CD is low. The internal CD signal is filtered before presented to CD register. The RF signal must be present for about 200 μs before the CD is set high.

- PTX device (PRIM_RX=0)

The PTX device will enter into RX mode from TX mode only when EN_AA=1 and NO_ACK=0 to receive acknowledge packet.

1.4 Packet processing

1.4.1 Packet format

There are two packet formats as follows.

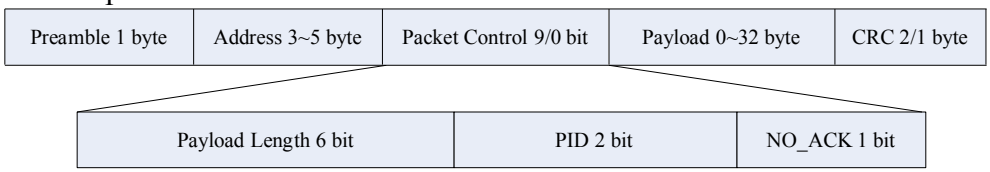


Figure 4 Packet Format at Normal Payload Mode

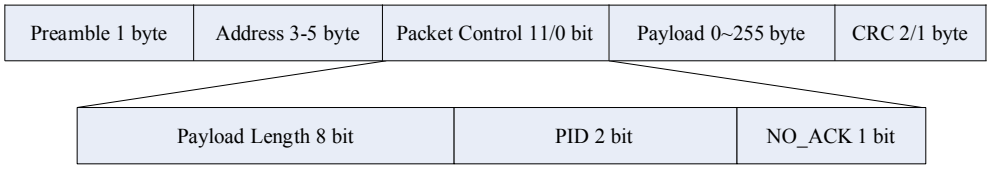


Figure 5 Packet Format at Long Payload Mode

In normal payload mode, there are three levels 32 bytes FIFO for both TX and RX, supporting both acknowledge mode or no acknowledge mode with up to six pipes.

In long payload mode, there is single level 255 bytes TX and RX FIFO.

Payload mode can be selected by LONG_PL register in register bank 1.

1.4.1.1 Preamble

The preamble is a bit sequence used to detect 0 and 1 levels in the receiver. The preamble is one byte long and is either 01010101 or 10101010. If the first bit in the address is 1 the preamble is automatically set to 10101010 and if the first bit is 0 the preamble is automatically set to 01010101. This is done to ensure there are enough transitions in the preamble to stabilize the receiver.

1.4.1.2 Address

This is the address for the receiver. An address ensures that the packet is detected by the target receiver. The address field can be configured to be 3, 4, or 5 bytes long by the AW register.

The PRX device can open up to six data pipes to support up to six PTX devices with unique addresses. All six PTX device addresses are searched simultaneously. In PRX side, the data pipes are enabled with the bits in the EN_RXADDR register. By default only data pipe 0 and 1 are enabled.

Each data pipe address is configured in the RX_ADDR_PX registers.

Each pipe can have up to 5 bytes configurable address. Data pipe 0 has a unique 5 byte address. Data pipes 1-5 share the 4 most significant address bytes. The LSB byte must be unique for all 6 pipes.

To ensure that the ACK packet from the PRX is transmitted to the correct PTX, the PRX takes the data pipe address where it received the packet and uses it as the TX address when transmitting the ACK packet.

On the PRX the RX_ADDR_Pn, defined as the pipe address, must be unique. On the PTX the TX_ADDR must be the same as the RX_ADDR_P0 on the PTX, and as the pipe address for the designated pipe on the PRX.

No other data pipe can receive data until a complete packet is received by a data pipe that has detected its address. When multiple PTX devices are transmitting to a PRX, the ARD can be used to skew the auto retransmission so that they only block each other once.

1.4.1.3 Packet control

When Dynamic Payload Length function is disabled, there is no packet control field.

When Dynamic Payload Length function is enabled, the packet control field contains a 6/8 bit payload length field, a 2 bit PID (Packet Identity) field and, a 1 bit NO_ACK flag.

- Payload length

The payload length field is only used if the Dynamic Payload Length function is enabled.

- PID

The 2 bit PID field is used to detect whether the received packet is new or retransmitted. PID prevents the PRX device from presenting the same payload more than once to the MCU. The PID field is incremented at the TX side for each new packet received through the SPI. The PID and CRC fields are used by the PRX device to determine whether a packet is old or new. When several data packets are lost on the link, the PID fields may become equal to the last received PID. If a packet has the same PID as the previous packet, JF24D compares the CRC sums from both packets. If the CRC sums are also equal, the last received packet is considered a copy of the previously received packet and discarded.

- NO_ACK

The NO_ACK flag is only used when the auto acknowledgement feature is used. Setting the flag high, tells the receiver that the packet is not to be auto acknowledged.

The PTX can set the NO_ACK flag bit in the Packet Control Field with this command: W_TX_PAYLOAD_NOACK

However, the function must first be enabled in the FEATURE register by setting the EN_DYN_ACK bit. When you use this option the PTX goes directly to standby-I mode after transmitting the packet and the PRX does not transmit an ACK packet when it receives the packet.

1.4.1.4 Payload

The payload is the user defined content of the packet. It can be 0 to 32 bytes wide in normal payload mode or 0 to 255 bytes wide in long payload mode, and it is transmitted on-air as it is uploaded (unmodified) to the device.

The JF24D provides two alternatives for handling payload lengths, static and dynamic payload length for both normal payload mode and long payload mode. The static payload length of each of six data pipes can be individually set in normal payload mode, but share same setting in long payload mode.

The default alternative is static payload length. With static payload length all packets between a transmitter and a receiver have the same length. Static payload length is set by the RX_PW_Px registers in normal payload mode or the LEN_LONG in long payload mode on the receiver side. The payload length on the transmitter side is set by the number of bytes clocked into the TX_FIFO and must equal the value in the RX_PW_Px register on the receiver side. In normal payload mode, each pipe has its own payload length, but has same payload length in long payload mode.

Dynamic Payload Length (DPL) is an alternative to static payload length. DPL enables the transmitter to send packets with variable payload length to the receiver. This means for a system with different payload lengths it is not necessary to scale the packet length to the longest payload.

With DPL feature the JF24D can decode the payload length of the received packet automatically instead of using the RX_PW_Px registers. The MCU can read the length of the received payload by using the R_RX_PL_WID command.

In order to enable DPL the EN_DPL bit in the FEATURE register must be set. In RX mode the DYNPD register has to be set. A PTX that transmits to a PRX with DPL enabled must have the DPL_P0 bit in DYNPD set.

1.4.1.5 CRC

The CRC is the error detection mechanism in the packet. The number of bytes in the CRC is set by the CRCO bit in the CONFIG register. It may either be 1 or 2 bytes and is

calculated over the address, Packet Control Field, and Payload.

The polynomial for 1 byte CRC is $X^8 + X^2 + X + 1$. Initial value 0xFF
The polynomial for 2 byte CRC is $X^{16} + X^{12} + X^5 + 1$. Initial value 0xFFFF

No packet is accepted by receive side if the CRC fails.

1.4.2 Packet handling

JF24D uses burst mode for payload transmission and receive.

The transmitter fetches payload from TX FIFO, automatically assembles it into packet and transmits the packet in a very short burst period with 1 Mbps or 2 Mbps air data rate. After transmission, JF24D sets TX_DS and gives an active low interrupt IRQ to MCU.

The receiver automatically validates and disassembles received packet, if there is a valid packet within the new payload, it will write the payload into RX FIFO, set RX_DR and give an active low interrupt IRQ to MCU.

When auto acknowledge is enabled (EN_AA=1), the PTX device will automatically wait for acknowledge packet after transmission, and re-transmit original packet with the delay of ARD until a acknowledge packet is received or the number of re-transmission exceeds a threshold ARC. If the later one happens, JF24D will set MAX_RT and give an active low interrupt IRQ to MCU. Two packet loss counters are incremented each time a packet is lost, ARC_CNT and PLOS_CNT in the OBSERVE_TX register. The ARC_CNT counts the number of retransmissions for the current transaction. The PLOS_CNT counts the total number of retransmissions since the last channel change. ARC_CNT is reset by initiating a new transaction. PLOS_CNT is reset by writing to the RF_CH register. It is possible to use the information in the OBSERVE_TX register to make an overall assessment of the channel quality.

The PTX device will retransmit if its RX FIFO is full but received ACK frame has payload.

As an alternative for PTX device to auto retransmit it is possible to manually set the JF24D to retransmit a packet a number of times. This is done by the REUSE_TX_PL command.

When auto acknowledge is enabled, the PRX device will automatically check the NO_ACK field in received packet, and if NO_ACK=0, it will automatically send a acknowledge packet to PTX device. If EN_ACK_PAY is set, and the acknowledge packet can also include pending payload in TX FIFO.

1.5 TX/RX FIFO

The data FIFO are used to store payload that is to be transmitted (TX FIFO) or payload that is received and ready to be clocked out (RX FIFO). The FIFO is accessible in both PTX mode and PRX mode.

The following FIFO is present in JF24D:

- Normal payload mode
  - TX three levels, 32 byte FIFO
  - RX three levels, 32 byte FIFO
- Long payload mode
  - TX single level, 255 byte FIFO
  - RX single level, 255 byte FIFO

Both FIFO have a controller and are accessible through the SPI by using dedicated SPI commands. A TX FIFO in PRX can store payload for ACK packets to three different PTX devices in normal payload mode or to only one PTX device in long payload mode. If the TX FIFO contains more than one payload to a pipe, payloads are handled using the first in - first out principle. The TX FIFO in a PRX is blocked if all pending payloads are addressed to pipes where the link to the PTX is lost. In this case, the MCU can flush the TX FIFO by using the FLUSH_TX command.

The RX FIFO in PRX may contain payload from up to three different PTX devices in normal payload mode, or to only one PTX devices in long payload mode.

.

A TX FIFO in PTX can have up to three payloads stored.

The TX FIFO can be written to by three commands, W_TX_PAYLOAD and W_TX_PAYLOAD_NO_ACK in PTX mode and W_ACK_PAYLOAD in PRX mode. All three commands give access to the TX_PLD register.

The RX FIFO can be read by the command R_RX_PAYLOAD in both PTX and PRX mode. This command gives access to the RX_PLD register.

The payload in TX FIFO in a PTX is NOT removed if the MAX_RT IRQ is asserted.

In the FIFO_STATUS register it is possible to read if the TX and RX FIFO are full or empty. The TX_REUSE bit is also available in the FIFO_STATUS register. TX_REUSE is set by the SPI command REUSE_TX_PL, and is reset by the SPI commands W_TX_PAYLOAD or FLUSH TX.

1.6 Interrupt

The JF24D has an active low interrupt (IRQ) pin. The IRQ pin is activated when

TX_DS IRQ, RX_DR IRQ or MAX_RT IRQ are set high by the state machine in the STATUS register. The IRQ pin resets when MCU writes '1' to the IRQ source bit in the STATUS register. The IRQ mask in the CONFIG register is used to select the IRQ sources that are allowed to assert the IRQ pin. By setting one of the MASK bits high, the corresponding IRQ source is disabled. By default all IRQ sources are enabled.

The 3 bit pipe information in the STATUS register is updated during the IRQ pin high to low transition. If the STATUS register is read during an IRQ pin high to low transition, the pipe information is unreliable.

1.7 SPI Interface

1.7.1 SPI command

The SPI commands are shown in **Table 2**. Every new command must be started by a high to low transition n CSN.

In parallel to the SPI command word applied on the MOSI pin, the STATUS register is shifted serially out on the MISO pin.

The serial shifting SPI commands is in the following format:

- <Command word: MSB bit to LSB bit (one byte)>
- <Data bytes: LSB byte to MSB byte, MSB bit in each byte first> for all registers at bank 0 and register 9 to register 14 at bank 1
- <Data bytes: MSB byte to LSB byte, MSB bit in each byte first> for register 0 to register 8 at bank 1

Table 2 SPI command

Command name	**Command word (binary)**	**# Data bytes**	**Operation**
R_REGISTER	000A AAAA	1 to 5 LSB byte first	Read command and status registers. AAAAA = 5 bit Register Map Address
W_REGISTER	001A AAAA	1 to 5 LSB byte first	Write command and status registers. AAAAA = 5 bit Register Map Address Executable in power down or standby modes only.
R_RX_PAYLOAD	0110 0001	1 to 32 or 1-255 LSB byte first	Read RX-payload: 1 – 32 bytes or 1-255 bytes. A read operation always starts at byte 0. Payload is deleted from FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	1010 0000	1 to 32 or 1 to 255 LSB byte first	Write TX-payload: 1 – 32 bytes or 1-255 bytes. A write operation always starts at byte 0 used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode Should not be executed during transmission of acknowledge, that is, acknowledge package will not be completed.

REUSE_TX_PL	1110 0011	0	Used for a PTX device Reuse last transmitted payload. Packets are repeatedly retransmitted as long as CE is high. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX payload reuse must not be activated or deactivated during package transmission
ACTIVATE	0101 0000	1	This write command followed by data 0x73 activates the following features: •R_RX_PL_WID •W_ACK_PAYLOAD •W_TX_PAYLOAD_NOACK A new ACTIVATE command with the same data deactivates them again. This is executable in power down or stand by modes only. The R_RX_PL_WID, W_ACK_PAYLOAD, and W_TX_PAYLOAD_NOACK features registers are initially in a deactivated state; a write has no effect, a read only results in zeros on MISO. To activate these registers, use the ACTIVATE command followed by data 0x73. Then they can be accessed as any other register in JF24D.Use the same command and data to deactivate the registers again. This write command followed by data 0x53 toggles the register bank, and the current register bank number can be read out from REG7 [7]
R_RX_PL_WID	0110 0000		Read RX-payload width for the top R_RX_PAYLOAD in the RX FIFO.
W_ACK_PAYLOAD	1010 1PPP	1 to 32 or 1 to 255 LSB byte first	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled using first in - first out principle. Write payload: 1– 32 bytes or 1– 255 bytes. A write operation always starts at byte 0.
W_TX_PAYLOAD_NOACK	1011 0000	1 to 32 or 1 to 255 LSB byte first	Used in TX mode. Disables AUTOACK on this specific packet.
NOP	1111 1111	0	No Operation. Might be used to read the STATUS register

1.7.2 SPI timing

Cn: SPI command bit
Sn: STATUS register bit
Dn: Data Bit (LSB byte to MSB byte, MSB bit in each byte first)

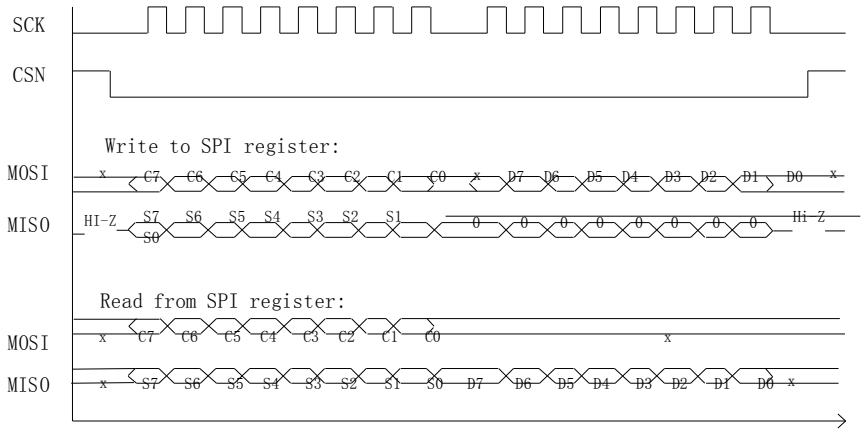


Figure 8 SPI timing

Note: The SPI timing is for bank 0 and register 9 to 14 at bank 1. For register 0 to 8 at bank 1, the byte order is inversed that the MSB byte is R/W before LSB byte.

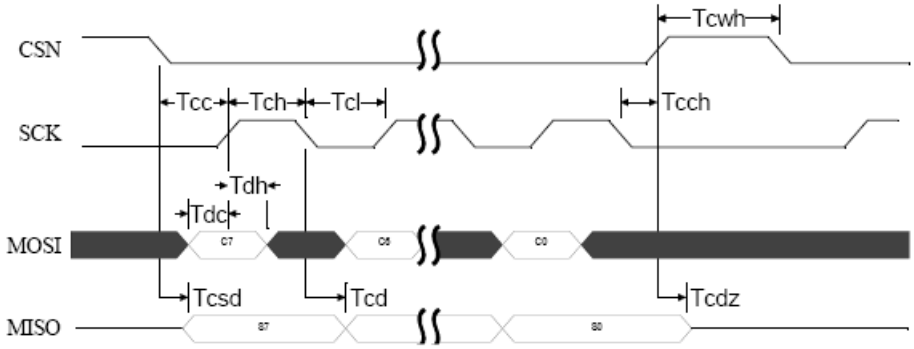


Figure 9 SPI NOP timing diagram

Table 3 SPI timing parameter

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	10		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		38	ns
Tcd	SCK to Data Valid		55	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	8	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		38	ns

1.7.3 Register map

There are two register banks, which can be toggled by SPI command “ACTIVATE” followed with 0x53 byte, and bank state can be read from REG7 [7].

1.7.3.1 Register bank 0

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
00	CONFIG				Configuration Register
	Reserved	7	0	R/W	Only '0' allowed
	MASK_RX_DR	6	0	R/W	Mask interrupt caused by RX_DR 1: Interrupt not reflected on the IRQ pin 0: Reflect RX_DR as active low interrupt on the IRQ pin
	MASK_TX_DS	5	0	R/W	Mask interrupt caused by TX_DS 1: Interrupt not reflected on the IRQ pin 0: Reflect TX_DS as active low interrupt on the IRQ pin
	MASK_MAX_RT	4	0	R/W	Mask interrupt caused by MAX_RT 1: Interrupt not reflected on the IRQ pin 0: Reflect MAX_RT as active low interrupt on the IRQ pin
	EN_CRC	3	1	R/W	Enable CRC. Forced high if one of the bits in the EN_AA is high
	CRCO	2	1	R/W	CRC encoding scheme '0' - 1 byte '1' - 2 bytes
	PWR_UP	1	1	R/W	1: POWER UP, 0:POWER DOWN
	PRIM_RX	0	0	R/W	RX/TX control, only can be switched in power down state (REG0[1]=0) 1: PRX, 0: PTX
01	EN_AA				Enable ‘Auto Acknowledgment’ Function
	Reserved	7:6	00	R/W	Only '00' allowed
	ENAA_P5	5	1	R/W	Enable auto acknowledgement data pipe 5
	ENAA_P4	4	1	R/W	Enable auto acknowledgement data pipe 4
	ENAA_P3	3	1	R/W	Enable auto acknowledgement data pipe 3
	ENAA_P2	2	1	R/W	Enable auto acknowledgement data pipe 2
	ENAA_P1	1	1	R/W	Enable auto acknowledgement data pipe 1
	ENAA_P0	0	1	R/W	Enable auto acknowledgement data pipe 0
02	EN_RXADDR				Enabled RX Addresses
	Reserved	7:6	00	R/W	Only '00' allowed
	ERX_P5	5	0	R/W	Enable data pipe 5.
	ERX_P4	4	0	R/W	Enable data pipe 4.
	ERX_P3	3	0	R/W	Enable data pipe 3.
	ERX_P2	2	0	R/W	Enable data pipe 2.
	ERX_P1	1	1	R/W	Enable data pipe 1.
	ERX_P0	0	1	R/W	Enable data pipe 0.
03	SETUP_AW				Setup of Address Widths (common for all data pipes)

	Reserved	7:2	000000	R/W	Only '000000' allowed
	AW	1:0	11	R/W	RX/TX Address field width '00' - Illegal '01' - 3 bytes '10' - 4 bytes '11' - 5 bytes LSB byte is used if address width is below 5 bytes
04	SETUP_RETR				Setup of Automatic Retransmission
	ARD	7:4	0000	R/W	Auto Retransmit Delay ‘0000’ – Wait 250 uS ‘0001’ – Wait 500 uS ‘0010’ – Wait 750 uS …….. ‘1111’ – Wait 4000 us (Delay defined from end of transmission to start of next transmission)a
	ARC	3:0	0011	R/W	Auto Retransmit Count ‘0000’ – Re-Transmit disabled ‘0001’ – Up to 1 Re-Transmit on fail of AA …… ‘1111’ – Up to 15 Re-Transmit on fail of AA
05	RF_CH				RF Channel
	Reserved	7	0	R/W	Only '0' allowed
	RF_CH	6:0	0000010	R/W	Sets the frequency channel JF24D operates on
06	RF_SETUP				RF Setup Register
	Reserved	7	111	R/W	Only '000' allowed
	RSSI_EN	6	1	R/W	Enable RSSI measurement 0: Disable 1: Enable
	DREG_ON	5	1	R/W	Digital regulator can be shut down or not 0: Can be shut down in stand-by I mode 1: Always on in any state except power down
	RF_PWR[2]	4	1	R/W	RF output power in TX mode
	RF_DR	3	1	R/W	Air Data Rate ‘0’ – 1Mbps ‘1’ – 2Mbps Register 4 and 13 in bank 1 have different setting in 1 Mbps and 2 Mbps data rate mode
	RF_PWR[1:0]	2:1	11	R/W	Set RF output power in TX mode RF_PWR[2:0]\ '000' – -35dBm '001' – -25 dBm '010' – -15 dBm '011' – -5 dBm '100' – -5 dBm '101' – -5 dBm '110' – 0 dBm '111' – 5 dBm
	LNA_HCURR	0	1	R/W	Setup LNA gain

07	STATUS				Status Register (In parallel to the SPI command word applied on the MOSI pin, the STATUS register is shifted serially out on the MISO pin)
	RBANK	7	0	R	Register bank selection states. Switch register bank is done by SPI command "ACTIVATE" followed by 0x53 0: Register bank 0 1: Register bank 1
	RX_DR	6	0	R/W	Data Ready RX FIFO interrupt Asserted when new data arrives RX FIFO Write 1 to clear bit.
	TX_DS	5	0	R/W	Data Sent TX FIFO interrupt Asserted when packet transmitted on TX. If AUTO_ACK is activated, this bit is set high only when ACK is received. Write 1 to clear bit.
	MAX_RT	4	0	R/W	Maximum number of TX retransmits interrupt Write 1 to clear bit. If MAX_RT is asserted it must be cleared to enable further communication.
	RX_P_NO	3:1	111	R	Data pipe number for the payload available for reading from RX_FIFO 000-101: Data Pipe Number 110: RX FIFO Empty 111: Not used
	TX_FULL	0	0	R	TX FIFO full flag. 1: TX FIFO full 0: Available locations in TX FIFO
08	OBSERVE_TX				Transmit observe register
	PLOS_CNT	7:4	0	R	Count lost packets. The counter is overflow protected to 15, and discontinues at max until reset. The counter is reset by writing to RF_CH.
	ARC_CNT	3:0	0	R	Count retransmitted packets. The counter is reset when transmission of a new packet starts.
09	CD				
	Reserved	7:1	000000	R	
	CD	0	0	R	Carrier Detect
0A	RX_ADDR_P0	39:0	0xE7E7E7E7E7	R/W	Receive address data pipe 0. 5 Bytes maximum length. (LSB byte is written first. Write the number of bytes defined by SETUP_AW)
0B	RX_ADDR_P1	39:0	0xC2C2C2C2C2	R/W	Receive address data pipe 1. 5 Bytes maximum length. (LSB byte is written first. Write the number of bytes defined by SETUP_AW)
0C	RX_ADDR_P2	7:0	0xC3	R/W	Receive address data pipe 2. Only LSB MSB bytes is equal to RX_ADDR_P1[39:8]
0D	RX_ADDR_P3	7:0	0xC4	R/W	Receive address data pipe 3. Only LSB MSB bytes is equal to RX_ADDR_P1[39:8]
0E	RX_ADDR_P4	7:0	0xC5	R/W	Receive address data pipe 4. Only LSB. MSB bytes is equal to RX_ADDR_P1[39:8]
0F	RX_ADDR_P5	7:0	0xC6	R/W	Receive address data pipe 5. Only LSB.

					MSB bytes is equal to RX_ADDR_P1[39:8]
10	TX_ADDR	39:0	0xE7E7E7E7E7	R/W	Transmit address. Used for a PTX device only. (LSB byte is written first) Set RX_ADDR_P0 equal to this address to handle automatic acknowledge if this is a PTX device
11	RX_PW_P0				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P0	5:0	0	R/W	Number of bytes in RX payload in data pipe 0 (1 to 32 bytes). 0: not used 1 = 1 byte … 32 = 32 bytes
12	RX_PW_P1				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P1	5:0	0	R/W	Number of bytes in RX payload in data pipe 1 (1 to 32 bytes). 0: not used 1 = 1 byte … 32 = 32 bytes
13	RX_PW_P2				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P2	5:0	0	R/W	Number of bytes in RX payload in data pipe 2 (1 to 32 bytes). 0: not used 1 = 1 byte … 32 = 32 bytes
14	RX_PW_P3				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P3	5:0	0	R/W	Number of bytes in RX payload in data pipe 3 (1 to 32 bytes). 0: not used 1 = 1 byte … 32 = 32 bytes
15	RX_PW_P4				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P4	5:0	0	R/W	Number of bytes in RX payload in data pipe 4 (1 to 32 bytes). 0: not used 1 = 1 byte … 32 = 32 bytes
16	RX_PW_P5				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P5	5:0	0	R/W	Number of bytes in RX payload in data pipe 5 (1 to 32 bytes). 0: not used 1 = 1 byte

					… 32 = 32 bytes
17	FIFO_STATUS				FIFO Status Register
	Reserved	7	0	R/W	Only '0' allowed
	TX_REUSE	6	0	R	Reuse last transmitted data packet if set high. The packet is repeatedly retransmitted as long as CE is high. TX_REUSE is set by the SPI command REUSE_TX_PL, and is reset by the SPI commands W_TX_PAYLOAD or FLUSH TX
	TX_FULL	5	0	R	TX FIFO full flag 1: TX FIFO full; 0: Available locations in TX FIFO
	TX_EMPTY	4	1	R	TX FIFO empty flag. 1: TX FIFO empty 0: Data in TX FIFO
	Reserved	3:2	00	R/W	Only '00' allowed
	RX_FULL	1	0	R	RX FIFO full flag 1: RX FIFO full 0: Available locations in RX FIFO
	RX_EMPTY	0	1	R	RX FIFO empty flag 1: RX FIFO empty 0: Data in RX FIFO
N/A	ACK_PLD	255:0	X	W	Written by separate SPI command ACK packet payload to data pipe number PPP given in SPI command Used in RX mode only Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled first in first out.
N/A	TX_PLD	255:0	X	W	Written by separate SPI command TX data pay-load register 1 - 32 bytes. This register is implemented as a FIFO with three levels. Used in TX mode only
N/A	RX_PLD	255:0	X	R	Read by separate SPI command RX data payload register. 1 - 32 bytes. This register is implemented as a FIFO with three levels. All RX channels share the same FIFO.
1C	DYNPD				Enable dynamic payload length
	Reserved	7:6	0	R/W	Only ‘00’ allowed
	DPL_P5	5	0	R/W	Enable dynamic payload length data pipe 5. (Requires EN_DPL and ENAA_P5)
	DPL_P4	4	0	R/W	Enable dynamic payload length data pipe 4. (Requires EN_DPL and ENAA_P4)
	DPL_P3	3	0	R/W	Enable dynamic payload length data pipe 3. (Requires EN_DPL and ENAA_P3)
	DPL_P2	2	0	R/W	Enable dynamic payload length data pipe 2. (Requires EN_DPL and ENAA_P2)
	DPL_P1	1	0	R/W	Enable dynamic payload length data pipe 1. (Requires EN_DPL and ENAA_P1)
	DPL_P0	0	0	R/W	Enable dynamic payload length data pipe 0. (Requires EN_DPL and ENAA_P0)
1D	FEATURE			R/W	Feature Register
	Reserved	7:3	0	R/W	Only ‘00000’ allowed

	EN_DPL	2	0	R/W	Enables Dynamic Payload Length
	EN_ACK_PAY	1	0	R/W	Enables Payload with ACK
	EN_DYN_ACK	0	0	R/W	Enables the W_TX_PAYLOAD_NOACK command
Note: Don't write reserved registers and registers at other addresses in register bank 0					

1.7.3.2 Register bank 1

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
00		31:0	0	W	Must write with 0x414B01F2
01		31:0	0	W	Must write with 0xC04B0630
02		31:0	0	W	Must write with 0xA0FCC400
03		31:0	0x 03001200	W	Must write with 0x17003560
04		31:0	0	W	Must write with 0x4199000B (1Mbps data rate mode) or 0x4199100B (2 Mbps data rate mode) Write with 0x41110421 with make JF24D transmit CW at the given channel
	XTALFC	16:13		W	Crystal offset compensation, center at 8. User can adjust this register to compensate crystal offset
05		31:0	0	W	Must write with 0x24017FBE
	RSSI_TH	29:26		W	RSSI Threshold for CD detect 0: -97 dBm, 2 dB/step, 15: -67 dBm
06		31:0	0	W	Must write with 0x00004000
07		31:0	0	W	Must write with 0x00000000
	RBANK	7		R	Register bank selection states. Switch register bank is done by SPI command "ACTIVATE" followed by 0x53 0: Register bank 0 1: Register bank 1
08	Chip ID	31:0	0	R	Chip ID 0x61616161
09			0		Must write with 0x00000000
0A			0		Must write with 0xF6F54EF6
0B			0		Must write with 0xD651185C
0C		31:0	0		Please initialize with 0x2D005540
	TX_LOCK_SEL	10:9		R/W	Tx PLL lock time selection 0: 120 us, 1: 200 us, 2: 300 us, 3: 500 us
	TX_RAMP_SEL	8:5		R/W	Tx PA ramping time selection 0: 10 us, 1: 20us, 2: 30 us, … , 15: 160 us
0D	NEW_FEATURE	31:0	0		Please initialize with 0x00007000 (1 Mbps data rate mode) or 0x00000400 (2 Mbps data rate mode)
	CYST_ACCU	14:12		R/W	Crystal accuracy, the worse accuracy requires the larger value Using 7 for crystal accuracy to about 100 PPM Using 0 for crystal accuracy better than 5
		11		R/W	Reserved

	MODU_MOD	10		R/W	Modulation type 1: FSK mode 0: GFSK mode
	GFSK_BT	9		R/W	1: BT = 0.5 0: BT = 1
	LONG_PL	8		R/W	Enable long payload in normal payload mode 1: Enable long payload mode 0: Normal payload mode
	LEN_LONG	7:0		R/W	Payload length for maximum 255 bytes payload
0E	RAMP	87:0	0x 8fbde72aa 16523081	W	Ramp curve Must write with 0xCFEF7CF208104082081041
Note: Don’t write reserved registers and no definition registers in register bank 1					