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MT7601U DATASHEET

802.11b/g/n/ Wi-Fi 1T1R Single Chip

Document Revision History

Revision	Date	Author	Description
1.0	20130903	Alex Lin	Formal release v1.0

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1 System Overview

1.1 General Descriptions

The MT7601U is a highly integrated Wi-Fi single chip which supports 150 Mbps PHY rate. It fully complies with IEEE 802.11n and IEEE 802.11 b/g standards, offering feature-rich wireless connectivity at high standards, and delivering reliable, cost-effective throughput from an extended distance.

Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. Intelligent MAC design deploys a high efficient DMA engine and hardware data processing accelerators which offloads the host processor.

The MT7601U is designed to support standard based features in the areas of security, quality of service and international regulations, giving end users the greatest performance any time and in any circumstance.

1.2 Features

1.2.1 Platform

- Embedded high-performance 32-bit RISC microprocessor
- Highly integrated RF with 55nm CMOS technology
- Integrate high efficiency switching regulator
- Best-in-class active and idle power consumption performance
- Compact 5mm x 5mm QFN40L package
- 1/2/3/4-wire PTA WiFi / Bluetooth coexistence
- Buffered clock output for co-clock with other SOC chipset
- Integrate EFUSE to eliminate the requirement for external EEPROM
- External serial flash support
- 7 programmable general purpose Input / Output
- 2 configurable LED pins
- Fully compliance with USB v2.0 High-speed mode
- Auto-calibration

1.2.2 WLAN

- IEEE 802.11 b/g/n compliant
- 1T1R mode with support of 150Mbps PHY rate
- Greenfield, mixed mode, legacy modes support
- Frame aggregation
- Integrated LNA, PA, and T/R switch
- IEEE 802.11 d/h/k support
- Security support for WFA WPA/WPA2 personal, WPS2.0, WAPI
- Supports 802.11w protected managed frames
- QoS support of WFA WMM, WMM PS
- Supports Wi-Fi Direct

- Per packet transmit power control
- Wake on WLAN

1.3 Applications

MT7601U is designed for a compact PCB design for USB interface. It is suitable for the following applications.

- Laptop NB
- Tablet/MID
- USB dongle
- DTV
- BDP

1.4 Block Diagram

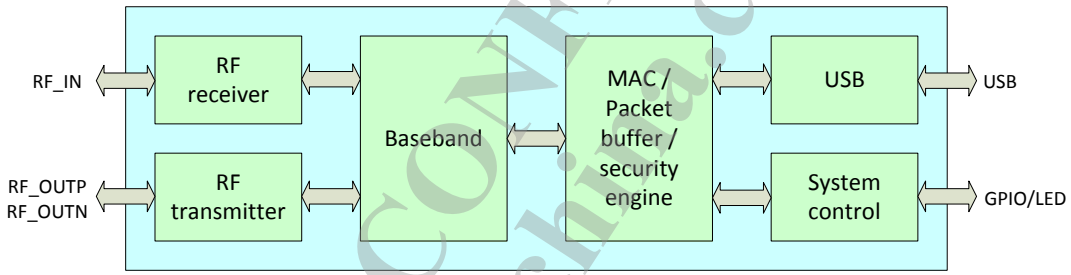


Figure 1 MT7601U block diagram

2 Product Descriptions

2.1 Pin Layout

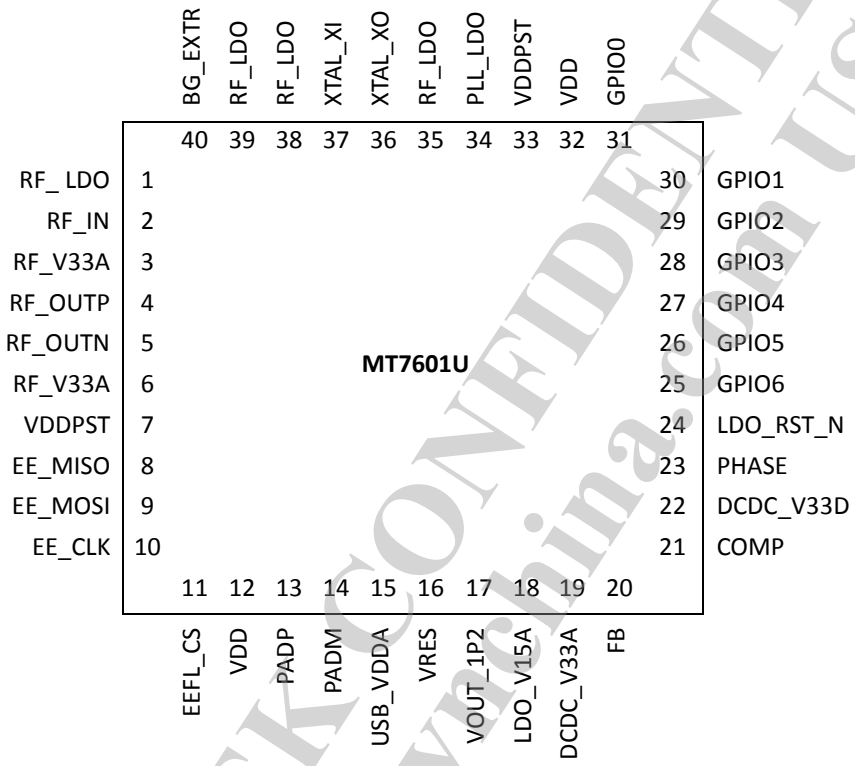


Figure 2 Top view of MT7601U QFN pin-out.

2.2 PIN Description

QFN40	Pin Name	Pin description	Default PU/PD	I/O	Supply domain
Reset and clocks					
24	LDO_RST_N	External system reset active low	N/A	Input	VDDPST
37	XTAL_XI	Crystal input or external clock input	N/A	Input	
36	XTAL_XO	Crystal output	N/A	Input	
USB interface					
15	USB_VDDA	USB 3.3V power supply	N/A		
16	VRES	USB BG reference	N/A		
13	PADP	USB D+ signal	N/A	In/out	USB_VDDA
14	PADM	USB D- signal	N/A	In/out	USB_VDDA
EEPROM/flash interface					
8	EE_MISO	External memory data input / Antenna select	PD	Input	VDDPST
9	EE_MOSI	External memory data output / Antenna select	PD	Output	VDDPST
10	EE_CLK	External clock	PU	Output	VDDPST
11	EEFL_CS	External chip select	PU	Output	VDDPST
Programmable I/O					
31	GPIO0	Programmable input/output / Bluetooth coexistence	PD	In/out	
30	GPIO1	Programmable input/output / Bluetooth coexistence	PD	In/out	VDDPST
29	GPIO2	Programmable input/output	PD	In/out	VDDPST
28	GPIO3	Programmable input/output / Bluetooth coexistence	PD	In/out	VDDPST
27	GPIO4	Programmable input/output / Bluetooth coexistence	PD	In/out	VDDPST
26	GPIO5	Programmable input/output	PD	In/out	VDDPST
25	GPIO6	Programmable input/output	PD	In/out	VDDPST
WIFI radio interface					
40	BG_EXTR	RF BG reference	N/A		
2	RF_IN	RF auxiliary RX input	N/A		
4	RF_OUTP	RF port	N/A		
5	RF_OUTN	RF port	N/A		
PMU/SMPS					
17	VOUT_1P2	LDO 1.2V output	N/A	Output	
18	LDO_V15A	SMPS 1.5V input	N/A	Iutput	
19,22	DCDC_V33	SMPS 3.3V power supply	N/A	Input	
20	FB	SMPS control	N/A		

21	COMP	SMPS control	N/A		
23	PHASE	SMPS control	N/A		
Power supplies					
7,33	VDDPST	Digital I/O power supply	N/A	Input	
12,32	VDD	Digital core power supply	N/A	Input	
3,6	RF_V33A	RF 3.3V power supply	N/A	Input	
1,35, 38,39	RF _LDO	RF power supply	N/A	Input	
34	PLL_LDO	RF power supply	N/A	Input	
E-PAD	DVSS	Digital ground	N/A		

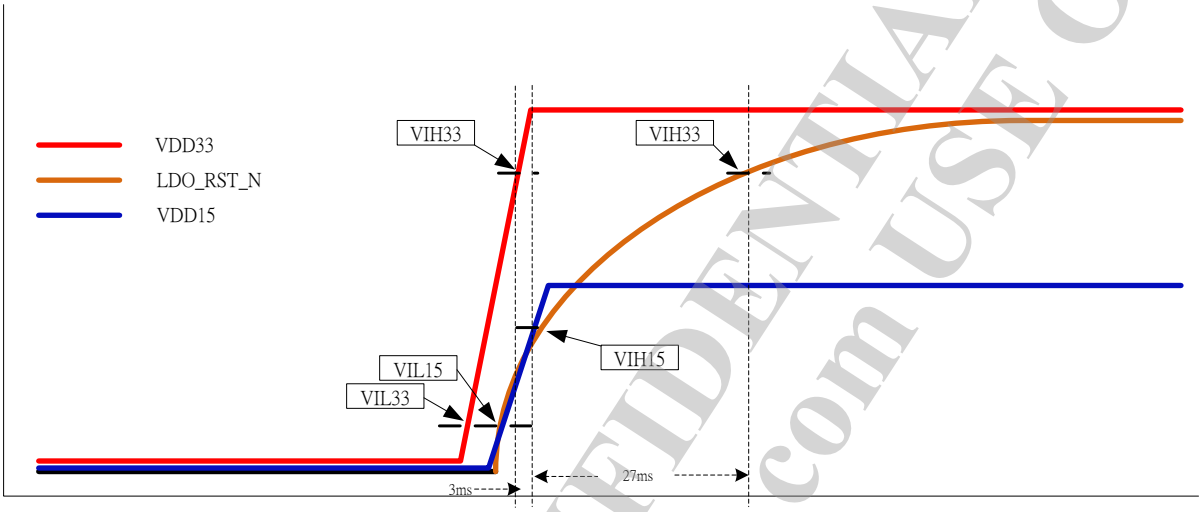
Table 1 Pin descriptions

2.3 Strapping option

QFN40	Pin Name	Pin description	Default PU/PD
8	EE_MISO	XTAL_20_SEL XTAL is 20MHz: Pull up XTAL is 40MHz: Pull down	PD
27	GPIO4	EXT_EE_SEL: Pull down	PD
25	GPIO6	CHIP_MODE[2]: Pull down	PD
10	EE_CLK	CHIP_MODE[1]: Pull down	PD
9	EE_MOSI	CHIP_MODE[0]: Pull up	PU

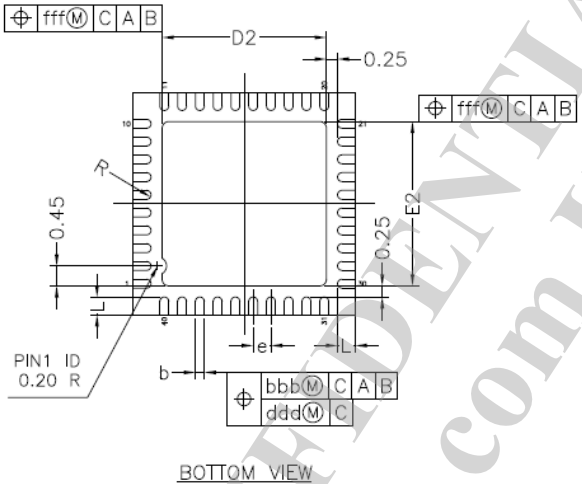
Table 2 Strapping option

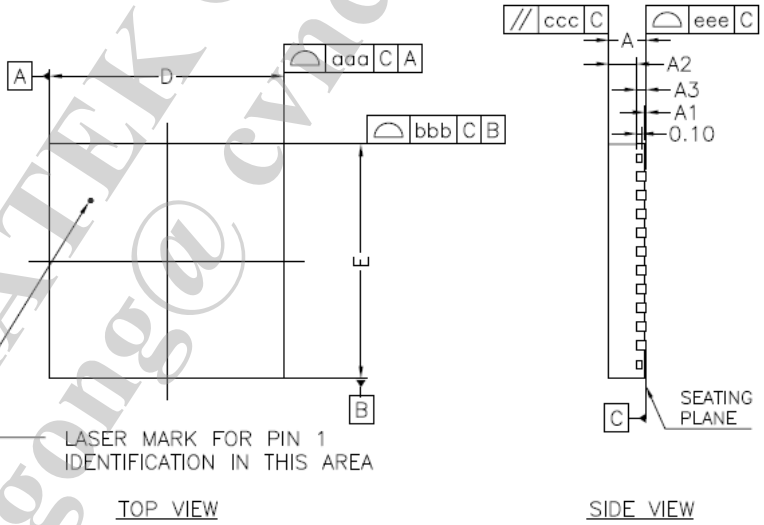
2.4 Power on sequence/reset

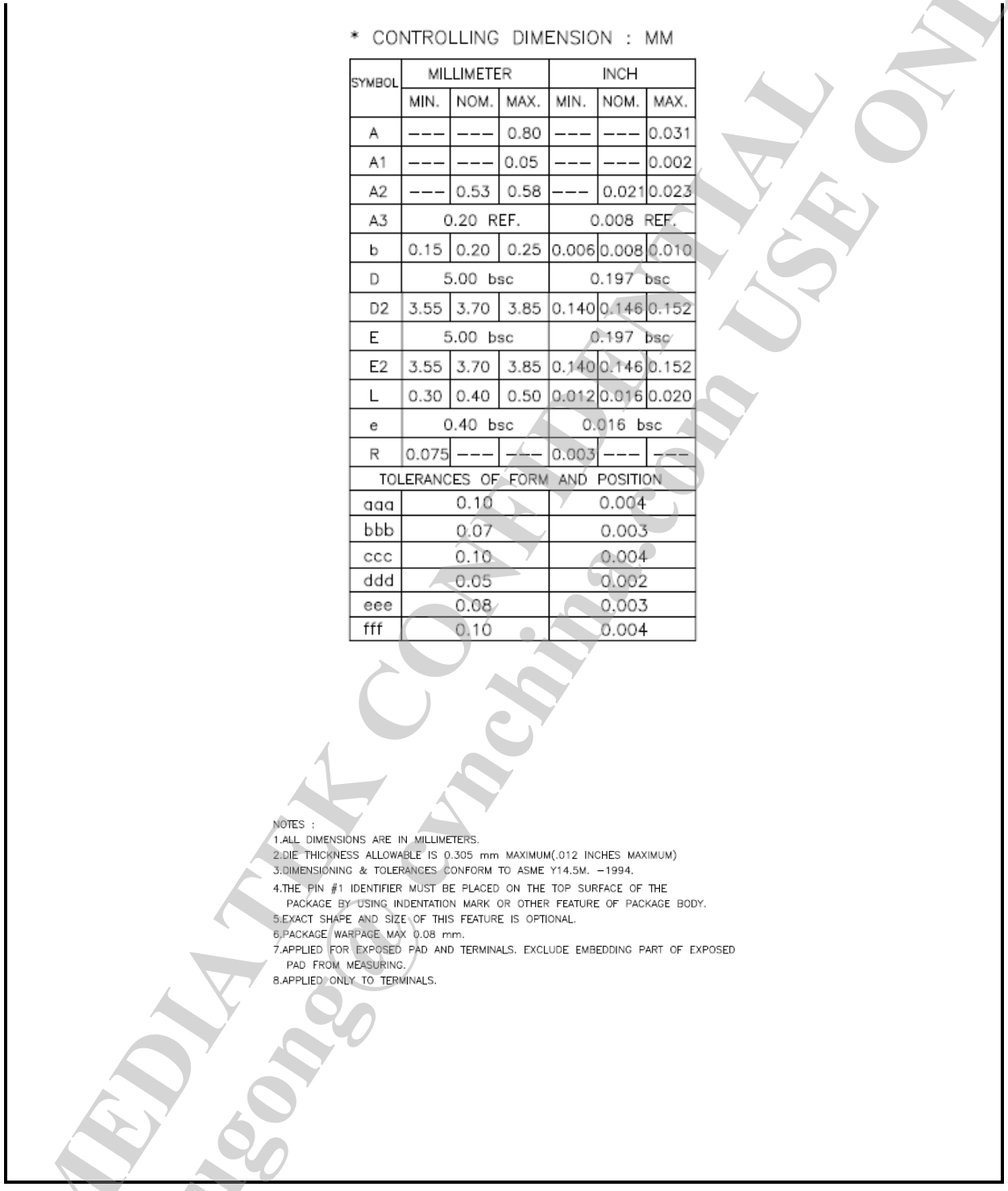


Note :
1. 3.3V need to be ready before 1.5V ready (>3ms)
2. VIH15 must be early than LDO_RST_N VIH33 ready (>27ms)

2.5 Package information







* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.80	---	---	0.031
A1	---	---	0.05	---	---	0.002
A2	---	0.53	0.58	---	0.021	0.023
A3	0.20 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	5.00 bsc			0.197 bsc		
D2	3.55	3.70	3.85	0.140	0.146	0.152
E	5.00 bsc			0.197 bsc		
E2	3.55	3.70	3.85	0.140	0.146	0.152
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 bsc			0.016 bsc		
R	0.075	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

Figure 3 Package outline drawing

2.6 Ordering Information

Part number	Package	Operational temperature range
MT7601UN/B	5x5x0.8 mm 40-QFN	-10~70°C

Table 3 Ordering information

2.7 TOP Marking Information


```
MT7601UN  : Part number
DDDD      : Date code
####      : Internal control code
BBBBBBB   : Lot number
```

Figure 4 Top marking

3 Electrical characteristics

3.1 Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.6	V
VDD12	1.2V Supply Voltage	-0.3 to 1.5	V
VDD15	1.6V Supply Voltage	-0.3 to 1.8	V
T_{STG}	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	2000	V

Table 4 Absolute maximum ratings

3.2 Recommended operating range

Symbol	Rating	MIN	TYP	MAX	Unit
VDD33	3.3V Supply Voltage	2.97	3.3	3.63	V
VDD12	1.2V Supply Voltage	1.14	1.2	1.26	V
VDD15	1.6V Supply Voltage	1.425	1.5	1.575	V
$T_{AMBIENT}$	Ambient Temperature	-10	-	70	°C

Table 5 Recommended operating range

3.3 DC characteristics

Symbol	Parameter	Conditions	MIN	MAX	Unit
V_{IL}	Input Low Voltage	LVTTL	-0.28	0.6	V
V_{IH}	Input High Voltage		2.0	3.63	V
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	LVTTL	0.68	1.36	V
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage		1.36	1.7	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 1.6~14 mA	-0.28	0.4	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 1.6~14 mA	2.4	VDD33+0.33	V
R_{PU}	Input Pull-Up Resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input Pull-Down Resistance	PU=low, PD=high	40	190	KΩ

Table 6 DC description

3.4 Thermal characteristics

Symbol	Description	Performance	
		TYP	Unit
P_D	Power Dissipation	1.45	W
T_A	Ambient Air Temperature	55	°C
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
Θ_{JA}	Junction to ambient temperature thermal resistance[1][2]	48.11	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	19.86	°C/W
Ψ_{Jt}	Junction to the package thermal resistance[3]	3.26	°C/W

Note:
[1] Air flow condition: Natural convection. 0.5m/s.
[2] PCB dimension 21mm x 11mm. 4-layer.
[3] 5mm x 5mm QFN40L package

Table 7 Thermal information

3.5 Current consumption

3.5.1 WLAN current consumption

Description	Performance	
	TYP	Unit
Sleep mode	1.1	mA
RX Active, HT40, MCS7, 2.4GHz	151	mA
RX Power saving, DTIM=1	15	mA
RX Listen	6	mA
TX HT40, MCS7 @15dBm, 2.4GHz	210	mA
TX CCK, 11Mbps @19dBm, 2.4GHz	242	mA

Note: All result is measured at the antenna port and VDD33 is 3.3V

Table 8 WLAN 2.4/5GHz Current Consumption

3.6 Wi-Fi RF specification

3.6.1 Wi-Fi 2.4GHz band RF receiver specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range		2412	-	2484	MHz
RX sensitivity	1 Mbps CCK	-	-98	-	dBm
	2 Mbps CCK	-	-95	-	dBm
	5.5 Mbps CCK	-	-93	-	dBm
	11 Mbps CCK	-	-89	-	dBm
RX sensitivity	6 Mbps OFDM	-	-91	-	dBm
	9 Mbps OFDM	-	-90	-	dBm
	12 Mbps OFDM	-	-89	-	dBm
	18 Mbps OFDM	-	-87	-	dBm
	24 Mbps OFDM	-	-84	-	dBm
	36 Mbps OFDM	-	-81	-	dBm
	48 Mbps OFDM	-	-76	-	dBm
	54 Mbps OFDM	-	-75	-	dBm
RX Sensitivity BW=20MHz Green Field 800ns Guard Interval Non-STBC	MCS 0	-	-91	-	dBm
	MCS 1	-	-89	-	dBm
	MCS 2	-	-87	-	dBm
	MCS 3	-	-84	-	dBm
	MCS 4	-	-81	-	dBm
	MCS 5	-	-77	-	dBm
	MCS 6	-	-75	-	dBm
	MCS 7	-	-74	-	dBm
RX Sensitivity BW=40MHz Green Field 800ns Guard Interval Non-STBC	MCS 0	-	-89	-	dBm
	MCS 1	-	-86	-	dBm
	MCS 2	-	-84	-	dBm
	MCS 3	-	-81	-	dBm
	MCS 4	-	-78	-	dBm
	MCS 5	-	-74	-	dBm
	MCS 6	-	-72	-	dBm
	MCS 7	-	-71	-	dBm
Maximum Receive Level	11 Mbps CCK	-	0	-	dBm
	6 Mbps OFDM	-	0	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-14	-	dBm
Receive Adjacent Channel Rejection	1 Mbps CCK	-	40	-	dBm
	11 Mbps CCK	-	40	-	dBm
	6 Mbps OFDM	-	37	-	dBm
	54 Mbps OFDM	-	25	-	dBm
Receive Adjacent Channel Rejection (HT20)	MCS 0	-	37	-	dBm
	MCS 7	-	24	-	dBm
Receive Adjacent Channel Rejection (HT40)	MCS 0	-	34	-	dBm
	MCS 7	-	20	-	dBm

Table 9 2.4GHz RF receiver specifications

3.6.2 Wi-Fi 2.4GHz band RF transmitter specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range		2412	-	2484	MHz
Output power	1~11 Mbps CCK	-	20	-	dBm
	6 Mbps OFDM	-	20	-	dBm
	54 Mbps OFDM	-	18	-	dBm
	HT20/HT40, MCS 0	-	20	-	dBm
	HT20/HT40, MCS 7	-	17	-	dBm
TSSI accuracy	Output power variation for close loop control	-1.5	-	1.5	dB
Carrier suppression		-	-	-30	dBc
Harmonic Output Power	2nd Harmonic	-	-45	-	dBm/MHz
	3nd Harmonic	-	-45	-	dBm/MHz

Table 10 2.4GHz RF transmitter specifications

3.7 PMU electrical characteristics

PARAMETER	CONDITIONS	PERFORMANCE			
		MIN	TYP	MAX	Unit
Switching regulator					
Input voltage		2.97	3.3	3.63	V
Output voltage	Default voltage setting in the programmable range[1]	1.4	1.5	1.6	V
Output current		-	-	300	mA
Quiescent current		-	-	3.5	mA
Line regulation	3.63V input voltage range @ no load	-	-	1	%
Load regulation	1mA to 300mA load current	-	-	0.05	mV/mA
Efficiency	300mA load current	-	80	-	%
Over-current Shutdown	Threshold	-	600	-	mA
Digital LDO					
Input voltage		1.4	1.5	1.6	V
Output voltage		1.08	1.2	1.32	V
Output current		-	-	200	mA
Quiescent current	No load	-	10	-	uA

Table 11 PMU electrical characteristics

4 Functional specification

4.1 System

4.1.1 Power Management Unit

Power Management Unit (PMU) contains Low Drop-out Regulators (LDOs), highly efficient switching regulator, and the reference band-gap circuit. The circuits are optimized for quiescent current, drop-out voltage, line/load regulation, ripple rejection, and output noise.

Only one power source is required for MT7601U, The 3.3V power source is directly supplied to the switching regulator, digital I/Os, USB PHY, and RF related circuit. It's converted to 1.5V by the switching regulator for low voltage circuits. The built-in digital LDOs and RF LDOs converts 1.5V to 1.2V for digital, RF, PCIe PHY, and BBPLL core circuits.

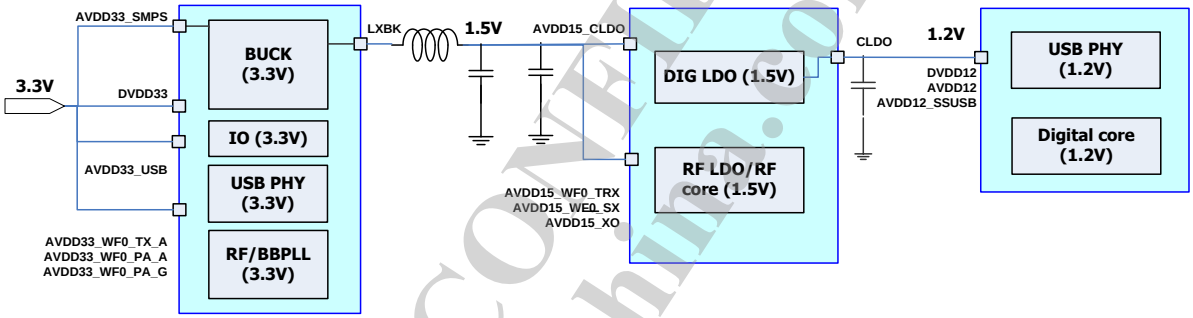


Figure 5 PMU block diagram (switching regulator enabled)

The switching regulator integrates the power MOS, and can provide 300mA output current driving. It has output current limiting protection to prevent from circuit damage due to abnormal usage. It can reach 80% efficiency when operating at full loading. When the system operates in low power mode, it's turned off by the firmware to reduce the power consumption. It also has low noise spread spectrum operation to reduce the switching noise and the soft-start function.

4.1.2 EFUSE OTP

MT7601U uses embedded Efuse to store device specific configuration information such as MAC addresses, USB enumeration information, and power control settings.

Below illustrated the major fields defined in the Efuse.

- MAC addresses.
- USB vendor/product IDs and descriptors.
- Wi-Fi country code.
- TSSI parameters, TX power level.
- NIC configuration: RF front-end configuration, baseband configuration.

4.2 Host interface architecture

4.2.1 USB

MT7601U supports the Universal Serial Bus Specification, Revision v2.0 (USB v2.0 specification). It supports high-speed, and full-speed specification, suspend/resume signaling, as well as remote wake-up signaling.

It offers 6 OUT Endpoints (Endpoint 0x04~0x09) and 2 IN Endpoints (Endpoint 0x84~0x85) for Wi-Fi data transmission with flexible queue management.
Data aggregation is used to enhance the throughput over USB interface.

4.3 MCU Subsystem

MCU subsystem contains the MCU, internal RAM/ROM.
MT7601U uses a 32-bit RISC MCU for low power consumption and efficient use of internal memory.
The MCU controls the host interface, USB protocol, and controls the Wi-Fi hardware.

ESD CAUTION

MT7601U is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT7601U is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.