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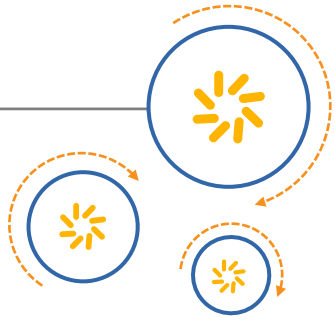

QCA8075 Five-Port 10/100/1000 Mbps Ethernet Transceiver

Preliminary Device Specification

80-Y9112-1 Rev. C

September 1, 2015

Questions or comments: https://createpoint.qti.qualcomm.com/

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Revision history

Revision	Date	Description
A	January 2015	Initial release, pre-ES.
B	April 2015	Added to this document revision ■ Section 1.3.13 PSGMII ■ Section 1.3.14 Power-on sequence ■ Section 2.2 Power-on strapping ■ Chapter 3 Electrical Characteristics ■ Chapter 6 PCB Mounting Guidelines Updated in this document revision ■ Section 1.1 Document overview: Updated documentation descriptions ■ Section 1.2 QCA8075 device description: Updated device descriptions ■ Section 1.3.3 Loopback modes: Updated remote PHY loopback diagrams ■ Section 1.3.6 Fiber mode support: Updated 100BASE-FX and 1000BASE-X remote fault indication descriptions ■ Section 1.3.8 Green ETHOS feature: Updated power saving and hibernation descriptions ■ Section 1.3.11 LED interface: Updated LED interface descriptions ■ Section 2.1 I/O parameter definitions: Updated MDC, INTn and INTn_WOL pin descriptions
C	September 2015	Chapter 1.1 Document overview: Updated primary QCA8075 documentation Chapter 2.1 I/O parameter definitions: Updated B23 and B39 Chapter 2.2 Power-on strapping: Updated LED_1000_2, LED_100_3, and LED_1000_3 Chapter 4.2 Part marking: Updated part marking Chapter 4.3 Device ordering information: Updated ordering numbers Chapter 4.5 Thermal characteristics: Added θ_{JB} and θ_{JC}

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1 Introduction

1.1 Document overview

Technical information for the QCA8075 device is primarily covered by the documents listed in Table 1-1. Each is a self-contained document, but a thorough understanding of the device and its applications requires familiarization with all of them. The device description in Section 1.3 is a good place to start.

Table 1-1 Primary QCA8075 documentation

Document No.	Title/Description
80-Y9112-1 (this document)	*QCA8075 Five-Port 10/100/1000 Mbps Ethernet Transceiver Preliminary Device Specification* Conveys all QCA8075 IC electrical and mechanical specifications. Additional material includes pin assignments; shipping, storage, and handling instructions; PCB mounting guidelines; and part reliability. This document can be used by company purchasing departments to facilitate procurement.
80-Y9112-2	*QCA8075 Five-Port 10/100/1000 Mbps Ethernet Transceiver Hardware Programming Reference* Describes how to use QCA8075 in different working modes and how to configure QCA8075 for the different function tests.
80-Y9112-3	*QCA8075 Device Revision Guide* Provides a history of device revisions and exceptions to the device specification; explains how to identify various device revisions; presents known issues (or bugs) for each revision and work-around to them; lists performance specification changes between each revision of the device specification

The QCA8075 Five-Port 10/100/1000 Mbps Ethernet Transceiver Device Specification is organized as follows:

Chapter 1 Gives a high-level functional description of the device, lists the device features, and defines marking conventions, terms, and acronyms used throughout this document.

Chapter 2 Defines the device pin assignments.

Chapter 3 Defines the device electrical characteristics, including absolute maximum ratings and recommended operating conditions.

Chapter 4 Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.

Chapter 5 Describes carrier, storage and handing information of the QCA8075 device.

Chapter 6 Presents procedures and specifications for mounting the QCA8075 device onto printed circuit boards (PCBs).

1.2 QCA8075 device description

The QCA8075 Ethernet transceiver is a 5-port, 10/100/1000 Mbps tri-speed Ethernet PHY. The QCA8075 Ethernet transceiver provides physical layer functions for half/full-duplex 10BASE-Te, 100BASE-TX, and full-duplex 1000BASE-T Ethernet to transmit and receive data over standard Category 5 (CAT-5) unshielded twisted pair cable.

The QCA8075 includes two SerDes. One can be configured to PSGMII or QSGMII for connection with MAC. The other can be configured to SGMII for connection with MAC or fiber port combined with copper port4 to form a combo port.

The QCA8075 Ethernet transceiver integrates Green ETHOS® power saving technologies which significantly save power in both active operation and idle condition. Green ETHOS power saving schemes include ultra-low power in cable unplugged mode or port power down mode, as well as automatically optimized power saving based on cable length. The QCA8075 Ethernet transceiver supports standard IEEE 802.3az Energy Efficient Ethernet (EEE) and furthermore the Wake-on-LAN (WoL) feature to manage and regulate total system power requirements.

The key features of the IEEE 802.3az standard include:

- 10BASE-Te: Reduced transmit amplitude
- 100BASE-TX and 1000BASE-T: Low Power Idle (LPI) mode to turn off unused analog and digital blocks to save power when data traffic is idle

The QCA8075 Ethernet transceiver embeds Cable Diagnostics Test (CDT) technology for measuring cable length, detecting the cable status, and identifying remote and local PHY malfunctions, bad or marginal patch cord segments or connectors.

The QCA8075 Ethernet transceiver requires only a single 3.3 V power supply. Embedded regulators are used to generate other required voltages.

1.3 Product features

- Supports three working modes with power-on strapping configuration:
  - Five 1000BASE-T/100BASE-TX/10BASE-Te ports with PSGMII to MAC
  - Four 1000BASE-T/100BASE-TX/10BASE-Te ports and one combo port (fiber/copper) with PSGMII to MAC
  - Five 1000BASE-T/100BASE-TX/10BASE-Te ports with QSGMII and SGMII to MAC
- The combo port supports auto media detection with programmable priority.
- The fiber port supports 1000BASE-X/100BASE-FX.

- Management interface (MDIO) supports broadcast write.
- CRC checker and packet counter
- Green ETHOS® power saving modes:
  - Automatic power saving at media disconnected state
  - Automatic power saving per cable length
  - Software power down
- IEEE 802.3az EEE
- Wake-on-LAN (WoL) to detect magic packet and notify the sleeping system to wake up
- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Robust Contact Electro-Static Discharge (ESD) protection without external protection circuit
- Robust Lightening Surge performance without external protection circuit
- Robust operation over up to 140 meters of CAT5e cable
- Automatic Channel Swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- IEEE 802.3u compliant auto-negotiation
- Jumbo frame support up to 9 KB (full-duplex)
- Management interface supports 1.5/1.8/2.5/3.3 V I/O voltage.
- 25 MHz single-ended clock input
- Multiple loopback modes for diagnostics
- Cable Diagnostic Test (CDT)
- Single power supply: 3.3 V, optional for internal switch regulator or external regulator for core voltage
- 9 mm × 9 mm, 108-pin DR-QFN package
- Industry temperature option available
- Heatsink-free design for commercial temperature part

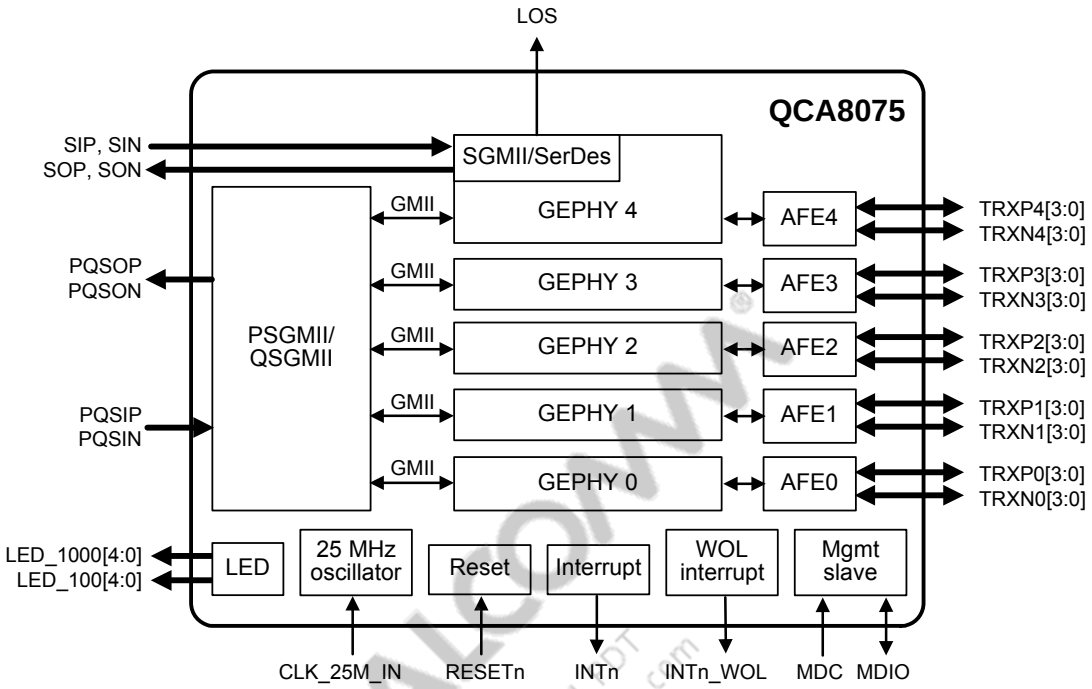


Figure 1-1 QCA8075 functional block diagram

1.3.1 Typical applications

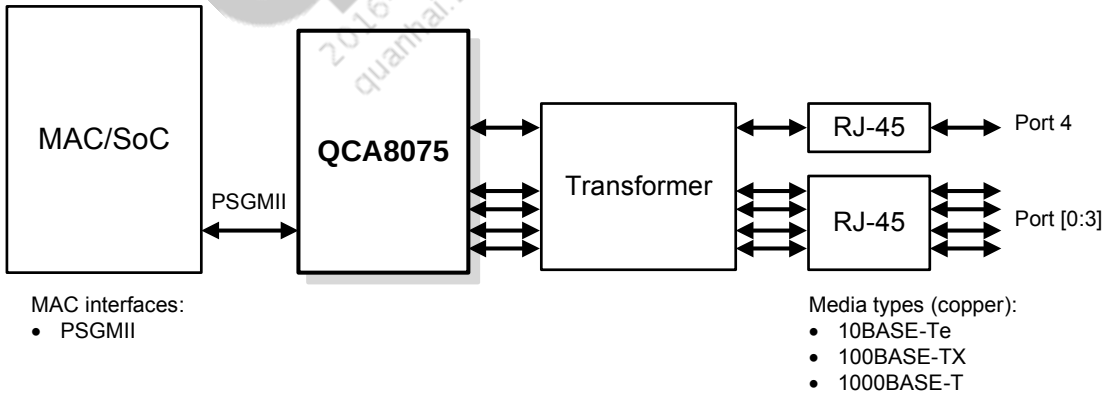


Figure 1-2 PSGMII application: 5 copper ports

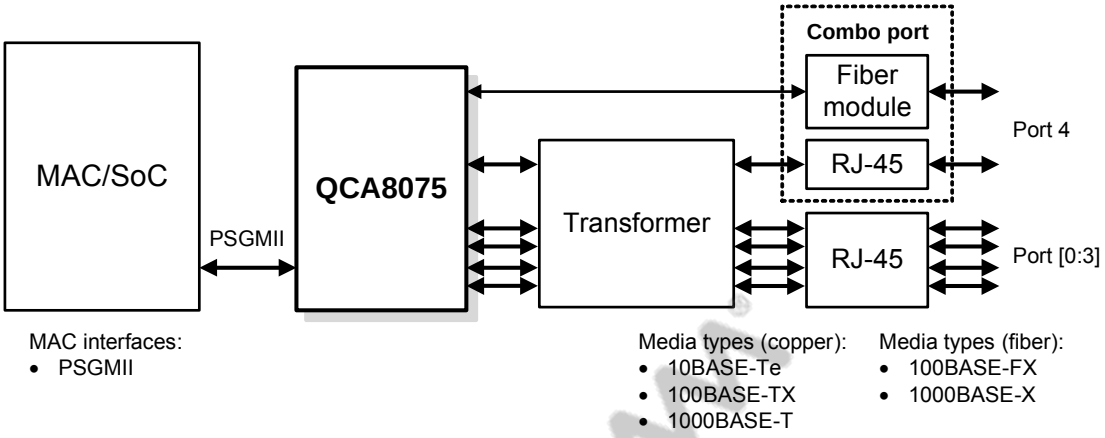


Figure 1-3 PSGMII application: 4 copper ports and 1 combo port

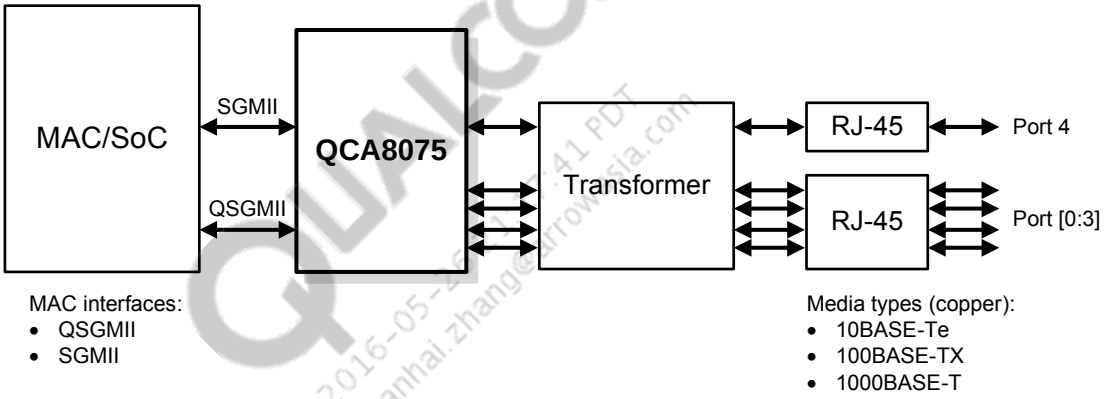


Figure 1-4 QSGMII + SGMII application: 5 copper ports

1.3.2 Receive functions

Decoder modes

Table 1-2 lists the receive function decoder modes.

Table 1-2 Receive function decoder mode

Mode	Description
1000BASE-T	In 1000BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately and data is output to the MAC interfaces.
100BASE-TX	In 100BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and decoded to 4-bit data by 5B/4B. This output runs to the MII receive data pins after data stream delimiters have been translated.
10BASE-Te	In 10BASE-Te mode, the recovered 10BASE-Te signal is decoded from Manchester and then aligned.

Analog-to-Digital converter

Each Rx channel includes an advanced high speed ADC with high resolution for better Signal-to-Noise Ratio (SNR) and lower error rates.

Echo canceller

Because hybrid circuit is used to transmit and receive simultaneously on each pair, echo occurs when the transmitter is not perfectly matched to the line. Connector or cable imperfections, such as patch panel discontinuity and variations in cable impedance along the twisted pair cable, can also result in drastic SNR degradation on the Rx signal.

The adaptive digital echo canceller is used to compensate for the varied channel conditions that result in SNR degradation on the Rx signal.

NEXT canceller

The 1000BASE-T physical layer uses all four twisted pairs to transmit data which incurs significant high frequency crosstalk occurs between adjacent pairs.

Three parallel NEXT cancellers are thus integrated on each Rx channel to cancel high frequency crosstalk by subtracting an estimate noise signals from the equalizer output.

Baseline wander canceller

Baseline wander occurs on Ethernet links AC-coupled to the transceiver. When the AC-coupling cannot maintain voltage levels for a specific time, the transmitted pulses are distorted which results in erroneous sampled values for affected pulses.

The baseline wander cancellation circuit continuously monitors and compensates for this issue, minimizing the impact of DC baseline shift on the overall error rate.

Digital adaptive equalizer

The digital adaptive equalizer, using a combination of Feedforward Equalizer (FFE) and Decision Feedback Equalizer (DFE), removes inter-symbol interference at the receiver by filtering unequalized signals from ADC output for optimized SNR.

Auto-negotiation

The auto-negotiation function for 10BASE-Te/100BASE-TX/1000BASE-T copper complies with IEEE 802.3 clauses 28 and 40.

Auto-negotiation provides a mechanism to exchange information between a pair of link partners to choose the optimized mode of operation in terms of speed, duplex modes, and master/slave preference. Auto-negotiation is initiated upon any of the following scenarios:

- Power-on reset
- Hardware reset
- Software reset
- Auto-negotiation restart

- Transition from power-down to power-up
- Link down

When auto-negotiation is disabled, the operation speed mode can be manually selected by register.

In 10BASE-Te/100BASE-TX, when one end disables auto-negotiation (force mode) and the other end enables auto-negotiation (advertise half-duplex), the link can be established and the end with auto-negotiation enabled works in half-duplex mode. Therefore, when the end in force mode is in half-duplex mode, the information transmission between the two link partners works normally; when the end in force mode is in full-duplex mode, mismatch occurs between the two link partners. The link cannot be established in 1000BASE-T under similar situation.

SmartSpeed

The SmartSpeed function is an enhanced auto-negotiation feature to allow automatic speed downgrade according to cabling conditions. When SmartSpeed is enabled and the failed link attempts reaches the configured number of trials, the QCA8075 automatically downgrades the highest advertised speed to the next lower speed, that is, from 1000 Mbps to 100 Mbps and from 100 Mbps to 10 Mbps.

Automatic MDI/MDIX crossover

During auto-negotiation, the automatic MDI/MDIX crossover function automatically determines and sets the required MDI configuration, eliminating the need for external crossover cable.

The algorithm described in IEEE 802.3 clause 40.4.4 ensures that only one device performs the required crossover when the remote device implements automatic MDI crossover as well.

For 1000BASE-T, swap can happen only between pair 0 and 1, or pair 2 and 3. See Table 1-3.

Table 1-3 Supported MDI pair combinations

0 (1, 2)	1 (3, 6)	2 (4, 5)	3 (7, 8)	Normal MDI
1 (3, 6)	0 (1, 2)	3 (7, 8)	2 (4, 5)	Normal MDI-X
0 (1, 2)	1 (3, 6)	3 (7, 8)	2 (4, 5)	Normal MDI with pair swap on 2 and 3 pair
1 (3, 6)	0 (1, 2)	2 (4, 5)	3 (7, 8)	Normal MDI-X with pair swap on 2 and 3 pair

Polarity correction

If cable polarity is incorrectly wired, the polarity correction function automatically corrects polarity errors on the receive pairs in 1000BASE-T, 100BASE-TX, and 10BASE-Te modes.

1.3.3 Loopback modes

The QCA8075 Ethernet transceiver supports the following loopback modes:

Digital loopback

Loops transmitted data back to the receiver using digital circuit in the QCA8075 device.

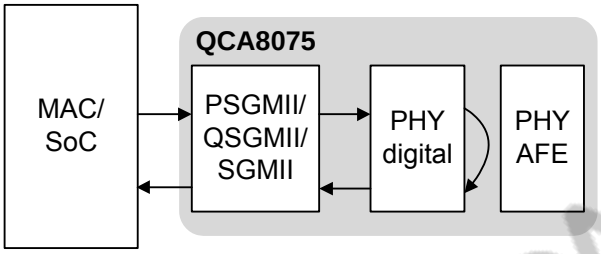


Figure 1-5 Digital loopback, copper port 0 to 4

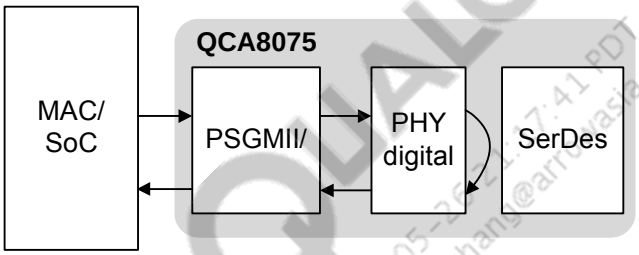


Figure 1-6 Digital loopback, fiber port 4

External cable loopback

Loops PSGMII/QSGMII/SGMII Tx back to Rx through the complete digital and analog path and an external cable. This is used to test the digital data paths and the analog circuits.

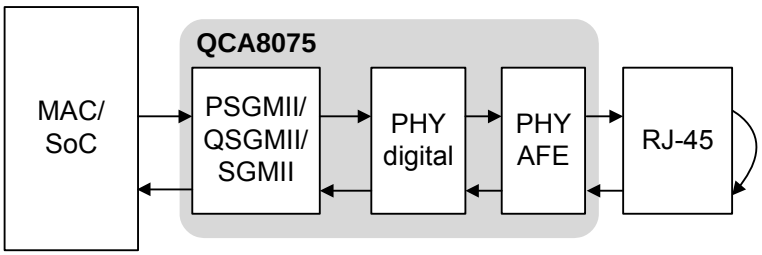


Figure 1-7 External cable loopback, copper port 0 to 4

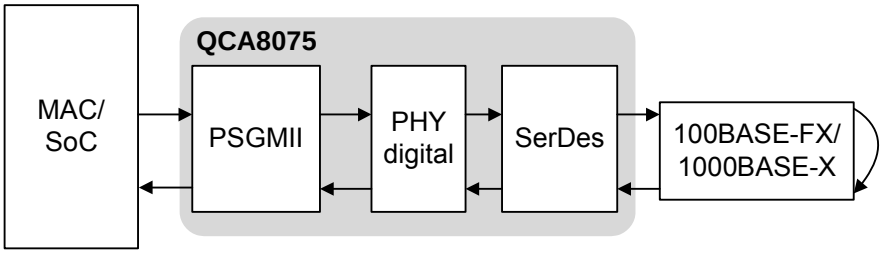


Figure 1-8 External cable loopback, fiber port 4

Remote PHY loopback

Loops MDI Rx back to MDI Tx to have the remote link partner detect the connectivity in the loop.

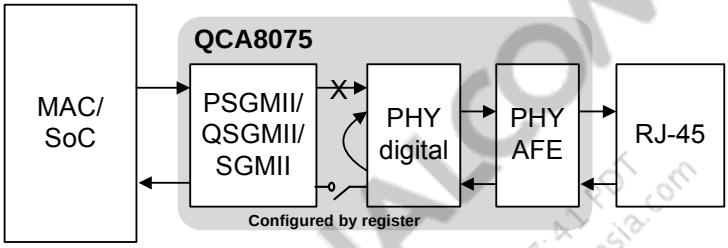


Figure 1-9 Remote PHY loopback, copper port 0 to 4

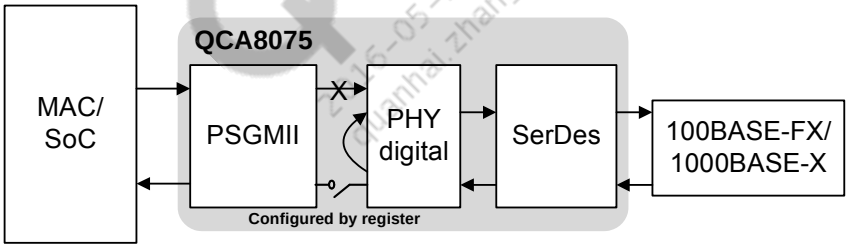


Figure 1-10 Remote PHY loopback, fiber port 4

1.3.4 Cable diagnostic test

The Cable Diagnostic Test (CDT) feature uses Time Domain Reflectometry (TDR) technology to identify malfunctions in remote and local PHYs, as well as bad or marginal cable, patch cord segments and connectors.

The following are the problems that can be diagnosed using CDT:

- Open
- Short
- Cable impedance mismatch
- Bad connector
- Termination mismatch

- Bad magnetic

CDT can be performed when no link partner is present. DSP algorithm is used to measure the cable length when the link partner is performing auto-negotiation.

1.3.5 CRC checker

The CRC checker is used to perform CRC check for each ingress and egress packet at PHY. The CRC checker maintains counters for correct and corrupted packets.

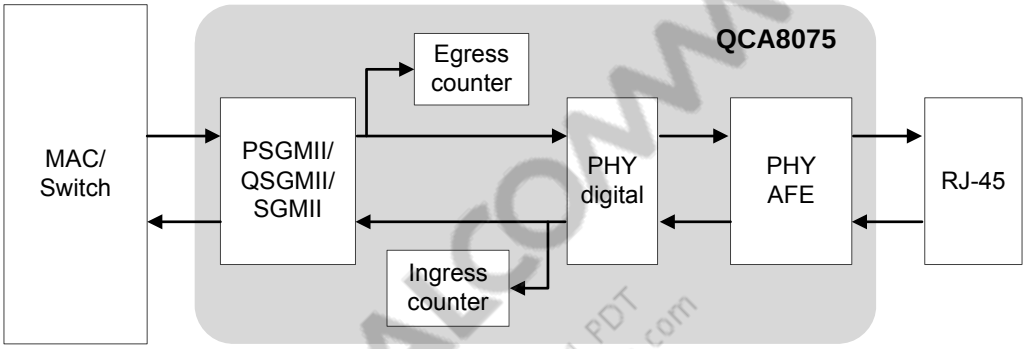


Figure 1-11 CRC checker, copper mode

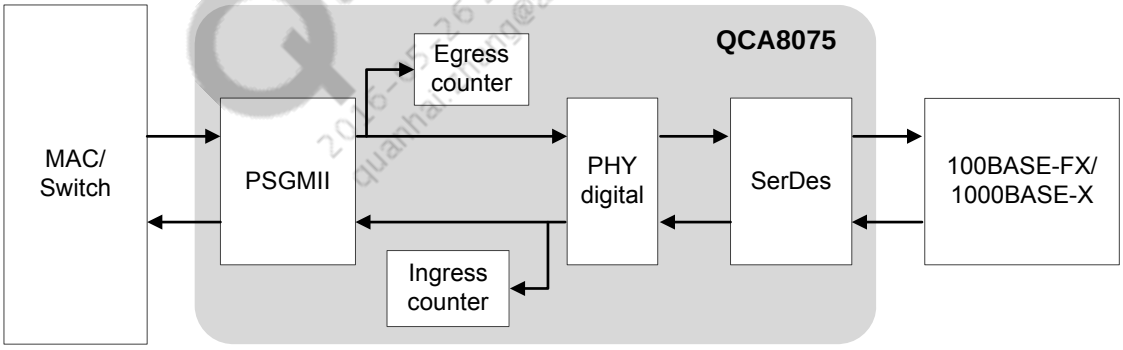


Figure 1-12 CRC checker, fiber mode

1.3.6 Fiber mode support

The QCA8075 transceiver provides additional IEEE 1000BASE-X and 100BASE-FX support through integrated SerDes for fiber applications. The QCA8075 also supports IEEE 802.3 remote fault indication and fault propagation in fiber application.

Unidirectional ability

The QCA8075 transceiver can encode and transmit data from MII/GMII regardless of whether the PHY has determined that a valid link has been established. This feature is usually enabled in carrier products (disabled by default). It is supported only when auto-negotiation is disabled and the PHY operates in full-duplex mode.

Far-End Fault: 100BASE-FX remote fault indication

Auto-negotiation provides a remote fault capability useful for detection of asymmetric link failures; i.e., channel error conditions detected by the far-end station but not the near-end station. Since auto-negotiation is not specified for 100BASE-FX, auto-negotiation's remote fault capability is unavailable. A remote fault capability for 100BASE-FX is particularly useful due to this medium's applicability over longer distances (making end-station checking inconvenient).

For these reasons, 100BASE-FX provides an optional Far-End Fault facility.

First, at local station, the loss of a receive signal (link) causes the transmitter to send a special pattern of data indicating that a fault has occurred. Eighty-four "1"s followed by a single "0" are sent three times, in-band, for detection by the remote station. This message does not meet the 100BASE-FX carrier sense criteria, thus it is not interpreted as normal traffic. If the remote station supports remote fault indication, the link is dropped; if not, the special data pattern is ignored.

A far-end fault bit indicates whether a remote fault pattern is received from the remote station. In case of a detected fault, both ends of the link can be notified of the failure, which is particularly useful given the distances of the fiber links.

The far end fault feature is support only when unidirectional ability is disabled.

1000BASE-X remote fault indication

Sensing of faults in a device as well as subsequent association of faults with the Remote Fault function encodings is optional in IEEE 802.3 and QCA8075 can support this feature. Remote Fault (RF) is encoded in bits D12 and D13 of the Base Page during the auto-negotiation of 1000BASE-X. The default value is 00. Remote Fault provides a standard transport mechanism for the transmission of simple fault and error information. The Remote Fault function indicates to the link partner that a fault or error condition has occurred. The two Remote Fault bits, RF1 and RF2, are encoded as specified in Table 1-4.

Table 1-4 Remote Fault encoding

RF1	RF2	Description
0	0	No error, link OK (default)
1	0	Link_Failure
1	1	Auto-negotiation_Error

The QCA8075 could indicate it has sensed a fault to its link partner by setting a nonzero Remote Fault encoding in its Base Page and renegotiating.

The Remote Fault encoding remains set until after the auto-negotiation process transitions into IDLE_DETECT state with the Base Page, at which time the Remote Fault encoding is reset to 00. On receipt of a Base Page with a nonzero Remote Fault encoding, QCA8075 will set the Remote Fault bit in the Status register (MII fiber page register 0x1[4]) to logic one.

1.3.7 Management interface

The IEEE 802.3u clause 22-compliant management interface provides access to the internal registers of the QCA8075 transceiver via the MDC and MDIO pins. MDC is the management data

clock input from the management entity (MAC or SoC). MDIO is the management data input/output that runs synchronously to MDC.

The management interface supports broadcast write operation. When broadcast write is enabled, write commands with broadcast address are accepted by all the ports simultaneously. Broadcast write is disabled by default.

The management frame consists of 32-bit preamble, 2-bit start of frame, 2-bit operation code, 5-bit PHY device address, 5-bit PHY register address, 2-bit turn around, 16-bit data field and at least 1-bit idle. See Table 1-5. The frame bits are transmitted in sequence from PRE to IDEL and each bit is triggered on the rising edge of MDC.

Table 1-5 Management interface frame fields

	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Table 1-6 Management interface field definitions

Field	Definition
PRE	A sequence of 32 contiguous single logic bits on MDIO with corresponding cycles on MDC to provide PHY with a pattern for synchronization.
ST	2-bit start of frame
OP	2-bit operation code. 10 = read transaction, 01 = write transaction
PHYAD	5-bit PHY device address. The bits[2:0] in the PHY address are configured by power-on strapping, thus eight PHYs can be connected to a single management interface. The PHYs connected to the same bus have unique PHY addresses. The first PHY address bit transmitted and received is the MSB of the address.
REGAD	5-bit register address. The 5-bit register address allows 32 registers to be addressed at each PHY. The first register address bit transmitted and received is the MSB of the address.
TA	2-bit field to avoid contention during a read operation. In read operation, both MAC and PHY are at high-impedance state for the first bit time. The PHY drives a zero during the second bit time of the turnaround. In write operation, the MAC must drive 10.
DATA	16-bit data from accessed register. MSB is transmitted first.
IDLE	High-impedance without driving state of the MDIO. At least one clocked idle state is required between frames.

1.3.8 Green ETHOS feature

Low power mode

The QCA8075 transceiver enters low power mode when software sets a register bit (POWER_ DOWN). In this mode, the QCA8075 transceiver ignores all signals on the MAC interface except the MDC/MDIO, and does not response to any activity on the media side. The QCA8075 transceiver cannot exit the low power mode until the register bit is cleared.

Power saving based on cable length

The QCA8075 supports 1000BASE-T power saving based on cable length. The power saving is done via adjusting analog MDI driver's amplitude and bias current.

Hibernation mode

Hibernation mode yields very low power consumption in contrast with normal operation mode. The QCA8075 support both copper and fiber hibernation. When copper cable is unplugged, the copper port enters into hibernation mode in about 10 seconds; when fiber cable is unplugged, the fiber port enters into hibernation mode in about 1 second. When cable is reconnected, the port wakes up to restore normal function.

1.3.9 IEEE 802.3az

IEEE 802.3az provides a mechanism to reduce power consumption between data packets bursts.

It supports two operating states: Active state for normal data transfer and Low Power Idle (LPI) state for power saving between the data packet bursts.

The link partners enter LPI state by sending short refresh signals to maintain the link. In the low-power state, PHY shuts down most of the analog and digital blocks. In Ethernet network where systems stay in non-burst mode most of time, therefore over 90% power can be saved with LPI enabled.

During link establishment, both link partners exchange information through auto-negotiation to determine if both parties are LPI-capable. LPI is supported for the following scenarios:

- 100BASE-TX EEE supports asymmetrical operation that allows Tx or Rx to enter the LPI mode independently.
- 1000BASE-T EEE requires symmetrical operation therefore both Tx and Rx must enter the LPI mode simultaneously.

IEEE 802.3az includes the following link states:

- Active: Act in regular mode for transmitting or receiving data.
- Sleep: Send specific signal to inform remote link partner of entering low-power state.
- Quiet: No signal transmitted on media. Most of the analog and digital blocks are shut down.
- Refresh: Periodically send specific training signal to maintain timing recovery and equalizer coefficients.
- Wake: Send specific wake-up signal to remote link partner to inform of entering Active state.

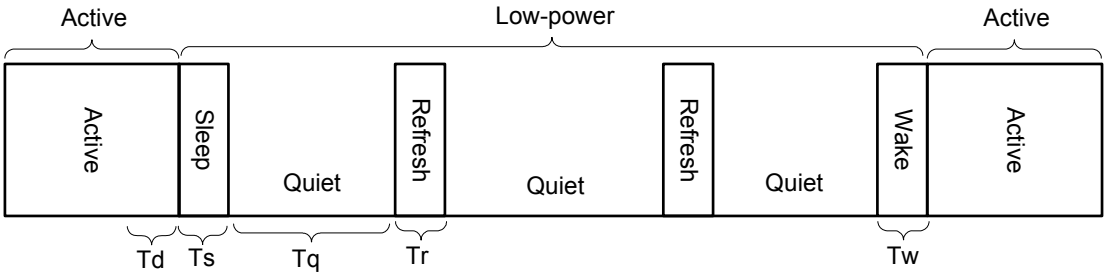


Figure 1-13 802.3az LPI operating mode

1. Td: Decision time, higher-layer control policy timing
2. Ts: Sleep time, Min. duration Sleep symbols sent before going to Quiet
3. Tq: Quiet duration, Max. duration PHY remains Quiet before Refresh
4. Tr: Refresh duration, Min. duration PHY sends Refresh symbols
5. Tw: Wake time, Max. period to permit the receiving system to wake up

1.3.10 Wake-on-LAN

Wake-on-LAN (WoL) is a mechanism to manage and regulate the total network power consumption. The QCA8075 transceiver supports automatic detection of a specific frame and notification via dedicated hardware interrupt pin. The specific frame contains a specific data sequence located anywhere inside the packet. The data sequence consists of 6 bytes of consecutive 1 (0xFFFFFFFFFFFF), followed by 16 repetitions of the MAC address of the computer to be waken up. See Figure 1-14.

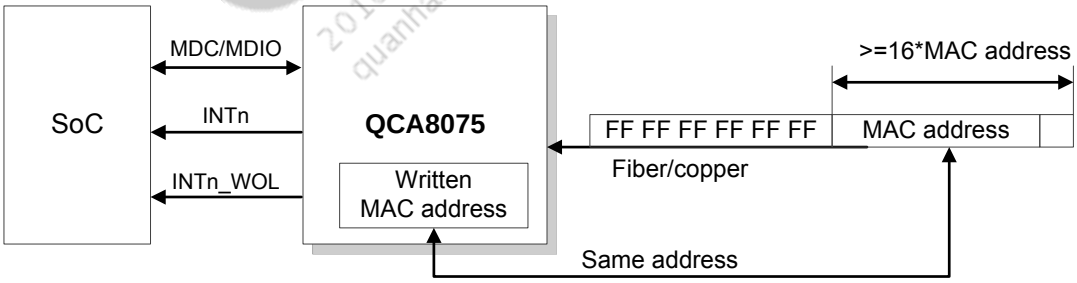


Figure 1-14 WoL application structure

1.3.11 LED interface

The QCA8075 transceiver includes ten 2.7 V status LED pins, two for each port. Each LED pin can be programmed to force on/off/blink and also can be programmed to indicate port status such as link, speed, active and collision. See Table 1-7 and Table 1-8 for default LED status.

Table 1-7 Default LED status for copper ports

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_100_n	On	Blink	On	Blink	Off	Off
LED_1000_n	Off	Off	Off	Off	On	Blink
1. On = active; Off = inactive 2. n = 0 to 4						

Table 1-8 Default LED status for fiber port

Symbol	100M link	100M active	1000M link	1000M active
LED_100_4	On	Blink	Off	Off
LED_1000_4	Off	Off	On	Blink
1. On = active; Off = inactive				

The active status of LED_100_n and LED_1000_n depends on external pull-up or pull-down. When the LED pin is externally pulled up, it is strapped high and active low; when the LED pin is externally pulled down, it is strapped low and active high.

1.3.12 Power supplies

The QCA8075 transceiver requires only one external 3.3 V power supply. The following power rails are generated by internal regulators.

- 2.7 V
- 1.0 V
- 1.2 V
- 1.5/1.8 V

1.3.13 PSGMII

Penta-Serial Gigabit Media Independent Interface (PSGMII) uses two data signals in each direction to transport network data and link information for five 10/100/1000 Mbps ports between PHY and MAC. The link operates at 6.25 Gbps using CDR technology to recover the clock from the PSGMII input data. Due to the high operation speed, each signal implemented as a differential pair to ensure signal integrity by minimizing system noise.

The PSGMII is nature extension of QSGMII and uses the same mechanism for channel mark as QSGMII. The QCA8075 includes one PSGMII to support five Gigabit Ethernet ports. The PSGMII integrates 100 Ohm differential termination resistors on both transmitter and receiver sides.

PSGMII uses CML driver with 0.6 V (typical) differential swing and 0.9 V (typical) common mode voltage to support both AC and DC coupled connection between PHY and MAC. When both Tx and Rx ends of the PSGMII link meet common mode voltage requirements, DC coupling

is recommended for reduced system costs and complexity as well as improved signal integrity. Otherwise, AC coupling connection is used. Typically, 0.1 µF or 0.01 µF capacitors are used.

1.3.14 Power-on sequence

The RESETn signal must be asserted and kept low for at least 1ms after 3.3V power and reference clock signals become stable. 3.3V rising duration from 10% to 90% should be larger than 2ms. The subsequent warm hardware reset needs at least 1ms.

Figure 1-15 shows the reset timing diagram.

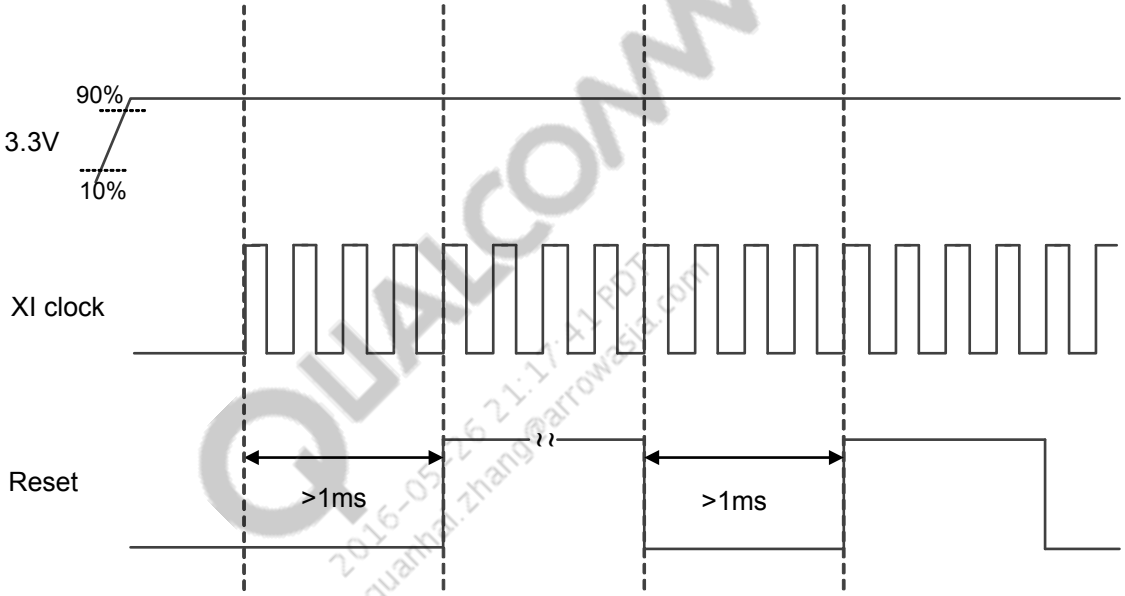


Figure 1-15 Reset timing diagram

1.4 Special marks

Table 1-9 defines special marks used in this document.

Table 1-9 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, SDC1_DATA[7:4] may indicate a range that is 4 bits in length, or DATA[7:0] may refer to all eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, RESIN_N.
0x000	Hexadecimal numbers are identified with an x in the number (for example, 0x0000). All numbers are decimal (base 10) unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number; for example, 0011 (binary).
|	A blue vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin Descriptions

The QCA8075 device is available in the 108-pin DR-QFN package that includes an exposed ground pad for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4.1 for package details. A high-level view of the pin assignment is shown in Figure 2-1.

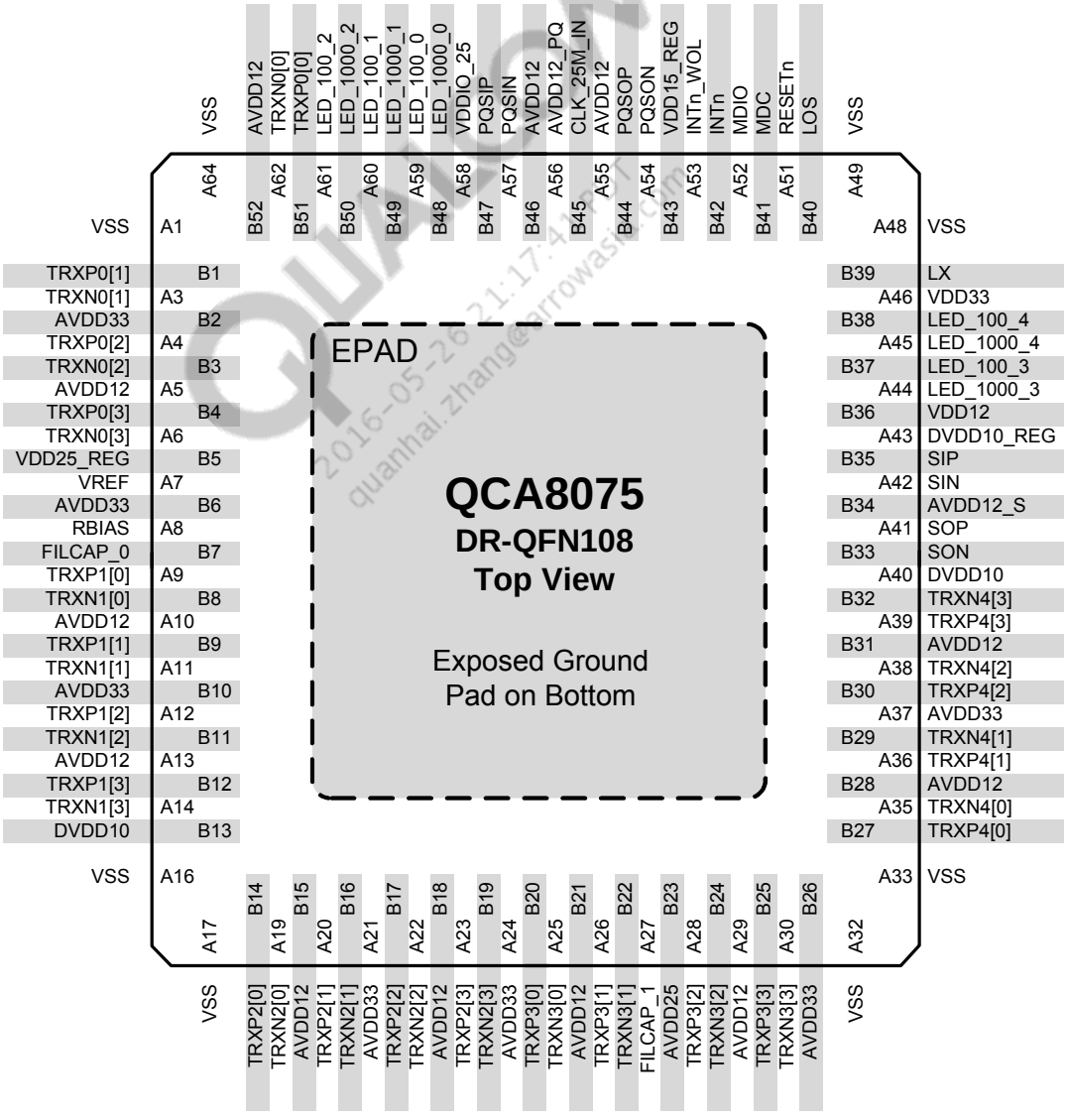


Figure 2-1 QCA8075 108-pin pinout (top view)

2.1 I/O parameter definitions

The following nomenclature is used for signal names:

NC	No connection should be made to this pin.
_n	Signal name suffix indicating active low signals
_P	Signal name suffix indicating the positive side of a differential signal
_N	Signal name suffix indicating the negative side of a differential signal

The following nomenclature is used for signal types:

IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up to prevent signals from floating when left open
IL	Input signals with weak internal pull-down to prevent signals from floating when left open
D	Open drain
I/O	Digital bidirectional signal
OA	Analog output signal
O	Digital output signal
P	Power or ground signal
PD	Internal pull-down for input
PU	Internal pull-up for input

Table 2-1 Pin description

Symbol	Pin	Type	Description
LED interface			
LED_1000_4	A45	I/O, PU	Parallel LED output for 1000BASE-T or 1000BASE-X of PHY4 Input for Power-On Strapping (POS) idac_adi[2]
LED_100_4	B38	I/O, PU	Parallel LED output for 100BASE-TX, 100BASE-FX, or 10BASE-Te of PHY4 Input for POS az_sel_pos
LED_1000_3	A44	I/O, PU	Parallel LED output for 1000BASE-T of PHY3 Input for POS control_dac_pos[2]
LED_100_3	B37	I/O, PU	Parallel LED output for 100BASE-TX or 10BASE-Te of PHY3 Input for POS control_dac_pos[1]
LED_1000_2	B50	I/O, PU	Parallel LED output for 1000BASE-T of PHY2 Input for POS control_dac_pos[0]
LED_100_2	A61	I/O, PU	Parallel LED output for 100BASE-TX or 10BASE-Te of PHY2 Input for POS phy_address_reg[4]
LED_1000_1	B49	I/O, PU	Parallel LED output for 1000BASE-T of PHY1 Input for POS phy_address_reg[3]

Table 2-1 Pin description (cont.)

Symbol	Pin	Type	Description
LED_100_1	A60	I/O, PU	Parallel LED output for 100BASE-TX or 10BASE-Te of PHY1 Input for POS mode3_pos
LED_1000_0	B48	I/O, PU	Parallel LED output for 1000BASE-T of PHY0 Input for POS mode2_pos
LED_100_0	A59	I/O, PU	Parallel LED output for 100BASE-TX or 10BASE-Te of PHY0 Input for POS mode1_pos
Management interface and interrupt			
MDC	B41	IH	Management data clock reference supporting up to 25 MHz This pin supports 1.5/1.8/2.7/3.3 V. Default is 1.8 V.
MDIO	A52	I/O, D, PU	Management data, normal I/O by default. Can be programmed to open-drain. This pin supports 1.5/1.8/2.7/3.3 V. Default is 1.8 V.
INTn	B42	D (I/O), PU	PHY interrupt output, active low This pin is open-drain by default, and can be changed to normal output by register. This pin supports 1.5/1.8/2.7 V. Default is 1.8 V.
INTn_WOL	A53	D (I/O), PU	Wake-on-LAN interrupt output, active low This pin is open-drain by default, and can be changed to normal output by register. This pin supports 1.5/1.8/2.7 V. Default is 1.8 V.
MDI The MDI pins integrate on-chip termination resistors. Do not connect termination resistors to these pins.			
TRXP0[0] TRXN0[0]	B51 A62	IA/OA	PHY0 Media Dependent Interface pair 0, connect to XFMR
TRXP0[1] TRXN0[1]	B1 A3	IA/OA	PHY0 Media Dependent Interface pair 1, connect to XFMR
TRXP0[2] TRXN0[2]	A4 B3	IA/OA	PHY0 Media Dependent Interface pair 2, connect to XFMR
TRXP0[3] TRXN0[3]	B4 A6	IA/OA	PHY0 Media Dependent Interface pair 3, connect to XFMR
TRXP1[0] TRXN1[0]	A9 B8	IA/OA	PHY1 Media Dependent Interface pair 0, connect to XFMR
TRXP1[1] TRXN1[1]	B9 A11	IA/OA	PHY1 Media Dependent Interface pair 1, connect to XFMR
TRXP1[2] TRXN1[2]	A12 B11	IA/OA	PHY1 Media Dependent Interface pair 2, connect to XFMR
TRXP1[3] TRXN1[3]	B12 A14	IA/OA	PHY1 Media Dependent Interface pair 3, connect to XFMR
TRXP2[0] TRXN2[0]	B14 A19	IA/OA	PHY2 Media Dependent Interface pair 0, connect to XFMR
TRXP2[1] TRXN2[1]	A20 B16	IA/OA	PHY2 Media Dependent Interface pair 1, connect to XFMR

Table 2-1 Pin description (cont.)

Symbol	Pin	Type	Description
TRXP2[2] TRXN2[2]	B17 A22	IA/OA	PHY2 Media Dependent Interface pair 2, connect to XFMR
TRXP2[3] TRXN2[3]	A23 B19	IA/OA	PHY2 Media Dependent Interface pair 3, connect to XFMR
TRXP3[0] TRXN3[0]	B20 A25	IA/OA	PHY3 Media Dependent Interface pair 0, connect to XFMR
TRXP3[1] TRXN3[1]	A26 B22	IA/OA	PHY3 Media Dependent Interface pair 1, connect to XFMR
TRXP3[2] TRXN3[2]	A28 B24	IA/OA	PHY3 Media Dependent Interface pair 2, connect to XFMR
TRXP3[3] TRXN3[3]	B25 A30	IA/OA	PHY3 Media Dependent Interface pair 3, connect to XFMR
TRXP4[0] TRXN4[0]	B27 A35	IA/OA	PHY4 Media Dependent Interface pair 0, connect to XFMR
TRXP4[1] TRXN4[1]	A36 B29	IA/OA	PHY4 Media Dependent Interface pair 1, connect to XFMR
TRXP4[2] TRXN4[2]	B30 A38	IA/OA	PHY4 Media Dependent Interface pair 2, connect to XFMR
TRXP4[3] TRXN4[3]	A39 B32	IA/OA	PHY4 Media Dependent Interface pair 3, connect to XFMR
System signal group/reference			
CLK_25M_IN	B45	IA	25 MHz reference clock input, 1.2 V level
RESETn	A51	IH	System reset input, active low This pin supports 1.5/1.8/2.7/3.3 V. Default is 1.8 V.
RBIAS	A8	IA/OA	Connect to 2.4 kΩ 1% resistor to GND.
LOS	B40	OD, PU	Loss of signal output for the BASE-T_SGMII application. High level indicates copper link down; low level for copper link up. This pin is open-drain by default, and can be changed to normal output by register. When configured to normal output, this pin supports 1.5/1.8/2.7 V. Default is 1.8 V.
VREF	A7	OA	1.2 V output for bandgap Connect a 1 nF capacitor to ground.
PSGMII/QSGMII			
PQSON PQSOP	A54 B44	OA	6.25 Gbps differential data outputs for PSGMII, or 5 Gbps differential data outputs for QSGMII
PQSIN PQSIP	A57 B47	IA	6.25 Gbps differential data inputs for PSGMII, or 5 Gbps differential data inputs for QSGMII
SGMII/1000BASE-X/100BASE-FX			
SON SOP	B33 A41	OA	1.25 Gbps differential data outputs for SGMII or 1000BASE-X

Table 2-1 Pin description (cont.)

Symbol	Pin	Type	Description
SIN SIP	A42 B35	IA	1.25 Gbps differential data inputs for SGMII or 1000BASE-X
Power			
FILCAP_0	B7	P	Connect a 1 µF and a 0.1 µF capacitors to ground.
FILCAP_1	A27	P	Connect a 1 µF and a 0.1 µF capacitors to ground.
AVDD33	B2, B6, B10, A21, A24, B26, A37	P	3.3 V analog power input
VDD33	A46	P	3.3 V digital power input for switch regulator
AVDD12	A5, A10, A13, B15, B18, B21, A29, B28, B31, A55, B46, B52	P	1.2 V analog power input
DVDD10	B13, A40	P	1.0 V digital power input Connect to pin A43.
VDDIO_25	A58	P	2.7 V digital I/O power and the power supply for VDD15_REG LDO
AVDD12_S	B34	P	1.2 V analog power input for SGMII Connect to pin B36 with a bead.
AVDD12_PQ	A56	P	1.2 V analog power input for PSGMII/QSGMII Connect to pin B36 with a bead.
AVDD25	B23	P	Connect a 0.1 µF capacitor to ground. This pin is connected to VDD25_REG inside chip.
DVDD10_REG	A43	P	1.0 V regulator output for DVDD10 Connect a 4.7 µF and a 0.1 µF capacitors to stabilize this voltage.
VDD25_REG	B5	P	2.7 V regulator output Connect a 1 µF and a 0.1 µF capacitors to GND to stabilize this voltage.
VDD12	B36	P	1.2 V digital power input for 1.0 V LDO input Connect directly to the power inductor of switch regulator. Connect to AVDD12 through a bead.
VDD15_REG	B43	P	1.5/1.8 V regulator output and the I/O power for the MDC, MDIO, RESETn, INTn, WOL_INTn, and LOS Connect a 1 µF and a 0.1 µF capacitors to stabilize this voltage.
LX	B39	OA	Inductor pin for 1.2 V switch regulator Connect an external 4.7 µH power inductor to this pin directly. Connect the other end of the inductor to B36 directly. Connect 22 µF + 1 µF + 0. 1µF ceramic capacitors to the other end of the inductor to stabilize this power supply.

Table 2-1 Pin description (cont.)

Symbol	Pin	Type	Description
Other			
VSS	A1, A16, A17, A32, A33, A48, A49, A64	P	Connect to ground.
GND	EPAD	P	Exposed ground pad on the back of the chip. Tied to ground.

2.2 Power-on strapping

The QCA8075 includes 10 LED pins. During hardware reset, these 10 LED pins are used as input for Power-On Strapping (POS) usage. After hardware reset is released, these 10 LED pins are used as output driven by internal PHY status. The POS functions are listed below.

Table 2-2 Power-on strapping

PIN symbol	POS configuration bit	Description	Default internal weak pull-up/down
LED_100_0	MODE[0]	MODE[2:0] are latched to configure chip operation mode. ■ 111 = PSGMII □ 5 copper ports ■ 110 = PSGMII □ 4 copper ports + 1 COMBO port (copper/fiber) ■ 101 = QSGMII + SGMII □ 5 copper ports ■ Others = Reserved The operation mode can be overwritten by port4 register 0x1F[2:0].	Pull up
LED_1000_0	MODE[1]		Pull up
LED_100_1	MODE[2]		Pull up
LED_1000_1	PHYAD3	The upper two bits of the physical address are set by PHYAD[4:3]. The PHYAD[2:0] are fixed to 0-5 for ports 0-4 and PSGMII respectively.	Pull down
LED_100_2	PHYAD4		Pull down
LED_1000_2	Reserved	Must be pulled up	Pull up
LED_100_3	Reserved	Must be pulled down	Pull up
LED_1000_3	Reserved	Must be pulled up	Pull up
LED_100_4	AZ_SEL	AZ_SEL is latched to MMD7 register 0x3C bits[2:1] to enable/disable IEEE 802.3az.	Pull up
LED_1000_4	Reserved	Must be pulled up	Pull up

3 Electrical Characteristics

3.1 Absolute maximum ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the QCA8075 device. Absolute maximum ratings are those values beyond which damage to the device can occur.

Functional operation under these conditions, or at any other condition beyond those indicated in this chapter, is not recommended.

NOTE Maximum rating for signals follow the supply domain of the signals.

Table 3-1 Absolute maximum ratings

Symbol	Parameter	Max rating	Unit
VDD33/AVDD33	3.3 V supply voltage	3.8	V
T_{store}	Storage temperature	-65 to 150	°C
V_{min}	Supply voltage min	GND-0.5	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
AVDD33	3.3 V analog power input	3.14	3.3	3.46	V
VDD33	3.3 V digital power input for switch regulator	3.14	3.3	3.46	V
T_A	Ambient temperature for normal operation (commercial chip version)	0	–	70	°C
	Ambient temperature for normal operation (industrial chip version)	-40	–	85	°C
T_J	Junction temperature	–	–	120	°C

3.3 QSGMII/PSGMII characteristics

Table 3-3 QSGMII/PSGMII transmitter output electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
T_Baud	Tx baud rate for QSGMII	–	5.00	–	GSym/s
	Tx baud rate for PSGMII	–	6.25	–	GSym/s
T_Vdiff	Output differential voltage (into floating load R_{load} = 100 Ω)	Programmable, 600 by default			mV/ppd
T_Rd	Differential resistance	80	100	120	Ω
T_tr, T_tf	Output rise/fall time (20% to 80%) for QSGMII	30	–	–	ps
	Output rise/fall time (20% to 80%) for PSGMII	24	–	–	ps
T_Ncm	Transmitter common mode noise	–	–	5% of T_Vdiff	mVppd
T_c	Output current into or out of the driver pins when either is short to ground or to each other	–	–	100	mA
T_Vcm	Output common mode voltage	760	900	1040	mV

Table 3-4 QSGMII/PSGMII receiver input electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
R_Baud	Rx baud rate for QSGMII	–	5.00	–	GSym/s
	Rx baud rate for PSGMII	–	6.25	–	GSym/s
R_Vdiff	Differential voltage	100	–	900	mV/ppd
R_Rdin	Differential resistance	80	100	120	Ω
R_Vrcm	Input common mode voltage (load type 0)[1]	-50	–	1850	mV
	Input common mode voltage (load type 1)[2]	750	900	1050	mV

1. Load type 0: AC coupling
2. Load type 1: DC coupling

Table 3-5 QSGMII/PSGMII transmit jitter specifications

Symbol	Parameters	Min	Typ	Max	Unit
T_UHPJ	Uncorrelated high probability jitter	–	–	0.15	Ulpp
T_DCD	Duty cycle distortion	–	–	0.05	Ulpp
T_Tj	Total Jitter	–	–	0.30	Ulpp
T_X1	Eye mask	–	–	0.15	UI
T_X2		–	–	0.40	UI
T_Y1		200	–	–	mV
T_Y2		–	–	450	mV

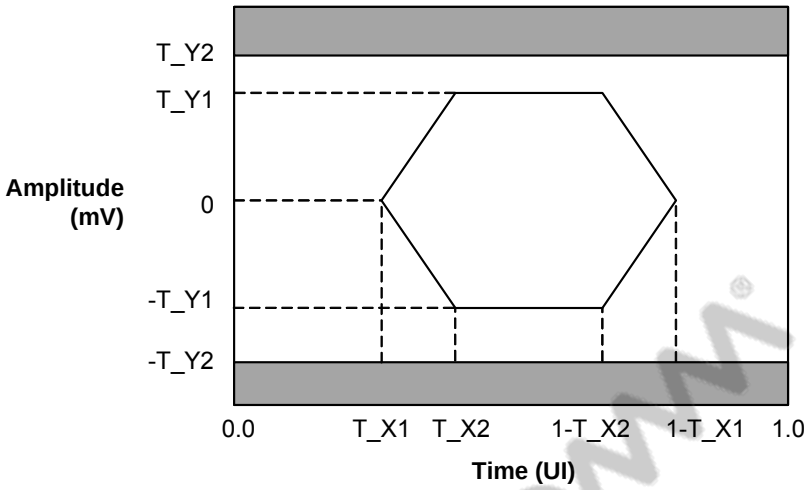


Figure 3-1 QSGMII/PSGMII transmit jitter eye diagram

Table 3-6 QSGMII/PSGMII receive jitter specifications

Symbol	Parameter	Min	Typ	Max	Unit
R_BHPJ	Bounded high probability jitter	–	–	0.45	Ulpp
R_SJ_max	Sinusoidal jitter, maximum	–	–	5	Ulpp
R_SJ_hf	Sinusoidal jitter, high frequency	–	–	0.05	Ulpp
R_TJ	Total jitter (sinusoidal jitter not included)	–	–	0.60	UI
R_X1	Eye mask	–	–	0.30	UI
R_Y1		–	–	50	mV
R_Y2		–	–	450	mV

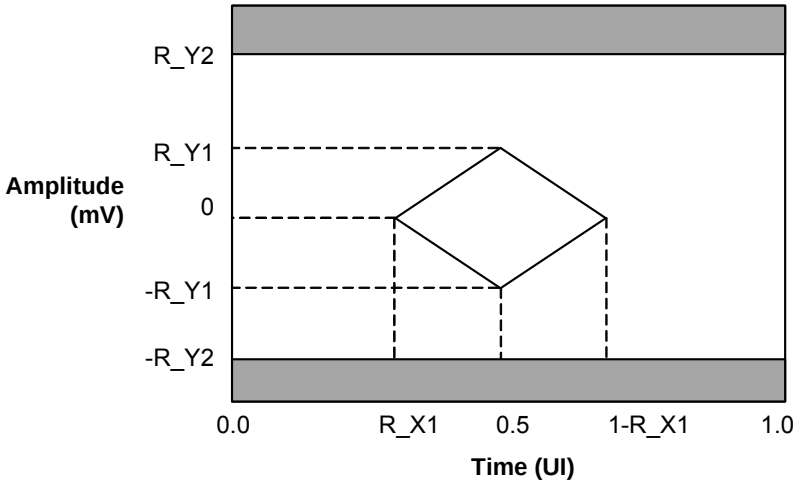


Figure 3-2 QSGMII/PSGMII receive jitter eye diagram

3.4 SGMII/SerDes characteristics

Table 3-7 shows the driver DC characteristics.

Table 3-7 Driver DC Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	Output voltage high	–	1050	1150	mV
V_{OL}	Output voltage low	600	750	–	mV
V_{RING}	Output ringing	–	–	10	%
$\|V_{OD}\|$	Output differential voltage	Programmable, 300 by default			mV
V_{OS}	Output offset voltage (common mode)	850	900	950	mV
R_O	Output impedance (single-ended, 50 Ω termination)	40	50	60	Ω
	Output impedance (single-ended, 75 Ω termination)	60	75	90	Ω
ΔR_O	Mismatch in a pair	–	–	10	%
$\Delta\|V_{OD}\|$	Change in V_{OD} between 0 and 1	–	–	25	mV
ΔV_{OS}	Change in V_{OS} between 0 and 1	–	–	25	mV
I_{SA}, I_{SB}	Output current on short to ground	–	–	40	mA
I_{SAB}	Output current when a and b are shorted	–	–	12	mA
I_{XA}, I_{XB}	Power off leakage current	–	–	10	mA

Table 3-8 shows the receiver DC characteristics.

Table 3-8 Receiver DC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IO}	Input offset voltage (common mode)	830	925	1030	mV
V_{IH}	Input voltage high	–	1150	1250	mV
V_{IL}	Input voltage low	590	700	–	mV
V_{IDTH}	Input differential threshold	-50	–	50	mV
V_{HYST}	Input differential hysteresis	25	–	–	mV
R_{IN}	Receiver differential input impedance, 50 Ω termination	80	100	120	Ω
	Receiver differential input impedance, 75 Ω termination	120	150	180	Ω

Table 3-9 shows the Driver AC characteristics.

Table 3-9 Driver DC characteristics

Symbol	Parameter	Min	Max	Unit
t_{fall}	Vod fall time (20%-80%)	100	200	ps
t_{rise}	Vod rise time (20%-80%)	100	200	ps
Tskew	Skew between two members of a differential pair	–	20	ps

1. Skew measured at 50% of the transition.

3.5 MDC/MDIO interface characteristics

3.5.1 MDIO/MDC AC characteristics

Figure 3-3 shows the MDC/MDIO AC timing diagram.

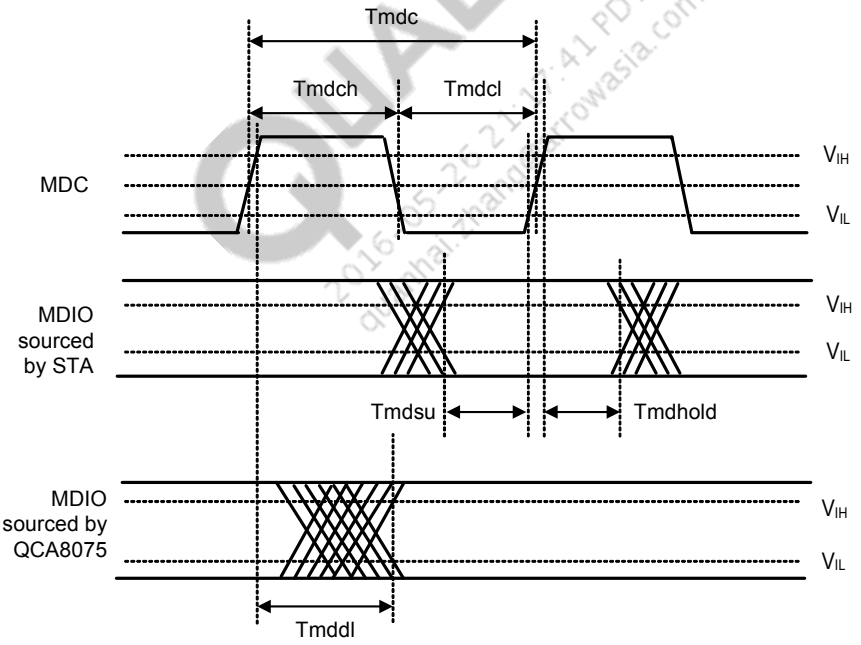


Figure 3-3 MDC/MDIO AC timing diagram

Table 3-10 MDC/MDIO AC characteristic

Symbol	Parameter	Min	Typ	Max	Unit
Tmdc	MDC period	40	–	–	ns
Tmdcl	MDC low period	16	–	–	ns
Tmdch	MDC high period	16	–	–	ns
Tmdsu	MDIO input setup time to MDC rising	10	–	–	ns

Table 3-10 MDC/MDIO AC characteristic (cont.)

Symbol	Parameter	Min	Typ	Max	Unit
Tmdhold	MDIO input hold time from MDC rising	10	–	–	ns
Tmddl	MDIO output delay from MDC rising in open drain mode	0	–	300	ns
	MDIO output delay from MDC rising in normal IO mode	0	–	20	ns

3.5.2 MDC/MDIO DC characteristics

Table 3-11 MDC/MDIO DC characteristic, 2.7 V I/O supply

Symbol	Parameter	Min	Max	Unit
V_{OH}	Output high voltage	2.4	3.0	V
V_{OL}	Output low voltage	GND -0.3	0.4	V
V_{IH}	Input high voltage	2.0	3.5	V
V_{IL}	Input low voltage	GND -0.3	0.4	V
I_{IH}	Input high current	–	0.4	mA
I_{IL}	Input low current	-0.4	–	mA

Table 3-12 MDC/MDIO DC characteristic, 1.8V I/O supply

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	1.4	2.1	V
V_{IL}	Input low voltage	GND -0.3	0.4	V
V_{OH}	Output high voltage	1.5	2.0	V
V_{OL}	Output low voltage	GND -0.3	0.3	V
I_{IH}	Input high current	–	0.3	mA
I_{IL}	Input low current	-0.3	–	mA

Table 3-13 MDC/MDIO DC characteristic, 1.5V I/O supply

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	1.2	1.8	V
V_{IL}	Input low voltage	GND -0.3	0.3	V
V_{OH}	Output high voltage	1.3	1.65	V
V_{OL}	Output low voltage	GND -0.3	0.2	V
I_{IH}	Input high current	–	0.2	mA
I_{IL}	Input low current	-0.2	–	mA

1. When INTn, INTn_WOL and LOS are configured to normal output by register, the output DC characteristics are the same with MDC/MDIO output DC characteristics.

3.6 RESETn input DC characteristics

Table 3-14 RESETn input DC characteristic, 2.7V I/O supply

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	2.0	3.6	V
V_{IL}	Input low voltage	GND -0.3	0.4	V

Table 3-15 RESETn input DC characteristic, 1.8V I/O supply

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	1.4	2.1	V
V_{IL}	Input low voltage	GND -0.3	0.4	V

Table 3-16 RESETn input DC characteristic, 1.5V I/O supply

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	1.2	1.8	V
V_{IL}	Input low voltage	GND -0.3	0.3	V

3.7 Reference Clock input characteristics

QCA8750 supports external 25MHz single-ended clock input as reference.

Table 3-17 External clock input characteristic

Symbol	Parameter	Min	Typ	Max	Unit
T_XI_PER	Input clock frequency	25.0 - 50ppm	25	25.0 + 50ppm	MHz
DC	Clock duty cycle measured at 50% point	40	50	60	%
T_XI_RISE	XI clock rise time measured at 20% to 80% points	–	–	2.5	ns
T_XI_FALL	XI clock fall time measured at 20% to 80% points	–	–	2.5	ns
V_IH_XI	The XI input high level	0.8	1.2	1.5	V
V_IL_XI	The XI input low level voltage	-0.3	0	0.15	V
C_{IN}	Load capacitance	–	1	2	pF
$Jitter_{RMS}$	Period RMS jitter (10 KHz to 3 MHz)	–	–	3.5	ps
$Jitter_{pk-pk}$	Period peak-to-peak jitter (10 KHz to 3 MHz)	–	–	40	ps

3.8 Power consumption

This section provides power consumption at typical operation condition:

AVDD33/VDD33=3.3V; T_A = 25 °C

Table 3-18 Power consumption

Test condition	3.3V typical current (mA)	Total power consumption w/o LED (mW)
PSGMII to 5 copper ports		
All ports software power down, minimum power	14	46.2
All ports 1000BASE-T full duplex line speed with more than 100m cable, maximum power	467	1541
PSGMII to 4 copper ports + 1 combo port		
All port software power down, minimum power	15	49.5
All ports 1000BASE-T full duplex line speed with more than 100m cable, maximum power	468	1544
QSGMII+SGMII to 5 copper ports		
All port software power down, minimum power	14	46.2
All ports 1000BASE-T full duplex line speed with more than 100m cable, maximum power	482	1590

4 Mechanical Information

4.1 Device physical dimensions

The QCA8075 device is available in the 9 mm × 9 mm × 0.90 mm Dual-Row Quad Flat pack No-lead (DR-QFN) package that includes a ground pad for improved grounding, mechanical strength, and thermal continuity. Pin 1 is located by an indicator mark on the top of the package.

Figure 4-1, Table 4-1, Figure 4-2, and Table 4-2 show the QCA8075 device mechanical dimensions, top and bottom views from two package assemblies.

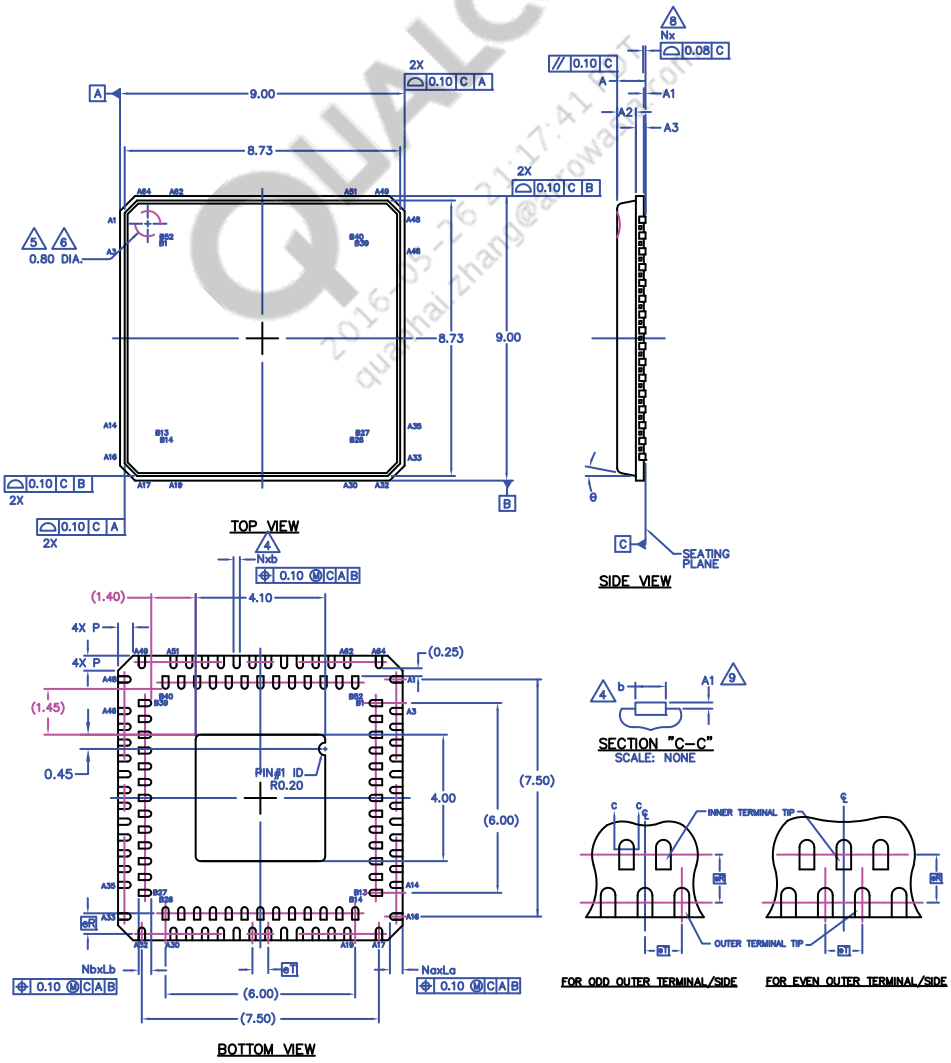


Figure 4-1 QCA8075 mechanical dimensions, top and bottom views (assembly 1)

Table 4-1 Mechanical dimensions (assembly 1)[1]

Dimension label	Min	Norm	Max	Unit
A	0.80	0.85	0.90	mm
A1	0.00	0.01	0.05	mm
A2	0.55	0.60	0.65	mm
A3		0.25 REF		mm
eT		0.50 BSC		mm
eR		0.65 BSC		mm
La	0.30	0.40	0.50	mm
Lb	0.30	0.40	0.50	mm
b	0.18	0.22	0.30	mm
θ	–	–	12	°
P	0.24	0.42	0.60	mm

1. Reference document: NT90-Y8679-C1 Rev. A

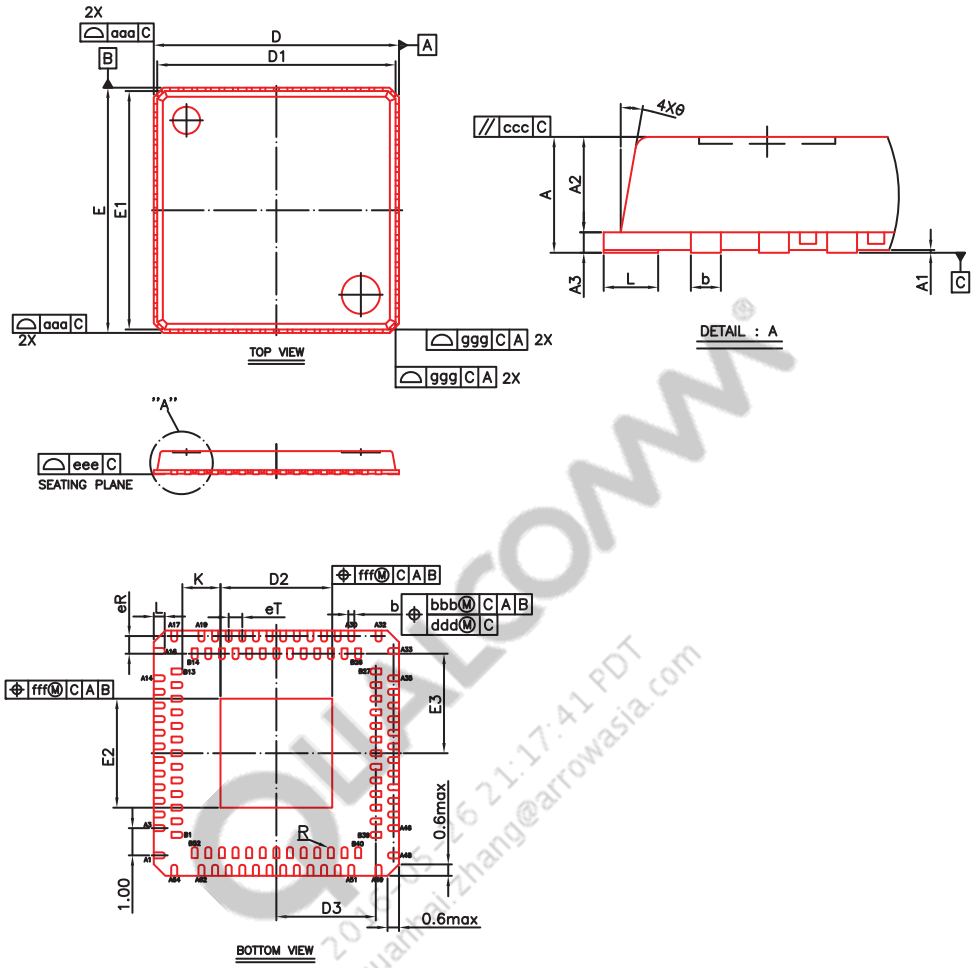


Figure 4-2 QCA8075 mechanical dimensions, top and bottom views (assembly 2)

Table 4-2 Mechanical dimensions (assembly 2)[1]

Dimension label	Min	Norm	Max	Unit
A	0.80	0.85	0.90	mm
A1	0.00	0.02	0.05	mm
A2	0.65	0.70	0.75	mm
A3		0.15 REF		mm
b	0.18	0.22	0.30	mm
D/E	8.90	9.00	9.10	mm
D1/E1		8.75 BSC		mm
D2	4.00	4.10	4.20	mm
E2	3.90	4.00	4.10	mm
D3/E3		3.65 BSC		mm
eT		0.50 BSC		mm
eR		0.65 BSC		mm
L	0.30	0.40	0.50	mm
θ	5	–	15	°
R	0.09	–	0.14	mm
K	0.20	–	–	mm
aaa		0.10		mm
bbb		0.10		mm
ccc		0.10		mm
ddd		0.05		mm
eee		0.08		mm
fff		0.10		mm
ggg		0.20		mm

1. Reference document: NT90-Y8679-D1 Rev. A

4.2 Part marking

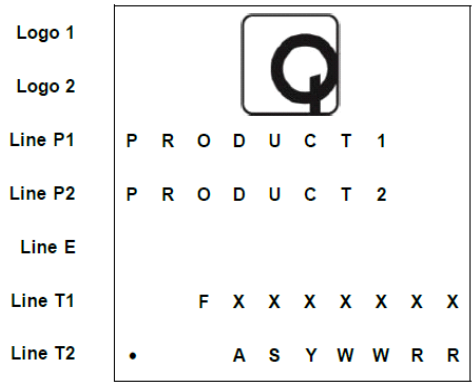


Figure 4-3 QCA8075 marking (top view)

1. Pin 1 is located bottom and left justified to marking area.

Table 4-3 QCA8075 marking line definitions

Line	Marking	Description
Logo 1 and 2	QUALCOMM	Qualcomm Atheros name or logo
P1	QCA8075	Qualcomm Atheros product name
P2	PAA	P = product configuration code AA = product feature code
E[1]		Blank space between P2 and T1
T1	FXXXXXXX	F = source of supply code XXXXXXX = wafer lot ID
T2	ASYWWRR	A = assembly site code S = assembly sequence number Y = single, last digit of year WW = work week (based on calendar year) RR = product revision

1. Line E may appear on the part marking for some samples. This is manufacturing information that is only relevant to Qualcomm and Qualcomm suppliers.

4.3 Device ordering information

Ordering numbers have the form shown in Figure 4-4.

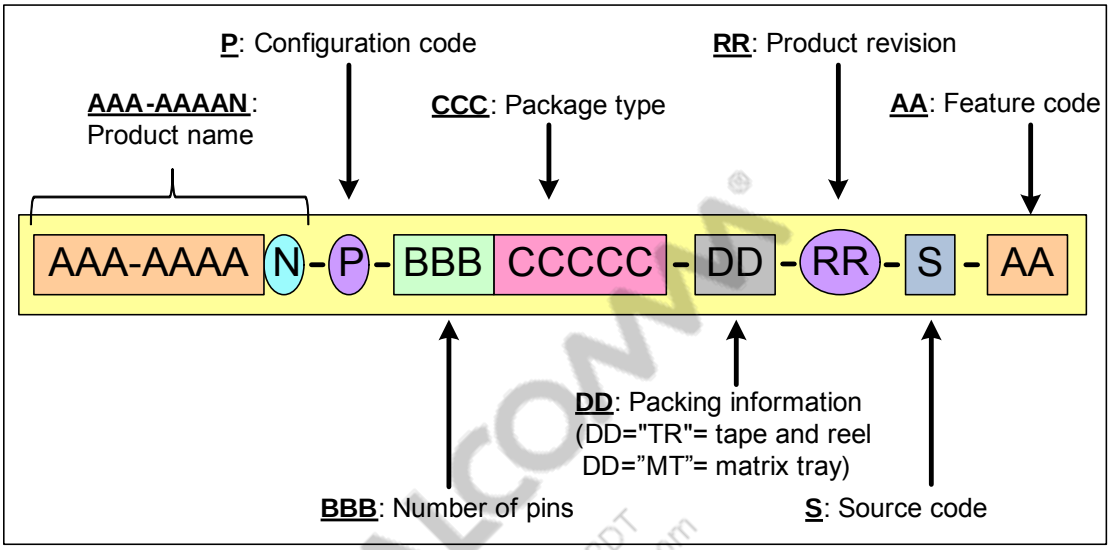


Figure 4-4 Device identification code

Table 4-4 shows the available ordering numbers.

Table 4-4 QCA8075 ordering numbers

PRR	Number	Descriptions
000	QCA-8075-0-108DRQFN-MT-00-0	RoHS & BrCl-free, Commercial Temperature
000	QCA-8075-0-108DRQFN-TR-00-0	RoHS & BrCl-free, Commercial Temperature, Tape-and-Reel
100	QCA-8075-1-108DRQFN-MT-00-0	RoHS & BrCl-free, Industrial Temperature
100	QCA-8075-1-108DRQFN-TR-00-0	RoHS & BrCl-free, Industrial Temperature, Tape-and-Reel
001	QCA-8075-0-108DRQFN-MT-01-0	RoHS & BrCl-free, Commercial Temperature
001	QCA-8075-0-108DRQFN-TR-01-0	RoHS & BrCl-free, Commercial Temperature, Tape-and-Reel
101	QCA-8075-1-108DRQFN-MT-01-0	RoHS & BrCl-free, Industrial Temperature
101	QCA-8075-1-108DRQFN-TR-01-0	RoHS & BrCl-free, Industrial Temperature, Tape-and-Reel

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. Qualcomm follows the latest IPC/JEDEC J-STD-609 standard revision for moisture-sensitivity qualification. The QCA8075 is classified as MSL3.

4.5 Thermal characteristics

Table 4-5 Thermal resistance

Parameter		Comment	Typical	Unit
θ_{JA}	Junction-to-Ambient	■ Jedec JESD51-2A ■ Jedec JESD51-7	27.8	°C/W
θ_{JB}	Junction-to-Board	■ Jedec JESD51-7 ■ Jedec JESD51-8 ■ Cold plate ring maintained at 25°C at top and bottom of PCB	33.3	°C/W
θ_{JC}	Junction-to-Case	■ No thermal vias ■ Jedec JESD51-7 ■ Jedec JESD51-8 ■ Cu block at top of package maintained at 25°C	15.8	°C/W
Ψ_{JT}	Junction-to-Top	■ Jedec JESD51-2A ■ Jedec JESD51-7	0.54	°C/W

5 Carrier, Storage, and Handling Information

5.1 Carrier

5.1.1 Tape and reel information

Carrier tape system conforms to the EIA-481 standard.

Simplified sketches of the QCA8075 tape carrier is shown in Figure 5-1 and Figure 5-2, including the part orientation. Tape and reel details for the QCA8075 are as follows:

- Reel diameter: 330 mm
- Hub size: 102 mm
- Tape width: 16 mm
- Tape pocket pitch: 12 mm
- Feed: Single
- Units per reel: 4,000

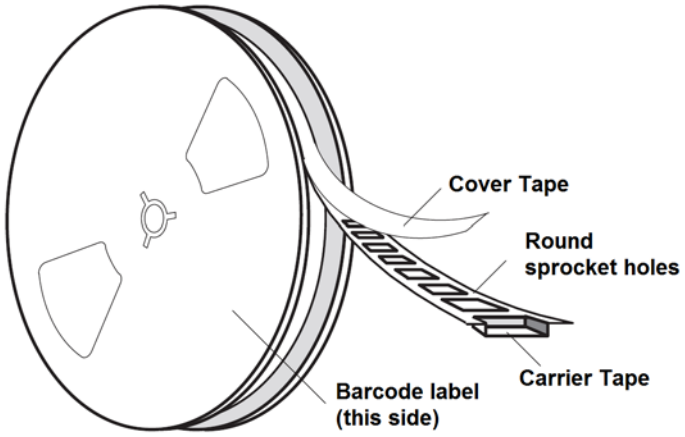


Figure 5-1 Tape orientation on reel

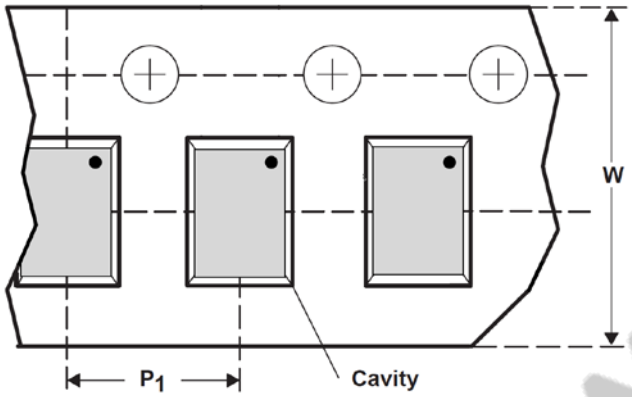
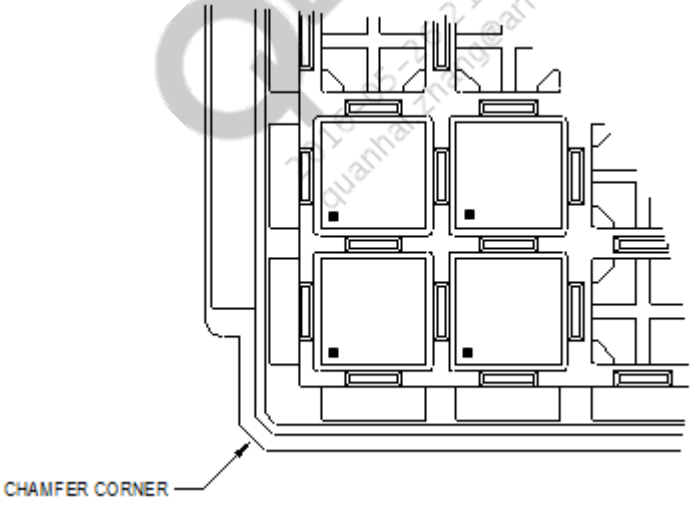


Figure 5-2 Part orientation in tape

5.1.2 Matrix tray information

All QTI matrix tray carriers confirm to JEDEC standards. The device pin 1 is oriented to the chamfered corner of the matrix tray. Each tray of the QCA8075 contains up to 260 devices. See Figure 5-3 for matrix-tray key attributes and dimensions.



Key dimensions	
Array	10 × 26 = 260
M	10.35 mm
M1	10.00 mm
M2	11.80 mm
M3	12.80 mm

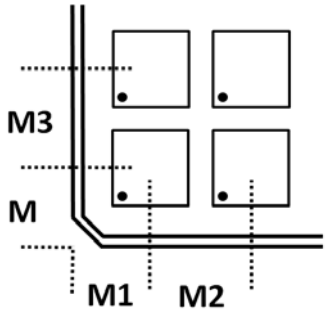


Figure 5-3 Matrix tray part orientation

5.2 Storage

5.2.1 Bagged storage conditions

QCA8075 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 1.

5.3 Handling

Tape handling is described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

It is not necessary to bake the QCA8075 if the conditions specified in Section 5.2.1 and Section 5.2.2 have not been exceeded.

It is necessary to bake the QCA8075 if any condition specified in Section 5.2.1 or Section 5.2.2 has been exceeded. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see *ASIC Packing Methods and Materials Specification* (80-VK055-1) for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Barcode label and packing for shipment

Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

6 PCB Mounting Guidelines

Guidelines for mounting the QCA8075 device onto a PCB are presented in this chapter, including land pad and stencil design details, surface mount technology (SMT) process characterization, and SMT process verification.

6.1 RoHS compliance

The device is externally lead-free and RoHS-compliant. Qualcomm Atheros defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products. Qualcomm Atheros package environmental programs, RoHS compliance details, and tables defining pertinent characteristics of all Qualcomm Atheros IC products are described in the *IC Package Environmental Roadmap* (80-V6921-1).

6.2 SMT parameters

The information presented in this section describes Qualcomm Atheros board-level characterization process parameters. It is included to assist customers when starting their SMT process development; it is not intended to be a specification for customer SMT processes.

NOTE Qualcomm Atheros recommends that customers follow their solder paste vendor recommendations for the screen-printing process parameters and reflow profile conditions.

Qualcomm Atheros characterization tests attempt to optimize the SMT process for the best board-level reliability possible. This is done by performing physical tests on evaluation boards, which may include:

- Drop shock
- Temperature cycling
- Bend cycle (optional)

6.2.1 Land pad and stencil design

Qualcomm Atheros recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile **prior to PCB production**. Optimizing the solder stencil-pattern design and print process is critical to ensure print uniformity,

decrease voiding, and increase board-level reliability. See *QCA DRQFN Surface Mount Requirements* (80-Y7781-1) for characterization.

6.2.2 Reflow profile

Reflow profile conditions typically used by Qualcomm Atheros for SnPb and lead-free systems are given in Table 6-1.

Table 6-1 Qualcomm Atheros typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Lead-free (high temperature condition limits)
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Dry out and flux activation	150 to 190°C	60 to 120 sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C[1]	50 to 70 sec
Preheat	Initial ramp	< 150°C	3°C/sec max

1. During the reflow state, the peak temperature should not exceed 245°C. This temperature should not be confused with the peak temperature reached during MSL testing. See QCA DRQFN Surface Mount Requirements (80-Y7781-1) for characterization

Figure 6-1 shows the typical SMT reflow profile.

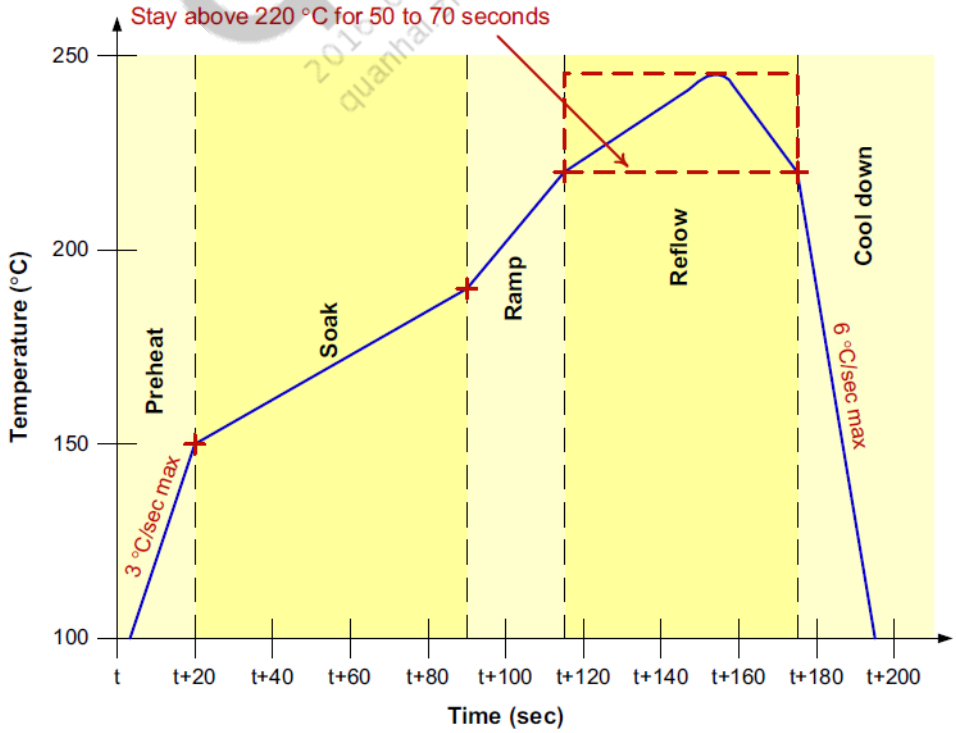


Figure 6-1 Typical SMT reflow profile

6.2.3 SMT peak package-body temperature

During a production board's reflow process, the temperature for the package must be controlled. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more).

Although the solder-paste manufacturer's recommendations for optimum temperature and duration for solder reflow must be followed, the Qualcomm Atheros recommended limits must not be exceeded.

6.2.4 SMT process verification

Qualcomm Atheros recommends verification of the SMT process prior to high-volume PCB fabrication, including:

- Electrical continuity
- X-ray inspection of the package installation for proper alignment, solder voids, solder balls, and solder bridging
- Visual inspection
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume

6.3 Board-level reliability

Qualcomm Atheros conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- (Optional) Cyclic bend testing (JESD22-B113)

See *Board-level Reliability* (BR80-NT096-1) for details.