RT5350
DATASHEET

Integrated IEEE 802.11n compliant 1T1R MAC/BBP/PA/RF Single Chip

Product Description

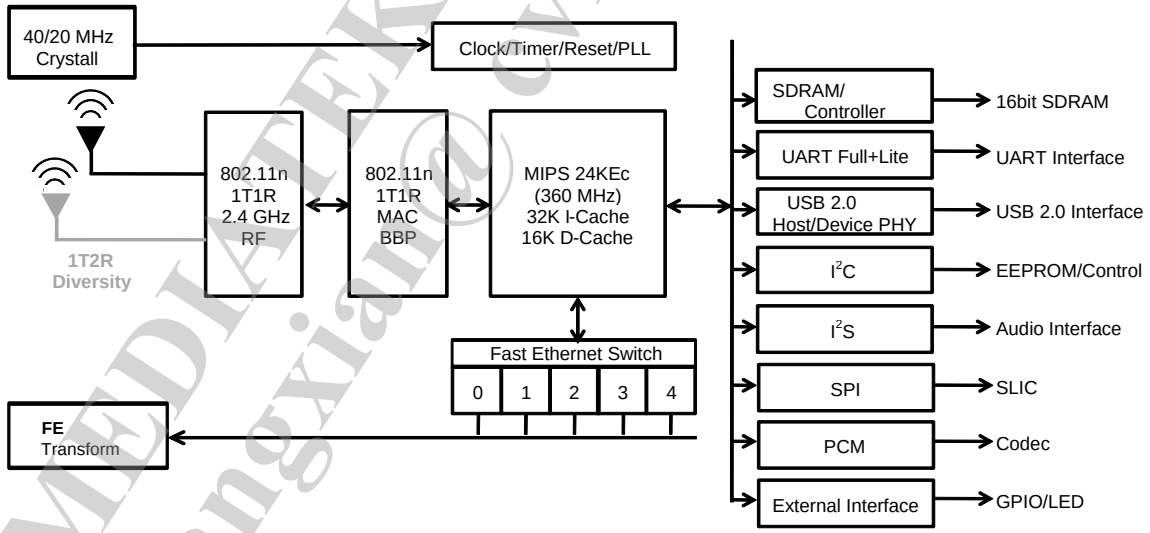
The RT5350 SoC combines Ralink's IEEE 802.11n compliant 1T1R MAC/BBP/PA/RF, a high performance 360 MHz MIPS24KEc CPU core, a 5-port integrated 10/100 Ethernet switch/PHY and a USB host/device. With the RT5350, there are very few external components required for 2.4 GHz 802.11n wireless products. The RT5350 employs Ralink's 2nd generation 802.11n technologies for longer range and better throughput. The embedded, high performance CPU can easily manage advanced applications such as Wi-Fi data processing without overloading the host processor. In addition, the RT5350 offers a variety of hardware interfaces (SPI/I^2S/I^2C/PCM/UART/USB) to support a range of possible applications

Applications:
- iNIC
- AP/Router

Key Features

- Embedded 1T1R 2.4G CMOS RF
- Embedded 802.11n 1T1R MAC/BBP with MLD enhancement
- Embedded PA/LNA
- 150 Mbps PHY data rate
- 20 Mhz/40 MHz channel width
- Legacy and high throughout modes
- Compressed block ACK
- Bluetooth Co-existence
- Multiple BSSID (up to 16)
- WEP64/128, WPA, WPA2, WAPI engines
- QOS - WMM, WMM Power Save
- Hardware frame aggregation
- Supports 802.11h TPC
- MIPS 24KEc 360 Mhz with 32 KB I cache/16 KB D cache
- Supports 16-bit SDR SDRAM (up to 64 MB)
- Supports boot from ROM, FLASH
- USB 2.0 HOST/Device dual mode x1
- Embedded 5-port 10/100 Mbps Ethernet switch and 5-port UTP PHY
- Supports 5 10/100 UTP ports
- Slow speed I/O : GPIO, SPI, I^2C, I^2S, PCM, UART, and JTAG
- Packaging and I/O voltage
- 12 mm x 12 mm TFBGA-196 package
- I/O: 3.3 V I/O

Functional Block Diagram



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Part Number	Packaging
RT5350F	Green/RoHS Compliant TFBGA 196 ball (12 mm x 12 mm)

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1.1 196-Pin BGA Package Diagram

Table 1-1 196-Pin BGA Package Diagram Top View (left portion)

	1	2	3	4	5	6	7
A	GND	WL_RF0_2G_INP	WL_RF0_2G_INN	GND	WL_RF_BB1_V12A	WL_PLL_VC_CAP	WL_PLL_X1
B	WL_RF0_PA_V33P	GND	WL_RF0_RF_V12A	GND	WL_RF0_IF_V12A	WL_PLL_V12A	WL_PLL_X2
C	WL_RF0_PA_OUTP	GND	GND	GND	GND	WL_VCO_VCO_V12A	WL_LDOPLL_OUT_V12
D	WL_RF0_PA_OUTN	GND	GND	GND	GND	GND	GND
E	WL_RF0_PA_V33N	GND	WL_RF0_PA1_V33A	GND	GND	GND	GND
F	GND	GND	GND	GND	SOC_IO_V33D	GND	GND
G	VOUT_1P2	LDO_V18A	LDOSEL	COMP	SOC_IO_V33D	GND	GND
H	UGATE	DCDC_V33A	EXT_LDO_1P2	FB	SOC_CO_V12D	GND	GND
J	LGATE	DCDC_V33D	SPI_MOSI	DCD_N	SOC_CO_V12D	GND	GND
K	WLAN_LED_N	TXD	EPHY_LED0_N	CTS_N	EPHY_V33A	EPHY_V33A	EPHY_V33A
L	EPHY_LED1_N	SPI_CS1	DSR_N	EPHY_LED2_N	EPHY_RXN_P0	EPHY_RXN_P1	EPHY_TXP_P2
M	EPHY_LED3_N	SPI_MISO	RIN	EPHY_LED4_N	EPHY_RXP_P0	EPHY_RXP_P1	EPHY_TXN_P2
N	SPI_CLK	TXD2	RXD	DTR_N	EPHY_TXN_P0	EPHY_TXN_P1	EPHY_RXN_P2
P	SPI_CS0	RTS_N	RXD2	EPHY_REF_RES	EPHY_TXP_P0	EPHY_TXP_P1	EPHY_RXP_P2

Table 1-2 196-Pin BGA Package Diagram Top View (right portion)

8	9	10	11	12	13	14	
WL_LDORF_IN_VX	WL_BG_V33A	PLL_AVDD_V12A	JTAG_TRST_N	JTAG_TCLK	JTAG_TMS	JTAG_TDI	A
WL_BG_RES_12K	WL_ADC_V12	PLL_DVDD_V12D	JTAG_TDO	GPIO0	I2C_SD	I2C_SCLK	B
WL_LDORF_OUT_V12	WL_RF_BB2_V12	PORST_N	MCKE	MCAS_N	MWE_N	MCS1_N	C
GND	GND	SOC_IO_V33D_1	MD1	MD2	MD3	MD4	D
GND	GND	MD0	MD5	MD7	MD9	MD10	E
GND	SOC_CO_V12D	SDRAM_IO_V33D	MD6	MD8	MD13	MD15	F
GND	SOC_CO_V12D	SDRAM_IO_V33D	MD11	MD12	MD14	MA0	G
GND	SOC_CO_V12D	SDRAM_IO_V33D	MA3	MA2	MA1	MCLK	H
GND	GND	MDQM0	MA9	MA6	MA5	MA4	J
EPHY_V33A	GND	GND	MCS0_N	MA11	MA8	MA7	K
EPHY_RXP_P3	EPHY_TXP_P4	GND	MRAS_N	MBA0	MA12	MA10	L
EPHY_RXN_P3	EPHY_TXN_P4	GND	GND	GND	MDQM1	MBA1	M
EPHY_TXN_P3	EPHY_RXN_P4	GND	UPHY0_VDDA_V33A	UPHY0_PADM	GND	GND	N
EPHY_TXP_P3	EPHY_RXP_P4	GND	UPHY0_VRES	UPHY0_PADP	UPHY0_VDDL_V12D	GND	P

1.2 Pin Description

Table 1-3 Pin Description

Pin	Name	I/O/IPU/IPD	Driving	Description
JTAG interfaces: 5 pins				
A11	JTAG_TRST_N	I, IPU	4 mA	JTAG TRST (active low) (pull low is necessary)
A12	JTAG_TCLK	I, IPD	4 mA	JTAG TCLK
A13	JTAG_TMS	I, IPD	4 mA	JTAG TMS
A14	JTAG_TDI	I, IPD	4 mA	JTAG TDI
B11	JTAG_TDO	O, IPD	4 mA	JTAG TDO
UART Lite interface: 2 pins				
P3	RXD2	I, IPD	4 mA	UART Lite RXD
N2	TXD2	O, IPD	4 mA	UART Lite TXD
UART Full interface: 8 pins				
N3	RXD	I, IPD	4 mA	UART RXD.
M3	RIN	I, IPD	4 mA	UART RIN.
K4	CTS_N	I, IPD	4 mA	UART CTS_N.
L3	DSR_N	I, IPD	4 mA	UART DSR_N.

Pin	Name	I/O/IPU/IPD	Driving	Description
J4	DCD_N	I, IPD	4 mA	UART DCD_N.
K2	TXD	O, IPD	4 mA	UART TXD.
N4	DTR_N	O, IPD	4 mA	UART DTR.
P2	RTS_N	O, IPD	4 mA	UART RTS.
SPI/EEPROM interface: 5 pins				
M2	SPI_MISO	I, IPD	4 mA	SPI Master In Slave Out
J3	SPI_MOSI	O, IPD	4 mA	SPI Master Out Slave In
N1	SPI_CLK	O, IPD	4 mA	SPI Clock
P1	SPI_CS0	O, IPD	4 mA	SPI Chip Select 0
L2	SPI_CS1	O, IPD	4 mA	SPI Chip Select 1
I2C interface: 2 pins				
B14	I2C_SCLK	I/O, IPU	8 mA	I2C Clock
B13	I2C_SD	O, IPU	8 mA	I2C Data
GPIO interface: 1 pins				
B12	GPIO0	I/O, IPD	8 mA	GPIO0
5-Port PHY: 26 pins				
K3	EPHY_LED0_N	O, IPD	4 mA	10/100 Phy Port #0 Activity Led
L1	EPHY_LED1_N	O, IPD	4 mA	10/100 PHY Port #1 Activity LED
L4	EPHY_LED2_N	O, IPD	4 mA	10/100 PHY Port #2 Activity LED
M1	EPHY_LED3_N	O, IPD	4 mA	10/100 PHY Port #3 Activity LED
M4	EPHY_LED4_N	O, IPD	4 mA	10/100 PHY Port #4 Activity LED
P4	EPHY_REF_RES	A		Connects to an external resistor to provide accurate bias current.
L5	EPHY_RXN_P0	I		10/100 PHY Port #0 RXN
M5	EPHY_RXP_P0	I		10/100 PHY Port #0 RXP
N5	EPHY_TXN_P0	O		10/100 PHY Port #0 TXN
P5	EPHY_TXP_P0	O		10/100 PHY Port #0 TXP
L6	EPHY_RXN_P1	I		10/100 PHY Port #1 RXN
M6	EPHY_RXP_P1	I		10/100 PHY Port #1 RXP
N6	EPHY_TXN_P1	O		10/100 PHY Port #1 TXN
P6	EPHY_TXP_P1	O		10/100 PHY Port #1 TXP
N7	EPHY_RXN_P2	I		10/100 PHY Port #2 RXN
P7	EPHY_RXP_P2	I		10/100 PHY Port #2 RXP
M7	EPHY_TXN_P2	O		10/100 PHY Port #2 TXN
L7	EPHY_TXP_P2	O		10/100 PHY Port #2 TXP
M8	EPHY_RXN_P3	I		10/100 PHY Port #3 RXN
L8	EPHY_RXP_P3	I		10/100 PHY Port #3 RXP
N8	EPHY_TXN_P3	O		10/100 PHY Port #3 TXN
P8	EPHY_TXP_P3	O		10/100 PHY Port #3 TXP
N9	EPHY_RXN_P4	I		10/100 PHY Port #4 RXN
P9	EPHY_RXP_P4	I		10/100 PHY Port #4 RXP
M9	EPHY_TXN_P4	O		10/100 PHY Port #4 TXN
L9	EPHY_TXP_P4	O		10/100 PHY Port #4 TXP
Misc signals: 2 pins				

Pin	Name	I/O/IPU/IPD	Driving	Description
C10	PORST_N	I, IPU	2 mA	Power On Reset
K1	WLAN_LED_N	O, IPD	4 mA	WLAN Activity LED
USB PHY interface: 5 pins				
N11	UPHY0_VDDA_V33A	P		3.3 V USB PHY analog power supply
P13	UPHY0_VDDL_V12D	P		1.2 V USB PHY digital power supply
P11	UPHY0_VRES	I/O		Connects to an external 8.2K Ohm resistor for band-gap reference circuit.
N12	UPHY0_PADM	I/O		USB data pin Data-
P12	UPHY0_PADP	I/O		USB data pin Data+
SDRAM Interface: 40 pins				
F14	MD15	I/O	4/8 mA	SDRAM Data bit #15
G13	MD14	I/O	4/8 mA	SDRAM Data bit #14
F13	MD13	I/O	4/8 mA	SDRAM Data bit #13
G12	MD12	I/O	4/8 mA	SDRAM Data bit #12
G11	MD11	I/O	4/8 mA	SDRAM Data bit #11
E14	MD10	I/O	4/8 mA	SDRAM Data bit #10
E13	MD9	I/O	4/8 mA	SDRAM Data bit #9
F12	MD8	I/O	4/8 mA	SDRAM Data bit #8
E12	MD7	I/O	4/8 mA	SDRAM Data bit #7
F11	MD6	I/O	4/8 mA	SDRAM Data bit #6
E11	MD5	I/O	4/8 mA	SDRAM Data bit #5
D14	MD4	I/O	4/8 mA	SDRAM Data bit #4
D13	MD3	I/O	4/8 mA	SDRAM Data bit #3
D12	MD2	I/O	4/8 mA	SDRAM Data bit #2
D11	MD1	I/O	4/8 mA	SDRAM Data bit it #1
E10	MD0	I/O	4/8 mA	SDRAM Data bit #0
L13	MA12	I/O	4/8 mA	SDRAM Address bit #12
K12	MA11	I/O	4/8 mA	SDRAM Address bit #11
L14	MA10	I/O	4/8 mA	SDRAM Address bit #10
J11	MA9	I/O	4/8 mA	SDRAM Address bit #9
K13	MA8	I/O	4/8 mA	SDRAM Address bit #8
K14	MA7	I/O	4/8 mA	SDRAM Address bit #7
J12	MA6	I/O	4/8 mA	SDRAM Address bit #6
J13	MA5	I/O	4/8 mA	SDRAM Address bit #5
J14	MA4	I/O	4/8 mA	SDRAM Address bit #4
H11	MA3	I/O	4/8 mA	SDRAM Address bit #3
H12	MA2	I/O	4/8 mA	SDRAM Address bit #2
H13	MA1	I/O	4/8 mA	SDRAM Address bit #1
G14	MA0	I/O	4/8 mA	SDRAM Address bit #0
M14	MBA1	I/O	4/8 mA	SDRAM MBA #1
L12	MBA0	I/O	4/8 mA	SDRAM MBA #0
L11	MRAS_N	I/O	4/8 mA	SDRAM MRAS_N
C12	MCAS_N	I/O	4/8 mA	SDRAM MCAS_N
C13	MWE_N	I/O	4/8 mA	SDRAM MWE_N
H14	MCLK	I/O	8/12 mA	SDRAM MCK
C11	MCKE	I/O	4/8 mA	SDRAM MCKE

Pin	Name	I/O/IPU/IPD	Driving	Description
M13	MDQM1	I/O	4/8 mA	SDRAM MDQM#1
J10	MDQM0	I/O	4/8 mA	SDRAM MDQM#0
K11	MCS0_N	I/O	4/8 mA	SDRAM MCS0_N
C14	MCS1_N	I/O	4/8 mA	SDRAM MCS1_N
LDO pins: 10 pins				
G2	LDO_V18A	P		1.8 V power input for internal MOS
G1	VOUT_1P2	P		1.2 V regulation output
G3	LDOSEL	I		Internal/External LDO select Default: floating, use internal Tied to 3.3V: use externally.
H3	EXT_LDO_1P2	P		Gate drive for external BJT
H2	DCDC_V33A	P		3.3 V analog power
G4	COMP	A		This pin is the error amplifier output and combines with the FB pin to compensate the voltage control.
H4	FB	A		Programmable feedback reference voltage for SW regulator and compensation network of the error amplifier
H1	UGATE	A		Gate drive for external upper MOSFET
J1	LGATE	A		Gate drive for external lower MOSFET
J2	DCDC_V33D	P		3.3 V power supply only for gate driver of SW (Ipeak<200 mA; Iavg<20 mA)
PLL interface: 2 pins				
B10	PLL_DVDD_V12D	P		1.2 V digital power supply to PLL
A10	PLL_AVDD_V12A	P		1.2 V analog power supply to PLL
RF interface, related LDO and power pins: 22 pins				
A2	WL_RF0_2G_INP	I		2.4 GHz RX0 input (positive)
A3	WL_RF0_2G_INN	I		2.4 GHz RX0 input (negative)
B1	WL_RF0_PA_V33P	P		3.3 V supply for RF channel 0
C1	WL_RF0_PA_OUTP	O		2.4 GHz TX PA output (negative)
D1	WL_RF0_PA_OUTN	O		2.4 GHz TX0 output (negative)
E1	WL_RF0_PA_V33N	P		3.3 V supply for RF channel 0
E3	WL_RF0_PA1_V33A	P		3.3 V supply for RF0 PA1
B5	WL_RF0_IF_V12A	P		1.2 V supply for IF0
B3	WL_RF0_RF_V12A	P		1.2 V supply for RF0
B9	WL_ADC_V12	P		1.2 V supply for ADC analog blocks
A5	WL_RF_BB1_V12A	P		1.2 V supply for analog baseband
C9	WL_RF_BB2_V12A	P		1.2 V supply for analog baseband

Pin	Name	I/O/IPU/IPD	Driving	Description
B8	WL_BG_RES_12K	I/O		External reference resistor (12K ohm)
A9	WL_BG_V33A	P		3.3 V supply for band gap reference
C8	WL_LDORF_OUT_V12	O		LDO 1.2V 200 mA output for RF core
C7	WL_LDOPLL_OUT_V12	O		LDO 1.2V 200 mA output for PLL core
A8	WL_LDORF_IN_VX	I		LDO 1.5~2 V 300 mA input for RF core and PLL
A7	WL_PLL_X1	I		Crystal oscillator input
B7	WL_PLL_X2	O		Crystal oscillator output
B6	WL_PLL_V12A	P		1.2V Supply for PLL
A6	WL_PLL_VC_CAP	I/O		PLL external loop filter
C6	WL_VCO_VCO_V12A	P		1.2 V Supply for VCO output buffer
Other power pins: 14 pins				
F5,G5,D10	SOC_IO_V33D	P		3.3 V digital I/O power supply
F10,G10,H10	SDRAM_IO_V33D	P		3.3 V/1.8 V SDRAM I/O power supply
H5,J5,F9,G9,H9	SOC_CO_V12D	P		1.2 V digital core power supply
K5,K6,K7	EPHY_V33A	P		3.3 V I/O power supply for EPHY
Ground pins: 51 pins				
A1, A4,B2,B4, C2,C3,C4,C5, D2, D3,D4,D5, D6,D7,D8,D9, E2,E4,E5,E6, E7,E8,E9, F1, F2,F3,F4,F6, F7,F8,G6,G7, G8,H6,H7,H8, J6,J7,J8,J9, K9,K10,L10,M10, M11,M12,N10,N13, N14,P10,P14	GND	G		Ground pin
	Total: 196 pins			

*NOTE:
1. IPD means internal pull-down; IPU means internal pull-up; P means power.
2. When SPI_CS1 acts as WATCH DOG RESET, a pull-high resistance is necessary.

1.3 Pin Sharing Scheme

Some pins are shared with GPIO to provide maximum flexibility for system designers. The RT5350 provides up to 28 GPIO pins. Users can configure SYSCFG and GPIOMODE registers in the System Control block to specify the pin function. Unless it specified explicitly, all the GPIO pins are in input mode after reset.

Table 1-4 GPIO Share Scheme

I/O Pad Group	Normal Mode	GPIO Mode
SPI_CS1	SPI_CS1	GPIO #27
SW_PHY_LED	EPHY_LED4_N	GPIO #26
	EPHY_LED3_N	GPIO #25
	EPHY_LED2_N	GPIO #24
	EPHY_LED1_N	GPIO #23
	EPHY_LED0_N	GPIO #22
JTAG	JTAG_TRST_N	GPIO #21
	JTAG_TCLK	GPIO #20
	JTAG_TMS	GPIO #19
	JTAG_TDI	GPIO #18
	JTAG_TDO	GPIO #17
UARTL	RXD2	GPIO #16
	TXD2	GPIO #15
UARTF	RIN	GPIO #14
	DSR_N	GPIO #13
	DCD_N	GPIO #12
	DTR_N	GPIO #11
	RXD	GPIO #10
	CTS_N	GPIO #9
	TXD	GPIO #8
	RTS_N	GPIO #7
SPI	SPI_MISO	GPIO #6
	SPI_MOSI	GPIO #5
	SPI_CLK	GPIO #4
	SPI_CS0	GPIO #3
I2C	I2C_SCLK	GPIO #2
	I2C_SD	GPIO #1
GPIO	GPIO0	GPIO #0

Table 1-5 UARTF Pin Sharing Scheme

UARTF_SHARE_MODE / Pin Name	3'b000 UARTF	3'b001 PCM, UARTF	3'b010 PCM, I^2S	3'b011 I^2S UARTF	3'b100 PCM, GPIO	3'b101 GPIO, UARTF	3'b110 GPIO I^2S	3'b111 GPIO (default)
RIN	RIN	PCMDTX	PCMDTX	RXD	PCMDTX	GPIO#14	GPIO#14	GPIO#14
DSR_N	DSR_N	PCMDRX	PCMDRX	CTS_N	PCMDRX	GPIO#13	GPIO#13	GPIO#13
DCD_N	DCD_N	PCMCLK	PCMCLK	TXD	PCMCLK	GPIO#12	GPIO#12	GPIO#12
DTR_N	DTR_N	PCMFS	PCMFS	RTS_N	PCMFS	GPIO#11	GPIO#11	GPIO#11
RXD	RXD	RXD	I2SSDI	I2SSDI	GPIO#10	RXD	I2SSDI	GPIO#10
CTS_N	CTS_N	CTS_N	I2SSDO	I2SSDO	GPIO#9	CTS_N	I2SSDO	GPIO#9
TXD	TXD	TXD	I2SWS	I2SWS	GPIO#8	TXD	I2SWS	GPIO#8
RTS_N	RTS_N	RTS_N	I2SCLK	I2SCLK	GPIO#7	RTS_N	I2SCLK	GPIO#7

Table 1-6 SPI_CS1 Pin Sharing Scheme: (SPI_CS1 _MODE)

SPI_CS1_MODE / Pin Name	2'b00	2'b01	2'b10 (default)
SPI_CS1	SPI_CS1	WDT_RST	GPIO#27

Table 1-7 MCS1 Pin Sharing Scheme: (REFCLK0_IS_OUT)

REFCLK0_IS_OUT / Pin Name	1'b0(default)	1'b1
MCS1	MCS1	REFCLK0_OUT

Table 1-8 EPHY_LED Pin Sharing Scheme: (EPHY_BT_GPIO_MODE)

EPHY_BT_GPIO_MODE / Pin Name	2'b00 (default) EPHY_LED	2'b01 GPIO	2'b10 BT_MODE
EPHY_LED4_N	EPHY_LED4_N	GPIO#26	BT_ANT
EPHY_LED3_N	EPHY_LED3_N	GPIO#25	BT_WACT
EPHY_LED2_N	EPHY_LED2_N	GPIO#24	BT_FREQ
EPHY_LED1_N	EPHY_LED1_N	GPIO#23	BT_STAT
EPHY_LED0_N	EPHY_LED0_N	GPIO#22	BT_ACT

NOTE:
1. All given GPIO support a current strength of 4 mA.
2. The default direction for GPIO pins are input (i.e. tri-state), except for these GPIO pins:
   - The GPIO17~21 are shared with the JTAG interface.
   - The default value for JTAG_GPIO_MODE is '0'.

Table 1-9 Share Pin Function description

Pin Share Name	I/O	Share Pin Function description
PCMDTX	O	DATA signal from PCM's host to external codec
PCMDRX	I	DATA signal from external codec to PCM's host.
PCMCLK	I/O	PCM's clock, it can be generate by PCM's host(Output direction), or provide by external(input direction). The clock frequency should match to the slot configuration of PCM host. e.g. 4 slots, PCM clock out/in should be 256KHz. 8 slots, PCM clock out/in should be 512KHz. 16 slots, PCM clock out/in should be 1.024MHz. 32 slots, PCM clock out/in should be 2.048MHz. 64 slots, PCM clock out/in should be 4.096MHz. 128 slots, PCM clock out/in should be 8.192MHz.
PCMFS	I/O	SYNC signal of PCM. In our design, the direction of this signal is independent in the direction of PCMCLK. It's direction and mode is configurable.
I2SSDI	I	Data input
I2SSDO	O	Data output
I2SWS	I/O	Channel Selection (or Word selection)(as output in master, and input in slave mode)
I2SCLK	I/O	I2S clock (as output in master, and input in slave mode)
BT_ACT	I/	Blue tooth active. (can be treated as a request)
BT_STAT	I/	TX or RX
BT_FREQ	I/	Blue tooth overlap WLAN band or not
BT_WACT	/O	WLAN is active. (can be treated as a grant)
BT_ANT	/O	Antenna select
WDT_RST	/O	Watchdog timeout reset
REFCLK0_OUT	/O	REFCLK0 output

1.4 Boot strapping description

Table 1-10 Boot Strapping Description From Signal Pad

Pin Name	Boot Strapping Signal Name	Description
SPI_CLK	XTAL_FREQ_HI	0: 20 MHz (default) 1: 40 MHz
WLAN_LED_N	BIGENDIAN	0: Little endian (default) 1: Big endian
EPHY_LED4_N	DRAM_FROM_EE	0: DRAM configuration from boot strapping.(default) 1: DRAM configuration(size/width) from EEPROM
{ EPHY_LED3_N, EPHY_LDE2_N}	DRAM_SIZE	INIC/AP(SDR) 0: 2 MB/8 MB (default) 1: 8 MB/16 MB 2: 16 MB/32 MB, 32 MB*2 3: 32 MB
{EPHY_LED1_N, EPHY_LED0_N}	CPU_CLK_SEL	CPU Clock Select 0: 360 Mhz (default) 1: Reserved 2: 320 Mhz 3: 300 Mhz
{ SPI_MOSI , TXD2, TXD}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. In non-test/debug operation, 0: Normal mode (boot from SPI serial flash) (default) 1: iNIC-USB mode 2: Reserved 3: Reserved 4: Reserved 5: iNIC-PHY mode (Only Port 0 can support this mode) 6: Scan mode 7: Debug/test mode

2 Maximum Ratings and Operating Conditions (TBD)

2.1 Absolute Maximum Ratings

Supply Voltage ..... 3.6 V
Vcc to Vcc Decouple..... –0.3 to +0.3 V
Input, Output or I/O Voltage.....GND –0.3 V to Vcc+0.3 V

2.2 Thermal Information

Maximum Junction Temperature (Plastic Package) .....125 °C
Maximum Lead Temperature (Soldering 10 s).....260 °C
Thermal characteristics without external heat sink in still air conditions
Thermal Resistance θJA (oC/W) for JEDEC 2L system PCB .....36.4 °C /W
Thermal Resistance θJA (oC/W) for JEDEC 4L system PCB .....26.3 °C /W
Thermal Resistance θJC (oC/W) for JEDEC 2L system PCB .....7.1 °C /W
Thermal Resistance θJC (oC/W) for JEDEC 4L system PCB .....6.9 °C /W
Thermal Characterization parameter ΨJt (oC/W) for JEDEC 2L system PCB .....2.4 °C /W
Thermal Characterization parameter ΨJt (oC/W) for JEDEC 4L system PCB .....1.7 °C /W

NOTE: JEDEC 51-9 system FR4 PCB size: 101.5x114.5mm (4”x4.5”)

2.3 Operating Conditions

Temperature Range .....-10 to 55 °C

2.4 Storage Condition

The calculated shelf life in a sealed bag is 12 months if stored between 0 °C and 40 °C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- Mounted within 168 hours of factory conditions < 30 °C /60% RH.
- Storage humidity needs to maintained at <10% RH.
- Baking is necessary if customer exposes the component to air over 168 hrs, baking condition: 125 °C / 8 hrs.

2.5 External Xtal Specfications

Frequency ..... 20 MHz/ 40 MHz
Frequency offset .....+/-20 ppm
VIH/VIL .....Vcc-0.3 V / 0.3 V
Duty Cycle .....45%~55%

2.6 DC Electrical Characteristics

Table 2-1 DC Electrical Characteristics

Parameters	Sym	Conditions	Min	Typ	Max	Unit
3.3V Supply Voltage	Vcc33		3.0	3.3	3.6	V
1.5V Supply Voltage	Vcc15	*1	1.45		3.6	V
VOUT_1P2 Output Voltage	Vout12	*1,2	1.15	1.25	1.375	V
1.2V Core Supply VoltageSOC_CO_V12D)	Vcc12		1.14		1.32	V
3.3V Current Consumption (include integrated PA)	Icc33			460		mA
1.5V Current Consumption	Icc15			430		mA
1.8V Current Consumption (@transformer center tap)	Icc18	EPHY speed 100M		220		mA

*Note:1. PMU design specification range.
2. LDO output is adjustable by internal register and have +/- 5% tolerance

Table 2-2 DC characteristics for GPIO pins with 4mA driving capability

Symbol	Parameter	Min	Normal	Max
VIH	Input High Voltage	2		
VIL	Input Low Voltage			0.8
VOH	Output High Voltage	2.4		
VOL	Output Low Voltage			0.4
IOH	High Level Output Current @VOH(min) (mA)	9.7	18.8	31.0
IOL	Low Level Output Current @VOL(max) (mA)	6.5	10.5	14.5

Table 2-3 DC characteristics for GPIO pins with 8mA driving capability

Symbol	Parameter	Min	Normal	Max
VIH	Input High Voltage	2		
VIL	Input Low Voltage			0.8
VOH	Output High Voltage	2.4		
VOL	Output Low Voltage			0.4
IOH	High Level Output Current @VOH(min) (mA)	14.0	27.2	44.9
IOL	Low Level Output Current @VOL(max) (mA)	9.8	15.6	21.6

2.7 AC Electrical Characteristics

Table 2-4 RF Receiver

Parameters	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
RF Frequency Range		2400		2500	MHz
RX Sensitivity (Measured at main antenna port)	CCK1M		-93		dBm
	CCK11M		-88		
	OFDM6M		-90		
	OFDM54M		-75		
	HT20, MCS7		-72		
	HT40, MCS7		-68		
RX Sensitivity (Measured at diversity antenna port)	CCK1M		-95		dBm
	CCK11M		-90		
	OFDM6M		-91		
	OFDM54M		-76		
	HT20, MCS7		-75		
	HT40, MCS7		-71		
Input P1dB	lna_gain<1:0> = 11		-40		dBm
	lna_gain<1:0> = 10		-25		
	lna_gain<1:0> = 01		-10		
IQ Gain Imbalance	Measured at ADC Input		0.1		dB
IQ Phase Imbalance			< 2		deg
RX Maximum Input Level	OFDM54M		-13		dBm
	HT40, MCS7		-13		
	CCK1M		0		
Adjacent Channel Rejection	OFDM6M		34		dB
	OFDM54M		22		
	CCK		37		

Table 2-5 RF Receive

Parameters	Conditions	Min	Typ	Max	Unit
RF Frequency Range		2400		2500	MHz
Output Power (Measured at antenna port)	CCK1M (Mask Compliant)		+19		dBm
	OFDM6M (Mask Compliant)		+20		
	OFDM54M for -30 dB EVM		+15		
	HT40, MCS7 for -30 dB EVM		+15		
Output P1dB	Measured at antenna		+25		dBm
ACPR (OFDM)	Pout=+15dBm, OFDM, 10MHz offset		48		dBc
Output Noise Floor	Pout=+15dBm, ALC Code = 010100		-120		dBm/Hz
LO Leakage	Pout=+18dBm		-50		dBm
Carrier Suppression			25		dBc
Single-Sideband Suppression	**w/o IQ calibration	33	40		dBc
Tx ALC Gain Control Step	6-bit control 00 to 27(HEX) = 39 levels		0.5		dB/step

2.7.1 SDRAM Interface

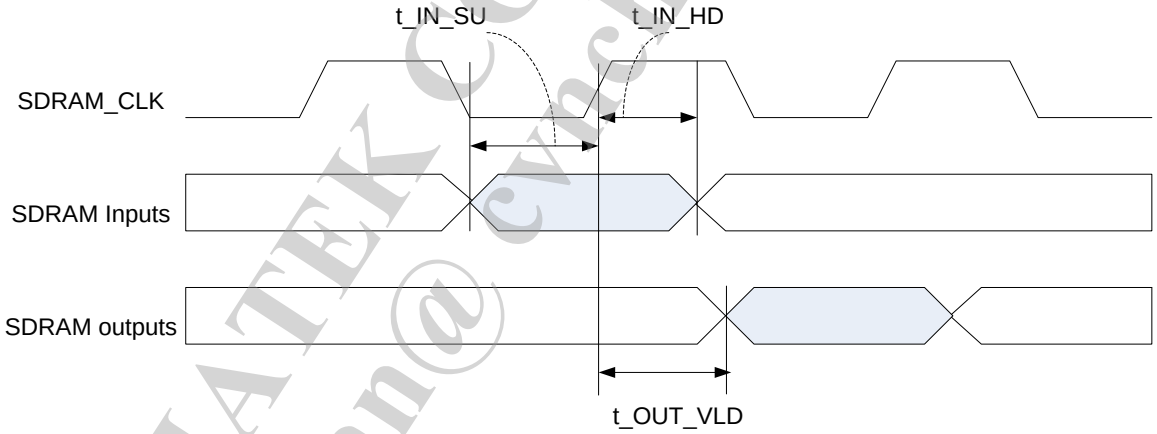


Figure 2-1 SDRAM Interface

Table 2-6 SDRAM Interface

Symbol	Description	Min	Max	Unit	Remark
t_IN_SU	Setup time for input signals (e.g. MD*)	1.5	-	ns	
t_IN_HD	Hold time for input signals	1.7	-	ns	
t_OUT_VLD	SDRAM_CLK to output signals (MA*, MD*, SDRAM_RAS_N,…) valid	0.8	5	ns	output load: 8 pF

2.7.2 Power On Sequence

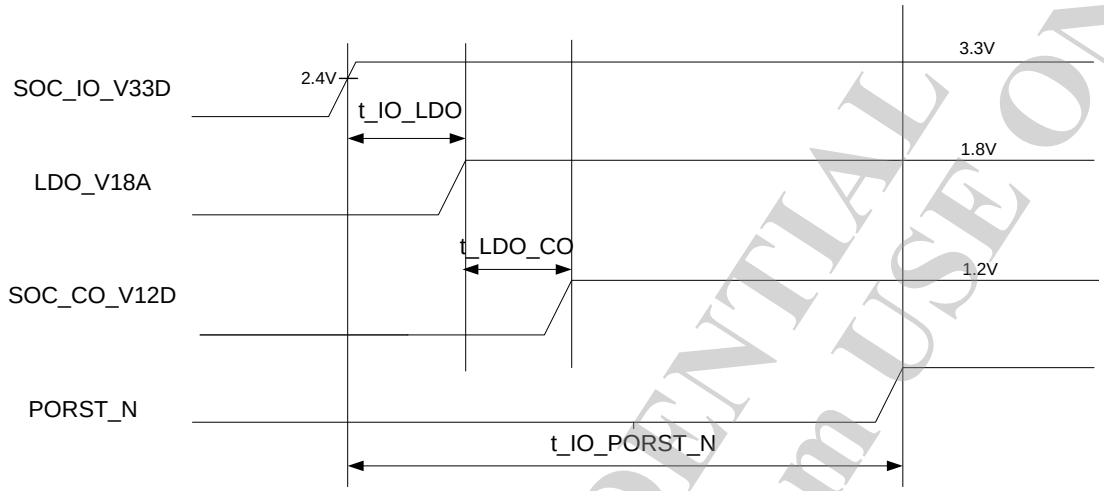


Figure 2-2 Power-On Sequence

Table 2-7 Power-On Sequence

Symbol	Description	Min	Max	Unit	Remark
t_IO_LDO	Time between ldo power on to io power on		3	ms	
t_LDO_CO	Time between core power on to ldo power on		3	ms	
t_IO_PORST_N	Time between I/O power on to PORST_N de-assertion	10	-	ms	

3 Function Description

3.1 Overview

The RT5350 SoC combines Ralink's 802.11n compliant 1T1R MAC/BBP/RF, a high performance 360 MHz MIPS24KEc CPU core and USB controller/PHY, to enable a multitude of high performance, cost-effective 802.11n applications.

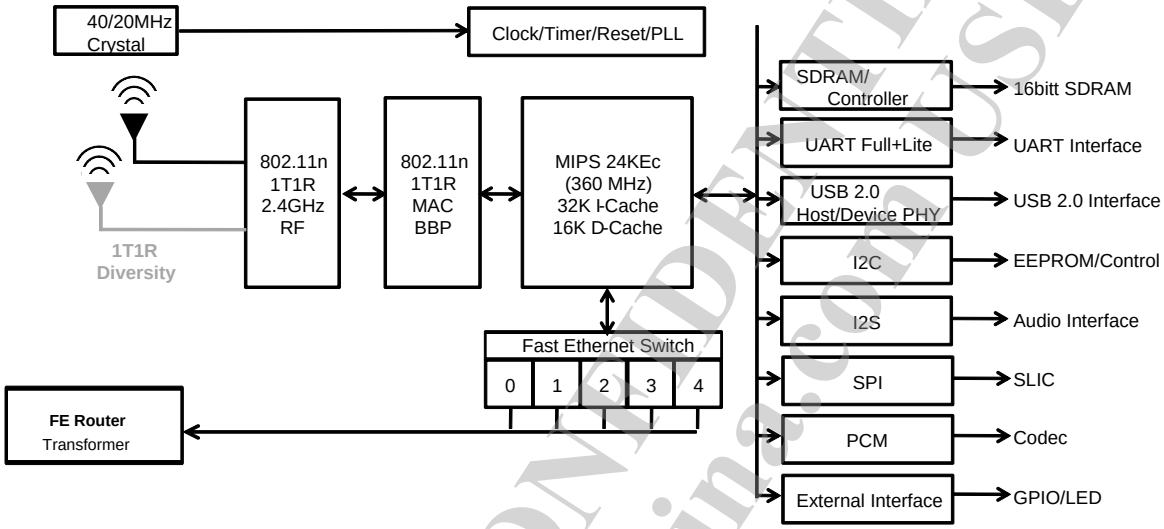


Figure 3-1 RT5350 Block Diagram

There are several bus masters (MIPS 24K, USB Host/Device, and 802.11n MAC/BBP/RF) in the RT5350 SoC on a high performance, low latency Rbus, (Ralink Bus). In addition, the RT5350 SoC supports lower speed peripherals such as UART, GPIO, and SPI via a low speed peripheral bus (Pbus). The SDRAM controller is the only bus slave on the Rbus. It includes an advanced memory scheduler to arbitrate the requests from bus masters, enhancing the performance of memory access intensive tasks.

The RT5350 SoC embeds Ralink's market proven 802.11n 1T1R MAC/BBP/RF to provide a 150 Mbps PHY rate on the wireless LAN interface. The MAC design employs a highly efficient DMA engine and hardware data processing accelerators, which free the CPU for user applications. The 802.11n 1T1R MAC/BBP/RF is designed to support international regulations and standards based features in the areas of security and quality of service, resulting in an enhanced end user experience.

3.2 Memory Map Summary

3-1 Memory Map

Start		End	Size	Description
0000.0000	-	03FF.FFFF	64 Mbps	SDRAM 64 MB
0400.0000	-	0FFF.FFFF	192 Mbps	Reserved
1000.0000	-	1000.00FF	256 Mbps	SYSCTL
1000.0100	-	1000.01FF	256 Mbps	TIMER
1000.0200	-	1000.02FF	256 Mbps	INTCTL
1000.0300	-	1000.03FF	256 Mbps	MEM_CTRL (SDR)
1000.0400	-	1000.04FF	256 Mbps	<<Reserved>>
1000.0500	-	1000.05FF	256 Mbps	UART
1000.0600	-	1000.06FF	256 Mbps	PIO
1000.0700	-	1000.07FF	256 Mbps	<<Reserved>>
1000.0800	-	1000.08FF	256 Mbps	<<Reserved>>
1000.0900	-	1000.09FF	256 Mbps	I2C
1000.0A00	-	1000.0AFF	256 Mbps	I2S
1000.0B00	-	1000.0BFF	256 Mbps	SPI
1000.0C00	-	1000.0CFF	256 Mbps	UARTLITE
1000.0D00	-	1000.0DFF	256 Mbps	MIPS CNT
1000.2000	-	1000.27FF	2 Kbps	PCM (up to 2 channels)
1000.2800	-	1000.2FFF	2 Kbps	Generic DMA (up to 16 channels)
1000.3000	-	1000.37FF	2 Kbps	<<Reserved>>
1000.3800	-	1000.3FFF	2 Kbps	<<Reserved>>
1000.4000	-	100F.FFFF		<<Reserved>>
1010.0000	-	1010.FFFF	64 Kbps	Frame Engine
1011.0000	-	1011.7FFF	32 Kbps	Ethernet switch
1011.8000		1011.BFFF	16 Kbps	ROM
1011.C000	-	1011.FFFF	16 Kbps	<<Reserved>>
1012.0000	-	1012.7FFF	16 Kbps	USB device
1012.8000	-	1012.FFFF	16 Kbps	<<Reserved>>
1013.0000	-	1013.7FFF	32 Kbps	<<Reserved>>
1013.8000	-	1013.FFFF	32 Kbps	<<Reserved>>
1014.0000	-	1017.FFFF	256 Kbps	<<Reserved>>
1018.0000	-	101B.FFFF	256 Kbps	802.11n MAC/BBP
101C.0000	-	101F.FFFF	256 Kbps	USB Host
1020.0000	-	1023.FFFF	256 Kbps	<<Reserved>>
1024.0000	-	1027.FFFF	256 Kbps	<<Reserved>>
1028.0000	-	1BFF.FFFF		<<Reserved>>
1C00.0000	-	1C00.3FFF	16 KB ROM	When system is powered on, the 16 KB internal boot ROM is mapped.

3.3 MIPS 24 Kbps Processor

3.3.1 Features

- 8-stage pipeline
- 32-bit address paths
- 64-bit data paths to caches and external interface
- MIPS32 -compatible instruction set
- Multiply-Accumulate and Multiply-Subtract instructions (MADD, MADDU, MSUB, MSUBU)
- Targeted Multiply instructions (MUL)
- Zero/One detect instructions (CLZ, CLO)
- Wait instructions (WAIT)
- Conditional Move instructions (MOVZ, MOVN)
- Prefetch instructions (PREF)
- MIPS32 Enhanced Architecture (Release 2) features
- Vectored interrupts and support for an external interrupt controller
- Programmable exception vector base
- Atomic interrupt enable/disable
- GPR shadow registers (optionally, one or three additional shadows can be added to minimize latency for interrupt handlers)
- Bit field manipulation instructions
- MIPS32 privileged resource architecture
- MIPS DSP ASE
- Fractional data types (Q15, Q31)
- Saturating arithmetic
- SIMD instructions operate on 2x16b or 4x8b simultaneously
- 3 additional pairs of accumulator registers
- Programmable memory management unit
- 32 dual-entry JTLB with variable page sizes
- 4-entry ITLB
- 8-entry DTLB
- Optional simple Fixed Mapping Translation (FMT) mechanism
- MIPS16e™ code compression
- 16-bit encodings of 32-bit instructions to improve code density
- Special PC-relative instructions for efficient loading of addresses and constants
- SAVE & RESTORE macro instructions for setting up and tearing down stack frames within subroutines
- Improved support for handling 8 and 16-bit datatypes
- Programmable L1 cache sizes
- Instruction cache size: 32 KB
- Data cache size: 16 KB
- 4-Way set associative
- Up to 8 outstanding load misses
- Write-back and write-through support
- 32-byte cache line size

3.3.2 Block Diagram

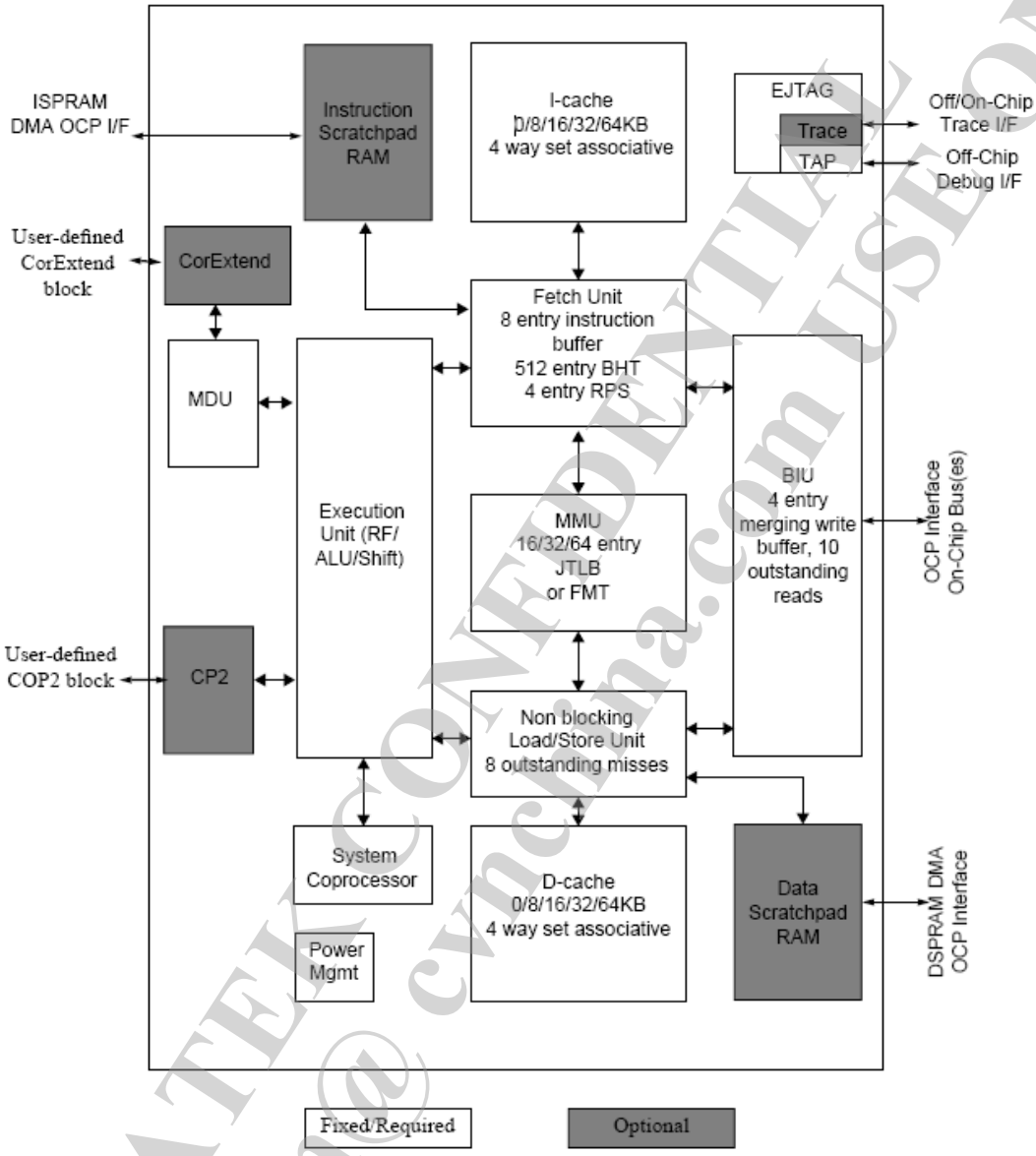


Figure 3-2 MIPS 24KEc Processor Diagram

3.3.3 Clock Plan

Table 3-2 Clock Plan

CPU	CPU: BUS (period)	BUS/SDR
360 MHz	1:3	120 MHz
320 MHz	1:4	80 MHz
300 MHz	1:3	100 MHz

3.4 System Control

3.4.1 Features

- Provides read-only chip revision registers.
- Provides a window to access boot-strapping signals.
- Supports memory remapping configurations.
- Supports software reset to each platform building block.
- Provides registers to determine GPIO and other peripheral pin muxing schemes.
- Provides some power-on-reset only test registers for software programmers.
- Combines miscellaneous registers (such as clock skew control, status register, and memo registers).

3.4.2 Block Diagram

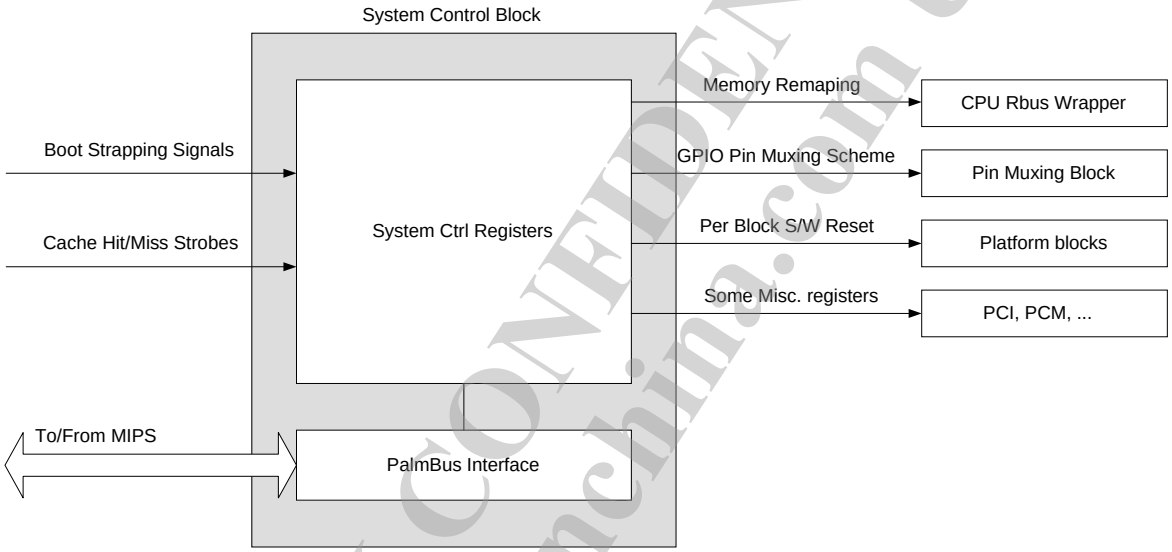


Figure 3-3 System Control Block Diagram

3.4.3 Register Description (base: 0x1000_0000)

CHIPID0_3: Chip ID ASCII Character 0-3 (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31:24	RO	CHIP_ID3	ASCII Chip Name Identification Character 3	0x33
23:16	RO	CHIP_ID2	ASCII Chip Name Identification Character 2	0x35
15:8	RO	CHIP_ID1	ASCII Chip Name Identification Character 1	0x54
7:0	RO	CHIP_ID0	ASCII Chip Name Identification Character 0	0x52

CHIPID4_7: Chip Name ASCII Character 4-7 (offset: 0x0004)

Bits	Type	Name	Description	Initial value
31:24	RO	CHIP_ID7	ASCII Chip Name Identification Character 7	0x20
23:16	RO	CHIP_ID6	ASCII Chip Name Identification Character 6	0x20
15:8	RO	CHIP_ID5	ASCII Chip Name Identification Character 5	0x30
7:0	RO	CHIP_ID4	ASCII Chip Name Identification Character 4	0x35

REVID: Chip Revision Identification (offset: 0x000c)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	-
11:8	RO	VER_ID	Chip Version Number	0x1
7:4	-	-	Reserved	-
3:0	RO	ECO_ID	Chip ECO Number	0x1

SYSCFG0: System Configuration Register 1 (offset: 0x0010)

Bits	Type	Name	Description	Initial value
31:24	BS	TEST_CODE	Test Code Default value is from bootstrap and can be modified by software.	-
23:19	-	-	Reserved	-
20	BS	XTAL_SEL	0: 20 MHz 1: 40 MHz	-
19	BS	BIG ENDIAN	0: Little endian 1: Big endian	-
18	BS	DRAM_FROM_EE	0: DRAM configuration from boot strapping. 1: DRAM configuration (size/width) from EEPROM	-
17	-	-	Reserved	-
16	-	-	Reserved	-
15	-	-	Reserved	-
14:12	BS	DRAM_SIZE	0: 2 MB 1: 8 MB 2: 16 MB 3: 32 MB 4: 64 MB 5-7: Reserved	-
11	-	-	Reserved	-
10	BS	CPU_CLK_SEL[1]		-
9	-	-	Reserved	-
8	BS	CPU_CLK_SEL[0]	CPU_CLK_SEL[1:0]: CPU/SYSCLK 0: 360/120 Mhz 1: -Reserved 2: 320/80 Mhz 3: 300/100 Mhz Default value is from bootstrap and the CPU PLL parameter can be modified by software, see CPU_PLL_DYN_CFG.CPU_CLK_SEL (offset: 0x48)	-
7:3	-	-	Reserved	-
2:0	BS	CHIP_MODE	A vector to set chip function/test/debug modes in non-test/debug operation. 0: Normal mode (AP mode) (default) 1: iNIC-USB mode 2-4: Reserved 5: iNIC PHY mode 6: Scan mode 7: Debug/test mode	-

SYSCFG1: System Configuration Register0 (offset: 0x0014)

Bits	Type	Name	Description	Initial value
27	-	-	Reserved	-
26	RW	PULL_EN	PAD Pull High/Low Enable 0: Disable 1: Enable	0x0
22:20	RW	SDR_PAD_DRV	SDRAM PAD Driving Strength SDR_PAD_DRV[2]: for MCLK PAD SDR_PAD_DRV[1] : for MD15-0 PAD SDR_PAD_DRV[0]: for other SDRAM control signal	0x0

			0: Low driving 1: High driving	
19:16	-	-	Reserved	-
13:11	-	-	Reserved	-
10	RW	USB0_HOST_MODE	0: Set USB #0 to device mode 1: Set USB #0 to host mode.	0x0
9	RW	USB_ISO_EN	USB PHY Isolation Enable In applications without USB, the UPHY_VDDL_V12D and UPHY_VDDA_V33A can be tied to GND to save UPHY power. In this application, set this bit to '1' to isolate.	0x0
3:1	-	-	Reserved	-
0	-	-	Reserved	-

TESTSTAT: Firmware Test Status Register (offset: 0x0018)

Bits	Type	Name	Description	Initial value
31:0	RW	TSETSTAT	Firmware Test Status NOTE: This register is reset only by a power-on reset.	0x0

TESTSTAT2: Firmware Test Status Register 2 (offset: 0x001c)

Bits	Type	Name	Description	Initial value
31:0	RW	TSETSTAT2	Firmware Test Status 2 NOTE: This register is reset only by a power-on reset.	0x0

Reserved Register (offset: 0x0020)

Bits	Type	Name	Description	Initial value
31:0	-	-	Reserved	0x0

Reserved Register (offset: 0x0024)

Bits	Type	Name	Description	Initial value
31:0	-	-	Reserved	0x0

Reserved Register (offset: 0x0028)

Bits	Type	Name	Description	Initial value
31:0	-	-	Reserved	0x0

CLKCFG0: Clock Configuration Register 0 (offset: 0x002c)

Bits	Type	Name	Description	Initial value
31:30	RW	SDRAM_CLK_SKEW	0: Zero delay 1: Delay 200 ps 2: Delay 400 ps 3: Delay 600 ps	0x1
29:23	-	-	Reserved	-
22:18	RW	INT_CLK_FDIV	The frequency divider used to generate the Fraction-N clock frequency. Valid values range from 1~31. Fraction-N clock frequency = (INT_CLK_FFRAC/INT_CLK_FDIV)*PLL_FREQ	0x08
17	-	-	Reserved	-
16:12	RW	INT_CLK_FFRAC	A parameter used in conjunction with INT_CLK_FDIV to generate the Fraction-N clock frequency. Valid values range from 0~31. Fraction-N clock Frequency =	0x0

			(INT_CLK_FFRAC/INT_CLK_FDIV)*PLL_FREQ	
11:9	RW	REFCLK0_RATE	0: 32 KHz 1: 12 MHz 2: 25 MHz 3: 40 MHz 4: 48 MHz 5: Reserved 6: Internal fraction-N_clk/2 7: Disable refclk output, MCS1 pin is in input mode if MCS1_AS_REFCLK0 = 1.	0x0
8	RW	MCS1_AS_REFCLK0	Controls whether MSC1 pin acts a a SDRAM chipset pin or outputs the frequency programmed in Reference Clock 0. 0: MCS1 1: Reference clock 0 output When this bit is '0', cs1 bank is accessible.	0x0
7:0	-	-	Reserved	-

CLKCFG1: Clock Configuration Register 1 (offset: 0x0030)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	-
30	-	-	Reserved	-
29	RW	SYS_TCK_EN	System Tick Enable	0x0
28:23	-	-	Reserved	-
23	RW	PDMA_CSR_CLK_GATE_BYP	PDMA CSR Clock Gating Bypass Control (for USB/WLAN/FE) 0: Disable bypass HW auto-clock gating control for power saving. 1: Bypass HW auto-clock gating control.	0x1
22	-	-	Reserved	-
21	-	-	Reserved	-
20	-	-	Reserved	-
19	-	-	Reserved	-
18	RW	UPHY0_CLK_EN	0: USB PHY0 clock is gated. 1: USB PHY0 clock is enabled.	0x1
17	-	-	Reserved	-
16	-	-	Reserved	-
15:0	-	-	Reserved	-

RSTCTRL: Reset Control Register (offset: 0x0034)

Bits	Type	Name	Description	Initial value
31:29	-	-	Reserved	-
28	RW	MIPS_CNT_RST	0: De-assert reset. 1: Reset the MIPS counter block.	0x0
27	-	-	Reserved	-
26	-	-	Reserved	-
25	RW	UDEV_RST	0: De-assert reset. 1: Reset the USB device block.	0x0
24	RW	EPHY_RST	0: De-assert reset. 1: Reset the Ethernet PHY block.	0x0
23	RW	ESW_RST	0: De-assert reset. 1: Reset the Ethernet switch block.	0x0
22	RW	UHST_RST	0: De-assert reset. 1: Reset the USB host block.	0x0

21	RW	FE_RST	0: De-assert reset. 1: Reset the frame engine block.	0x0
20	RW	WLAN_RST	0: De-assert reset. 1: Reset the RT2863 block.	0x0
19	RW	UARTL_RST	0: De-assert reset. 1: Reset the UART Lite block.	0x0
18	RW	SPI	0: De-assert reset. 1: Reset the SPI block.	0x0
17	RW	I2S	0: De-assert reset. 1: Reset the I^2S block.	0x0
16	RW	I2C	0: De-assert reset. 1: Reset the I^2C block.	0x0
15	-	-	Reserved	-
14	RW	DMA	0: De-assert reset. 1: Reset the DMA block.	0x0
13	RW	PIO	0: De-assert reset. 1: Reset the PIO block.	0x0
12	RW	UART_RST	0: De-assert reset. 1: Reset the UART block.	0x0
11	RW	PCM_RST	0: De-assert reset. 1: Reset the PCM block.	0x0
10	RW	MC_RST	0: De-assert reset. 1: Reset the Memory Controller block.	0x0
9	RW	INTC_RST	0: De-assert reset. 1: Reset the Interrupt Controller block.	0x0
8	RW	TIMER_RST	0: De-assert reset. 1: Reset the Timer block.	0x0
7:1	-	Reserved		-
0	W1C	SYS_RST	1: Reset the whole SoC.	0x0

RSTSTAT: Reset Status Register (offset: 0x0038)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	0x0
3	RC	SWCPURST	Software CPU reset occurred. This bit is set if software resets the CPU by writing to the RSTCPU bit in RSTCTL. Writing a '1' will clear this bit. Writing a '0' has no effect. NOTE : This register is reset only by a power-on reset.	0x0
2	RC	SWSYSRST	Software system reset occurred. This bit is set if software resets the chip by writing to the RSTSYS bit in RSTCTL. Writing a '1' will clear this bit. Writing a '0' has no effect. NOTE: This register is reset only by a power on reset.	0x0
1	RC	WDRST	Watchdog reset occurred. This bit is set if the watchdog timer resets the chip. Writing a '1' will clear this bit. Writing a '0' has nno effect. NOTE: This register is reset only by power-on reset.	0x0
0	-	-	Reserved	0x0

CPU_SYS_CLKCFG: CPU and SYS Clock Control (offset: 0x003c)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	0x0
30:24	RW	OCP_FDIV	The divider number of OCP (bus) clock frequency	0x03

			It is referenced when the CPU_OCP_RATIO is set to “3’b100”. The OCP bus clock will be CPU_FREQ/OCP_FDIV.	
23:20	-	-	Reserved	-
19:16	RW	CPU_OCP_RATIO	The ratio is system bus frequency compared to the CPU frequency. Value / Ratio (CPU : SYS) 4’b0000 Reserved 4’b0001 Reserved 4’b0010 2 : 1 4’b0011 Reserved 4’b0100 3 : 1 4’b0101 Reserved 4’b0110 4 : 1 4’b0111 5 : 1 4’b1000 10 : 1 NOTE: If the chip runs in USB OHCI mode, the OCP freqency cannot be lower than 12 MHz. It means that PLL_FREQ*(CPU_FFRAC/CPU_FDIV)/(CPU_OCP_RATIO+1) >= 30 MHz.	BS
15:13	-	-	Reserved	0x0
12:8	RW	CPU_FDIV	CPU Frequency Divider The frequency divider used to generate the CPU frequency. Input a value in the following equation to determine the CPU frequency. The value must be larger than or equal to CPU_FFRAC. Valid values range from 1~31. CPU frequency = (CPU_FFRAC/CPU_FDIV)*PLL_FREQ NOTE: If the chip runs in USB OHCI mode, the OCP frequency cannot be lower than 12 MHz. It means that PLL_FREQ*(CPU_FFRAC/CPU_FDIV)/(CPU_OCP_RATIO+1) >= 30 MHz.	0x01
7:5	-	-	Reserved	0x0
4:0	RW	CPU_FFRAC	CPU Frequency Fractional A parameter use in conjunction with the CPU frequency divider to determine the CPU frequency. Input a value in the following equation to determine the CPU frequency. Valid values range from 0~31. CPU frequency = (CPU_FFRAC/CPU_FDIV)*PLL_FREQ NOTE: If the chip runs in USB OHCI mode, the OCP freqency cannot be lower than 12 MHz. It means that PLL_FREQ*(CPU_FFRAC/CPU_FDIV)/(CPU_OCP_RATIO+1) >= 30 MHz.	0x01

CLK_LUT_CFG: CPU and SYS Clock Auto Control (offset: 0x0040)

Bits	Type	Name	Description	Initial value
31	RW	CLK_LUT_EN	Clock Lookup Table Enable 0: Disable 1: Enable	0x0
30:23	RW	LUT_CNT	The counter is used to count the period of the DRAM is idle. When the counter counts down to zero, the CPU clock automatically changes to a specified frequency. (360M*CPU_AUTO_FFRAC/CPU_AUTO_FDIV). The count period is ((AUTO_CNT+1)*16-1)us (range is from 15 us ~ 4095 us).	0x0
22:16	RW	LUT_OCP_FDIV	The divider number of OCP (bus) clock frequency in auto	0x03

			mode. It is referenced when CPU_AUTO_OCP_RATIO is set to "3'b100". The OCP bus clock is CPU_FREQ/AUTO_OCP_FDIV in auto-enable mode.	
15:13	RW	CPU_LUT_OCP_RATIO	The ratio is the system bus frequency compared to the CPU frequency. 3'b000: 1 : 1 (CPU : SYS) 3'b001: 1 : 2 (CPU : SYS) 3'b010: 1 : 3 (CPU : SYS) 3'b011: 1 : 4 (CPU : SYS) 3'b100: 1: AUTO_OCP_FDIV (Soft setting) NOTE: If the chip runs in USB OHCI mode, the OCP freqency cannot be lower than 12 MHz. It means that PLL_FREQ*(CPU_FFRAC/CPU_FDIV)/(CPU_OCP_RATIO+1) >= 30 MHz.	0x2
12:8	RW	CPU_LUT_FDIV	The frequency divider used to generate the CPUfrequency. Input this value into the equation below to determine the CPU frequency. The value must be larger than or equal to CPU_FFRAC. Valid values range from 1~31. CPU frequency = (CPU_FFRAC/CPU_FDIV)*PLL_FREQ NOTE: If the chip runs in USB OHCI mode, the OCP freqency cannot be lower than 12 MHz. It means that PLL_FREQ*(CPU_FFRAC/CPU_FDIV)/(CPU_OCP_RATIO+1) >= 30 MHz.	0x05
7:5	RW	LUT_FREQ_SCAL	Lookup table for clock frequency scaling 3'b100~3'b111: Reserved 3'b011: Sleep and RP results in scaling down of the clock frequency. 3'b010: Sleep results in scaling down of the clock frequency. 3'b001: RP results in scaling down of the clock frequency. 3'b000: The clock frequency scaling down is not introduced.	**0x0**
4:0	RW	CPU_LUT_FFRAC	CPU Frequency Fraction A parameter use in conjunction with the CPU frequency divider to determine the CPU frequency. Input a value in the following equation to determine the CPU frequency. Valid values range from 0~31. CPU frequency = (CPU_FFRAC/CPU_FDIV)*PLL_FREQ NOTE: If the chip runs in USB OHCI mode, the OCP frequency cannot be lower than 12 MHz. It means that PLL_FREQ*(CPU_FFRAC/CPU_FDIV)/(CPU_OCP_RATIO+1) >= 30 MHz.	0x01

CPU_PLL_DYN_CFG: CPU PLL Dynamic Configuration (offset: 0x0048)

Bits	Type	Name	Description	Initial value
31:25	RW	CPLL_F	CPLL Feedback Divider Control	BS
24:20	RW	CPLL_R	CPLL Divider Control	BS
19:18	RW	CPLL_OD	CPLL Output Divider Control	BS
17:16	RW	CPLL_BS	CPLL Output Band Control	BS
15:10	-	-	Reserved	-
9	-	-	Reserved	-
8	RW	CPLL_NEW_PARMS	CPLL uses new parameters (CPLL_F, CPLL_R, CPLL_OD, CPLL_BS).	0x0
7:3	-	-	Reserved	-
2	RW	CPLL_PD	Sets the CPU PLL into power-down mode.	0x0
1	RW	CPU_CLK_240M	Selects the CPU source clock from a temporary 240 Mhz clock.	0x0

			0: CPU clock runs according to CPU_CLK_SEL. 1: CPU clock runs at 240 Mhz.	
0	RO	CPLL_LD	Reads the CPLL lockdown status.	0x1

RF_RX_SD_CFG: RF Rx Signal Detection Power Saving Control (offset: 0x0058)

Bits	Type	Name	Description	Initial value
31	RW	RX_SD_EN	RX_SD_ACT Signal Control to RF Enable 0: Disable 1: Enable	0x0
30:15	-	-	Reserved	-
14:8	RW	ACT_TIME	The Active Time period control for RX_SD_ACT (range is 1~128 us). The period formula is (ACT_TIME + 1) * 1 us EX: ACT_TIME is "2", the RX_SD_ACT will be active for (2+1)*1 us = 3 us.	0x02
7	-	-	Reserved	-
6:0	RW	NONACT_TIME	The Non-active Time period control for RX_SD_ACT. (range is 1~128 us) The period formula is (NONACT_TIME + 1) * 1 us EX: NONACT_TIME is "127", the RX_SD_ACT will not active for (127+1)*1 us = 128 us.	0x7f

GPIOMODE: GPIO Purpose Select (offset: 0x0060)

Bits	Type	Name	Description	Initial value
31:23	-	-	Reserved	-
22:21	RW	SPI_CS1_MODE	Sets SPI_CS1 to act as a watchdog timeout pin. 2'b00: SPI_CS1 2'b01: Watchdog reset output (active low for 3 system clocks) 2'b10: GPIO mode 2'b11: Reserved	0x2
20:16	-	-	Reserved	-
15:14	RW	EPHY_BT_GPIO_MODE	00: Normal mode, as EPHY LED0-4 01: GPIO mode 10: BT mode 11: Reserved	0x0
13:7	-	-	Reserved	-
6	RW	JTAG_GPIO_MODE	0: Normal mode 1: GPIO mode	0x0
5	RW	UARTL_GPIO_MODE	0: Normal mode 1: GPIO mode	0x1
4:2	RW	UARTF_SHARE_MODE	UARF full interface is shared with PCM, I2S, GPIO. The detailed UARTF mode pin sharing is shown in the previous session.	0x7
1	RW	SPI_GPIO_MODE	0: Normal mode 1: GPIO mode	0x1
0	RW	I2C_GPIO_MODE	0: Normal mode 1: GPIO mode	0x1

PMU: (offset: 0x0088)

Bits	Type	Name	Description	Initial value
31:23	-	-	Reserved	-
22	RW	a_undisb	Under Voltage Monitor Function (default: 1)	0x1
21:20	-	-	Reserved	-

19:12	RW	a_vtune	Programmable output voltage level (default: <10100100>) MSB is read only and is fixed to 1'b1.	0xc9
11	-	-	Reserved	-
10:8	RW	a_dly	Output power MOSFET dead zone control (default: <011>)	0x3
7:4	RW	a_drven	Output power MOSFET driving control (default: <0100>)	0x4
3:0	-	-	Reserved	-

PMU1: (offset: 0x008c)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:16	RW	a_opt_ldolevel	IDO Output Level Selection MSB is read only and is fixed to 1'b1.	0xd6
15:8	RW	a_dig_ldolevel	IDO Output Level Selection MSB is read only and is fixed to 1'b1.	0x9b
7:0	-	-	Reserved	-

3.5 Timer

3.5.1 Features

- Independent clock pre-scale for each timer
- Independent interrupts for each timer
- Two general purpose timers
- Periodic mode
- Free-running mode
- Time-out mode
- Second timer may be used as watchdog timer
- Watchdog timer resets system on time-out
- Timer Modes
  - Periodic:
    In periodic mode, the timer counts down to zero from the load value. An interrupt is generated when the count is zero. After reaching zero, the load value is reloaded into the timer and the timer counts down again. A load value of zero disables the timer.
  - Timeout:
  - In timeout mode, the timer counts down to zero from the load value. An interrupt is generated when the count is zero. In this mode, the ENABLE bit is reset when the timer reaches zero, stopping the counter. After reaching zero, the load value is reloaded into the timer. A load value of zero disables the timer.
  - Free-running:
    In free-running mode, the timer counts down to zero from FFFFh. An interrupt is generated when the count is zero. After reaching zero, FFFFh is reloaded into the timer. This mode is identical to the periodic mode with a load value of 65535. However, it is worth noting that if firmware writes to the load value register in this mode, the timer still loads that value even though that value will be ignored thereafter. Also note that when the timer is first enabled, it will begin counting down from its current value, not necessarily FFFFh.
  - Watchdog:
    In watchdog mode, the timer counts down to zero from the load value. If the load value is not reloaded or the timer is not disabled before the count is zero, the chip is reset. When this occurs, every register in the chip is reset except the watchdog reset status bit WDRST in the RSTSTAT register in the system control block; it remains set to alert firmware of the timeout event when it re-executes its bootstrap.

3.5.2 Block Diagram

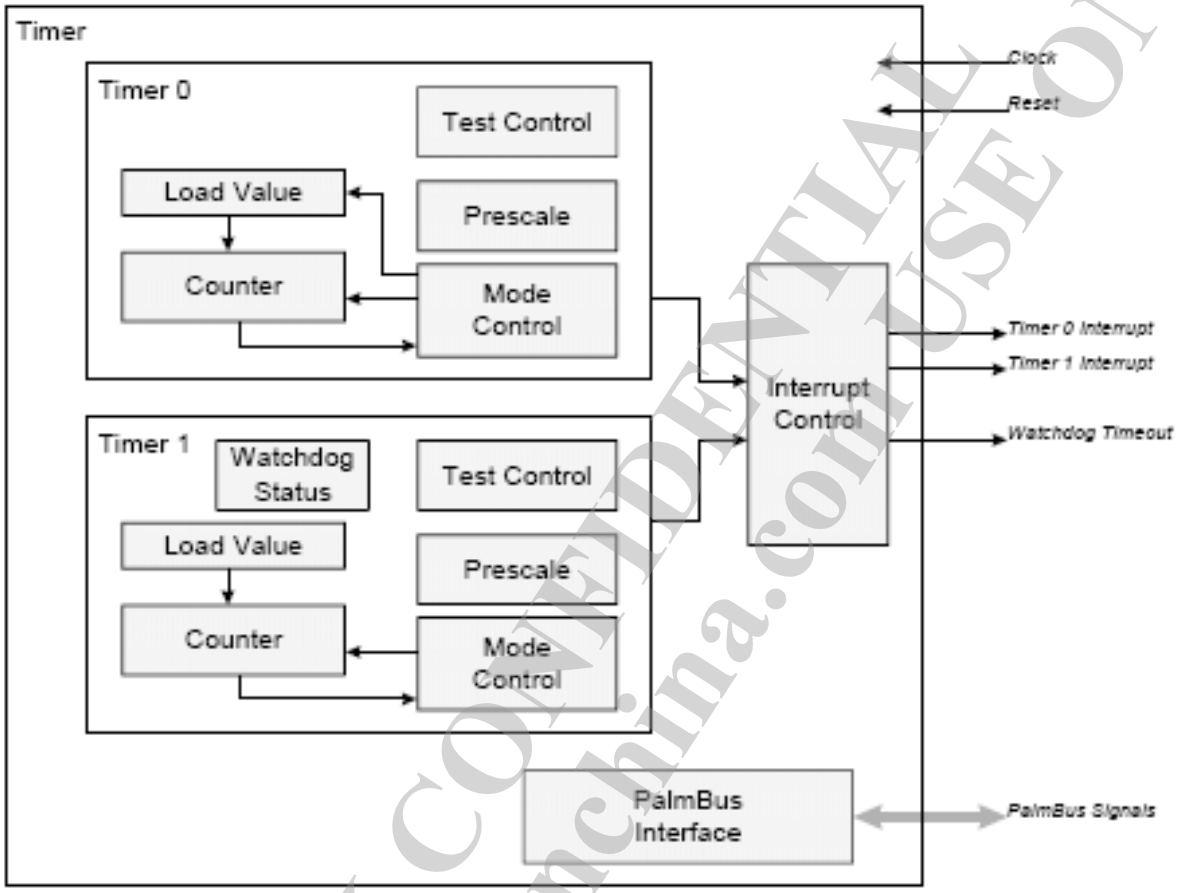


Figure 3-4 Timer Block Diagram

3.5.3 Register Description (base: 0x1000_0100)

TMRSTAT: Timer Status Register (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31:6	-	-	Reserved	-
5	WO	TMR1RST	Resets Timer 1 . Writing a '1' to this bit resets Timer 1 to 0xFFFF if in free-running mode, or the value specified in the TMR1LOAD register in all other modes. Writing a '0' to this bit has no effect. Reading this bit returns a '0'.	0x0
4	WO	TMR0RST	Resets Timer 0. Writing a '1' to this bit resets Timer 0 to 0xFFFF if in free-running mode, or the value specified in the TMR0LOAD register in all other modes. Writing a '0' to this bit has no effect. Reading this bit returns a '0'.	0x0
3:2	-	-	Reserved	-
1	W1C	TMR1INT	Timer 1 Interrupt Status This bit is set if Timer 1 has expired. The Timer 1 interrupt to the processor is set when this bit is '1'. Writing a '1' to this bit clears the interrupt. Writing a '0' has no effect.	0x0
0	W1C	TMR0INT	Timer 0 Interrupt Status This bit is set if Timer 0 has expired. The Timer 0 interrupt to the processor is set when this bit is '1'. Writing a '1' to this bit clears the interrupt. Writing a '0' has no effect.	0x0

TMR0LOAD: Timer 0 Load Value (offset: 0x0010)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	-
15:0	RW	TMRLOAD	Timer Load Value This register contains the load value for the timer. In all modes, this value is loaded into the timer counter when this register is written. In all modes except free-running mode, this value is reloaded into the timer counter after the timer counter reaches 0. It may be updated at any time; the new value will be written to the counter immediately. Writing a load value of 0 disables the timer, except in free-running mode.	0x0

TMR0VAL: Timer 0 Counter Value (offset: 0x0014)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	-
15:0	RO	TMRVAL	Timer Counter Value This register contains the current value of the timer. During functional operation, writes have no effect.	0xffff

TMR0CTL: Timer 0 Control (offset: 0x0018)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	-
15	RW	TESTEN	Reserved for test. This bit should be written with a '0'.	0x0
14:8	-	-	Reserved	-
7	RW	ENABLE	Timer Enable 0: Disable the timer. The timer stops counting and will retain its current value. 1: Enable the timer. The timer begins counting from its current value.	0x0
6	-	-	Reserved	-
5:4	RW	MODE	Timer Mode 0: Free-running 1: Periodic 2: Time-out 3: Time-out	0x0
3:0	RW	PRESCALE	Timer Clock Pre-scale These bits are used to scale the timer clock in order to achieve higher resolution or longer timer periods. Their definitions are below. Value / Timer Clock Frequency 0 / System clock 1 / System clock / 4 2 / System clock / 8 3 / System clock / 16 . / . . / System clock / 32768 14 / System clock /65536 15 / NOTE: The pre-scale value should not be changed unless the timer is disabled.	0x0

TMR1LOAD: Timer 1 Load Value (offset: 0x0020)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	-
15:0	RW	TMRLOAD	Timer Load Value This register contains the load value for the timer. In all modes, this value is loaded into the timer counter when this register is written. In all modes except free-running mode, this value is reloaded into the timer counter after the timer counter reaches '0'. It may be updated at any time; the new value will be written to the counter immediately. Writing a load value of '0' disables the timer, except in free-running mode.	0x0

TMR1VAL: Timer 1 Counter Value (offset: 0x0024)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	-
15:0	RO	TMRVAL	Timer Counter Value This register contains the current value of the timer. During functional operation, writes have no effect.	0xffff

TMR1CTL: Timer 1 Control (offset: 0x0028)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	-
15	RW	TESTEN	Reserved for test. This bit should be written with a '0'.	0x0
14:8	-	-	Reserved	-
7	RW	ENABLE	Timer Enable 0: Disable the timer. The timer stops counting and retains its current value. 1: Enable the timer. The timer begins counting from its current value.	0x0
6	RW	WD_TIMEOUT_SRC	Watchdog Timeout Alarm Source 0: From Timer 1 1: From PMU watchdog timer	0x0
5:4	RW	MODE	Timer Mode 0: Free-running 1: Periodic 2: Time-out 3: Watchdog	0x0
3	-	-	Reserved	-
2:0	RW	PRESCALE	Timer Clock Pre-scale These bits are used to scale the timer clock in order to achieve higher resolution or longer timer periods. Their definitions are below. Value / Timer Clock Frequency 0 / System clock 1 / System clock / 4 2 / System clock / 8 3 / System clock / 16 . / . . / . 14 / System clock / 32768 15 / System clock / 65536 NOTE: The pre-scale value should not be changed unless the timer is disabled.	0x0

3.6 Interrupt Controller

3.6.1 Features

- Supports a central point for interrupt aggregation for platform related blocks.
- Separated interrupt enable and disable registers.
- Supports global disable function.
- 2-level Interrupt priority selection.
- Each interrupt source can be directed to IRQ#0 or IRQ#1.

NOTE: RT5350 supports MIPS 24K's vector interrupt mechanism.
There are 6 hardware interrupts supported by MIPS 24K. The interrupt allocation is shown below:

Table 3-3 MIPS Hardware Interrupt Allocation

MIPS H/W Interrupt Pins	Connect to	Remark
HW_INT#5	Timer interrupt	Highest priority
HW_INT#4	802.11n NIC	
HW_INT#3	FE	
HW_INT#2	Reserved	
HW_INT#1	Other high priority interrupts (IRQ#1)	
HW_INT#0	Other low priority interrupts (IRQ#0)	Lowest priority

3.6.2 Block Diagram

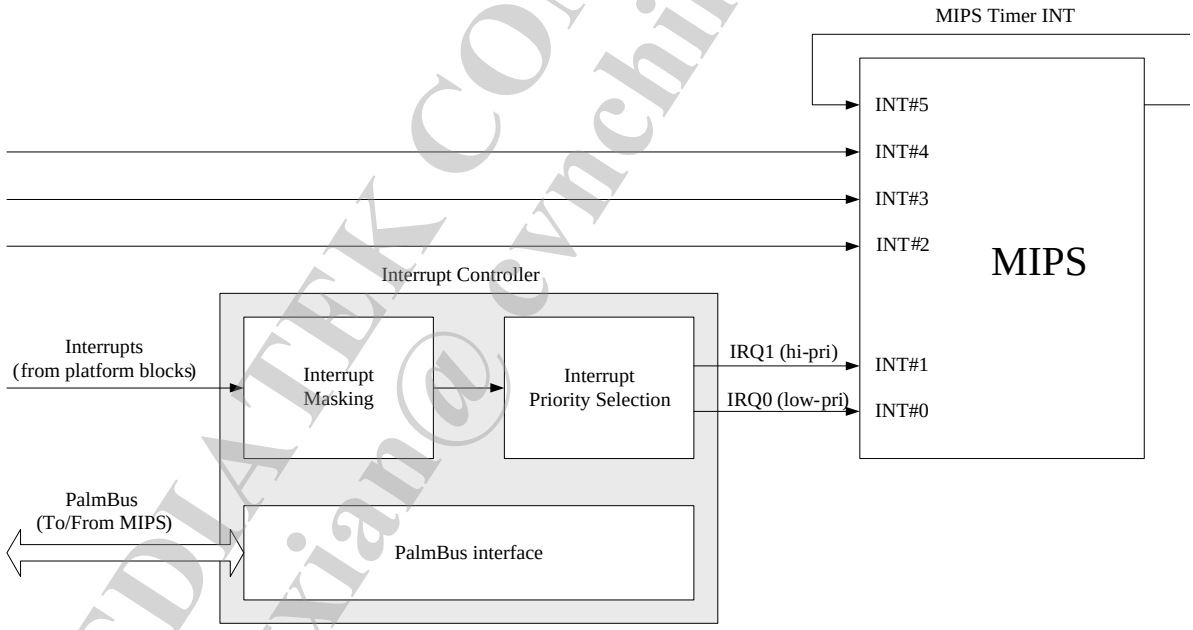


Figure 3-5 Interrupt Controller Block Diagram

3.6.3 Register Description (base: 0x1000_0200)

IRQ0STAT: Interrupt Type 0 Status After Enabling Mask (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	-
19	RO	UDEV	USB device interrupt status after mask	0x0
18	RO	UHST	USB host interrupt status after mask	0x0
17	RO	ESW	Ethernet switch interrupt status after mask	0x0
16	-	-	Reserved	-

15:13	-	-	Reserved	-
12	RO	UARTLITE	UARTLITE interrupt status after mask	0x0
11	RO	-	Reserved	-
10	RO	I2S	I^2S interrupt status after mask	0x0
9	RO	PC	MIPS performance counter interrupt status after mask	0x0
8	RO	-	Reserved	-
7	RO	DMA	DMA interrupt status after mask	0x0
6	RO	PIO	PIO interrupt status after mask	0x0
5	RO	UART	UART interrupt status after mask	0x0
4	RO	PCM	PCM interrupt status after mask	0x0
3	RO	ILL_ACC	Illegal access interrupt status after mask	0x0
2	RO	WDTIMER	Watchdog timer interrupt status after mask	0x0
1	RO	TIMER0	Timer 0 interrupt status after mask	0x0
0	RO	SYSCTL	System control interrupt status after mask	0x0

These bits are set if the corresponding interrupt is asserted from the source and with the following two conditions:

- The interrupt is not masked (bit not set in the INTDIS register).
- The interrupt type is set to INT0 (in the INTTYPE register).

NOTE: Writes to these bits are ignored and each bit cannot be simultaneously active in both the IRQ0STAT and IRQ1STAT registers.

IRQ1STAT: Interrupt Type 1 Status after Enable Mask (offset: 0x0004)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	-
19	RO	UDEV	USB device interrupt status after mask	0x0
18	RO	UHST	USB host interrupt status after mask	0x0
17	RO	ESW	Ethernet switch interrupt status after mask	0x0
16	-	-	Reserved	-
15:13	-	-	Reserved	-
12	RO	UARTLITE	UARTLITE interrupt status after mask	0x0
11	-	-	Reserved	-
10	RO	I2S	I^2S interrupt status after mask	0x0
9	RO	PC	MIPS Performance Counter interrupt status after mask	0x0
8	-	-	Reserved	-
7	RO	DMA	DMA interrupt status after mask	0x0
6	RO	PIO	PIO interrupt status after mask	0x0
5	RO	UART	UART interrupt status after mask	0x0
4	RO	PCM	PCM interrupt status after mask	0x0
3	RO	ILL_ACC	Illegal access interrupt status after mask	0x0
2	RO	WDTIMER	Watchdog Timer interrupt status after mask	0x0
1	RO	TIMER0	Timer 0 interrupt status after mask	0x0
0	RO	SYSCTL	System control interrupt status after mask	0x0

These bits are set if the corresponding interrupt is asserted from the source and with the following two conditions:

- The interrupt is not masked (bit not set in the INTDIS register).
- The interrupt type is set to INT1 (in the INTTYPE register).

NOTE: Writes to these bits are ignored and each bit cannot be simultaneously active in both the IRQ0STAT and IRQ1STAT registers.

INTTYPE: Interrupt Type (offset: 0x0020)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	-
19	RW	UDEV	USB device interrupt status type	0x0

18	RW	UHST	USB host interrupt status type	0x0
17	RW	ESW	Ethernet switch interrupt status type	0x0
16	-	-	Reserved	-
15:13	-	-	Reserved	-
12	RW	UARTLITE	UARTLITE interrupt status type	0x0
11	-	-	Reserved	-
10	RW	I2S	I^2S interrupt status type	0x0
9	RW	PC	MIPS performance counter interrupt status type	0x0
8	-	-	Reserved	-
7	RW	DMA	DMA interrupt status after type	0x0
6	RW	PIO	PIO interrupt status after type	0x0
5	RW	UART	UART interrupt status type	0x0
4	RW	PCM	PCM interrupt status type	0x0
3	RW	ILL_ACC	Illegal access interrupt status type	0x0
2	RW	WDTIMER	Watchdog timer interrupt status type	0x0
1	RW	TIMER0	Timer 0 interrupt status type	0x0
0	RW	SYSCTL	System control interrupt status type	0x0

These bits control whether an interrupt is IRQ0 or IRQ1. The interrupt type may be changed at any time; if the interrupt type is changed while the interrupt is active, the interrupt is immediately redirected.

INTRAW: Raw Interrupt Status Before Enabling Mask (offset: 0x0030)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	-
19	RO	UDEV	USB device interrupt status before mask	0x0
18	RO	UHST	USB host interrupt status before mask	0x0
17	RO	ESW	Ethernet switch interrupt status before mask	0x0
16	-	-	Reserved	-
15:13	-	-	Reserved	-
12	RO	UARTLITE	UARTLITE interrupt status before mask	0x0
11	RO	-	Reserved	-
10	RO	I2S	I^2S interrupt status before r mask	0x0
9	RO	PC	MIPS performance counter interrupt status before mask	0x0
8	-	-	Reserved	-
7	RO	DMA	DMA interrupt status before mask	0x0
6	RO	PIO	PIO interrupt status before mask	0x0
5	RO	UART	UART interrupt status before mask	-
4	RO	PCM	PCM interrupt status before mask	0x0
3	RO	ILL_ACC	Illegal access interrupt status before mask	0x0
2	RO	WDTIMER	Watchdog timer interrupt status before mask	0x0
1	RO	TIMER0	Timer 0 interrupt status before mask	0x0
0	RO	SYSCTL	System control interrupt status before mask	0x0

These bits are set if the corresponding interrupt is asserted from the source. The status bit is set if the interrupt is active, even if it is masked, and regardless of the interrupt type. This provides a single-access snapshot of all active interrupts for implementation of a polling system.

INTENA: Interrupt Enable (offset: 0x0034)

Bits	Type	Name	Description	Initial value
31	RW	GLOBAL	Global Interrupt Enable Writing a '1' to this bit allows interrupt masking to be performed based on each interrupt's individual enable mask. A read returns the global status ('1' if enabled).	0x0
30:20	-	-	Reserved	-
19	RW	UDEV	USB Device Interrupt Enable	0x0

18	RW	UHST	USB Host Interrupt Enable	0x0
17	RW	ESW	Ethernet Switch Interrupt Enable	0x0
16	-	-	Reserved	-
15:13	-	-	Reserved	-
12	RW	UARTLITE	UARTLITE Interrupt Enable	0x0
11	-	-	Reserved	-
10	RW	I2S	I^2S Interrupt Enable	0x0
9	RW	PC	MIPS Performance Counter Interrupt Enable	0x0
8	-	-	Reserved	-
7	RW	DMA	DMA Interrupt Enable	0x0
6	RW	PIO	PIO Interrupt Enable	0x0
5	RW	UART	UART Interrupt Enable	0x0
4	RW	PCM	PCM Interrupt Enable	0x0
3	RW	ILL_ACC	Illegal Access Interrupt Enable	0x0
2	RW	WDTIMER	Watchdog Timer Interrupt Enable	0x0
1	RW	TIMER0	Timer 0 Interrupt Enable	0x0
0	RW	SYSCTL	System Control Interrupt Enable	0x0

Writing a ‘1’ to these bits (except the GLOBAL bit) enables the mask for the corresponding interrupt. The interrupt is asserted and the bit is set in the IRQ0STAT or IRQ1STAT registers if an interrupt is enabled. Writes of '0' are ignored. Reading either the INTENA or INTDIS register returns the current mask, where an interrupt is masked (disabled) if the bit is ‘0, and unmasked (enabled) if the bit is ‘1.

INTDIS: Interrupt Disable (offset: 0x0038)

Bits	Type	Name	Description	Initial value
31	RW	GLOBAL	Disables the global interrupt. Writing a ‘1’ to this bit allows interrupt masking to be performed based on each interrupt’s individual disable mask. A read returns the global status (‘1’ if disabled).	0x0
30:20	-	-	Reserved	-
19	RW	UDEV	Disables the USB device interrupt status.	0x0
18	RW	UHST	Disables the USB host interrupt status.	0x0
17	RW	ESW	Disables the Ethernet switch interrupt.	0x0
16	-	-	Reserved	-
15:13	-	-	Reserved	-
12	RW	UARTLITE	Disables the UARTLITE interrupt.	0x0
11	-	-	Reserved	-
10	RW	I2S	Disables the I^2S interrupt.	0x0
9	RW	PC	Disables the MIPS performance counter interrupt.	0x0
8	RW	NAND	NAND flash controller interrupt.	0x0
7	RW	DMA	Disables the DMA interrupt.	0x0
6	RW	PIO	Disables the PIO interrupt.	0x0
5	RW	UART	Disables the UART interrupt.	0x0
4	RW	PCM	Disables the PCM interrupt.	0x0
3	RW	ILL_ACC	Disables the illegal access interrupt.	0x0
2	RW	WDTIMER	Disables the watchdog timer interrupt.	0x0
1	RW	TIMER0	Disables the Timer 0 interrupt.	0x0
0	RW	SYSCTL	Disables the system control interrupt.	0x0

Writing a ‘1’ to these bits (except the GLOBAL bit) disables the mask for the corresponding interrupt. The interrupt is asserted and the bit is set in the IRQ0STAT or IRQ1STAT registers if an interrupt is enabled. Writing '0' is ignored. Reading either the INTENA or INTDIS register returns the current mask, where an interrupt is masked (disabled) if the bit is ‘0, and unmasked (enabled) if the bit is ‘1’.

3.7 System Tick Counter

3.7.1 Register Description (base: 0x1000_0d00)

STCK_CNT_CFG: MIPS Configuration Register (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31:2	-	-	Reserved	0x0
1	RW	EXT_STK_EN	External System Tick Enable 0: Use MIPS internal timer interrupt. 1: Use external timer interrupt from external MIPS counter.	0x0
0	RW	CNT_EN	Counter Enable 0: Disable the free run counter. 1: Enable the free run counter.	0x0

CMP_CNT: MIPS Compare Register (offset: 0x0004)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:0	RW	CMP_CNT	If the free run counter equals the compare counter, then the timer circuit generates an interrupt. The interrupt remains active until the compare counter is written again.	0x0

CNT: MIPS Counter Register (offset: 0x0008)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:0	RW	CNT	The CPU busy counter increases by 1 every 20 us (50 KHz). Count is writable/readable and carries on counting from whatever value that is loaded into it.	0x0

3.8 UART

3.8.1 Features

- 16550-compatible register set, except for the divisor latch register.
- 5-8 data bits
- 1-2 stop bits (1 or 2 stop bits are supported with 5 data bits)
- Even, odd, stick, or no parity
- All standard baud rates up to 345600 b/s
- 16-byte receive buffer
- 16-byte transmit buffer
- Receive buffer threshold interrupt
- Transmit buffer threshold interrupt
- False start bit detection in asynchronous mode
- Internal diagnostic capabilities
- Break simulation
- Loop-back control for communications link fault isolation

3.8.2 Block Diagram

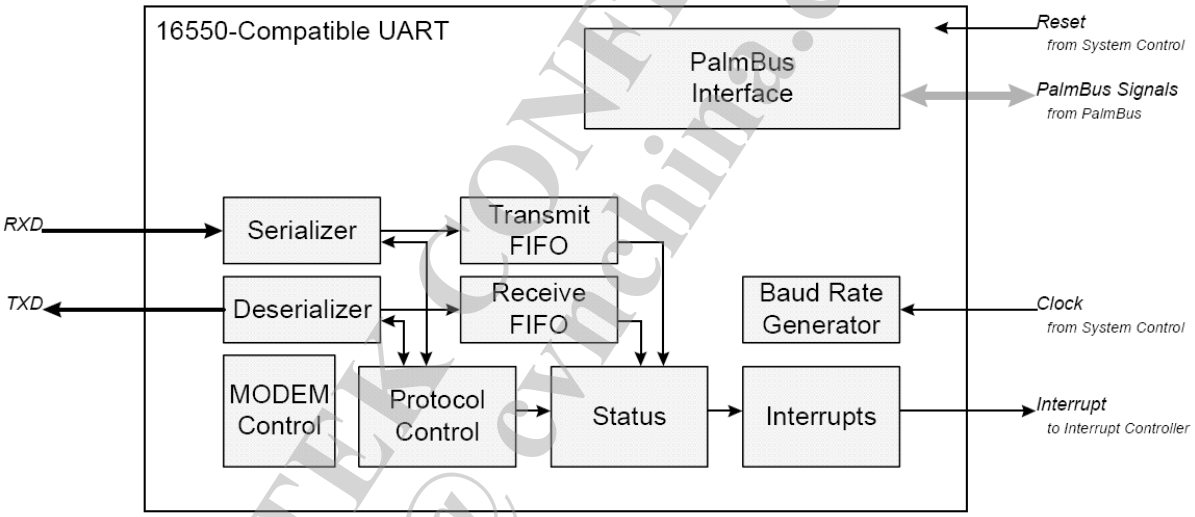


Figure 3-6 UART Block Diagram

3.8.3 Register Description (base: 0x1000_0500)

RBR: Receive Buffer Register (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7	RO	RXD[7:0]	Receive Buffer Data Data is transferred to this register from the receive shift register after a full character is received. If the contents of this register have not been read before another character is received, the OE bit in the LSR register is set, indicating a receive buffer overrun.	0x0

TBR: Transmit Buffer Register (offset: 0x0004)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7	WO	TXD[7:0]	Transmit Buffer Data When a character is written to this register, it is stored in the transmitter holding register. If the transmitter register is empty, the character is moved to the transmitter register, starting transmission.	0x0

IER: Interrupt Enable Register (offset: 0x0008)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	0x0
3	RW	EDSSI	Modem Interrupt Enable 1: Modem status (DCD, RI, DSR, CTS, DDCD, TERI, DDSR, and DCTS) interrupts. 0: Disable modem status (DCD, RI, DSR, CTS, DDCD, TERI, DDSR, and DCTS) interrupts.	0x0
2	RW	ELSI	Receiver Line Status Interrupt Enable 1: Enable line status (OE, PE, FE, and BI) interrupts. 0: Disable line status (OE, PE, FE, and BI) interrupts.	0x0
1	RW	ETBEI	Transmitter Buffer Line Status Interrupt Enable 1: Enable transmit buffer empty (THRE) interrupt. 0: Disable transmit buffer empty (THRE) interrupt.	0x0
0	RW	ERBFI	Receiver Buffer Empty Interrupt Enable 1: Enable data ready (DR) or character time-out interrupt. 0: Disable data ready (DR) or character time-out interrupt.	0x0

IIR: Interrupt Identification Register (offset: 0x000c)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:6	RO	FIFOENA[1:0]	FIFOs enabled These bits reflect the FIFO enable bit setting in the FIFO control register. When the FIFO enable bit is set, both of these bits are set high to a value of '11'. When the FIFO enable bit is cleared, both of these bits are set low to a value of '00'.	0x0
5:4	-	-	Reserved	0x0
3:1	RO	INTID[2:0]	Interrupt Identifier These bits provide a snapshot of the interrupt type, and may be used as the offset into an interrupt vector table. The interrupt encoding is given below. ID / Priority / Type / Source 7 / / Undefined / 6 / / Undefined / 5 / / Undefined / 4 / / Undefined / 3 / 1 / Receiver line status / OE,PE,FE,BI 2 / 2 / Receiver buffer full / DR 1 / 3 / Transmit buffer empty / THRE 0 / / Undefined / If more than one category of interrupt is asserted, only the highest priority ID will be given. The line and modem status interrupts are cleared by reading the corresponding status register (LSR, MSR). The receive buffer full interrupt is cleared when all of the data is read from the receiver buffer. The transmitter buffer empty is cleared when data is written to the TBR register. See also "Interrupt Priorities".	0x0
0	RO	INTPEND	Interrupt Pending 0: An interrupt bit is set and is not masked. 1: No interrupts are pending.	0x1

FCR: FIFO Control Register (offset: 0x0010)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:6	RW	RXTRIG[1:0]	Receiver Trigger Level The data ready interrupt (DR) is asserted when the receiver buffer depth is equal to the number of characters programmed in the trigger register. The trigger level encoding is as follows: RXTRIG / Trigger Level 0 / 1 1 / 4 2 / 8 3 / 14 NOTE: This register is not used if the receive FIFO is disabled.	0x0
5:4	RW	TXTRIG[1:0]	Transmitter Trigger Level The THRE interrupt is asserted if the transmitter buffer depth is less than or equal to the number of characters programmed in the trigger register. The trigger level encoding is as follows: TXTRIG / Trigger Level 0 / 1 1 / 4 2 / 8 3 / 12	0x0
3	RW	DMAMODE	DMA Transfer Enable This bit is writeable and readable, but has no other hardware function.	0x0
2	RW	TXRST	Transmitter Reset Writing a '1' to this bit clears the transmit FIFO and resets the transmitter status. The shift register is not cleared.	0x0
1	RW	RXRST	Receiver Reset Writing a '1' to this bit clears the receive FIFO and resets the receiver status. The shift register is not cleared.	0x0
0	RW	FIFOENA	0: The transmit and receive FIFOs have the effective depth of one character. 1: The transmit and receive FIFOs are enabled. NOTE: The FIFO status and data are automatically cleared when this bit is changed.	0x0

LCR: Line Control Register (offset: 0x0014)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7	RW	DLAB	Divisor Latch Access bit This bit has no functionality, and is retained for compatibility only	0x0
6	RW	SETBRK	Set Break Condition 0: Normal functionality. 1: Force TXD pin to '0'. Transmitter otherwise operates normally.	0x0
5	RW	FORCEPAR	Force Parity bit 0: Normal functionality. 1: If even parity is selected, the transmitted and checked parity is forced to '0'; if odd parity is selected, the transmitted and checked	0x0

			parity if forced to '1'.	
4	RW	EPS	Even Parity Select 0: Odd parity selected (checksum, including parity is '1'). 1: Even parity selected (checksum, including parity is '0'). NOTE: This bit is ignored if the PEN bit is '0'.	0x0
3	RW	PEN	Parity Enable 0: Parity is not transmitted or checked. 1: Parity is generated (transmitted), and checked (received).	0x0
2	RW	STB	Stop Bit Select 0: 1 stop bit is transmitted and received. 1: 1.5 stop bits are transmitted and received if WLS is '0'; 2 stop bits are transmitted and received if WLS is '1', '2', or '3'.	0x0
1:0:	RW	WLS[1:0]	Word Length Select 0: Each character is 5 bits in length. 1: Each character is 6 bits in length. 2: Each character is 7 bits in length. 3: Each character is 8 bits in length.	0x0

MCR: Modem Control Register (offset: 0x0018)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	0x0
4	RW	LOOP	Loopback Mode Enable 0: Normal operation. 1: The UART is put into loop-back mode, used for self-test: The TXD pin is driven high; the TXD signal connections are made internally. Signal / Wrapped back through… TXD / RXD DTRN / DSRN RTSN / CTSN OUT1N / RIN OUT2N / DCDN	0x0
3	RW	OUT2	Out2 Value 0: OUT2N pin is driven to a high level. 1: OUT2N pin is driven to a low level. NOTE: This bit is only functional in loop-back mode.	0x0
2	RW	OUT1	Out1 Value 0: OUT1N pin is driven to a high level. 1: OUT1N pin is driven to a low level. NOTE: This bit is only functional in loop-back mode.	0x0
1	RW	RTS	Out1 Value 0: RTSN pin is driven to a high level. 1: RTSN pin is driven to a low level.	0x0
1	RW	DTR	Reserved 0: DTRN pin is driven to a high level. 1: DTRN pin is driven to a low level.	0x0

LSR: Line Status Register (offset: 0x001c)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7	RC	ERINFIFO	The FIFO contains data which has a parity or framing error. This bit is set when the FIFO contains data that was received with a parity error, framing error, or break condition.	0x0
6	RC	TEMT	Transmitter Empty	0x1

			This bit is set when the transmitter shift register is empty. It clears as soon as data is written to the TBR register.	
5	RC	THRE	Transmitter Holding Register Empty This bit is set when the transmitter holding register is empty. It clears as soon as data is written to the TBR register.	0x1
4	RC	BI	Break Interrupt This bit is set if a break is received, that is when the RXD signal is at a low state for more than one character transmission time (from start bit to stop bit). Under this condition, a single 'zero' is received.	0x0
3	RC	FE	Framing Error This bit is set if a valid stop bit is not detected. If a framing error occurs, the receiver attempts to re-synchronize by sampling the start bit twice and then taking the data.	0x0
2	RC	PE	Parity Error This bit is set if the received parity is different from the expected value.	0x0
1	RC	OE	Overrun Error This bit is set when a receive overrun occurs. This happens if a character is received before the previous character has been read by firmware.	0x0
0	RC	DR	Data Ready This bit is set when a character is received, and has been transferred into the receiver buffer register. This bit is reset when all the characters are read from the receiver buffer register.	0x0

MSR: Modem Status Register (offset: 0x0020)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7	RC	DCD	Data Carrier Detect This bit is set when the DCDN (Data Carrier Detect) pin is at a low value.	0x0
6	RC	RI	Ring Indicator This bit is set when the RIN (Ring Indicator) pin is at a low value.	0x1
5	RC	DSR	Data Set Ready This bit is set when the DSRN (Data Set Ready) pin is at a low value.	0x0
4	RC	CTS	Clear To Send This bit is set when the CTSN (Clear To Send) pin is at a low value.	0x0
3	RC	DDCD	Delta Data Carrier Detect This bit is set when the DCDN (Data Carrier Detect) pin changes.	0x0
2	RC	TERI	Trailing Edge Ring Indicator This bit is set when the RIN (Ring Indicator) pin changes from a low to a high value.	0x0
1	RC	DDSR	Delta Data Set Ready This bit is set when the DSRN (Data Set Ready) pin changes.	0x0
0	RC	DCTS	Delta Clear To Send This bit is set when the CTSN (Clear To Send) pin changes.	0x0

SCRATCH: Scratch Register (offset: 0x0024)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RW	SCRATCH [7:0]	Scratch This register is defined as a scratch register in 16550 application. It has no hardware function, and is retained for compatibility only.	0x0

DL: Clock Divider Divisor Latch (offset: 0x0028)

<table>
<tr><th>Bits</th><th>Type</th><th>Name</th><th>Description</th><th>Initial value</th></tr>
<tr><td>31:16</td><td>-</td><td>-</td><td>Reserved</td><td>0x0</td></tr>
<tr><td>15:0</td><td>RW</td><td>DL[15:0]</td><td>Divisor Latch
This register is used in the clock divider to generate the baud clock. The baud rate (transfer rate in bits per second) is defined as:
baud rate = 40 MHz / (CLKDIV * 16).
NOTE: In standard 16550 implementation, this register is accessible as two 8-bit halves only. In this implementation, the DL register is accessible as a single 16-bit entity only.
NOTE: DL[15:0] should be >= 4
<table>
<tr><th>Src clock (MHz)</th><th>Req Baud rate</th><th>DL[15:0]</th><th>Err Rate (%)</th></tr>
<tr><td>40000000</td><td>57000</td><td>44</td><td>-0.32%</td></tr>
<tr><td></td><td>115200</td><td>22</td><td>-1.36%</td></tr>
<tr><td></td><td>230400</td><td>11</td><td>-1.36%</td></tr>
<tr><td></td><td>345600</td><td>7</td><td>3.34%</td></tr>
<tr><td></td><td>460800</td><td>5</td><td>8.51%</td></tr>
</table></td><td>0x1</td></tr>
</table>

DLLO: Clock Divider Divisor Latch Low (offset: 0x002c)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RW	DLLO[7:0]	This register is the equivalent to the lower 8 bits of the DL register. It is provided for 16550 compatibility. NOTE: In standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.	0x1

DLHI: Clock Divider Divisor Latch High (offset: 0x0030)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RW	DLHI[7:0]	This register is the equivalent to the upper 8 bits of the DL register. It is provided for 16550 compatibility. NOTE: In standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.	0x0

3.9 UART Lite

3.9.1 Features

- 2-pin UART
- 16550-compatible register set, except for divisor latch register
- 5-8 data bits
- 1-2 stop bits (1 or 2 stop bits are supported with 5 data bits)
- Even, odd, stick, or no parity
- All standard baud rates up to 345600 b/s
- 16-byte receive buffer
- 16-byte transmit buffer
- Receive buffer threshold interrupt
- Transmit buffer threshold interrupt
- False start bit detection in asynchronous mode
- Internal diagnostic capabilities
- Break simulation
- Loopback control for communications link fault isolation

3.9.2 Block Diagram

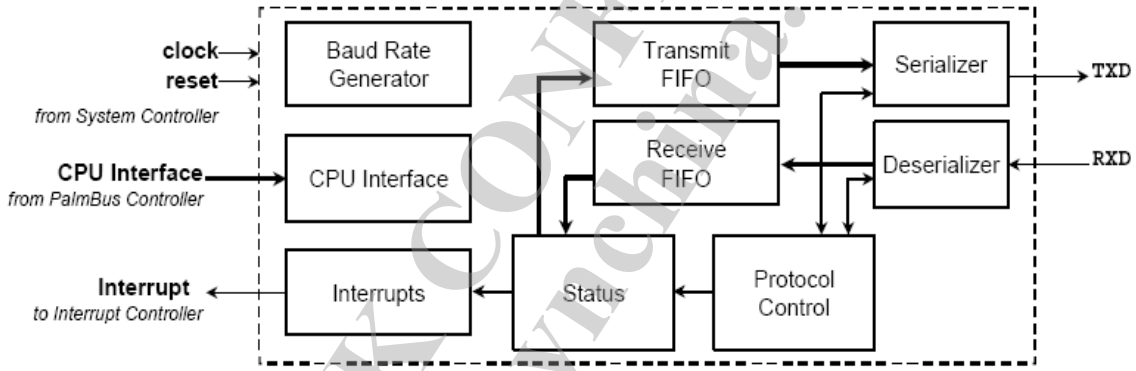


Figure 3-7 UART Lite Block Diagram

3.9.3 Register Description (base: 0x1000_0c00)

RBR: Receive Buffer Register (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RO	RXD[7:0]	Receive Buffer Data Data is transferred to this register from the receive shift register after a full character is received. If the contents of this register have not been read before another character is received, the OE bit in the LSR register is set, indicating a receive buffer overrun.	0x0

TBR: Transmit Buffer Register (offset: 0x0004)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	WO	TXD[7:0]	Transmit Buffer Data When a character is written to this register, it is stored in the transmitter holding register. If the transmitter register is empty, the character is moved to the transmitter register, starting transmission.	0x0

IER : Interrupt Enable Register (offset: 0x0008)

Bits	Type	Name	Description	Initial value
31:3	-	-	Reserved	0x0
2	RW	ELSI	Enable Receiver Line Status Interrupt 0: Disable line status (OE, PE, FE, and BI) interrupts. 1: Enable line status (OE, PE, FE, and BI) interrupts.	0x0
1	RW	ETBEI	Enable Transmitter Buffer Line Status Interrupt 0: Disable transmit buffer empty (THRE) interrupt. 1: Enable transmit buffer empty (THRE) interrupt.	0x0
0	RW	ERBFI	Enable Receiver Buffer Empty Interrupt 0: Disable data ready (DR) or character time-out interrupt. 1: Enable data ready (DR) or character time-out interrupt.	0x0

IIR: Interrupt Identification Register (offset: 0x000c)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:6	RO	FIFOENA [1:0]	FIFO Enable These bits reflect the FIFO enable bit setting in the FIFO control register. When the FIFO enable bit is set, both of these bits are set high to a value of '11'. When the FIFO enable bit is cleared, both of these bits are set low to a value of '00'.	0x0
5:4	-	-	Reserved	0x0
3:1	RO	INTID[2:0]	Interrupt Identifier These bits provide a snapshot of the interrupt type, and may be used as the offset into an interrupt vector table. The interrupt encoding is given below. ID / Priority / Type / Source 7 / Undefined 6 / Undefined 5 / Undefined 4 / Undefined 3 / 1 / Receiver Line Status / OE,PE,FE,BI 2 / 2 / Receiver Buffer Full / DR 1 / 3 / Transmit buffer Empty / THRE 0 / 4 / Modem Status / DCTD,DDSR, RI, DCD If more than one category of interrupt is asserted, only the highest priority ID is given. The line and modem status interrupts are cleared by reading the corresponding status register (LSR, MSR). The receive buffer full interrupt is cleared when all of the data is read from the receiver buffer. The transmitter buffer empty is cleared when data is written to the TBR register. See also "Interrupt Priorities".	0x0
0	RO	INTPEND	Interrupt Pending 0: An interrupt bit is set and is not masked. 1: No interrupts are pending.	RS

FCR: FIFO Control Register (offset: 0x0010)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:6	RW	RXTRIG [1:0]	Receiver Trigger Level The data ready interrupt (DR) is asserted when the receiver buffer depth is equal to the number of characters programmed in the	0x0

			trigger register. The trigger level encoding is as follows: RXTRIG / Trigger Level: 0 → 1; 1 → 4; 2 → 8; 3 → 14 NOTE: This register is not used if the receive FIFO is disabled.	
5:4	RW	TXTRIG [1:0]	Transmitter Trigger Level The THRE interrupt is asserted if the transmitter buffer depth is less than or equal to the number of characters programmed in the trigger register. The trigger level encoding is as follows: TXTRIG / Trigger Level: 0 → 1; 1 → 4; 2 → 8; 3 → 12	0x0
3	RW	DMAMODE	DMA Transfer Enable This bit is writeable and readable, but has no other hardware function.	0x0
2	RW	TXRST	Transmitter Reset Writing a '1' to this bit clears the transmit FIFO and resets the transmitter status. The shift register is not cleared.	0x0
1	RW	RXRST	Receiver Reset Writing a '1' to this bit clears the receive FIFO and resets the receiver status. The shift register is not cleared.	0x0
0	RW	FIFOENA	0: The transmit and receive FIFOs have the effective depth of one character. 1: The transmit and receive FIFOs are enabled. NOTE: The FIFO status and data are automatically cleared when this bit is changed.	0x0

LCR: Line Control Register (offset: 0x0014)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7	RW	DLAB	Divisor Latch Access Bit This bit has no functionality and is retained for compatibility only	0x0
6	RW	SETBRK	Set Break Condition 0: Normal functionality. 1: Force the TXD pin to '0'. The transmitter otherwise operates normally.	0x0
5	RW	FORCEPAR	Force Parity Bit 0: Normal functionality. 1: If even parity is selected, the (transmitted and checked) parity is forced to '0'; if odd parity is selected, the (transmitted and checked) parity if forced to '1'.	0x0
4	RW	EPS	Select Even Parity 0: Odd parity selected (checksum, including parity is '1'). 1: Even parity selected (checksum, including parity is '0'). NOTE: This bit is ignored if the PEN bit is '0'.	0x0
3	RW	PEN	Parity Enable 0: Parity is not transmitted or checked. 1: Parity is generated (transmit), and checked (receive).	0x0
2	RW	STB	Stop Bit Select 0: 1 stop bit is transmitted and received.	0x0

			1: 1.5 stop bits are transmitted and received if WLS is '0'; 2 stop bits are transmitted and received if WLS is '1', '2', or '3'.	
1:0:	RW	WLS[1:0]	Word Length Select 0: Each character is 5 bits in length. 1: Each character is 6 bits in length. 2: Each character is 7 bits in length. 3: Each character is 8 bits in length.	0x0

MCR: Modem Control Register (offset: 0x0018)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	0x0
4	RW	LOOP	Loopback Mode Enable 0: Normal operation. 1: The UART is put into loop-back mode, used for self-test: The TXD pin is driven high; the TXD signal are connected to RXD internally.	0x0
3:0	-	-	Reserved	0x0

LSR: Line Status Register (offset: 0x001c)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7	RC	ERINFIFO	The FIFO contains data which had a parity or framing error. This bit is set when the FIFO contains data that was received with a parity error, framing error or break condition.	0x0
6	RC	TEMT	Transmitter Empty This bit is set when the transmitter shift register is empty, it clears as soon as data is written to the TBR register.	0x1
5	RC	THRE	Transmitter Holding Register Empty This bit is set when the transmitter holding register is empty, it clears as soon as data is written to the TBR register.	0x1
4	RC	BI	Break Interrupt This bit is set if a break is received, that is when the RXD signal is at a low state for more than one character transmission time (from start bit to stop bit). Under this condition, a single '0' is received.	0x0
3	RC	FE	Framing Error This bit is set if a valid stop bit is not detected. If a framing error occurs, the receiver attempts to re-synchronize by sampling the start bit twice and then takes the data.	0x0
2	RC	PE	Parity error This bit is set if the received parity is different from the expected value.	0x0
1	RC	OE	Overrun Error This bit is set when a receive overrun occurs. This happens if a character is received before the previous character has been read by firmware.	0x0
0	RC	DR	Data Ready This bit is set when a character is received and has been transferred to the receiver buffer register. This bit is reset when all the characters are read from the receiver buffer register.	RS

DL: Clock Divider Divisor Latch (offset: 0x0028)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:0	RW	DL[15:0]	Divisor Latch	0x1

			This register is used in the clock divider to generate the baud clock. The baud rate (transfer rate in bits per second) is defined as: Baud rate = system clock frequency / (CLKDIV * 16). NOTE: In standard 16550 implementation, this register is accessible as two 8-bit halves only. In this implementation, the DL register is accessible as a single 16-bit entity only. NOTE: DL[15:0] should be >= 4 Srcclockm (MHz) Req Baud rate DL[15:0] Err Rate (%) 40000000 57000 44 -0.32% 115200 22 -1.36% 230400 11 -1.36% 345600 7 3.34% 460800 5 8.51%	

DLLO: Clock Divider Divisor Latch Low (offset: 0x002c)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RW	DLLO[7:0]	This register is equivalent to the lower 8 bits of the DL register. It is provided for 16550 compatibility. NOTE: In a standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.This register is the equivalent to the lower 8 bits of the DL	0x1

DLHI: Clock Divider Divisor Latch High (offset: 0x0030)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RW	DLHI[7:0]	This register is equivalent to the upper 8 bits of the DL register. It is provided for 16550 compatibility. NOTE: In a standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.	0x0

IFCTL：Interface Control (offset: 0x0034)

Bits	Type	Name	Description	Initial value
31:1	-	-	Reserved	0x0
0	RW	IFCTL	Open Collector Mode Control This register controls whether the UART Lite TXD output functions in open collector mode or is always driven. When set to '0', the output is always driven with the value of the transmit data signal. When set to a '1', the TXD output functions in open collector mode, where the TXD output is either driven low (when the transmit data output is active low) or tri-stated (when the transmit data output is active high.	0x0

3.10 Programmable I/O

3.10.1 Features

- Supports 28 programmable I/Os.
- Parameterized numbers of independent inputs, outputs, and inputs.
- Independent polarity controls for each pin.
- Independently masked edge detect interrupt on any input transition.
- Programmable I/O pins are shared pin with JTAG, UART-Lite, UART, SPI, PCM, I2C, EPHY_LED.

3.10.2 Block Diagram

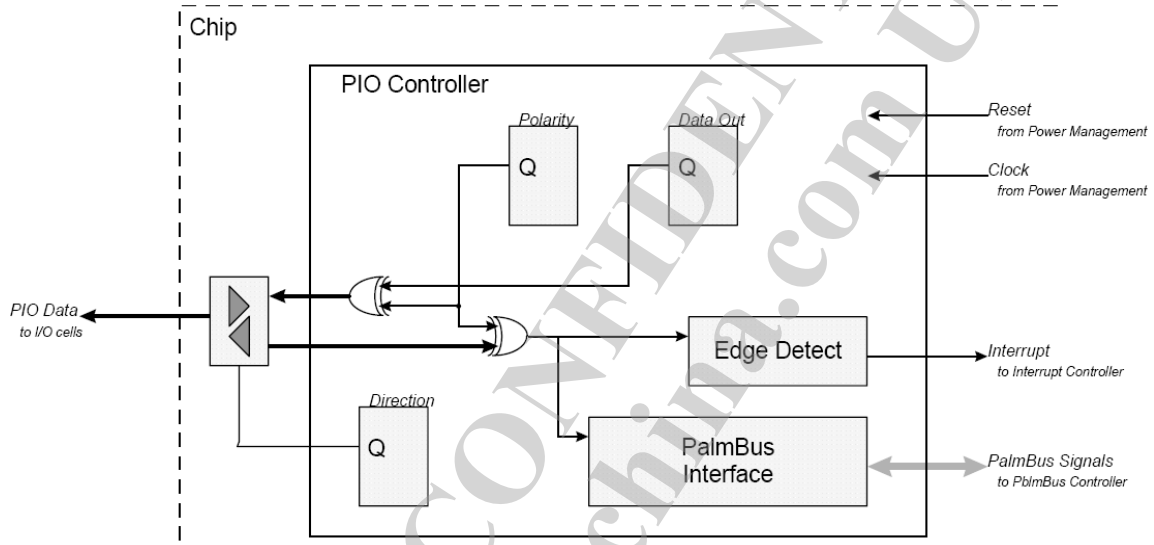


Figure 3-8 Program I/O Block Diagram

3.10.3 Register Description (base: 0x1000_0600)

GPIO21_00_INT: Programmed I/O Interrupt Status (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31:22	-	-	Reserved	0x0
21:0	RC	PIOINT[21:0]	A PIOINT bit is set when its corresponding PIO pin changes value and the edge for that pin is enabled via the PIORMSK or PIOFMSK register. A pin must be set as an input in the PIODIR register to generate an interrupt. All bits are cleared by writing '1' to either this register or the PIOEDGE register. NOTE: Changes to the PIO pins can only be detected when the clock is running.	0x0

GPIO21_00_EDGE: Programmed I/O Edge Status (offset: 0x0004)

Bits	Type	Name	Description	Initial value
31:22	-	-	Reserved	0x0
21:0	RC	PIOEDGE[21:0]	The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMSK or PIOFMSK register. If the interrupt is enabled, upon getting an interrupt condition (the corresponding PIOINT bit is set), the PIOEDGE bit is '1' if a rising edge triggered the interrupt, or '0' if a falling edge triggered the interrupt. If the interrupt is masked (disabled), the PIOEDGE bit is set on either a rising or falling edge and remain set until cleared by firmware. Bits corresponding to pins that are not set as inputs will never be set. All bits are	RS

			cleared by writing '1' to either this register or the PIOINT register. NOTE: Changes to the PIO pins can only be detected when the clock is running.	

GPIO21_00_RENA: Programmed I/O Rising Edge Interrupt Enable (offset: 0x0008)

Bits	Type	Name	Description	Initial value
31:22	-	-	Reserved	0x0
21:0	RW	PIORENA[21:0]	Rising Edge Mask for Individual Programmed I/O Pins The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '0' to a '1', i.e. a rising edge. A '1' allows the interrupt to be set; a '0' does not allow the interrupt and it is not set. NOTE: Edge detection is done after the polarity is adjusted according to the PIOPOL register.	0x0

GPIO21_00_FENA: Programmed I/O Falling Edge Interrupt Enable (offset: 0x000c)

Bits	Type	Name	Description	Initial value
31:22	-	-	Reserved	0x0
21:0	RW	PIOFMASK [21:0]	Falling Edge Mask for Individual Programmed I/O Pins The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '1' to a '0', i.e. a falling edge. A '1' allows the interrupt to be set; a '0' does not allow the interrupt so that it is not set. NOTE: Edge detection is done after the polarity is adjusted according to the PIOPOL register.	0x0

GPIO21_00_DATA: Programmed I/O Data (offset: 0x0020)

Bits	Type	Name	Description	Initial value
31:22	-	-	Reserved	0x0
21:0	RW	PIODATA[21:0]	Data Pins for Programmed I/O These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins. NOTE: 1. The value of any bit in this register is inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes. 2. The values read from the PIO pins are not synchronized; the user should be sure that the data does not change when this register is read, and should also be aware that the bits which are not static at that time may be inaccurate.	RS

GPIO21_00_DIR: Programmed I/O Direction (offset: 0x0024)

Bits	Type	Name	Description	Initial value
31:22	-	-	Reserved	0x0
21:0	RW	PIODIR[21:0]	Program I/O Pin Direction These bits are used for selecting the data direction of the PIO pins. To configure any pin as an output, the corresponding bit should be set to '1'; to configure any pin as an input, the corresponding bit should be set to '0'. The value driven onto the PIO pins is controlled by the PIOPOL and PIODATA registers.	0x0

GPIO21_00_POL: Programmed I/O Pin Polarity (offset: 0x0028)

Bits	Type	Name	Description	Initial value
31:22	-	-	Reserved	0x0
21:0	RW	PIOPOL[21:0]	Program I/O Pin Polarity These bits are used for controlling the polarity of the data driven on or read from the PIO pins. To invert the polarity of the data at any PIO pin, the corresponding bit should be set to '1'; a value of '0' does not modify the pin data. NOTE: The polarity controls affect both input and output modes.	0x0

GPIO21_00_SET: Set PIO Data Bit (offset: 0x002c)

Bits	Type	Name	Description	Initial value
31:22	-	-	Reserved	0x0
21:0	RC	PIOSET[21:0]	These bits are used for setting bits in the PIODATA output register. Writing a '1' sets the corresponding bit in the PIODATA register. Writing a '0' has no effect.	0x0

GPIO21_00_RESET: Clear PIO Data bit (offset: 0x0030)

Bits	Type	Name	Description	Initial value
31:22	-	-	Reserved	0x0
21:0	RC	PIORESET[21:0]	These bits are used for clearing bits in the PIODATA output register. 0: No effect. 1: Clears the corresponding bit in the PIODATA register.	0x0

GPIO21_00_TOG: Toggle PIO Data Bit (offset: 0x0034)

Bits	Type	Name	Description	Initial value
31:22	-	-	Reserved	0x0
21:0	RC	PIOTOG[21:0]	These bits are used for toggling bits in the PIODATA output register. 0: No effect. 1: Inverts the corresponding bit in the PIODATA register.	0x0

GPIO27_22_INT: Program I/O Interrupt Status (offset: 0x0060)

Bits	Type	Name	Description	Initial value
5:0	RC	PIOINT[5:0]	A PIOINT bit is set when its corresponding PIO pin changes value and the edge for that pin are enabled via the PIORMSK or PIOFMSK register. A pin must be set as an input in the PIODIR register to generate an interrupt. All bits are cleared by writing '1' to either this register or the PIOEDGE register. NOTE: Changes to the PIO pins can only be detected when the clock is running.	0x0

GPIO27_22_EDGE: Program I/O Edge Status (offset: 0x0064)

Bits	Type	Name	Description	Initial value
5:0	RC	PIOEDGE[5:0]	The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMSK or PIOFMSK register. If the interrupt is enabled, upon getting an interrupt condition (the corresponding PIOINT bit is set), the PIOEDGE bit is '1' if a rising edge triggered the interrupt, or '0' if a falling edge triggered the interrupt. If the interrupt is masked (disabled), the PIOEDGE bit is set on either a rising or falling	RS

			edge and remains set until cleared by firmware. Bits corresponding to pins that are not set as inputs are never set. All bits are cleared by writing '1' to either this register or the PIOINT register. NOTE: Changes to the PIO pins can only be detected when the clock is running.	

GPIO27_22_RENA: Program I/O Rising Edge Interrupt Enable (offset: 0x0068)

Bits	Type	Name	Description	Initial value
5:0	RW	PIORENA[5:0]	Rising Edge Mask for Individual Programmed I/O Pins The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '0' to a '1', i.e. a rising edge. A '1' allows the interrupt to be set; a '0' does not allow the interrupt so that it will not be set. NOTE: Edge detection is done after polarity is adjusted according to the PIOPOL register.	0x0

GPIO27_22_FENA: Program I/O Falling Edge Interrupt Enable (offset: 0x006c)

Bits	Type	Name	Description	Initial value
5:0	RW	PIORENA[5:0]	Falling Edge Mask for Individual Programmed I/O Pins The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '1' to a '0', i.e. a falling edge. A '1' allows the interrupt to be set; a '0' does not allow the interrupt so that it is not be set. NOTE: Edge detection is done after polarity is adjusted according to the PIOPOL register.	0x0

GPIO27_22_DATA: Program I/O Data (offset: 0x0070)

Bits	Type	Name	Description	Initial value
5:0	RW	PIODATA[5:0]	Program I/O Data Pin These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register is driven at the pin. A read of this register returns the value of the signals currently on the PIO pins. NOTE: 1. The value of any bit in this register is inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes. 2. The values read from the PIO pins are not synchronized; the user should be sure that the data does not change when this register is read, and should also be aware that the bits which are not static at that time may be inaccurate.	RS

GPIO27_22_DIR: Program I/O Direction (offset: 0x0074)

Bits	Type	Name	Description	Initial value
5:0	RW	PIODIR [5:0]	Program I/O Pin Direction These bits are used for selecting the data direction of the PIO pins. To configure any pin as an output, the corresponding bit should be set to '1'; to configure any pin as an input, the corresponding bit should be set to '0'. The value driven onto the PIO pins is controlled by the PIOPOL and PIODATA registers.	0x0

GPIO27_22_POL: Program I/O Pin Polarity (offset: 0x0078)

Bits	Type	Name	Description	Initial value
5:0	RW	PIOPOL [5:0]	Program I/O Pin Polarity These bits are used for controlling the polarity of the data driven on or read from the PIO pins. To invert the polarity of the data at any PIO pin, the corresponding bit should be set to '1'; a value of '0' does not modify the pin data. NOTE: The polarity controls affect both input and output modes.	0x0

GPIO27_22_SET: Set PIO Data Bit (offset: 0x007c)

Bits	Type	Name	Description	Initial value
5:0	RC	PIOSET [5:0]	These bits are used for clearing bits in the PIODATA output register. Writing a '1' clears the corresponding bit in the PIODATA register. Writing a '0' has no effect.	0x0

GPIO27_22_RESET: Clear PIO Data Bit (offset: 0x0080)

Bits	Type	Name	Description	Initial value
5:0	RC	PIORESET [5:0]	These bits are used for setting bits in the PIODATA output register. Writing a '1' sets the corresponding bit in the PIODATA register. Writing a '0' has no effect.	0x0

GPIO27_22_TOG: Toggle PIO Data Bit (offset: 0x0084)

Bits	Type	Name	Description	Initial value
5:0	RC	PIOTOG [5:0]	These bits are used for toggling bits in the PIODATA output register. Writing a '1' inverts the corresponding bit in the PIODATA register. Writing a '0' has no effect.	RS

3.11 I²C Controller

3.11.1 Features

- Two I²C host controllers
- Programmable I²C bus clock rate
- Supports the synchronous inter-integrated circuits (I2C) serial protocol
- Bi-directional data transfer
- Programmable address width up to 8 bits
- Sequential byte read or write capability
- Device address and data address can be transmitted for device, page, and address selection
- Supports standard mode and fast mode.

3.11.2 Block Diagram

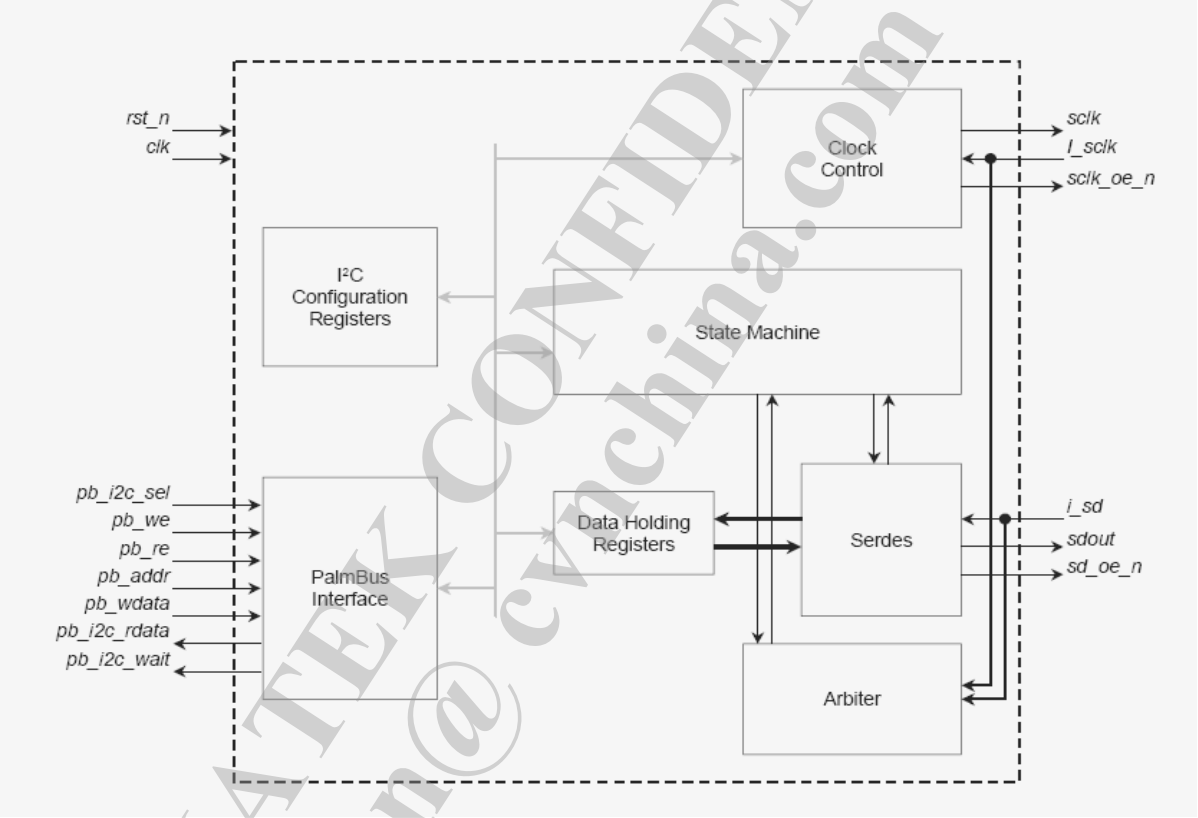


Figure 3-9 1 I²C Controller Block Diagram

3.11.3 Register Description (base: 0x1000_0900)

CONFIG: I²C Configuration Register (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:5	RW	ADDRLEN [2:0]	Address Length The value written to this register plus one indicates the number of address bits to be transferred from the I²C ADDR register. Set this field to '0' for a 1-bit address, '1' for a 2-bit address, etc.	0x0
4:2	RW	DEVADLEN [2:0]	Device Address Length The value written to this register plus one indicates the number of device address bits to be transferred from the DEVADDR register. This field should be set to '6' for compliance with I²C bus protocol.	0x0

1	RW	ADDRDIS	0: Normal transfers occur when the address is transmitted, followed by read or write data. 1: The controller reads or writes serial data without transferring the address.	0x0
0	RW	DEVADDIS	0: The device address is transmitted before the data address. 1: The controller does not transfer the device address. NOTE: 1. If this bit is set, the ADDRDIS bit is ignored, and an address is always transmitted. 2. Most I²C slave devices require a device address to be transmitted. This bit should typically be set to '0'.	0x0

CLKDIV: I²C Clock Divisor Register (offset: 0x0004)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:0	RW	CLKDIV[15:0]	Clock Divisor The value written to this register is used to generate the I²C bus SCLK signal by applying the following equation: SCLK frequency = 40 MHz / (2 x CLKDIV). NOTE: 1. Only values of 8 and above are valid. 2. Due to synchronization between the I²C internal clock and the system clock, the exact equation is actually SCLK frequency = pb_clk frequency / ((2 x CLKDIV) + 5). For most systems, CLKDIV is usually programmed to very larger numbers since the system clock frequency should be orders of magnitude faster than the I²C bus clock. This makes the synchronization errors insignificant and the simpler equation given above approximates the exact equation.	0x0

DEVADDR: I²C Device Address Register (offset: 0x0008)

Bits	Type	Name	Description	Initial value
31:7	-	-	Reserved	0x0
6:0	RW	DEVADDR[6:0]	I²C Device Address This value is transmitted as the device address if the DEVADDIS bit in the CONFIG register is not set to '1'.	0x0

ADDR: I²C Address Register (offset: 0x000c)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RW	ADDR[7:0]	I²C Address These bits store the 8-bits of the address to be sent to the external I²C slave devices when the ADDRDIS bit is '0'.	0x0

DATAOUT: I²C Data Out Register (offset: 0x0010)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RW	DATAOUT [7:0]	I²C Data Out These bits store the 8-bits of data to be written to the external I²C slave devices during a write transfer.	0x0

DATAIN: I²C Data In Register (offset: 0x0014)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RO	DATAIN[7:0]	I²C Data In These bits store the 8-bits of data received from the external I²C slave devices during a read transaction. The DATARDY bit in the STATUS register is set to '1' when data is valid in this register.	0x0

STATUS: I²C Status Register (offset: 0x0018)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	0x0
4	RO	STARTERR	Start Overflow Error This bit is set when the STARTXFR register is written and a transfer is in progress. When this occurs, the write to the STARTXFR register is ignored. This bit is automatically cleared if firmware writes to the STARTXFR register when the BUSY bit is cleared.	0x0
3	RO	ACKERR	I²C Acknowledge Error Detect This bit is set when the host controller does not receive a proper acknowledge from the I²C slave device after the transmission of a device address, address, or data out. This bit is automatically cleared when firmware writes to the STARTXFR register.	0x0
2	RO	DATARDY	I²C Data Ready for Read This bit indicates that the receive buffer contains valid data. It is set when data is received from an I²C slave device and is transferred from the interface shift register to the DATAIN register. This bit is automatically cleared when firmware reads the DATAIN register.	0x0
1	RO	SDOEMPTY	I²C serial Data Out Register Empty This bit indicates that the transmit data buffer is empty. It is cleared when the DATAOUT register is written to by software, and set to '1' when transmit data is transferred from the DATAOUT register to the interface shift register. Firmware may write to the DATAOUT register when this bit is '1'.	0x1
0	RO	BUSY	I²C State Machine Busy This bit is '1' when the I²C interface is active, and '0' when it is idle. Firmware may initiate an I²C transfer when this bit is '0', and should not modify any I²C host controller registers while it is '1'.	0x0

STARTXFR: I²C Transfer Start Register (offset: 0x001c)

Bits	Type	Name	Description	Initial value
31:3	-	-	Reserved	0x0
2	RW	NO_STOP	Initiate transfer without STOP. It is applied to generate the SR (Start Repeat) transaction.	0x0

1	RW	NODATA	Initiate Transfer Without Transferring Data When this register is written with this bit set, an address-only transaction is initiated. If DEVADDIS is '0', the device address, direction, address, and stop condition are transmitted to the I^2C slave device. If DEVADDIS is '1', the address and stop condition are transmitted to the I^2C slave device. This bit should be written with a '0' for normal I^2C bus accesses. NOTE: ADDRDIS is ignored if this bit is set for a transaction.	0x0
0	RW	RWDIR	Read/Write Direction When this register is written with this bit set, a read transaction is initiated; when written with this bit reset, a write transaction is initiated. NOTE: This bit is shifted out to the I^2C slave device after the device address; if DEVADDIS is '1', this bit is not shifted out to the device.	0x0

BYTECNT: I^2C Byte Counter Register (offset: 0x0020)

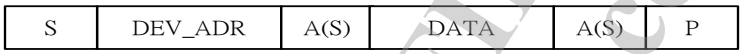
Bits	Type	Name	Description	Initial value
31:6	-	-	Reserved	0x0
5:0	RW	BYTCNT[5:0]	Byte Count Used for sequential reads/writes. The value written to this register plus one indicates the number of data bytes to be written to or read from the external I^2C slave device. If its value is non-zero, multiple sequential read or write cycles are issued with a single address (and/or device address).	0x0

3.11.4 Programming Description

Write Operation: (Single)

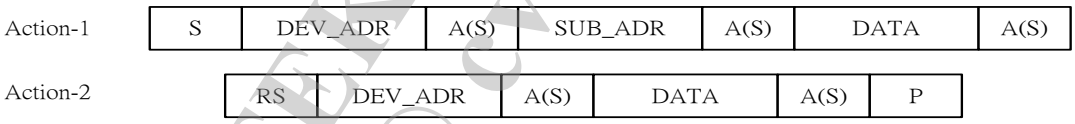
PS: the bit-width of DEV_ADR is defined in REG(CONFIG) bit[7:5]
the bit-width of SUB_ADR is defined in REG(CONFIG) bit[4:2]

PS: As REG(CONFIG) bit[1]=1'b1, the SUB_ADR field will be absent. (the waveform will be shown as below.)

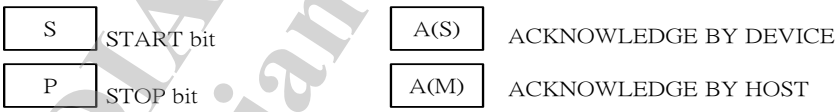


PS: As REG(CONFIG) bit[0]=1'b1, the DEV_ADR field will be absent. (the waveform will be shown as below.)

Sequence Write Operation:



Action-1: SET REG(STARTXFR) bit[2]=1'b1, the "STOP" <P> field will absent.
Action-2: SET REG(STARTXFR) bit[2]=1'b0, the "STOP" <P> field will appear.



Initialization:

1. Set the clock frequency of I^2C by configuring the REG(CLKDIV).
2. Set the bit width of DEV_ADDR & SUB_ADDR by configuring REG(CONFIG).

Read/Write Operation:

3. Write the DEV_ADDR and SUB_ADDR to REG(DEVADDR) & REG(ADDR).
4. Write the DATAout (REG(DATAOUT)) for write operation.
5. Write the operation cfg by REG(STARTXFR) to kick off the command.
6. Read the BUSY status by REG(STATUS) to monitor if the operation is done.
7. Read back the REG(DATAIN) for read operation.

Multiple Data Transfer: (write operation.)

E.g. we want to write (n+1) beats data by I2C

Burst Write Operation:
1) Write the DEV_ADDR and SUB_ADDR to REG(DEVADDR) & REG(ADDR)
2) Write (N) to REG(BYTECNT).
3) Write the REG(DATAOUT) for write operation.
4) Write the operation cfg by REG(STARTXFR) to kick off the command.
5) Read the SDOEMPTY bit by REG(STATUS) to monitor if the data is sent.
6) quit as all data is written, otherwise put the new data to the REG(DATAOUT) for write operation.
7) continue step 4.

Multiple Data Transfer: (read operation.)

E.g. we want to read (n+1) beats data by I2C

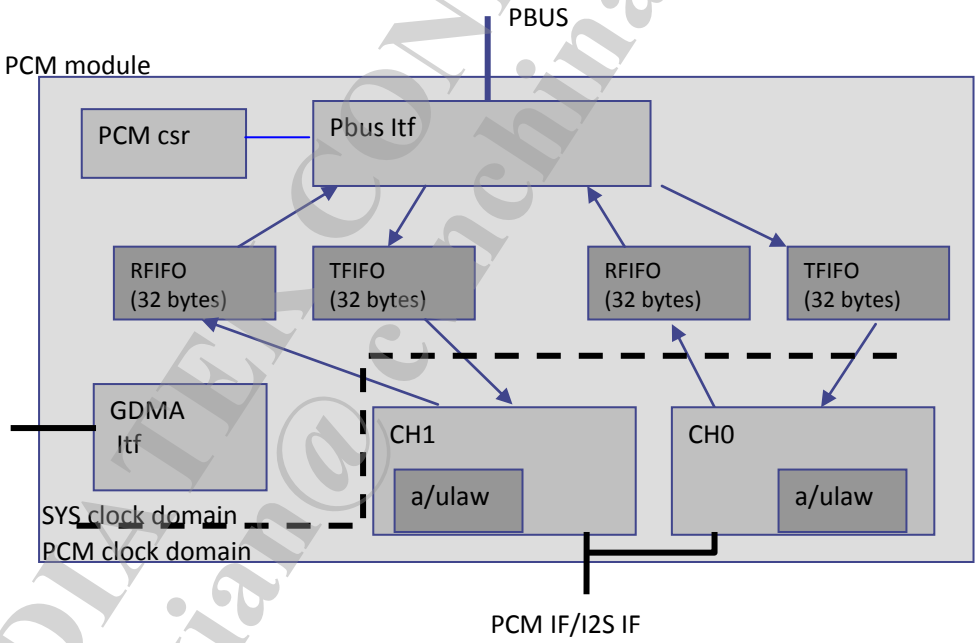
Burst Read Operation:
1) Write the DEV_ADDR and SUB_ADDR to REG(DEVADDR) & REG(ADDR)
2) Write (N) to REG(BYTECNT).
3) Write the operation cfg by REG(STARTXFR) to kick off the command.
4) Read the DATARDY bit by REG(STATUS) to monitor if the data is obtained.
5) Read REG(DATAIN) and continue step-4 until all bytes are read.

3.12 PCM Controller

3.12.1 Features

- The PCM module provides a PBUS interface for register configuration and data transfer.
- Two clock sources are reserved for the PCM circuit (from the internal clock generator, int_pcm_clk, and from the external clock source, ext_pcm_clk).
- The PCM module can drive a clock out (with fractional-N clock divider) to an external codec.
- 2 PCM channels are available. 4~128 slots are configurable.
- Each channel supports a-law(8-bits)/u-law(8-bits)/raw-PCM(16-bits) transfer.
- Hardware conversion of a-law< = >raw-16 and u-law < = > raw-16 are implemented in design.
- Supports long(8 cycle)/short(1 cycles)/configurable (interval & start point are configurable) FSYNC.
- All signals are driven by rising edge and latched by falling edge.
- The last bit of DTX is tri-stated on falling edge.
- The beginning of a slot is configurable by 10-bit registers for each channel.
- 32 bytes FIFO are available for each channel
- The PCM interface can emulate I^2S interface (16-bits data-width only).
- MSB/LSB order is configurable.
- Supports both a-law/u-law (8-bit) ➔ linear PCM (16-bit) and linear PCM (16-bit) ➔ a-law/u-law (8-bit).

3.12.2 Block Diagram



Two clocks domains are partitioned in this design. PCM converters (ulaw< = >raw-16bit and alaw< = >raw-16bit) are implemented in PCM module. The threshold of FIFO is configurable. When the threshold is reached, PCM (a) triggers the DMA interface to notify an external DMA engine to transfer data, and then (b) triggers the interrupts to the host.

The interrupt sources include:

- The threshold is reached.
- FIFO is under-run or overrun.
- A fault is detected at the DMA interface.

The A-law and u-law converter is implemented based on the ITU-G.711 A-law and u-law table. In this design, both a-law/u-law (8-bit) ➔ linear PCM (16-bit) and linear PCM (16-bit) ➔ a-law/u-law (8-bit) is supported.

The data-flow from codec to PCM-controller (Rx-flow) is shown as below:

- PCM-controller latches the data from DRX at the indicated time slot and then writes it to FIFO. If FIFO is full, the data is lost.
- When the RX-FIFO reaches the threshold, two actions may be taken.
- When DMA_ENA=1, DMA_REQ is asserted to request a burst transfer. It also re-checks the FIFO threshold after DMA_END is asserted by GDMA (GDMA should be configured before the channel is enabled).
- The interrupt source is asserted to notify HOST. HOST checks the RFIFO_AVAIL information and then gets back the data from FIFO.

The data-flow from PCM-controller to codec (Tx-flow) is shown as below:

- After GDMA is configured, software should be configured and the PCM channel should be enabled.
- The empty FIFO should behave as follows:
  - When DMA_ENA=1, DMA_REQ is triggered to request a burst transfer. It also re-checks the FIFO threshold after DMA_END is asserted by GDMA (a burst is completed.).
  - The interrupt source is asserted to notify HOST. HOST writes the data to the TX-FIFO. After that, HOST rechecks the TFIFO_EMPTY information and then writes more data if available.

NOTE: When DMA_ENA=1, the burst size of GDMA should less than the threshold value.

3.12.3 Register Description (base: 0x1000_2000)

GLB_CFG: GLB_CFG Register (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31	RW	PCM_EN	PCM Enable 0: Disable. All FSM and PCM module control registers are set to default values. 1: Enable	0x0
30	RW	DMA_EN	DMA Enable 0: Disable the DMA interface, transfers data with software. 1: Enable the DMA interface, transfers data with DMA.	0x0
29:23	-	-	Reserved	0x0
22:20	RW	RFF_THRES	RXFIFO Threshold When the threshold is reached, the host/DMA is notified to fill FIFO. (unit = word) It should be >2 and <6. When data in the FIFO is under the threshold, an interrupt and DMA are triggered.	0x4
19	-	-	Reserved	0x0
18:16	RW	TFF_THRES	TXFIFO Threshold When the threshold is reached, the host/DMA is notified to fill FIFO. (unit = word) It should be >2 and <6. When data in FIFO is over the threshold, interrupt & DMA are triggered.	0x4
15:10	-	-	Reserved	0x0
9	RW	CH1-TX_EN	Channel 1 Tx Enable	0x0
8	RW	CH0-TX_EN	Channel 0 Tx Enable	0x0
7:2	-	-	Reserved	0x0
1	RW	CH1-RX_EN	Channel 1 Rx Enable	0x0
0	RW	CH0-RX_EN	Channel 0 Rx Enable 0: Disable 1: Enable	0x0

PCM_CFG: PCM_CFG Register (offset: 0x0004)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	0x0

30	RW	CLKOUT_EN	PCM_CLK_OUT Enable 0: The PCM clock is provided from an external codec/OSC. 1: The PCM clock is provided from the internal divider. NOTE: Normally, the register should be asserted to '1', and it should be asserted after divider configuration and the divider clock are enabled.	0x0
29:28	-	-	Reserved	0x0
27	RW	EXT_FSYNC	External FSYNC 0: FSYNC is generated by an internal circuit. 1: FSYNC is provided externally.	0x0
26	RW	LONG_FSYNC	FSYNC Mode 0: Short FSYNC 1: Long FSYNC	0x0
25	RW	FSYNC_POL	FSYNC Polarity 0: FSYNC is low active. 1: FSYNC is high active.	0x1
24	RW	DTX_TRI	Tristate the DTX as fall edge as last bit. 0: Non-tristate the DTX. 1: Tristate the DTX.	0x1
23:3	-	-	Reserved	0x0
2:0	RW	SLOT_MODE	The number of slots in each PCM frame. 0: 4 slots, PCM clock out/in should be 256 KHz. 1: 8 slots, PCM clock out/in should be 512 KHz. 2: 16 slots, PCM clock out/in should be 1.024 MHz. 3: 32 slots, PCM clock out/in should be 2.048 MHz. 4: 64 slots, PCM clock out/in should be 4.096 MHz. 5: 128 slots, PCM clock out/in should be 8.192 MHz. Other: Reserved. NOTE: When using the external clock, the frequency clock should be equal to the PCM_clock out. Otherwise, the PCM_CLKin should be 8.192 MHz.	0x0

INT_STATUS: INT_STATUS Register (offset: 0x0008)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15	W1C	CH1T_DMA_FAULT	Notifies the detection of an error in CH1-TX's DMA signals. 1: Clear	0x0
14	W1C	CH1T_OVRUN	The FIFO of CH1-TX overrun. 1: Clear	0x0
13	W1C	CH1T_UNRUN	The FIFO of CH1-TX underrun. 1: Clear	0x0
12	W1C	CH1T_THRES	The FIFO of CH1-TX is lower than the defined threshold. 1: Clear	0x0
11	W1C	CH1R_DMA_FAULT	Notifies the detection of an error in the CH1-RX's DMA signals. 1: Clear	0x0
10	W1C	CH1R_OVRUN	The FIFO of CH1-RX overrun. 1: Clear	0x0
9	W1C	CH1R_UNRUN	The FIFO of CH1-RX underrun. 1: Clear	0x0
8	W1C	CH1R_THRES	The FIFO of CH1-RX is lower than the defined threshold. 1: Clear	0x0
7	W1C	CH0T_DMA_FAULT	Notifies the detection of an error in the CH0-TX's DMA signals. 1: Clear	0x0
6	W1C	CH0T_OVRUN	The FIFO of CH0-TX overrun.	0x0

			1: Clear	
5	W1C	CH0T_UNRUN	The FIFO of CH0-TX underrun. 1: Clear	0x0
4	W1C	CH0T_THRES	The FIFO of CH0-TX is lower than the defined threshold. 1: Clear	0x0
3	W1C	CH0R_DMA_FAULT	Notifies the detection of an error in the CH0-RX's DMA signals. 1: Clear	0x0
2	W1C	CH0R_OVRUN	The FIFO of CH0-RX overrun. 1: Clear	0x0
1	W1C	CH0R_UNRUN	The FIFO of CH0-RX underrun. 1: Clear	0x0
0	W1C	CH0R_THRES	The FIFO of CH0-RX is lower than the defined threshold. 1: Clear	0x0

INT_EN: INT_EN Register (offset: 0x000c)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15	RW	INT15_EN	Enables INT_STATUS[15].	0x0
14	RW	INT14_EN	Enables INT_STATUS[14].	0x0
13	RW	INT13_EN	Enables INT_STATUS[13].	0x0
12	RW	INT12_EN	Enables INT_STATUS[12].	0x0
11	RW	INT11_EN	Enables INT_STATUS[11].	0x0
10	RW	INT10_EN	Enables INT_STATUS[10].	0x0
9	RW	INT9_EN	Enables INT_STATUS[9].	0x0
8	RW	INT8_EN	Enables INT_STATUS[8].	0x0
7	RW	INT7_EN	Enables INT_STATUS[7].	0x0
6	RW	INT6_EN	Enables INT_STATUS[6].	0x0
5	RW	INT5_EN	Enables INT_STATUS[5].	0x0
4	RW	INT4_EN	Enables INT_STATUS[4].	0x0
3	RW	INT3_EN	Enables INT_STATUS[3].	0x0
2	RW	INT2_EN	Enables INT_STATUS[2].	0x0
1	RW	INT1_EN	Enables INT_STATUS[1].	0x0
0	RW	INT0_EN	Enables INT_STATUS[0].	0x0

FF_STATUS: FF_STATUS Register (offset: 0x0010)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:12	RO	CH1RFF_AVCNT	CH1- Available FIFO space can be read (unit=word).	0x0
11:8	RO	CH1TFF_EPCNT	CH1- Available FIFO space can be written (unit=word).	0x8
7:4	RO	CH0RFF_AVCNT	CH0- Available FIFO space can be read (unit=word).	0x0
3:0	RO	CH0TFF_EPCNT	CH0- Available FIFO space can be written (unit=word).	0x8

CH0_CFG: CH0_CFG Register (offset: 0x0020)

Bits	Type	Name	Description	Initial value
31	RW	LBK_EN	Loopback Enable 0: Normal mode 1: Loopback (Asyn-TXFIFO➔DTX➔DRX➔Asyn-RXFIFO)	0x0
30	RW	EXT_LBK_EN	External Loopback Enable 0: Normal mode 1: Enable external loopback. (Ext-Codec➔DRX➔DTX➔Ext-Codec)	0x0

29:27	RW	CMP_MODE	Compression Mode 000: Disable the HW converter, linear raw-data (16-bit). 010: Disable the HW converter, linear raw-data (8-bit), A-law or u-law (8-bit). 011: Reserved 100: Enable the HW converter, raw-data (16-bit) ➔ u-law mode (8-bit) (PCM bus is compressed format). 101: Enable the HW converter, u-law mode (8-bit) ➔ raw-data (16-bit) (PCM bus is raw, 16-bit format). 110: Enable the HW converter, raw-data (16-bit) ➔ A-law mode (8-bit) (PCM bus is compressed format). 111: Enable the HW converter, A-law mode (8-bit) ➔ raw data (16-bit) (PCM bus is raw, 16-bit format).	0x0
26:10	-	-	Reserved	0x0
9:0	RW	TS_START	Time Slot Starting Location	0x1

CH1_CFG: CH1_CFG Register (offset: 0x0024)

Bits	Type	Name	Description	Initial value
31	RW	LBK_EN	Loopback Enable 0: Normal mode 1: Loopback (Asyn-TXFIFO➔DTX➔DRX➔Asyn-RXFIFO)	0x0
30	RW	EXT_LBK_EN	External Loopback Enable 0: Normal mode 1: Enable external loopback. (Ext-Codec➔DRX➔DTX➔Ext-Codec)	0x0
29:27	RW	CMP_MODE	Compression Mode 000: Disable the HW converter, linear raw data (16-bit). 010: Disable the HW converter, linear raw data (8-bit), A-law or u-law (8-bit). 011: Reserved 100: Enable the HW converter, raw data (16-bit) ➔ u-law mode (8-bit) (PCM bus be in compressed format). 101: Enable the HW converter, u-law mode (8-bit) ➔ raw-data (16-bit) (PCM bus is raw, 16-bit format). 110: Enable the HW converter, raw-data (16-bit) ➔ A-law mode (8-bit) (PCM bus is compressed format). 111: Enable the HW converter, A-law mode (8-bit) ➔ raw-data (16-bit) (PCM bus is raw, 16-bit format).	0x0
26:10	-	-	Reserved	0x0
9:0	RW	TS_START	Time Slot Starting Location	0x1

FSYNC_CFG: FSYNC Configuration Register (offset: 0x0030)

Bits	Type	Name	Description	Initial value
31	RW	Cfg_fsync_en	Configurable FSYNC Enable	0x0
30	RW	Pos_sample	The controller samples data with 0: Negative edge of PCM clock. 1: Positive edge of PCM clock. NOTE: This configuration should be '0' if DTX_TRI=1.	0x0
29:22	-	-	Reserved	0x0
21:12	RW	Fsync_start	The Start Point of Configurable FSYNC	0x0
11:10	-	-	Reserved	0x0
9:0	RW	Fsync_intv	The Interval of Configurable FSYNC.	0x0

CH_CFG2: Extended Channel Configuration Register (offset: 0x0034)

Bits	Type	Name	Description	Initial value
31:20	-	-	-	-
19	RW	CH1_RXFF_CLR	CH1 RXFIFO Clear 0: Normal operation 1: Clear	0x0
18	RW	CH1_TXFF_CLR	CH1 TXFIFO Clear 0: Normal operation 1: Clear	0x0
17	-	-	Reserved	0x0
16	RW	CH1_LSB	CH1 Transmit in LSB Order Enable	0x0
15:4	-	-	Reserved	0x0
3	RW	CH0_RXFF_CLR	CH0 RXFIFO Enable 0: Normal operation 1: Clear	0x0
2	RW	CH0_TXFF_CLR	CH0 TXFIFO Enable 0: Normal operation 1: Clear	0x0
1	RW	-	Reserved	0x0
0	RW	CH0_LSB	CH0 Transmit in LSB Order Enable	0x0

RSV_REG16: RSV_REG16 Register (offset: 0x0038)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:0	RW	SPARE_REG	Spare register for future use	0x0

DIVCOMP_Cfg: Integer Part of the Divider Register (offset: 0x0050)

Bits	Type	Name	Description	Initial value
31	RW	CLK_EN	Enables the clock divider.	0x0
30:8	-	-	Reserved	0x0
7:0	RW	DIVCOMP	A parameter in an equation which determines FreqOut. See DIVINT.	0x0

DIVINT_Cfg: Integer Part of the Divider Register (offset: 0x0054)

Bits	Type	Name	Description	Initial value
31:10	-	-	Reserved	0x0
9:0	RW	DIVINT	A parameter in an equation which determines FreqOut. Formula: FreqOut = (1/2) * FreqIn * (1/(DIVINT+(DIVCOMP/(2^8))) FreqIn is always fixed to 40 MHz.	0x0

DIGDELAY_Cfg: Digital Delay Configuration Register (offset: 0x0060)

Bits	Type	Name	Description	Initial value
31	RW	TXD_CLR_GLT	TXD Glitch Detected Flag Clear 0: Normal operation 1: Clear	0x0
30	RW	CHEN_CLR_GLT	CHEN Glitch Detected Flag Clear 0: Normal operation 1: Clear	0x0
29:27	-	-	Reserved.	0x0
26	RO	TXD_GLT_ST	TXD Signal Glitch Detected Status It can be cleared by bit[31].	0x0
25:24	-	-	Reserved.	0x0

23	RO	CHEN1N_GLT_ST	CHEN-1 Signal Glitch Detected Status It can be cleared by bit[30] (negedge sample).	0x0
22	RO	CHEN0N_GLT_ST	CHEN-1 Signal Glitch Detected Status It can be cleared by bit[30] (negedge sample).	0x0
21:20	-	-	Reserved.	0x0
19	RO	CHEN1P_GLT_ST	CHEN-1 Signal Glitch Detected Status It can be cleared by bit[30] (posedge sample).	0x0
18	RO	CHEN0P_GLT_ST	CHEN-0 Signal Glitch Detected Status It can be cleared by bit[30] (posedge sample).	0x0
17	RO	CHEN1PD_GLT_ST	CHEN-1 Signal Glitch Detected Status It can be cleared by bit[30] (posedge sample, delay 1 cycle)	0x0
16	RO	CHEN0PD_GLT_ST	CHEN-1 Signal Glitch Detected Status It can be cleared by bit[30] (posedge sample, delay 1 cycle).	0x0
15	RW	TXD_DIGDLY_EN	Digital Delay Path 0: Disable 1: Enable	0x0
14:13	-	-	Reserved	0x0
12:8	RW	TXD_DLYVAL	Delay Count Value	0x2
7	RW	CHEN_DIGDLY_EN	Digital Delay Path Delay 0: Disable 1: Enable	0x0
6:5	-	-	Reserved	0x0
4:0	RW	CHEN_DLYVAL	Delay Count Value The error of delay = clk_period * (sync_delay + sync_delta + (dlycnt_cfg) + 1) e.g. sync_delay = 2, dlyval=2 final delay = clk_period * (2 + (-1/0/+1) + (2) + 1) = clk_period * (4/5/6) = clk_period * (4~6)	0x2

CH0_FIFO: CH0_FIFO Register (offset: 0x0080)

Bits	Type	Name	Description	Initial value
31:0	RW	CH0_FIFO	FIFO Access Point	0x0

CH1_FIFO: CH1_FIFO Register (offset: 0x0084)

Bits	Type	Name	Description	Initial value
31:0	RW	CH1_FIFO	FIFO Access Point	0x0

The PCM Initialization Flow:

1. Set PCM_CFG.
2. Set CH0/1_CFG.
3. Write PCM data to FIFO CH0/1_FIFO.
4. Set GLB_CFG to enable the PCM and channel.
5. Set the dividor clock.
6. Enable the clock.
7. Monitor FF_STATUS to receive/transmit other PCM data.

3.12.4 An Example of PCM Configuration

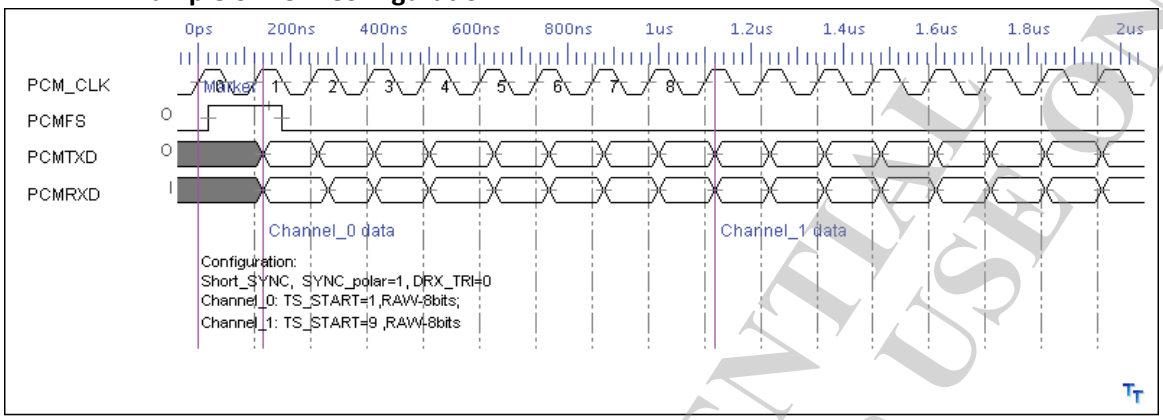


Figure 3-10 PCM Configuration Example 1

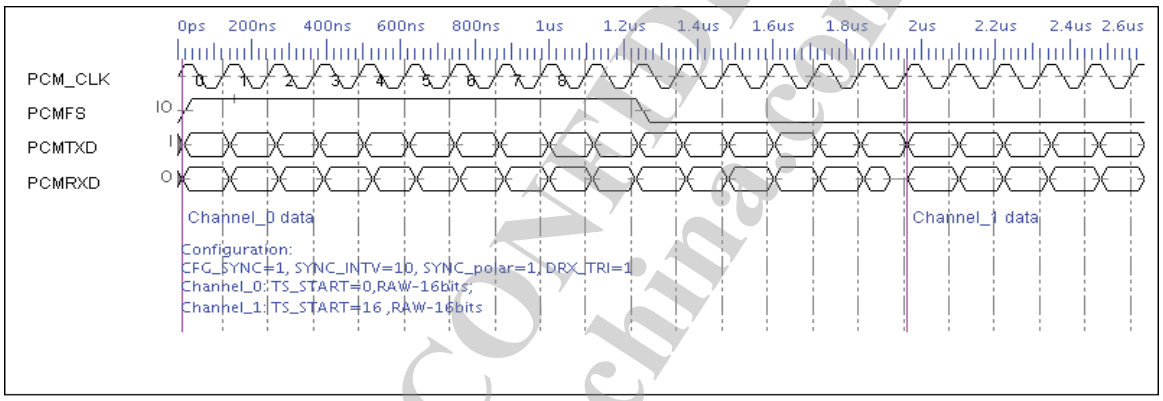


Figure 3-11 PCM Configuration Example 2

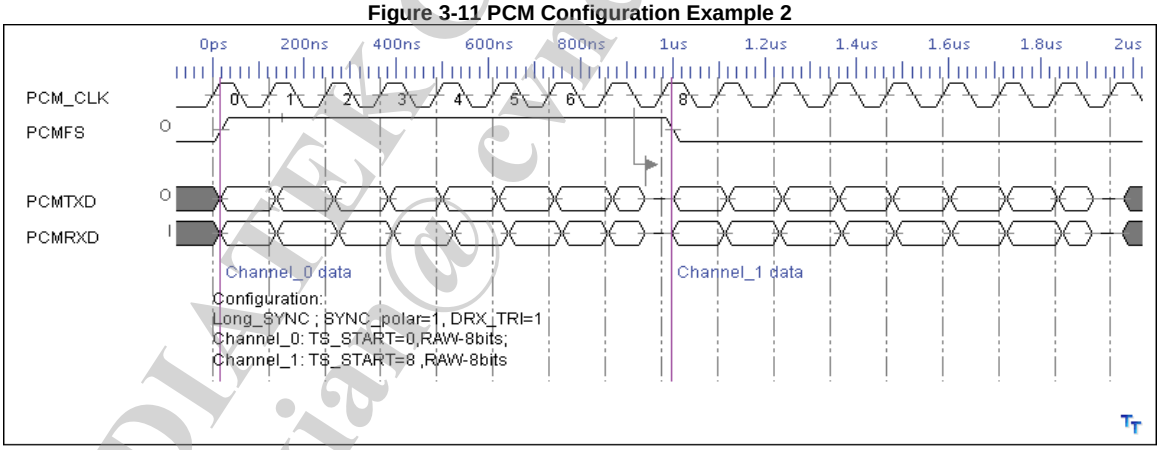


Figure 3-12 PCM Configuration Example 3

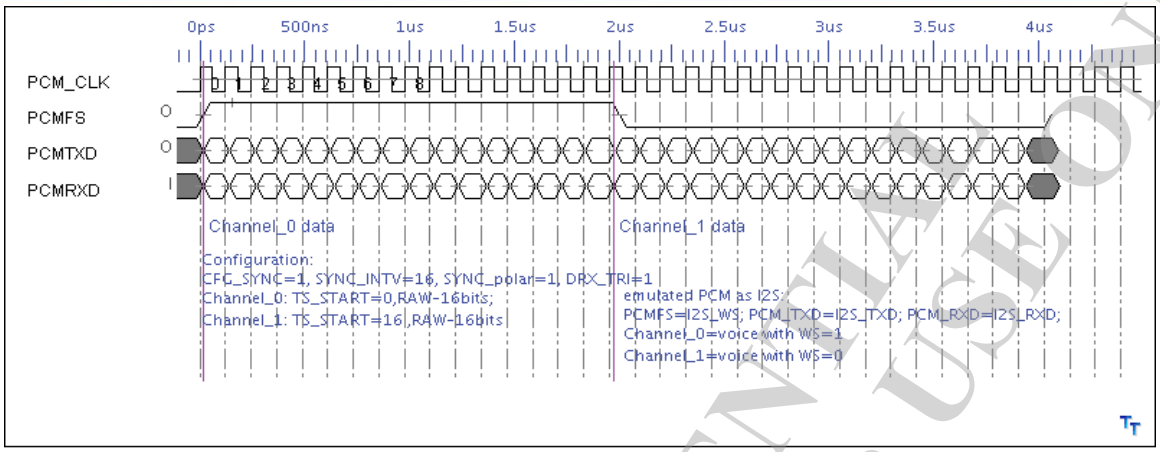


Figure 3-13 PCM Configuration Example 4

3.13 Generic DMA Controller

3.13.1 Features

- Supports 16 DMA channels.
- Supports 16 DMA requests.
- Programmable hardware channel priority
- Programmable DMA burst size (1,2,4,8,16 burst transfer)
- Supports 32-bit wide transactions.
- Big endian and little endian support
- Supports memory to memory, memory to peripheral, peripheral to memory, peripheral to peripheral transfers.
- Interrupts for each channel. They also can be masked, independently.
- Each channel transaction can be masked temporarily by the software, and released by the hardware automatically.

3.13.2 Block Diagram

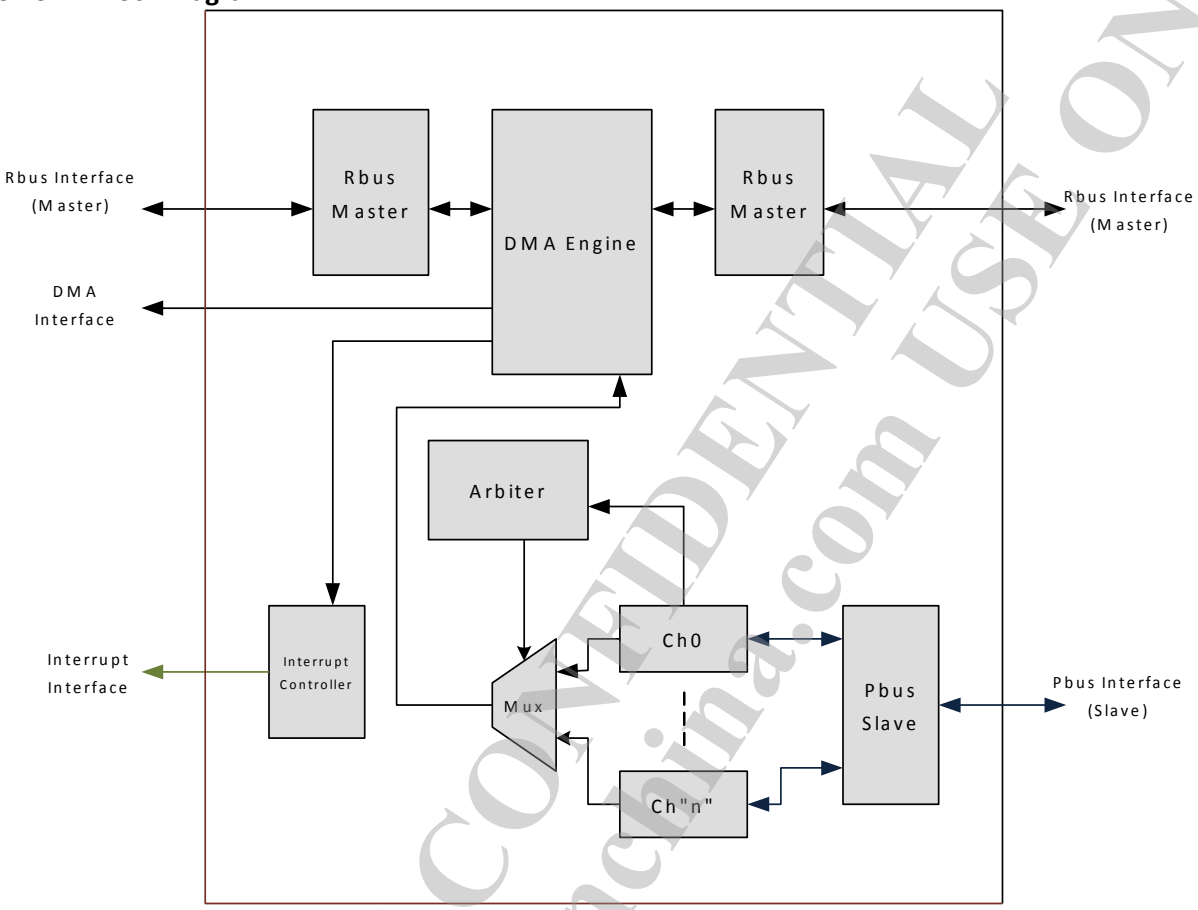


Figure 3-14 Generic DMA Controller Block Diagram

3.13.3 Peripheral Channel Connection

Table 3-4 Peripheral Channel Connection

Channel number	Peripheral
0~1	Reserved
2	I2S Controller (TXDMA)
3	I2S Controller (RXDMA)
4	PCM Controller (RDMA, channel 0)
5	PCM Controller (RDMA, channel 1)
6	PCM Controller (TDMA, channel 0)
7	PCM Controller (TDMA, channel 1)
8~15	Reserved

3.13.4 Register Description (base: 0x1000_2800)

GDMA_SAn: GDMA Channel n Source Address (offset: 0x0000, 0x0010, 0x0020, 0x0030, 0x0040, 0x0050, 0x0060, 0x0070, 0x0080, 0x0090, 0x00a0, 0x00b0, 0x00c0, 0x00d0, 0x00e0, 0x00f0)
(n:0~15)

Bits	Type	Name	Description	Initial value
31:0	RW	CHANNEL SOURCE ADDRESS	Channel Source Address This register contains the source address information.	0x0

GDMA_DAn: GDMA Channel n Destination Address (offset: 0x0004, 0x0014, 0x0024, 0x0034, 0x0044, 0x0054, 0x0064, 0x0074, 0x0084, 0x0094, 0x00a4, 0x00b4, 0x00c4, 0x00d4, 0x00e4, 0x00f4)
(n:0~15)

Bits	Type	Name	Description	Initial value
31:0	RW	CHANNEL DESTINATION ADDRESS	Channel Destination Address This register contains the destination address information.	0x0

GDMA_CT0n: GDMA Channel n Control Register 0 (offset: 0x0008, 0x0018, 0x0028, 0x0038, 0x0048, 0x0058, 0x0068, 0x0078, 0x0088, 0x0098, 0x00a8, 0x00b8, 0x00c8, 0x00d8, 0x00e8, 0x00f8)

(n:0~15)

Bits	Type	Name	Description	Initial value
31:16	RW	Transfer Count	These registers contain the number of the data bytes needed to be transfered.	0x0
15:8	-	-	Reserved	0x0
7	RW	Source Burst Mode	The value represents the source burst mode. 'b0: Incremental mode 'b1: Fix mode	0x0
6	RW	Destination Burst Mode	The value represents the destination burst mode. 'b0: Incremental mode 'b1: Fix mode	0x0
5:3	RW	Burst Size	The number of transfers for a burst transaction. 'b000: 1 transfer 'b001: 2 transfers 'b010: 4 transfers 'b011: 8 transfers 'b100: 16 transfers Others: Undefined	0x0
2	RW	Transmit Done Interrupt Enable	Enables the transmit done interrupt. 'b0: Disable 'b1: Enable	0x0
1	RW	Channel Enable	Enables a channel. 'b0: Disable 'b1: Enable This bit is de-asserted by the hardware when the transaction is done.	0x0
0	RW	Hardware/Software Mode Select	Selects hardware or software mode. 'b0: Hardware mode 'b1: Software mode In software mode, the data transfer starts when the channel enable bit is set. In hardware mode, the data transfer starts when the DMA request is asserted.	0x0

GDMA_CT1n: GDMA Channel n Control Register 1 (offset: 0x000c, 0x001c, 0x002c, 0x003c, 0x004c, 0x005c, 0x006c, 0x007c, 0x008c, 0x009c, 0x00ac, 0x00bc, 0x00cc, 0x00dc, 0x00ec, 0x00fc)

(n:0~15)

Bits	Type	Name	Description	Initial value
31:22	-	-	Reserved	0x0

21:16	RW	Source DMA Request	DMA Request Source Sets the interrupt ID for source DMA on a channel. 0: DMA_REQ0 1: DMA_REQ1 2: DMA_REQ2 … n: DMA_REQn 32: The source of the transfer is memory. Others: Undefined	0x0
15:14	-	-	Reserved	0x0
13:8	RW	Destination DMA Request	Destination DMA request Sets the interrupt ID for destination DMA on a channel. 0: DMA_REQ0 1: DMA_REQ1 2: DMA_REQ2 … n: DMA_REQn 32: The destination of the transfer is memory. Others: Undefined	0x0
7:3	RW	Next Unmasked Channel	The value represents the next unmasked channel. When the transaction is done, the hardware will clear the channel mask bit of the next unmasked channel. 0: Channel 0 1: Channel 1 2: Channel 2 ... n: Channel n If the hardware does not need to clear any channel mask bit, these bits must be set to their own channel.	0x0
2	RW	Coherent Interrupt Enable	When set to 1'b1, the GDMA issues a dummy read to the destination after the last write to the destination. This ensures the last write arrived at MEM and avoids a race problem between interrupt and data to MEM. NOTE: Do not set this to '1'b1' if the destination is not MEM.	0x0
1	RW	Channel Unmasked Interrupt Enable	Channel Unmasked Interrupt Enable 'b0: Disable 'b1: Enable When this bit is set, an interrupt is asserted when the hardware wants to clear the channel mask bit and the channel mask bit is originally '0' .	0x0
0	RW	Channel Mask	Channel Mask 'b0: This channel is not masked. 'b1: This channel is masked. When this channel mask is set, the GDMA transaction does not start until this bit is cleared by the hardware.	0x0

GDMA_UNMASKINT: GDMA Unmasked Interrupt Status Register (offset: 0x0200)

Bits	Type	Name	Description	Initial value
31:0	W1C	Unmasked Interrupt Status	This register contains the unmasked interrupt status. This bit is set when the hardware wants to clear the channel mask bit and the channel mask bit is originally '0'. Bitn~bit0 is for channel-n ~ channel-0, respectively.	0x0

GDMA_DONEINT: GDMA Interrupt Status Register (offset: 0x0204)

Bits	Type	Name	Description	Initial value
31:0	W1C	Transmit Done Interrupt Status	This register contains the transmit-done interrupt status. Bitn~bit0 is for channel-n ~ channel-0, respectively.	0x0

GDMA_GCT: GDMA Global Control Register (offset: 0x0220)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	-
4:3	RO	Total channel number	2'b0: 8 channel 2'b1: 16 channel 2'b2: 32 channel 2'b3: Reserved	0x1
2:1	RO	IP version	Version of GDMA core	0x2
0	RW	Arbitration Selection	Selects the channel arbitration method. 1'b0: Channel-0 has the highest priority. Channel-1~ Channel-n are round-robin. 1'b1: Channel-0 doesn't have the highest priority. Channel-0~Channel-n are round-robin.	0x0

GDMA_REQSTS: GDMA Request Status Register (offset: 0x02a0)

Bits	Type	Name	Descr iption	Initial value
31:0	RO	GDMA Request Signal Status	This register contains the GDMA request signals status. Bitn~bit0 is for GDMA_REQn ~ GDMA_REQ0, respectively.	0x0

GDMA_ACKSTS: GDMA Acknowledge Status Register (offset: 0x02a4)

Bits	Type	Name	Description	Initial value
31:0	RO	GDMA Acknowledge Signal Status	This register contains the GDMA acknowledge signals status. Bitn~bit0 is for GDMA_ACKn ~ GDMA_ACK0, respectively.	0x0

GDMA_FINSTS: GDMA Finish Status Register (offset: 0x02a8)

Bits	Type	Name	Description	Initial value
31:0	RO	GDMA Finish Signal Status	This register contains the GDMA finish signals status. Bitn~bit0 is for GDMA_FINISHn ~ GDMA_FINISH0, respectively.	0x0

3.14 SPI Controller

3.14.1 Features

- Supports up to 2 SPI master operations.
- Programmable clock polarity
- Programmable interface clock rate
- Programmable bit ordering
- Firmware-controlled SPI enable
- Programmable payload (address + data) length

3.14.2 Block Diagram

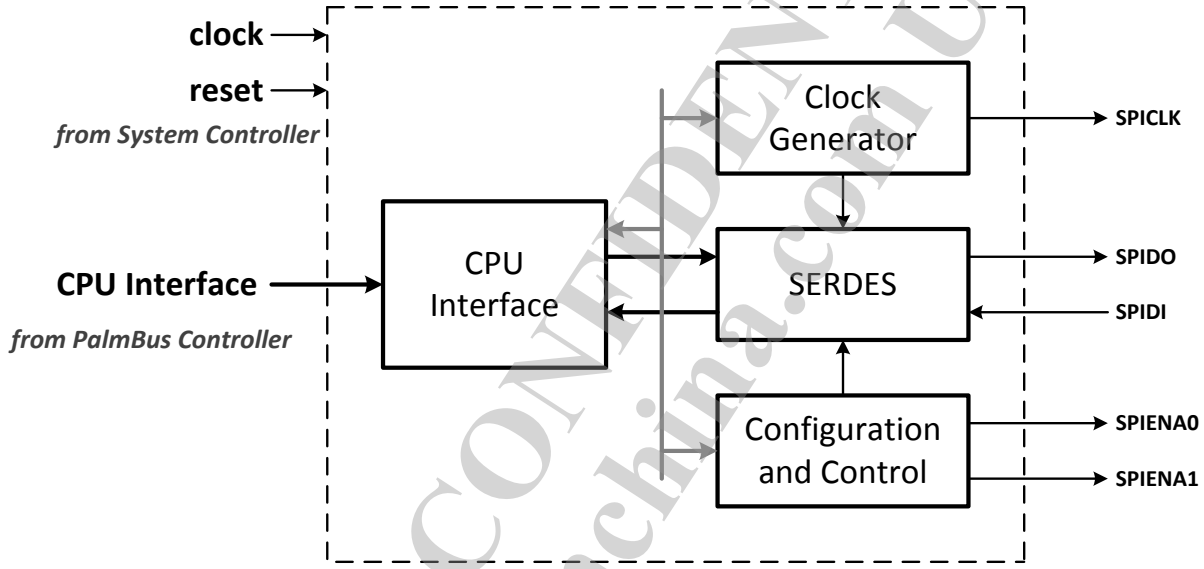


Figure 3-15 SPI Controller Block Diagram

3.14.3 Register Description (base: 0x1000_0b00)

SPISTAT0: SPI Interface 0 Status (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31:1	-	-	Reserved	0x0
0	RO	BUSY	SPI transfer in progress. 0: The SPI interface is inactive. 1: An SPI transfer is in progress. NOTE: This bit must be '0' before initiating a transfer. Any attempt to start a data transfer is ignored if this bit is a '1'.	0x0

SPICFG0: SPI Interface 0 Configuration (offset: 0x0010)

Bits	Type	Name	Description	Initial value
31:9	-	-	Reserved	0x0
8	RW	MSBFIRST	Bit Transfer Order 0: LSB bits of data sent/received first. 1: MSB bits of data sent/received first. NOTE: This bit applies to both the command and data.	0x1
7	-	-	Reserved	0x0

6	RW	SPICLKPOL	SPI Clock Default State 0: The default state of the SPICLK is logic '0'. 1: The default state of the SPICLK is logic '1'. NOTE: This bit is ignored if the SPI interface block is a slave (SPISLAVE bit is set).	0x0
5	RW	RXCKEDGE	SPI Clock Default State 0: Data is captured on the rising edge of the SPICLK signal. 1: Data is captured on the falling edge of the SPICLK signal.	0x0
4	RW	TXCKEDGE	SPI Clock Default State 0: Data is transmitted on the rising edge of the SPICLK signal. 1: Data is transmitted on the falling edge of the SPICLK signal.	0x0
3	RW	HIZSPI	Tri-state all SPI Pins. 0: SPICLK and SPIENA pin are driven. 1: SPICLK and SPIENA pin are tri-stated. NOTE: This bit overrides all normal functionality.	0x0
2:0	RW	SPICLK[2:0]	SPI Clock Divide Control 0: SPICLK rate is system clock rate/2. 1: SPICLK rate is system clock rate/4. 2: SPICLK rate is system clock rate/8. 3: SPICLK rate is system clock rate/16. 4: SPICLK rate is system clock rate/32. 5: SPICLK rate is system clock rate/64. 6: SPICLK rate is system clock rate/128. 7: SPICLK is disabled. NOTE: These rates may be changed in the future.	0x0

SPICTL0: SPI Interface 0 Control (offset: 0x0014)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	0x0
3	RW	HIZSDO	Tri-state Data Out 0: The SPIDO pin remains driven after the cycle is complete. 1: The SPIDO pin is tri-stated after the cycle is complete. NOTE: This bit applies to write transfers only; for read transfers the SPIDO pin is tri-stated during the transfer.	0x0
2	RW	STARTWR	Start SPI Write Transfer 0: No effect. 1: The contents of the SPIDATA register are transferred to the SPI slave device. NOTE: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	0x0
1	RW	STARTRD	0: No effect. 1: A read from the SPI slave is started; the read data is placed in the SPIDATA register. NOTE: The BUSY bit in the SPISTAT register is set when a this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	0x0
0	RW	SPIENA	0: The SPIENA pin is negated. 1: The SPIENA pin is asserted.	0x0

SPIDATA0: SPI Interface 0 Data (offset: 0x0020)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RW	SPIDATA[7:0]	This register is used for command/data transfers on the SPI interface. The use of this register is given below: Write: the bits to be transferred are written here, including both command and data bits. If values are transmitted MSB (most significant bit) first, the command is placed in the upper bits and the data in the lower bits. Bit 0 of the data is written to SPIDATA [0]; bit 0 of the command follows the MSB of the data. If data is transmitted LSB (least significant bit) first, the command is placed in the lower bits and the data is placed in the upper bits. Read: the command bits are written here. Bit 0 of the command is written to SPIDATA[0]. When the transfer is complete, the data transferred from the slave may be read from the lower bits of this register.	0x0

SPISTAT1: SPI Interface 1 Status (offset: 0x0040)

Bits	Type	Name	Description	Initial value
31:2	-	-	Reserved	0x0
0	RO	BUSY	SPI Transfer in Progress 0: The SPI interface is inactive. 1: An SPI transfer is in progress. NOTE: This bit must be '0' before initiating a transfer. Any attempt to start a data transfer is ignored if this bit is a '1'.	0x0

SPICFG1: SPI Interface 1 Configuration (offset: 0x0050)

Bits	Type	Name	Description	Initial value
31:9	-	-	Reserved	0x0
8	RW	MSBFIRST	Bit Transfer Order 0: LSB bits of data sent/received first. 1: MSB bits of data sent/received first. NOTE: This bit applies to both the command and data.	0x1
7	-	-	Reserved	0x0
6	RW	SPICLKPOL	SPI Clock Default State 0: The default state of the SPICLK is logic '0'. 1: The default state of the SPICLK is logic '1'. NOTE: This bit is ignored if the SPI interface block is a slave (SPISLAVE bit is set).	0x0
5	RW	RXCKEDGE	SPI Clock Default State 0: Data is captured on the rising edge of the SPICLK signal. 1: Data is captured on the falling edge of the SPICLK signal.	0x0
4	RW	TXCKEDGE	SPI Clock Default State 0: Data is transmitted on the rising edge of the SPICLK signal. 1: Data is transmitted on the falling edge of the SPICLK signal.	0x0
3	RW	HIZSPI	Tri-state all SPI Pins. 0: SPICLK and SPIENA pin are driven. 1: SPICLK and SPIENA pin are tri-stated. NOTE: This bit overrides all normal functionality.	0x0

2:0	RW	SPICLK[2:0]	SPI Clock Divide Control 0: SPICLK rate is system clock rate/2. 1: SPICLK rate is system clock rate/4. 2: SPICLK rate is system clock rate/8. 3: SPICLK rate is system clock rate/16. 4: SPICLK rate is system clock rate/32. 5: SPICLK rate is system clock rate/64. 6: SPICLK rate is system clock rate/128. 7: SPICLK is disabled. NOTE: These rates may be changed in the future.	0x0

SPICTL1: SPI Interface 1 Control (offset: 0x0054)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	0x0
3	RW	HIZSDO	Tri-state Data Out 0: The SPIDO pin remains driven after the cycle is complete. 1: The SPIDO pin is tri-stated after the cycle is complete. NOTE: This bit applies to write transfers only; for read transfers the SPIDO pin is tri-stated during the transfer.	0x0
2	RW	STARTWR	Start SPI Write Transfer 0: No effect. 1: The contents of the SPIDATA register are transferred to the SPI slave device. NOTE: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	0x0
1	RW	STARTRD	0: No effect. 1: A read from the SPI slave is started; the read data is placed in the SPIDATA register. NOTE: The BUSY bit in the SPISTAT register is set when a this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	0x0
0	RW	SPIENA	0: The SPIENA pin is negated. 1: The SPIENA pin is asserted.	0x0

SPIDATA1: SPI Interface 1 Data (offset: 0x0060)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RW	SPIDATA[7:0]	This register is used for command/data transfers on the SPI interface. The use of this register is given below: Write: the bits to be transferred are written here, including both command and data bits. If values are transmitted MSB (most significant bit) first, the command is placed in the upper bits and the data in the lower bits. Bit 0 of the data is written to SPIDATA[0]; bit 0 of the command follows the MSB of the data. If data is transmitted LSB (least significant bit) first, the command is placed in the lower bits and the data is placed in the upper bits. Read: the command bits are written here. Bit 0 of the command is written to SPIDATA[0]. When the transfer is complete, the data transferred from the slave may be read from the lower bits of this register.	0x0

SPIARB: SPI Interface ARBITER (offset: 0x00f0)

NOTE: This register must be configured before activating SPI interface 1.

Bits	Type	Name	Description	Initial value
31	RW	ARB_EN	Arbiter Enable 0: Only the SPI interface 0 works. 1: The SPI Interface 0/1 works concurrently.	0x0
30:2	-	-	Reserved	0x0
1	RW	SPI1_POR	SPI Interface 1 Chip Polarity Indicator Enable 0: Indicate the chip enable is low active 1: Indicate the chip enable is high active	0x1
0	RW	SPI0_POR	SPI Interface 0 Chip Polarity Indicator Enable 0: Indicate the chip enable is low active 1: Indicate the chip enable is high active	0x1

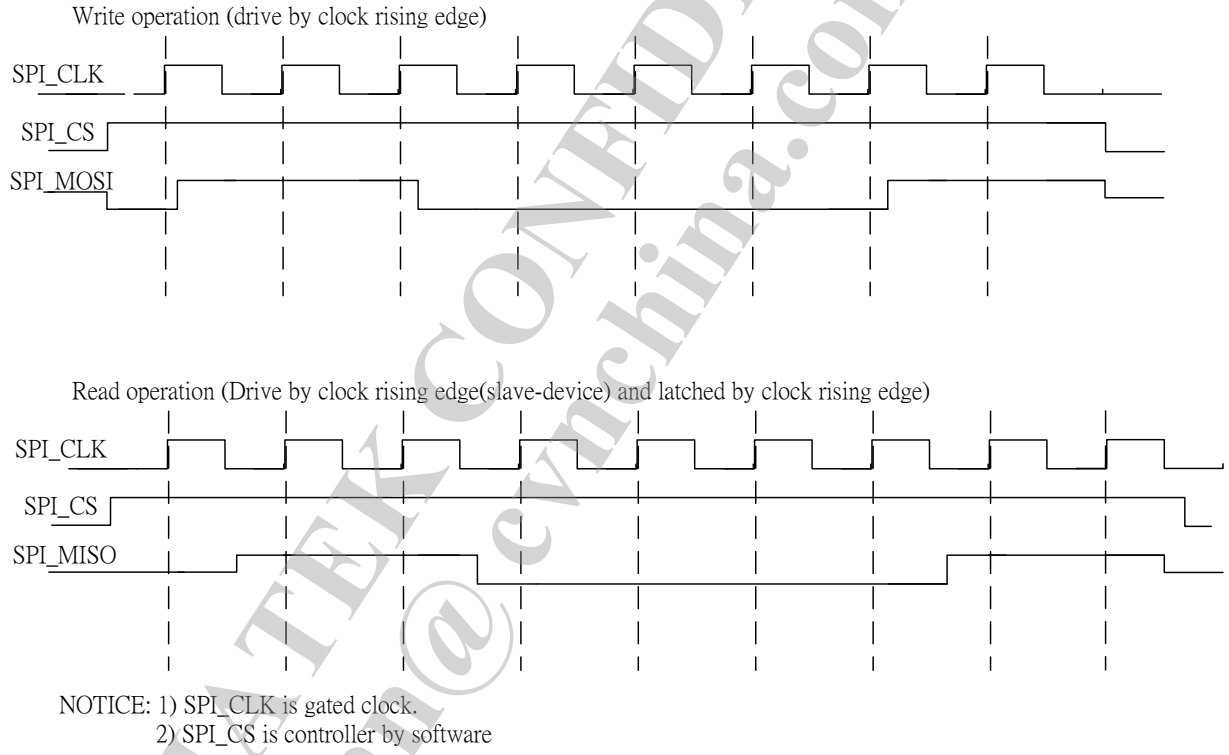


Figure 3-16 Waveform of SPI Interface

3.15 I²S Controller

3.15.1 Features

- I²S transmitter/Receiver, which can be configured as master or slave.
- Supports 16-bit data, sample rate 8 Khz, 16 Khz, 22.05 Khz, 44.1 Khz, and 48 Khz
- Supports stereo audio data transfer.
- 32-byte FIFO is available for data transmission.
- Supports GDMA access
- Supports an external 12 Mhz bit clock (in slave mode)

3.15.2 Block Diagram

The block diagram of the I²S transmitter is shown below.

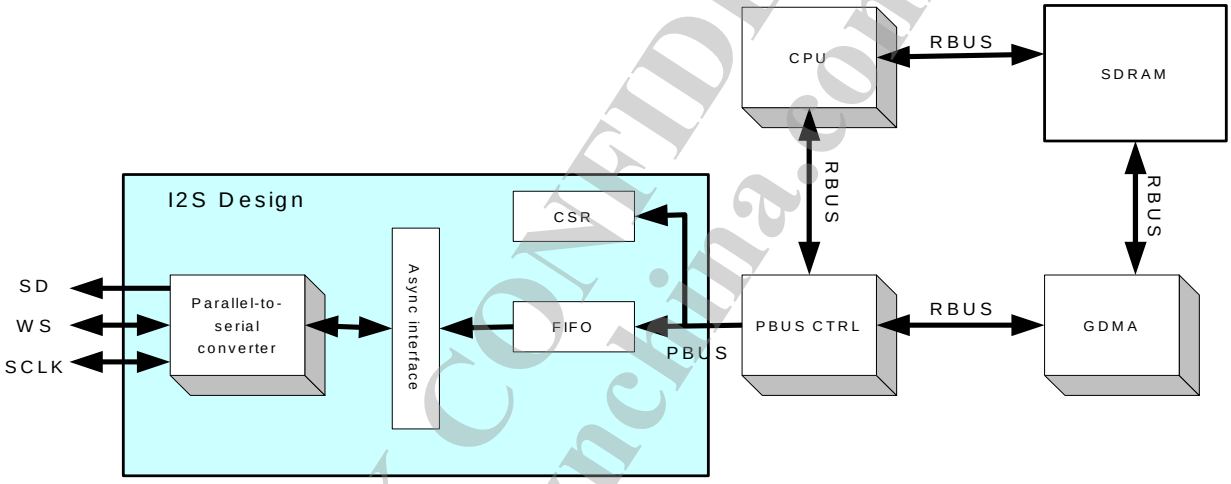


Figure 3-17 I²S Transmitter Block Diagram

The I²S interface consists of two separate cores, a transmitter and a receiver. Both can operate in either master or slave mode. Here we design only the transmitter in master or slave mode.

3.15.3 I²S Signal Timing for I²S Data Format

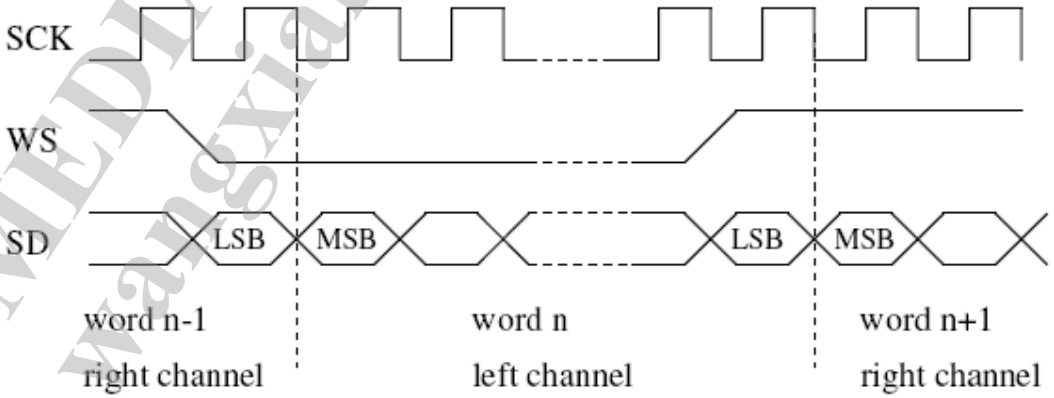


Figure 3-18 I²S Transmitter/Receiver

Serial data is transmitted in 2's complement with the MSB first. The transmitter always sends the MSB of the next word one clock period after the WS changes. Serial data sent by the transmitter may be synchronized with either the trailing (HIGH-to-LOW) or the leading (LOW-to-HIGH) edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when transmitting data that is synchronized with the leading edge.

The word select line indicates the channel being transmitted:

- WS = 0; channel 1 (left)
- WS = 1; channel 2 (right).

WS may change either on a trailing or leading edge of the serial clock, but it doesn't need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The WS line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word.

3.15.4 Register Description of I²S (base: 0x1000_0a00)

I2S_CFG: Tx/Rx Configuration (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31	RW	I2S_EN	I²S Enable 0: Disable, all I²S control registers are cleared to their default values. 1: Enable	0x0
30	RW	DMA_EN	DMA Enable 0: Disable DMA access. 1: Enable DMa access.	0x0
29:25	-	Reserved	Reserved	0x0
24	RW	TX_EN	Transmitter On/off Control 0: Disable the transmitter. 1: Enable the transmitter.	0x0
23:21	-	Reserved	Reserved	0x0
20	RW	RX_EN	Receiver On/off control 0: Disable receiver. 1: Enable receiver.	0x0
19:17	-	Reserved	Reserved	0x0
16	RW	SLAVE_MODE	Master or Slave 0: Master: using the internal clock 1: Slave: using an external clock	0x1
15	-	Reserved	Reserved	0x0
14:12	RW	RX_FF_THRES	FIFO Threshold When the threshold is reached, the host/DMA is notified to fill the FIFO. (unit = word) It should be >2 and <6.	0x4
11	-	Reserved	Reserved	0x0
10	-	Reserved	Reserved	0x0
9	-	Reserved	Reserved	0x0
8:7	-	Reserved	Reserved	0x0
6:4	RW	TX_FF_THRES	FIFO Threshold When the threshold is reached, the host/DMA is notified to fill the FIFO. (unit = word) It should be >2 and <6.	0x4
3	-	Reserved	Reserved	0x0

2	-	Reserved	Reserved	0x0
1	-	Reserved	Reserved	0x0
0	-	Reserved	Reserved	0x0

INT_STATUS: I²S Interrupt Status (offset: 0x0004)

Bits	Type	Name	Description	Initial value
31:8	-	Reserved	Reserved	0x0
7	RW	RX_DMA_FAULT	Detects errors in Rx DMA signals.	0x0
6	RW	RX_OVRUN	The Rx FIFO has an overflow. 1: Clear	0x0
5	RW	RX_UNRUN	The Rx FIFO has an underflow. 1: Clear	0x0
4	RW	RX_THRES	The Rx FIFO is lower than the defined threshold. 1: Clear	0x0
3	RW	TX_DMA_FAULT	Detects errors in Tx DMA signals.	0x0
2	RW	TX_OVRUN	The Tx FIFO has an overflow. 1: Clear	0x0
1	RW	TX_UNRUN	The Tx FIFO has an underflow. 1: Clear	0x0
0	RW	TX_THRES	The FIFO is lower than the defined threshold. 1: Clear	0x0

INT_EN: I²S Interrupt Enable Control Register (offset: 0x0008)

Bits	Type	Name	Description	Initial value
31:9	-	Reserved	Reserved	0x0
7	RW	RX_INT3_EN	Enables INT_STATUS[7].	0x0
6	RW	RX_INT2_EN	Enables INT_STATUS[6].	0x0
5	RW	RX_INT1_EN	Enables INT_STATUS[5].	0x0
4	RW	RX_INT0_EN	Enables INT_STATUS[4].	0x0
3	RW	TX_INT3_EN	Enables INT_STATUS[3].	0x0
2	RW	TX_INT2_EN	Enables INT_STATUS[2].	0x0
1	RW	TX_INT1_EN	Enables INT_STATUS[1].	0x0
0	RW	TX_INT0_EN	Enables INT_STATUS[0].	0x0

FF_STATUS: I2S Tx/Rx FIFO Status (offset: 0x000c)

Bits	Type	Name	Description	Initial value
31:8	-	Reserved	Reserved	0x0
7:4	RO	RX_AVCNT	Available FIFO space can be read.	0x0
3:0	RO	TX_EPCNT	Available FIFO space can be written.	0x8

TX_FIFO_WREG: Write Data Buffer offset: 0x0010)

Bits	Type	Name	Description	Initial value
31:0	RW	TX_FIFO_WDATA	Writes data buffer.	0x0

RX_FIFO_RREG: Read Data Buffer (offset: 0x0014)

Bits	Type	Name	Description	Initial value
31:0	RO	RX_FIFO_WDATA	Reads data buffer.	0x0

I²S_CFG1: I²S Loopback Test Control Register (offset: 0x0018)

Bits	Type	Name	Description	Initial value
31	RW	LBK_EN	Loopback Enable 0: Normal mode	0x0

			1: Loopback mode Async_txFifio → Tx → Rx → Async_rxFifio	
30	RW	EXT_LBK_EN	External Loopback Enable 0: Normal mode 1: Enable external loopback External A/D → Rx → Tx → External D/A	0x0
29:2	-	Reserved	Reserved	0x0
1:0	-	Reserved	Reserved	0x0

DIVCOMP_CFG: Integer Part of Dividor Register (offset: 0x0020)

Bits	Type	Name	Description	Initial value
31	RW	CLK_EN	Clock Dividor	0x0
30:9	-	-	Reserved	0x0
8:0	RW	DIVCOMP	A parameter in an equation which determines FreqOut. See DIVINT.	0x0

DIVINT_CFG: Integer part of Dividor Register (offset: 0x0024)

Bits	Type	Name	Description	Initial value
31:10	-	-	Reserved	0x0
9:0	RW	DIVINT	A parameter in an equation which determines FreqOut. Formula: FreqOut = FreqIn *(1/2) *{1 / [DIVINT+DIVCOMP/(512)]} FreqIn is always fixed to 40 MHz.	0x0

3.16 Memory Controller

3.16.1 Features

- Supports 2 SDRAM (16 b) chip selection.
- Supports 1 SRAM (8/16 b) chip selection.
- Supports 32 MB/SDRAM per chip selection.
- Supports SDRAM transaction overlapping by early active and hidden pre-charge.
- Supports user SDRAM Init commands.
- Supports 4 banks per SDRAM chip selection.
- SDRAM burst length: 4 (fixed).
- Supports Wrap-4 transfer.
- Supports Bank-Raw-Column and Raw-Bank-Column address mapping.

3.16.2 Block Diagram

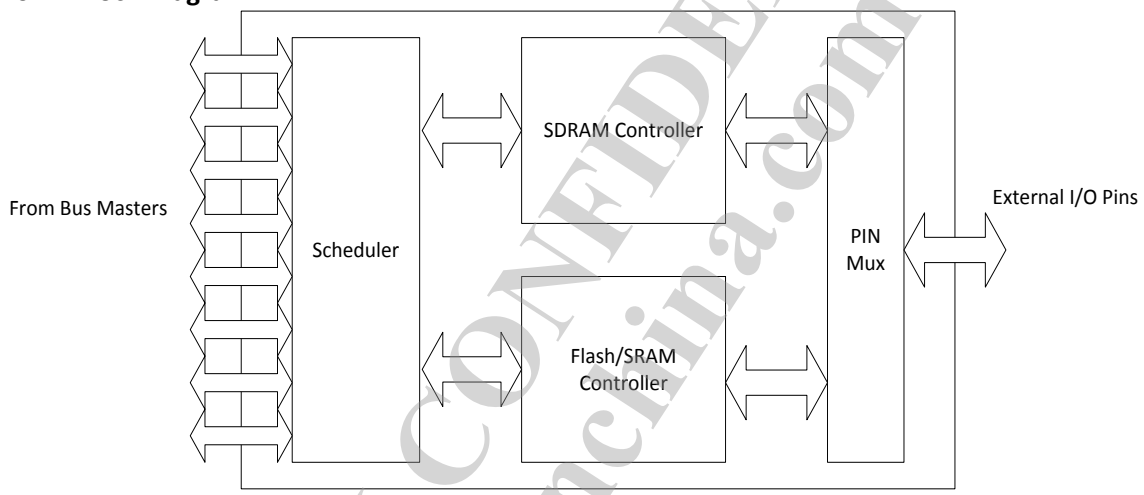


Figure 3-19 SRAM/SDRAM Controller Block Diagram

3.16.3 SDRAM Initialization Sequence

SDRAMs require an initialization sequence before they are ready for reading and writing. The initialization sequence is described below.

1. Set SDRAM related timing in SDRAM_CFG0.
2. Set SDRAM size and refresh time in SDRAM_CFG1. Register with SDRAM_INIT_START = 1.
3. Read SDRAM_INIT_DONE in the SDRAM_CFG1 register.
4. If SDRAM_INIT_DONE !=1, go to 3, otherwise the SDRAM initialization sequence is finished.

Table 3-5 Turn Off Power Saving

Size	DRAM width (16-bit), total bus width 16	DRAM width (16-bit), total bus width 32	DRAM width (32-bit), total bus width 32
16 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xA0000600	SDRAM0: 0xD1825272, SDRAM1: 0xA1000600	N/A
64 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xA0010600	SDRAM0: 0xD1825272, SDRAM1: 0xA1010600	SDRAM0: 0xD1825272, SDRAM1: 0xA1000600
128 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xA0110600	SDRAM0: 0xD1825272, SDRAM1: 0xA1110600	SDRAM0: 0xD1825272, SDRAM1: 0xA1010600
256 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xA0120600	SDRAM0: 0xD1825272, SDRAM1: 0xA1120600	SDRAM0: 0xD1825272, SDRAM1: 0xA1110600
512 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xA0220600	SDRAM0: 0xD1825272, SDRAM1: 0xA1220600	SDRAM0: 0xD1825272, SDRAM1: 0xA1120600
1024 Mb	N/A	N/A	N/A
2048 Mb	N/A	N/A	N/A

Table 3-6 Turn On Power Saving with Precharge Power Down Mode

Size	DRAM width (16-bit), total bus width 16	DRAM width (16-bit), total bus width 32	DRAM width (32-bit), total bus width 32
16 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB0000600	SDRAM0: 0xD1825272, SDRAM1: 0xB1000600	N/A
64 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB0010600	SDRAM0: 0xD1825272, SDRAM1: 0xB1010600	SDRAM0: 0xD1825272, SDRAM1: 0xB1000600
128 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB0110600	SDRAM0: 0xD1825272, SDRAM1: 0xB1110600	SDRAM0: 0xD1825272, SDRAM1: 0xB1010600
256 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB0120600	SDRAM0: 0xD1825272, SDRAM1: 0xB1120600	SDRAM0: 0xD1825272, SDRAM1: 0xB1110600
512 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB0220600	SDRAM0: 0xD1825272, SDRAM1: 0xB1220600	SDRAM0: 0xD1825272, SDRAM1: 0xB1120600
1024 Mb	N/A	N/A	N/A
2048 Mb	N/A	N/A	N/A

Table 3-7 Turn On Power Saving with Active Power Down Mode

Size	DRAM width (16-bit), total bus width 16	DRAM width (16-bit), total bus width 32	DRAM width (32-bit), total bus width 32
16 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB8000600	SDRAM0: 0xD1825272, SDRAM1: 0xB9000600	N/A (ISSI does not have this size)
64 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB8010600	SDRAM0: 0xD1825272, SDRAM1: 0xB9010600	SDRAM0: 0xD1825272, SDRAM1: 0xB9000600
128 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB8110600	SDRAM0: 0xD1825272, SDRAM1: 0xB9110600	SDRAM0: 0xD1825272, SDRAM1: 0xB9010600
256 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB8120600	SDRAM0: 0xD1825272, SDRAM1: 0xB9120600	SDRAM0: 0xD1825272, SDRAM1: 0xB9110600
512 Mb	SDRAM0: 0xD1825272, SDRAM1: 0xB8220600	SDRAM0: 0xD1825272, SDRAM1: 0xB9220600	SDRAM0: 0xD1825272, SDRAM1: 0xB9120600
1024 Mb	N/A	N/A	N/A
2048 Mb	N/A	N/A	N/A

3.16.4 Register Description (base: 0x1000_0300)

SDRAM_CFG0: SDRAM Configuration 0 (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31	RO	ALWAYS_ONE	Used as an identification for the Rbus controller.	0x1
30:29	-	-	Reserved	0x0
28	RW	TWR	Write recovery time number of system clock cycles – 1.	0x1
27:24	RW	TMRD	LOAD MODE to any other command delay number of system clock cycles – 1.	0x1
23:20	RW	TRFC	AUTO REFRESH period number of system clock cycles – 1.	0x9
19:18	-	-	Reserved	0x0
17:16	RW	TCAS	READ command to data valid delay (CAS latency) in number of system clock cycles – 1.	0x2
15:12	RW	TRAS	ACTIVE to PRECHARGE command delay in number of system clock cycles – 1.	0x5
11:10	-	-	Reserved	0x0
9:8	RW	TRCD	ACTIVE to READ or WRITE delay in number of system clock cycles – 1.	0x2
7:4	RW	TRC	ACTIVE to ACTIVE command period in number of system clock cycles -1	0x8
3:2	-	-	Reserved	0x0

1:0	RW	TRP	PRECHARGE command period in number of system clock cycles – 1.	0x2

SDRAM_CFG1: SDRAM Configuration 1 (offset: 0x0004)

Bits	Type	Name	Description	Initial value
31	RW	SDRAM_INIT_START	Write '1' to perform SDRAM initialization sequence. Can not set it to '0' after initialization.	0x0
30	RO	SDRAM_INIT_DONE	0: SDRAM has not been initialized. 1: SDRMA has been initialized.	0x0
29	RW	RBC_MAPPING	0: {BANK ADDR, ROW ADDR, COL ADDR} address mapping scheme 1: {ROW ADDR, BANK ADDR, COL ADDR} address mapping scheme	0x0
28	RW	PWR_DOWN_EN	0: Disable SDRAM precharge power-down mode. 1: Enable SDRAM precharge power-down mode to save standby power. When enabled, SDRAM will power-down..	0x0
27	RW	PWR_DOWN_MODE	0: Precharge power down mode 1: Active power down mode	0x0
26:25	-	-	Reserved	0x0
24	RW	SDRAM_WIDTH	Number of SDRAM Data Bus Bits 0: 16 bits (default) 1: Reserved	0x0
23:22	-	-	Reserved	0x0
21:20	RW	NUMCOLS	Number of Column Address Bits 0: 8 column address bits 1: 9 column address bits (default) 2: 10 column address bits 3: 11 column address bits	0x1
19:18	-	-	Reserved	0x0
17:16	RW	NUMROWS	Number of Row Address Bits 0: 11 row address bits 1: 12 row address bits (default) 2: 13 row address bits 3: 14 row address bits (not allocable if boot from NAND flash is enabled.)	0x2
15:0	RW	TREFR	Auto-refresh period in number of SDRAM clock cycles – 1.	0x600

*NOTE: SDRAM Self Refresh Mode and Power Down will be supported later.

DRAM_ARB_CFG: DRAM Arbiter Configuration (offset: 0x0008)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	0x0
30	RW	Round_Robin_EN	Enables round-robin policy for the arbiter. 0: Disable 1: Enable	0x0
29	RW	CPU_POST_LOCK_EN	Enables the arbiter to lock the CPU for an interval after servicing. 0: Disable 1: Enable	0x0
28	RW	CPU_PRE_LOCK_EN	Enables the arbiter to lock the CPU when a CPU command in the OCP bus is detected. 0: Disable 1: Enable	0x0
27:16	-	0	Reserved	0x000
15:8	RW	DMA_PENDING	The counter is used to cancel the CPU lock when a DMA request	0x00

		_CNT	is pending for the specified clock count. The valid value is 1~255. '0' cancels the CPU pre/post lock function.	
7:4	-	-	Reserved	0x0
3:0	RW	CPU_LOCK_ CNT	The counter is used to measure the period for which the CPU is locked after servicing the CPU. The valid range is 1~15 cycles. '0' means the post lock period is 0 cycles.	0x0

ILL_ACC_ADDR: Illegal Access Address Capture (offset: 0x0010)

Bits	Type	Name	Description	Initial value
31:0	RO	ILL_ACC_ADDR	If any bus masters (including the CPU) issue illegal accesses (e.g. accessing reserved memory space, non-double-word accessing configuration registers), the address of the illegal transaction is captured in this register. An illegal interrupt is generated to indicate this exception.	0x0

ILL_ACC_TYPE: Illegal Access TYPE Capture (offset: 0x0014)

Bits	Type	Name	Description	Initial value
31	W1C	ILL_INT_STATUS	0: Indicate the illegal access interrupt is cleared. 1: Indicate the illegal access interrupt is pending. Write '1' to this bit to clear both ILL_ACC_ADDR and ILL_ACC_TYPE registers and thus clear the ILL_INT_STATUS.	0x0
30	RO	ILL_ACC_WR	Indicates the read/write status of the illegal access. 1 : Illegal access is written. 0 : Illegal access is read. This value is reset to '0' when ILL_ACC_ADDR is written.	0x0
29:20	-	-	Reserved	0x0
19:16	RO	ILL_ACC_BSEL	Illegal Access Byte Select Indicates illegal access to which byte(s.) This value is reset to '0' when ILL_ACC_ADDR is written.	0x0
15:11	-	-	Reserved	0x0
10:8	RO	ILL_IID	Indicates the initiator ID of the illegal access. 0: CPU 1: DMA 2: PPE 3: Ethernet PDMA Rx 4: Ethernet PDMA Tx 5: PCI/PCIE 6: Embedded WLAN MAC/BBP 7: USB This value is reset to '0' when ILL_ACC_ADDR is written.	0x0
7:0	RO	ILL_ACC_LEN	Indicates the access size of the illegal access. (unit: bytes) This value is reset to '0' when ILL_ACC_ADDR is written.	0x0

SDR_PWR_SAVE_CNT: (offset: 0x001c)

Bits	Type	Name	Description	Initial value
31:24	RO	PD_CNT	A counter to show the times when self-refresh mode is entered (only for DDR2).	0x0
23:0	RW	SR_TAR_CNT	This counter is only referenced when SDR(PWR_DOWN_EN) is set. This counter is used to count the period of the SDR IDLE status. When the IDLE period reaches the specified time period (SR_TAR_CNT*16/SYS_CLK_FREQ), the SDR automatically enters power saving or self-refresh mode. Use software to	0x3ffff

			configure a suitable value for this bit. Here is the reference table. 125 MHz: 0x3ffff * 16* 8.0ns ~= 46 ms	

3.17 USB Host Controller & PHY

3.17.1 Features

- Complies with the USB 2.0 Specification.
- Complies with Host Controller Interface (OHCI) Specification, Version 1.0a.
- Supports ping and split transactions.
- Descriptor and data prefetching.
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- UTMI (legacy), UTMI+ to the PHY

3.17.2 Block Diagram

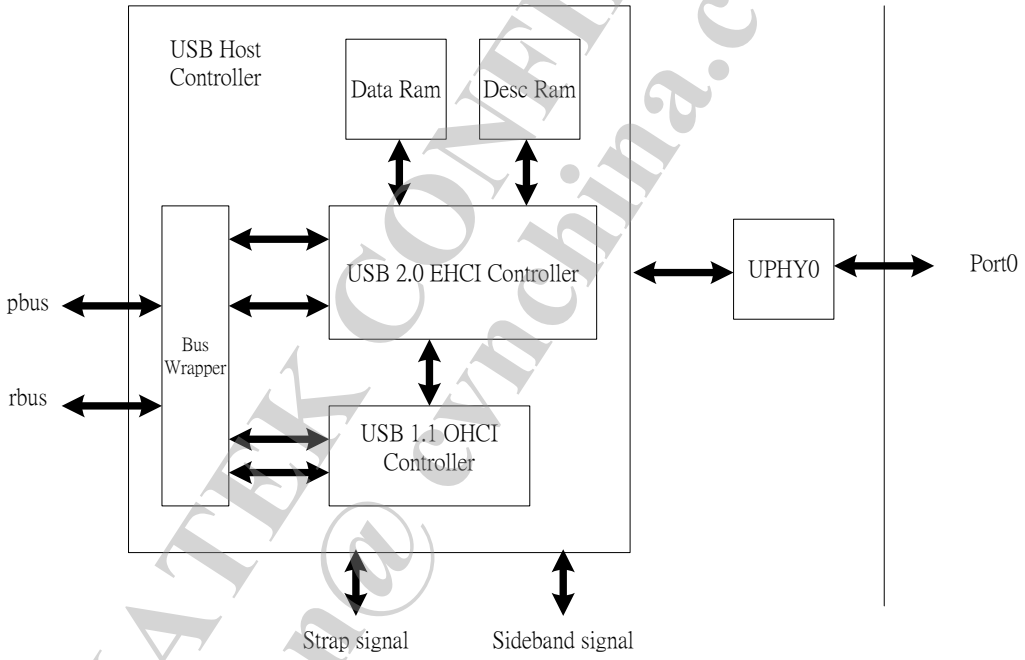


Figure 3-20 USB Host Controller & PHY Block Diagram

3.17.3 Register Description (base: 0x101c_0000)

NOTE: To program EHCI and OHCI registers and initialize the core, refer to the Enhanced Host Controller Interface Specification for Universal Serial Bus and the Open Host Controller Interface Specification for USB, respectively.

3.17.4 EHCI Operation register (base: 0x101c_0000)

3-8 EHCI Capability Register

Mnemonic	Register Name	Offset From EHCI AHB Slave Start Address	Default Value
HCCAPBASE	Capability Register	USBBASE[1] + 00h	32'h01000010
HCSPARAMS	Structural Parameter	USBBASE + 04h	32'h00001116
HCCPARAMS	Capability Parameter	USBBASE + 08h	32'h0000A010 **Note:** The Isochronous Scheduling Threshold value is set to 1 by default. If Descriptor/Data Prefetch is selected, the value is set 2.

USBBASE is fixed to the EHCI slave start address = 0x101c_0000.

3-9 EHCI Operational Registers

Mnemonic	Register Name	Offset From EHCI AHB Slave Start Address[1]	Default Value
USBCMD	USB Command	USBOPBASE[1] + 00h	32'h00080000 or 32'h00080B00[2]
USBSTS	USB Status	USBOPBASE + 04h	32'h00001000
USBINTR	USB Interrupt Enable	USBOPBASE + 08h	32'h00000000
FRINDEX	USB Frame Index	USBOPBASE + 0ch	32'h00000000
CTRLDSSEGMENT	4G Segment Selector	USBOPBASE + 10h	32'h00000000
PERIODICLISTBASE	Periodic Frame List Base Address Register	USBOPBASE + 14h	32'h00000000
ASYNCLISTADDR	Asynchronous List Address	USBOPBASE + 18h	32'h00000000

1. USBOPBASE is fixed to the EHCI slave start address + `h10 (offset = `h10).
2. The default value depends on whether Async park capability is enabled. Disabled = 32'h0008_0000 and enabled = 32'h0008_0B00.

The default value is:

- 32'h0008_0000 if Async park capability is disabled (through coreConsultant).
- 32'h0008_0B00 if Async park capability is enabled.

3-10 EHCI Auxiliary Power Well Registers

Mnemonic	Register Name	Offset From EHCI AHB Slave Start Address	Default Value
CONFIGFLAG	Configured Flag Register	USBOPBASE + 40h	32'h00000000
PORTSC_1 to PORTSC_15	Port Status/Control	USBOPBASE + 44h	32'h00002000

3.17.5 OHCI Operation register (base: 0x101c_1000)

Offset	31 0
0	HcRevision
4	HcControl
8	HcCommandStatus
C	HcInterruptStatus
10	HcInterruptEnable
14	HcInterruptDisable
18	HcHCCA
1C	HcPeriodCurrentED
20	HcControlHeadED
24	HcControlCurrentED
28	HcBulkHeadED
2C	HcBulkCurrentED
30	HcDoneHead
34	HcFmInterval
38	HcFmRemaining
3C	HcFmNumber
40	HcPeriodicStart
44	HcLSThreshold
48	HcRhDescriptorA
4C	HcRhDescriptorB
50	HcRhStatus
54	HcRhPortStatus[1]
...	...
54+4*NDP	HcRhPortStatus[NDP]

3.18 USB Device Controller

3.18.1 Features

- The USB 2.0 Specification (Revision 1.0a) operates in high-speed (HS, 480 Mbps), full-speed (FS, 12 Mbps), and low-speed (LS, 1.5 Mbps) modes.
- Supports 1 bulk-in and bulk out endpoints, including control endpoint 0.
- Packet DMA (PDMA) is integrated for efficient data transfer.
- Supports bulk-out aggregation features. More than one packet can be aggregated to single bulk transfer.
- Supports four Rx descriptor rings and two Tx descriptor rings for QoS service.

3.18.1.1 PDMA Descriptor Format

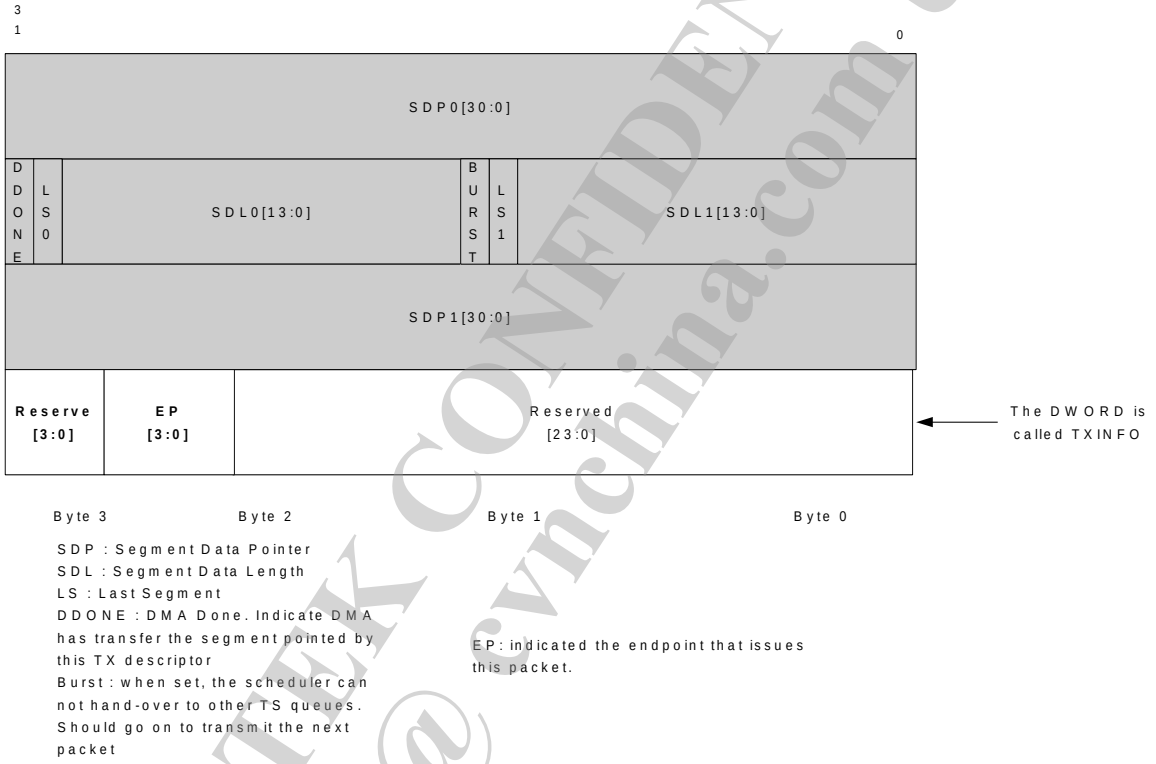
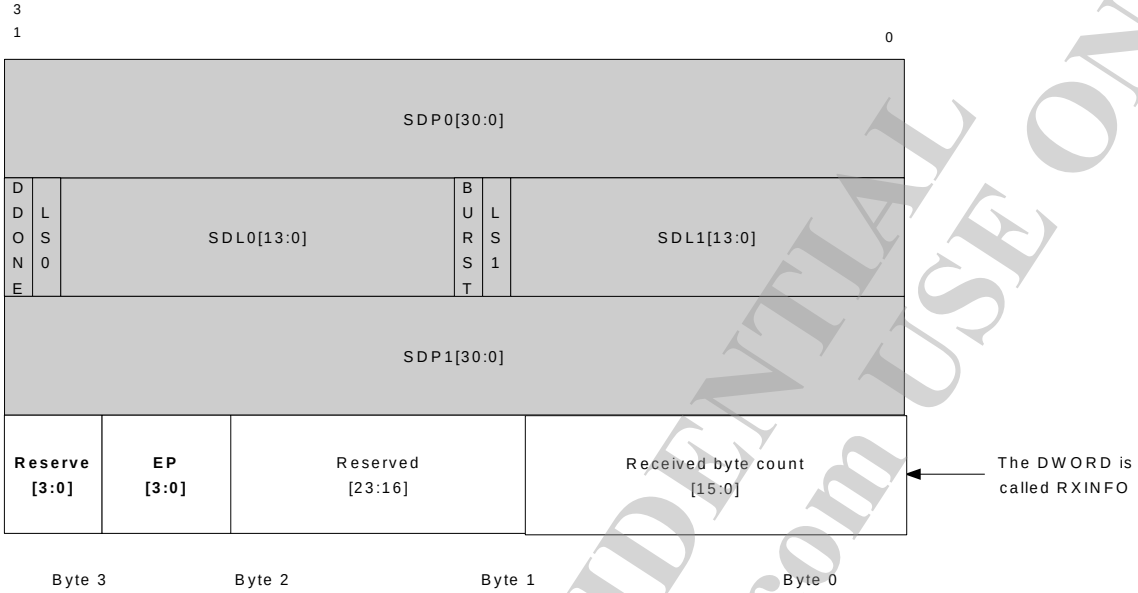


Figure 3-21 PDMA Tx Descriptor Format

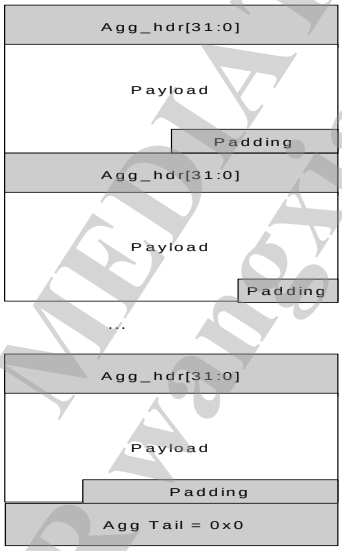


SDP : Segment Data Pointer
SDL : Segment Data Length
LS : Last Segment
DDONE : DMA Done. Indicate DMA has transfer the segment pointed by this TX descriptor
Burst : when set, the scheduler can not hand-over to other TS queues. Should go on to transmit the next packet

EP: indicated the endpoint that issues this packet.

Figure 3-22 PDMA Rx Descriptor Format

3.18.1.2 Bulk-out Aggregation Format



Agg_hdr[31:0]
Agg_hdr[31:16] reserved;
Agg_hdr[15:0] payload_length;

Notice:
1) Each aggregation frame should add padding to align 4 byte boundary.
2) the payload_length indicator the length of payload (no include padding)

Figure 3-23 Bulk-out Aggregation Format

3.18.2 Register Description (base: 0x1012_0000)

3.18.2.1 USB Control Registers

Refer to ***case_cusb2_spec.pdf***.
Registers address = Byte address * 4.

3.18.2.2 UDMA Registers

UDMA_CTRL: (offset: 0x0800)

Bits	Type	Name	Description	Initial value
31:25	-	-	Reserved	0x0
24	RW	EPOUT1_DMAEN	EPOUT1 UDMA Enable	0x0
23:17	-	-	Reserved	0x0
16	RW	EPOUT1_AGGEN	EPOUT1 UDMA De-aggregation Enable	0x0
15:10	-	-	Reserved	0x0
9:8	RW	EPOUT1_QSEL	EPOUT1 Rx Ring Mapping.	0x0
7:5	-	-	Reserved	0x0
4	RW	WAKEUP_EN	USB Wakeup Host Enable	0x0
3:2	-	-	Reserved	0x0
1	RW	UDMA_RX_EN	UDMA Rx Enable	0x0
0	RW	UDMA_TX_EN	UDMA Tx Enable	0x0

UDMA_WRR: (offset: 0x0804)

Bits	Type	Name	Description	Initial value
31:30	-	-	Reserved	0x0
29:28	RW	SCH_MODE	Scheduling Mode 00: WRR 01: Strict priority, EP1 > EP2 > EP3 > EP4 > EP5 > EP6 10: Mixed mode, EP1 > EP2 > WRR(EP3, EP4, EP5, EP6)	0x0
27:23	-	-	Reserved	0x0
22:20	RW	SCH_WT_EP6	Scheduling Weight of EPOUT6	0x0
19	-	-	Reserved	0x0
18:16	RW	SCH_WT_EP5	Scheduling Weight of EPOUT5	0x0
15	-	-	Reserved	0x0
14:12	RW	SCH_WT_EP4	Scheduling Weight of EPOUT4	0x0
11	-	-	Reserved	0x0
10:8	RW	SCH_WT_EP3	Scheduling Weight of EPOUT3	0x0
7	-	-	Reserved	0x0
6:4	RW	SCH_WT_EP2	Scheduling Weight of EPOUT2	0x0
3	-	-	Reserved	0x0
2:0	RW	SCH_WT_EP1	Scheduling Weight of EPOUT1	0x0

3.18.2.3 PDMA Registers

TX_RING_NUM = 2

RX_RING_NUM = 4

TX_BASE_PTRn: (offset: 0x1000, 0x1010, 0x1020, 0x1030)
(n=0~TX_RING_NUM-1, offset = 0x1000 + n*10)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:0	RW	TX_BASE_PTR0	Points to the base address of TX_Ring0 (4-DWORD aligned address).	0x0

TX_MAX_CNTn: (offset: 0x1004, ox1014, 0x1024, 0x1034)
(n=0~TX_RING_NUM-1, offset = 0x1004 + n*10)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RW	TX_MAX_CNT0	The maximum number of TXD count in TXD_Ring0.	0x0

TX_CTX_IDXn: (offset: 0x1008, 0x1018, 0x1028, 0x1038)
(n=0~TX_RING_NUM-1, offset = 0x1008 + n*10)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RW	TX_CTX_IDX0	Points to the next TXD that the CPU will use.	0x0

TX_DTX_IDXn: (offset: 0x100c, 0x101c, 0x102c, 0x103c)
(n=0~TX_RING_NUM-1, offset = 0x100c + n*10)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RO	TX_DTX_IDX0	Points to the next TXD that the DMA will use.	0x0

RX_BASE_PTR0: (offset: 0x1100, 0x1110)
(n=0~RX_RING_NUM-1, offset = 0x1100 + n*10)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:0	RW	RX_BASE_PTR0	Points to the base address of RXD Ring #0 (GE ports). It should be a 4-DWORD aligned address.	0x0

RX_MAX_CNT0: (offset: 0x1104, 0x1114)
(n=0~RX_RING_NUM-1, offset = 0x1104 + n*10)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RW	RX_MAX_CNT0	The maximum RXD count in RXD Ring #0.	0x0

RX_CALC_IDX0: (offset: 0x1108, 0x1118)
(n=0~RX_RING_NUM-1, offset = 0x1100 + n*10)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RW	RX_CALC_IDX0	Points to the next RXD that the CPU will allocate to RXD Ring #0.	0x0

FS _DRX_IDX0: (offset: 0x110c, 0x111c)
(n=0~RX_RING_NUM-1, offset = 0x1100 + n*10)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RW	RX_DRX_IDX0	Points to the next RXD that the DMA will use in FDS Ring #0. It should be a 4-DWORD aligned address.	0x0

PDMA_INFO: (offset:0x1200)

Bits	Type	Name	Description	Initial value
31:28	RO	VERSION	PDMA Controller Version	0x1
27:24	RO	INDEX_WIDTH	Ring Index Width	0xC
23:16	RO	BASE_PTR_WIDTH	Base Pointer Width, x Base_addr[31:32-x] is shared with all ring base addresses.	0x0

			Only ring 0's base address [31:32-x] field is writable. NOTE: '0' means no bit in the base_address is shared.	
15:8	RO	RX_RING_NUM	Rx Ring Number	0x1
7:0	RO	TX_RING_NUM	Tx Ring Number	0x2

PDMA_GLO_CFG: (offset: 0x1204)

Bits	Type	Name	Description	Initial value
31:29	-	-	Reserved	0x0
28:16	RW	HDR_SEG_LEN	Specifies the header segment size in bytes to support the Rx header/payload scattering function, when set to a non-zero value. When set to '0', the header/payload scattering feature is disabled.	0x0
15:8	-	-	Reserved	0x0
7	RW	BIG_ENDIAN	Endian Mode Selection DMA applies the endian rule to convert payload and Tx/Rx information. DMA does not apply the endian rule to the register or descriptor. 0: Little endian 1: Big endian	0x0
6	RW	TX_WB_DDONE	0: Disable TX_DMA writing back DDONE into TXD. 1: Enable TX_DMA writing back DDONE into TXD.	0x1
5	-	-	Reserved	0x0
4	RW	WPDMA_BT_SIZE	WPDMA Burst Size 0: 4 DWORD (16 bytes) 1: 8 DWORD (32 bytes)	0x1
3	RO	RX_DMA_BUSY	0: RX_DMA is not busy. 1: RX_DMA is busy.	0x0
2	RW	RX_DMA_EN	0: Disable RX_DMA. When disabled, RX_DMA finishes on the current Rx packet and then stops. 1: Enable RX_DMA.	0x0
1	RO	TX_DMA_BUSY	0: TX_DMA is not busy. 1: TX_DMA is busy.	0x0
0	RW	TX_DMA_EN	0: Disable TX_DMA. When disabled, TX_DMA finishes on the current Tx packet and then stops. 1: Enable TX_DMA.	0x0

PDMA_RST_IDX: (offset:0x1208)

Bits	Type	Name	Description	Initial value
31:18	-	-	Reserved	0x0
17	W1C	RST_DRX_IDX1	1: Reset RX_DMARX_IDX1 to '0'.	0x0
16	W1C	RST_DRX_IDX0	1: Reset RX_DMARX_IDX0 to '0'.	0x0
15:2	-	-	Reserved	0x0
1	W1C	RST_DTX_IDX1	1:Reset TX_DMATX_IDX1 to '0'.	0x0
0	W1C	RST_DTX_IDX0	1:Reset TX_DMATX_IDX0 to '0'.	0x0

DELAY_INT_CFG: (offset: 0x120c)

Bits	Type	Name	Description	Initial value
31	RW	TXDLY_INT_EN	0: Disable Tx delayed interrupt mechanism. 1: Enable Tx delayed interrupt mechanism.	0x0
30:24	RW	TXMAX_PINT	Maximum Number of Pended Interrupts When the number of pended interrupts is equal to or greater than the value specified here or the interrupt pended time is	0x0

			reached (see below), a final TX_DLY_INT is generated. 0: Disable the pended interrupt count check.	
23:16	RW	TXMAX_PTIME	Maximum Pended Time for Internal TX_DONE_INT0-5 When the pended time is equal to or greater than TXMAX_PTIME x 20 us or the number of pended TX_DONE_INT0-5 is equal or greater than TXMAX_PINT (see above), a final TX_DLY_INT is generated. 0: Disable the pended interrupt time check.	0x0
15	RW	RXDLY_INT_EN	0: Disable the Rx delayed interrupt mechanism. 1: Enable the Rx delayed interrupt mechanism.	0x0
14:8	RW	RXMAX_PINT	Maximum Number of Pended Interrupts When the number of pended interrupts is equal to or greater than the value specified here or the interrupt pended time limit is reached (see below), a final RX_DLY_INT is generated. 0: Disable the pended interrupt count check.	0x0
7:0	RW	RXMAX_PTIME	Maximum Pended Time for Internal RX_DONE_INT When the pended time is equal to or greater than RXMAX_PTIME x 20 us, or the number of pended RX_DONE_INT is equal to or greater than RXMAX_PCNT (see above), a final RX_DLY_INT is generated. 0: Disable the pended interrupt time check.	0x0

FREEQ_THRES: (offset: 0x1210)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	0x0
3:0	RW	FreeQ_THRES	Blocks this interface when Rx descriptors reach this threshold.	0x2

INT_STATUS: (offset: 0x1220)

Bits	Type	Name	Description	Initial value
31	RW	RX_COHERENT	RX_DMA finds a data coherent event when checking the DDONE bit. Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
30	RW	RX_DLY_INT	WPDMA Rx Related Interrupt Summary 1: Clear the interrupt. Read to get the raw interrupt status.	0x0
29	RW	TX_COHERENT	TX_DMA finds a data coherent event when checking the DDONE bit. Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
28	RW	TX_DLY_INT	WPDMA Tx Related Interrupt Summary Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
27:18	-	-	Reserved	0x0
17	RW	RX_DONE_INT1	Rx Queue #1 Packet Receive Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
16	RW	RX_DONE_INT0	RX Queue #0 Packet Receive Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
15:2	-	-	Reserved	0x0
1	RW	TX_DONE_INT1	Tx Queue #1 Packet Transmit Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
0	RW	TX_DONE_INT0	Tx Queue #0 Packet Transmit Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0

INT_MASK: (offset:0x1228)

Bits	Type	Name	Description	Initial value
31	RW	RX_COHERENT_INT_MSK	RX_DMA Data Coherent Event Interrupt Enable 0: Disable the interrupt. 1: Enable the interrupt.	0x0
30	RW	RX_ DLY_INT_MSK	WPDMA Rx Related Interrupt Summary 0: Disable the interrupt. 1: Enable the interrupt.	0x0
29	RW	TX_COHERENT_INT_MSK	TX_DMA Data Coherent Event Interrupt Enable 0: Disable the interrupt. 1: Enable the interrupt.	0x0
28	RW	TX_DLY_INT_MSK	WPDMA Tx Related Interrupt Summary 0: Disable the interrupt. 1: Enable the interrupt.	0x0
27:18	-	-	Reserved	0x0
17	RW	RX_DONE_INT_MSK1	Rx Queue #1 Packet Receive Interrupt 0: Disable the interrupt. 1: Enable the interrupt.	0x0
16	RW	RX_DONE_INT_MSK0	Rx Queue #0 Packet Receive Interrupt 0: Disable the interrupt. 1: Enable the interrupt.	0x0
15:2	-	-	Reserved	0x0
1	RW	TX_DONE_INT_MSK1	Tx Queue #1 Packet Transmit Interrupt 0: Disable the interrupt. 1: Enable the interrupt.	0x0
0	RW	TX_DONE_INT_MSK0	Tx Queue #0 Packet Transmit Interrupt 0: Disable the interrupt. 1: Enable the interrupt.	0x0

PDMA_SCH: (offset: 0x1280)

Bits	Type	Name	Description	Initial value
31:26	-	-	Reserved	-
25:24	RW	SCH_MODE	Scheduling Mode 00: WRR 01: Strict priority, Q3 > Q2 > Q1 > Q0 10: Mixed mode, Q3 > WRR(Q2,Q1, Q0) 11: Mixed mode, Q3 > Q2 > WRR(Q1, Q0)	0x0
23:0	-	-	Reserved	-

PDMA_WRR: (offset: 0x1284)

Bits	Type	Name	Description	Initial value
31:15	-	-	Reserved	-
14:12	RW	SCH_WT_Q3	Scheduling Weight of Tx Q3	0x0
11	-	-	Reserved	-
10:8	RW	SCH_WT_Q2	Scheduling Weight of Tx Q2	0x0
7	-	-	Reserved	-
6:4	RW	SCH_WT_Q1	Scheduling Weight of Tx Q1	0x0
3	-	-	Reserved	-
2:0	RW	SCH_WT_Q0	Scheduling Weight of Tx Q0	0x0

3.19 Frame Engine

3.19.1 Features

- Supports 4 Tx descriptor rings and 2 Rx descriptor rings.
- Scatter/gather DMA
- Delayed interrupt
- Configurable 4/8 double-word burst length
- Configurable Tx/Rx flow control mechanism
- Frames separated to 2 Rx rings by priority tag or source port
- Rx checksum offload
- Tx/Rx counters for debugging

3.19.2 Block Diagram

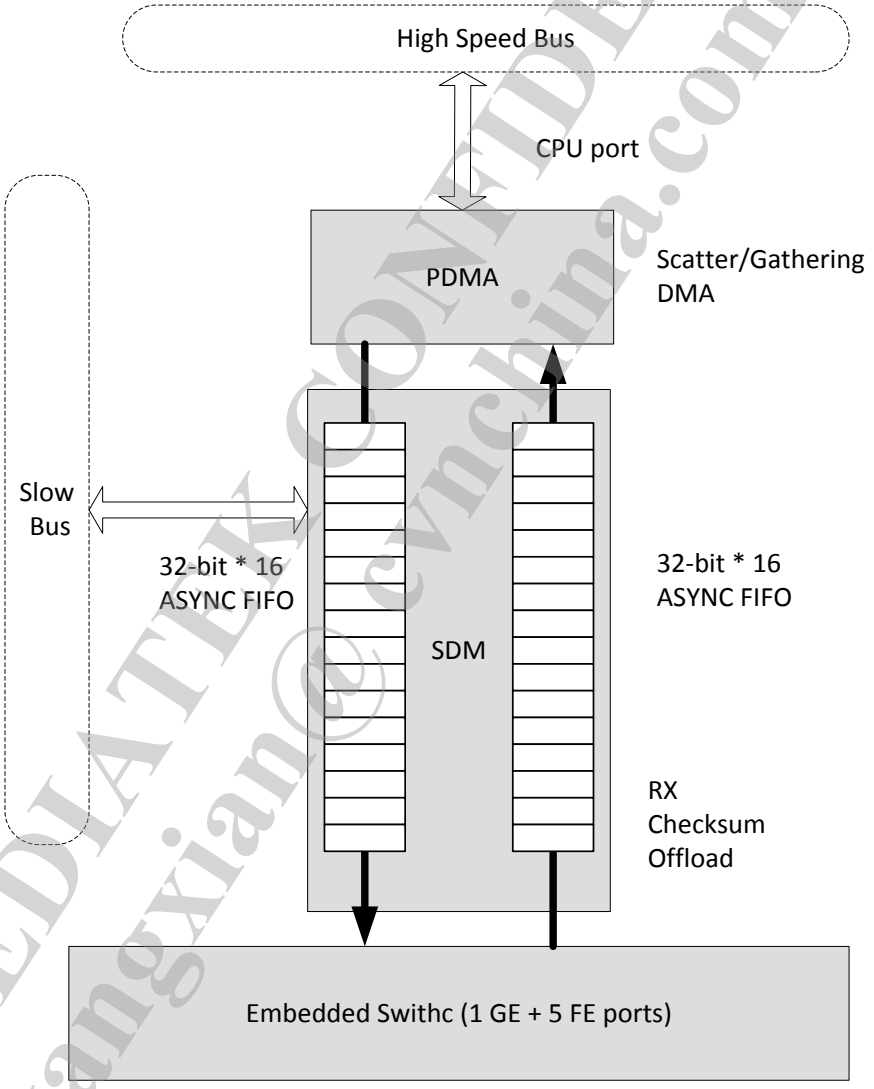
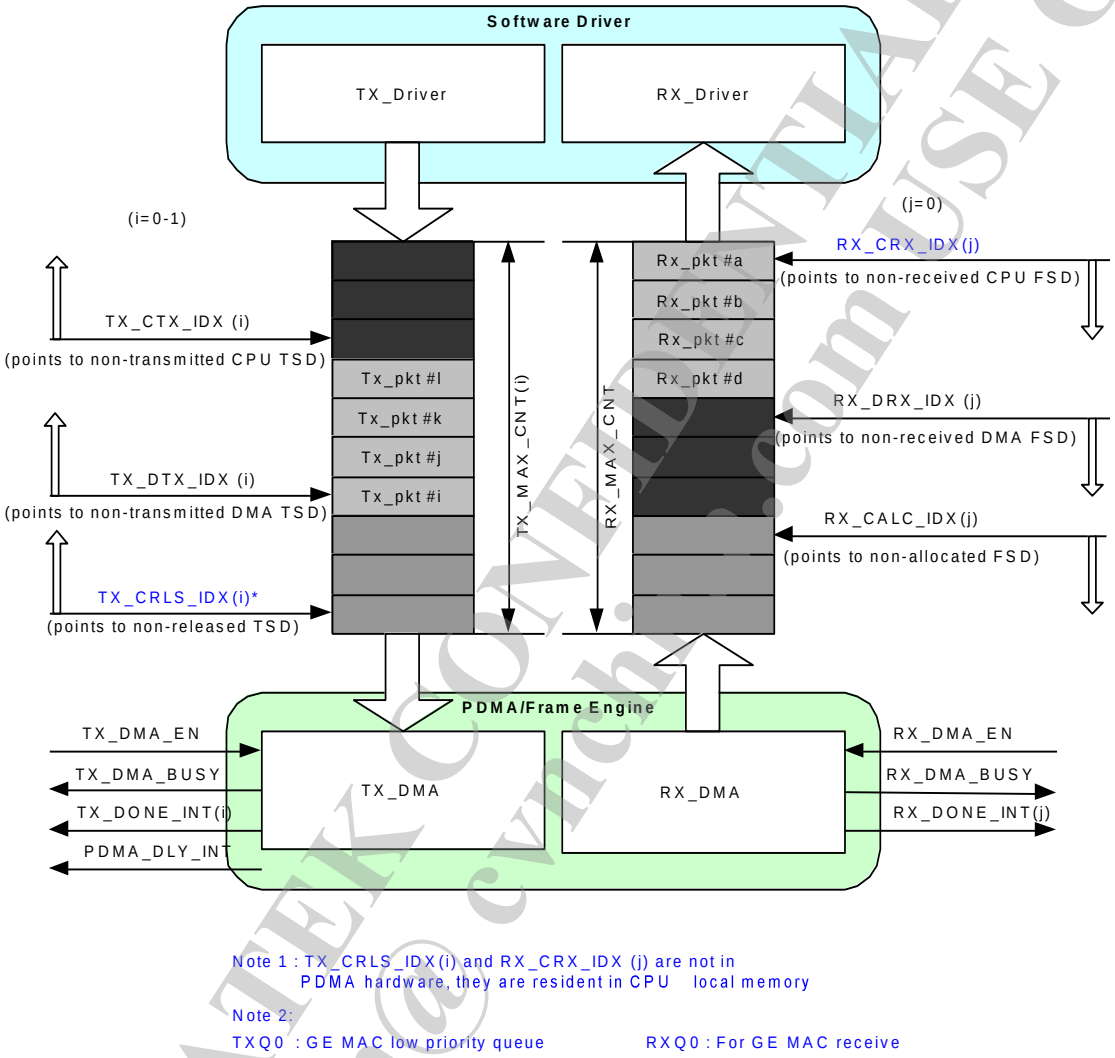


Figure 3-24 Frame Engine Block Diagram

3.19.2.1 PDMA FIFO-like Ring Concept



Note 1 : TX_CRLS_IDX(i) and RX_CRX_IDX (j) are not in PDMA hardware, they are resident in CPU local memory

Note 2:

TXQ0 : GE MAC low priority queue RXQ0 : For GE MAC receive

Figure 3-25 PDMA FIFO-like Ring Concept

3.19.2.2 PDMA Descriptor Format

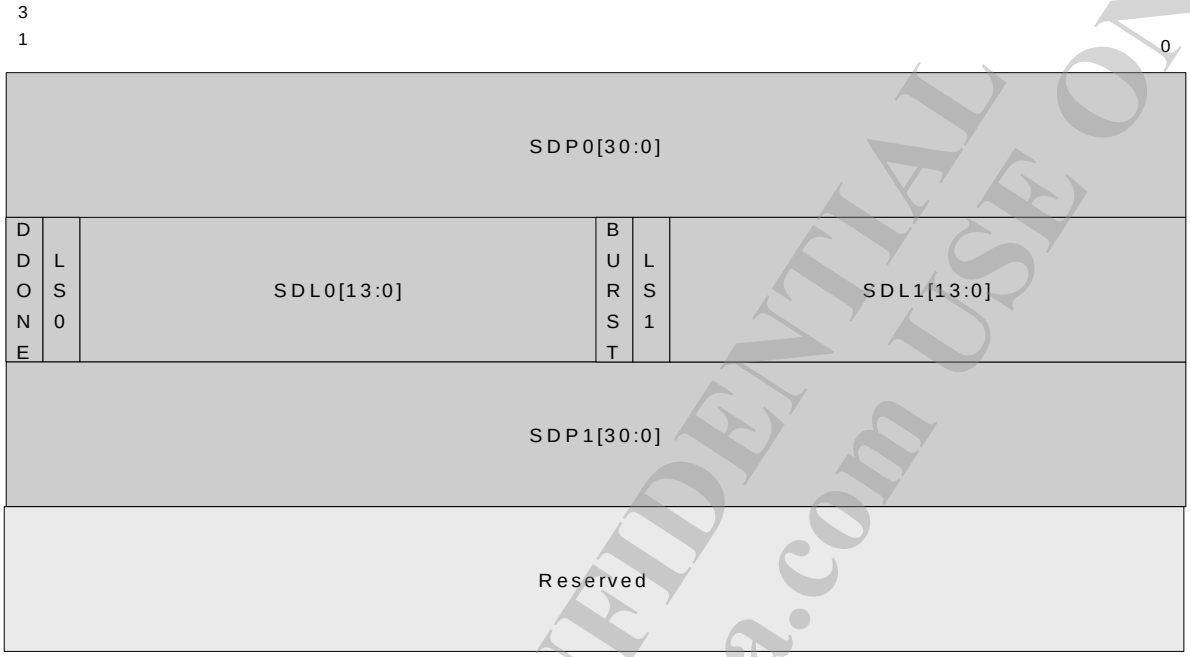


Figure 3-26 PDMA Tx Descriptor Format

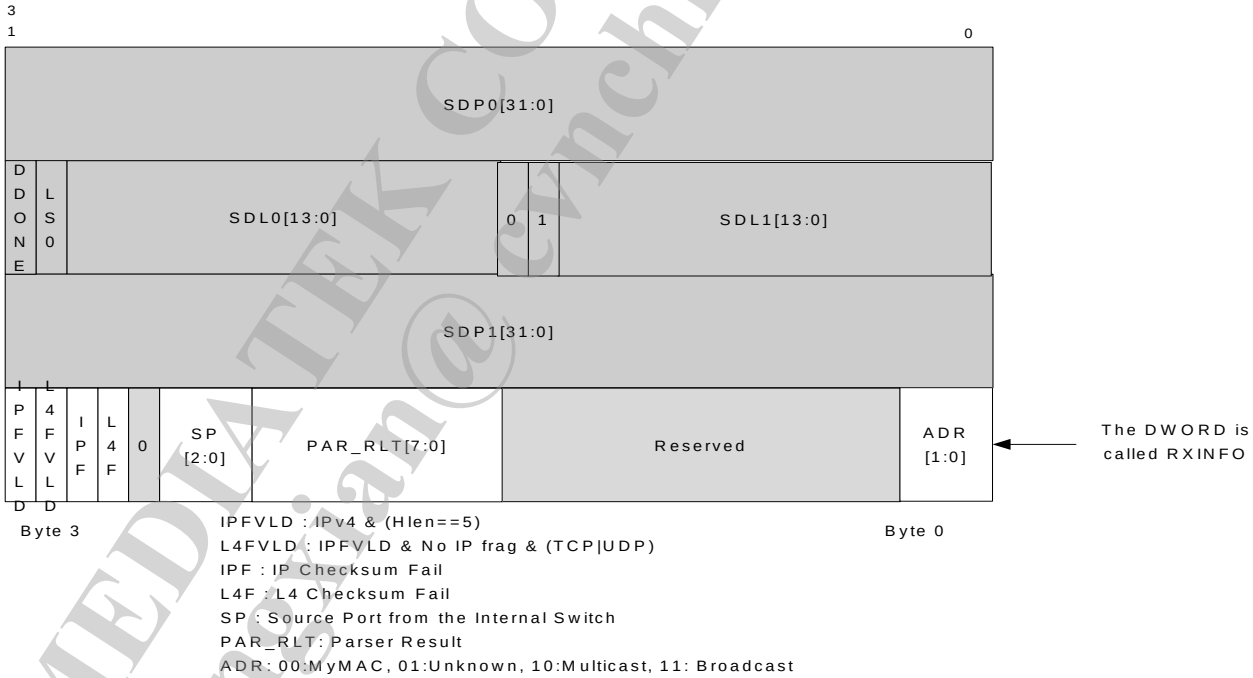


Figure 3-27 PDMA Rx Descriptor Format

3.19.3 PDMA Register Description (base: 0x1010_0800)

TX_BASE_PTRn: (offset: 0x0000, 0x0010, 0x0020, 0x0030)(n: 0~3)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	-
15:0	RW	TX_BASE_PTR	Points to the base address of TX_Ring0 (4-DWORD aligned address).	0x0

TX_MAX_CNTn: (offset: 0x0004, 0x0014, 0x0024, 0x0034)(n: 0~3)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	-
7:0	RW	TX_MAX_CNT	The maximum number of TXD count in TXD_Ring0.	0x0

TX_CTX_IDXn: (offset:0x0008, 0x0018, 0x0028, 0x0038)(n: 0~3)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	-
7:0	RW	TX_CTX_IDX	Points to the next TXD that the CPU will use.	0x0

TX_DTX_IDXn: (offset: 0x000c, 0x001c, 0x002c, 0x003c)(n: 0~3)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	-
7:0	RO	TX_DTX_IDX	Points to the next TXD that the DMA will use.	0x0

RX_BASE_PTRn: (offset: 0x0100, 0x0110)(n: 0~1)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	-
15:0	RW	RX_BASE_PTR	Points to the base address of RXD Ring #0 (GE ports). It should be a 4-DWORD aligned address.	0x0

RX_MAX_CNTn: (offset: 0x0104, 0x0114)(n: 0~1)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	-
7:0	RW	RX_MAX_CNT	The maximum RXD count in the RXD ring #0.	0x0

RX_CALC_IDXn: (offset: 0x0108, 0x0118)(n: 0~1)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	-
7:0	RW	RX_CALC_IDX0	Points to the next RXD that the CPU allocates to RXD Ring #0.	0x0

RX_DRX_IDXn: (offset: 0x010c, 0x011c)(n: 0~1)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	-
7:0	RW	RX_DRX_IDX0	Points to the next RXD that the DMA will use in RXD Ring #0. It should be a 4-DWORD aligned address.	0x0

PDMA_INFO: (offset: 0x0200)

Bits	Type	Name	Description	Initial value
31:28	RO	VERSION	PDMA Controller Version	0x1
27:24	RO	INDEX_WIDTH	Ring Index Width	0xC
23:16	RO	BASE_PTR_WIDTH	Base Pointer Width, x Base_addr[31:32-x] is shared with all ring base addresses. Only Ring 0's base address [31:32-x] field is writable. NOTE: '0'means no bit in the base_address is shared.	0x0
15:8	RO	RX_RING_NUM	Rx Ring Number	0x2
7:0	RO	TX_RING_NUM	Tx Ring Number	0x4

PDMA_GLO_CFG: (offset: 0x0204)

Bits	Type	Name	Description	Initial value
31:29	-	-	Reserved	-
28:16	RW	HDR_SEG_LEN	Specifies the header segment size in bytes to support the Rx header/payload scattering function, when set to a non-'0' value. When set to '0', the header/payload scattering feature is disabled.	0x0
15:8	-	-	Reserved	-
7	RW	BIG_ENDIAN	Endian Mode Selection DMA applies the endian rule to convert payload and Tx/Rx information. DMA does not apply the endian rule to the register or descriptor. 0: Little endian 1: Big endian	0x0
6	RW	TX_WB_DDONE	0: Disable TX_DMA writing back DDONE into TXD. 1: Enable TX_DMA writing back DDONE into TXD.	0x1
5	-	-	Reserved	-
4	RW	WPDMA_BT_SIZE	WPDMA Burst Size 0: 4 DWORD (16 bytes) 1: 8 DWORD (32 bytes)	0x1
3	RO	RX_DMA_BUSY	0: RX_DMA is not busy. 1: RX_DMA is busy.	0x0
2	RW	RX_DMA_EN	0: Disable RX_DMA. When disabled, RX_DMA finishes receiving the current packet and then stops. 1: Enable RX_DMA.	0x0
1	RO	TX_DMA_BUSY	0: TX_DMA is not busy. 1: TX_DMA is busy.	0x0
0	RW	TX_DMA_EN	0: Disable TX_DMA. When disabled, TX_DMA finishes the sending the current packet and then stops. 1: Enable TX_DMA.	0x0

PDMA_RST_IDX: (offset: 0x0208)

Bits	Type	Name	Description	Initial value
31:18	-	-	Reserved	-
17	W1C	RST_DRX_IDX1	1: Reset RX_DMARX_IDX1 to '0'.	0x0
16	W1C	RST_DRX_IDX0	1: Reset RX_DMARX_IDX0 to '0'.	0x0
15:4	-	-	Reserved	-
3	W1C	RST_DTX_IDX3	1: Reset TX_DMATX_IDX3 to '0'.	0x0
2	W1C	RST_DTX_IDX2	1: Reset TX_DMATX_IDX2 to '0'.	0x0
1	W1C	RST_DTX_IDX1	1: Reset TX_DMATX_IDX1 to '0'.	0x0
0	W1C	RST_DTX_IDX0	1: Reset TX_DMATX_IDX0 to '0'.	0x0

DELAY_INT_CFG: (offset: 0x020c)

Bits	Type	Name	Description	Initial value
31	RW	TXDLY_INT_EN	0: Disable Tx delayed interrupt mechanism. 1: Enable Tx delayed interrupt mechanism.	0x0
30:24	RW	TXMAX_PINT	Maximum Number of Pended Interrupts When the number of pended interrupts is equal to or greater than the value specified here or the interrupt pended time limit is reached (see below), a final TX_DLY_INT is generated. 0: Disable the pended interrupt count check.	0x0
23:16	RW	TXMAX_PTIME	Maximum Pended Time for Internal TX_DONE_INT0-5.	0x0

			When the pended time is equal to or greater than TXMAX_PTIME x 20 us or the number of pended TX_DONE_INT0-5 is equal to or greater than TXMAX_PINT (see above), a final TX_DLY_INT is generated. 0: Disable the pended interrupt time check.	
15	RW	RXDLY_INT_EN	0: Disable Rx delayed interrupt mechanism. 1: Enable Rx delayed interrupt mechanism.	0x0
14:8	RW	RXMAX_PINT	Maximum Number of Pended Interrupts When the number of pended interrupts is equal to or greater than the value specified here or the interrupt pending time limit is reached (see below), a final RX_DLY_INT is generated. 0: Disable the pending interrupt count check.	0x0
7:0	RW	RXMAX_PTIME	Maximum Pended Time for Internal RX_DONE_INT. When the pended time is equal to or greater than RXMAX_PTIME x 20 us, or the number of pended RX_DONE_INT is equal to or greater than RXMAX_PCNT (see above), a final RX_DLY_INT is generated. 0: Disable the pended interrupt time check.	0x0

FREEQ_THRES: (offset: 0x0210)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	-
3:0	RW	FreeQ_THRES	Blocks the interface when Rx descriptors reach this threshold.	0x2

INT_STATUS: (offset: 0x0220)

Bits	Type	Name	Description	Initial value
31	RW	RX_COHERENT	RX_DMA finds a data coherent event when checking the DDONE bit. Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
30	RW	RX_DLY_INT	WPDMA Rx Related Interrupts Summary Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
29	RW	TX_COHERENT	TX_DMA finds a data coherent event when checking the DDONE bit. Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
28	RW	TX_DLY_INT	WPDMA Tx Related Interrupt Summary Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
27:18	-	-	Reserved	-
17	RW	RX_DONE_INT1	Rx Queue #1 Packet Receive Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
16	RW	RX_DONE_INT0	Rx Queue #0 Packet Receive Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
15:4	-	-	Reserved	-
3	RW	TX_DONE_INT3	Tx Queue #3 Packet Transmit Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0

2	RW	TX_DONE_INT2	Tx Queue #2 Packet Transmit Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
1	RW	TX_DONE_INT1	Tx Queue #1 Packet Transmit Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
0	RW	TX_DONE_INT0	Tx Queue #0 Packet Transmit Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0

INT_MASK: (offset: 0x0228)

Bits	Type	Name	Description	Initial value
31	RW	RX_COHERENT_INT_MSK	RX_DMA Data Coherent Event Interrupt Enable 0: Disable the interrupt. 1: Enable the interrupt.	0x0
30	RW	RX_ DLY_INT_MSK	WPDMA Rx Related Interrupt Summary 0: Disable the interrupt. 1: Enable the interrupt.	0x0
29	RW	TX_COHERENT_INT_MSK	TX_DMA Data Coherent Events Interrupt Enable 0: Disable the interrupt. 1: Enable the interrupt.	0x0
28	RW	TX_DLY_INT_MSK	WPDMA Tx Related Interrupts Summary 0: Disable the interrupt. 1: Enable the interrupt.	0x0
27:18	-	-	Reserved	-
17	RW	RX_DONE_INT_MSK1	Rx Queue #1 Packet Receive Interrupt 0: Disable the interrupt. 1: Enable the interrupt.	0x0
16	RW	RX_DONE_INT_MSK0	Rx Queue #0 Packet Receive Interrupt 0: Disable the interrupt. 1: Enable the interrupt.	0x0
15:2	-	-	Reserved	-
3	RW	TX_DONE_INT_MSK3	Tx Queue #3 Packet Receive Interrupt 0: Disable the interrupt. 1: Enable the interrupt.	0x0
2	RW	TX_DONE_INT_MSK2	Tx Queue #2 Packet Receive Interrupt 0: Disable the interrupt. 1: Enable the interrupt.	0x0
1	RW	TX_DONE_INT_MSK1	Tx Queue #1 Packet Receive Interrupt 0: Disable the interrupt. 1: Enable the interrupt.	0x0
0	RW	TX_DONE_INT_MSK0	Tx Queue #0 Packet Receive Interrupt 0: Disable the interrupt. 1: Enable the interrupt.	0x0

PDMA_SCH: (offset: 0x0280)

Bits	Type	Name	Description	Initial value
31:26	-	-	Reserved	-
25:24	RW	SCH_MODE	Scheduling Mode 00: WRR 01: Strict priority, Q3 > Q2 > Q1 > Q0 10: Mixed mode, Q3 > WRR(Q2,Q1, Q0) 11: Mixed mode, Q3 > Q2 > WRR(Q1, Q0)	0x0
23:0	-	-	Reserved	-

PDMA_WRR: (offset: 0x0284)

Bits	Type	Name	Description	Initial value
31:15	-	-	Reserved	-
14:12	RW	SCH_WT_Q3	Scheduling Weight of Tx Q3	0x0
11	-	-	Reserved	-
10:8	RW	SCH_WT_Q2	Scheduling Weight of Tx Q2	0x0
7	-	-	Reserved	-
6:4	RW	SCH_WT_Q1	Scheduling Weight of Tx Q1	0x0
3	-	-	Reserved	-
2:0	RW	SCH_WT_Q0	Scheduling weight of Tx Q0	0x0

3.19.4 SDM Register Description (base: 0x1010_0c00)

SDM_CON: Switch DMA Configuration Register (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23	RW	PDMA_FC	Tx PDMA Flow Control Enable When this bit is set, the downstream flow-control is enabled on the PDMA 4 Tx ring (SDM_TRING). 0: Disable 1: Enable	0x0
22	RW	PORT_MAP	Rx Ring Selection The received frame is collected into the corresponding PDMA Rx ring based on the source port or priority tag. 0: Priority tag (SDM_RRING[7:0]) 1: Source port (SDM_RRING[12:8])	0x0
21	RW	LOOP_EN	Frame Engine Loopback Mode Enable When this bit is set, the received frame by the frame engine is forwarded directly to the internal switch without modification.	0x0
20	RW	TCI_81XX	Special Tag Recognition Enable When this bit is set, PID(0x8100) is recognized by the first byte (0x81) only. The second byte may be used for special purposes such as the incoming source port.	0x0
19	RW	UN_DROR_EN	Drop Unknown MAC Addresses 0: Disable 1: Enable	0x0
18	RW	UDPCS	UDP Packet Checksum Rx Offload Enable 0: Disable- the checksum result is showed on the Rx descriptor. 1: Enable- the checksum error packet is dropped.	0x1
17	RW	TCPCS	TCP Packet Checksum Rx Offload Enable 0: Disable- the checksum result is shown on the Rx descriptor. 1: Enable- the checksum error packet is dropped.	0x1
16	RW	IPCS	IP Header Checksum Rx Offload Enable 0: Disable- the checksum result is shown on the Rx descriptor. 1: Enable- the checksum error packet is dropped.	0x1
15:0	RW	EXT_VLAN	Outer VLAN Protocol ID The specific value is used to recognize the outer VLAN protocol ID only. For both the inner VLAN or the general VLAN-tagged frame, the value PID=0x8100 is the unique Protocol ID.	0x8100

SDM_RRING: Switch DMA Rx Ring Register (offset: 0x0004)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	-
19	RW	QUE3_RING_FC	Pauses switch queue 3 according to the Rx ring number. When the Rx ring number reaches the reserved free threshold	0x0

			(FREEQ_THRES), queue 3 to the CPU is paused. 0: Rx ring #0 1: Rx ring #1	
18	RW	QUE2_RING_FC	Pauses switch queue 2 according to the Rx ring number. 0: Rx ring #0 1: Rx ring #1	0x0
17	RW	QUE1_RING_FC	Pauses switch queue 1 according to the Rx ring number. 0: Rx ring #0 1: Rx ring #1	0x0
16	RW	QUE0_RING_FC	Pauses switch queue 0 according to the Rx ring number. 0: Rx ring #0 1: Rx ring #1	0x0
15:13	-	-	Reserved	-
12	RW	PORT4_RING	Frames received from source port 4 are sent to the specified Rx ring number. NOTE: To use the source port, the special tag between FE and SW should be enabled. 0: Rx ring #0 1: Rx ring #1	0x0
11	RW	PORT3_RING	Frames received from source port 3 are sent to the specified Rx ring number. 0: Rx ring #0 1: Rx ring #1	0x0
10	RW	PORT2_RING	Frames received from source port 2 are sent to the specified Rx ring number. 0: Rx ring #0 1: Rx ring #1	0x0
9	RW	PORT1_RING	Frames received from source port 1 are sent to the specified Rx ring number. 0: Rx ring #0 1: Rx ring #1	0x0
8	RW	PORT0_RING	Frames received from source port 1 are sent to the specified Rx ring number. 0: Rx ring #0 1: Rx ring #1	0x0
7	RW	PRI7_RING	Frames received with priority tag 7 are sent to the specified Rx ring number. 0: Rx ring #0 1: Rx ring #1	0x0
6	RW	PRI6_RING	Frames received with priority tag 6 are sent to the specified Rx ring number. 0: Rx ring #0 1: Rx ring #1	0x0
5	RW	PRI5_RING	Frames received with priority tag 5 are sent to the specified Rx ring number. 0: Rx ring #0 1: Rx ring #1	0x0
4	RW	PRI4_RING	Frames received with priority tag 4 are sent to the specified Rx ring number. 0: Rx ring #0 1: Rx ring #1	0x0
3	RW	PRI3_RING	Frames received with priority tag 3 are sent to the specified Rx ring number. 0: Rx ring #0	0x0

			1: Rx ring #1	
2	RW	PRI2_RING	Frames received with priority tag 2 are sent to the specified Rx ring number. 0: Rx ring #0 1: Rx ring #1	0x0
1	RW	PRI1_RING	Frames received with priority tag 1 are sent to the specified Rx ring number. 0: Rx ring #0 1: Rx ring #1	0x0
0	RW	PRI0_RING	Frames received with priority tag 0 are sent to the specified Rx ring number. 0: Rx ring #0 1: Rx ring #1	0x0

SDM_TRING: Switch DMA Tx Ring Register (offset: 0x0008)

Bits	Type	Name	Description	Initial value
31:28	RW	RING3_WAN_FC	WAN Port Tx Ring 3 Pause Tx ring 3 is paused when the specified switch egress queue on the WAN port is congested. Bit 0: WAN port queue #0 Bit 1: WAN port queue #1 Bit 2: WAN port queue #2 Bit 3: WAN port queue #3	0x0
27:24	RW	RING2_WAN_FC	WAN Port Tx Ring 2 Pause Tx ring 2 is paused when the specified switch egress queue on the WAN port is congested. Bit 0: WAN port queue #0 Bit 1: WAN port queue #1 Bit 2: WAN port queue #2 Bit 3: WAN port queue #3	0x0
23:20	RW	RING1_WAN_FC	WAN Port TX Ring 1 Pause Tx ring 1 is paused when the specified switch egress queue on the WAN port is congested. Bit 0: WAN port queue #0 Bit 1: WAN port queue #1 Bit 2: WAN port queue #2 Bit 3: WAN port queue #3	0x0
19:16	RW	RING0_WAN_FC	WAN Port TX Ring 0 Pause Tx ring 0 is paused when the specified switch egress queue on the WAN port is congested. Bit 0: WAN port queue #0 Bit 1: WAN port queue #1 Bit 2: WAN port queue #2 Bit 3: WAN port queue #3	0x0
15:12	RW	RING3_LAN_FC	LAN Port Tx Ring 3 Pause Tx ring 3 is paused when the specified switch egress queue on the LAN port is congested. Bit 0: LAN port queue #0 Bit 1: LAN port queue #1 Bit 2: LAN port queue #2 Bit 3: LAN port queue #3	0x0
11:8	RW	RING2_LAN_FC	LAN Port Tx Ring 2 Pause Tx ring 2 is paused when the specified switch egress queue on the LAN port is congested. Bit 0: LAN port queue #0	0x0

			Bit 1: LAN port queue #1 Bit 2: LAN port queue #2 Bit 3: LAN port queue #3	
7:4	RW	RING1_LAN_FC	LAN Port Tx Ring 1 Pause The Tx ring 1 is paused when the specified switch egress queue on the LAN port is congested. Bit 0: LAN port queue #0 Bit 1: LAN port queue #1 Bit 2: LAN port queue #2 Bit 3: LAN port queue #3	0x0
3:0	RW	RING0_LAN_FC	Tx Ring 0 LAN Port Pause Tx ring 0 is paused when the specified switch egress queue on the LAN port is congested. Bit 0: LAN port queue #0 Bit 1: LAN port queue #1 Bit 2: LAN port queue #2 Bit 3: LAN port queue #3	0x0

SDM_MAC_ADRL: Switch MAC Address LSB Register (offset: 0x000c)

Bits	Type	Name	Description	Initial value
31:0	RW	MY_MAC_L	MAC Address bit 31 – bit 0	0x0

SDM_MAC_ADRH: Switch MAC Address MSB Register (offset: 0x0010)

Bits	Type	Name	Description	Initial value
31:16	-	RES	Reserved	-
15:0	RW	MY_MAC_H	MAC Address bit 47 – bit 32	0x0

SDM_TPCNT: Switch DMA TX Packet Counter (offset: 0x0100)

Bits	Type	Name	Description	Initial value
31:0	RC	TX_PCNT	Transmit Packet Count Counts the packets transmitted from the frame engine to the switch.	0x0

SDM_TBCNT: Switch DMA Tx Byte Counter (offset: 0x0104)

Bits	Type	Name	Description	Initial value
31:0	RC	TX_BCNT	Transmit Byte Count Counts the bytes transmitted from the frame engine to the switch transmit byte count	0x0

SDM_RPCNT: Switch DMA Rx Packet Counter(offset: 0x0108)

Bits	Type	Name	Description	Initial value
31:0	RC	RX_PCNT	Receive Packet Count Counts the packets received by the frame engine from the switch.	0x0

SDM_RBCNT: Switch DMA Rx Byte Counter (offset: 0x010c)

Bits	Type	Name	Description	Initial value
31:0	RC	RX_BCNT	Receive Byte Count Counts the bytes received by the frame engine from the switch.	0x0

SDM_CS_ERR: Switch DMA Rx Checksum Error Counter (offset: 0x0110)

Bits	Type	Name	Description	Initial value
31:0	RC	TX_PCNT	Receive Checksum Error Count Counts the checksum errors received by the frame engine.	0x0

3.20 Ethernet Switch

3.20.1 Features

- Supports IEEE 802.3 full duplex flow control.
- 5 10/100 Mbps PHY
- Supports spanning tree port states
- Supports 1K MAC address table with direct or XOR hash.
- QoS
  - Four priority queues per port
  - Packet classification based on incoming port, IEEE 802.1p, or IP ToS/DSCP.
  - Strict-priority queue (PQ) and weighted round robin (WRR)
- VLAN
  - Port based VLAN
  - Double VLAN tagging
  - 802.1q tag VLAN
  - 16 VIDs
- Read/writeable MAC address table
- MAC security – port/MAC address binding
- MAC clone support – hash with VID
- IGMP and MLD support
- Per-port broadcast storm prevention
- IGMPv1/v2, MLDv1 support
- Support Ingress Rate Limit by FC or drop
- Support Egress Rate Limit

NOTE: The RT5350 does not support a port 5 Gigabit MAC. The corresponding port 5 registers are reserved and invalid.

3.20.2 Block Diagram

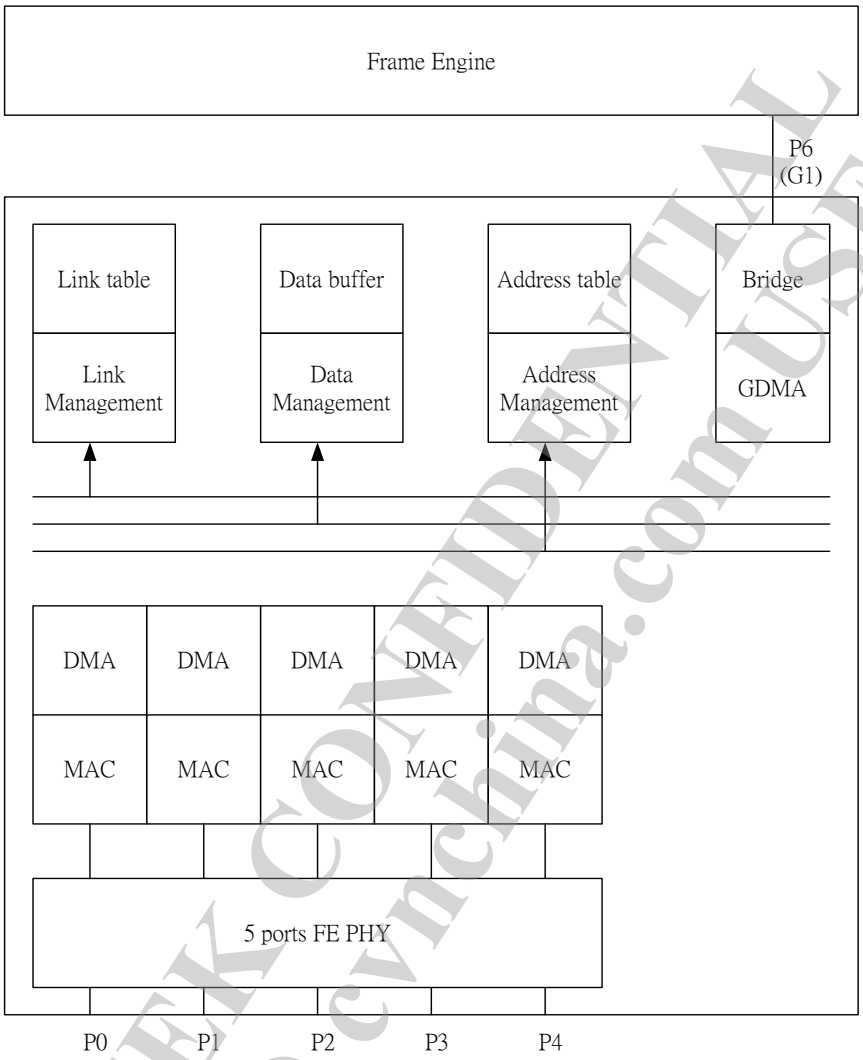


Figure 3-28 Ethernet Switch Block Diagram

3.20.3 Frame Classification

3-11 Reserved Multicast Address Frames

FTAG	DA	Type	IPv4/IPv6 Protocol	Description
BC	FF-FF-FF-FF-FF-FF	-	-	Broadcast frames
MC	Bit.40=1'b1	-	-	Multicast frames
IGMP	01-00-5E-xx-xx-xx	08-00	0x02	IGMP message packet
IP_MULT	01-00-5E-xx-xx-xx	-		IP multicast frames
MLD	33-33-xx-xx-xx-xx	86-DD	0x00 (Hop_by_Hop) 0x3A (ICMPv6)	MLD/ICMPv6 message packet
IPV6_MULT	33-33-xx-xx-xx-xx	-		IPv6 multicast frames
PAUSE	-	88-08	-	Discarded
	01-80-C2-00-00-01 Or Unicast DA	88-08	Followed by 00-01	MAC control pause frame (< 1518 bytes) Discarded
RMC	01-80-C2-00-00-00	-	-	BPDU
	01-80-C2-00-00-02 ~ 01-80-c2-00-00-xx			Reserved group/multicast frames

3.20.4 Register Description (base: 0x1011_0000)

NOTE: In RT5350, the registers related to P5 (port 5) are not applicable. Please keep them as default settings.

ISR: Interrupt Status Register (offset: 0x0000)

Bits	Type	Name	Description	Initial value
31	RO	PKT_CNT_	Packet Counter Interrupt Status Indicator This bit indicates a change in the packet counter interrupt status (PCIS offset: 0x14C). To clear this bit, write '1' to the PCRI register.	0x0
30	-	-	Reserved	0x0
29	RW	WATCHDOG1_TMR_ EXPIRED	P5 No Packets Transmitted Alert This bit indicates that P5 has not transmitted a packet for 3 seconds when P5 needs to transmit a packet. 1: Clear this bit. NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
28	RW	WATCHDOG0_TMR_ EXPIRED	Abnormal Alert This bit indicates that the global queue block counts have been less than buf_starvation_th for three seconds. 1: Clear this bit.	0x0
27	RW	HAS_INTRUDER	Intruder Alert This bit indicates that an unsecured packet is coming into a secured port. 1: Clear this bit.	0x0
26	RW	PORT_ST_CHG	Port Status Change Indicates a change in the status of a port. 1: Clear this bit.	0x0
25	RW	BC_STORM	BC Storm The device is undergoing a broadcast storm. 1: Clear this bit.	0x0
24	RW	MUST_DROP_LAN	Queue Exhausted The global queue is used up and all packets are dropped. Write '1' to clear this bit.	0x0
23	RW	GLOBAL_QUE_ FULL	Global Queue Full 1: Clear this bit.	0x0
22:21	-	-	Reserved	-
20	RW	LAN_QUE_FULL[6]	Port 6 out queue is full. 1: Clear this bit.	0x0
19	RW	LAN_QUE_FULL[5]	Port 5 out queue is full. 1: Clear this bit. NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
18	RW	LAN_QUE_FULL[4]	Port 4 out queue is full. 1: Clear this bit.	0x0
17	RW	LAN_QUE_FULL[3]	Port 3 out queue is full. 1: Clear this bit.	0x0
16	RW	LAN_QUE_FULL[2]	Port 2 out queue is full. 1: Clear this bit.	0x0
15	RW	LAN_QUE_FULL[1]	Port 1 out queue is full. 1: Clear this bit.	0x0
14	RW	LAN_QUE_FULL[0]	Port 0 out queue is full. 1: Clear this bit.	0x0
13:0	-	-	Reserved	0x0

IMR: Interrupt Mask Register (offset: 0x0004)

Bits	Type	Name	Description	Initial value
31	RW	PKT_CNT_MASK_31	Packet Counter Recycle Interrupt Mask Iindicates that any status change of the packet counter interrupt status (PCIS offset: 0x14C).	0x1
30	-	-	Reserved	-
29	RW	SW_INT_MASK_29	P5 No Packets Transmitted Alert Indicates that P5 has not transmitted a packet for 3 seconds when P5 needs to transmit a packet. NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x1
28	RW	SW_INT_MASK_28	Abnormal Alert Indicates that the global queue block counts have been less than buf_starvation_th for three seconds.	0x1
27	RW	SW_INT_MASK_27	Intruder Alert Indicates that an unsecured packet is coming into a secured port.	0x1
26	RW	SW_INT_MASK_26	Port Status Change Indicates a change in the status of a port.	0x1
25	RW	SW_INT_MASK_25	BC Storm The device is undergoing a broadcast storm.	0x1
24	RW	SW_INT_MASK_24	Queue Exhausted The global queue is used up and all packets are dropped.	0x1
23	RW	SW_INT_MASK_23	The shared queue is full.	0x1
22:21	-	-	Reserved	-
20	RW	SW_INT_MASK_20	Port 6 queue is full.	0x1
19	RW	SW_INT_MASK_19	Port 5 queue is full. NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x1
18	RW	SW_INT_MASK_18	Port 4 queue is full.	0x1
17	RW	SW_INT_MASK_17	Port 3 queue is full.	0x1
16	RW	SW_INT_MASK_16	Port 2 queue is full.	0x1
15	RW	SW_INT_MASK_15	Port 1 queue is full.	0x1
14	RW	SW_INT_MASK_14	Port 0 queue is full.	0x1
13:0	-	-	Reserved	-

FCT0: Flow Control Threshold 0 (offset: 0x0008)

Bits	Type	Name	Description	Initial value
31:24	RW	FC_RLS_TH	Flow Control Release Threshold Flow control is disabled when the global queue block counts are greater than the release threshold.	0xFF
23:16	RW	FC_SET_TH	Flow Control Set Threshold Flow control is enabled when the global queue block counts are less than the set threshold.	0xC8
15:8	RW	DROP_RLS_TH	Drop Release **T**hreshold The switch stops dropping packets when the global queue block counts are greater than the drop-release threshold.	0x6E
7:0	RW	DROP_SET_TH	Drop **S**et **T**hreshold The switch starts dropping packets when the global queue block counts are less than the drop-set threshold.	0x5A

FCT1: Flow Control Threshold 1 (offset: 0x000c)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	-
7:0	RW	PORT_TH	Per Port Output Threshold When the global queue reaches the flow control or drop threshold on register FCT0, the per port output threshold is checked to enable flow-control or packet-drop depending on the per queue minimum reserved blocks of the register PFC2.	0x14

PFC0: Priority Flow Control – 0 (offset: 0x0010)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	-
27:24	RW	MTCC_LMT	Maximum Back-off Count Limit After the limit is reached, collision packets are dropped.	0xF
23	-	-	Reserved	-
22:16	RW	TURN_OFF_FC	Turns off the FC when receiving highest priority packets. 0: Disable 1: Enable	0x0
15:12	RW	VO_NUM	The number (weighting) of voice packets to be sent before moving to the control load queue. Packet transmission by each queue is determined by weighted round robin scheduling. After transmitting the specified number of packets then proceed to next queue. [Note] If the number of VO_NUM is equal to zero, all queues are forced into strict priority mode and Voice queue has the highest priority. 0: All queues are forced to the strict priority mode.	0x0
11:8	RW	CL_NUM	The number of control load packets to be sent before moving to the best effort queue. Packet transmission by each queue is determined by weighted round robin scheduling. After transmitting the specified number of packets then proceed to next queue.	0x0
7:4	RW	BE_NUM	The number of best effort packets to be sent before moving to the background queue. Packet transmission by each queue is determined by weighted round robin scheduling. After transmitting the specified number of packets then proceed to next queue.	0x0
3:0	RW	BK_NUM	The number of background packets to be sent before moving to the voice queue. Packet transmission by each queue is determined by weighted round robin scheduling. After transmitting the specified number of packets then proceed to next queue.	0x0

PFC1: Priority Flow Control –1 (offset: 0x0014)

Bits	Type	Name	Description	Initial value
31	RW	CPU_USE_Q1_EN	Sets the CPU port to only use q1. 0: Default priority resolution 1: Packets forwarded to the CPU port use the best-effort queue.	0x0

30:24	RW	EN_TOS[7:0]	Enables ToS on Port 6 ~ port 0. Checks the ToS field in IP packet headers for priority resolution. 0: Disable 1: Enable NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x0
23	RW	IGMP_to_CPU	Enables IGMP forwarding to the CPU. 1'b0: IGMP message is flooded to all ports. 1'b1: IGMP message is forwarded to the CPU port only.	0x0
22:16	RW	EN_VLAN	Enables per port VLAN-tag VID membership and priority tag checking. 0: Disable 1: Enable NOTE: Port 5 function is only valid when the port 5 Gigabit MAC is implemented.	0x0
15	RW	PRIORITY_OPTION	Priority Resolution Option 0: 802.1p → TOS → Per port 1: TOS → 802.1p → Per port	0x0
14	-	-	Reserved	-
13:12	RW	PORT_PRI6	Port Priority Sets this register to assign default priority queue for each port.	0x1
11:10	RW	PORT_PRI5	Port Priority Sets this register to assign the default priority queue for each port. NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x1
9:8	RW	PORT_PRI4	Port Priority Sets this register to assign the default priority queue for each port.	0x1
7:6	RW	PORT_PRI3	Port Priority Sets this register to assign the default priority queue for each port.	0x1
5:4	RW	PORT_PRI2	Port Priority Sets this register to assign the default priority queue for each port.	0x1
3:2	RW	PORT_PRI1	Port Priority Sets this register to assign the default priority queue for each port.	0x1
1:0	RW	PORT_PRI0	Port Priority Sets this register to assign the default priority queue for each port.	0x1

PFC2: Priority Flow Control –2 (offset: 0x0018)

Bits	Type	Name	Description	Initial value
31:24	RW	PRI_TH_VO	Voice threshold – highest priority The minimum reserved packet block count which the output queue can store when the flow-control/drop threshold of registers FTC0 and FCT1 is reached. If the number of queued blocks exceeds the threshold, the incoming packet is paused or dropped.	0x3

23:16	RW	PRI_TH_CL	Control Load Threshold The minimum reserved packet block count which the output queue can store when the flow-control/drop threshold of registers FTC0 and FCT1 is reached. If the number of queued blocks exceeds the threshold, the incoming packet is paused or dropped.	0x3
15:8	RW	PRI_TH_BE	Best Effort Threshold The minimum reserved packet block count which the output queue can store when the flow-control/drop threshold of registers FTC0 and FCT1 is reached. If the number of queued blocks exceeds the threshold, the incoming packet is paused or dropped.	0x3
7:0	RW	PRI_TH_BK	Background Threshold – Lowest Priority The minimum reserved packet block count which the output queue can store when the flow-control/drop threshold of registers FTC0 and FCT1 is reached. If the number of queued blocks exceeds the threshold, the incoming packet is paused or dropped.	0x3

GQS0: Global Queue Status – 0 (offset: 0x001c)

Bits	Type	Name	Description	Initial value
31:30	RW	PRI7_QUE	Queue Mapping for Priority Tag #7	0x3
29:28	RW	PRI6_QUE	Queue Mapping for Priority Tag #6	0x3
27:26	RW	PRI5_QUE	Queue Mapping for Priority Tag #5	0x2
25:24	RW	PRI4_QUE	Queue Mapping for Priority Tag #4	0x2
23:22	RW	PRI3_QUE	Queue Mapping for Priority Tag #3	0x1
21:20	RW	PRI2_QUE	Queue Mapping for Priority Tag #2	0x0
19:18	RW	PRI1_QUE	Queue Mapping for Priority Tag #1	0x0
17:16	RW	PRI0_QUE	Queue Mapping for Priority Tag #0	0x1
15:9	-	-	Reserved	0x0
8:0	RO	EMPTY_CNT	Global Queue Block Counts This field indicates the number of block counts left in the global free queue.	0x16e

GQS1: Global Queue Status – 1 (offset: 0x0020)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	-
30:24	RO	OUTQUE_FULL_VO	Congested Voice Queue The corresponding queue is congested.	0x0
24	-	-	Reserved	-
23:16	RO	OUTQUE_FULL_CL	Congested Control Load Queue The corresponding queue is congested.	0x0
15	-	-	Reserved	-
14:8	RO	OUTQUE_FULL_BE	Congested Best Effort Queue The corresponding queue is congested.	0x0
7	-	-	Reserved	-
6:0	RO	OUTQUE_FULL_BK	Congested Background Queue The corresponding queue is congested.	0x0

ATS: Address Table Search (offset: 0x0024)

Bits	Type	Name	Description	Initial value
31:3	-	-	Reserved	0x0

2	RS	AT_LKUP_IDLE	Address Lookup Idle This field indicates that the address table engine is in an idle state.	0x0
1	RW	SEARCH_NXT_ADDR	Search for the Next Address (self_clear).	0x0
0	RW	BEGIN_SEARCH_ADDR	Start Searching the Address Table (self_clear).	0x0

ATS0: Address Table Status 0 (offset: 0x0028)

Bits	Type	Name	Description	Initial value
31:22	RO	HASH_ADD_LU	Address Table Lookup Address	0x0
21:19	-	-	Reserved	-
18:12	RO	R_PORT MAP	Port Map The MAC found at bit = 1.	0x0
11	-	-	Reserved	-
10:7	RO	R_VID	VLAN Index	0x0
6:4	RO	R_AGE_FIELD	Aging Field	0x0
3	-	-	Reserved	-
2	RO	R_MC_INGRESS	MC Ingress	0x0
1	RO	AT_TABLE_END	Indicates that the search has reached the end of the address table.	0x0
0	RO	SEARCH_RDY	Data is ready (read clear)	0x0

ATS1: Address Table Status 1 (offset: 0x002c)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	-
15:0	RO	MAC_AD_SER0	Read MAC Address [15:0]	0x0

ATS2: Address Table Status 2 (offset: 0x0030)

Bits	Type	Name	Description	Initial value
31:0	RO	MAC_AD_SER1	Read MAC Address [47:16]	0x0

WMAD0: WT_MAC_AD0 (offset: 0x0034)

Bits	Type	Name	Description	Initial value
31:22	RO	HASH_ADD_CFG	Address Table Configuration Address	0x0
21:19	-	-	Reserved	-
19	RO	AT_CFG_IDLE	Address Table Configuration SM Idle	0x1
18:12	RW	W_PORT_MAP	Write Port Bit-map	0x0
11	-	-	Reserved	-
10:7	RW	W_INDEX	Write VLAN index 0: VLAN 0 ~ 15: VLAN 15	0x0
6:4	RW	W_AGE_FIELD	Write Aging Field 111b : Static address 001b ~110b: The entry is valid and will be aged out. 000b : Default, entry is invalid.	0x0
3	RW	-SA_FILTER	SA_FILTER 0: Default 1: The corresponding packet is dropped when the SA is matched.	0x0
2	RW	W_MC_INGRESS	Write Mc_Ingress bit	0x0

1	RO	W_MAC_DONE	MAC Write Done 0: Default 1: MAC address write OK (read_clear).	0x0
0	RW	W_MAC_CMD	MAC Address Write Command 0: Default 1: Writes data set in the above commands to the MAC table. (self_clear).	0x0

WMAD1: WT_MAC_AD1 (offset: 0x0038)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:0	RW	W_MAC_15_0	Write MAC Address [15:0]	0x0

WMAD2: WT_MAC_AD2 (offset: 0x003c)

Bits	Type	Name	Description	Initial value
31:0	RW	W_MAC_47_16	Write MAC Address [47:16]	0x0

PVIDC0: PVID Configuration 0 (offset: 0x0040)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:12	RW	P1_PVID	Port 1 PVID Setting	0x1
11:0	RW	P0_PVID	Port 0 PVID Setting	0x1

PVIDC1: PVID Configuration 1 (offset: 0x0044)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:12	RW	P3_PVID	Port 3 PVID Setting	0x1
11:0	RW	P2_PVID	Port 2 PVID Setting	0x1

PVIDC2: PVID Configuration 2 (offset: 0x0048)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:12	RW	P5_PVID	Port 5 PVID Setting NOTE: This feature is only valid when the port 5 Gigabit MAC is implemented.	0x1
11:0	RW	P4_PVID	Port4 PVID Setting	0x1

PVIDC3: PVID Configuration 3 (offset: 0x004c)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	0x0
30:28	RW	QUE3_PRIT	Priority Tag Egress Mapping for Voice Queue #3	0x7
27	-	-	Reserved	0x0
26:24	RW	QUE2_PRIT	Priority Tag Egress Mapping for Control Load Queue #2	0x5
23	-	-	Reserved	0x0
22:20	RW	QUE1_PRIT	Priority Tag Egress Mapping for Best Effort Queue #1	0x0
19	-	-	Reserved	0x0
18:16	RW	QUE0_PRIT	Priority Tag Egress Mapping for Background Queue #0	0x2
15:12	-	-	Reserved	0x0
11:0	RW	P6_PVID	Port 6 PVID setting	0x1

VLANI0: VLAN Identifier 0 (offset: 0x0050)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:12	RW	VID1	VLAN Field Identifier for VLAN 1	0x2
11:0	RW	VID0	VLAN Field Identifier for VLAN 0	0x1

VLANI1: VLAN Identifier 1 (offset: 0x0054)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:12	RW	VID3	VLAN Field Identifier for VLAN 3	0x4
11:0	RW	VID2	VLAN Field Identifier for VLAN 2	0x3

VLANI2: VLAN Identifier 2 (offset: 0x0058)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:12	RW	VID5	VLAN Field Identifier for VLAN 5	0x6
11:0	RW	VID4	VLAN Field Identifier for VLAN 4	0x5

VLANI3: VLAN Identifier 3 (offset: 0x005c)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:12	RW	VID7	VLAN Field Identifier for VLAN 7	0x8
11:0	RW	VID6	VLAN Field Identifier for VLAN 6	0x7

VLANI4: VLAN Identifier 4 (offset: 0x0060)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:12	RW	VID9	VLAN Field Identifier for VLAN 9	0xA
11:0	RW	VID8	VLAN Field Identifier for VLAN 8	0x9

VLANI5: VLAN Identifier 5 (offset: 0x0064)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:12	RW	VID11	VLAN Field Identifier for VLAN 11	0xC
11:0	RW	VID10	VLAN Field Identifier for VLAN 10	0xB

VLANI6: VLAN Identifier 6 (offset: 0x0068)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0x0
23:12	RW	VID13	VLAN Field Identifier for VLAN 13	0xE
11:0	RW	VID12	VLAN Field Identifier for VLAN 12	0xD

VLANI7: VLAN Identifier 7 (offset: 0x006c)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0x0
23:12	RW	VID15	VLAN Identifier for VLAN 15	0x10
11:0	RW	VID14	VLAN Identifier for VLAN 14	0xF

VMSC0: VLAN Member Port Configuration 0 (offset: 0x0070)

Bits	Type	Name	Description	Initial value
30:24	RW	VLAN_MEMSET_3	VLAN 3 Member Port	0x7F
22:16	RW	VLAN_MEMSET _2	VLAN 2 Member Port	0x7F

15:8	RW	VLAN_MEMSET _1	VLAN 1 Member Port	0x7F
7:0	RW	VLAN_MEMSET _0	VLAN 0 Member Port	0x7F

VMSC1: VLAN Member Port Configuration 1 (offset: 0x0074)

Bits	Type	Name	Description	Initial value
30:24	RW	VLAN_MEMSET_7	VLAN 7 Member Port	0x7F
22:16	RW	VLAN_MEMSET _6	VLAN 6 Member Port	0x7F
15:8	RW	VLAN_MEMSET _5	VLAN 5 Member Port	0x7F
7:0	RW	VLAN_MEMSET _4	VLAN 4 Member Port	0x7F

VMSC2: VLAN Member Port Configuration 2 (offset: 0x0078)

Bits	Type	Name	Description	Initial value
30:24	RW	VLAN_MEMSET_11	VLAN 11 Member Port	0x7F
22:16	RW	VLAN_MEMSET _10	VLAN 10 Member Port	0x7F
15:8	RW	VLAN_MEMSET _9	VLAN 9 Member Port	0x7F
7:0	RW	VLAN_MEMSET _8	VLAN 8 Member Port	0x7F

VMSC3: VLAN Member Port Configuration 3 (offset: 0x007c)

Bits	Type	Name	Description	Initial value
30:24	RW	VLAN_MEMSET_15	VLAN 15 Member Port	0x7F
22:16	RW	VLAN_MEMSET _14	VLAN 14 Member Port	0x7F
15:8	RW	VLAN_MEMSET _13	VLAN 13 Member Port	0x7F
7:0	RW	VLAN_MEMSET _12	VLAN 12 Member Port	0x7F

POA: Port Ability (offset: 0x0080)

Bits	Type	Name	Description	Initial value
31	RO	G1_LINK	Port 6 Link Status 0: Link down 1: Link up	0x0
30	RO	G0_LINK	Port 5 Link Status 0: Link down 1: Link up NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
29:25	RO	LINK	Port 4 ~ Port 0 Link Status 0: Link down 1: Link up	0x0
24:23	RO	G1_XFC	Flow Control Status of Port 6 The flow control capability status bit after auto-negotiation or force mode. 00b: Flow control off 1xb: Full duplex and Tx flow control are enabled. x1b: Full duplex and Rx flow control are enabled.	0x0
22:21	RO	G0_XFC	Flow Control Status of Port 5 The flow control capability status bit after auto-negotiation or force mode. 00b: Flow control off 1xb: Full duplex and Tx flow control are enabled. x1b: Full duplex and Rx flow control are enabled. NOTE: This feature is only valid when the port 5 Gigabit MAC is implemented.	0x0

20:16	RO	XFC	Flow Control Status of Ports 0 ~ 4 The flow control capability status bit after auto-negotiation or force mode. 0: Flow control off 1: Full duplex and 802.3x flow control are enabled. (after AN or forced).	0x0
15:9	RO	DUPLEX	Port 6 ~ Port 0 Duplex Mode 0: Half duplex 1: Full duplex NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x0
8:7	RO	G1_SPD	MII Port 6 Speed Mode 00: 10 MHz 01: 100 MHz 10: 1 GHz	0x0
6:5	RO	G0_SPD	MII Port 5 Speed Mode 00: 10 MHz 01: 100 MHz 10: 1 GHz NOTE: This feature is only valid when the port 5 Gigabit MAC is implemented.	0x0
4:0	RO	SPEED	Port 4 ~ Port 0 Speed Mode 0: 10 MHz 1: 100 MHz	0x0

FPA: Force Port 4 ~ Port 0 Ability (offset: 0x0084)

Bits	Type	Name	Description	Initial value
31:27	RW	FORCE_MODE	Port 4 ~ Port 0 Force Mode 0: Default 1: Force mode. Auto-negotiation status is ignored. All port functions are forced according to the following fields of the register FPA.	0x0
26:22	RW	FORCE_LNK	Port 4 ~ Port 0 PHY Link This field is valid only when FORCE_MODE is set. The final resolution is reported to POA register. 0: Link down 1: Link up	0x0
21	-	-	Reserved	-
20:16	RW	FORCE_XFC	Port 4 ~ Port 0 Flow Control of the PHY Port This field is valid only when FORCE_MODE is set. The final resolution is reported to POA register. 0: Default OFF 1: 802.3x flow control ON	0x0
15:13	-	-	Reserved	-
12:8	RW	FORCE_DPX	Port 4 ~ Port 0 Duplex This field is valid only when FORCE_MODE is set. The final resolution is reported to POA register. 0: Half duplex 1: Full duplex	0x0
7:6	-	-	Reserved	-
5	RW	XTAL_COMP	Crystal Rate Compensation 0: Disable 1: When the switch has transmitted 20 000 bytes, the switch will compensate for the reduction in crystal rate.	0x0

4:0	RW	FORCE_SPD	Port 4 ~ Port 0 Speed This field is valid only when FORCE_MDOE is set. The final resolution is reported to POA register. 0: 10 MHz 1: 100 MHz	0x0

PTS: Port Status (offset: 0x0088)

Bits	Type	Name	Description	Initial value
31:10	-	-	Reserved	-
9	RO	G1_TXC_STATUS	Port 6 TXC status, 1 = error, no TXC	0x0
8	RO	G0_TXC_STATUS	Port 5 TXC status, 1 = error, no TXC NOTE: This feature is only valid when the port 5 Gigabit MAC is implemented.	0x0
7	-	-	Reserved	-
6:0	RO	SECURED_ST	Security Status 1: Indicates an illegal source address is detected when SA_secured mode is enabled (read_clear). NOTE: Port 5 function is only valid when the port 5 Gigabit MAC is implemented.	0x0

SOCPC: SoC Port Control (offset: 0x008c)

Bits	Type	Name	Description	Initial value
31:26	-	-	Reserved	-
25	RW	CRC_PADDING	CRC Padding From the CPU If this bit is set, all packets from the CPU do not need to append a CRC and the outgoing LAN/WAN port will calculate and append a CRC. 0: Packets from the CPU need CRC appending. 1: Packets from the CPU do not need CRC appending.	0x1
24:23	RW	CPU_SELECTION	CPU **S**election 00b: Port 6 01b: Port 0 10b: Port 4 11b: Port 5 NOTE: This feature is only valid when the port is implemented.	0x0
22:16	RW	DISBC2C PU	When this bit = 1, BC frames from the corresponding port are not forwarded to the CPU. 1'b0: Forwarded to the CPU port. 1'b1: Not forwarded to the CPU port. NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x7F
15	RW	UNI_FCBP_OPTION	Unicast frame flow control/back pressure option 0: If FC/BP is disabled on all ports, the switch uses only drop_threshold to drop frames. If any port disables FC/BP, this port uses fc_threshold and to drop frames. 1: When FC/BP is disabled on the destination Tx port, the switch only uses drop_threshold to drop frames. If FC/BP is enabled on the destination Tx port, the switch uses fc_threshold and drop_threshold to drop frames.	0x0

14:8	RW	DISMC2C_PU	When this bit = 1, MC frames from the corresponding port are not forwarded to the CPU. 1'b0: Forwarded to the CPU port. 1'b1: Not forwarded to the CPU port. NOTE: Port 5 function is only valid when the port 5 Gigabit MAC is implemented.	0x7F
7	-	-	Reserved	-
6:0	RW	DISUN2C_PU	When this bit=1, unknown UC frames from the corresponding port are not forwarded to the CPU. 1'b0: Forwarded to the CPU port. 1'b1: Not forwarded to the CPU port. NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x7F

POC1: Port Control 0 (offset: 0x0090)

Bits	Type	Name	Description	Initial value
31:30	RW	HASH_ADDR_SHIFT	Address Table Hashing Algorithm Option for Member Set Index	0x0
29	RW	DIS_GMII_PORT_1	Disables Port 6 0: Enable port 6 1: Disable port 6	0x1
28	RW	DIS_GMII_PORT_0	Disables Port 5 0: Enable port 5 1: Disable port 5 NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x1
27:23	RW	DIS_PORT	Disables the PHY Port. 0: Enable the PHY port. 1: Disable the PHY port.	0x1F
22:16	RW	DISRMC2_CPU	Unknown Reserved Multicast Frames are not forwarded to the CPU. 1'b0: Unknown reserved multicast forward rule (SGC.RMC_RULE) applied. 1'b1: Not forwarded to the CPU port. NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x0
15	-	-	Reserved	-
14:8	RW	EN_FC	Applies 802.3x Status after Auto-negotiation. This field can individually control the 802.3x capability after auto-negotiation is done. 0: Ignore the AN status for 802.3x capability. 1: Follow the AN status for 802.3x capability. NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x7F
7	RW	MC_FCBP_OPTION-	Multicast Flow Control/Back Pressure Option 0: When FC/BP is disabled on all ports, the switch uses only drop_threshold to drop frames. If FC/BP is enabled, the switch uses fc_threshold and drop_threshold to drop frames. 1: When FC/BP is disabled on the destination Tx port, the switch uses only drop_threshold to drop frames. If FC/BP is enabled, the destination Tx port uses fc_threshold and drop_threshold.	0x0

6:0	RW	EN_BP	Applies Back Pressure Capability 0: Ignore the back pressure mode (default OFF). 1: Apply back pressure based on SGC.BP_MODE. NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x7F

POC1: Port Control 1 (offset: 0x0094)

Bits	Type	Name	Description	Initial value
31:23	-	-	Reserved	-
29:23	RW	DisIPMC2CPU	Unknown IP multicast Frame not forwarded to the CPU. 1'b0: Unknown IP multicast forward rule (SGC.IP_MULT_RULE) applied. 1'b1: Unknown IP multicast frame not forwarded to the CPU port. NOTE: This function is only valid when the port is implemented.	0x0
22:16	RW	BLOCKING_STATE	Port State for Spanning Tree Protocol 0: Normal state 1: Blocking state, RMC packets are forwarded to the CPU (need programming address table). NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x0
15	-	-	Reserved	-
14:8	RW	DIS_LRNING	Disables SA Learning. 0: Enable source MAC learning (default). 1: Disable source MAC learning. NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x0
7	-	-	Reserved	0x0
6:0	RW	SA_SECURED _PORT	SA Secured Mode 0: SAs are not required to match. 1: SAs must match. If they do not match the packets are discarded. NOTE: 1. dis_learn and sa_secured must be set at the same time. 2. Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x0

POC2: Port Control 2 (offset: 0x0098)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	-
30	RW	G1_TXC_CHECK	0: Port 6 TXC is not checked. 1: Checks the port 6 TXC. If no TXC clock is detected, the MII port is disabled.	0x0
29	RW	G0_TXC_CHECK	0: Port 6 TXC is not checked. 1: Checks the port 5 TXC. If no TXC clock is detected, the MII port is disabled. NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
28:26	-	-	Reserved	-

25	RW	MLD2CPU_EN	MLD message packets are forwarded to the CPU. 1'b0: MLD message packets are flooded to all ports. 1'b1: MLD message packets are flooded to the CPU port only.	0x0
24:23	RW	IPV6_MULT_RULE	Unknown IPV6 Multicast Frame Forward Rule If no match for an IPV6 multicast frame can be found in the address table, then one of the following actions are taken. 00: BC 01: Forward to the CPU 10: Drop 11: Reserved	0x0
22:16	RW	DIS_UC_PAUSE	Disable Unicast Pause Frames 0: The switch examines the unicast pause frame when DA!=0180c20001 and a unicast stream is forwarded to the CPU. 1: The switch does not examine a unicast pause frame when DA!= 0180c20001 and a unicast stream is sent to the CPU. NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x0
15	RW	PER_VLAN_UNTAG_EN	Allows VLAN untagging by port. 0: Use UNTAG_EN per port. 1: Enable the use of untag in a VLAN table bitmap.	0x0
14:8	RW	ENAGING PORT	Port Aging 0: Disable aging on a MAC address belonging to a specified port(s). 1: Enable aging. NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x7F
7	-	-	Reserved	-
6:0	RW	UNTAG_EN	Per **P**ort VLAN **T**ag **R**emoval 0: Disable 1: Enable VLAN tag field removal. NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x0

SGC: Switch Global Control (offset: 0x009c)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	-
30	RW	BKOFF_ALG	Backoff Algorithm Option 0: Set the Ralink proprietary algorithm (default). 1: Comply with UNH test.	0x1
29	RW	LEN_ERR_CHK	Enables checking of the length of a received frame. When this bit is set, the length of encapsulated frames in received packets is checked. 0: Disabled (default) 1: Comply with UNH test.	0x1

28:27	RW	IP_MULT_RULE	Unknown IP Multicase Frame Forward Rule If no match for an IP multicase frame can be found in the address table, then one of the following actions are taken. 00: BC 01: Forward to CPU 10: Drop 11: Reserved	0x0
26:25	RW	RMC_RULE	Unknown Reserved Multicast Frame Forward Rule If no match for a reserved multicast frame can be found in the address table, then one of the following actions are taken. 00: To all ports (not include blocking state port) 01: Forward to the CPU 10: Drop 11: Reserved	0x0
24:23	RW	LED_FLASH_ TIME	LED Flash Frequency 00: 30 ms 01: 60 ms 10: 240 ms 11: 480 ms	0x0
22:21	RW	BISH_TH	Memory Bishop Threshold 11: Skip if 8 blocks fail memory testing, 0. 00: Skip if 16 blocks fail memory testing (default, from pins). 01: Skip if 48 blocks fail memory testing. 10: Skip if 64 blocks fail memory testing.	0x0
20	RO	BISH_DIS	Built In Self-hop 0: Enable the skip function (default, from pin)	0x0
19:18	RW	BP_MODE	Back Pressure Mode. 00: Disable 01: BP jam - the jam number is set by bp_num. 10: BP jamALL - jam the packet until the BP condition is released (default). 11: BP carrier - use carrier insertion to carry out back pressure.	0x2
17:16	RW	DISMIIPORT_ WASTX	Disable GMII port was_transmit This function is useful for late CRS PHY, such as HPNA2.0 or power-LAN. 0: Enable 1: Disable was_transmit NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
15:12	RW	BP_JAM_CNT	Back Pressure Jam Number The consecutive jam count when back pressure is enabled. The default is a 10-packet jam then one no-jam packet.	0xA
11	RW	DISABLE TX BACKOFF	Disable Collision Backoff Timer 0: Backoff period based on backoff algorithm (default). 1: Re-transmits immediately after collision.	0x0

10:9	RW	ADDRESS_HASH_ALG	MAC Address Hashing Algorithm 00: Direct mode, using the last 10 bits as the hashing address. 01: XOR48 mode 10: XOR32 mode 11: Reserved	0x0
8	RW	DIS_PKT_TX_ABORT	Disable Packet Tx Abort 0: Enable collision 16 packet abort and late collision abort. 1: Disable collision 16 packet abort and late collision abort.	0x0
7:6	RW	PKT_MAX_LEN	Maximum Packet Length. Bits / Untagged / VLAN-tagged 00b / 1536 bytes / 1536 bytes 01b / 1518 bytes / 1522 bytes 10b / 1522 bytes / 1526 bytes 11b / Reserved / Reserved	0x1
5:4	RW	BC_STORM_PROT	Global Broadcast Storm Protection BC is blocked depending on the specified number of BC blocks in output queues. 00: Disable 01: 64 blocks 10: 96 blocks 11: 128 blocks	0x0
3:0	RW	AGING INTERVAL	Aging Timer 0000: Disable aging timer 0001: 300 sec 0010 ~ 0111: 600 ~ 38400 sec 1xxx: Fast age (60 sec)	0x1

STRT: Switch Reset (offset: 0x00a0)

Bits	Type	Name	Description	Initial value
31:0	WO	Reset_SW	Resets the switch engine, data, address, link memory, CPU port, and AHB interface when writing data to the STRT register.	0x0

LEDP0: LED Port0 (offset: 0x00a4)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	-
3:0	RW	P0_LED	Port 0 LED State, default = link/activity 4'b0000: Link 4'b0001: 100 MHz speed 4'b0010: Duplex 4'b0011: Activity 4'b0100: Collision 4'b0101: Link/activity 4'b0110: Duplex/collsion 4'b0111: 10 MHz speed/activity 4'b1000: 100 MHz speed/activity 4'b1011: Off 4'b1100: On 4'b1010: Blink	0x5

LEDP1: LED Port 1 (offset: 0x00a8)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	-
3:0	RW	P1_LED	Port 1 LED State, default = link/activity	0x5

LEDP2: LED Port 2 (offset: 0x00ac)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	-
3:0	RW	P2_LED	Port 2 LED State, default = link/activity	0x5

LEDP3: LED Port 3 (offset: 0x00b0)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	-
3:0	RW	P3_LED	Port 3 LED State, default = link/activity	0x5

LEDP4: LED Port 4 (offset: 0x00b4)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	-
3:0	RW	P4_LED	Port 4 LED State, default = link/activity	0x5

WDTR: Watch Dog Trigger Reset (offset: 0x00b8)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	-
7:0	RW	BUF_STARV_TH	Buffer Starvation Threshold Switch interrupts the CPU when the global queue block counts are less than the threshold for 3 seconds.	0x1E

DES: Debug Signal (offset: 0x00bc)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:0	RO	DEBUG_SIGNAL	Port 5 debug signal	0x0

PCR0: PHY Control Register 0 (offset: 0x00c0)

Bits	Type	Name	Description	Initial value
31:16	RW	WT_NWAY_DATA	The data to be written into the PHY.	0x0
15	-	-	Reserved	-
14	RW	RD_PHY_CMD	Read Command To enable read command on PHY, write '1' to this bit. After the command is completed, this bit is self-cleared.	0x0
13	RW	WT_PHY_CMD	Write Command To enable write command on PHY, write '1' to this bit. After the command is completed, this bit is self-cleared.	0x0
12:8	RW	CPU_PHY_REG_ADDR	PHY Register Address	0x0
7:5	-	-	Reserved	0x0
4:0	RW	CPU_PHY_ADDR	PHY Address NOTE: The internal 5-port PHY reserves the PHY address starting from 5'd0 ~ 5'd4. For the external PHY, the PHY address from 5'd5 to 5'd31 can be applied. The default PHY address of Port 5 is 5'd5 for auto-polling function.	0x0

PCR1: PHY Control Register 1 (offset: 0x00c4)

Bits	Type	Name	Description	Initial value
31:16	RO	RD_DATA	Read Data	0x0
15:2	-	-	Reserved	-
1	RO	RD_RDY	Read operation is done, read clear.	0x0
0	RO	WT_DONE	Write operation is done, read clear.	0x0

FPA1: Force Port 5 ~Port 6 Ability (offset: 0x00c8)

Bits	Type	Name	Description	Initial value
31:30	-	-	Reserved	-
29	RW	AP_EN	Port 5 Auto-polling Enable NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
28:24	RW	EXT_PHY_ADDR_BASE	Port 5 External PHY Base Address NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x5
23:22	R/W	G0_RXCLK_SKEW_SEL	Port 5 Rx clock skew selection 00: no dealy 01: delay 150ps 10: delay 300ps 11: clock inversion	0x1
21	R/W	G0_RXCLK_MODE_SEL	Port 5 Rx clock control 0: delay 2ns on input rx_clk 1: no delay	0x0
20	R/W	G0_TXCLK_MODE_SEL	Port 5 Tx clock skew selection 0: HP mode (clock and data are in-phase) 1: 3Com mode (clock and data is 90 degree offset)	0x1
19	-	-	Reserved	0x0
18	RW	TURBO_MII_CLK	Port 5 revMII Mode Clock Selection 0: 25 MHz output clock 1: 31.25 MHz output clock NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
17:14	-	-	Reserved	-
13	RW	FORCE_RGMII_LINK1	Forces a link on port 6. This field is valid only when FORCE_MODE is set. The final resolution is reported to POA register. 0: Link down 1: Link up	0x0
12	RW	FORCE_RGMII_LINK0	Forces a link on port 5. This field is valid only when FORCE_MODE is set. The final resolution is reported to POA register. 0: Link down 1: Link up NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
11	RW	FORCE_RGMII_EN1	Enables force mode on port 6. 0: Reserved 1: Force mode. Auto-negotiation status is ignored. Port 5 functionality is forced according to the following fields of the register FPA1.	0x0
10	RW	FORCE_RGMII_EN0	Enables force mode on port 5. 0: Default	0x0

			1: Force mode. Auto-negotiation status is ignored. Port 5 functionality is forced according to the following fields of the register FPA1. NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	
9:8	RW	FORCE_ RGMII_XFC1	Forces flow control on port 6. This field is valid only when FORCE_MODE is set. The final resolution is reported to POA register. 1x: For Tx x1: For Rx	0x3
7:6	RW	FORCE_ RGMII_XFC0	Forces flow control on port 5. This field is valid only when FORCE_MODE is set. The final resolution is reported to POA register. 1x: For Tx x1: For Rx NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
5	RW	FORCE_ RGMII_DPX1	Forces duplex mode on port 6. This field is valid only when FORCE_MODE is set. The final resolution is reported to POA register. 0: Half duplex 1: Full duplex	0x1
4	RW	FORCE_ RGMII_DPX0	Forces duplex mode on port 5. This field is valid only when FORCE_MODE is set. The final resolution is reported to POA register. 0: Half duplex 1: Full duplex NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
3:2	RW	FORCE_ RGMII_SPD1	Forces a speed setting on port 6. This field is valid only when FORCE_MODE is set. The final resolution is reported to POA register. 1x: 1 Gbps 01: 100 Mbps 00: 10 Mbps	0x2
1:0	RW	FORCE_ RGMII_SPD0	Force a speed setting on port 5. This field is valid only when FORCE_MODE is set. The final resolution is reported to POA register. 1x: 1 Gbps 01: 100 Mbps 00: 10 Mbps NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0

FCT2: Flow Control Threshold 2 (offset: 0x00cc)

Bits	Type	Name	Description	Initial value
31:25	-	-	Reserved	-
24:18	RW	DIS_IPV6MC2CPU	Unknown IPv6 multicast frame not forwarded to the CPU. 1'b0: Unknown IPv6 multicast forward rule (POC2.IPV6_MULT_RULE) is followed. 1'b1: Not forwarded to the CPU port.	0x0
17:13	RW	MUST_DROP_RLS_ TH	If the global queue pointer is higher than the threshold, the must drop condition is released.	0x5

12:8	RW	MUST_DROP_SET_TH	If the global queue pointer exceeds the threshold, all incoming packets are dropped.	0x3
7:6	-	-	Reserved	-
5:0	RW	MC_PER_PORT_TH	MC Packets Per Port Threshold When the global queue reaches the flow control threshold on register FCT0, the per port output threshold for MC packets is checked to enable flow-control or packet-drop on incoming MC packets.	0xC

QSS0: Queue_Status_0 (offset: 0x00d0)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:15	RO	BE_CNT_R	Shows the block counter for the link control best effort queue.	0x0
14:5	RO	BK_CNT_R	Shows the block counter for the link control background queue.	0x0
4:0	RW	SEE_CNT_PORT_SEL	Selects the port for the link control block counter.	0x0

QSS1: Queue_Status_1 (offset: 0x00d4)

Bits	Type	Name	Description	Initial value
31:18	-	-	Reserved	-
17:9	RO	VO_CNT_R	Shows the block counter for the link control voice queue.	0x0
8:0	RO	CL_CNT_R	Shows the block counter for the link control load queue.	0x0

DEC: Debug Control (offset: 0x00d8)

Bits	Type	Name	Description	Initial value
31:24	RW	SW2FE_BRIDGE IPG	SW2FE Bridge IPG Byte Count Inter-frame byte count between the consecutive frames flowing from the switch to the frame engine.	0x40
23:16	RW	FE2SW_BRIDGE IPG	FE2SW Bridge IPG Byte Count Inter-frame byte count between the consecutive frames flowing from the frame engine to the switch.	0x40
15:9	-	-	Reserved	-
8	RW	BRIDGE_EN	FE2SW Bridge IPG Prevention Enable 1'b0: Disable 1'b1: Enable IPG Prevention when FE2SW_BRIDGE_IPG is too short (8'd16) to receive the next frame.	0x1
7:6	-	-	Reserved	-
5:3	RW	DEBUG_SW_PORT_SEL	Port 5 Debug Selection Control NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
2:0	-	-	Reserved	-

MTI: Memory Test Information (offset: 0x00dc)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	-

15:7	RO	SKIP_BLOCKS	Skip Block Counter This field indicates how many blocks are skipped due to a memory bit fault.	0x0
6	RS	SW_MEM_TEST_DONE	Switch Memory Test Done	0x0
5	RS	LK_RAM_TEST_DONE	Link Ram Test Done	0x0
4	RO	LK_RAM_TEST_FAIL	Link Ram Test Failed	0x0
3	RS	AT_RAM_TEST_DONE	Address Table Ram Test Done	0x0
2	RO	AT_RAM_TEST_FAIL	Address Table Ram Test Failed	0x0
1	RS	DT_RAM_TEST_DONE	Data Buffer Ram Test Done	0x0
0	RO	DT_RAM_TEST_FAIL	Data Buffer Ram Test Failed	0x0

PPC: Port 6 Packet Counter (offset: 0x00e0)

Bits	Type	Name	Description	Initial value
31:16	RO	SW2FE_CNT	Switch to Frame Engine Packet Counter	0x0
15:0	RO	FE2SW_CNT	Frame Engine to Switch Packet Counter	0x0

SGC2: Switch Global Control 2 (offset: 0x00e4)

Bits	Type	Name	Description	Initial value
31	RW	P6_RXFC_QUE_EN	Port 6 Egress Queue Rx Flow Control Enable 0: Rx flow control on port 6 pauses all 4 egress queues. 1: Rx flow control on port 6 pauses 4 egress queues independently according to corresponding congestion signals.	0x0
30	RW	P6_TXFC_WL_EN	Tx flow control on port 6 is determined by the switch's WAN/LAN port. 0: Tx flow control on port 6 is determined by switch congestion at any port and any queue. 1: Tx flow control on port 6 is determined by switch congestion at the WAN/LAN port.	0x0
29:24	RW	LAN_PMAP	LAN Port Bit Map This field indicates per port attributes used for flow control. 0: WAN port 1: LAN port NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x0
23	RW	SPECIAL_TAG_EN	Special Tag Enable 0: (Default) Rx special tags are enabled according to the global control bit- CPU_TPID_EN. Tx special tags are enabled according to the per port TX_CPU_TPID_BIT_MAP. 1: CPU_TPID_EN is not used. Both the Tx and Rx special tags feature are decided by the per port TX_CPU_TPID_BIT_MAP.	0x0
22:16	RW	TX_CPU_TPID_BIT_MAP	Transmit CPU TPID(0x810?) Port Bit Map 0: Default (TPID=0x8100) 1: TPID=0x810? depending on Tx/Rx usage NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x0
15:13	-	-	Reserved	-

12	RW	P6_TXFC_QUE_EN	Tx Flow Control Per Queue on Port 6 This bit is only valid when P6_TXFC_WL_EN is enabled. 0: 4 congestion signals to the frame engine are decided by the wired-or result of all egress queues on the switch's WAN/LAN ports. 1: 4 congestion signals to the frame engine are decided by the individual and the corresponding 4 egress queues on the switch's WAN/LAN ports.	0x0
11	RW	ARBITER_LAN_EN	Enables the memory arbiter only on P0~P4. 0: Memory arbiter is enabled on all ports (default). 1: Enable the memory arbiter only for P0~P4.	0x0
10	RW	CPU_TPID_EN	CPU TPID(81xx) Enable 0: Disable. CPU TPID=8100 1: Enable. CPU TPID=810x	0x0
9	RW	ARBITER_GPT_EN	Memory Arbiter only for P5 and P6 0: Default 1: Memory arbiter only for P5 and P6.	0x0
8	RW	SLOT_4TO1	Memory Arbiter Ratio Selection 0: (P5,P6) : (P0-P4) = 3:2 1: (P5,P6) : (P0-P4) = 4:1	0x0
7	-	-	Reserved	-
6:0	RW	DOUBLE_TAG_EN	Double Tag Field Enable When this bit is set, the incoming packet inserts an outer or double tag. 0: Disables the double tag field. 1: Enables double tag field. NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x0

P0PC: Port 0 Packet Counter (offset: 0x00e8)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT0	Port 0 Rx Bad Packet Counter	0x0
15:0	RO	GOOD_PKT_CNT0	Port 0 Rx Good Packet Counter	0x0

P1PC: Port 1 Packet Counter (offset: 0x00ec)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT1	Port 1 Rx Bad Packet Counter	0x0
15:0	RO	GOOD_PKT_CNT1	Port 1 Rx Good Packet Counter	0x0

P2PC: Port 2 Packet Counter (offset: 0x00f0)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT2	Port 2 Rx Bad Packet Counter	0x0
15:0	RO	GOOD_PKT_CNT2	Port 2 Rx Good Packet Counter	0x0

P3PC: Port 3 Packet Counter (offset: 0x00f4)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT3	Port 3 Rx Bad Packet Counter.	0x0
15:0	RO	GOOD_PKT_CNT3	Port 3 Rx Good Packet Counter.	0x0

P4PC: Port 4 Packet Counter (offset: 0x00f8)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT4	Port 4 Rx Bad Packet Counter	0x0
15:0	RO	GOOD_PKT_CNT4	Port 4 Rx Good Packet Counter	0x0

P5PC: Port 5 Packet Counter (offset: 0x00fc)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT5	Port 5 Rx Bad Packet Counter NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
15:0	RO	GOOD_PKT_CNT5	Port 5 Rx Good Packet Counter NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0

VUB0: VLAN Untag Block 0 (offset: 0x0100)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	-
27:21	RW	VLAN_3_UNTAG_EN	Port 0 ~ 6 Untag_en of VLAN 3 NOTE: Port 5 function is only valid when port 5 Gigabit MAC is implemented.	0x0
20:14	RW	VLAN_2_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 2	0x0
13:7	RW	VLAN_1_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 1	0x0
6:0	RW	VLAN_0_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 0	0x0

VUB0: VLAN Untag Block 1 (offset: 0x0104)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	-
27:21	RW	VLAN_7_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 7.	0x0
20:14	RW	VLAN_6_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 6.	0x0
13:7	RW	VLAN_5_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 5.	0x0
6:0	RW	VLAN_4_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 4.	0x0

VUB0: VLAN Untag Block 2 (offset: 0x0108)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	-
27:21	RW	VLAN_11_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 11.	0x0
20:14	RW	VLAN_10_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 10.	0x0
13:7	RW	VLAN_9_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 9.	0x0
6:0	RW	VLAN_8_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 8.	0x0

VUB0: VLAN Untag Block 3 (offset: 0x010c)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	-
27:21	RW	VLAN_15_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 15.	0x0
20:14	RW	VLAN_14_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 14.	0x0
13:7	RW	VLAN_13_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 13.	0x0
6:0	RW	VLAN_12_UNTAG_EN	Port 0 ~ 6 untag_en of VLAN 12.	0x0

BMU_CTRL: Broadcast/Multicast/Unknown Rate Limit Control (offset: 0x0110)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	-
30:24	RW	ONE_US_CYCLE_NUM	One Micro-second Cycle Number This field is used to calculate 1 us period.	0x7C
23	-	-	Reserved	-

22:20	RW	P5_RATE_LIMIT_CTRL	Port 5 Rate Limit Control NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
19	-	-	Reserved	-
18:16	RW	P4_RATE_LIMIT_CTRL	Port 4 Rate Limit Control	0x0
15	-	-	Reserved	-
14:12	RW	P3_RATE_LIMIT_CTRL	Port 3 Rate Limit Control	0x0
11	-	-	Reserved	-
10:8	RW	P2_RATE_LIMIT_CTRL	Port 2 Rate Limit Control	0x0
7	-	-	Reserved	-
6:4	RW	P1_RATE_LIMIT_CTRL	Port 1 Rate Limit Control	0x0
3	-	-	Reserved	-
2:0	RW	P0_RATE_LIMIT_CTRL	Port 0 Rate Limit Control 0: Enable unknown frames. 1: Enable multicast frames. 2: Enable broadcast frames.	0x0

BMU_LMT_NUM_1: Broadcast/Multicast/Unknown Rate Limit Frame Number 1 (offset: 0x0114)

Bits	Type	Name	Description	Initial value
31:16	RW	RATE_LIMIT_NUMBER_100M	The maximum number of broadcast, multicast, or unknown frames received in 100 Mbps in a 100 ms interval.	0xFFFF
15:0	RW	RATE_LIMIT_NUMBER_10M	The maximum number of broadcast, multicast, or unknown frames received in 10 Mbps in a 1 sec interval.	0xFFFF

RL_NUM_10M: Rate Limit Frame Number 2 (offset: 0x0118)

Bits	Type	Name	Description	Initial value
31	RW	INGRESS_RATE_BYTE_OPTION	Ingress Rate Byte Option 0: Add 1: Minus	0x0
30:24	RW	INGRESS_RATE_BYTE_NUM	Ingress Rate Byte Number	0x18
23	RW	EGRESS_RATE_BYTE_OPTION	Egress Rate Byte Option 0: Add 1: Minus	0x0
22:16	RW	EGRESS_RATE_BYTE_NUM	Egress Rate Byte Number.	0x18
15:0	RW	RATE_LIMIT_NUMBER_1000M	The maximum number of broadcast, multicast, or unknown frames received in 1000 Mbps in a 10 ms interval. NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0xFFFF

P01_ING_CTRL: Port 0 & 1 Ingress Rate Limit Control (offset: 0x011c)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	-
30	RW	P1_INGRESS_Ctrl	Port 1 Ingress Limit Control 0: Disable 1: Enable	0x0

29	RW	P1_MNG_PKT_BYPASS	Port 1 Management Packet Bypass Allows management frames to be ignored when dropping packets based on the ingress rate limit. Only BPDU, IGMP, and MLD packets are bypassed. 0: All packets are included. 1: Management frames packets are excluded.	0x0
28	RW	P1_INGRESS_FLOW_CTRL_ON	Port 1 Ingress Rate Flow Control When the bit is set, the pause frame is used prior to dropping a packet according to P1_ING_THRES. If the bucket is empty, then P1 discards the received packets except those packets specified in P1_MNG_PKY_BYPASS mode. 0: Disable 1: Enable	0x0
27:26	RW	P1_TIMER_TICK	Port 1 Timer Tick 0: 512 us 1: 128 us 2: 32 us 3: 8 us	0x0
25:16	RW	P1_TOKEN	Port 1 Token. Sets the number of bytes to be added into the bucket for every timer tick (unit: byte). The maximum space of this bucket is 16'hFFFF bytes.	0x0
15	-	-	Reserved	-
14	RW	P0_INGRESS_CTRL	Port 0 Ingress Limit Control 0: Disable 1: Enable	0x0
13	RW	P0_MNG_PKT_BYPASS	Port 0 Management Packet Bypass Allows management frames to be ignored when dropping packets based on the ingress rate limit. Only BPDU, IGMP and MLD packets are bypassed. 0: All packets are included. 1: Management frame packets are excluded.	0x0
12	RW	P0_INGRESS_FLOW_CTRL_ON	Port 0 Ingress Rate Flow Control When the bit is set, the pause frame is used prior to dropping a packet according to P0_ING_THRES. If the bucket is empty, then P0 discards the received packets except those packets specified in P0_MNG_PKY_BYPASS mode. 0: Disable 1: Enable	0x0
11:10	RW	P0_TIMER_TICK	Port 0 Timer Tick 0: 512 us 1: 128 us 2: 32 us 3: 8 us	0x0
9:0	RW	P0_TOKEN	Port 0 Token Sets the number of bytes to be added into the bucket for every timer tick (unit: byte). The maximum space of the bucket is 16'hFFFF bytes.	0x0

P23_ING_CTRL: Port 2 & 3 Ingress Rate Limit Control (offset: 0x0120)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	-

30	RW	P3_INGRESS_CTRL	Port 3 Ingress Limit Control 0: Disable 1: Enable	0x0
29	RW	P3_MNG_PKT_BYPASS	Port 3 Management Packet Bypass Allows management frames to be ignored when dropping packets based on the ingress rate limit. Only BPDU, IGMP and MLD packets are bypassed. 0: All packets are included. 1: Management frame packets are excluded.	0x0
28	RW	P3_INGRESS_FLOW_CTRL_ON	Port 3 Ingress Rate Flow Control When the bit is set, the pause frame is used prior to dropping a packet according to P3_ING_THRES. If the bucket is empty, then P3 discards the received packets except those packets in P3_MNG_PKY_BYPASS mode. 0: Disable 1: Enable	0x0
27:26	RW	P3_TIMER_TICK	Port 3 timer Tick 0: 512 us 1: 128 us 2: 32 us 3: 8 us	0x0
25:16	RW	P3_TOKEN	Port 3 Token Sets the number of bytes to be added into the bucket for every timer tick (unit: byte). The maximum space of this bucket is 16'hFFFF bytes.	0x0
15	-	-	Reserved	-
14	RW	P2_INGRESS_CTRL	Port 2 Ingress Limit Control 0: Disable 1: Enable	0x0
13	RW	P2_MNG_PKT_BYPASS	Port 2 Management Packet Bypass Allows management frames to be ignored when dropping packets based on the ingress rate limit. Only BPDU, IGMP and MLD packets are bypassed. 0: All packets are included. 1: Management frame packets are excluded.	0x0
12	RW	P2_INGRESS_FLOW_CTRL_ON	Port 2 Ingress Rate Flow Control When the bit is set, the pause frame is used prior to dropping a packet according to P2_ING_THRES. If the bucket is empty, then Port 2 discards the received packets except those packets in P2_MNG_PKY_BYPASS mode. 0: Disable 1: Enable	0x0
11:10	RW	P2_TIMER_TICK	Port 2 Timer Tick 0: 512 us 1: 128 us 2: 32 us 3: 8 us	0x0
9:0	RW	P2_TOKEN	Port 2 Token For every timer tick, the number of token bytes is added into the bucket (unit: byte). The maximum space of this bucket is 16'hFFFF bytes.	0x0

P45_ING_CTRL: Port 4 & 5 Ingress Rate Limit Control (offset: 0x0124)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	-
30	RW	P5_INGRESS_CTRL	Port 5 Ingress Limit Control. 0: Disable 1: Enable NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
29	RW	P5_MNG_PKT_BYPASS	Port 5 Management Packet Bypass Allows management frames to be ignored when dropping packets based on the ingress rate limit. Only BPDU, IGMP and MLD packets are bypassed. 0: All packets are included. 1: Management frame packets are excluded. NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
28	RW	P5_INGRESS_FLOW_CTRL_ON	Port 5 Ingress Rate Flow Control When the bit is set, the pause frame is used prior to dropping a packet according to P4_ING_THRES. If the bucket is empty, then Port 4 discards the received packets except those packets in P4_MNG_PKY_BYPASS mode. 0: Disable 1: Enable NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
27:26	RW	P5_TIMER_TICK	Port 5 timer Tick 0: 512 us 1: 128 us 2: 32 us 3: 8 us NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
25:16	RW	P5_TOKEN	Port 5 Token Sets the number of bytes to be added into the bucket for every timer tick (unit: byte). The maximum space of this bucket is 16'hFFFF bytes. NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
15	-	-	Reserved	-
14	RW	P4_INGRESS_CTRL	Port 4 Ingress Limit Control 0: Disable 1: Enable	0x0
13	RW	P4_MNG_PKT_BYPASS	Port 4 Management Packet Bypass Allows management frames to be ignored when dropping packets based on the ingress rate limit. Only BPDU, IGMP and MLD packets are bypassed. 0: All packets are included. 1: Management frame packets are excluded.	0x0

12	RW	P4_INGRESS_ FLOW_CTRL_ON	Port 4 Ingress Rate Flow Control When the bit is set, the pause frame is used prior to dropping a packet according to P4_ING_THRES. If the bucket is empty, then Port 4 discards the received packets except those packets in P4_MNG_PKY_BYPASS mode. 0: Disable 1: Enable	0x0
11:10	RW	P4_TIMER_TICK	Port 4 Timer Tick 0: 512 us 1: 128 us 2: 32 us 3: 8 us	0x0
9:0	RW	P4_TOKEN	Port 4 Token. Sets the number of bytes to be added into the bucket for every timer tick (unit: byte).The maximum space of this bucket is 16'hFFFF bytes.	0x0

P0_ING_THRES: Port 0 Ingress Rate Limit Threshold (offset: 0x0128)

Bits	Type	Name	Description	Initial value
31:16	RW	P0_IN_FC_OFF_ THRESHOLD	Port 0 Ingress Rate Limit flow Control Off If P0_INGRESS_FLOW_CTRL_ON = 1 and port 0 flow control capability is on (XFC status in 0x80), then port 0 initiates a PAUSE OFF frame or stops backpressure.	0xaaaa
15:0	RW	P0_IN_FCON_ THRES	Port 0 ingress rate limit flow control on. If P0_INGRESS_FLOW_CTRL_ON = 1 and Port 0 flow control capability is on (XFC status in 0x80), then Port 0 initiates a PAUSE ON frame or backpressure.	0x5555

P1_ING_THRES: Port 1 Ingress Rate Limit Threshold (offset: 0x012c)

Bits	Type	Name	Description	Initial value
31:16	RW	P1_IN_FC_OFF_ THRESHOLD	Port 1 Ingress Rate Limit Flow Control Off	0xaaaa
15:0	RW	P1_IN_FCON_THRES	Port 1 Ingress Rate Limit Flow Control On	0x5555

P2_ING_THRES: Port 2 Ingress Rate Limit Threshold (offset: 0x0130)

Bits	Type	Name	Description	Initial value
31:16	RW	P2_IN_FC_OFF_THRESHOLD	Port 2 Ingress Rate Limit Flow Control Off	0xaaaa
15:0	RW	P2_IN_FCON_THRES	Port 2 Ingress Rate Limit Flow Control On	0x5555

P3_ING_THRES: Port 3 Ingress Rate Limit Threshold (offset: 0x0134)

Bits	Type	Name	Description	Initial value
31:16	RW	P3_IN_FC_OFF_THRESHOLD	Port 3 Ingress Rate Limit Flow Control Off	0xaaaa
15:0	RW	P3_IN_FCON_THRES	Port 3 Ingress Rate Limit Flow Control On	0x5555

P4_ING_THRES: Port 4 Ingress Rate Limit Threshold (offset: 0x0138)

Bits	Type	Name	Description	Initial value
31:16	RW	P4_IN_FC_OFF_THRESHOLD	Port 4 Ingress Rate Limit Flow Control Off	0xaaaa
15:0	RW	P4_IN_FCON_THRES	Port 4 Ingress Rate Limit Flow Control On	0x5555

P5_ING_THRES: Port 5 Ingress Rate Limit Threshold (offset: 0x013c)

Bits	Type	Name	Description	Initial value
31:16	RW	P5_IN_FC_OFF_THRESHOLD	Disables Port 5 Ingress Rate Limit Flow Control NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0xaaaa
15:0	RW	P5_IN_FCON_THRES	Enables Port 5 Ingress Rate Limit Flow Control NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x5555

P01_EG_CTRL: Port 0 & 1 Egress Rate Limit Control (offset: 0x0140)

Bits	Type	Name	Description	Initial value
31:29	-	-	Reserved	-
28	RW	P1_EGRESS_CTRL	Port 1 Egress Control 0: Disable 1: Enable	0x0
27:26	RW	P1_TIMER_TICK	Port 1 Timer Tick 0: 512 us 1: 128 us 2: 32 us 3: 8 us	0x0
25:16	RW	P1_TOKEN	Port 1 Token Sets the number of bytes to be added into the bucket for every timer tick (unit: byte). The maximum space of this bucket is 16'hFFFF bytes.	0x0
15:13	-	-	Reserved	0x0
12	RW	P0_EGRESS_CTRL	Port 0 Egress Control 0: Disable 1: Enable	0x0
11:10	RW	P0_TIMER_TICK	Port 0 Timer Tick 0: 512 us 1: 128 us 2: 32 us 3: 8 us	0x0
9:0	RW	P0_TOKEN	Port 0 Token Sets the number of bytes to be added into the bucket for every timer tick (unit: byte). The maximum space of this bucket is 16'hFFFF bytes.	0x0

P23_EG_CTRL: Port 2 & 3 Egress Rate Limit Control(offset: 0x0144)

Bits	Type	Name	Description	Initial value
31:29	-	-	Reserved	-
28	RW	P3_EGRESS_CTRL	Port 3 Egress Control 0: Disable 1: Enable	0x0
27:26	RW	P3_TIMER_TICK	Port 3 Timer Tick 0: 512 us 1: 128 us 2: 32 us 3: 8 us	0x0
25:16	RW	P3_TOKEN	Port 3 Token Sets the number of bytes to be added into the bucket for every timer tick (unit: byte). The maximum space of this bucket is 16'hFFFF bytes.	0x0
15:13	-	-	Reserved	-

12	RW	P2_EGRESS_CTRL	Port 2 Egress Control 0: Disable 1: Enable	0x0
11:10	RW	P2_TIMER_TICK	Port 2 Timer Tick 0: 512 us 1: 128 us 2: 32 us 3: 8 us	0x0
9:0	RW	P2_TOKEN	Port 2 Token Sets the number of bytes to be added into the bucket for every timer tick (unit: byte). The maximum space of this bucket is 16'hFFFF bytes.	0x0

P45_EG_CTRL: Port 4 & 5 Egress Rate Limit Control (offset: 0x0148)

Bits	Type	Name	Description	Initial value
31:29	-	-	Reserved	-
28	RW	P5_EGRESS_CTRL	Port 5 Egress Control 0: Disable 1: Enable NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
27:26	RW	P5_TIMER_TICK	Port 5 Timer Tick 0: 512 us 1: 128 us 2: 32 us 3: 8 us NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
25:16	RW	P5_TOKEN	Port 5 Token Sets the number of bytes to be added into the bucket for every timer tick (unit: byte). The maximum space of this bucket is 16'hFFFF bytes. NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
15:13	-	-	Reserved	-
12	RW	P4_EGRESS_CTRL	Port 4 Egress Control 0: Disable 1: Enable	0x0
11:10	RW	P4_TIMER_TICK	Port 4 Timer Tick 0: 512 us 1: 128 us 2: 32 us 3: 8 us	0x0
9:0	RW	P4_TOKEN	Port 4 Token Sets the number of bytes to be added into the bucket for every timer tick (unit: byte). The maximum space of this bucket is 16'hFFFF bytes.	0x0

PCRI: Packet Counter Recycle Indication (offset: 0x014c)

Bits	Type	Name	Description	Initial value
31	RW	PTK_CNT_CLR	When this bit is set, all Tx/Rx packet counters are cleared. This bit can be set to self-clear automatically.	0x0
30	-	-	Reserved	-

29:24	W1C	TCOL_PKT_REC	This bit sets the packet collision counter for tranmitted packets on each port to recycle the count. Write '1' to clear this bit.	0x0
23:22	-	-	Reserved	-
22:16	W1C	TXOK_PKT_REC	This bit sets the packet collision counter for tranmitted packets on each port to recycle the count Write '1' to clear this bit.	0x0
15:14	-	-	Reserved	-
13:8	W1C	BADD_PKT_REC	This bit sets the packet collision counter for tranmitted packets on each port to recycle the count Write '1' to clear this bit.	0x0
8:7	-	-	Reserved	-
6:0	W1C	GOOD_PKT_REC	This bit sets the packet collision counter for tranmitted packets on each port to recycle the count Write '1' to clear this bit.	0x0

P0TPC: Port 0 Tx Packet Counter (offset: 0x0150)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT0	Packet collision counter for transmitted packets on port 0.	0x0
15:0	RO	GOOD_PKT_CNT0	Packet counter for successfully transmitted packets on port 0.	0x0

P1TPC: Port 1 Tx Packet Counter (offset: 0x0154)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT1	Packet collision counter for transmitted packets on port 1.	0x0
15:0	RO	GOOD_PKT_CNT1	Packet counter for successfully transmitted packets on port 1.	0x0

P2TPC: Port 2 Packet Counter (offset: 0x0158)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT2	Packet collision counter for transmitted packets on port 2.	0x0
15:0	RO	GOOD_PKT_CNT2	Packet counter for successfully transmitted packets on port 2.	0x0

P3TPC: Port 3 Tx Packet Counter (offset: 0x015c)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT3	Packet collision counter for transmitted packets on port 3.	0x0
15:0	RO	GOOD_PKT_CNT3	Packet counter for successfully transmitted packets on port 3.	0x0

P4TPC: Port 4 Tx Packet Counter (offset: 0x0160)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT4	Packet collision counter for transmitted packets on port 4.	0x0
15:0	RO	GOOD_PKT_CNT4	Packet counter for successfully transmitted packets on port 4.	0x0

P5TPC: Port 5 Tx packet counter (offset: 0x0164)

Bits	Type	Name	Description	Initial value
31:16	RO	BAD_PKT_CNT5	Packet collision counter for transmitted packets on port 5. NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0
15:0	RO	GOOD_PKT_CNT5	Packet counter for successfully transmitted packets on port 5. NOTE: This feature is only valid when port 5 Gigabit MAC is implemented.	0x0

LEDC: LED Control Register (offset: 0x0168)

Bits	Type	Name	Description	Initial value
31:5	-	RES	Reserved	0x0
4:0	RW	LED_POLARITY	LED Polarity Control for each port 1'b0: Low active 1'b1: High active	0x0

3.20.5 MII Control Register

These registers are accessed by PCR0 (PHY control register 0) and PCR1 indirectly.
Among them, PHY reg0~1 and 4~6 are unique for each port. PHY reg2~3 are common to all five ports.

Legend:

SC: Self-clearing, RC: Read-clearing

LL: Latching low, LH: Latching high

R/W: Read/write, RO: Read-only

CR Address: 00(d00) Reset State: 3100

Bit	Read/Write	Name	Description	Default
15	RW; SC	MR_MAIN_RESET	0: Normal 1: Reset Resets all digital logic, except phy_reg.	0x0
14	RW	LOOPBACK_MII	MII loopback	0x0
13	RW	FORCE_SPEED	0: 10 Mbps, when mr_autoneg_enable = 1'b0 1: 100 Mbps	0x1
12	RW	MR_AUTONEG_ENABLE	0: Normal 1: Enabled	0x1
11	RW	POWERDOWN	Sets PHY into Power Down mode. Analog Tx, analog Rx, and analog AD are powered down.	0x0
10	-	-	Reserved	0x0
9	RW; SC	MR_RESTART_NEGOTIATION	0: Normal 1: Restart auto-negotiation	0x0
8	RW	FORCE_DUPLEX	0: Half duplex, when mr_autoneg_enable = 1'b0. 1: Full duplex	0x1
7:0	-	-	Reserved	0x0

MII Status Register

CR Address: 01(d01) Reset State: 7849

Bit	Read/Write	Name	Description	Default
15	-	100 BASE T4	Not supported	0x0
14	RO	100BASE-X full duplex	0: PHY does not support a 100BASE-X connection in full duplex mode.	0x1

			1: PHY supports a 100BASE-X connection in full duplex mode.	
13	RO	100BASE-X half duplex	0: PHY does not support a 100BASE-X connection in half duplex mode. 1: PHY supports a 100BASE-X connection in half duplex mode.	0x1
12	RO	10 Mbps full duplex	0: PHY does not support a 10 Mbps/s connection in full duplex mode. 1: PHY supports a 10 Mbps/s connection in full duplex mode.	0x1
11	RO	10 Mbps half duplex	0: PHY does not support a 10 Mbps/s connection in half duplex mode. 1: PHY supports a 10 Mbps/s connection in half duplex mode.	0x1
10	RO	100BASE-T2 full duplex	Not supported	0x0
9	RO	100BASE-T2 half duplex	Not supported	0x0
8:7	-	-	Reserved	-
6	RO	MF Preamble Suppression	0: PHY cannot accept management frames with preamble suppression. 1: PHY can accept management frames with preamble suppression.	0x1
5	RO	mr_autoneg_complete	0: Auto-negotiate incomplete. 1: Auto-negotiate completed.	0x0
4	-	-	Reserved	-
3	RO	Autoneg Ability	0: PHY cannot auto-negotiate. 1: PHY can auto-negotiate.	0x1
2	RO/LL	Link Status	0: Link is down. 1: link is up.	0x0
1	RO/LH; RC	Jabber Detect	1: Jabber condition detected.	0x0
0	RO	Extended Capability	0: Basic register set capabilities only 1: Extended register capabilities	0x1

PHY Identifier Register

CR Address: 02(d02) Reset State: 00c3

Bit	Read/Write	Name	Description	Default
15:0	RO	PHY_ID[31-16]	OUI (bits 3-18). Ralink OUI =000C43	0xc3

PHY version register

CR Address: 03(d03) Reset State: 0800

Bit	Read/Write	Name	Description	Default
15:10	RO	PHY_ID[15-10]	OUI (bits 19-24)	0x2
9:4	RO	PHY_ID[9-4]	Manufacturer's model number (bits 5-0)	0x0
3:0	RO	PHY_ID[3-0]	Revision number (bits 3-0); Bit 0 in register 3 is the LS bit of the PHY identifier.	0x0

Auto-Negotiation advertisement register

CR Address: 04(d04) Reset State: 05e1

Bit	Read/Write	Name	Description	Default
15	R0	Next Page Enable	0: Set to not use the next page. 1: Set to use the next page.	0x0
14	-	-	Reserved	0x0

13	RW	Remote Fault Enable	0: No remote fault 1: Auto-negotiation fault detected	0x0
12:11	RO	Not Implemented	Technology ability A7-A6	0x0
10	R W	Pause	Technology ability A5	0x1
9	RO	Not Implemented	Technology ability A4	0x0
8	RW	100Base-TX Full Duplex Capable	0: Does not support full duplex 100Base-TX transmission. 1: Supports full duplex 100Base-TX transmission.	0x1
7	RW	100Base-TX Half Duplex Capable	0: Does not support half duplex 100 Base-TX transmission. 1: Supports half duplex 100 Base-TX transmission.	0x1
6	RW	10Base-T Full Duplex Capable	0: Does not support full duplex 10Base-T transmission. 1: Supports full duplex 10Base-TX transmission.	0x1
5	RW	10Base-T Half Duplex Capable	0: Does not support half duplex 10Base-T transmission. 1: Supports half duplex 10Base-TX transmission.	0x1
4:0	RW	Selector Field	Identifies type of message	0x1

Auto-Negotiation Link partner (LP) ability register

CR Address: 05(d05) Reset State: 0000

Bit	Read/ Write	Name	Description	Default
15	R O	Next Page	0: Base page is requested. 1: Link partner is requesting next page function.	0x0
14	R O	Acknowledge	0: Acknowledge not received. 1: Link partner acknowledge received successfully.	0x0
13	R O	Remote Fault	0: No remote fault 1: Auto-negotiation fault detected.	0x0
12:11	R O	Not implemented	Technology ability A7-A6	0x0
10	R O	Pause	Technology ability A5	0x0
9	R O	Not Implemented	Technology ability A4	0x0
8	R O	100Base-TX Full Duplex Capable	0: Does not support full duplex 100Base-TX transmission. 1: Supports full duplex 100Base-TX transmission.	0x0
7	R O	100 Base-TX Half Duplex Capable	0: Does not support half duplex 100Base-TX transmission. 1: Supports half duplex 100Base-TX transmission.	0x0
6	R O	10Base-T Full Duplex Capable	0: Does not support full duplex 10Base-T transmission. 1: Supports full duplex 10Base-T transmission.	0x0
5	R O	10Base-T Half Duplex Capable	0: Does not support half duplex 10Base-T transmission. 1: Supports half duplex 10Base-T transmission.	0x0
4:0	RO	Selector Field	Identifies type of message.	0x0

Auto-Negotiation expansion register

CR Address: 06(d06) Reset State: 0000

Bit	R/W/Type	Name	Description	Default
15:5	-	-	Reserved	-
4	RO/LH; RC	Parallel Detection Fault	0: No fault detected. 1: Local device parallel fault detected.	0x0
3	RO	Link Partner Next Page	0: The link partner does not support next paging.	0x0

		Able	1: The link partner supports next paging.	
2	RO	mr_np_able	0: The local device does not support next paging. 1: The local device supports next paging.	0x0
1	RO/LH; RC	Page Received	0: A new page has not been received. 1: A new page has been received.	0x0
0	RO	Link Partner Auto-negotiation Able	0: The link partner does not support auto-negotiation. 1: The link partner supports auto-negotiation.	0x0

3.20.6 Function Description

3.20.6.1 Flow Control Settings

For both FE or GE ports, flow control enable/disable is decided by the following:

1. Force mode is the highest priority.
   - 1.1. GE ports use FPA: Force port 5 ~ port 6 ability (offset: 0xC8)
     - 1.1.1. [11:10] Enable port 6 or 5 force mode.
     - 1.1.2. [9:8] Port 6 flow control ability (support asymmetric flow control [9]:TX [8]:RX).
     - 1.1.3. [7:6] Port 5 flow control ability
   - 1.2. FE ports use FPA: Force Port 4 ~ Port 0 Ability (offset: 0x84)
     - 1.2.1. [31:27] Enable port 4 ~ 0 force mode.
     - 1.2.2. [26:22] Port 4 ~ 0 flow control ability (only supports symmetric flow control).

If force mode is disabled, then use the flow control status after auto-negotiation. But there is one exception for flow control: when POC1: Port Control 0 (offset: 0x90) [14:8] "EN_FC " pause flow control is disabled, then flow control is disabled without regard to the AN result. (For GE ports, port 5 or 6, EN_FC[port_num] = 0 disables both Tx and Rx flow control.)

Regardless of whether force or AN mode is used, the final flow control enable/disable value shows on POA: Port ability (offset: 0x80) [24:16] for port 0 ~ 6.

2. Another exception on PFC0: Priority flow control – 0 (offset: 0x10) [23:16]. Turn off flow control, For Q3 traffic, the user can use this register to turn off the flow control.

3.20.6.2 VID and Tagging

3.20.6.3 VID and VLAN Member Set

RT5350 supports 16 VLANs. It can be configured to identify any 16 out of 4096 possible VIDs. These 16 VIDs could be configured by setting VIDx (X=0~15) registers. To configure the member set ports of a given VLAN, one can set the VLAN_MEMSET_x (x=0~15) register. Each bit of the VLAN_MEMSET_x register corresponds to the associated port. For example, to configure port #1 and port #3 as member ports of VLAN 5, one can set VLAN_MEMSET_5 as 8'b00001010.

3.20.6.3.1 Tag and Untag

There is a per port register to configure the egress tag and untag setting. To prevent a VLAN tagged frame from being transmitted from a given port x, set UNTAG_EN[x]=1. To configure a VLAN tagged frame to be transmitted from port y, set UNTAG_EN[y]=0. RT5350 supports VLAN tag/untag on a per egress port basis. It does not support tagging on a per VLAN/port basis.

3.20.6.3.2 Port VID

There is per port Px_PVID register to support PVID. The Px_PVID is assigned to an incoming frame which is untagged or priority tagged (i.e. VID field =0).

3.20.6.3.3 Double Tag

RT5350 supports double VLAN tags by setting a per ingress port register – DOUBLE_TAG_EN[x]. When RT5350 receives a frame from a port with DOUBLE_TAG_EN = 1, it ignores the VLAN tag filed, if any, and inserts the associated PVID in front of the frame after the MAC SA field. Then, it follows the frame forwarding decision

based on this PVID. When this frame is finally transmitted to an egress port with UNTAG_EN=0, the egress packet is double VLAN tagged if its incoming format is a single VLAN tag. It is single VLAN tagged if its incoming format is non-VLAN tagged. Please see the following figure for some examples.

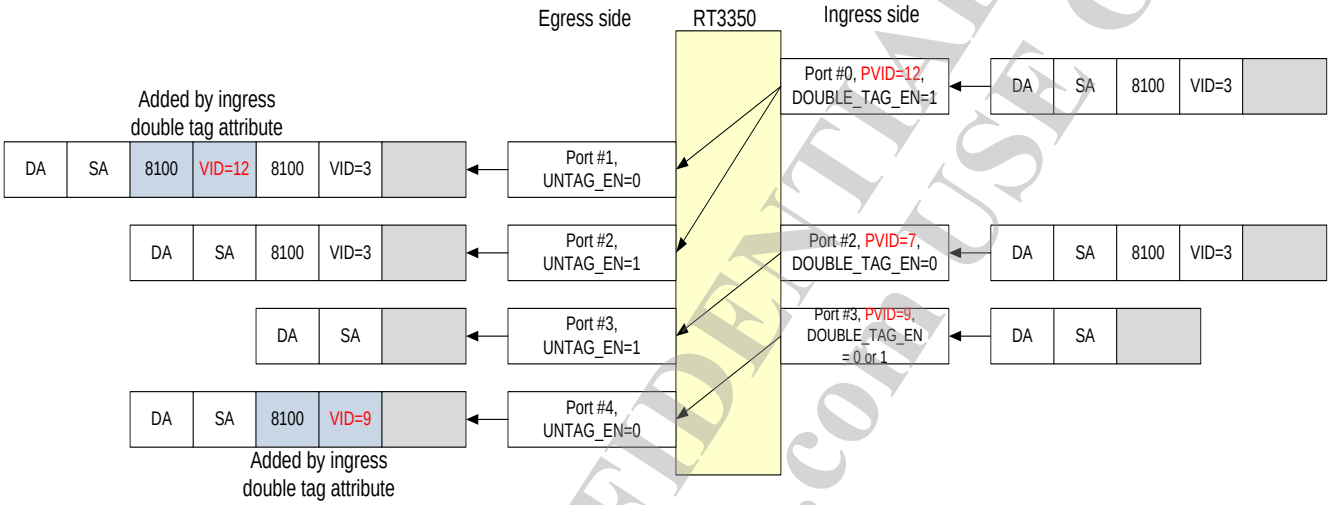


Figure 3-29 Double Tag

3.20.6.3.4 Special Tag

In order to let the recipient (e.g. RT5350 internal CPU or external 3rd party CPU) know the incoming port number of a received frame, a special tag is supported to rewrite the TPID (0x8100) filed with the incoming port number. The format of this rewritten TPID is : 810x, where x specifies the incoming port number. To enable this feature, one should set CPU_TPID_EN=1 first and specify output ports that need incoming port number to be carried by TPID by setting the associated ports in TX_CPU_TPID_BIT_MAP[6:0]. Please be noted, this special tag feature is a supplement to the existing VLAN tag feature. If the egress frame does not have a VLAN tag, there is no way for RT5350 to insert the incoming port number into the modified TPID field. If the egress frame is double VLAN tagged, the special tag applies to the outer VLAN tag only. Please see the following figure for some examples.

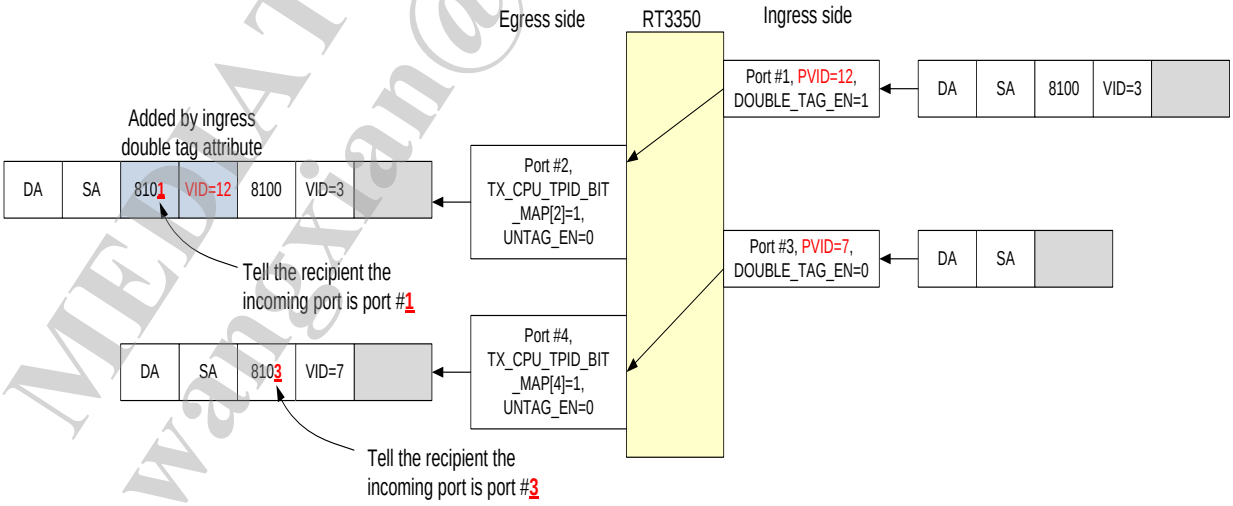


Figure 3-30 Special Tag

3.20.6.4 Packet Classification, QoS, Scheduling and Buffer Control

RT5350 supports 4 CoS queues per egress port. When a frame is received, it is classified by IP DSCP, the 802.1p tag, and incoming port priority. The classification sequence is the 802.1p tag first, then IP DSCP, and finally the incoming port priority. To enable IP DSCP classification for port x, one has to set EN_TOS[x] to 1. To enable 802.1p tag classification for port x, one has to set EN_VLAN[x] to 1. If both EN_TOS[x] and EN_VLAN[x] are zero or could not be applied (for non-IP or non-VLAN frames), frame will be classified by the PORT_PRIx register. The IP DSCP and 802.1p user priority to CoS queue mapping are specified by the following tables:

3-12 IP DSCP to CoS Queue Mapping

IP DSCP (decimal value)	CoS Queue Mapping
0~15	BK_q
16~31	BE_q
32~47	CL_q
48~63	VO_q

3-13 802.1p Priority to CoS Queue Mapping

802.1p priority (decimal value)	CoS Queue Mapping
1, 2	BK_q
0, 3	BE_q
4, 5	CL_q
6, 7	VO_q

On the egress side, there is a SP/WRR scheduler for each output port to schedule frame transmission. To use the WRR scheduler, assign the weight for each of the VO/CL/BE/BK queues to specify the service ratio. A strict priority mode is also supported to treat VO queue as the highest priority through assigning its weight (VO_NUM) to zero.

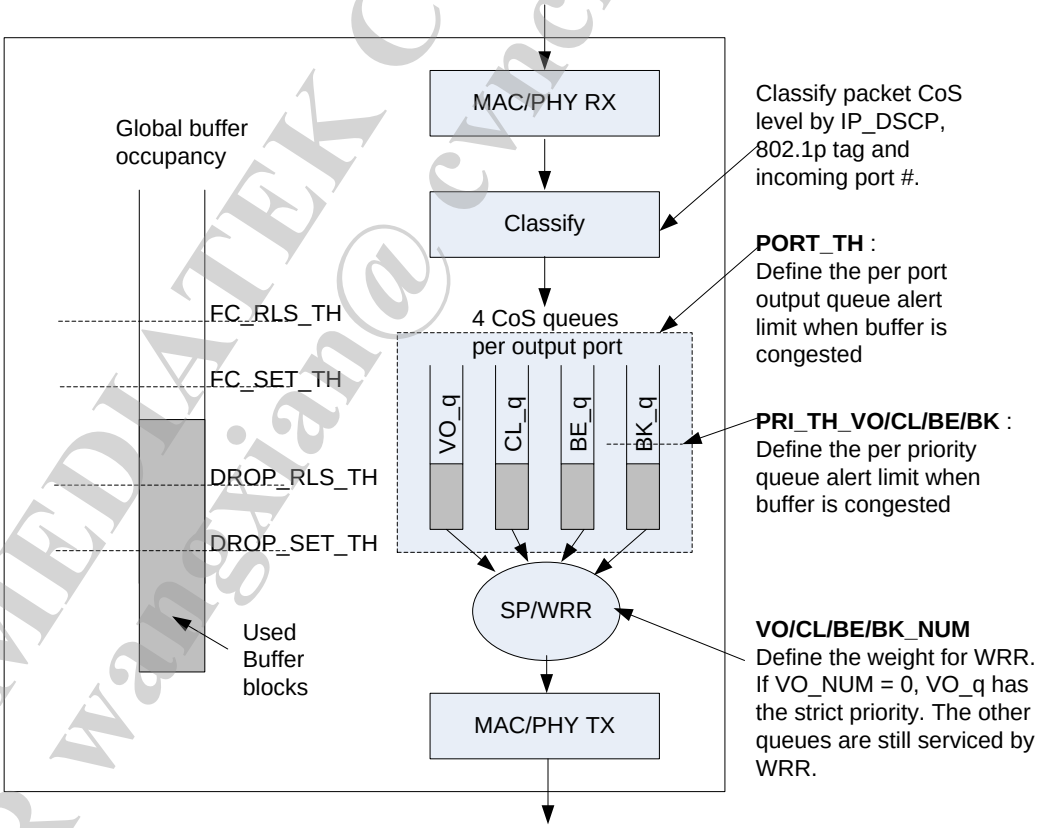


Figure 3-31 Packet Classification, QoS, Scheduling, and Buffer Control

To support QoS-aware flow control, there is a global per CoS queue threshold setting to define the alert threshold when the global packet buffer becomes congested. When the global buffer block count is lower than FC_SET_TH, an incoming frame triggers a pause_ON frame to be transmitted if the PORT_TH of the destination port and PRI_TH_xx (xx = VO or CL or BE or BK) are both reached. This sophisticated buffer control mechanism ensures that high priority traffic (e.g. VoIP) is not dropped or paused if it is put in strict priority VO_q and its source rate is controlled.

The above description for QoS-aware flow control applies even if we enable SW2FE_WL_FC_EN (switch to frame engine WAN-LAN flow control) for a one-armed router application. Since there is only a single GE port connecting the frame engine and the embedded Ethernet switch, the traditional 802.3x pause mechanism might block all frames from the CPU to the Ethernet switch regardless of a frame's destination (LAN or WAN). In other words, there is HOL (Head-of-Line blocking in this one-armed router case. To avoid HOL, LAN ports can be configured on the Ethernet switch by specifying the ports in the LAN_PMAP register. Together with a separated LAN/WAN GDMA in the frame engine, a more effective QoS-aware flow control is supported.

3.20.6.5 Spanning Tree Protocol

To eliminate LAN loops, Spanning Tree Protocol (STP) can be used to detect a loop and maintain the spanning tree topology. RT5350 can support different port states, frame forwarding and learning capability to meet STP requirements. The table below expresses the relative port states and the corresponding capabilities.

3-14 STP Port States

Port State	Receive BPDU	Transmit BPDU	Learn Address	Forward Frame
Disabled	-	-	-	-
Blocking	V	-	-	-
Listening	V	V	-	-
Learning	V	V	V	-
Forwarding	V	V	V	V

To emulate different port behaviors, the following registers can be configured based on the port state to which the software applies a port.

- Disabled
  - Disable frame transmission (POC1.BLOCKING_STATE=0x1).
  - Do not participate in the operation of the spanning tree protocol (SGC.RMC_RULE=0x2).
  - Disable source MAC learning (POC1.DIS_LRNING=0x1).
- Blocking
  - Disable frame transmission (POC1.BLOCKING_STATE=0x1).
  - Participate in the spanning tree protocol (SGC.RMC_RULE=0x1).
  - Disable source MAC learning (POC1.DIS_LRNING=0x1).
- Listening
  - Disable frame transmission (POC1.BLOCKING_STATE=0x1).
  - Participate in the operation of the spanning tree protocol (SGC.RMC_RULE=0x1).
  - Disable source MAC learning (POC1.DIS_LRNING=0x1).
- Learning
  - Discard frame transmission (POC1.BLOCKING_STATE=0x1).
  - Participate in the operation of the spanning tree protocol (SGC.RMC_RULE=0x1).
  - Enable source MAC learning (POC1.DIS_LRNING=0x0).
- Forwarding
  - Enable frame transmission (POC1.BLOCKING_STATE=0x0).
  - Participate in the operation of the spanning tree protocol (SGC.RMC_RULE=0x1).
  - Enable source MAC learning (POC1.DIS_LRNING=0x0).

3.21 802.11n 1T1R MAC/BBP

3.21.1 Features

- 1x1 modes
- 150 MHz PHY rate support
- Legacy and high throughput modes
- 20 MHz/40 MHz bandwidth
- Reverse direction data flow and frame aggregation
- WEP 64/128, WPA, WPA2, WAPI support
- QoS – WMM, WMM-PS
- Wake-on wireless LAN
- 16-Multiple BSSID support
- Supports international standards 802.11d + h
- Cisco CCX V1.0 V2.0 V3.0 compliance
- Bluetooth co-existence
- Low power with advanced power management

3.21.2 Block Diagram

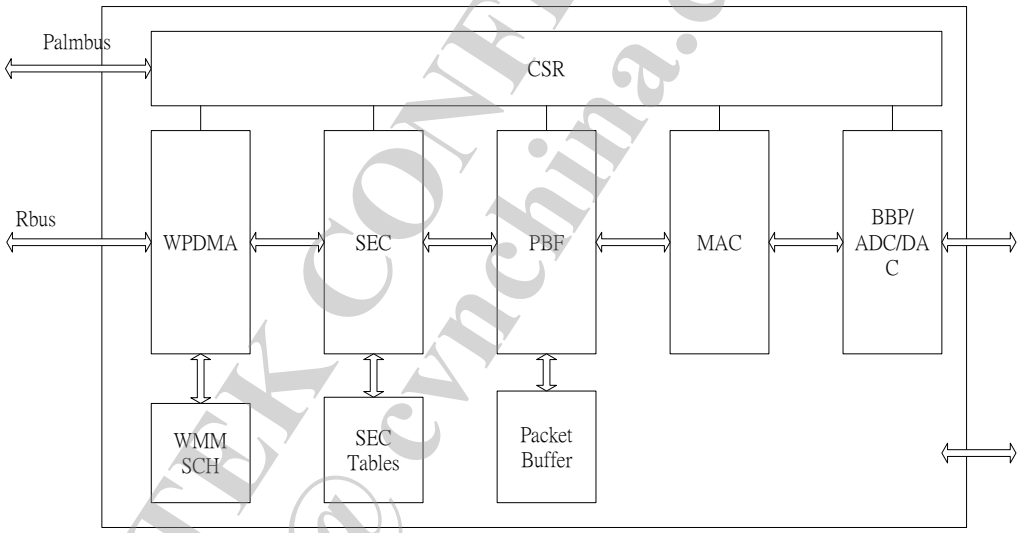


Figure 3-32 802.11n 1T1R MAC/BBP Block Diagram

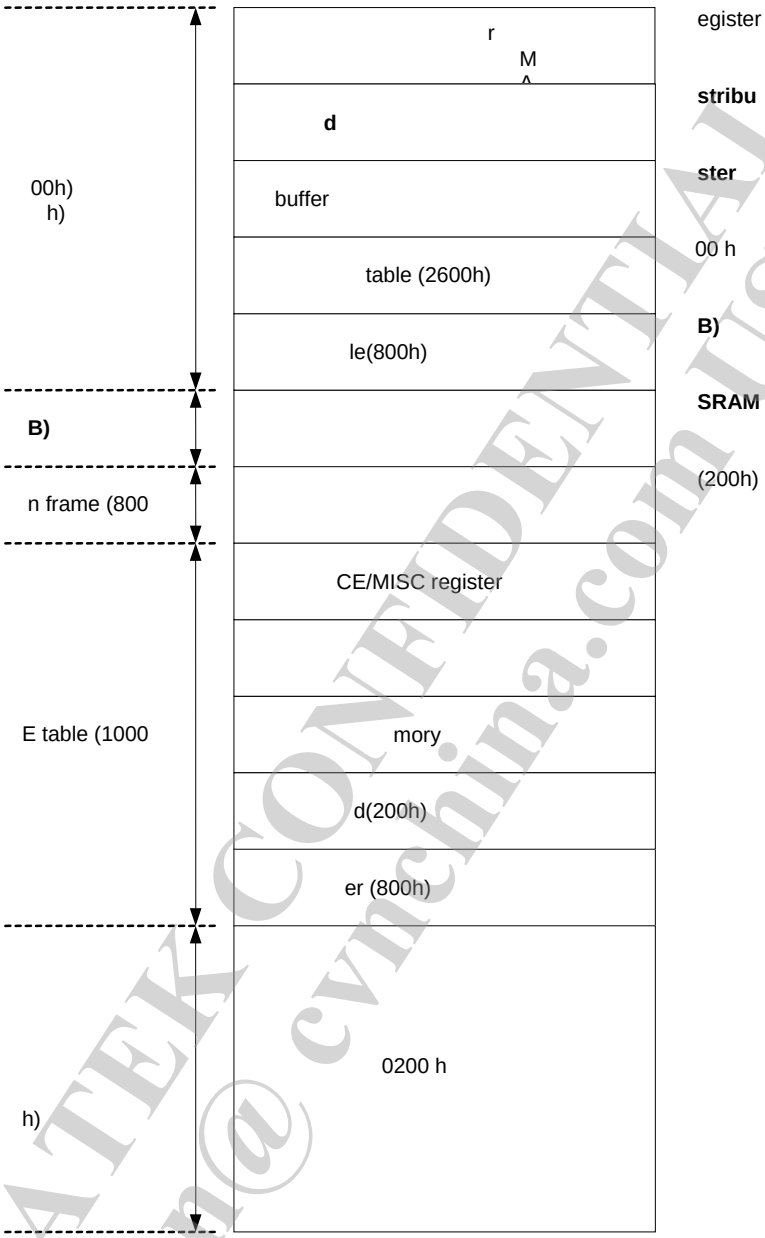


Figure 3-33 802.11n 3T3R MAC/BBP Register Map

3.21.3 Register Description - SCH/WPDMA (base: 0x1018_0000)

INT_STATUS: (offset: 0x0200)

Bits	Type	Name	Description	Initial value
31:21	-	-	Reserved	0x0
20	RW	RADAR_INT	BBP Radar Detection Interrupt	0x0
19:18	-	-	Reserved	0x0
17	RW	TX_COHERENT	TX_DMA detects a data coherent event when checking the DDONE bit. Write '1' to clear the interrupt. Read to get the raw interrupt status.	0x0
16	RW	RX_COHERENT	RX_DMA detects a data coherent event when checking the DDONE bit. Write '1' to clear the interrupt.	0x0

			Read to get the raw interrupt status.	
15	RW	MAC_INT_4	MAC interrupt 4: GP timer interrupt	0x0
14	RW	MAC_INT_3	MAC interrupt 3: Auto wakeup interrupt	0x0
13	RW	MAC_INT_2	MAC interrupt 2: Tx status interrupt	0x0
12	RW	MAC_INT_1	MAC interrupt 1: Pre-TBTT interrupt	0x0
11	RW	MAC_INT_0	MAC interrupt 0: TBTT interrupt	0x0
10	RO	TX_RX_COHERENT	When TX_COHERENT or RX_COHERENT is on, this bit is set.	0x0
9	RW	MCU_CMD_INT	MCU Command Interrupt	0x0
8	RW	TX_DONE_INT5	Tx Queue #5 Packet Transmit Interrupt 1: Clear the interrupt.	0x0
7	RW	TX_DONE_INT4	Tx Queue #4 Packet Transmit Interrupt Read to get the raw interrupt status. 1: Clear the interrupt..	0x0
6	RW	TX_DONE_INT3	Tx Queue #3 Packet Transmit Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
5	RW	TX_DONE_INT2	Tx Queue #2 Packet Transmit Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
4	RW	TX_DONE_INT1	Tx Queue #1 Packet Transmit Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
3	RW	TX_DONE_INT0	Tx Queue #0 Packet Transmit Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
2	RW	RX_DONE_INT	Rx Packet Receive Interrupt Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
1	RW	TX_DLY_INT	Summary Of All WPDMA Tx Related Interrupts Read to get the raw interrupt status. 1: Clear the interrupt.	0x0
0	RW	RX_DLY_INT	Summary Of All WPDMA Rx Related Interrupts Read to get the raw interrupt status. 1: Clear the interrupt.	0x0

INT_MASK: (offset: 0x0204)

Bits	Type	Name	Description	Initial value
31:21	-	-	Reserved	0x0
20	RW	RADAR_INT_EN	BBP Radar Detection Interrupt Enable 0: Disable the interrupt. 1: Enable the interrupt.	0x0
19:18	-	-	Reserved	0x0
17	RW	TX_COHERENT_EN	TX_DMA Data Coherent Interrupt Enable 0: Disable the interrupt. 1: Enable the interrupt.	0x0
16	RW	RX_COHERENT_EN	RX_DMA Data Coherent Interrupt Enable 0: Disable the interrupt. 1: Enable the interrupt.	0x0
15	RW	MAC_INT4_EN	MAC Interrupt 4: GP timer interrupt.	0x0
14	RW	MAC_INT3_EN	MAC Interrupt 3: Auto wakeup interrupt.	0x0
13	RW	MAC_INT2_EN	MAC Interrupt 2: Tx status interrupt.	0x0
12	RW	MAC_INT1_EN	MAC Interrupt 1: Pre-TBTT interrupt.	0x0

11	RW	MAC_INT0_EN	MAC Interrupt 0: TBTT interrupt.	0x0
10	-	-	Reserved	0x0
9	RW	MCU_CMD_INT_MSK	MCU Command Interrupt Enable 0 : Disable the interrupt. 1 : Enable the interrupt.	0x0
8	RW	TX_DONE_INT_MSK5	Tx Queue #5 Packet Transmit Interrupt 0 : Disable the interrupt. 1 : Enable the interrupt.	0x0
7	RW	TX_DONE_INT_MSK4	Tx Queue #4 Packet Transmit Interrupt 0 : Disable the interrupt. 1 : Enable the interrupt.	0x0
6	RW	TX_DONE_INT_MSK 3	Tx Queue #3 Packet Transmit Interrupt 0 : Disable the interrupt. 1 : Enable the interrupt.	0x0
5	RW	TX_DONE_INT_MSK 2	Tx Queue #2 Packet Transmit Interrupt 0 : Disable the interrupt. 1 : Enable the interrupt.	0x0
4	RW	TX_DONE_INT_MSK 1	Tx Queue #1 Packet Transmit Interrupt 0 : Disable the interrupt. 1 : Enable the interrupt.	0x0
3	RW	TX_DONE_INT_MSK 0	Tx Queue #0 Packet Transmit Interrupt 0 : Disable the interrupt. 1 : Enable the interrupt.	0x0
2	RW	RX_DONE_INT_MSK	Rx Packet Receive Interrupt 0 : Disable the interrupt. 1 : Enable the interrupt.	0x0
1	RW	TX_DLY_INT_MSK	Summary Of All WPDMA Tx Related Interrupts 0 : Disable the interrupt. 1 : Enable the interrupt.	0x0
0	RW	RX_ DLY_INT_MSK	Summary Of All WPDMA Rx Related Interrupts 0 : Disable the interrupt. 1 : Enable the interrupt.	0x0

WPDMA_GLO_CFG: (offset: 0x0208)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:8	RW	HDR_SEG_LEN	Specifies the header segment size in bytes required to support the Rx header/payload scattering function, when set to a non-zero value. 0: Disable the header/payload scattering feature.	0x0
7	RW	BIG_ENDIAN	The endian mode selection. DMA applies the endian rule to convert payload and Tx/Rx information. DMA does not apply endian rule to register or descriptor. 1: Big endian 0: Little endian	0x0
6	RW	TX_WB_DDONE	0: Disable TX_DMA writing back DDONE into TXD. 1: Enable TX_DMA writing back DDONE into TXD.	0x1
5:4	RW	WPDMA_BT_SIZE	Defines the burst size of WPDMA. 0: 4 DWORD (16 bytes) 1: 8 DWORD (32 bytes) 2: 16 DWORD (64 bytes) 3: 32 DWORD (128 bytes)	0x2
3	RO	RX_DMA_BUSY	0: RX_DMA is not busy. 1: RX_DMA is busy.	0x0

2	RW	RX_DMA_EN	0: Disable RX_DMA. When disabled, RX_DMA will finish the current receiving packet, then stop. 1: Enable RX_DMA.	0x0
1	RO	TX_DMA_BUSY	0: TX_DMA is not busy. 1: TX_DMA is busy.	0x0
0	RW	TX_DMA_EN	0: Disable TX_DMA. When disabled, TX_DMA finishes sending the current packet, then stops. 1: Enable TX_DMA.	0x0

WPDMA_RST_IDX: (offset: 0x020c)

Bits	Type	Name	Description	Initial value
31:17	-	-	Reserved	0x0
16	W1C	RST_DRX_IDX0	1: Reset RX_DMARX_IDX0 to 0.	0x0
15:6	-	-	Reserved	0x0
5	W1C	RST_DTX_IDX5	1: Reset TX_DMATX_IDX5 to 0.	0x0
4	W1C	RST_DTX_IDX4	1: Reset TX_DMATX_IDX4 to 0.	0x0
3	W1C	RST_DTX_IDX3	1: Reset TX_DMATX_IDX3 to 0.	0x0
2	W1C	RST_DTX_IDX2	1: Reset TX_DMATX_IDX2 to 0.	0x0
1	W1C	RST_DTX_IDX1	1: Reset TX_DMATX_IDX1 to 0.	0x0
0	W1C	RST_DTX_IDX0	1: Reset TX_DMATX_IDX0 to 0.	0x0

DELAY_INT_CFG: (offset: 0x0210)

Bits	Type	Name	Description	Initial value
31	RW	TXDLY_INT_EN	0: Disable the Tx delayed interrupt mechanism. 1: Enable the Tx delayed interrupt mechanism.	0x0
30:24	RW	TXMAX_PINT	Specified Maximum Number Of Pended Interrupts When the number of pended interrupts is equal to or greater than the value specified here or the interrupt pending time has reached the limit (see below), a final TX_DLY_INT is generated. 0: Disable the pending interrupt count check.	0x0
23:16	RW	TXMAX_PTIME	Specified Maximum Pending Time For the Internal TX_DONE_INT0-5. When the pending time is equal to or greater than TXMAX_PTIME x 20 us or the number of pended TX_DONE_INT0-5 is equal to or greater than TXMAX_PINT (see above), a final TX_DLY_INT is generated. 0: Disable the pending interrupt time check.	0x0
15	RW	RXDLY_INT_EN	0: Disable Rx delayed interrupt mechanism. 1: Enable Rx delayed interrupt mechanism.	0x0
14:8	RW	RXMAX_PINT	Specified Maximum Number Of Pended Interrupts When the number of pended interrupts is equal to or greater than the value specified here or the interrupt pending time has reached the limit (see below), a final RX_DLY_INT is generated. 0: Disable the pending interrupt count check.	0x0
7:0	RW	RXMAX_PTIME	Specified Maximum Pending Time For The Internal RX_DONE_INT When the pending time is equal to or greater than RXMAX_PTIME x 20 us, or the number of pended RX_DONE_INT is equal to or greater than RXMAX_PCNT (see above), a final RX_DLY_INT is generated. 0: Disable the pending interrupt time check.	0x0

WMM_AIFSN_CFG: (offset: 0x0214)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:12	RW	AIFSN3	WMM parameter AIFSN3	0x0
11:8	RW	AIFSN2	WMM parameter AIFSN2	0x0
7:4	RW	AIFSN1	WMM parameter AIFSN1	0x0
3:0	RW	AIFSN0	WMM parameter AIFSN0	0x0

WMM_CWMIN_CFG: (offset: 0x0218)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:12	RW	CW_MIN3	WMM parameter Cw_min3	0x0
11:8	RW	CW_MIN2	WMM parameter Cw_min2	0x0
7:4	RW	CW_MIN1	WMM parameter Cw_min1	0x0
3:0	RW	CW_MIN0	WMM parameter Cw_min0	0x0

WMM_CWMAX_CFG: (offset: 0x021c)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:12	RW	CW_MAX3	WMM parameter Cw_max3	0x0
11:8	RW	CW_MAX2	WMM parameter Cw_max2	0x0
7:4	RW	CW_MAX1	WMM parameter Cw_max1	0x0
3:0	RW	CW_MAX0	WMM parameter Cw_max0	0x0

WMM_TXOP0_CFG: (offset: 0x0220)

Bits	Type	Name	Description	Initial value
31:16	RW	TXOP1	WMM parameter TXOP1	0x0
15:0	RW	TXOP0	WMM parameter TXOP0	0x0

WMM_TXOP1_CFG: (offset: 0x0224)

Bits	Type	Name	Description	Initial value
31:16	RW	TXOP3	WMM parameter TXOP3	0x0
15:0	RW	TXOP2	WMM parameter TXOP2	0x0

TX_BASE_PTRn: (offset: 0x0230, 0x0240, 0x0250, 0x0260, 0x0270, 0x0280)

Bits	Type	Name	Description	Initial value
31:0	RW	TX_BASE_PTRn	Points to the base address of TX_Ringn (4-DWORD aligned address).	0x0

TX_MAX_CNTn: (offset: 0x0234, 0x0244, 0x0254, 0x0264, 0x0274, 0x0284)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	0x0
11:0	RW	TX_MAX_CNTn	The maximum number of TXD count in TXD_Ringn.	0x0

TX_CTX_IDXn: (offset: 0x0238, 0x0248, 0x0258, 0x0268, 0x0278, 0x0288)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	0x0
11:0	RW	TX_CTX_IDXn	Points to the next TXD the CPU needs to read.	0x0

TX_DTX_IDXn: (offset: 0x023c, 0x024c, 0x025c, 0x026c, 0x027c, 0x028c)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	0x0
11:0	RO	TX_DTX_IDXn	Points to the next TXD the DMA will transfer.	0x0

RX_BASE_PTR: (offset: 0x0290)

Bits	Type	Name	Description	Initial value
31:0	RW	RX_BASE_PTR0	Points to the base address of the RXD ring #0 (GE ports). It should be a 4-DWORD aligned address.	0x0

RX_MAX_CNT: (offset: 0x0294)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	0x0
11:0	RW	RX_MAX_CNT0	The maximum RXD count in RXD ring #0.	0x0

RX_CALC_IDX: (offset: 0x0298)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	0x0
11:0	RW	RX_CALC_IDX0	Points to the next RXD the CPU will allocate to the RXD ring #0.	0x0

FS _DRX_IDX: (offset: 0x029c)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	0x0
11:0	RW	RX_DRX_IDX0	Points to the next RXD the DMA will use in FDS ring #0. It should be a 4-DWORD aligned address.	0x0

US_CYC_CNT: (offset: 0x02a4)

Bits	Type	Name	Description	Initial value
31:25	-	-	Reserved	0x0
24	RW	TEST_EN	Test Mode Enable	0x0
23:16	RW	TEST_SEL	Test Mode Select	0xf0
15:9	-	-	Reserved	0x0
8	RW	BT_MODE_EN	Blue-Tooth Mode Enable	0x0
7:0	RW	US_CYC_CNT	Clock cycle count in 1 us. It is dependent on the system clock rate. 8'h7D: System clock rate = 125 Mhz. 8'h85: System clock rate = 133 Mhz.	0x21

3.21.3.1 Register Description - PBF (base: 0x1018_0000)

SYS_CTRL: (offset: 0x0400)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0x0
19	RW	SHR_MSEL	Shared Memory Access Selection 0: Address 0x4000 – 0x7FFF mapping to lower 16 kB of shared memory. 1: Address 0x4000 – 0x7FFF mapping to higher 4 kB of shared memory.	0x0
18:17	RW	PBF_MSEL	Packet Buffer Memory Access Selection 00: Address 0x8000 – 0xFFFF mapping to 1st 32 kB of packet buffer. 01: Address 0x8000 – 0xFFFF mapping to 2nd 32 kB of	0x0

			packet buffer. 10: Address 0x8000 – 0xFFFF mapping to 3rd 32 kB of packet buffer.	
16	RW	HST_PM_SEL	Host Program RAM Write Selection Selects a RAM block that the host program can write to.	0x0
15	-	-	Reserved	0x0
14	RW	CAP_MODE	Packet Buffer Capture Mode 0: Packet buffer in normal mode. 1: Packet buffer in BBP capture mode.	0x0
13	-	-	Reserved	0x1
12	RW	CLKSELECT	MAC/PBF Clock Source Selection 0: From PLL 1: From 40 MHz clock input	0x0
11	RW	PBF_CLKEN	PBF Clock Enable	0x0
10	RW	MAC_CLK_EN	MAC clock Enable	0x0
9	RW	DMA_CLK_EN	DMA clock Enable	0x0
8	-	-	Reserved	0x0
7	RW	MCU_READY	MCU is ready. 8051 writes '1' to this bit to inform the host the internal MCU is ready.	0x0
6:5	-	-	Reserved	0x0
4	RW	ASY_RESET	Resets the ASYNC interface. 1: Resets ASYNC.	0x0
3	RW	PBF_RESET	Resets the PBF hardware. 1: Resets PBF.	0x0
2	RW	MAC_RESET	Resets the MAC hardware. 1: Resets the MAC .	0x0
1	RW	DMA_RESET	Resets the DMA hardware. 1: Resets the DMA.	0x0
0	W1C	MCU_RESET	Resets the MCU hardware. This bit is auto-cleared after several clock cycles.	0x0

HOST_CMD: (offset: 0x0404)

Bits	Type	Name	Description	Initial value
31:0	RW	HST_CMD	Host Command Code A host write to this register triggers an interrupt to 8051.	0x0

PBF_CFG: (offset: 0x0408)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0x0
23:21	RW	TX1Q_NUM	Queue depth of Tx1Q. The maximum number is 7.	0x7
20:16	RW	TX2Q_NUM	Queue depth of Tx2Q. The maximum number is 20.	0x14
15	RW	NULL0_MODE	HCCA NULL0 Frame Auto Mode In this mode, NULL0 frame will be automatically transmitted if TXQ1 is enabled but empty. After a NULL0 frame is transmitted, TXQ1 is disabled. 0: Disable 1: Enable	0x0
14	RW	NULL1_MODE	HCCA NULL1 Frame Auto Mode In this mode, all TXQ (0/1/2) is disabled after a NULL1 frame is transmitted. 0: Disable 1: Enable	0x0
13	RW	RX_DROP_MODE	Rx Drop Mode	0x0

			When set, PBF drops Rx packets before they go to DMA. 0: Normal mode 1: Drop mode	
12	RW	TX0Q_MODE	Tx0Q Operation Mode 0: Auto mode 1: Manual mode	0x0
11	RW	TX1Q_MODE	Tx1Q Operation Mode 0: Auto mode 1: Manual mode	0x0
10	RW	TX2Q_MODE	Tx2Q Operation Mode 0: Auto mode 1: Manual mode	0x0
9	RW	RX0Q_MODE	Rx0Q Operation Mode 0: Auto mode 1: Manual mode	0x0
8	RW	HCCA_MODE	HCCA Auto Mode In this mode, TXQ1 is enabled when CF-POLL arrives. 0: Disable 1: Enable	0x0
7:5	-	-	Reserved	0x0
4	RW	TX0Q_EN	Tx0Q Enable 0: Disable 1: Enable	0x1
3	RW	TX1Q_EN	Tx1Q Enable 0: Disable 1: Enable	0x0
2	RW	TX2Q_EN	Tx2Q Enable 0: Disable 1: Enable	0x1
1	RW	RX0Q_EN	Rx0Q Enable 0: Disable 1: Enable	0x1
0	-	-	Reserved	0x0

MAX_PCNT: (offset: 0x040c)

Bits	Type	Name	Description	Initial value
31:24	RW	MAX_TX0Q_PCNT	Maximum Tx0Q Buffer Page Count	0x1f
23:16	RW	MAX_TX1Q_PCNT	Maximum Tx1Q Buffer Page Count	0x3f
15:8	RW	MAX_TX2Q_PCNT	Maximum Tx2Q Buffer Page Count	0x9f
7:0	RW	MAX_RX0Q_PCNT	Maximum Rx0Q Buffer Page Count	0x9f

BUF_CTRL: (offset: 0x0410)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	0x0
11	W1C	WRITE_TX0Q	Manual write to Tx0Q.	0x0
10	W1C	WRITE_TX1Q	Manual write to Tx1Q.	0x0
9	W1C	WRITE_TX2Q	Manual write to Tx2Q	0x0
8	W1C	WRITE_RX0Q	Manual write to Rx0Q	0x0
7	W1C	NULL0_KICK	Kicks out NULL0 frame. This bit is cleared after the NULL0 frame is transmitted.	0x0
6	W1C	NULL1_KICK	Kicks out NULL1 frame. This bit is cleared after the NULL1 frame is transmitted.	0x0
5	W1C	BUF_RESET	Resets the buffer.	0x0

4	-	-	Reserved	0x0
3	W1C	READ_TX0Q	Manual read from Tx0Q.	0x0
2	W1C	READ_TX1Q	Manual read from Tx1Q.	0x0
1	W1C	READ_TX2Q	Manual read from Tx2Q.	0x0
0	W1C	READ_RX0Q	Manual read Rx0Q.	0x0

MCU_INT_STA: (offset: 0x0414)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	0x0
27	RW	MAC_INT_11	MAC Interrupt 11: Reserved	0x0
26	RW	MAC_INT_10	MAC Interrupt 10: Reserved	0x0
25	RW	MAC_INT_9	MAC Interrupt 9: Reserved	0x0
24	RW	MAC_INT_8	MAC Interrupt 8: Rx QoS CF-Poll interrupt	0x0
23	RW	MAC_INT_7	MAC Interrupt 7: TXOP early termination interrupt	0x0
22	RW	MAC_INT_6	MAC Interrupt 6: TXOP early timeout interrupt	0x0
21	RW	MAC_INT_5	MAC Interrupt 5: Reserved	0x0
20	RW	MAC_INT_4	MAC Interrupt 4: GP timer interrupt	0x0
19	RW	MAC_INT_3	MAC Interrupt 3: Auto wakeup interrupt	0x0
18	RW	MAC_INT_2	MAC Interrupt 2: Tx status interrupt	0x0
17	RW	MAC_INT_1	MAC Interrupt 1: Pre-TBTT interrupt	0x0
16	RW	MAC_INT_0	MAC Interrupt 0: TBTT interrupt	0x0
15	RW	ADCL5H8_INT	RF ADC Change from 5-bits to 8-bits Interrupt	0x0
14	RW	RX_SD_INT	RF Rx Signal Detection Interrupt	0x0
13:12	-	-	Reserved	0x0
11	RW	DTX0_INT	DMA to TX0Q Frame Transfer Complete Interrupt	0x0
10	RW	DTX1_INT	DMA to TX1Q Frame Transfer Complete Interrupt	0x0
9	RW	DTX2_INT	DMA to TX2Q Frame Transfer Complete Interrupt	0x0
8	RW	DRX0_INT	RX0Q to DMA Frame Transfer Complete Interrupt	0x0
7	RW	HCMD_INT	Host Command Interrupt	0x0
6	RW	N0TX_INT	NULL0 Frame Tx Complete Interrupt	0x0
5	RW	N1TX_INT	NULL1 Frame Tx Complete Interrupt	0x0
4	RW	BCNTX_INT	Beacon Frame Tx Complete Interrupt	0x0
3	RW	MTX0_INT	TX0Q to MAC Frame Transfer Complete Interrupt	0x0
2	RW	MTX1_INT	TX1Q to MAC Frame Transfer Complete Interrupt	0x0
1	RW	MTX2_INT	TX2Q to MAC Frame Transfer Complete Interrupt	0x0
0	RW	MRX0_INT	MAC to RX0Q Frame Transfer Complete Interrupt	0x0

MCU_INT_ENA: (offset: 0x0418)

Bits	Type	Name	Description	Initial value
31:28	-	-	Reserved	0x0
27	RW	MAC_INT11_EN	MAC interrupt 11 Enable	0x0
26	RW	MAC_INT10_EN	MAC interrupt 10 Enable	0x0
25	RW	MAC_INT9_EN	MAC interrupt 9 Enable	0x0
24	RW	MAC_INT8_EN	MAC Interrupt 8 Enable	0x0
23	RW	MAC_INT7_EN	MAC Interrupt 7 Enable	0x0
22	RW	MAC_INT6_EN	MAC Interrupt 6 Enable	0x0
21	RW	MAC_INT5_EN	MAC Interrupt 5 Enable	0x0
20	RW	MAC_INT4_EN	MAC Interrupt 4 Enable	0x0
19	RW	MAC_INT3_EN	MAC Interrupt 3 Enable	0x0
18	RW	MAC_INT2_EN	MAC Interrupt 2 Enable	0x0
17	RW	MAC_INT1_EN	MAC Interrupt 1 Enable	0x0
16	RW	MAC_INT0_EN	MAC Interrupt 0 Enable	0x0

15:12	-	-	Reserved	0x0
11	RW	DTX0_INT_EN	DMA to TX0Q Frame Transfer Complete Interrupt Enable	0x0
10	RW	DTX1_INT_EN	DMA to TX1Q Frame Transfer Complete Interrupt Enable	0x0
9	RW	DTX2_INT_EN	DMA to TX2Q Frame Transfer Complete Interrupt Enable	0x0
8	RW	DRX0_INT_EN	RX0Q to DMA Frame Transfer Complete Interrupt Enable	0x0
7	RW	HCMD_INT_EN	Host Command Interrupt Enable	0x0
6	RW	N0TX_INT_EN	NULL0 Frame Tx Complete Interrupt Enable	0x0
5	RW	N1TX_INT_EN	NULL1 Frame Tx Complete Interrupt Enable	0x0
4	RW	BCNTX_INT_EN	Beacon Frame Tx Complete Interrupt Enable	0x0
3	RW	MTX0_INT_EN	TX0Q to MAC Frame Transfer Complete Interrupt Enable	0x0
2	RW	MTX1_INT_EN	TX1Q to MAC Frame Transfer Complete Interrupt Enable	0x0
1	RW	MTX2_INT_EN	TX2Q to MAC Frame Transfer Complete Interrupt Enable	0x0
0	RW	MRX0_INT_EN	MAC to RX0Q Frame Transfer Complete Interrupt Enable	0x0

TX0Q_IO: (offset: 0x041c)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:0	RW	TX0Q_IO	TX0Q IO port. This register is used in manual mode.	0x0

TX1Q_IO: (offset: 0x0420)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:0	RW	TX1Q_IO	TX1Q IO port. This register is used in manual mode.	0x0

TX2Q_IO: (offset: 0x0424)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:0	RW	TX2Q_IO	TX2Q IO port. This register is used in manual mode.	0x0

RX0Q_IO: (offset: 0x0428)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:0	RW	RX0Q_IO	RX0Q IO port. This register is used in manual mode.	0x0

BCN_OFFSET0: (offset: 0x042c)

Bits	Type	Name	Description	Initial value
31:24	RW	BCN3_OFFSET	Beacon #3 Address Offset in shared memory. Unit is 64 bytes.	0xec
23:16	RW	BCN2_OFFSET	Beacon #2 Address Offset in shared memory. Unit is 64 bytes.	0xe8
15:8	RW	BCN1_OFFSET	Beacon #1 Address Offset in shared memory. Unit is 64 bytes.	0xe4
7:0	RW	BCN0_OFFSET	Beacon #0 Address Offset in shared memory. Unit is 64 bytes.	0xe0

NOTE:
There are two beacon frame buffers on this chip. They are located at 0x4000 - 0x4FFF (SHR_MSEL = 1) and 0x6000 – 0x7FFF (SHR_MSEL = 0).
The physical address of beacon frame is calculated by:

If OFFSET < 0x40

Set SHR_MSEL = 1 (SYS_CTRL[19] = 1)

Beacon frame starting address = OFFSET *64 + 0x4000 (0x4000 – 0x4FFF)

Else if OFFSET >= 0x80

Set SHR_MSEL = 0 (SYS_CTRL[19] = 0)
Beacon frame starting address = OFFSET *64 + 0x4000 (0x6000 – 0x7FFF)

Else

This address can not be the beacon buffer.

BCN_OFFSET1: (offset: 0x0430)

Bits	Type	Name	Description	Initial value
31:24	RW	BCN7_OFFSET	Beacon #7 Address Offset in shared memory. Unit is 64 bytes.	0xfc
23:16	RW	BCN6_OFFSET	Beacon #6 Address Offset in shared memory. Unit is 64 bytes.	0xf8
15:8	RW	BCN5_OFFSET	Beacon #5 Address Offset in shared memory. Unit is 64 bytes.	0xf4
7:0	RW	BCN4_OFFSET	Beacon #4 Address Offset in shared memory. Unit is 64 bytes.	0xf0

TXRXQ_STA: (offset: 0x0434)

Bits	Type	Name	Description	Initial value
31:24	RO	RX0Q_STA	RxQ Status	0x22
23:16	RO	TX2Q_STA	Tx2Q Status	0x2
15:8	RO	TX1Q_STA	Tx1Q Status	0x2
7:0	RO	TX0Q_STA	Tx0Q Status	0x2

TXRXQ_PCNT: (offset: 0x0438)

Bits	Type	Name	Description	Initial value
31:24	RO	RX0Q_PCNT	Page Count in RxQ	0x0
23:16	RO	TX2Q_PCNT	Page Count in Tx2Q	0x0
15:8	RO	TX1Q_PCNT	Page Count in Tx1Q	0x0
7:0	RO	TX0Q_PCNT	Page Count in Tx0Q	0x0

PBF_DBG: (offset: 0x043c)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7:0	RO	FREE_PCNT	Free Page Count	0xfe

CAP_CTRL: (offset: 0x0440)

Bits	Type	Name	Description	Initial value
31	RW	CAP_ADC_FEQ	Data Source 0: Data from the ADC output 1: Data from the FEQ output	0x0
30	WC	CAP_START	Data Capture Start 0: No action 1: Start data capture (cleared automatically after capture finished).	0x0
29	W1C	MAN_TRIG	Manual Capture Trigger	0x0
28:16	RW	TRIG_OFFSET	Starting Address Offset Before Trigger Point	0x140
15:13	-	-	Reserved	0x0
12:0	RO	START_ADDR	Starting Address Of Captured Data	0x0

3.21.3.2 Register Description – RF TEST (base: 0x1018_0000)

CSR_RF_CFG: (offset: 0x0500)

Bits	Type	Name	Description	Initial value
31:18	-	-	Reserved	0x0

17	RW	RF_CSR_KICK	Write – kick RF register read/write 0: Do nothing 1: Kick read/write process Read – Polling RF register read/write 0: Idle 1: Busy	0x0
16	RW	RF_CSR_WR	0: Read 1: Write	0x0
15:14	-	-	Reserved	0x0
13:8	RW	TESTCSR_RFACC_REGNUM	RF Register ID R0 ~ R63 0 for R0, 1 for R1 and so on.	0x0
7:0	RW	RF_CSR_DATA	Write – Data written to RF. Read – Data read from RF.	0x0

3.21.3.3 Register Description - MAC (base: 0x1018_0000)

ASIC_VER_ID: (offset: 0x1000)

Bits	Type	Name	Description	Initial value
31:16	RO	VER_ID	ASIC Version ID	0x2860
15:0	RO	REV_ID	ASIC Reversion ID	0x0101

MAC_SYS_CTRL: (offset: 0x1004)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7	RW	RX_TS_EN	Write 32-bit hardware Rx timestamp instead of (RXWI->RSSI), and write (RXWI->RSSI) instead of (RXWI->SNR). 0: Disable 1: Enable NOTE: For QA Rx sniffer mode only.	0x0
6	RW	WLAN_HALT_EN	External WLAN Halt Control Signal Enable 0: Disable 1: Enable	0x0
5	RW	PBF_LOOP_EN	Packet Buffer Loopback (Tx->Rx) Enable 0: Disable 1: Enable	0x0
4	RW	CONT_TX_TEST	Continuous Tx Production Test Override MAC_RX_EN, MAC_TX_EN. 0: Disable 1: Enable	0x0
3	RW	MAC_RX_EN	MAC Rx Enable 0: Disable 1: Enable	0x0
2	RW	MAC_TX_EN	MAC Tx Enable 0: Disable 1: Enable	0x0
1	RW	BBP_HRST	BBP Hard-reset 0: BBP in normal state 1: BBP in reset state NOTE: Whole BBP including BBP registers will be reset.	0x1
0	RW	MAC_SRST	MAC Soft-reset 0: MAC in normal state 1: MAC in reset state NOTE: MAC registers and tables will **NOT** be reset.	0x1

NOTE: MAC hard-reset is outside the scope of MAC registers.

MAC_ADDR_DW0: (offset: 0x1008)

Bits	Type	Name	Description	Initial value
31:24	RW	MAC_ADDR_3	MAC Address Byte 3	0x0
23:16	RW	MAC_ADDR_2	MAC Address Byte 2	0x0
15:8	RW	MAC_ADDR_1	MAC Address Byte 1	0x0
7:0	RW	MAC_ADDR_0	MAC Address Byte 0	0x0

MAC_ADDR_DW1: (offset: 0x100c)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:8	RW	MAC_ADDR_5	MAC Address Byte 5	0x0
7:0	RW	MAC_ADDR_4	MAC Address Byte 4	0x0

NOTE: Byte 0 is the first byte on the network. Its LSB bit is the first bit on the network. For a MAC address captured on the network with order 00:01:02:03:04:05, byte0=00, byte1=01 etc.

MAC_BSSID_DW0: (offset: 0x1010)

Bits	Type	Name	Description	Initial value
31:24	RW	BSSID_3	BSSID Byte 3	0x0
23:16	RW	BSSID_2	BSSID Byte 2	0x0
15:8	RW	BSSID_1	BSSID Byte 1	0x0
7:0	RW	BSSID_0	BSSID Byte 0	0x0

MAC_BSSID_DW1: (offset: 0x1014)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
23	R/W	MULTI_BCN_ NUM_ BIT3	Multiple BSSID Beacon number (extension bit3) Use together with MULTI_BCN_NUM: (MULTI_BCN_NUM_BIT3 * 8) + MULTI_BCN_NUM = total number of multiple BSSID beacons. 0: One back-off beacon 1-15: SIFS-burst beacon count	0
22	R/W	MULTI_BSSID_ MODE_BIT2	Multiple BSSID mode (extension bit2) Use together with MULTI_BSSID_MODE: (MULTI_BSSID_MODE_BIT2 * 4) + MULTI_BSSID_MODE = 0: 1-BSSID mode 1: 2-BSSID mode 2: 4-BSSID mode 3: 8-BSSID mode 4: 16-BSSID mode 5-7: Undefined	0
21	R/W	NEW_MULTI_ BSSID_MODE	New multiple BSSID mode 0: Use MAC address Byte5 to distinguish different BSSID. 1: Use MAC address Byte0 to distinguish different BSSID. New BSSID numbering rule: ▪ Byte0.bit0 of the MAC address is a broadcast/multicast bit. ▪ Byte0.bit1 of the MAC address is a local administration bit and should be set to 1 in extended multiple BSSIDs.	0

			▪ Byte0.bit[5:2] of the MAC address is the extended multiple BSSID index if 16-MBSS mode is set. NOTE: The following reserved-bit rules apply. ▪ Byte0.bit[5:2] should be reserved as 0 in 16-MBSS mode. ▪ Byte0.bit[4:2] should be reserved as 0 in 8-MBSS mode. ▪ Byte0.bit[3:2] should be reserved as 0 in 4-MBSS mode. ▪ Byte0.bit 2 should be reserved as 0 in 2-MBSS mode. For example: In 4-BSSID mode with the MAC address set to 00:0c:43:28:60:01, based on the new rule, the extended 3-BSSID is 02:0c:43:28:60:01, 06:0c:43:28:60:01, and 0a:0c:43:28:60:01.	
20:18	R/W	MULTI_BCN_ NUM	Reads or sets the number of BSSID beacons transmitted in a beacon interval. 0: One back-off beacon 1-7: One back-off beacon and the specified number of SIFS-burst beacons.	0
17:16	R/W	MULTI_BSSID_ MODE	Multiple BSSID mode In multiple-BSSID AP mode, BSSID is the same as MAC_ADDR, that is, this device owns multiple MAC_ADDR in this mode. The multiple MAC_ADDR/BSSID are distinguished by [bit2: bit0] of byte5. 0: 1-BSSID mode (BSS index = 0) 1: 2-BSSID mode (byte5.bit0 is the BSS index) 2: 4-BSSID mode (byte5.bit[1:0] is the BSS index) 3: 8-BSSID mode (byte5.bit[2:0] is the BSS index)	0
15:8	R/W	BSSID_5	BSSID byte5	0
7:0	R/W	BSSID_4	BSSID byte4	0

MAX_LEN_CFG: (offset: 0x1018)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0x0
19:16	RW	MIN_MPDU_LEN	Minimum MPDU Length (unit: bytes) MAC drops the MPDU if the length is less than this limitation. Applied only in MAC Rx.	0xa
15:14	-	-	Reserved	0x0
13:12	RW	MAX_PSDU_LEN	Maximum PSDU Length (power factor) 0: 2^13 = 8 KB 1: 2^14 = 16 KB 2: 2^15 = 32 KB 3: 2^16 = 64 KB MAC will NOT generate A-MPDU with length greater than this limitation. Applied only in MAC Tx.	0x0
11:0	RW	MAX_MPDU_LEN	Maximum MPDU Length (unit: bytes) MAC will drop the MPDU if the length is greater than this limitation. Applied only in MAC RX.	0xfff

BBP_CSR_CFG: (offset: 0x101c)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0x0
19	RW	BBP_RW_MODE	BBP Register R/W Mode 0: Serial mode 1: Parallel mode	0x1
18	RW	BBP_PAR_DUR	BBP Register Parallel R/W Pulse Width 0: Pulse width = 62.5 ns 1: Pulse width = 112.5 ns NOTE: Please set BBP_PAR_DUR=1 in 802.11j mode.	0x0
17	RW	BBP_CSR_KICK	Write - Kick BBP Register read/write 0: Do nothing 1: Kick read/write process Read - Polling BBP register read/write progress 0: Idle 1: Busy	0x0
16	RW	BBP_CSR_RW	0: Write 1: Read	0x0
15:8	RW	BBP_ADDR	BBP Register ID 0: R0 1: R1, and so on.	0x0
7:0	RW	BBP_DATA	Write - Data written to BBP Read - Data read from BBP	0x0

RF_CSR_CFG0: (offset: 0x1020)

Bits	Type	Name	Description	Initial value
31	RW	RF_REG_CTRL	Write: 1 - RF_REG0/1/2 to RF chip Read: 0: Idle 1: Busy	0x0
30	RW	RF_LE_SEL	RF_LE Selection 0: Activate RF_LE0. 1: Activate RF_LE1.	0x0
29	RW	RF_LE_STBY	RF_LE Standby Mode 0: RF_LE is high when on standby 1: RF_LE is low when on standby	0x0
28:24	RW	RF_REG_WIDTH	RF Register Bit Width Default: 22	0x16
23:0	RW	RF_REG_0	RF Register 0 ID and content	0x0

RF_CSR_CFG1: (offset: 0x1024)

Bits	Type	Name	Description	Initial value
31:25	-	-	Reserved	0x0
24	RW	RF_DUR	Gap between BB_CONTROL_RF and RF_LE 0: 3 system clock cycles (37.5 usec) 1: 5 system clock cycles (62.5 usec)	0x0
23:0	RW	RF_REG_1	RF Register 1 ID and content	0x0

RF_CSR_CFG2: (offset: 0x1028)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0x0
23:0	RW	RF_REG_2	RF register2 ID and content	0x0

NOTE: Software should make sure the first bit (MSB in the specified bit number) written to RF is '0' for RF chip mode selection.

LED_CFG: (offset: 0x102c)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	0x0
30	RW	LED_POL	LED Polarity 0: Active low 1: Active high	0x0
29:28	RW	Y_LED_MODE	Yellow LED Mode 0: Off 1: Blinking upon Tx 2: Periodic slow blinking 3: Always on	0x0
27:26	RW	G_LED_MODE	Green LED Mode 0: Off 1: Blinking upon Tx 2: Periodic slow blinking 3: Always on	0x2
25:24	RW	R_LED_MODE	Red LED Mode 0: Off 1: Blinking upon Tx 2: Periodic slow blinking 3: Always on	0x1
23:22	-	-	Reserved	0x0
21:16	RW	SLOW_BLK_TIME	Slow Blinking Period (unit: 1 sec)	0x3
15:8	RW	LED_OFF_TIME	Tx Blinking Off Period (unit: 1 ms)	0x1e
7:0	RW	LED_ON_TIME	Tx Blinking On Period (unit: 1 ms)	0x46

XIFS_TIME_CFG: (offset: 0x1100)

Bits	Type	Name	Description	Initial value
31:30	-	-	Reserved	0x0
29	RW	BB_RXEND_EN	BB_RX_END Signal Enable Start deferring SIFS from the BB_RX_END signal from the BBP RX logic circuit. 0: Disable to start deferring SIFS from the last bit of the last packet received. 1: Enable	0x11
28:20	RW	EIFS_TIME	EIFS Time (unit: 1 us) EIFS is the defer time after reception of a CRC error packet. After deferring EIFS, the normal back-off process may proceed.	0x13a
19:16	RW	OFDM_XIFS_TIME	Delayed OFDM SIFS Time Compensator (unit: 1 us) When BB_RX_END from BBP is a delayed version the SIFS deferred is (OFDM_SIFS_TIME - OFDM_XIFS_TIME)	0x4
15:8	RW	OFDM_SIFS_TIME	OFDM SIFS Time (unit: 1 us) Applied after OFDM Tx/Rx.	0x10
7:0	RW	CCK_SIFS_TIME	CCK SIFS Time (unit: 1 us) Applied after CCK Tx/Rx.	0xa

NOTE:

1. EIFS = SIFS + ACK @ 1 Mbps + DIFS = 10 us (SIFS) + 192 us (long preamble) + 14*8us (ACK) + 50 us (DIFS) = 364. However, MAC should start back-off procedure after (EIFS-DIFS).
2. EIFS is not applied if MAC is a TXOP initiator that owns the channel.
3. EIFS is not started if AMPDU is only partially corrupted.

Caution: It is recommended that both CCK_SIFS_TIME and OFDM_SIFS_TIME are not less than the Tx/Rx transition time. If the SIFS value is not long enough, a SIFS burst transmission may be replaced with a PIFS burst one.

BKOFF_SLOT_CFG: (offset:0x1104)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	0x0
11:8	RW	CC_DELAY_TIME	Channel Clear Delay (unit: 1 us) This value specifies the Tx guard time after a channel is clear.	0x2
7:0	RW	SLOT_TIME	Slot Time (unit: 1 us) This value specifies the slot boundary after deferring SIFS time. NOTE: Default 20 us is for 11b/g. 11a and 11g-short-slot-mode is 9 us.	0x14

NAV_TIME_CFG: (offset: 0x1108)

Bits	Type	Name	Description	Initial value
31	WC	NAV_UPD	NAV Timer Manual Update 0: Do nothing 1: Update NAV timer with NAV_UPD_VAL	0x0
30:16	RW	NAV_UPD_VAL	NAV Timer Manual Update Value (unit: 1 us)	0x0
15	RW	NAV_CLR_EN	NAV Timer Auto-Clear Enable When enabled, MAC automatically clears the NAV timer after receiving a CF-End frame from the previous NAV holder STA. 0: Disable 1: Enable	0x1
14:0	RO	NAV_TIMER	NAV Timer (unit: 1 us) The timer is set by other STA and automatically counts down to zero. The STA that set the NAV timer is called the NAV holder. When the NAV timer is non-zero, the MAC does not send any packets.	0x0

CH_TIME_CFG: (offset: 0x110c)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	0x0
4	RW	EIFS_AS_CH_BUSY	Treats the EIFS as a busy channel. 0: Disable 1: Enable	0x1
3	RW	NAV_AS_CH_BUSY	Treats the NAV as a busy channel. 0: Disable 1: Enable	0x1
2	RW	RX_AS_CH_BUSY	Treats the Rx Busy as a busy channel. 0: Disable 1: Enable	0x1
1	RW	TX_AS_CH_BUSY	Treats the Tx Busy as a busy channel. 0: Disable 1: Enable	0x1
0	RW	CH_STA_TIMER_EN	Channel Statistic Timer Enable 0: Disable 1: Enable	0x0

PBF_LIFE_TIMER: (offset: 0x1110)

Bits	Type	Name	Description	Initial value
31:0	RO	PBF_LIFE_TIMER	Tx/Rx MPDU Timestamp Timer (free run) (unit: 1 us)	0x0

BCN_TIME_CFG: (offset: 0x1114)

Bits	Type	Name	Description	Initial value
31:24	RW	TSF_INS_COMP	TSF Insertion Compensation Value (unit: 1 us) When inserting the TSF, add this value with local TSF timer as the Tx timestamp.	0x0
23:21	-	-	Reserved	0x0
20	RW	BCN_TX_EN	Beacon Frame Transmission Enable When enabled, the MAC sends a beacon frame at TBTT interrupt. 0: Disable 1: Enable	0x0
19	RW	TBTT_TIMER_EN	TBTT Timer Enable When enabled, the TBTT interrupt is issued periodically at the period specified in (BCN_INTVAL). 0: Disable 1: Enable	0x0
18:17	RW	TSF_SYNC_MODE	Local 64-bit TSF Timer Synchronization Mode 00: Disable 01: (STA infra-structure mode) Upon reception of the beacon frame from an associated BSS, the local TSF is always updated with remote TSF. 10: (STA ad-hoc mode) Upon the reception of a beacon frame from an associated BSS, the local TSF is updated with remote TSF only if the remote TSF is greater than local TSF. 11: (AP mode) does not SYNC with any station.	0x0
16	RW	TSF_TIMER_EN	Local 64-bit TSF Timer Enable When enabled, the TSF timer restarts from zero. 0: Disable 1: Enable	0x0
15:0	RW	BCN_INTVAL	Beacon Interval (unit: 64 us) This value specifies the interval between beacon frames.Maximum beacon interval is about 4 sec.	0x640

TBTT_SYNC_CFG: (offset: 0x1118)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0x0
23:20	RW	BCN_CWMIN	Beacon Transmission CWMIN after TBTT Interrupt (unit: slot)	0x4
19:16	RW	BCN_AIFSN	Beacon Transmission AIFSN after TBTT Interrupt (unit: slot)	0x2
15:8	RW	BCN_EXP_WIN	Beacon Expecting Window Duration (unit: 64 us) The window starts from TBTT interrupt. The phase of “TBTT interrupt train” is NOT adjusted by the arrival of a beacon within the window.	0x20
7:0	RW	TBTT_ADJUST	IBSS Mode TBTT Phase Adaptive Adjustment Step (unit: 1 us), default value is 16 us. In IBSS mode (ad hoc mode), if consecutive Tx beacon failures (or consecutive success) occur, the TBTT timer adjusts its phase to meet the external ad hoc TBTT time.	0x10

TSF_TIMER_DW0: (offset: 0x111c)

Bits	Type	Name	Description	Initial value
31:0	RO	TSF_TIMER_DW0	Local TSF Timer LSB 32 bits (unit: 1 us)	0x0

TSF_TIMER_DW1: (offset: 0x1120)

Bits	Type	Name	Description	Initial value
31:0	RO	TSF_TIMER_DW1	Local TSF Timer MSB 32 bits (unit: 1 us)	0x0

TBTT_TIMER: (offset: 0x1124)

Bits	Type	Name	Description	Initial value
31:17	-	-	Reserved	0x0
16:0	RO	TBTT_TIMER	TBTT Timer (unit: 32 us) Shows the time remaining on the TBTT timer as it counts down to the next TBTT. When TBTT_TIMER_EN is enabled, the timer counts down from BCN_INTVAL to zero. When TBTT_TIMER_EN is disabled, the timer stays at zero.	0x0

INT_TIMER_CFG: (offset: 0x1128)

Bits	Type	Name	Description	Initial value
31:16	RW	GP_TIMER	Period of General Purpose Interrupt Timer (unit: 64 us)	0x0
15:0	RW	PRE_TBTT_TIMER	Pre-TBTT Interrupt Timer (unit: 64 us) The value specifies the interrupt timing before the TBTT interrupt.	0x0

INT_TIMER_EN: (offset: 0x112c)

Bits	Type	Name	Description	Initial value
31:2	-	-	Reserved	0x0
1	RW	GP_TIMER_EN	Periodic General Purpose Interrupt Timer Enable 0: Disable 1: Enable	0x0
0	RW	PRE_TBTT_INT_EN	Pre-TBTT Interrupt Enable 0: Disable 1: Enable	0x0

CH_IDLE_STA: (offset: 0x1130)

Bits	Type	Name	Description	Initial value
31:0	RC	CH_IDLE_TIME	Channel Idle Time (unit: 1 us)	0x0

In application, the channel busy time is derived by the equation:
CH_BUSY_TIME = host polling period – CH_IDLE_TIME

Reserved: (offset: 0x1134)

Bits	Type	Name	Description	Initial value
31:0	-	-	Reserved	0x0

MAC_STATUS_REG: (offset: 0x1200)

Bits	Type	Name	Description	Initial value
31:2	-	-	Reserved	0x0
1	RO	RX_STATUS	Rx Status 0: Idle 1: Busy	0x0

0	RO	TX_STATUS	Tx Status 0: Idle 1: Busy	0x0

PWR_PIN_CFG: (offset: 0x1204)

Bits	Type	Name	Description	Initial value
31:4	-	-	Reserved	0x0
3	RW	IO_ADDA_PD	AD/DA Power Down	0x0
2	RW	IO_PLL_PD	PLL Power Down	0x0
1	RW	IO_RA_PE	RA_PE	0x1
0	RW	IO_RF_PE	RF_PE	0x1

AUTO_WAKEUP_CFG: (offset: 0x1208)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15	RW	AUTO_WAKEUP_EN	Auto-wakeup Interrupt Enable Auto wakeup interrupt is issued after #(SLEEP_TBTT_NUM) TBTTs' at WAKEUP_LEAD_TIME before the target wakeup TBTT. 0: Disable 1: Enable NOTE: Please make sure TBTT_TIMER_EN is enabled.	0x0
14:8	RW	SLEEP_TBTT_NUM	Sleeping TBTT Number	0x0
7:0	RW	WAKEUP_LEAD_TIME	Auto Wake Up Lead Time (unit: 1TU=1024 us)	0x14

3.21.3.4 MAC Tx Configuration Registers (offset: 0x1300)

EDCA_AC0_CFG (BE): (offset: 0x1300)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0x0
19:16	RW	AC0_CWMAX	AC0 CWMAX (unit: power of 2)	0x7
15:12	RW	AC0_CWMIN	AC0 CWMIN (unit: power of 2)	0x3
11:8	RW	AC0_AIFSN	AC0 AIFSN (unit: # of time slots)	0x2
7:0	RW	AC0_TXOP	AC0 TXOP limit (unit: 32 us)	0x0

EDCA_AC1_CFG (BK): (offset: 0x1304)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0x0
19:16	RW	AC1_CWMAX	AC1 CWMAX (unit: power of 2)	0x7
15:12	RW	AC1_CWMIN	AC1 CWMIN (unit: power of 2)	0x3
11:8	RW	AC1_AIFSN	AC1 AIFSN (unit: # of time slots)	0x2
7:0	RW	AC1_TXOP	AC1 TXOP limit (unit: 32 us)	0x0

EDCA_AC2_CFG (VI): (offset: 0x1308)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0x0
19:16	RW	AC2_CWMAX	AC2 CWMAX (unit: power of 2)	0x7
15:12	RW	AC2_CWMIN	AC2 CWMIN (unit: power of 2)	0x3
11:8	RW	AC2_AIFSN	AC2 AIFSN (unit: # of time slots)	0x2
7:0	RW	AC2_TXOP	AC2 TXOP limit (unit: 32 us)	0x0

EDCA_AC3_CFG (VO): (offset: 0x130c)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0x0

19:16	RW	AC3_CWMAX	AC3 CWMAX (unit: power of 2)	0x7
15:12	RW	AC3_CWMIN	AC3 CWMIN (unit: power of 2)	0x3
11:8	RW	AC3_AIFSN	AC3 AIFSN (unit: # of time slots)	0x2
7:0	RW	AC3_TXOP	AC3 TXOP limit (unit: 32 us)	0x0

EDCA_TID_AC_MAP: (offset: 0x1310)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:14	RW	TID7_AC_MAP	AC value when TID=7	0x3
13:12	RW	TID6_AC_MAP	AC value when TID=6	0x3
11:10	RW	TID5_AC_MAP	AC value when TID=5	0x2
9:8	RW	TID4_AC_MAP	AC value when TID=4	0x2
7:6	RW	TID3_AC_MAP	AC value when TID=3	0x0
5:4	RW	TID2_AC_MAP	AC value when TID=2	0x1
3:2	RW	TID1_AC_MAP	AC value when TID=1	0x1
1:0	RW	TID0_AC_MAP	AC value when TID=0	0x0

NOTE: Default according 802.11e Table 20.23—User priority to Access Category mappings.

TX_PWR_CFG_0: (offset: 0x1314)

Bits	Type	Name	Description	Initial value
31:24	RW	TX_PWR_OFDM_12	Tx Power for OFDM 12M/18M	0x66
23:16	RW	TX_PWR_OFDM_6	Tx Power for OFDM 6M/9M	0x66
15:8	RW	TX_PWR_CCK_5	Tx Power for CCK5.5M/11M	0x66
7:0	RW	TX_PWR_CCK_1	Tx Power for CCK1M/2M	0x66

TX_PWR_CFG_1: (offset: 0x1318)

Bits	Type	Name	Description	Initial value
31:24	RW	TX_PWR_MCS_2	Tx Power for HT MCS=2,3	0x66
23:16	RW	TX_PWR_MCS_0	Tx Power for HT MCS=0,1	0x66
15:8	RW	TX_PWR_OFDM_48	Tx Power for OFDM 48M/54M	0x66
7:0	RW	TX_PWR_OFDM_24	Tx Power for OFDM 24M/36M	0x66

TX_PWR_CFG_2: (offset: 0x131c)

Bits	Type	Name	Description	Initial value
31:24	RW	TX_PWR_MCS_10	Tx Power for HT MCS=10,11	0x66
23:16	RW	TX_PWR_MCS_8	Tx Power for HT MCS=8,9	0x66
15:8	RW	TX_PWR_MCS_6	Tx Power for HT MCS=6,7	0x66
7:0	RW	TX_PWR_MCS_4	Tx Power for HT MCS=4,5	0x66

TX_PWR_CFG_3: (offset: 0x1320)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0x66
23:16	-	-	Reserved	0x66
15:8	RW	TX_PWR_MCS_14	Tx Power for HT MCS=14,15	0x66
7:0	RW	TX_PWR_MCS_12	Tx Power for HT MCS=12,13	0x66

TX_PWR_CFG_4: (offset: 0x1324)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:8	-	-	Reserved	0x66
7:0	-	-	Reserved	0x66

TX_PIN_CFG: (offset: 0x1328)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0x0
19	RW	TRSW_POL	TRSW_EN Polarity Sets the polarity of the antenna switch. 0: Sets Rx to logic high and Tx to logic low. 1: Sets Rx to logic low and Tx to logic high.	0x0
18	RW	TRSW_EN	TRSW_EN Enable Enables the antenna switch	0x1
17	RW	RFTR_POL	RF_TR Polarity Sets the polarity of the RF. 0: Sets Rx to logic high and Tx to logic low. 1: Sets Rx to logic low and Tx to logic high.	0x0
16	RW	RFTR_EN	RF_TR Enable Enables RF.	0x1
15	RW	LNA_PE_G1_POL	LNA_PE_G1 Polarity Sets the polarity of the Low Noise Amplifier. 0: Sets LNA Rx to logic high. 1: Sets LNA Rx to logic low.	0x0
14	RW	LNA_PE_A1_POL	LNA_PE_A1 Polarity Sets the polarity of a 5 GHz dual LNA. 0: Sets LNA Rx to logic high. 1: Sets LNA Rx to logic low.	0x0
13	RW	LNA_PE_G0_POL	LNA_PE_G0 Polarity Sets the polarity of a 2.4 GHz dual LNA. 0: Sets LNA Rx to logic high. 1: Sets LNA Rx to logic low.	0x0
12	RW	LNA_PE_A0_POL	LNA_PE_A0 Polarity Sets the polarity of a 5 GHz single LNA. 0: Sets LNA Rx to logic high. 1: Sets LNA Rx to logic low.	0x0
11	RW	LNA_PE_G1_EN	LNA_PE_G1 Enable Enables a 2.4 GHz dual LNA. 0: Disable 1: Enable	0x1
10	RW	LNA_PE_A1_EN	LNA_PE_A1 Enable Enables 5 GHz dual LNA. 0: Disable 1: Enable	0x1
9	RW	LNA_PE_G0_EN	LNA_PE_G0 Enable Enables 2.4 GHz dual LNA 0: Disable 1: Enable	0x1
8	RW	LNA_PE_A0_EN	LNA_PE_A0 Enable Enables a 5 GHz single LNA 0: Disable 1: Enable	0x1
7	RW	PA_PE_G1_POL	PA_PE_G1 Polarity Sets the polarity of a 2.4 GHz dual LNA. 0: Sets LNA Rx to logic high. 1: Sets LNA Rx to logic low.	0x0
6	RW	PA_PE_A1_POL	PA_PE_A1 Polarity Sets the polarity of the 5 GHz dual power amplifier. 0: Sets the power amplifier Tx to logic high.	0x0

			1: Sets power amplifier Tx to logic low.	
5	RW	PA_PE_G0_POL	PA_PE_G0 Polarity Sets the polarity of the 2.4 GHz dual power amplifier. 0: Sets the power amplifier Tx to logic high. 1: Sets power amplifier Tx to logic low.	0x0
4	RW	PA_PE_A0_POL	PA_PE_A0 Polarity Sets the polarity of the 5 GHz dual power amplifier. 0: Sets the power amplifier Tx to logic high. 1: Sets power amplifier Tx to logic low.	0x0
3	RW	PA_PE_G1_EN	PA_PE_G1 Enable Enables a 2.4 GHz dual power amplifier.	0x1
2	RW	PA_PE_A1_EN	PA_PE_A1 Enable Enables a 5 GHz dual power amplifier.	0x1
1	RW	PA_PE_G0_EN	PA_PE_G0 Enable Enables a 2.4 GHz dual power amplifier.	0x1
0	RW	PA_PE_A0_EN	PA_PE_A0 Enable Enables a 5 GHz dual power amplifier.	0x1

TX_BAND_CFG: (offset: 0x132c)

Bits	Type	Name	Description	Initial value
31:3	-	-	Reserved	0x0
2	RW	5G_BAND_SEL_N	5 GHz Band Selection PIN (complement of 5G_BAND_SEL_P)	0x1
1	RW	5G_BAND_SEL_P	5 GHz Band Selection PIN	0x0
0	RW	TX_BAND_SEL	0: Use lower 40 Mhz band in 20 Mhz Tx. 1: Use upper 40 Mhz band in 20 Mhz Tx.	0x0

NOTE: TX_BAND_SEL is effective only when the Tx/Rx bandwidth control register R4 of BBP is set to 40 Mhz.

TX_SW_CFG0: (offset: 0x1330)

Bits	Type	Name	Description	Initial value
31:24	RW	DLY_RFTR_EN	Delay of RF_TR Assertion	0x0
23:16	RW	DLY_TRSW_EN	Delay of TR_SW Assertion	0x4
15:8	RW	DLY_PAPE_EN	Delay of PA_PE Assertion	0x8
7:0	RW	DLY_TXPE_EN	Delay of TX_PE Assertion	0xc

NOTE:
1. The timing unit is 0.25 us.
2. SIFS_TIME should compensate with DLY_TXPE_EN.

TX_SW_CFG1: (offset: 0x1334)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0x0
23:16	RW	DLY_RFTR_DIS	Delay of RF_TR De-assertion	0xc
15:8	RW	DLY_TRSW_DIS	Delay of TR_SW De-assertion	0x8
7:0	RW	DLY_PAPE_DIS	Delay of PA_PE De-assertion	0x8

NOTE:
1. The timing unit is 0.25 us.
2. The delay is started from TX_END event of BBP.
3. TX_PE is de-asserted automatically when the last data byte is passed to BBP.

TX_SW_CFG2: (offset: 0x1338)

Bits	Type	Name	Description	Initial value
31:24	RW	DLY_LNA_EN	Delay of LNA* Assertion	0x0
23:16	RW	DLY_LNA_DIS	Delay of LNA* De-assertion	0xc

15:8	RW	DLY_DAC_EN	Delay of DAC_PE Assertion	0x4
7:0	RW	DLY_DAC_DIS	Delay of DAC_PE De-assertion	0x8

NOTE:
1. The timing unit is 0.25 us.
2. LNA* includes LNA_A0, LNA_A1, LNA_G0, LNA_G1.

TXOP_THRES_CFG: (offset: 0x133c)

Bits	Type	Name	Description	Initial value
31:24	RW	TXOP_REM_THRES	Remaining TXOP Threshold (unit: 32 us) When the remaining TXOP is less than the threshold, the TXOP is passed silently.	0x0
23:16	RW	CF_END_THRES	CF-END Threshold (unit: 32 us) When the remaining TXOP is greater than the threshold, the CF-END is sent to release the remaining TXOP reserved by long NAV. Set 0xFF to disable CF_END transmission.	0x0
15:8	RW	RDG_IN_THRES	RX RDG Threshold (unit: 32 us) When the remaining TXOP (specified in the duration field of the Rx frame with RDG=1) is greater than or equal to the threshold, the granted reverse direction TXOP may be used.	0x0
7:0	RW	RDG_OUT_THRES	TX RDG Threshold (unit: 32 us) When the remaining TXOP is greater than or equal to the threshold, RDG in the Tx frame may be set to '1'.	0x0

TXOP_CTRL_CFG: (offset: 0x1340)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	0x0
19:16	RW	EXT_CW_MIN	Cwmin for Extension Channel Backoff When EXT_CCA_EN is enabled, 40 Mhz transmission is suppressed to 20 Mhz if the extension CCA is busy or extension channel backoff is not finished. Default: Cwmin=0, disabled.	0x0
15:8	RW	EXT_CCA_DLY	Extension CCA Signal Delay Time (unit: usec) Creates a delayed version of extension CCA signal reference time for extension channel IFS. Default: (ofdm SIFS) + (long slot time) = 16 + 20 = 36 (usec)	0x24
7	RW	EXT_CCA_EN	Extension CCA Reference Enable When transmitting in 40 Mhz mode, transmission is deferred until extension CCA is also clear. 0: Disable 1: Enable	0x0
6	RW	LSIG_TXOP_EN	L-SIG TXOP Protection Enable Extension of mix mode L-SIG protection range to following ACK/CTS.	0x0
5:0	RW	TXOP_TRUN_EN	TXOP Truncation Enable Bit 0: TXOP timeout truncation Bit 1: Truncation for AC change Bit 2: Truncation for TX rate group change Bit 3: Truncation for user TXOP mode Bit 4: Truncation for MIMO power save RTS/CTS Bit 5: Reserved 0: Disable 1: Enable	0x3f

TX_RTS_CFG: (offset: 0x1344)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0x0
24	RW	RTS_FBK_EN	RTS Rate Fallback Enable	0x0
23:8	RW	RTS_THRES	RTS Threshold (unit: 1 byte) MPDU or AMPDU with a length greater than the RTS threshold are protected with RTS/CTS exchange at the beginning of the TXOP.	0xffff
7:0	RW	RTS_RTY_LIMIT	Auto RTS Retry Limit	0x7

TX_TIMEOUT_CFG: (offset: 0x1348)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0x0
23:16	RW	TXOP_TIMEOUT	TXOP Timeout value for TXOP truncation (unit: 1 usec) Default: For 20 us long time slot. NOTE: It is recommended that (SLOT_TIME) > (TXOP_TIMEOUT) > (RX_ACK_TIMEOUT)	0xf
15:8	RW	RX_ACK_TIMEOUT	RX ACK/CTS Timeout Value for Tx procedure (unit: 1 usec) Default: For 20 us long slot time. NOTE: It is recommended that (SLOT_TIME) > (TXOP_TIMEOUT) > (RX_ACK_TIMEOUT)	0xa
7:4	RW	MPDU_LIFE_TIME	Tx MPDU Expiration Time Expiration time = 2^(9+MPDU_LIFE_TIME) us Default value is 2^(9+9) ~= 256 ms	0x9
3:0	-	-	Reserved	0x0

TX_RTY_CFG: (offset: 0x134c)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	0x0
30	RW	TX_AUTOFB_EN	Tx Retry PHY Rate Auto-fallback Enable 0: Disable 1: Enable	0x0
29	RW	AGG_RTY_MODE	Aggregate MPDU Retry Mode 0: Expires according to the retry limit. 1: Expires according to the MPDU life timer.	0x1
28	RW	NAG_RTY_MODE	Non-aggregate MPDU Retry Mode 0: Expiry based on the retry limit 1: Expiry based on the MPDU life timer	0x0
27:16	RW	LONG_RTY_THRES	Long Retry Threshold The long retry limit is appied to MPDU with a length over this threshold.	0xbb8
15:8	RW	LONG_RTY_LIMIT	Long Retry Limit	0x4
7:0	RW	SHORT_RTY_LIMIT	Short Retry Limit	0x7

TX_LINK_CFG: (offset: 0x1350)

Bits	Type	Name	Description	Initial value
31:24	RO	REMOTE_MFS	Remote MCS Feedback Sequence Number	0x7f
23:16	RO	REMOTE_MFB	Remote MCS Feedback	0x7f
15:13	-	-	Reserved	0x0
12	RW	TX_CFACK_EN	Piggyback CF-ACK Enable 0: Disable 1: Enable	0x0

11	RW	TX_RDG_EN	RDG Tx Enable 0: Disable 1: Enable	0x0
10	RW	TX_MRQ_EN	MCS Request Tx Enable 0: Disable 1: Enable	0x0
9	RW	REMOTE_UMFS_EN	Remote Unsolicited MFB Enable 0: Do not apply remote unsolicited MFB (MFS=7). 1: Apply unsolicited MFB.	0x0
8	RW	TX_MFB_EN	Tx Remote MFB Enable 0: Disable 1: Enable	0x0
7:0	RW	REMOTE_MFB_LITETIME	Remote MFB Lifetime (unit: 32 us)	0x20

HT_FBK_CFG0: (offset: 0x1354)

Bits	Type	Name	Description	Initial value
31:28	RW	HT_MCS7_FBK	Auto-fall back MCS when HT MCS =7	0x6
27:24	RW	HT_MCS6_FBK	Auto-fall back MCS when HT MCS =6	0x5
23:20	RW	HT_MCS5_FBK	Auto-fall back MCS when HT MCS =5	0x4
19:16	RW	HT_MCS4_FBK	Auto-fall back MCS when HT MCS =4	0x3
15:12	RW	HT_MCS3_FBK	Auto-fall back MCS when HT MCS =3	0x2
11:8	RW	HT_MCS2_FBK	Auto-fall back MCS when HT MCS =2	0x1
7:4	RW	HT_MCS1_FBK	Auto-fall back MCS when HT MCS =1	0x0
3:0	RW	HT_MCS0_FBK	Auto-fall back MCS when HT MCS =0	0x0

HT_FBK_CFG1: (offset: 0x1358)

Bits	Type	Name	Description	Initial value
31:28	RW	HT_MCS15_FBK	Auto-fallback MCS when HT MCS =15	0xe
27:24	RW	HT_MCS14_FBK	Auto-fallback MCS when HT MCS =14	0xd
23:20	RW	HT_MCS13_FBK	Auto-fallback MCS when HT MCS =13	0xc
19:16	RW	HT_MCS12_FBK	Auto-fallback MCS when HT MCS =12	0xb
15:12	RW	HT_MCS11_FBK	Auto-fallback MCS when HT MCS =11	0xa
11:8	RW	HT_MCS10_FBK	Auto-fallback MCS when HT MCS =10	0x9
7:4	RW	HT_MCS9_FBK	Auto-fallback MCS when HT MCS =9	0x8
3:0	RW	HT_MCS8_FBK	Auto-fallback MCS when HT MCS =8	0x8

NOTE:
1. The MCS is a fallback stopping state, when the fallback MCS is the same as the current MCS.
2. HT Tx PHY rates do not fall back to legacy PHY rates.

LG_FBK_CFG0: (offset: 0x135c)

Bits	Type	Name	Description	Initial value
31:28	RW	OFDM7_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 54 Mbps.	0xe
27:24	RW	OFDM6_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 48 Mbps.	0xd
23:20	RW	OFDM5_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 36 Mbps.	0xc
19:16	RW	OFDM4_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 24 Mbps.	0xb
15:12	RW	OFDM3_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 18 Mbps.	0xa
11:8	RW	OFDM2_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 12 Mbps.	0x9

7:4	RW	OFDM1_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 9 Mbps.	0x8
3:0	RW	OFDM0_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 6 Mbps.	0x8

LG_FBK_CFG1: (offset: 0x1360)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:12	RW	CCK3_FBK	Auto-fallback MCS when the previous Tx rate is CCK 11 Mbps.	0x2
11:8	RW	CCK2_FBK	Auto-fallback MCS when the previous Tx rate is CCK 5.5 Mbps.	0x1
7:4	RW	CCK1_FBK	Auto-fallback MCS when the previous Tx rate is CCK 2 Mbps.	0x0
3:0	RW	CCK0_FBK	Auto-fallback MCS when the previous Tx rate is CCK 1 Mbps.	0x0

NOTE: Bit 3 of each legacy fallback rate indicates a setting of either OFDM or CCK. 0=CCK, 1=OFDM.

CCK_PROT_CFG: (offset: 0x1364)

Bits	Type	Name	Description	Initial value
31:27	-	-	Reserved	0x0
26	RW	CCK_RTSTH_EN	RTS Threshold on CCK Tx Enable 0: Disable 1: Enable	0x0
25:20	RW	CCK_TXOP_ALLOW	CCK TXOP Allowance (0: Disallow, 1: Allow) Bit 20: Allow CCK Tx Bit 21: Allow OFDM Tx Bit 22: Allow MM-20 Tx Bit 23: Allow MM-40 Tx Bit 24: Allow GF-20 Tx Bit 25: Allow GF-40 Tx	0x1
19:18	RW	CCK_PROT_NAV	TXOP Protection Type for CCK Tx 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0x0
17:16	RW	CCK_PROT_CTRL	Protection Control Frame Type for CCK Tx 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0x0
15:0	RW	CCK_PROT_RATE	Protection Control Frame Rate for CCK Tx (Including RTS/CTS-to-self/CF-END) Default: CCK 11M	0x3

OFDM_PROT_CFG: (offset: 0x1368)

Bits	Type	Name	Description	Initial value
31:27	-	-	Reserved	0x0
26	RW	OFDM_RTSTH_EN	RTS Threshold on OFDM Tx Enable 0: Disable 1: Enable	0x0
25:20	RW	OFDM_PROT_TXOP	OFDM TXOP Allowance 0: Disallow 1: Allow Bit 20: Allow CCK Tx. Bit 21: Allow OFDM Tx.	0x2

			Bit 22: Allow MM-20 Tx. Bit 23: Allow MM-40 Tx. Bit 24: Allow GF-20 Tx. Bit 25: Allow GF-40 Tx.	
19:18	RW	OFDM_PROT_NAV	TXOP Protection Type for OFDM Tx 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0x0
17:16	RW	OFDM_PROT_CTRL	Protection Control Frame Type for OFDM Tx 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0x0
15:0	RW	OFDM_PROT_RATE	Protection Control Frame Rate for OFDM Tx (Including RTS/CTS-to-self/CF-END) Default: CCK 11 MHz	0x3

MM20_PROT_CFG: (offset: 0x136c)

Bits	Type	Name	Description	Initial value
31:27	-	-	Reserved	0x0
26	RW	MM20_RTSTH_EN	RTS Threshold on MM20 Tx Enable 0: Disable 1: Enable	0x0
25:20	RW	MM20_PROT_TXOP	MM20 TXOP Allowance 0: Disallow 1: Allow Bit 20: Allow CCK Tx. Bit 21: Allow OFDM Tx. Bit 22: Allow MM-20 Tx. Bit 23: Allow MM-40 Tx. Bit 24: Allow GF-20 Tx. Bit 25: Allow GF-40 Tx.	0x4
19:18	RW	MM20_PROT_NAV	TXOP Protection Type for MM20 Tx 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0x0
17:16	RW	MM20_PROT_CTRL	Protection Control Frame Type for MM20 Tx 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (none)	0x0
15:0	RW	MM20_PROT_RATE	Protection Control Frame Rate for MM20 TX (Including RTS/CTS-to-self/CF-END) Default: OFDM 24M	0x4004

MM40_PROT_CFG: (offset: 0x1370)

Bits	Type	Name	Description	Initial value
31:27	-	-	Reserved	0x0
26	RW	MM40_RTSTH_EN	RTS Threshold on MM40 Tx Enable 0: Disable 1: Enable	0x0
25:20	RW	MM40_PROT_TXOP	MM40 TXOP Allowance	0x8

			0: Disallow 1: Allow Bit 20: Allow CCK Tx. Bit 21: Allow OFDM Tx. Bit 22: Allow MM-20 Tx. Bit 23: Allow MM-40 Tx. Bit 24: Allow GF-20 Tx. Bit 25: Allow GF-40 Tx.	
19:18	RW	MM40_PROT_NAV	TXOP Protection Type for MM40 Tx 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0x0
17:16	RW	MM40_PROT_CTRL	Protection Control Frame Type for MM40 Tx 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0x0
15:0	RW	MM40_PROT_RATE	Protection Control Frame Rate for MM40 Tx (Including RTS/CTS-to-self/CF-END) Default: duplicate OFDM 24 MHx	0x4084

GF20_PROT_CFG: (offset: 0x1374)

Bits	Type	Name	Description	Initial value
31:27	-	-	Reserved	0x0
26	RW	GF20_RTSTH_EN	RTS Threshold on GF20 Tx Enable 0: Disable 1: Enable	0x0
25:20	RW	GF20_PROT_TXOP	GF20 TXOP Allowance 0: Disallow 1: Allow Bit 20: Allow CCK Tx. Bit 21: Allow OFDM Tx. Bit 22: Allow MM-20 Tx. Bit 23: Allow MM-40 Tx. Bit 24: Allow GF-20 Tx. Bit 25: Allow GF-40 Tx.	0x10
19:18	RW	GF20_PROT_NAV	TXOP Protection Type for GF20 Tx 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0x0
17:16	RW	GF20_PROT_CTRL	Protection Control Frame Type for GF20 Tx 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0x0
15:0	RW	GF20_PROT_RATE	Protection Control Frame Rate for GF20 Tx (Including RTS/CTS-to-self/CF-END) Default: OFDM 24 MHz	0x4004

GF40_PROT_CFG: (offset: 0x1378)

Bits	Type	Name	Description	Initial value
31:27	-	-	Reserved	0x0
26	RW	GF40_RTSTH_EN	RTS Threshold on GF40 Tx Enable 0: Disable 1: enable	0x0
25:20	RW	GF40_PROT_TXOP	GF40 TXOP Allowance 0: Disallow 1: Allow Bit 20: Allow CCK Tx. Bit 21: Allow OFDM Tx. Bit 22: Allow MM-20 Tx. Bit 23: Allow MM-40 Tx. Bit 24: Allow GF-20 Tx. Bit 25: Allow GF-40 Tx.	0x10
19:18	RW	GF40_PROT_NAV	TXOP Protection Type for GF40 Tx 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0x0
17:16	RW	GF40_PROT_CTRL	Protection Control Frame Type for GF40 Tx 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0x0
15:0	RW	GF40_PROT_RATE	Protection Control Frame Rate for GF40 Tx (Including RTS/CTS-to-self/CF-END) Default: duplicate OFDM 24 MHz	0x4084

EXP_CTS_TIME: (offset: 0x137c)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	0x0
30:16	RW	EXP_OFDM_CTS_TIME	Expected Time for OFDM CTS Response (unit: 1 us) Used for outgoing NAV setting. Default: SIFS + 6 Mbps CTS	0x38
15	RO		Reserved	0x0
14:0	RW	EXP_CCK_CTS_TIME	Expected Time for CCK CTS Response (unit: 1 us) Used for outgoing NAV setting. Default: SIFS + 1 Mbps CTS	0x13a

EXP_ACK_TIME: (offset: 0x1380)

Bits	Type	Name	Description	Initial value
31	-	-	Reserved	0x0
30:16	RW	EXP_OFDM_ACK_TIME	Expected Time for OFDM ACK Response (unit: 1 us) Used for outgoing NAV setting. Default: SIFS + 6 Mbps ACK preamble	0x24
15	-	-	Reserved	0x0
14:0	RW	EXP_CCK_ACK_TIME	Expected Time for OFDM ACK Response (unit: 1 us) Used for outgoing NAV setting. Default: SIFS + 1 Mbps ACK preamble	0xca

3.21.3.5 MAC Rx Configuration Registers

RX_FILTR_CFG: (offset: 0x1400)

Bits	Type	Name	Description	Initial value

31:17	-	-	Reserved	0x0
16	RW	DROP_CTRL_RSV	Drop Reserve Control Subtype	0x1
15	RW	DROP_BAR	Drop BAR	0x0
14	RW	DROP_BA	Drop BA	0x1
13	RW	DROP_PSPOLL	Drop PS-Poll	0x0
12	RW	DROP_RTS	Drop RTS	0x1
11	RW	DROP_CTS	Drop CT	0x1
10	RW	DROP_ACK	Drop ACK	0x1
9	RW	DROP_CFEND	Drop CF-END	0x1
8	RW	DROP_CFACK	Drop CF-END + CF-ACK	0x1
7	RW	DROP_DUPL	Drop Duplicated Frame	0x1
6	RW	DROP_BC	Drop Broadcast Frame	0x0
5	RW	DROP_MC	Drop Multicast Frame	0x0
4	RW	DROP_VER_ERR	Drop 802.11 Version Error Frame	0x1
3	RW	DROP_NOT_MYBSS	Drop frame that is not my BSSID.	0x1
2	RW	DROP_UC_NOME	Drop Not-to-Me Unicast Frame	0x1
1	RW	DROP_PHY_ERR	Drop Physical Error Frame	0x1
0	RW	DROP_CRC_ERR	Drop CRC Error Frame	0x1

NOTE: 0: Disable, 1: Enable.

AUTO_RSP_CFG: (offset: 0x1404)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	0x0
7	RW	CTRL_PWR_BIT	Control Frame Power Bit Value	0x0
6	RW	BAC_ACK_POLICY	BA Frame -> BAC -> Ack Policy Bit Value	0x0
5	-	-	Reserved	0x0
4	RW	CCK_SHORT_EN	CCK Short Preamble Auto-response Enable 0: Disable 1: Enable	0x0
3	RW	CTS_40M_REF	In Duplicate Legacy CTS Response Mode, refer to extension CCA to decide duplicate or not. 0: Disable 1: Enable	0x0
2	RW	CTS_40M_MODE	Duplicate Legacy CTS Response Mode 0: Disable 1: Enable	0x0
1	RW	BAC_ACKPOLICY_EN	BAC ACK Policy Bit Enable 0: Disable; this bit is ignored. 1: Enable; no BA auto responding upon reception of a BAR with no ACK policy.	0x1
0	RW	AUTO_RSP_EN	Auto-respond Enable	0x1

LEGACY_BASIC_RATE: (offset: 0x1408)

Bits	Type	Name	Description	Initial value
31:12	-	-	Reserved	0x0
11:0	RW	LEGACY_BASIC_RATE	Legacy basic rate bit mask Bit 0: 1 Mbps is the basic rate. Bit 1: 2 Mbps is the basic rate. Bit 2: 5.5 Mbps is the basic rate. Bit 3: 11 Mbps is the basic rate. Bit 4: 6 Mbps is the basic rate. Bit 5: 9 Mbps is the basic rate. Bit 6: 12 Mbps is the basic rate.	0x0

			Bit 7: 18 Mbps is the basic rate. Bit 8: 24 Mbps is the basic rate. Bit 9: 36 Mbps is the basic rate. Bit 10: 48 Mbps is the basic rate. Bit 11: 54 Mbps is the basic rate. 0: Disable 1: Enable	

HT_BASIC_RATE: (offset: 0x140c)

Bits	Type	Name	Description	Initial value
31:16	RW	-	Reserved	0x0
15:0	RW	HT_BASIC_RATE	HT Basic Rate for auto responding control frame Bit 15 =1, enables MCS feedback.	0x0

HT_CTRL_CFG: (offset: 0x1410)

Bits	Type	Name	Description	Initial value
31:9	-	-	Reserved	0x0
8:0	RW	HT_CTRL_THRES	Remaining TXOP Threshold for HT Control Frame auto responding. (unit: us)	0x100

SIFS_COST_CFG: (offset: 0x1414)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:8	RW	OFDM_SIFS_COST	OFDM SIFS Time (unit: 1 us) Applied after OFDM Tx/Rx.	0x10
7:0	RW	CCK_SIFS_COST	CCK SIFS Time (unit: 1 us) Applied after CCK Tx/Rx.	0xa

NOTE: The OFDM_SIFS_COST and CCK_SIFS_COST are used only for duration field calculation. They do not affect the responding timing.

RX_PARSER_CFG: (offset: 0x1418)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
0	RW	NAV_ALL_EN	NAV for All Received Frames Enable 0: Disable (unicast to me frame does not set the NAV). 1: Enable	0x0

3.21.3.6 MAC Security Configuration Registers

TX_SEC_CNT0: (offset: 0x1500)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_SEC_ERR_CNT	Tx SEC Packet Error Count	0x0
15:0	RC	TX_SEC_CPL_CNT	Tx SEC Packet Complete Count	0x0

RX_SEC_CNT0: (offset: 0x1504)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:0	RC	RX_SEC_CPL_CNT	Rx SEC Packet Complete Count	0x0

CCMP_FC_MUTE: (offset: 0x1508)

Bits	Type	Name	Description	Initial value
31:16	RW	HT_CCMP_FC_MUTE	HT Rate CCMP FC Mute	0xc78f
15:0	RW	LG_CCMP_FC_MUTE	Legacy Rate CCMP FC Mute	0xc78f

3.21.3.7 MAC HCCA/PSMP CSR

TXOP_HLDR_ADDR0: (offset: 0x1600)

Bits	Type	Name	Description	Initial value
31:24	RW	TXOP_HOL_3	TXOP Holder MAC Address Byte 3	0x0
23:16	RW	TXOP_HOL_2	TXOP Holder MAC Address Byte 2	0x0
15:8	RW	TXOP_HOL_1	TXOP Holder MAC Address Byte 1	0x0
7:0	RW	TXOP_HOL_0	TXOP Holder MAC Address Byte 0	0x0

TXOP_HLDR_ADDR1: (offset: 0x1604)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	0x0
15:8	RW	TXOP_HOL_5	TXOP Holder MAC Address Byte 5	0x0
7:0	RW	TXOP_HOL_4	TXOP Holder MAC Address Byte 4	0x0

NOTE: Byte 0 is the first byte on network. Its LSB bit is the first bit on network. For a MAC address captured on the network with order 00:01:02:03:04:05, byte 0=00, byte 1=01 etc.

TXOP_HLDR_ET: (offset: 0x1608)

Bits	Type	Name	Description	Initial value
31:26	-	-	Reserved	0x0
25	RW	TXOP_ETM1_EN	TXOP Holder Early Termination Interrupt Enable (Type 1) Upon receipt of a QoS data frame from TXOP_HLDR_ADDR (A2) and when the queue size (QS) in the QOS control field (QC) is equal to zero, the TXOP holder early termination interrupt is issued. 0: Disable 1: Enable	0x0
24	RW	TXOP_ETM0_EN	TXOP Holder Early Termination Interrupt Enable (Type 0). When the Rx packet is from the TXOP holder specified in QOS_CSR0,1 (matched with Addr2) and the duration value is less than or equal to the early termination duration threshold specified below, the TXOP holder early termination interrupt is issued after the CRC check is ok. Upon receipt of a QoS data frame from TXOP_HLDR_ADDR (A2) and duration (DUR) is less than or equal to the early termination duration threshold (TXOP_ETM_THRES), the TXOP holder early termination interrupt is issued. 0: Disable 1: Enable	0x0
23:16	RW	TXOP_ETM_THRES	TXOP Early Termination Duration Threshold (unit: 1 usec)	0x0
15:9	-	-	Reserved	0x0
8	WC	TXOP_ETO_EN	TXOP Holder Early Timeout Enable Write '1' to enable early timeout check (interrupt when timed out). When enabled, hardware expects a CCA event. If hardware does not sense CCA over the TXOP holder early timeout threshold (TXOP_ETO_THRES), the TXOP holder early timeout interrupt is then issued.	0x0
7:1	RW	TXOP_ETO_THRES	TXOP Holder Early Timeout Threshold (unit: 1 usec)	0x0
0	RW	PER_RX_RST_EN	Baseband RX_PE per Rx Reset Enable 0: Disable 1: Enable	0x0

NOTE:
1. TXOP holder early timeout interrupt (TXOP_ETO_INT) is used by AP for HC purpose.

2. TXOP holder early termination interrupt (TXOP_ETM_INT) is used by STA (both AP and non-AP STA) for HC purpose.

QOS_CFPOLL_RA_DW0: (offset: 0x160c)

Bits	Type	Name	Description	Initial value
31:24	RO	CFPOLL_A1_BYTE3	Byte 3 of A1 of Received QoS Data (+) CF-Poll frame	0x0
23:16	RO	CFPOLL_A1_BYTE2	Byte 2 of A1 of Received QoS Data (+) CF-Poll frame	0x0
15:8	RO	CFPOLL_A1_BYTE1	Byte 1 of A1 of Received QoS Data (+) CF-Poll frame	0x0
7:0	RO	CFPOLL_A1_BYTE0	Byte 0 of A1 of Received QoS Data (+) CF-Poll frame	0x0

QOS_CFPOLL_A1_DW1: (offset: 0x1610)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0x0
16	RO	CFPOLL_A1_TOME	0: Qos CF-Poll Not To Me 1: QoS CF-Poll To Me	0x0
15:8	RO	CFPOLL_A1_BYTE5	Byte 5 of A1 of Received QoS Data (+) CF-Poll frame	0x0
7:0	RO	CFPOLL_A1_BYTE4	Byte 4 of A1 of Received QoS Data (+) CF-Poll frame	0x0

QOS_CFPOLL_QC: (offset: 0x1614)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	0x0
15:8	RO	CFPOLL_QC_BYTE1	Byte 1 of QC of Received QoS Data (+) CF-Poll frame	0x0
7:0	RO	CFPOLL_QC_BYTE0	Byte 0 of QC of Received QoS Data (+) CF-Poll frame	0x0

NOTE: CFPOLL_RA_DW0, CFPOLL_RA_DW1, and CFPOLL_QC are updated after the reception of a QoS Data (+) CF-Poll frame and the Rx QoS CF-Poll interrupt (RX_QOS_CFPOLL_INT) is launched then.

3.21.3.8 MAC Statistics Counters

RX_STA_CNT0: (offset: 0x1700)

Bits	Type	Name	Description	Initial value
31:16	RC	PHY_ERRCNT	Rx PHY Error Frame Count	0x0
15:0	RC	CRC_ERRCNT	Rx CRC Error Frame Count	0x0

NOTE:
1. Rx PHY error means PSDU length is shorter than indicated by PLCP.
2. Rx PHY error is also treated as a CRC error.

RX_STA_CNT1: (offset: 0x1704)

Bits	Type	Name	Description	Initial value
31:16	RC	PLPC_ERRCNT	RX PLCP Error Count	0x0
15:0	RC	CCA_ERRCNT	CCA False Alarm count	0x0

NOTE:
1. CCA false alarm means there is no PLCP after CCA indication.
2. RX PLCP error means there is no PSDU after PLCP indication.

RX_STA_CNT2: (offset: 0x1708)

Bits	Type	Name	Description	Initial value
31:16	RC	RX_OVFL_CNT	Rx FIFO Overflow Frame Count	0x0
15:0	RC	RX_DUPL_CNT	Rx Duplicated Filtered Frame Count	0x0

NOTE: MAC does NOT auto respond ACK/BA to the frame originator when frame is lost due to RXFIFO overflow. However, MAC responds when the frame is duplicated filtered.

TX_STA_CNT0: (offset: 0x170c)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_BCN_CNT	Tx Beacon Count	0x0

15:0	RC	TX_FAIL_CNT	Failed Tx Count	0x0

TX_STA_CNT1: (offset: 0x1710)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_RTY_CNT	Tx retransmission count	0x0
15:0	RC	TX_SUCC_CNT	Successful Tx count	0x0

TX_STA_CNT2: (offset: 0x1714)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_UDFL_CNT	Tx Underflow Count	0x0
15:0	RC	TX_ZERO_CNT	Tx Zero Length Frame Count	0x0

TX_STAT_FIFO: (offset: 0x1718)

Bits	Type	Name	Description	Initial value
31:16	RO	TXQ_RATE	Tx Success Rate	0x0
15:8	RO	TXQ_WCID	Tx WCID Indicates the wireless client ID.	0x0
7	RO	TXQ_ACKREQ	Tx Acknowledge Required 0: Not required 1: Required	0x0
6	RO	TXQ_AGG	Tx Aggregate 0: Non-aggregated 1: Aggregated	0x0
5	RO	TXQ_OK	Tx Success 0: Failed 1: Success	0x0
4:1	RO	TXQ_PID	Tx Packet ID (Latched from TXWI)	0x0
0	RC	TXQ_VLD	Tx Status Queue Valid 0: Queue empty 1: Valid	0x0

NOTE: Tx status FIFO size = 16.

TX_NAG_AGG_CNT: (offset: 0x171c)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_CNT	Aggregate Tx Count	0x0
15:0	RC	TX_NAG_CNT	Non-aggregate Tx Count	0x0

TX_AGG_CNT0: (offset: 0x1720)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_2_CNT	Aggregate size = 2 MPDU count	0x0
15:0	RC	TX_AGG_1_CNT	Aggregate size = 1 MPDU count	0x0

TX_AGG_CNT1: (offset: 0x1724)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_4_CNT	Aggregate size = 4 MPDU count	0x0
15:0	RC	TX_AGG_3_CNT	Aggregate size = 3 MPDU count	0x0

TX_AGG_CNT2: (offset: 0x1728)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_6_CNT	Aggregate size = 6 MPDU count	0x0
15:0	RC	TX_AGG_5_CNT	Aggregate size = 5 MPDU count	0x0

TX_AGG_CNT3: (offset: 0x172c)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_8_CNT	Aggregate size = 8 MPDU count	0x0
15:0	RC	TX_AGG_7_CNT	Aggregate size = 7 MPDU count	0x0

TX_AGG_CNT4: (offset: 0x1730)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_10_CNT	Aggregate size = 10 MPDU count	0x0
15:0	RC	TX_AGG_9_CNT	Aggregate size = 9 MPDU count	0x0

TX_AGG_CNT5: (offset: 0x1734)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_12_CNT	Aggregate size = 12 MPDU count	0x0
15:0	RC	TX_AGG_11_CNT	Aggregate size = 11 MPDU count	0x0

TX_AGG_CNT6: (offset: 0x1738)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_14_CNT	Aggregate size = 14 MPDU count	0x0
15:0	RC	TX_AGG_13_CNT	Aggregate size = 13 MPDU count	0x0

TX_AGG_CNT7: (offset: 0x173c)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_16_CNT	Aggregate size > 16 MPDU count	0x0
15:0	RC	TX_AGG_15_CNT	Aggregate size = 15 MPDU count	0x0

MPDU_DENSITY_CNT: (offset: 0x1740)

Bits	Type	Name	Description	Initial value
31:16	RC	RX_ZERO_DEL_CNT	Rx Zero Length Delimiter Count	0x0
15:0	RC	TX_ZERO_DEL_CNT	Tx Zero Length Delimiter Count	0x0

3.21.3.9 MAC Search Table (base: 0x1018_0000, offset: 0x1800)

Rx WCID Search Entry Format (8 bytes)

Offset	Type	Name	Description	Initial value
0x00	RW	WC_MAC_ADDR0	Client MAC Address Byte 0	0x0
0x01	RW	WC_MAC_ADDR1	Client MAC Address Byte 1	0x0
0x02	RW	WC_MAC_ADDR2	Client MAC Address Byte 2	0x0
0x03	RW	WC_MAC_ADDR3	Client MAC Address Byte 3	0x0
0x04	RW	WC_MAC_ADDR4	Client MAC Address Byte 4	0x0
0x05	RW	WC_MAC_ADDR5	Client MAC Address Byte 5	0x0
0x06	RW	BA_SESS_MASK0	BA Session Mask (lower) Bit 0 for TID0 Bit 7 for TID7	0x0
0x07	RW	BA_SESS_MASK1	BA Session Mask (upper) Bit 8 for TID8 Bit 15 for TID15	0x0

Rx WCID Search Table (offset:0x1800)

Offset	Type	Name	Description	Initial value
0x1800	RW	WC_ENTRY_0	WC MAC Address with WCID=0	0x0
0x1808	RW	WC_ENTRY_1	WC MAC Address with WCID=1	0x0
….	RW	….	WC MAC Address with WCID=2~253	0x0

0x1FF0	RW	WC_ENTRY_254	WC MAC Address with WCID=254	0x0
0x1FF8	RW	WC_ENTRY_255	Reserved (shall not be used)	0x0

NOTE: WCID=Wireless Client ID

3.21.3.10 Security table/CIS/Beacon/NULL frame (base : 1018_0000, offset: 0x4000)

3.21.4 Security Key Format (8DW)

Offset	Type	Name	Description	Initial value
0x00	RW	SECKEY_DW0	Security Key Byte 3~0	*
0x04	RW	SECKEY_DW1	Security Key Byte 7~4	*
0x08	RW	SECKEY_DW2	Security Key Byte 11~8	*
0x0C	RW	SECKEY_DW3	Security key Byte 15~12	*
0x10	RW	TXMIC_DW0	Tx MIC Key Byte 3~0	*
0x14	RW	TXMIC_DW1	Tx MIC Key Byte 7~4	*
0x18	RW	RXMIC_DW0	Rx MIC Key Byte 3~0	*
0x1C	RW	RXMIC_DW1	Rx MIC Key Byte 7~4	*

NOTE:
1. For WEP40, CKIP40, only bytes 4~0 of the security key are valid.
2. For WEP104, CKIP104, only byte12~0 of the security key are valid.
3. For TKIP, AES, all the bytes of the security key are valid.
4. Tx/Rx MIC key is used only for TKIP MIC calculation.

3.21.5 IV/EIV Format (2 DW)

When TXINFO.WIV=0, hardware automatically look up IV/EIV from this table and update IV/EIV after encryption is finished.

Offset	Type	Name	Description	Initial value
0x00	RW	IV_FIELED	IV Field	*
0x04	RW	EIV_FIELED	EIV Field	*

NOTE:
1. The key index and extension IV bit are initialized by software. The MSB octet of IV is not modified by hardware.
2. IV/EIV packet number (PN) counter modes:
   2.1. For WEP40, WEP104, CKIP40, CKIP104, CKIP128 mode, PN=IV[23:0]. EIV[31:0] is not used.
   2.2. For TKIP mode, PN = {EIV[31:0], IV[7:0], IV[23:16]}, IV[15:8]=(IV[7:0] | 0x20) & 0x7f) is generated by hardware.
   2.3. For AES-CCMP, PN = {EIV[31:0], IV[15:0]}.
   2.4. PN = PN + 1 after each encryption.
3. Software may initialize the PN counter to any value.

3.21.6 WCID Attribute Entry Format (1DW)

Offset	Type	Name	Description	Initial value
31:10	-	-	Reserved	*
9:7	RW	RXWI_UDF	RXWI User Defined Field This field is tagged in the RXWI.UDF fields for the WCID.	*
6:4	RW	BSS_IDX	Multiple-BSS index for the WCID	*
3:1	RW	RX_PKEY_MODE	Pairwise Key Security Mode 0: No security 1: WEP40 2: WEP104 3: TKIP 4: AES-CCMP 5: CKIP40 6: CKIP104	*

			7: CKIP128	
0	RW	RX_PKEY_EN	Key Table Selection 0: Shared key table 1: Pairwise key table	*

3.21.7 Shared Key Mode Entry Format (1DW)

Bits	Type	Name	Description	Initial Value
31	-	-	Reserved	*
30:28	RW	SKEY_MODE_7+	Shared Key7+(8x) Mode, x=0~3	*
27	-	-	Reserved	*
26:24	RW	SKEY_MODE_6+	Shared Key6+(8x) Mode, x=0~3	*
23	-	-	Reserved	*
22:20	RW	SKEY_MODE_5+	Shared Key5+(8x) Mode, x=0~3	*
19	-	-	Reserved	*
18:16	RW	SKEY_MODE_4+	Shared Key4+(8x) Mode, x=0~3	*
15	-	-	Reserved	*
14:12	RW	SKEY_MODE_3+	Shared Key3+(8x) Mode, x=0~3	*
11	-	-	Reserved	*
10:8	RW	SKEY_MODE_2+	Shared Key2+(8x) Mode, x=0~3	*
7	-	-	Reserved	*
6:4	RW	SKEY_MODE_1+	Shared Key1+(8x) Mode, x=0~3	*
3	-	-	Reserved	*
2:0	RW	SKEY_MODE_0+	Shared Key0+(8x) Mode, x=0~3	*

Key mode definition:
0: No security
1: WEP40
2: WEP104
3: TKIP
4: AES-CCMP
5: CKIP40
6: CKIP104
7: CKIP128

3.21.7.1 Security Tables

Pair-wise Key Table (offset: 0x4000)

Offset	Type	Name	Description	Initial value
0x4000	RW	PKEY_0	Pairwise Key for WCID0	*
0x4020	RW	PKEY_1	Pairwise Key for WCID1	*
….	RW	….	Pairwise key for WCID2~253	*
0x5FC0	RW	PKEY_254	Pairwise key for WCID254	*
0x5FE0	RW	PKEY_255	Pairwise key for WCID255 (not used)	*

IV/EIV Table (offset:0x6000)

Offset	Type	Name	Description	Initial value
0x6000	RW	IVEIV_0	IV/EIV for WCID0	*
0x6008	RW	IVEIV_1	IV/EIV for WCID1	*
….	RW	….	IV/EIV for WCID2~253	*
0x67F0	RW	IVEIV_254	IV/EIV for WCID254	*
0x67F8	RW	IVEIV_255	IV/EIV for WCID255 (not used)	*

WCID Attribute Table (offset:0x6800)

Offset	Type	Name	Description	Initial value
0x6800	RW	WCID_ATTR_0	WCID Attribute for WCID0	*

0x6804	RW	WCID_ATTR_1	WCID Attribute for WCID1	*
….	RW	….	WCID Attribute for WCID2~253	*
0x6BF8	RW	WCID_ATTR_254	WCID Attribute for WCID254	*
0x6BFC	RW	WCID_ATTR_255	WCID Attribute for WCID255	*

Shared Key Table (offset:0x6C00)

Offset	Type	Name	Description	Initial value
0x6C00	RW	SKEY_0	Shared Key for BSS_IDX=0, KEY_IDX=0	*
0x6C20	RW	SKEY_1	Shared Key for BSS_IDX=0, KEY_IDX=1	*
0x6C40	RW	SKEY_2	Shared Key for BSS_IDX=0, KEY_IDX=2	*
0x6C60	RW	SKEY_3	Shared Key for BSS_IDX=0, KEY_IDX=3	*
0x6C80	RW	SKEY_4	Shared Key for BSS_IDX=1, KEY_IDX=0	*
0x6CA0	RW	SKEY_5	Shared Key for BSS_IDX=1, KEY_IDX=1	*
0x6CC0	RW	SKEY_6	Shared Key for BSS_IDX=1, KEY_IDX=2	*
0x6CE0	RW	SKEY_7	Shared Key for BSS_IDX=1, KEY_IDX=3	*
0x6D00	RW	SKEY_8	Shared Key for BSS_IDX=2, KEY_IDX=0	*
0x6D20	RW	SKEY_9	Shared Key for BSS_IDX=2, KEY_IDX=1	*
0x6D40	RW	SKEY_10	Shared Key for BSS_IDX=2, KEY_IDX=2	*
0x6D60	RW	SKEY_11	Shared Key for BSS_IDX=2, KEY_IDX=3	*
0x6D80	RW	SKEY_12	Shared Key for BSS_IDX=3, KEY_IDX=0	*
0x6DA0	RW	SKEY_13	Shared Key for BSS_IDX=3, KEY_IDX=1	*
0x6DC0	RW	SKEY_14	Shared Key for BSS_IDX=3, KEY_IDX=2	*
0x6DE0	RW	SKEY_15	Shared Key for BSS_IDX=3, KEY_IDX=3	*
0x6E00	RW	SKEY_16	Shared Key for BSS_IDX=4, KEY_IDX=0	*
0x6E20	RW	SKEY_17	Shared Key for BSS_IDX=4, KEY_IDX=1	*
0x6E40	RW	SKEY_18	Shared Key for BSS_IDX=4, KEY_IDX=2	*
0x6E60	RW	SKEY_19	Shared Key for BSS_IDX=4, KEY_IDX=3	*
0x6E80	RW	SKEY_20	Shared Key for BSS_IDX=5, KEY_IDX=0	*
0x6EA0	RW	SKEY_21	Shared Key for BSS_IDX=5, KEY_IDX=1	*
0x6EC0	RW	SKEY_22	Shared Key for BSS_IDX=5, KEY_IDX=2	*
0x6EE0	RW	SKEY_23	Shared Key for BSS_IDX=5, KEY_IDX=3	*
0x6F00	RW	SKEY_24	Shared Key for BSS_IDX=6, KEY_IDX=0	*
0x6F20	RW	SKEY_25	Shared Key for BSS_IDX=6, KEY_IDX=1	*
0x6F40	RW	SKEY_26	Shared Key for BSS_IDX=6, KEY_IDX=2	*
0x6F60	RW	SKEY_27	Shared Key for BSS_IDX=6, KEY_IDX=3	*
0x6F80	RW	SKEY_28	Shared Key for BSS_IDX=7, KEY_IDX=0	*
0x6FA0	RW	SKEY_29	Shared Key for BSS_IDX=7, KEY_IDX=1	*
0x6FC0	RW	SKEY_30	Shared Key for BSS_IDX=7, KEY_IDX=2	*
0x6FE0	RW	SKEY_31	Shared Key for BSS_IDX=7, KEY_IDX=3	*

Shared Key Mode (offset: 0x7000)

Offset	Type	Name	Description	Initial value
0x7000	RW	SKEY_MODE_0_7	Shared mode for SKEY0-SKEY7	*
0x7004	RW	SKEY_MODE_8_15	Shared mode for SKEY8-SKEY15	*
0x7008	RW	SKEY_MODE_16_23	Shared mode forSKEY16-SKEY23	*
0x700C	RW	SKEY_MODE_24_31	Shared mode for SKEY24-SKEY31	*

3.21.8 Descriptor and Wireless information

3.21.8.1 Tx Frame Information

To transmit a frame, the driver needs to prepare the Tx frame information for hardware. The Tx frame information contains the transmission control, the header, and the payload. The transmission control information (the TXWI) is used by the MAC and BBP and is applied to the associated Tx frame on transmission. The header and payload is the content of an 802.11 packet.

The Tx information could be scattered across several segments. The TX descriptor (the TXD) specifies the location and length of the Tx frame information segment. Tx frame information could be linked by use of several TXD. These TXD are arranged in a TXD ring in serial. The diagram below illustrates the linking between TXD and Tx frame information.

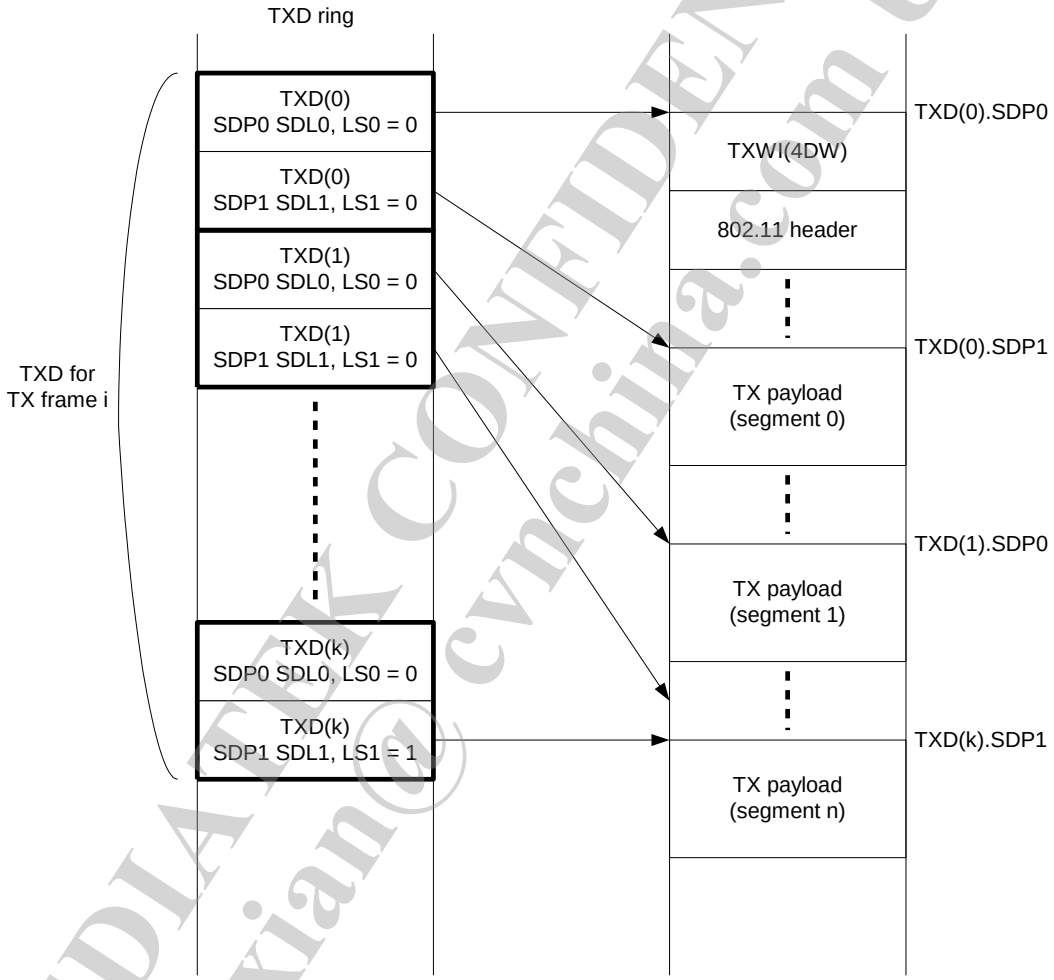


Figure 3-34 Tx Frame Information

3.21.8.2 Tx Descriptor Format

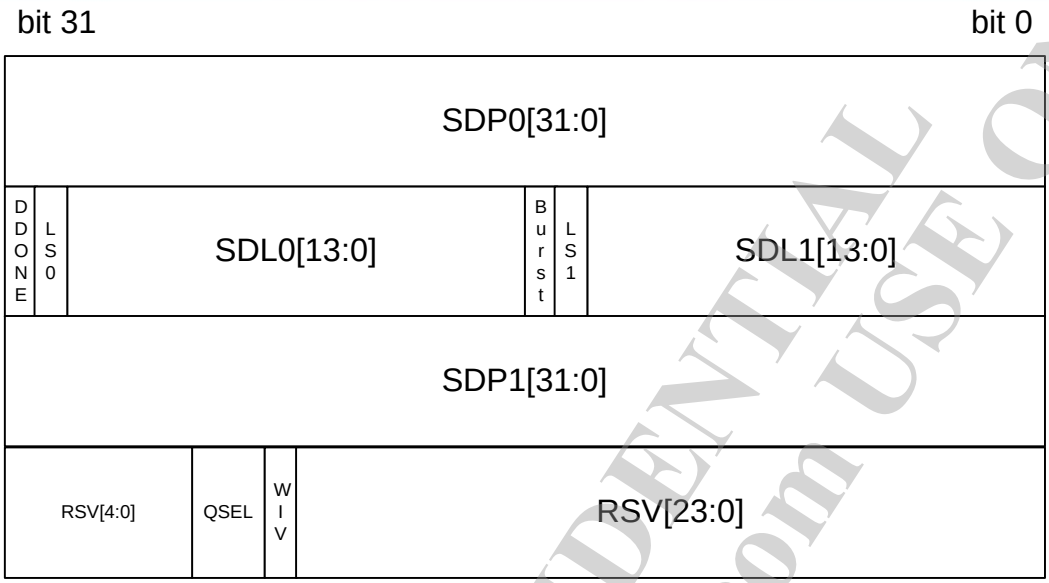


Figure 3-35 Tx Descriptor Format

- SDP0: Segment Data Pointer 0.
- SDL0: Segment Data Length for the data pointed to by SDP0.
- SDP1: Segment Data Pointer 1.
- SDL1: Segment Data Length for the data pointed to by SDP1.
- LS0: Data pointed to by SDP0 is the last segment.
- LS1: Data pointed to by SDP1 is the last segment.
- DDONE (DMA Done) The DMA has transferred the segments pointed to by this Tx descriptor.
- Burst: Forces the DMA to access the next Tx frame from the same queue.
- QSEL: The ID of the on-chip queue that the Tx frame is moved into.
- 0: MGMT queue
- 1: HCCA queue
- 2: EDCA queue
- 3: Unused.
- WIV:
- 0: Driver has prepared only the first 8-byte TXWI.
- 1: Driver has prepared all of the 16-byte TXWI.

3.21.8.3 TXWI Format

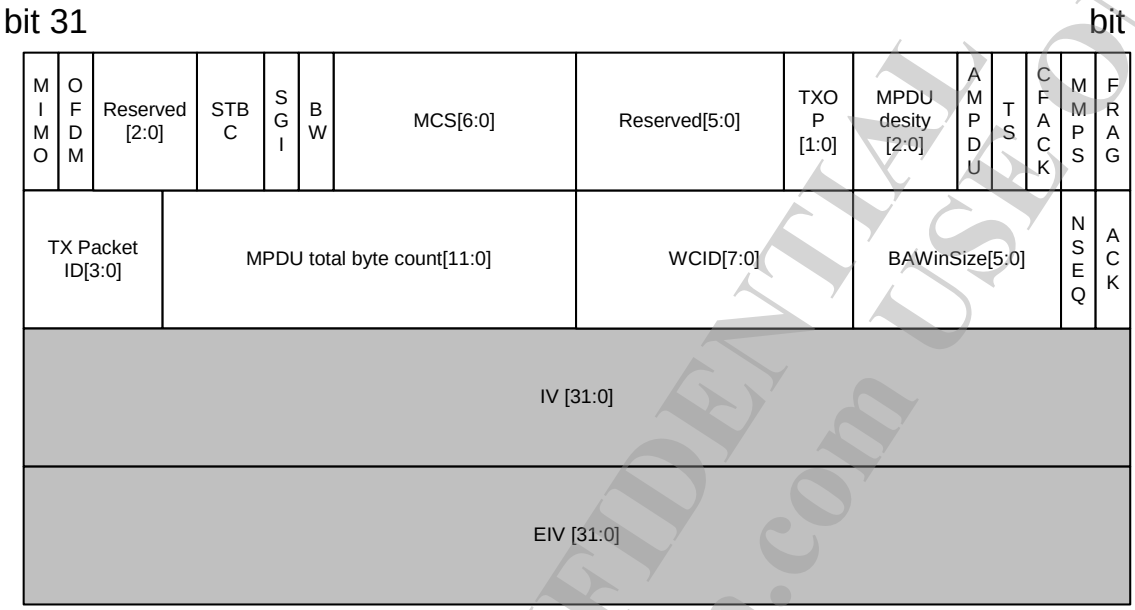


Figure 3-36 TXWI Format

- FRAG: 1: Informs the TKIP engine this is a fragment, so that TKIP MIC is appended by the driver to the last fragment; hardware TKIP engine only needs to insert IV/EIV and ICV.
- MMPS: 1: The remote peer is in dynamic MIMO-PS mode.
- CFACK: 1: If an ACK is required to the same peer as this outgoing DATA frame, then MAC Tx sends a single DATA+CFACK frame instead of a separate ACK and DATA frames.
- 0: No piggyback ACK allowed for the RA of this frame.
- TS: 1: This is a Beacon or ProbeResponse frame and MAC needs to auto insert an 8-byte timestamp after the 802.11 WLAN header.
- AMPDU: This frame is eligible for AMPDU. MAC Tx aggregates subsequent outgoing frames having <same RA, same TID, AMPDU=1> whenever TXOP allows. Even if there is only one DATA frame to be sent, as long as the AMPDU bit in TXWI is ON, MAC still packages it as an AMPDU with an implicit BAR. This adds only a 4-byte AMPDU delimiter overhead into the outgoing frame and implies the response frame is a BA instead of ACK.
- NOTE: The driver should set AMPDU=1 only after a BA session is successfully negotiated, because block ACK is the only way to acknowledge in the case of AMPDUs.
- MPDU density: ¼ usec ~ 16 usec per-peer parameter used in outgoing A-MPDU. This field complies with the “Minimum MDPU Starting Spacing” of the A-MPDU parameter field of draft 1.08.
  000- no restriction
  001- 1/4 µsec
  010- 1/2 µsec
  011- 1 µsec
  100- 2 µsec
  101- 4 µsec
  110- 8 µsec
  111- 16 µsec
- TXOP: Tx back off mode.
  0: HT TXOP rule
  1: PIFS Tx
  2: SIFS (only when the previous frame exchange is successful)
  3: Back off.
- MCS/BW/ShortGI/OFDM/MIMO: Tx data rate and MIMO parameters for this outgoing frame to be filled into BBP.

- ACK: This bit informs MAC to wait for ACK or not after transmission of the frame. Even though QOD DATA frame has an ACK policy in its QOS CONTROL field, MAC Tx solely depends on this ACK bit to decide whether to wait for ACK or not.
- NSEQ: 1: Informs the MAC to use the special H/W SEQ number register in the MAC block.
- BA window size: Tells the MAC the maximum number of to-be-BAed frames allowed by the RA (RA's BA re-ordering buffer size).
- WCID (Wireless Client Index): Lookup result of ADDR1 in the peer table (255=not found). This index is also used to find all the attributes of the wireless peer (e.g. Tx rate, Tx power, pairwise KEY, IV, EIV,). This index has consistent meaning in both driver and hardware.
- MSDU total byte count: Total length of this frame.
- Packet ID: Sets an identification number for a packet specified by the driver which is latched into the Tx result register stack. The driver uses this field to identify the Tx results of a particular frame.
- IV: Used by the encryption engine.
- EIV: Used by the encryption engine.

3.21.8.4 Rx Descriptor Ring

The Rx descriptor (the RXD) specifies the location to place the payload of the received frame (the Rx payload) and the associated receiving information (the RXWI). One RXD serves for one receiving frame. Only SDP0 and SDL0 are useful in the RXD. The RXD is arranged in the RXD ring in serial. The hardware links the RXWI and Rx payload in serial and places it in the location specified in SDP0. See the diagram below.

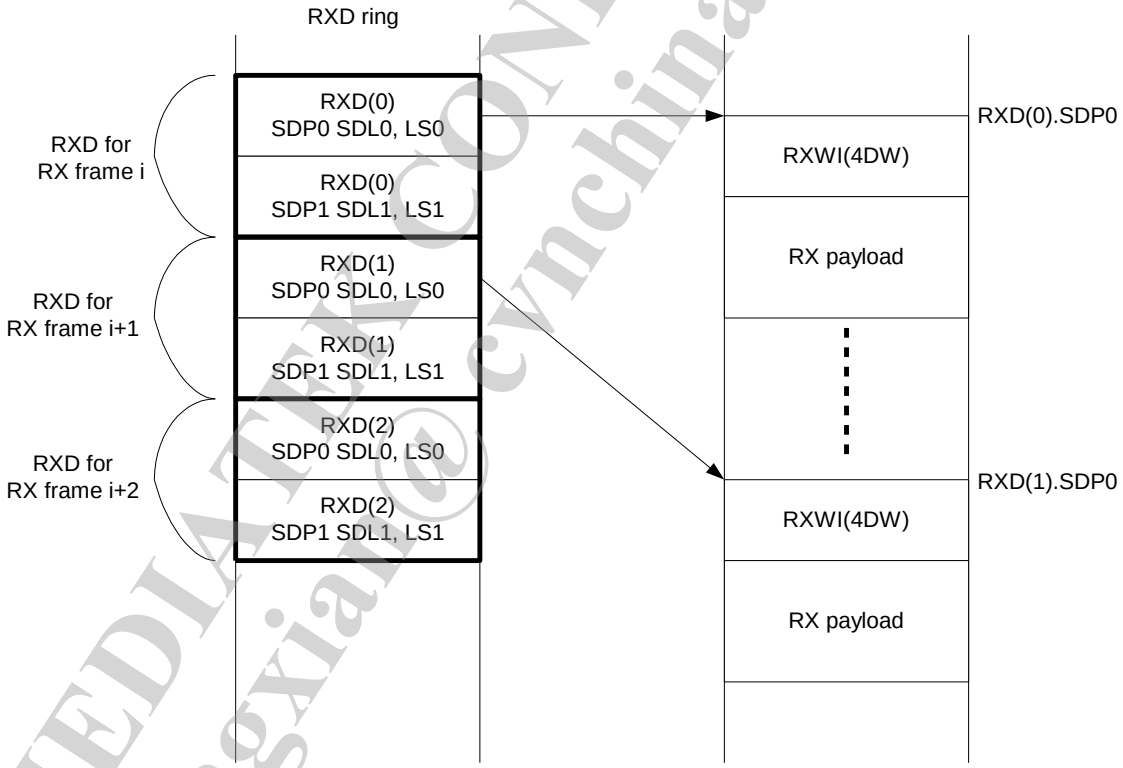


Figure 3-37 Rx Descriptor Ring

3.21.8.5 RX Descriptor Format

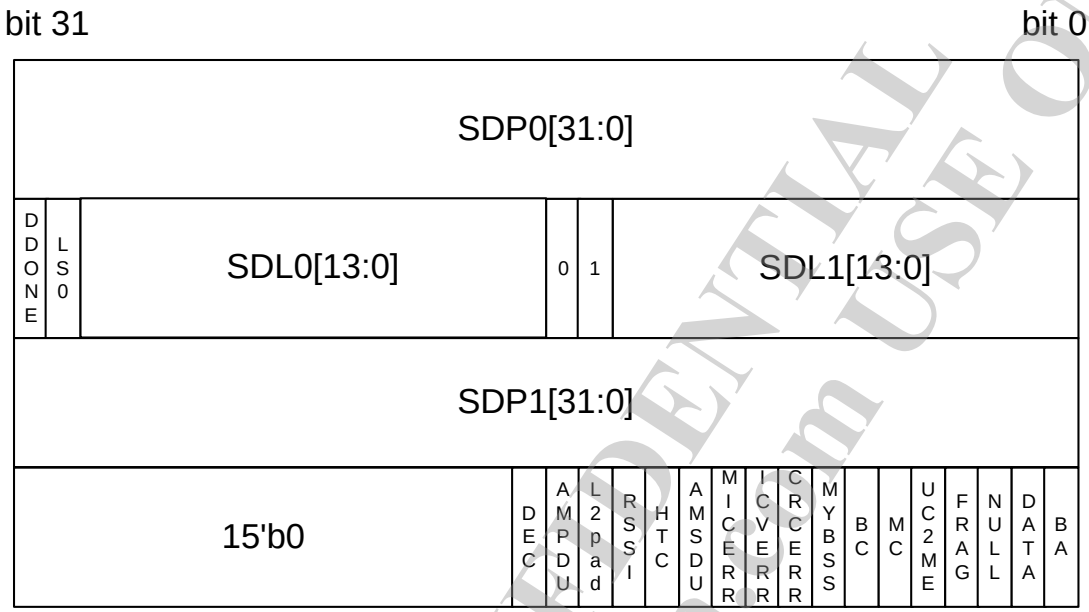


Figure 3-38 Rx Descriptor Format

The following fields are driver-specified.

- SDP0: Segment Data Pointer 0.
- SDL0: Segment Data Length for the data pointed to by SDP0.
- SDP1: Segment Data Pointer 1.
- SDL1: Segment Data Length for the data pointed to by SDP1.
- DDONE (DMA done): DMA has moved the Rx frame to the specified location. Set by hardware and cleared by driver.

The following fields are filled by hardware.

- BA: The received frame is part of BA session, so re-ordering is required.
- DATA: 1: The received frame is DATA type.
- NULL: 1: The received frame has sub-type NULL/QOS-NULL.
- FRAG: 1: The receive frame is a fragment.
- UC2ME: 1: The received frame ADDR1 = my MAC address.
- MC: 1: The received frame ADDR1 = multicast.
- BC: 1: The received frame ADDR1 = ff:ff:ff:ff:ff:ff.
- MyBSS: 1: The received frame BSSID is one of my BSS (as an AP, max 4 BSSID supported).
- CRC error: 1: The received frame has a CRC error.
- ICV error: 1: The received frame has a ICV error.
- MIC error: 1: The received frame has a MIC error (Rx CNRL register should support individual pass-up of the error frame to the driver in order to implement the MIC error detection feature).
- AMSDU: The received frame is in A-MSDU sub frame format which is <802.3 + MSDU + padding>.
- HTC: 1: This received frame came with an HTC field, 0: No HTC field.
- RSSI: 1: RSSI information is available in RSSI0, RSSI1, RSSI2 fields.
- L2Pad: 1: The L2 header is recognizable and is 2-byte-padded to ensure payloads aligns at 4-byte boundary. 0: L2 header not extra padded.
- AMPDU: 1: This is an AMPDU segregated frame.
- DEC: 1: This is a decrypted frame.

3.21.8.6 RXWI Format

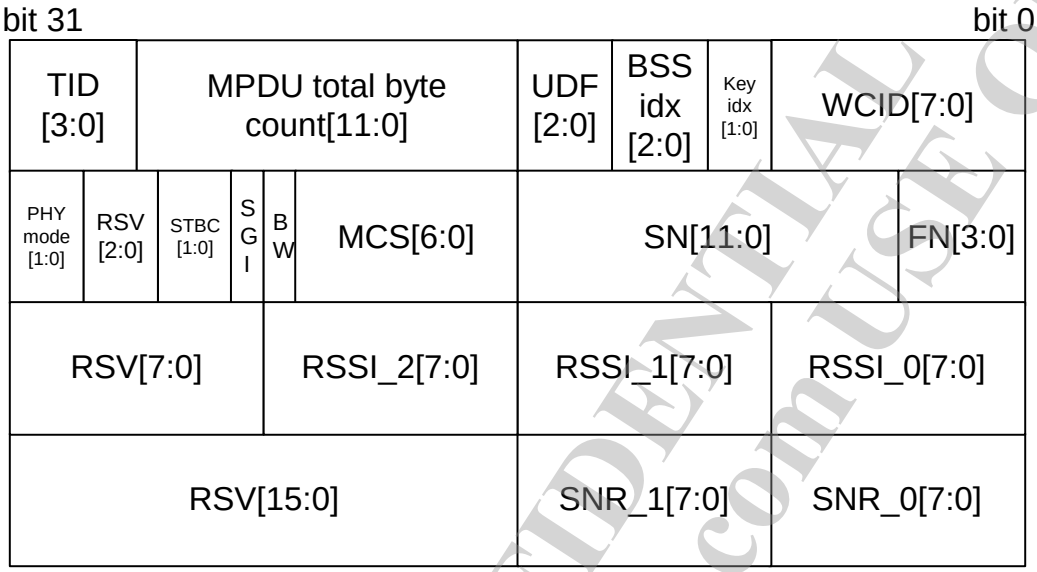


Figure 3-39 RXWI Format

- WCID: The index of ADDR2 in the pairwise KEY table. This value uniquely identifies the TA. WCID=255 means the TA is not found.
- KEY Index: 0~3 are extracted from the IV field. For driver reference only, no particular usage so far.
- BSSID index: 0~7 for BSSID0~7. Extracted from the 802.11 header (the last three bits of BSSID field).
- UDF: User Defined Field.
- MPDU total byte count: The entire MPDU length.
- TID: Extracted from 8002.11 QoS control field.
- FN: Fragment number of the received MPDU. Extracted from the 802.11 header.
- SN: Sequence number of the received MPDU. Used for BA re-ordering especially when AMSDU are auto-segregated by hardware and have lost the 802.11 header.
- MCS/BW/SGI/PHYmode: Rx data rate and related MIMO parameters of this frame are obtained from PLCP header. See next section for the details.
- RSSI0, RSSI1, RSSI2: BBP reported RSSI information of the received frame.
- SNR0, SNR1: BBP reported SNR information of the received frame.

3.21.8.7 Brief PHY Rate Format and Definition

A 16-bit brief PHY rate is used in MAC hardware. It is the same PHY rate field as that described in TXWI and RXWI.

Bit	Name	Description
15:14	PHY MODE	Preamble Mode 0: Legacy CCK 1: Legacy OFDM 2: HT mix mode 3: HT green field
13:11	-	Reserved
10:9	-	Reserved
8	SGI	Short Guard Interval, only support for HT mode 0: 800 ns 1: 400 ns

7	BW	Bandwidth Supports both legacy and HT modes. 40 Mhz in legacy mode means duplicate legacy. 0: 20 Mhz 1: 40 Mhz
6:0	MCS	Modulation Coding Scheme

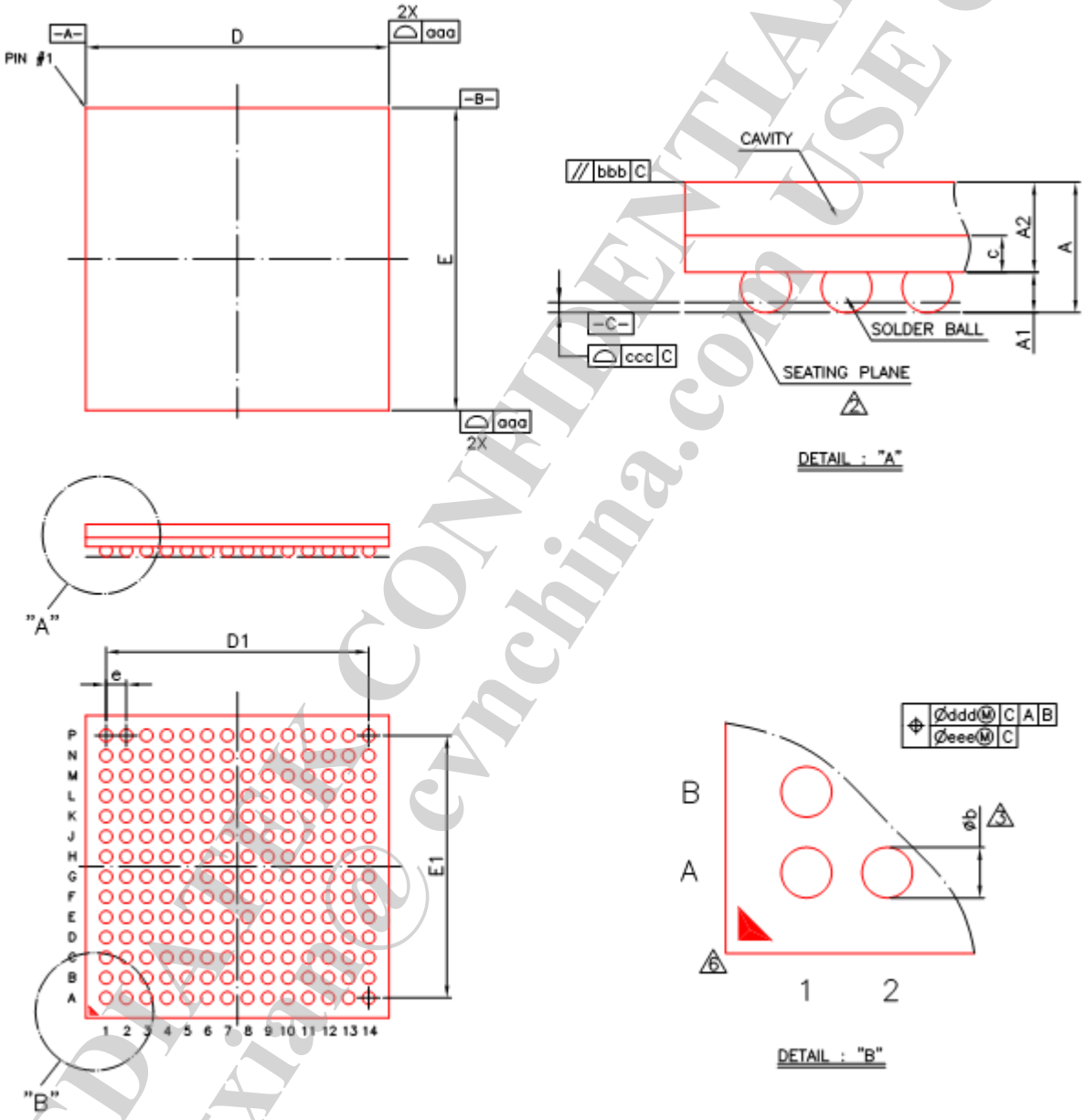
3-15 Brief PHY Rate Format

MODE = Legacy CCK	
MCS = 0	Long Preamble CCK 1 Mbps
MCS = 1	Long Preamble CCK 2 Mbps
MCS = 2	Long Preamble CCK 5.5 Mbps
MCS = 3	Long Preamble CCK 11 Mbps
MCS = 8	Short Preamble CCK 1 Mbps * illegal rate
MCS = 9	Short Preamble CCK 2 Mbps
MCS = 10	Short Preamble 5.5 Mbps
MCS = 11	Short Preamble 11 Mbps
Other MCS codes are reserved in legacy CCK mode. BW and SGI are reserved in legacy CCK mode.	
MODE = Legacy OFDM	
MCS = 0	6 Mbps
MCS = 1	9 Mbps
MCS = 2	12 Mbps
MCS = 3	18 Mbps
MCS = 4	24 Mbps
MCS = 5	36 Mbps
MCS = 6	48 Mbps
MCS = 7	54 Mbps
Other MCS code in legacy CCK mode are reserved When BW = 1, duplicate legacy OFDM is sent. SGI is reserved in legacy OFDM mode.	
MODE = HT mix mode / HT green field	
MCS = 0 (1S)	(BW=0, SGI=0) 6.5 Mbps
MCS = 1	(BW=0, SGI=0) 13 Mbps
MCS = 2	(BW=0, SGI=0) 19.5 Mbps
MCS = 3	(BW=0, SGI=0) 26 Mbps
MCS = 4	(BW=0, SGI=0) 39 Mbps
MCS = 5	(BW=0, SGI=0) 52 Mbps
MCS = 6	(BW=0, SGI=0) 58.5Mbps
MCS = 7	(BW=0, SGI=0) 65 Mbps
MCS = 8 (2S)	(BW=0, SGI=0) 13 Mbps
MCS = 9	(BW=0, SGI=0) 26 Mbps
MCS = 10	(BW=0, SGI=0) 39 Mbps
MCS = 11	(BW=0, SGI=0) 52 Mbps
MCS = 12	(BW=0, SGI=0) 78 Mbps
MCS = 13	(BW=0, SGI=0) 104 Mbps
MCS = 14	(BW=0, SGI=0) 117 Mbps
MCS = 15	(BW=0, SGI=0) 130 Mbps
MCS = 32	(BW=1, SGI=0) HT duplicate 6 Mbps

When BW=1, PHY_RATE = PHY_RATE * 2
When SGI=1, PHY_RATE = PHY_RATE * 10/9
The effects of BW and SGI are accumulative.
When MCS=0~7(1S), SGI option is supported. BW option is supported.
When MCS=8~15(2S), SGI option is supported. BW option is supported.
When MCS=32, only SGI option is supported. BW option is not supported. (BW =1)
Other MCS code in HT mode are reserved

4 Packaging Physical Dimensions

4.1 TFBGA 196B（12×12×0.94 mm）



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.35	0.40	0.45	0.014	0.016	0.018
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	11.90	12.00	12.10	0.469	0.472	0.476
E	11.90	12.00	12.10	0.469	0.472	0.476
D1	---	10.40	---	---	0.409	---
E1	---	10.40	---	---	0.409	---
e	---	0.80	---	---	0.031	---
b	0.45	0.50	0.55	0.018	0.020	0.022
aaa	0.15			0.006		
bbb	0.20			0.008		
ccc	0.20			0.008		
ddd	0.15			0.006		
eee	0.08			0.003		
MD/ME	14/14			14/14		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. SPECIAL CHARACTERISTICS C CLASS: bbb, ccc
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

5 Revision History

Rev	Date	From	Description
1.0	2010/11/25	James hu	Initial Release
1.1	2011/08/08	James hu	1. Revise 2.6DC Electrical Characteristics 2. Revise Power ON Sequence 3. Add pull low is necessary in the description of JTAG_TRST_N