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AR7240: A High Performance And Cost-Effective Network Processor

General Description

The Atheros AR7240 is a high performance and cost effective network processor for access point, router and gateway applications. It includes a MIPS 24K processor, PCI Express host interface, integrated 802.3 Ethernet Switch with five 10/100 Mbps Fast Ethernet MAC/PHY, one USB 1.1 MAC/PHY, external memory interface for serial Flash, DDR1 interface, a high-speed UART, and GPIOs that can be used for LED controls or other general purpose interface configurations.

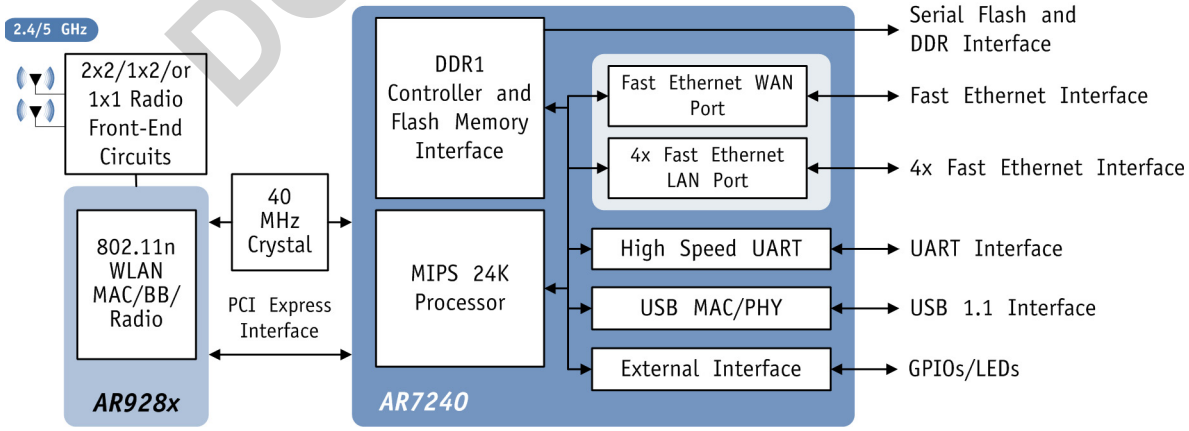
The AR7240 is a memory-centric architecture including various DMA controlled interfaces that access the DDR memory.

The AR7240 network processor, when paired with the AR928x single chip 802.11n MAC/BB/Radio family, provides the best-in-class WLAN solution capable of supporting 802.11a/b/g/n standards.

Features

- Integrated MIPS 24K 32-bit processor operating at up to 400 MHz
- 64K instruction cache and 32K data cache
- Integrated Ethernet Switch with four 10/100 802.3 Ethernet LAN ports and one WAN port
- 16-bit DDR1 memory interface supporting up to 400 M transfers per second
- An external serial Flash memory interface (max. 16 MBytes)
- One USB 1.1 Host Controller with built-in MAC/PHY
- High-speed UART and multiple GPIO pins for general purpose I/O or LED control
- A single lane PCI Express 1.1 interface which can be used for interfacing to the AR928x single chip 802.11n MAC/BB/Radio
- JTAG port support for processor core
- 14 mm x 14 mm 128-pin LQFP lead-free package

System Block Diagram



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1. Pin Descriptions

This section contains a package pinout (see Figure 1-1 and Table 1-2) and a tabular listing of the signal descriptions.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

I	Digital input signal
I/O	A digital bidirectional signal
IA	Analog input signal
IA/OA	Analog bidirectional signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
O	A digital output signal
OA	An analog output signal
OD	A digital output signal with open drain
P	A power or ground signal

Figure 1-1 shows the AR7240 pinout.

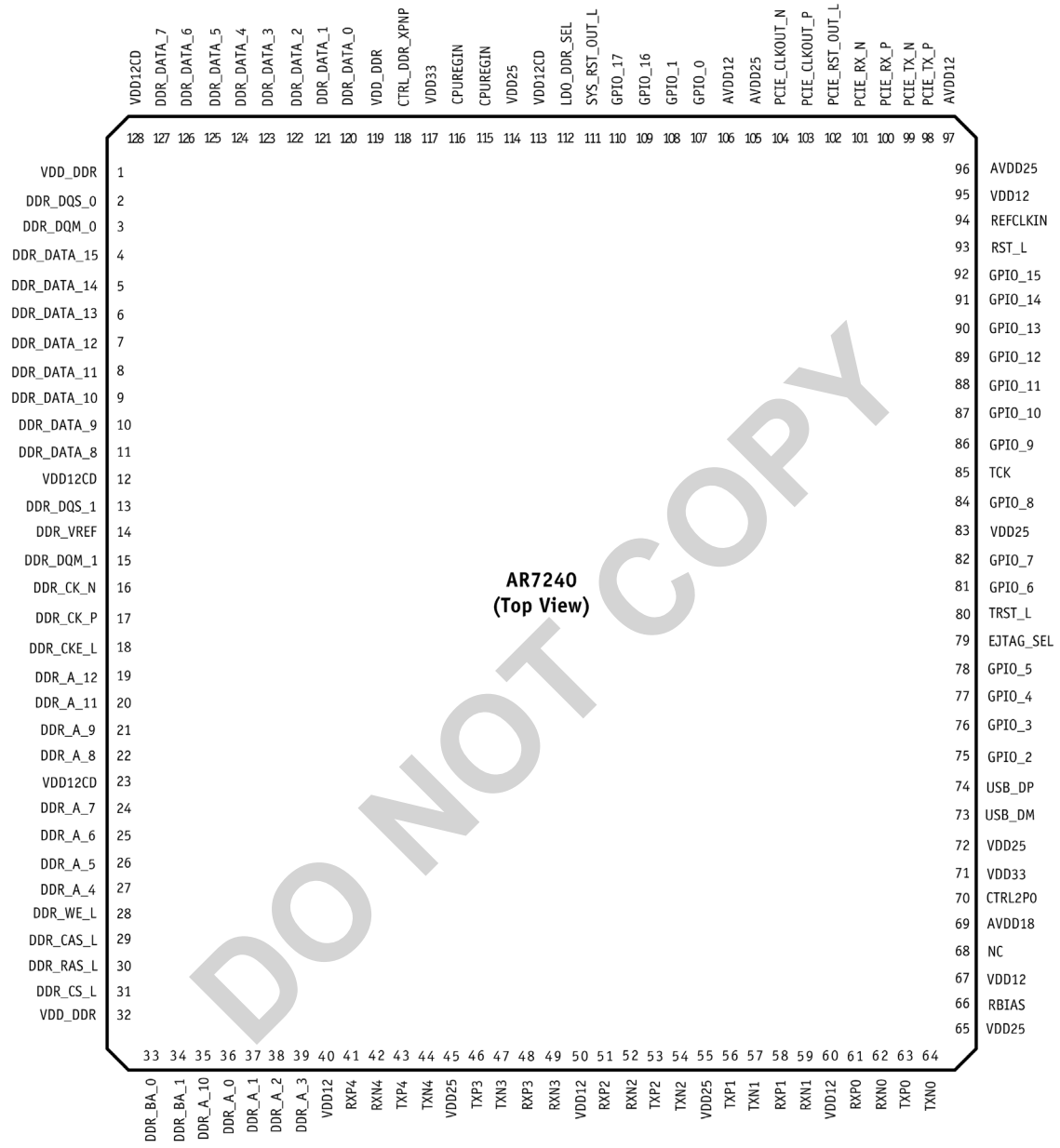


Figure 1-1. **LQFP-128 Package Pinout**

Table 1-1 shows the multiplexed GPIO pins for the AR7240, controlled by the register "GPIO Function (GPIO_FUNCTION)" on page 43.

Table 1-1. **Multiplexed GPIO Pins**

Symbol	Pin	Type	Interface
GPIO_2	75	O	SPI_CS_0
GPIO_3	76	O	SPI_CLK
GPIO_4	77	I	SPI_MOSI
GPIO_5	78	O	SPI_MISO
GPIO_6	81	I	TDI
GPIO_7	82	O	TDO
GPIO_8	84	I	TMS
GPIO_9	86	I	UART_SIN
GPIO_10	87	O	UART_SOUT
GPIO_11	88	O	UART_RTS
GPIO_12	89	I	UART_CTS
GPIO_13[1]	90	O	LED_0
GPIO_14[1]	91	O	LED_1
GPIO_15[1]	92	O	LED_2
GPIO_16[1]	109	O	LED_3
GPIO_17[1]	110	O	LED_4

[1]This pin is intended for driving Ethernet LEDs and cannot be used as an input.

Table 1-2. **Signal-to-Pin Relationships and Descriptions**

Symbol	Pin	Type	Description
PCI Express			
PCIE_CLKOUT_N	104	OA	Differential reference clock (100 MHz)
PCIE_CLKOUT_P	103	OA	
PCIE_RST_OUT_L	102	OD	PCI Express reset, open drain
PCIE_RX_N	101	IA	Differential receive
PCIE_RX_P	100	IA	
PCIE_TX_N	99	OA	Differential transmit
PCIE_TX_P	98	OA	
Reset and Clock			
RST_L	93	IH	Power on reset with internal weak pull-up. Refer to reference design schematics. For electrical characteristics, see Table 4-3 on page 152.
SYS_RST_OUT_L	111	OD	System reset out, open drain, pull up is required
REFCLKIN	94	I	40 MHz reference clock input, AC coupled, can be sine wave or square wave. An external 100 pF capacitor should connect between REFCLKIN and the clock source. See Table 4-6 and Table 4-7 on page 153 for more information.
JTAG			
EJTAG_SEL	79	IL	0 JTAG 1 EJTAG (enhanced JTAG)
TRST_L	80	IL	JTAG/EJTAG reset
TMS[1]	84	IL	JTAG/EJTAG mode select
TDI[1]	81	IL	JTAG/EJTAG data input
TDO[1]	82	O	JTAG/EJTAG data output
TCK	85	IH	JTAG/EJTAG clock
LED			
LED_0[1]	90	OD	If ETH_SWITCH_LED0_EN is set, it becomes open drain and provides drive strength of 10 mA
LED_1[1]	91	OD	If ETH_SWITCH_LED1_EN is set, it becomes open drain and provides drive strength of 10 mA
LED_2[1]	92	OD	If ETH_SWITCH_LED2_EN is set, it becomes open drain and provides drive strength of 10 mA
LED_3[1]	109	OD	If ETH_SWITCH_LED3_EN is set, it becomes open drain and provides drive strength of 10 mA
LED_4[1]	110	OD	If ETH_SWITCH_LED4_EN is set, it becomes open drain and provides drive strength of 10 mA

Table 1-2. **Signal-to-Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
Serial Interface			
SPI_CS_0[1]	75	O	SPI chip select
SPI_CLK[1]	76	O	Serial interface clock
SPI_MISO[1]	77	O	Data transmission from the AR7240 to an external device. On reset, SPI_MISO (GPIO_5) is input and SPI_MISO (GPIO_4) is output so it can directly interface with a SPI device such as a serial flash. If a serial flash is not used, these pins may be used as GPIO pins.
SPI_MOSI[1]	78	IL	Data transmission from an external device to the AR7240. On reset, SPI_MISO (GPIO_5) is input and SPI_MISO (GPIO_4) is output so that it can directly interface with a SPI device such as a serial flash. If a serial flash is not used, these pins may be used as GPIO pins.
GPIO (see also Table 1-1)			
GPIO_0	107	I/O	General purpose input/output with weak pull down and drive strength of 2 mA. For electrical characteristics, see Table 4-3 on page 152.
GPIO_1	108	I/O	
GPIO_2	75	I/O	
GPIO_3	76	I/O	
GPIO_4	77	I/O	
GPIO_5	78	I/O	
GPIO_6	81	I/O	
GPIO_7	82	I/O	
GPIO_8	84	I/O	
GPIO_9	86	I/O	
GPIO_10	87	I/O	
GPIO_11	88	I/O	
GPIO_12	89	I/O	
GPIO_13	90	O	These pins are intended for driving Ethernet LEDs and cannot be used as inputs. See the pin descriptions for "LED" on page 12.
GPIO_14	91	O	
GPIO_15	92	O	
GPIO_16	109	O	
GPIO_17	110	O	
UART			
UART_CTS[1]	89	IL	UART clear to send signal
UART_RTS[1]	88	O	UART ready to send signal (optional UART interface pin)
UART_SOUT[1]	87	O	Serial data out
UART_SIN[1]	86	IL	Serial data in
USB			
USB_DP	74	A	USB 1.1
USB_DM	73	A	USB 1.1

Table 1-2. **Signal-to-Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
DDR			
DDR_A_0	36	O	DDR address
DDR_A_1	37	O	
DDR_A_2	38	O	
DDR_A_3	39	O	
DDR_A_4	27	O	
DDR_A_5	26	O	
DDR_A_6	25	O	
DDR_A_7	24	O	
DDR_A_8	22	O	
DDR_A_9	21	O	
DDR_A_10	35	O	
DDR_A_11	20	O	
DDR_A_12	19	O	
DDR_BA_0	33	O	DDR bank address
DDR_BA_1	34	O	
DDR_CS_L	31	O	DDR chip select
DDR_CK_N	16	O	DDR clock
DDR_CK_P	17	O	
DDR_CKE_L	18	O	DDR clock enable
DDR_RAS_L	30	O	DDR row address strobe
DDR_CAS_L	29	O	DDR column address strobe
DDR_WE_L	28	O	DDR write enable
DDR_DQM_0	3	O	DDR data mask
DDR_DQM_1	15	O	
DDR_DQS_0	2	I/O	DDR data strobe
DDR_DQS_1	13	I/O	
DDR_VREF	14	I	DDR reference level for SSTL signals

Table 1-2. **Signal-to-Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
DDR_DATA_0	120	I/O	DDR data bus
DDR_DATA_1	121	I/O	
DDR_DATA_2	122	I/O	
DDR_DATA_3	123	I/O	
DDR_DATA_4	124	I/O	
DDR_DATA_5	125	I/O	
DDR_DATA_6	126	I/O	
DDR_DATA_7	127	I/O	
DDR_DATA_8	11	I/O	
DDR_DATA_9	10	I/O	
DDR_DATA_10	9	I/O	
DDR_DATA_11	8	I/O	
DDR_DATA_12	7	I/O	
DDR_DATA_13	6	I/O	
DDR_DATA_14	5	I/O	
DDR_DATA_15	4	I/O	
Ethernet			
TXP0	63	IA/OA	Channel 0 transmit
TXN0	64	IA/OA	
RXN0	62	IA/OA	Channel 0 receive
RXP0	61	IA/OA	
TXN1	57	IA/OA	Channel 1 transmit
TXP1	56	IA/OA	
RXP1	58	IA/OA	Channel 1 receive
RXN1	59	IA/OA	
TXP2	53	IA/OA	Channel 2 transmit
TXN2	54	IA/OA	
RXN2	52	IA/OA	Channel 2 receive
RXP2	51	IA/OA	
TXN3	47	IA/OA	Channel 3 transmit
TXP3	46	IA/OA	
RXP3	48	IA/OA	Channel 3 receive
RXN3	49	IA/OA	
TXP4	43	IA/OA	Channel 4 transmit
TXN4	44	IA/OA	
RXN4	42	IA/OA	Channel 4 receive
RXP4	41	IA/OA	
RBIAS	66	OA	Connect to 2.37 KΩ ±1% resistor to ground

Table 1-2. **Signal-to-Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
Regulator Control			
LDO_DDR_SEL	112	I	Selects the regulated DDR voltage, must be set to 1 for DDR1
CTRL2P0	70	OA	External PNP control. Connect to the base of an external PNP: collector to AVDD18 and emitter to VDD33
CTRL_DDR_XPNP	118	OA	External PNP Control. Connect to the base of an external PNP: collector to VDD_DDR and emitter to VDD33
CPUREGIN	115, 116	I	CPU regulator control inputs. Minimum voltage is 1.8 V. A 1Ω resistor may be used in series between these pins and the VDD_DDR pins when in DDR1 mode (LDO_DDR_SEL=1). See Figure 4-1, "Output Voltages Regulated by the AR7240," on page 154.

[1]This pin is multiplexed. See Table 1-1.

Symbol	Pin	Description
Power[1]		
VDD12	40, 50, 60, 67, 95	Regulated 1.2 V output from the AR7240
VDD25	45, 55, 65, 72, 83, 114	Regulated 2.5 V output from the AR7240; normal IO voltage
VDD12CD	12, 23, 113, 128	Regulated 1.28 V output from the AR7240; core voltage of CPU/ DDR blocks, connect pins 12 and 23 to pins 113 and 128
VDD33	71, 117	3.3 V power supply
VDD_DDR	1, 32, 119	Regulated 2.6 V for DDR1. Connect to the collector of the external PNP (PNP1 in Figure 4-1 on page 154)
AVDD18	69	Regulated 2.0 V from the AR7240; connect to the collector of the external PNP (PNP2 in Figure 4-1 on page 154)
AVDD12	97, 106	PCIE 1.2 V power supply, connect to VDD12
AVDD25	96, 105	PCIE 2.5 V power supply, connect to VDD25
Ground Pad		
Exposed Ground Pad	—	Tied to GND (see "Package Dimensions" on page 162)
No Connection		
NC	68	No connection

[1]Refer to Figure 4-1, "Output Voltages Regulated by the AR7240," on page 154 and to the reference design schematics for details.

2. System Architecture

Figure 2-1 illustrates the AR7240 system architecture.

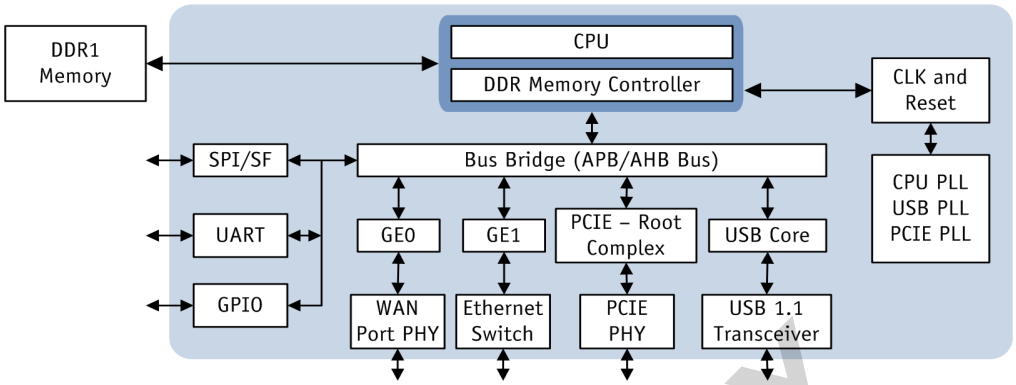


Figure 2-1. **AR7240 Functional Block Diagram**

Table 2-1 summarizes the functional blocks that comprise the AR7240.

Table 2-1. **Functional Block Descriptions**

Block	Description
CPU	A MIPS 24 K processor that can run up to 400 MHz (an external voltage regulator is required to run at 400 MHz; see page 155). It includes a 64 K four-way set associative instruction cache, 32 K four-way set associative data cache, single cycle multiply-accumulate and MIPS32 and MIPS16 instruction sets. Non-blocking cache reads are also supported. See page 18.
DDR Memory Controller	Supports a 16-bit DDR memory interface of up to 400 Mbps/pin. It supports one dedicated point-to-point interface for the CPU and similarly dedicated point-to-point interfaces for the CPU, USB, Ethernet and PCIE master devices.
PHY/ Ethernet Switch	Four LAN ports and one WAN port with integrated PHY. LED indication for each port is supported. The four LAN ports connect to the CPU through the GE1 GMII interface, and four transmit queue priorities are supported in each LAN port. The WAN port connects to the CPU using the GE0 MII interface. The MII interface also can support up to four priority queues, with either simple priority or a weighted round robin arbitration mechanism. Switch functions such as QoS and VLAN are supported.
USB	Universal Serial Bus 1.1 host interface
PCIE	The root complex single lane interface that can support up to 2.56 Gbps
PLL	The PLL block consists of five PLLs used to generate: ■ A clock for CPU/DDR, tunable from 300 MHz to 450 MHz ■ PLL for 48 MHz reference clock for the USB core and to generate a 25 MHz reference clock for the Ethernet Switch ■ PCIE 100 MHz clocks with dither support ■ PCIE PHY PLL generates 250 MHz and 2.5 GHz clock for the PCIE interface ■ PLL to generate 125 MHz from a 25 MHz clock
UART	16650 equivalent UART for debug/console
Bus Bridge	High speed peripheral bus; the APB connects peripherals such as GPIO, UART, and SPI for Flash to the bus bridge. The AHB connects high-performance peripheral interfaces such as the GB Ethernet and USB interfaces to the bus bridge.
SPI	SPI interface that can be used for serial Flash
GPIO	Two dedicated and 16 multiplexed GPIO pins that can be used for general purpose controls, SPI, UART, LEDs, and EJTAG. See Table 1-1 on page 11 for GPIO multiplexing.

2.1 MIPS Processor

The AR7240 integrates an embedded MIPS 24Kc processor. For complete information on the 24Kc processor, visit: http://www.mips.com/products/processors/32-64-bit-cores/mips32-24k/

Under MIPS 24K Family, choose the resources tab and refer to:

- MIPS32 24Kc Processor Core Datasheet
- MIPS32 24Kc Processor Core Family Software User's Manual

2.2 Configuration

Table 2-2 summarizes the configuration settings used by the AR7240.

Upon reset, the CPU puts out an address of 0xBFC00000 which is mapped to the flash address space.

Table 2-2. **Core Processor Configuration Settings**

Setting	Description
Cache Size	The AR7240 implements 64KB 4-way set associative instruction cache and 32KB 4-way set associative data cache. It supports single cycle multiply-accumulate, MIPS32 and MIPS16 instruction sets and non-blocking cached reads.
Endian	The AR7240 implements big Endian addressing.
Block Addressing	The AR7240 implements sequential ordering.

2.2.1 Processor Frequency

The AR7240 processor supports a clock frequency of up to 400 MHz.

NOTE: An external voltage regulator is required for VDD12CD and VDD12 when operating at 400 MHz. Refer to "External Voltage Regulator With 400 MHz Operation" on page 155 for more information.

2.3 AR7240 Address MAP

The address space for the AR7240 is divided into two 256 MBytes (MB) regions. The lower region maps to the DDR memory. The upper region maps to the AHB bus bridge. The 512 MBytes decoded region is repeated through the 4 GBytes of the processor's address space. Figure 2-2 shows the address space allocation.

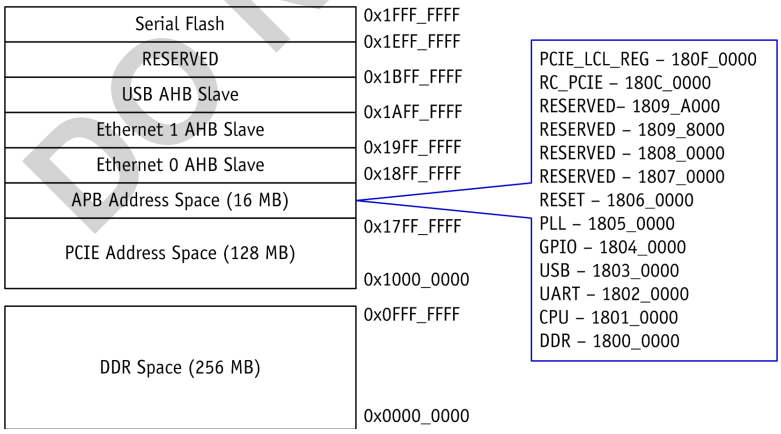


Figure 2-2. **Address Space Allocation**

2.4 AHB Master Bus

The 256 MByte address space region for AHB devices is divided into two major windows, 128 MByte for the PCIE and the remainder for the internal DDR AHB master interfaces such as APB, GE0, GE1, serial flash, etc.

2.5 APB Bridge

One 16 MByte window of the AHB address space is devoted to an APB device mapper. The APB space contains the register address spaces of most of the interfaces, including PCIE, serial flash, GPIO, and UART. This space also provides access to the watchdog timer and four general purpose timers. See "Reset Control Registers" on page 48.

2.6 DDR Memory Controller

The AR7240 supports a 16-bit DDR memory interface of up to 64 MBytes of memory in a single device. It supports one dedicated point-to-point interface for the CPU and similarly dedicated point-to-point interfaces for the CPU, USB, Ethernet and PCIE master devices. Write transactions are buffered at each interface. It implements separate arbitration for each bank thus allowing efficient pipelined RAS/CAS/precharge scheduling.

The DDR block has five AHB-slave interfaces for GE0, GE1, USB, PCIE, and CPU. External DDR is powered by the AR7240 using an external power transistor. The LDO_DDR_SEL pin input selects the AR7240 internal regulator to generate VDD_DDR output voltage to power the external DDR1 memory.

Table 2-3 shows the LDO_DDR_SEL configurations.

Table 2-3. **LDO_DDR_SEL Voltage Configuration**

LDO-DDR_SEL Input	DDR Voltage	Device Type
1	2.6V	DDR1

The VDD_DDR is divided by two externally to generate DDR_VREF for the AR7240 DDR I/O and the DDR memory chip. See the reference design schematics for more information. Figure 4-1 on page 154 shows the output voltages regulated by the AR7240.

Table 2-4 shows the DDR configurations supported by the AR7240.

Table 2-4. **DDR Configurations**

Device Type/Total Capacity	Device Count	Device Type
128 MBits (8 Mx16)	1	DDR1
256 MBits (16 Mx16)	1	DDR1
512 MBits (32 Mx16)	1	DDR1

Table 2-5 shows the correspondence of the internal CPU address, the AR7240 DDR interface address, and the address of the DDR memory device.

Table 2-5. **Address Mapping**

CPU Address Bit	AR7240 DDR Interface Address	Corresponding 16-bit DDR Memory Device Address[1]
0	DDR_A_0, Unused (x16 DRAM)	
1	DDR_A_1	CAS0
2	DDR_A_2	CAS1
3	DDR_A_3	CAS2
4	DDR_A_4	CAS3
5	DDR_A_5	CAS4
6	DDR_A_6	CAS5
7	DDR_A_7	CAS6
8	DDR_A_8	CAS7
9	DDR_A_9	CAS8
10	DDR_A_0	RAS0
11	DDR_BA_0	BA0
12	DDR_BA_1	BA1
13	DDR_A_1	RAS1
14	DDR_A_2	RAS2
15	DDR_A_3	RAS3
16	DDR_A_4	RAS4
17	DDR_A_5	RAS5
18	DDR_A_6	RAS6
19	DDR_A_7	RAS7
20	DDR_A_8	RAS8
21	DDR_A_9	RAS9
22	DDR_A_10	RAS10
23	DDR_A_11	RAS11
24	DDR_A_12	RAS12
25	DDR_A_11	CAS9
26	DDR_A_12	CAS11

[1]CAS10 is a precharge bit, typically 0.

2.7 Serial Flash (SPI)

The SPI interface is controlled by the bit SPI_EN in the register "GPIO Function (GPIO_FUNCTION)" on page 43. This bit is enabled upon reset. The single SPI chip select is dedicated to an external flash to boot the chip. Two configurable chip selects are available to bit-bang using GPIOs that configure external components. As an AHB slave, the SPI controller only supports word transactions.

The CPU can perform a cached read access of the serial flash, but write access is not cached. Write transactions are possible by bit-banging GPIO registers, only when bit [0] in the register "SPI Function Select (SPI_FUNC_SELECT)"is set to 1.

The AR7240 supports a maximum flash size of 16 MBytes controlled by REMAP_DISABLE, bit [6], in the register "SPI Control (SPI_CONTROL)" on page 118. By default, only 4 MBytes are accessible until bit [6] is set to 1.

2.8 UART

The AR7240 contains a single 16550 equivalent UART port for debug/console. The UART pins are multiplexed with GPIO pins, therefore the "GPIO Function (GPIO_FUNCTION)" register bits are used to control which GPIO pins are used for UART functions.

2.9 GE0 and GE1

The AR7240 integrates two Gigabit Ethernet ports that are connected to the Ethernet Switch. The GE0 and GE1 support 2K transmit (Tx) FIFO and 2K receive (Rx) FIFO. The WAN port is a MII interface that connects directly to a PHY inside the Ethernet Switch. Another port connects to the Ethernet Switch using a GMII interface. Through the Ethernet Switch this port connects to the four LAN ports. See Figure 2-4 on page 23.

The GMII and MII MAC interface to the Ethernet Switch supports four Tx queues, each with its own descriptor chain. A priority of DMA_TX_Q0 is higher than DMA_TX_Q1, and so on. The DMA configuration registers are separate for each queue. Two arbitration mechanisms are supported: a simple priority and a weighted round robin arbitration. The register "DMA Transfer Arbitration Configuration (DMATXARBCFG)" on page 90 controls the behavior of the arbiter. If simple priority arbitration is chosen by setting the RRMODE bit to zero, the Q1 chain is processed only after all packets in Q0 are transmitted.

Similarly for rest of the queues. In case of round robin arbitration on a long term the number of packets sent per queue is guaranteed to be in the ratio of the weights programmed. A weight of ZERO is prohibited. It should be noted that the weights are on a packet basis and not based on the number of bytes transmitted on that queue. Moreover, a 19-bit free running counter (running on AHB_CLK) value is updated on the descriptor field on both the Tx and Rx descriptor as shown in Figure 2-3. This update is done as part of the descriptor update that the MAC DMA core already does on Tx or Rx completion. Software tracks the latency on per packet basis using the descriptor timestamp and free timer register.

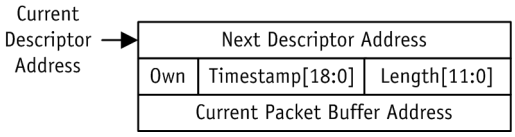


Figure 2-3. **Descriptor Format**

The current value of the free counter can be controlled / read by the CPU through the register "Ethernet Free Timer" on page 88. Two resolutions of the timer are supported.

2.9.1 Descriptor Definitions

Before any DMA transfers can be carried out, two sets of descriptors must be initialized in host memory: one for Tx operations and one for Rx operations. Each set takes the form of a linked list (typically closed to form a ring buffer). The entry point into the buffer used at the start of any transfer sequence is given by the descriptor picked out by the DMA Tx/Rx descriptor register. Each descriptor comprises a sequence of three 32-bit memory locations as shown in this section.

Table 2-6. **Descriptor Components**

Address	Names	Description	Page
0x0	PacketStartAddr	Start Address for Packet Data	page 21
0x4	PacketSize	Size of Packet, Overrides, and Empty Flag	page 22
0x8	NextDescriptor	Location of Next Descriptor	page 22

2.9.2 PacketStartAddr

Address: 0x0
Access: Read/Write

Start address for packet data. Note that start addresses used in any sequence of descriptors must be spaced to allow sufficient room in any location for a packet of the maximum size transferred.

Bit	Description
31:2	Top 30 bits of packet start address The built-in DMA controller reads the register to locate the first byte of data in host memory.
1:0	These bits are ignored by the DMA controller, because it is a system requirement that all transfers are 32-bit aligned in host memory. Default is 0.

2.9.3 PacketSize

Address: 0x4
Access: Read/Write

Size of the packet, time stamp, and the empty flag.

Bit	Description	
31	Empty flag	
	Tx Operations	This bit indicates the availability of the data associated with the packet. On successful completion of a Tx operation, the DMA controller writes a 1 to this location to indicate that the associated data has been transferred from this location, guaranteeing that data cannot be accidentally transferred twice.
	Rx Operations	This bit indicates the availability of the specified location to store the received packet. The setting of this flag is used to validate the descriptor. On successful completion of a Rx operation, the DMA controller writes a 0 to this location to indicate that this location has been used to store the received packet, guaranteeing that received data is not accidentally overwritten by a subsequent packet.
30:12	Time stamp	
11:0	Packet size	
	Tx Operations	Returns the size of packet to be transferred in bytes
	Rx Operations	The DMA controller writes the number of bytes received to this field; the value of this field prior to the transfer being made is ignored

2.9.4 NextDescriptor

Address: 0x8
Access: Read/Write

Location of next descriptor.

Bit	Description
31:2	Top 30 bits of packet start address The built-in DMA controller reads the register to locate the first byte of data in host memory. The descriptors should form a closed linked list.
1:0	These bits are ignored by the DMA controller, because it is a system requirement that all transfers are 32-bit aligned in host memory. Default is 0.

2.10 MDC/MDIO Interface

The MDC/MDIO interface, which is internal to the AR7240, allows users to access the internal registers of the switch. Table 2-7 shows the format required to access the MII registers in the embedded PHY. The PHY-address is from 0x00 to 0x04. The OP code 10 indicates the read command and 01 indicates the write command.

Table 2-7. **MDC/MDIO Interface Format**

start	Op	00	Phy-addr [2:0]	reg_addr [4:0]	TA [1:0]	Data [15:0]

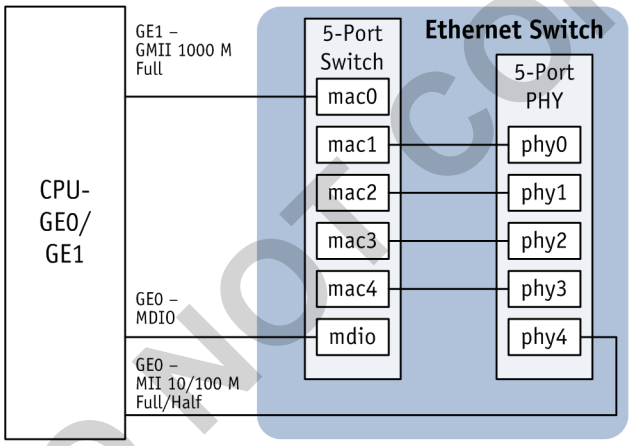
The internal switch registers are 32 bits wide, but MDIO access is only 16 bits wide, so two access cycles are required to access all 32 bits of the internal registers. Address spacing is more than the MDIO-supported 10 bits, thus upper address bits must be written to the internal registers, similar to the page mode access method. For example, register address bits [18:9] are treated as a page address and written out first as High_addr [9:0] (see Table 2-8). Then the register would be accessed via Table 2-7, where Low_addr [7:1] is the register address bit [8:2] and Low_addr [0] is 0 for Data [15:0] or Low_addr [0] is 1 for Data [31:16].

Table 2-8. **Initial Register Address Bits**

start	Op	2'b11	8'b0	6'b0	High_addr [9:0]

2.11 Ethernet Switch Controller

Figure 2-4 shows the Ethernet Switch block diagram.



Notes:
1. mac0 connects to the CPU port and only supports 1000M full duplex mode.
2. phy4 connects to the CPU directly and supports 10/100M full and half duplex.
3. The MDIO interface connects the Ethernet switch to the configuration register.

Figure 2-4. **Ethernet Switch Block Diagram**

The Ethernet Switch controller performs the majority of the switch functions of the AR7240. The controller contains five 10/100 Mbps Fast Ethernet ports, each containing four levels of Quality of Service, 802.1Q VLANs, port based VLANs and RMON statistic counters. The AR7240 integrates five 10/100 two speed Ethernet transceivers (PHYs) and one single port 10/100/1000 media access controllers (MAC) as well as a wire-speed, non-blocking shared memory switch fabric.

The included 1 KB entry address lookup table uses two entries per bucket to avoid hash collisions and maintain packet-forwarding performance. The address entry table provides read/write access from the serial and CPU interfaces where each entry can be configured as a static entry. 1024 MAC addresses are supported with automatic learning, aging and static address support. The Ethernet Switch also supports basic switch features including port mirroring, broadcast storm support, flow control in full-duplex, and back pressure in half duplex, 802.3 auto-negotiation, port locking, MIB counters, ingress and egress rate limitation, and automatic speed and duplex communication between PHYs and MACs.

Table 2-9 summarizes the AR7240 Ethernet Switch functions.

Table 2-9. **Ethernet Switch**

Block	Description
Media Access Controllers (MAC)	The AR7240 integrates six independent fast Ethernet MACs that perform all functions in the IEEE 802.3 and IEEE 802.3u specifications, including frame formatting, frame stripping, CRC checking, CSMA/CD, collision handling, and back-pressure flow control, etc. Each MAC supports 10 Mbps or 100 Mbps operation in either full-duplex or half-duplex mode.
Full-Duplex Flow Control	The AR7240 device supports IEEE 802.3x full-duplex flow control, force-mode full-duplex flow control, and half-duplex back pressure. If the link partner supports auto-negotiation, the 802.3x full-duplex flow control auto-negotiates between the remote node and the AR7240. If full-duplex flow control is enabled, when free buffer space is almost empty, the AR7240 sends out an IEEE 802.3x compliant PAUSE to stop the remote device from sending more frames.
Half-Duplex Flow Control	Half-duplex flow control regulates the remote station to avoid dropping packets during network congestion. A back pressure function is supported for half-duplex operations. When free buffer space is almost empty, the AR7240 device transmits a jam pattern on the port and forces a collision. If the half-duplex flow control mode is not set, the incoming packet is dropped if no buffer space is available.
Inter-Packet Gap (IPG)	The IPG is the idle time between any to successive packets from the same port. The typical IPG is 9.6 µs for 10 Mbps Ethernet and 960 ns for 100 Mbps Fast Ethernet.
Port Locking	The AR7240 supports port locking. If one port is set for port locking, only received frames with the unicast source address found in the ARL table and do not have a member violation, can be sent out. Other blocked frames are dropped or redirected to the CPU port by the control register, LOCK_DROP_EN.
Frame Forwarding Prevention	The AR7240 can be configured to prevent the forwarding of unicast or multicast frames that contain an unknown destination address. This can be accomplished on a per-port basis, so that frames with unknown addresses only go out to the port where a server or router is connected. Broadcast frames forwarded to the CPU port can also be prevented.
Illegal Frames	The AR7240 discards all illegal frames such as CRC error, oversized packets (length greater than maximum length), and runt packets (length less than 64 bytes).
VLANs	See "VLANs For LAN Ports" on page 25.
QoS	See "Quality of Service (QoS) For LAN Ports" on page 26.

2.11.1 VLANs For LAN Ports

The switch supports 16 IEEE 802.1Q VLANs and port-based VLAN functionality for all frames, including management frames when 802.1Q is enabled on the ingress port. Untagged frames conform to the port-based VLAN even if the ingress port has 802.1Q mode enabled. See Table 2-10.

Table 2-10. **Ethernet Switch VLAN**

VLAN	Description
Port-Based	Each ingress port contains a register restricting the output (or egress) ports it can send frames to. This port-based VLAN register has a field called PORT_VID_MEM that contains the port based setting. If bit [0] of PORT_VID_MEM is set to one, the port is allowed to send frames to Port 0, bit [2] for Port 2, and so on. At reset, each port's PORT_VID_MEM is set to a value of all 1s, except for each port's own bit, which clears to zero. Note that the CPU port is port 0.
IEEE 802.1Q VLANs	The AR7240 supports a maximum of 16 entries in the VLAN table. The device supports 4096 VLAN ID range from 0 to 4095. The AR7240 only supports shared VLAN learning (SVL). This means that forwarding decisions are based on the frame's destination MAC address, which should be unique among all VLANs.

Tagging and untagging egress frames is supported using 802.1Q VLANs, or statically using Port Based VLANs. Frames may go out from the switch in three methods:

- Transmit Unmodified
  Untagged frames egress a port untagged while tagged frames leave tagged.
- Transmit Untagged
  Untagged frames leave a port unmodified while tagged frames leave untagged.
- Transmit Tagged
  Tagged frames leave a port unmodified while an IEEE tag is added to untagged frames before leaving.

When a tag is added to an untagged frame, the frame inserts directly after the frame's source address and includes four bytes.

- The first byte is always 0x81.
- The second byte is always 0x00.
- PRI bits indicate frame priority determined by the source port's priority setting.
- The CFI bit is always set to 0.

VID bits indicate the VID assigned to the frame as determined in the source port default VID.

A tagged frame leaving a port tagged may have its VID bits modified. If the ingressing frame's VID was 0x000, the ingress port's default VID is assigned to the frame instead.

Double Tagging is a method of isolating one IEEE 802.1Q VLAN from other IEEE 802.1Q VLANs in a hierarchical fashion that is compatible with IEEE 802.1Q ready switches, as long as those switches support a maximum frame size of 1526 bytes or more. In this way, an extra, or double, tag is placed in front of a frame's normal tag thereby increasing the frame's size by four bytes.

Ingress double tagging can be selected on a port-by-port basis. Typically, any port that has ingress double tagging enabled will also have egress double tagging enabled. Ingress double tagging enabled ports expect all ingress frames to contain an extra tag that must be removed from the frame before performing the port's ingress policy on the frame. In this mode, the ingress policy removes the first IEEE 802.3ac tag that appears after the source address in every frame. If the untagged frame is not modified, all data from the removed tags is ignored by the switch.

2.11.2 Quality of Service (QoS) For LAN Ports

The AR7240 recognizes the QoS information of ingress frames and map to different egress priority levels. The AR7240 determines the priority of the frames based on DA, TOS/TC, VLAN, and port. Each has an enable bit that can be applied. When more than one type of priority is selected, the order in which the frame priority should be applied can be determined. Priority enable bits and select order bits are set by port base at 0x110 for port 0, 0x210 for port 1, and so on.

Priority Determined	Description
DA	Set DA_PRI_EN bit [18] to 1 and add the address to the ARL table-set priority_over_en to 1. ARL priority bits [59:58] can be used as DA priority.
ToS/TC	Set IP_PRI_EN bit [16] to 1, and set the IP priority mapping register (0x60–0x6C).
VLAN	Set VLAN_PRI_EN (bit [17]) to 1, and set the TAG priority mapping register (0x70).
Port's Default Authority	Set PORT_PRI_EN to 1, and set port base register ING_PORT_PRIORITY (bits [19:28] in 0x108, 0x208, etc.).

When more than one priority enable bit is set to 1, bits [7:0] in 0x110, 0x210, etc. (DA_PRI_SEL, IP_PRI_SEL, VLAN_PRI_SEL, PORT_PRI_SEL) can determine the order in which the frame priority should be applied. If *_PRI_SEL is set to 00, frame priority is determined by that first. Otherwise, priority is determined by which *_PRI_SEL is set to 01, then 10, 11, etc.

On arrival, packets are directed into one of the four available priority queues based on:

- Priority bits in the header field
- The frame destination address (if in the ARL table with a defined priority with the priority bit is enabled)
- The frame VID (if in the VLAN table and the priority override is enabled)
- The 802.3 tag containing 802.1p priority information (if enabled on the port)
- The port's default priority as defined in the register

Each of the priority classification rules have enables so designers may use any combination; priority can be disabled or the order may be selected separately on a per-port basis.

Congestion in the flow of packets for an extended period of time forces frames to drop without flow control. Higher priority flows receive a higher percentage of the open buffers, and this percentage is determined by the scheduling mode. Features such as back pressure and pause-frame control are implemented to supports zero packet loss during traffic congestion. The AR7240 ensures that all uncongested flows traverse the switch without degradation, regardless od congestion situations elsewhere in the switch.

QoS for the AR7240 may follow one of three priority schemes, either fixed, weighted fair, or a mixed mode scheme. In the fixed priority scheme, all egress packets leave the switch starting with the highest priority queue. Once that queue has been emptied, the next highest priority queue begins its packet dispersal until it has been emptied and so on. This method insures that all high priority packets will be sent out from the switch as soon as possible.

For the weighted fair scheme, packets are egressed from the chip in the order of 8, 4, 2, 1 packets for the four priorities queue of the AR7240. (eight packets egress from the highest priority queue, then four from the second highest queue, and so on). This method allows the highest priority to get its packets out first and the other remaining queues are not totally starved from egressing.

The mixed mode scheme mixes both the weighted fair and fixed schemes. The highest priority queue disperses its packets first until the queue has been emptied, and the remaining queues will follow the 4, 2, 1 weighted egress scheme as mentioned previously. This ensures that the highest priority queue will egress its packets as soon as possible, while the remaining queues equally disperse their packets without queue starvation.

2.12 Rate Limiting

The AR7240 supports port-based ingress and egress rate limiting. All frames may be limited but management frames and known multicast frames are the only types that can be selected by the user. The ingress limit rate may be set from zero to 1 Gbps in steps of 32 Kbps. The port base register is used to determine the limited bytes to count. The default setting for rate limiting is to include the frame's bytes from the beginning of the preamble to the end of the RCS with a added minimum IFG.

2.12.1 Broadcast Storm Control

The AR7240 supports broadcast storm control. Some switch designs may require limiting the reception rate of frames. The types of frames to be limited can be selected separately on a per-port basis.The maximum rate desired needs to be selected by the user and then programmed. Eleven different frame rates from 1k (2^0K) to 2^{10}K per second.

The statistics counter block maintains a set of forty MIB counters per port. These counters provide a set of Ethernet statistics for frames received on ingress and transmitted on egress. A register interface allows the CPU to capture, read, or clear the counter values.

The counters support:

- RMON MIB
- Ethernet-like MIB
- MIB II
- Bridge MIB
- RFC2819

The CPU interface supports:

- Autocast MIB counters after half-full
- Autocast MIB counters after time out
- Autocast MIB counters when requested
- Clearing all MIB counters

The MIB counters in the switch are for LAN's and CPU port. For WAN, the MIB counters are in GE1.

See "Statistics Counters" on page 142.

2.13 Switch Operation

Two tables embedded in the AR7240 aid in allocation of ingress packets, the ARL table and the VLAN table.

The address database is stored in the embedded SRAM and can store up to 1024 address entries. The default aging time for this table is 300 seconds. One address can be searched in the table and it may be used to get the next read out of the whole table. Entries in the table may be loaded and purged. All entries maybe be flushed, and this may be divided to flush just non-static entries, all entries per port or all non-static entries per port.

The VLAN table supports a single search, and it may be used to get the next read out of the whole table. Entries may be loaded or purged and entries may be flushed, either as a whole or per port.

2.14 Port Mirroring

Ingress, egress and destination address packets can be mirrored by the AR7240. To mirror the DA packets, the mirror enable bit must be set in the ARL table. To mirror a port, simply set the mirror port number.

Port mirroring is only among the LAN ports and not for WAN.

2.15 Port States

Table 2-11 shows the port states supported by the AR7240.

Table 2-11. **Port States**

State	Description
Disabled	Frames are not allowed to enter or leave a disabled port. Learning does not take place on disabled ports.
Blocking	Only MGMP frames are allowed to enter a blocked port. All other frame types are discarded. Learning is disabled on blocked ports.
Listening	Only management frames may enter or leave a listening port. All other frame types are discarded. Learning is disabled on listening ports.
Learning	Only management frames may enter or leave a learning port. All other frame types are discarded but learning occurs on all good frames, including non-management frames.
Forwarding	Normal operation. All frames may enter or leave a forwarding port. Learning occurs on all good frames.

3. Register Descriptions

These sections describe the internal registers for the various AR7240 blocks.

The AR7240 has two types of registers:

- Registers that are directly memory mapped to the CPU address space (see Table 3-1).
- Registers that are indirectly mapped through the MDIO interface of GE0. All the Ethernet Switch related registers fall in this category (see "Ethernet Switch Registers" on page 120).

Table 3-1 summarizes the CPU mapped registers for the AR7240.

Table 3-1. **CPU Mapped Registers Summary**

Address	Description	Page
0x18000000–0x18000094	DDR Registers	page 29
0x18020000–0x18020018	UART Registers	page 34
0x18040000–0x18040028	GPIO Registers	page 40
0x18050000–0x18050028	PLL Control Registers	page 44
0x18060000–0x18060090	Reset Control Registers	page 48
0x180F0000–0x180F0050	PCIE Local Registers	page 53
0x19000000–0x190002BC	GE0 Registers	page 63
0x1A000000–0x1A0002BC	GE1 Registers	page 63
0x1B000000–0x1B000058	USB Registers	page 106
0x1F000000–0x1F00000C	SPI Registers	page 118
0x0000–0x204A4	Ethernet Switch Registers	page 120
0x10000000–0x1000003C	PCIE Configuration Space Registers	page 144

3.1 DDR Registers

Table 3-2 summarizes the DDR registers for the AR7240.

Table 3-2. **DDR Registers Summary**

Address	Name	Description	Page
0x18000000	DDR_CONFIG	DDR DRAM Configuration	page 30
0x18000004	DDR_CONFIG2	DDR DRAM Configuration	page 30
0x18000008	DDR_MODE_REGISTER	DDR Mode Registration	page 31
0x1800000C	DDR_EXTENDED_MODE_REGISTER	DDR Extended Mode Registration	page 31
0x18000010	DDR_CONTROL	DDR Control	page 31
0x18000014	DDR_REFRESH	DDR Refresh	page 31
0x18000018	DDR_RD_DATA_THIS_ CYCLE	DDR Current Cycle Read	page 31
0x1800001C	TAP_CONTROL_0	DQS Delay Tap Control for Byte 0	page 32
0x18000020	TAP_CONTROL_1	DQS Delay Tap Control for Byte 1	page 32
0x1800007C	DDR_WB_FLUSH_GE0	GE0 Write Buffer Flush	page 32
0x18000080	DDR_WB_FLUSH_GE1	GE1 Write Buffer Flush	page 32
0x18000084	DDR_WB_FLUSH_USB	USB Write Buffer Flush	page 33
0x18000088	DDR_WB_FLUSH_PCIE	PCIE Write Buffer Flash	page 33
0x1800008C	DDR_DDR_CONFIG	DDR Config	page 33
0x18000090	DDR_EMR2	DDR Extended Mode	page 33
0x18000094	DDR_EMR3	DDR Extended Mode	page 33

3.1.1 DRR DRAM Configuration (DDR_CONFIG)

Address: 0x18000000
Access: Read/Write
Reset: See field description

This register is used to configure the DDR DRAM parameters.

Bit	Bit Name	Reset	Description
4:0	TRAS	0x10	DRAM tRAS parameter rounded up in memory core clock cycles
8:5	TRCD	0x6	DRAM tRCD parameter rounded up in memory core clock cycles
12:9	TRP	0x6	DRAM tRP parameter rounded up in memory core clock cycles
16:13	TRRD	0x4	DRAM tRRD parameter rounded up in memory core clock cycles
22:17	TRFC	0x1E	DRAM tRFC parameter rounded up in memory core clock cycles
26:23	TMRD	0xF	DRAM tMRD parameter rounded up in memory core clock cycles
29:27	CAS_LATENCY	0x6	DRAM CAS latency parameter rounded up in memory core clock cycles
30	OPEN_PAGE	0x1	Controller open page policy. This policy increases bus efficiency if accesses are local to a page but increase random read/write latency.
		0	Page open
		1	Page closed
31	CAS_LATENCY_MSB	0x0	MSB bit of four-bit CAS_LATENCY field

3.1.2 DDR DRAM Configuration 2 (DDR_CONFIG2)

Address: 0x18000004
Access: Read/Write
Reset: See field description

This is the second register is used to configure the DDR DRAM parameters.

Bit	Bit Name	Reset	Description
3:0	BURST_LENGTH	0x8	DRAM burst length setting. Only 0x8 is supported.
4	BURST_TYPE	0x0	DRAM burst type
		0	Sequential
		1	Not supported
5	CNTL_OE_EN	0x1	A control bit to allow the memory controller to tri-state the address/ control outputs
6	PHASE_SELECT	0x0	Selects the output phase
7	CKE	0x1	DRAM CKE bit
11:8	TWR	0x6	DRAM tWR parameter rounded up in memory core clock cycles
16:12	TRTW	0x10	DRAM tRTW parameter rounded up in memory core clock cycles. The value should be calculated as CAS Latency + Burst Length + bus turn around time.
20:17	TRTP	0x8	DRAM read to precharge parameter rounded up in memory core clock cycles. the normal value is two clock cycles.
25:21	TWTR	0xE	DRAM tWTR parameter rounded up in memory core clock cycles
29:26	GATE_OPEN _LATENCY	0x6	Memory CAS latency * 2
30	RES	—	Reserved
31	HALF_WIDTH_ LOW	0x1	This bit controls which part of the 32-bit DDR DQ bus is populated with DRAM in a 16-bit wide memory system
		0	Not supported
		1	15:0

3.1.3 DDR Mode (DDR_MODE_REGISTER)

Address: 0x18000008
Access: Read/Write
Reset: See field description

This register is used to set the DDR mode register value.

Bit	Bit Name	Reset	Description
12:0	VALUE	0x133	Mode register value. Reset to CAS 3, BL=8, Sequential, DLL reset off.
31:13	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.1.4 DDR Extended Mode (DDR_EXTENDED_MODE_REGISTER)

Address: 0x1800000C
Access: Read/Write
Reset: See field description

This register is used to set the extended DDR mode register value.

Bit	Bit Name	Reset	Description
12:0	VALUE	0x2	Extended mode register value. Reset to weak driver, DLL on.
31:13	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.1.5 DDR Control (DDR_CONTROL)

Address: 0x18000010
Access: Read/Write
Reset: 0x0

This register is used to force update cycles in the DDR control.

Bit	Bit Name	Description
0	MRS	Forces an MRS update cycle
1	EMRS	Forces an EMRS update cycle
2	REF	Forces an AUTO REFRESH cycle
3	PREA	Forces a PRECHARGE ALL cycle
4	EMR2	Forces an EMR2S update cycle
5	EMR3	Forces an EMR3S update cycle
31:6	RES	Reserved

3.1.6 DDR Refresh Control (DDR_REFRESH)

Address: 0x18000014
Access: Read/Write
Reset: See field description

This register is used to configure the settings to refresh the DDR,

Bit	Bit Name	Reset	Description
13:0	PERIOD	0x2000	Sets the refresh period intervals
14	ENABLE	0x0	Setting this bit will enable a DDR refresh
31:15	RES	0x0	Reserved

3.1.7 DDR Read Data Cycle (DDR_RD_DATA_THIS_CYCLE)

Address: 0x18000018
Access: Read/Write
Reset: 0xFFFF

This register is used to set the parameters to read the DDR and capture bit masks.

Bit	Bit Name	Description
23:0	VEC	DDR read and capture bit mask. Each bit represents a cycle of valid data. Set to 0xFFFF for 16-bit wide memory systems.
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.

3.1.8 DQS Delay Tap Control for Byte 0 (TAP_CONTROL_0)

Address: 0x1800001C
Access: Read/Write
Reset: See field descriptions

This register is used along with DQ Lane 0, DQ[7:0], DQS_0.

Bit	Bit Name	Reset	Description
4:0	TAP	0x5	Tap setting for delay chain
5	RES	0x0	Reserved
6	BYPASS_EN	0x0	Bypass enable. Short-circuits the first four taps directly to the output. Only used in the slow corner where absolute minimum delay is needed.
31:7	RES	0x0	Reserved

3.1.9 DQS Delay Tap Control for Byte 1 (TAP_CONTROL_1)

Address: 0x18000020
Access: Read/Write
Reset: See field descriptions

This register is used along with DQ Lane 1, DQ[15:8], DQS_1.

Bit	Bit Name	Reset	Description
4:0	TAP	0x5	Tap setting for delay chain
5	RES	0x0	Reserved
6	BYPASS_EN	0x0	Bypass enable. Short-circuits the first four taps directly to the output. Only used in the slow corner where absolute minimum delay is needed.
31:7	RES	0x0	Reserved

3.1.10 GE0 Interface Write Buffer Flush (DDR_WB_FLUSH_GE0)

Address: 0x1800007C
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the GE0 interface.

Bit	Bit Name	Description
0	FLUSH	Set this bit to 1 to flush the write buffer for the GE0 interface. This bit will reset to 0 when the flush is complete.
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.

3.1.11 GE1 Interface Write Buffer Flush (DDR_WB_FLUSH_GE1)

Address: 0x18000080
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the GE1 interface.

Bit	Bit Name	Type	Reset	Description
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the GE1 interface. This bit will reset to 0 when the flush is complete.
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.1.12 USB Interface Write Buffer Flush (DDR_WB_FLUSH_USB)

Address: 0x18000084
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the USB interface.

Bit	Bit Name	Type	Reset	Description
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the USB interface. This bit will reset to 0 when the flush is complete.
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.1.13 PCIE Interface Write Buffer Flush (DDR_WB_FLUSH_PCIE)

Address: 0x18000088
Access: Read/Write
Reset: 0x0

This register is used to flush the write buffer for the PCIE interface.

Bit	Bit Name	Type	Reset	Description
0	FLUSH	RW	0x0	Set this bit to 1 to flush the write buffer for the PCIE interface. This bit will reset to 0 when the flush is complete.
31:1	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.1.14 DDR Configuration (DDR_CONFIG)

Address: 0x1800008C
Access: Read/Write
Reset: 0x0858

Bit	Bit Name	Type	RW	Description	
0	ENABLE_DDR	RW	0x0	0	DDR1, must be set to 0
31:2	RES	RO	0x0	Reserved	

3.1.15 Extended Mode 2 (DDR_EMR2)

Address: 0x18000090
Access: Read/Write
Reset: 0x0

This register is used set the extended mode register 2 value.

Bit	Bit Name	Type	Reset	Description
12:0	VALUE	RW	0x0	Sets the extended mode register 2 value
31:13	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.1.16 Extended Mode 3 (DDR_EMR3)

Address: 0x18000094
Access: Read/Write
Reset: 0x0

This register is used set the extended mode register 3 value.

Bit	Bit Name	Type	Reset	Description
12:0	VALUE	RW	0x0	Sets the extended mode register 2 value
31:13	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.2 UART Registers

Table 3-3 summarizes the UART registers for the AR7240.

Table 3-3. **UART Registers Summary**

Address	Name	Description	Page
0x18020000	RBR	Receive Buffer	page 34
0x18020000	THR	Transmit Holding	page 34
0x18020000	DLL	Divisor Latch Low	page 35
0x18020004	DLH	Divisor Latch High	page 35
0x18020004	IER	Interrupt Enable	page 35
0x18020008	IIR	Interrupt Identity	page 36
0x18020008	FCR	FIFO Control	page 36
0x1802000C	LCR	Line Control	page 37
0x18020010	MCR	Modem Control	page 37
0x18020014	LSR	Line Status	page 38
0x18020018	MSR	Modem Status	page 39

3.2.1 Receive Buffer (RBR)

Address: 0x18020000
Access: Read-Only
Reset: 0x0

This read-only register contains the data byte received on the serial input port (SIN). The data in this register is only valid if the Data Ready (DR) bit in the Line Status Register (LSR) is set. In the non-FIFO mode (FIFO_MODE = 0), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. In FIFO mode (FIFO_MODE = 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already residing in the FIFO is full and this register will be preserved but any incoming data will be lost. An overrun will error will also occur.

Bit	Bit Name	Description
7:0	RBR	The receive buffer register value
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.

3.2.2 Transmit Holding (THR)

Address: 0x18020000
Access: Write-Only
Reset: 0x0

This write-only register contains data to be transmitted on the serial port (s_{OUT}). Data can be written to the THR any time the THR Empty (THRE) bit of the Line Status Register is set. If FIFOs are not enabled and the THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFOs are enabled and the THRE is set, up to sixteen characters of data may be written to the THR before the FIFO is full. Attempting to write data when the FIFO is full results in the write data being lost.

Bit	Bit Name	Description
7:0	THR	The transmit buffer value
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.

3.2.3 Divisor Latch Low (DLL)

Address: 0x18020000
Access: Read/Write
Reset: 0x0

This register, in conjunction with the Divisor Latch High (DLH) register forms a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. It is accessed by first setting the DLAB bit (bit 7) in the Line Control Register (LCR). The output baud rate is equal to the input clock frequency divided by sixteen times (*16) the value of the baud rate divisor:

baud = (clock freq)/ (16 * divisor)

Bit	Bit Name	Type	Reset	Description
7:0	DLL	RW	0x0	Divisor Latch Low
31:8	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.2.4 Divisor Latch High (DLH)

Address: 0x18020004
Access: Read/Write
Reset: 0x0

This register, in conjunction with the Divisor Latch Low (DLL) register forms a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. It is accessed by first setting the DLAB bit (bit 7) in the Line Control Register (LCR). The output baud rate is equal to the input clock frequency divided by sixteen times (*16) the value of the baud rate divisor:

baud = (clock freq)/ (16 * divisor)

Bit	Bit Name	Description
7:0	DLH	Divisor Latch High
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.

3.2.5 Interrupt Enable (IER)

Address: 0x18020004
Access: Read/Write
Reset: 0x0

This register contains four bits that enable the generation of interrupts. These four bits are the Enable Received Data Available Interrupt (ERBFI), the Enable Transmitter Holding Register Empty Interrupt (ETBEI), the Enable Receiver Line Status Interrupt (ELSI), and the Enable Modem Status Interrupt (EDSSI).

Bit	Bit Name	Description
0	ERBFI	Enable Received Data Available Interrupt
1	ETBEI	Enable Register Empty Interrupt
2	ELSI	Enable Receiver Line Status Interrupt
3	EDDSI	Enable Modem Status Interrupt
31:4	RES	Reserved. Must be written with zero. Contains zeros when read.

3.2.6 Interrupt Identity (IIR)

Address: 0x18020008
Access: Read-Only
Reset: 0x0

This read-only register identifies the source of an interrupt. The two upper bits of the register are FIFO-enabled bits.

Bit	Bit Name	Description	
3:0	IID	Used to identify the source of the interrupt	
		0000	Modem status changed
		0001	No interrupt pending
		0010	THR empty
		0100	Received data available
		0110	Receiver status
		1100	Character time out
5:4	RES	Reserved. Must be written with zero. Contains zeros when read.	
7:6	FIFO_STATUS	FIFO enable status bits	
		0	FIFO disabled
		1	FIFO enabled
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.	

3.2.7 FIFO Control (FCR)

Address: 0x18020008
Access: Write-Only
Reset: 0x0

This write-only register is used to set the parameters for FIFO control. If FIFO mode is 0, this register has no effect. If FIFO mode is 1, this register will control the read and write data FIFO operation and the mode of operation for the DMA signals TXRDY_N and RXRDY_N. Setting bit 0 enables the transmit and receive FIFOs. Writing a one to bit 1 resets and flushes data in the receive FIFO while writing a one to bit 2 resets and flushes data in the transmit FIFO. FIFOs are reset anytime bit 0 changes value. If the FIFO mode is enabled, (FIFO mode = 1 and bit 0 is set to 1) bits 3, 6, and 7 are active. Bit 3 determines the DMA signalling mode for TXRDY_N and RXRDY_N output signals. Bit 6 and bit 7 set the trigger level in the receiver FIFO for both the RXRDY_N signal and the Enable Received Data Available Interrupt (ERBFI). This register will also return current time values.

Bit	Bit Name	Description	
0	FIFO_EN	Setting this bit enables the transmit and receive FIFOs. The FIFOs are also reset any time this bit changes its value.	
1	RCVR_FIFO_RST	Writing this bit resets and flushes data in the receive FIFO	
2	XMIT_FIFO_RST	Writing this bit resets and flushes data in the transmit FIFO	
3	DMA_MODE	This bit determines the DMA signalling mode for TXRDY_N and RXRDY_N output signals	
5:4	RES	Reserved. Must be written with zero. Contains zeros when read.	
7:6	RCVR_TRIG	This bit sets the trigger level in the receiver FIFO for both the RXRDY_N signal and the Enable Received Data Available Interrupt (ERBFI)	
		00	1 byte in FIFO
		01	4 bytes in FIFO
		10	8 bytes in FIFO
		11	14 bytes in FIFO
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.	

3.2.8 Line Control (LCR)

Address: 0x1802000C
Access: Read/Write
Reset: 0x0

This register controls the format of the data that is transmitted and received by the UART controller.

Bit	Bit Name	Description	
1:0	CLS	Used to control the number of bits per character	
		00	5 bits
		01	6 bits
		10	7 bits
		11	8 bits
2	STOP	Used to control the number of stop bits transmitted. If bit 2 is a logic 0, one stop bit is transmitted in the serial data. If bit 2 is a logic 1 and the data bits are set to 5, one and a half stop bits are generated. Otherwise, two stop bits are generated and transmitted in the serial data out.	
3	PEN	Used to enable parity when set	
4	EPS	Used to set the Even/Odd Parity. If parity is enabled, this bit selects between even and odd parity. If this bit is a logic 1, an even number of logic 1s are transmitted or checked. If this bit is a logic 0, an odd number of logic 1s are transmitted or checked.	
5	RES	Reserved. Must be written with zero. Contains zeros when read.	
6	BREAK	Setting this bit sends a break signal by holding the SOUT line low (when not in Loopback Mode, as determined by Modem Control Register bit 4), until the BREAK bit is cleared. When in loopback Mode, the break condition is internally looped back to the receiver.	
7	DLAB	The divisor latch address bit. Setting this bit enables reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after the initial baud rate setup in order to access the other registers.	
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.	

3.2.9 Modem Control (MCR)

Address: 0x18020010
Access: Read/Write
Reset: See field description

This register controls the interface with the modem.

Bit	Bit Name	Reset	Description
0	DTR	0x1	Used to drive the UART output DTR_L. Not supported.
1	RTS	0x1	Used to drive the UART output RTS_L
2	OUT1	0x1	Used to drive the UART output UART_OUT1_L. Not supported.
3	OUT2	0x1	Used to drive the UART output UART_OUT2_L. Not supported.
4	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
5	LOOPBACK	0x1	When set, the data on the SOUT line is held HIGH, while the serial data output is looped back to the SIN line, internally. In this mode, all the interrupts are fully functional. This feature is also used for diagnostic purposes. The modem control inputs (DSR_L, CTS_L, RI_L, DCD_L) are disconnected and the four modem control outputs (DTR_L, RTS_L, OUT1_L, OUT1_L) are looped back to the inputs, internally.
31:6	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.2.10 Line Status (LSR)

Address: 0x18020014
Access: Read/Write
Reset: 0x0

This register contains the status of the receiver and transmitter data transfers. This status may be read by the user at any time.

Bit	Bit Name	Description
0	DR	The data ready bit. When set, indicates that the receiver contains at least one character in the RBR or the receiver FIFO. This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty when in FIFO mode.
1	OE	The overrun error bit. When set, indicates an overrun error has occurred because a new data character was received before the previous data was read. In non-FIFO mode, this bit is set when a new character arrives in the receiver before the previous character has been read from the RBR. In FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives in the receiver. The data in FIFO is retained and the data in the receive shift register is lost.
2	PE	The parity error bit. This bit is set whenever there is a parity bit error in the receiver if the Parity Enable (PEN) bit in the LCR is set. In FIFO mode, the parity error associated with the character received will come to the top of FIFO so it can be noticed.
3	FE	The framing error bit. This bit is set whenever there is a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In FIFO mode, the framing error associated with the character received will come to the top of FIFO so it can be noticed. The OE, PE and FE bits are reset when a read of the LSR is performed.
4	BI	The break interrupt bit. This bit is set whenever the serial input (SIN) is held in a logic zero state for longer than the sum of (start time + data bits + parity + stop bits). A break condition on SIN causes one, and only one character, consisting of all zeros which will be received by the UART. In FIFO mode, the character associated with the break condition is carried through FIFO and revealed when the character reaches the top of FIFO. Reading the LSR clears the BI bit. In non-FIFO mode, the BI direction occurs immediately and continues until the LSR has been read.
5	THRE	The transmitter holding register empty bit. When set, indicates the UART controller can accept a new character for transmission. This bit is set whenever data is transferred from the THR to the transmit shift register and no new data has been written to the THR. This also causes a THRE Interrupt to occur, if enabled.
6	TEMT	The transmitter empty bit. This bit is set in FIFO mode whenever the Transmitter Shift Register and the FIFO are both empty. In non-FIFO mode, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
7	FERR	The error in receiver FIFO bit. This bit is only active when the FIFOs are enabled. This bit is set when there is at least one parity error, framing error or break in the FIFO. This bit is cleared when the LSR is read AND the character with the error is at the top of the receiver FIFO AND there are no subsequent errors in the FIFO.
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.

3.2.11 Modem Status (MSR)

Address: 0x18020018
Access: Read/Write
Reset: 0x0

This register contains the current status of the modem control input lines and if they have changed.

Bit	Bit Name	Description
0	DCTS	This bit records whether the modem control line CTS_L has changed since the last time the CPU read the MSR
1	DDSR	This bit records whether the modem control line DSR_L has changed since the last time the CPU read the MSR. Not supported.
2	TERI	This bit indicates if the RI_L has changed from an active low, to an inactive high state since the last time the MSR was read
3	DDCD	This bit records whether the modem control line DCD_L has changed since the last time the CPU read the MSR. Not supported.
4	CTS	This bit contains information on the current state of the modem control lines. CTS (bit [4]) is the compliment of CTS_L.
5	DSR	This bit contains information on the current state of the modem control lines. DSR (bit [5]) is the compliment of DSR_L. Not supported.
6	RI	This bit contains information on the current state of the modem control lines. RI (bit [6]) is the compliment of RI_L. Not supported.
7	DCD	This bit contains information on the current state of the modem control lines. DCD (bit [6]) is the compliment of DCD_L. Not supported.
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.

3.3 GPIO Registers

Table 3-4 summarizes the GPIO registers for the AR7240.

Table 3-4. **GPIO Registers Summary**

Address	Name	Description	Page
0x18040000	GPIO_OE	General Purpose I/O Output Enable	page 40
0x18040004	GPIO_IN	General Purpose I/O Input Value	page 40
0x18040008	GPIO_OUT	General Purpose I/O Output Value	page 41
0x1804000C	GPIO_SET	General Purpose I/O Bit Set	page 41
0x18040010	GPIO_CLEAR	General Purpose I/O bit Clear	page 41
0x18040014	GPIO_INT	General Purpose I/O Interrupt Enable	page 41
0x18040018	GPIO_INT_TYPE	General Purpose I/O Interrupt Type	page 42
0x1804001C	GPIO_INT_POLARITY	General Purpose I/O Interrupt Polarity	page 42
0x18040020	GPIO_INT_PENDING	General Purpose I/O Interrupt Pending	page 42
0x18040024	GPIO_INT_MASK	General Purpose I/O Interrupt Mask	page 42
0x18040028	GPIO_FUNCTION	General Purpose I/O Function	page 43

3.3.1 GPIO Output Enable (GPIO_OE)

Address: 0x18040000
Access: Read/Write
Reset: 0x0

This register is used to enable the per bit output or input.

Bit	Bit Name	Description	
17:0	OE	Used to enable output or input per bit	
		0	Enables this register to be used as an input.
		1	Enables this register to be used as an output
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.	

3.3.2 GPIO Input Value (GPIO_IN)

Address: 0x18040004
Access: Read-Only
Reset: 0x0

This register denotes the current values of each of the GPIO pins.

Bit	Bit Name	Description
17:0	IN	Denotes the current values of each of the GPIO pins.
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.3.3 GPIO Output Value (GPIO_OUT)

Address: 0x18040008
Access: Read/Write
Reset: 0x0

This register denotes the driver output value.

Bit	Bit Name	Description
17:0	OUT	Denotes the driver output value. Setting the corresponding bit in the OE register to 1 will drive the value in the corresponding bit of this register.
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.3.4 GPIO Per Bit Set (GPIO_SET)

Address: 0x1804000C
Access: Write-Only
Reset: 0x0

The bit of this register is set in response to other bits being set.

Bit	Bit Name	Description
17:0	SET	When writing, any bit that is set will cause the corresponding GPIO bit to be set. Any bit that is not set will have no effect.
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.3.5 GPIO Per Bit Clear (GPIO_CLEAR)

Address: 0x18040010
Access: Write-Only
Reset: 0x0

The bit of this register is set in response to other bits being cleared.

Bit	Bit Name	Description
17:0	SET	When writing, any bit that is set will cause the corresponding GPIO bit to be cleared. Any bit that is not set will have no effect.
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.3.6 GPIO Interrupt Enable (GPIO_INT)

Address: 0x18040014
Access: Read/Write
Reset: 0x0

The register sets the bit for interrupts into GPIO lines.

Bit	Bit Name	Description
17:0	INT	For each bit set, that bit will be considered an interrupt into the GPIO interrupt line
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.3.7 GPIO Interrupt Type (GPIO_INT_TYPE)

Address: 0x18040018
Access: Read/Write
Reset: 0x0

This register is used to set the interrupt type for GPIOs.

Bit	Bit Name	Description	
17:0	TYPE	Used to set the type of interrupt	
		0	This bit is an edge-sensitive interrupt
		1	This bit is a level-sensitive interrupt
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.	

3.3.8 GPIO Interrupt Polarity (GPIO_INT_POLARITY)

Address: 0x1804001C
Access: Read/Write
Reset: 0x0

This register is used to indicate the level and edge status of the GPIO interrupt.

Bit	Bit Name	Description	
17:0	POLARITY	Each bit controls the corresponding GPIO interrupt polarity	
		0	Indicates that the interrupt is active low (level) or falling edge (edge)
		1	Indicates that the interrupt is active high (level) or rising edge (edge)
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.	

3.3.9 GPIO Interrupt Pending (GPIO_INT_PENDING)

Address: 0x18040020
Access: Read/Write
Reset: 0x0

This register is used to indicate current pending interrupts.

Bit	Bit Name	Description
17:0	PENDING	Indicates that an interrupt is currently pending for a GPIO bit. For edge sensitive interrupts, this register is read-with-clear.
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.3.10 GPIO Interrupt Mask (GPIO_INT_MASK)

Address: 0x18040024
Access: Read/Write
Reset: 0x0

This register is used to send interrupt messages to the central controller.

Bit	Bit Name	Description
17:0	MASK	When set, the corresponding control in the INT_PENDING register is passed on to the centra1 interrupt controller.
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.3.11 GPIO Function (GPIO_FUNCTION)

Address: 0x18040028
Access: Read/Write
Reset: 0x0

This register is used to enable and disable the functionality of certain multiplexed GPIO pins.

Bit	Bit Name	Description
0	JTAG_DISABLE	This bit disables JTAG functionality in GPIO pins 6, 7, and 8. This bit also enables GPIO functionality.
1	UART_EN	Enables UART I/O on GPIO pins 9 and 10
2	UART_RTS_CTS_EN	This bit enables UART RTS/CTS on pins GPIO pins 11 and 12
7:3	ETH_SWITCH_ LEDX_EN	This bit enables Link LED indication for the five Ethernet ports on GPIO pins 13-17
8	CLK_OBS1_ ENABLE	This bit enables observation of the divide by 2 version of the PCIE_CORE_CLK (125 MHz) on pin GPIO_13
9	CLK_OBS2_ ENABLE	This bit enables observation of the 25MHz reference clock to the Ethernet Switch on pin GPIO_14
10	CLK_OBS3_ ENABLE	This bit enables observation of the divide by 4 version of the AHB_CLK (200 MHz) on pin GPIO_15
11	CLO_OBS4_ ENABLE	This bit enables the observation of the USB 48 MHz signal on pin GPIO_16
12	CLK_OBS5_ ENABLE	This bit enables observation of the GE1 125 MHz clock on pin GPIO_17
13	SPI_CS_EN1	Enables GPIO_0 as an additional SPI chip select output
14	SPI_CS_EN2	Enables pin GPIO_1 as an additional SPI chip select output
15	RES	Reserved. This pin must be written with 1.
17:16	RES	Reserved. Must be written with zero. Contains zeros when read.
18	SPI_EN	Enables SPI function on the GPIO pins
19	GE0_MII_CLK_ EN	Enables observation of the 25 MHz GE0 clock from Ethernet Switch on pin GPIO_1
31:20	RES	Reserved. Must be written with zero. Contains zeros when read.

3.4 PLL Control Registers

Table 3-5 summarizes the AR7240 PLL control registers.

Table 3-5. **PLL Control Registers Summary**

Address	Name	Description	Page
0x18050000	CPU_PLL_CONFIG	CPU Phase Lock Loop Configuration	page 44
0x18050004	ETH_USB_PLL_CONFIG	USB Phase Lock Loop Configuration	page 45
0x18050008	CPU_CLOCK_CONTROL	CPU Clock Control	page 45
0x1805000C	CPU_SYNC	Processor Core SI_OCP Synch Generation	page 45
0x18050010	PCIE_PLL_CONFIG	PCIE Phase Lock Loop Configuration	page 46
0x18050014	PCIE_PLL_MAX_LIMIT	PCIE PLL Dither Maximum Limit	page 46
0x18050018	PCIE_PLL_MIN_LIMIT	PCIE PLL Dither Minimum Limit	page 46
0x1805001C	PCIE_PLL_UPDATE_STEP	PCIE PLL Dither Update Step	page 47
0x1805002C	LDO_CONTROL_SELECT	LDO Control Select	page 47
0x18050030	ETH_CLOCK_SPARE	Ethernet Switch Clock Control	page 47
0x18050034	CURRENT_PCIE_PLL_DITHER	Current PCIE PLL Dither	page 47

3.4.1 CPU Phase Lock Loop Configuration (CPU_PLL_CONFIG)

Address: 0x18050000
Access: Read/Write
Reset: See field description

Provides access to the PLL setup control signals. Any write to this register freezes all high-speed clocks for 61 µs. The clock select lines and PLL control lines will change after 30.5 µs, then another 30.5 µs will pass before being enabled to allow the clocks to settle.

Bit	Bit Name	Reset	Description
9:0	DIV	0x28	The primary multiplier
13:10	REFDIV	0x2	Reference clock divider
15:14	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
16	BYPASS	0x1	The bypass PLL. This bit defaults to 1 for testing purposes. Software must enable the PLL for normal operation.
17	UPDATING	0x0	This bit is set during the PLL update process. After software writes to the PLL_CONTROL register, it takes about 45 µs for the update to occur. Software may poll this bit to see if the update has taken place.
			0 PLL update completed
			1 PLL update pending
18	NOPWD	0x0	This bit prevents the PLL from being powered down when the PLL bypass is asserted or when it is in light sleep
19	AHB_DIV	0x1	The AHB clock divisor
			0 Divide by 2
			1 Divide by 4
21:20	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
23:22	DDR_DIV_SEL	0x0	DDR clock divisor
			0 Divide by 1
			1 Divide by 2
24	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
25	RESET	0x1	CPU PLL reset
31:26	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.4.2 USB Phase Lock Loop Configuration (ETH_USB_PLL_CONFIG)

Address: 0x18050004
Access: See field description
Reset: See field description

Provides access to the PLL setup control signals. Any write to this register will freeze all high-speed clocks for 61 µs. The clock select lines and PLL control lines will change after 30.5 µs, then another 30.5 µs will pass before being enabled to allow the clocks to settle.

Bit	Bit Name	Type	Reset	Description
9:0	DIV	RW	0x1E	The primary multiplier
13:10	REFDIV	RW	0x2	Reference clock divider
15:14	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
16	BYPASS	RW	0x1	The bypass PLL. This bit defaults to 1 for testing purposes. Software must enable the PLL for normal operation.
17	UPDATING	RO	0x0	This bit is set during the PLL update process. After software writes to the PLL_CONTROL register, it takes about 45 µs for the update to occur. Software may poll this bit to see if the update has taken place.
				0 PLL update completed
				1 PLL update pending
18	NOPWD	RW	0x0	This bit prevents the PLL from being powered down when the PLL bypass is asserted or when it is in light sleep
19	PLL_RESET	RW	0x1	Resets the PLL dividers
24:20	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
25	RESET	RW	0x1	USB PLL reset
31:26	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.4.3 CPU Clock Control (CPU_CLOCK_CONTROL)

Address: 0x18050008
Access: Read/Write
Reset: 0x0

Sets and resets the clock switch.

Bit	Bit Name	Description
0	CLOCK_SWITCH	The clock switch trigger
1	RESET_SWITCH	Reset during the clock switch trigger
31:2	RES	Reserved. Must be written with zero. Contains zeros when read.

3.4.4 Processor Core SI_OCPSync Generation (CPU_SYNC)

Address: 0x1805000C
Access: Read/Write
Reset: See field description

Sets the maximum limits of the fractional and integer parts.

Bit	Bit Name	Reset	Description
15:0	PATTERN	0xFFFF	The pattern executed on SI_OCPSync from the LSB to the MSB
19:16	LENGTH	0x0	The length of the pattern +1
31:20	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.4.5 PCIE Phase Lock Loop Configuration (PCIE_PLL_CONFIG)

Address: 0x18050010
Access: See field description
Reset: See field description

Provides access to the PLL setup control signals. Any write to this register will freeze all high speed clocks for 61 µs. The clock select lines and PLL control lines will change after 30.5 µs, then another 30.5 µs passes before enable to allow the clocks to settle.

Bit	Bit Name	Type	Reset	Description
9:0	DIV	RW	0x50	Primary multiplier
13:10	REFDIV	RW	0x4	Reference clock divider
15:14	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
16	BYPASS	RW	0x1	Bypass PLL. This defaults to 1 for test purposes. Software must enable the PLL for normal operation.
17	UPDATING	RO	0x0	This bit is set during the PLL update. After software writes PLL_CONTROL, it takes about 45 µs for the update to occur. Software may poll this bit to see if the update has taken place. 0 PLL update is complete 1 PLL update is pending
18	NOPWD	RW	0x0	Prevents the PLL from being powered down when PLLBYPASS is asserted or when in light sleep.
24:19	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
25	RESET	RW	0x1	PCIE PLL reset
31:26	RES	0x0	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.4.6 PCIE PLL Dither Maximum Limit (PCIE_PLL_MAX_LIMIT)

Address: 0x18050014
Access: Read/Write
Reset: See field description

Sets the maximum limits of the fractional and integer parts.

Bit	Bit Name	Reset	Description
14:0	DIVFRAC_MAX	0x0	The maximum limit of the fractional part. Ideally, this should be set to decimal 32758.
24:15	DIVINT_MAX	0x19	The maximum limit of the integer part. Ideally this should be set to decimal 19.
29:25	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
30	USE_MAX	0x1	This bit forces the maximum value specified to be used. This bit is effective only when the EN_DITHER is set to 0.
31	EN_DITHER	0x1	Used to disable the dither logic. If disabled, either the maximum value or the minimum is used, depending on the USE_MAX bit setting.

3.4.7 PCIE PLL Dither Minimum Limit (PCIE_PLL_MIN_LIMIT)

Address: 0x18050018
Access: Read/Write
Reset: See field description

Sets the maximum limits of the fractional and integer parts.

Bit	Bit Name	Reset	Description
15:0	DIVFRAC_MIN	0x29498	The minimum limit of the fractional part
23:16	DIVINT_MIN	0x19	The minimum limit of the integer part
31:24	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.4.8 PCIE PLL Dither Update Step (PCIE_PLL_UPDATE_STEP)

Address: 0x1805001C
Access: Read/Write
Reset: See field description

Sets and resets the clock switch.

Bit	Bit Name	Reset	Description
14:0	STEP_FRAC	0x010	This bit specifies the quantum by which the fractional part of the fractional divider needs to be updated for each update
24:15	STEP_INT	0x0	These bits represent the integer part of the step value of the divider
31:28	UPDATE_COUNT	0x0	Specifies the number of sigma-delta clocks per update

3.4.9 LDO Control Select (LDO_CONTROL_SELECT)

Address: 0x1805002C
Access: Read-Only
Reset: See field description

Provide status of the DDP selection and CPU/DDR reference voltage.

Bit	Bit Name	Reset	Description
0	DDR1_SEL	0x1	Reflects the status of the PC_DDR_SEL pin input.
2:1	CPU_REFSEL	0x3	Indicates the selected CPU/DDR reference voltage
31:3	RES	0x0	Reserved

3.4.10 Ethernet Clock Control (ETH_CLOCK_SPARE)

Address: 0x18050030
Access: Read-Only
Reset: 0x0

This register determines the source of the source of the 25 MHz clock to the Ethernet Switch.

Bit	Bit Name	Description	
0	ETH_CLK	Determines the source of the 25 MHz clock to Ethernet Switch	
		0	The clock is taken from the Ethernet PLL
		1	The 25 MHz XTAL clock source is used
31:1	RES	Reserved	

3.4.11 Current PCIE PLL Dither (CURRENT_PCIE_PLL_DITHER)

Address: 0x18050034
Access: Read-Only
Reset: 0x0

This register is used to indicate the parts of the divider.

Bit	Bit Name	Description
14:0	FRAC	Indicates the fractional part of the DivFrac to the PCIE PLL
24:15	INT	Indicates the integer part of the DivInt to the PCIE PLL
31:25	RES	Reserved

3.5 Reset Control Registers

Table 3-6 summarizes the AR7240 reset control registers.

Table 3-6. **Reset Control Registers Summary**

Address	Name	Description	Page
0x18060000	RST_GENERAL_TIMER0	General Purpose Timer 0	page 48
0x18060004	RST_GENERAL_TIMER0_RELOAD	General Purpose Timer 0 Reload	page 48
0x18060008	RST_WATCHDOG_TIMER_CONTROL	Watchdog Timer Control	page 49
0x1806000C	RST_WATCHDOG_TIMER	Watchdog Timer	page 49
0x18060010	RST_MISC_INTERRUPT_STATUS	Miscellaneous Interrupt Status	page 50
0x18060014	RST_MISC_INTERRUPT_MASK	Miscellaneous Interrupt Mask	page 51
0x18060018	RST_GLOBAL_INTERRUPT_STATUS	Global Interrupt Status	page 51
0x1806001C	RST_RESET	Reset	page 52
0x18060094	RST_GENERAL_TIMER1	General Purpose Timer 1	page 48
0x18060098	RST_GENERAL_TIMER1_RELOAD	General Purpose Timer 1 Reload	page 48
0x1806009C	RST_GENERAL_TIMER2	General Purpose Timer 2	page 48
0x180600A0	RST_GENERAL_TIMER2_RELOAD	General Purpose Timer 2 Reload	page 48
0x180600A4	RST_GENERAL_TIMER3	General Purpose Timer 3	page 48
0x180600A8	RST_GENERAL_TIMER3_RELOAD	General Purpose Timer 3 Reload	page 48
0x18060090	RST_REVISION_ID	Chip Revision ID	page 52

3.5.1 General Purpose Timers (RST_GENERAL_TIMER)

Timer0 Address: 0x18060000
Timer1 Address: 0x18060094
Timer2 Address: 0x1806009C
Timer3 Address: 0x180600A4
Access: Read/Write
Reset: 0x0

This timer counts down to zero, sets, interrupts, and then reloads from the General Timer Reload register. This definition holds true for timer0, timer1, timer2, and timer3.

Bit	Bit Name	Type	Reset	Description
31:0	TIMER	RW	0x0	Timer value

3.5.2 General Purpose Timers Reload (RST_GENERAL_TIMER_RELOAD)

Timer0 Reload Address: 0x18060004
Timer1 Reload Address: 0x18060098
Timer2 Reload Address: 0x180600A0
Timer3 Reload Address: 0x180600A8
Access: Read/Write
Reset: 0x0

This register contains the value that will be loaded into the General Timer register when it decrements to zero. This definition holds true for timer 0, timer1, timer2, and timer3.

Bit	Bit Name	Description
31:0	RELOAD_VALUE	Timer reload value

3.5.3 Watchdog Timer Control Register (RST_WATCHDOG_TIMER_CONTROL)

Address: 0x18060008
Access: See field description
Reset: 0x0

Sets the action to take when the watchdog timer reaches zero. The options are reset, non-maskable interrupt and general purpose interrupt after reaching zero.

Bit	Bit Name	Type	Description	
1:0	ACTION	RW	The action to be taken after the timer reaches zero	
			00	No action
			01	General purpose interrupt
			10	Non-maskable interrupt
			11	Full chip reset
30:2	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
31	LAST	RO	Indicates if the last reset was due to a watchdog timeout	

3.5.4 Watchdog Timer Register (RST_WATCHDOG_TIMER)

Address: 0x1806000C
Access: Read/Write
Reset: 0x0

Specifies the action for the watchdog timer control to take when this watchdog timer reaches zero.

Bit	Bit Name	Description
31:0	TIMER	Counts down to zero and stays at zero until the software sets this timer to another value. These bits should be set to a non-zero value before updating the "Watchdog Timer Control Register (RST_WATCHDOG_TIMER_CONTROL)" register to a non-zero number.

3.5.5 Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS)

Address: 0x18060010
Access: Read-Write to Clear
Reset: 0x0

Sets the current state of the interrupt lines that are combined to form the MiscInterupt to the processor. All bits of this register need a write to clear.

Bit	Bit Name	Description
0	TIMER_INT	Interrupt occurring in correspondence to the general purpose timer0. This bit is cleared after being read. The timer has already been reloaded from the General Timer Reload register.
1	ERROR_INT	An interrupt caused by an error on the internal PIO bus. Error logic registers must be read and cleared before this interrupt can be cleared.
2	GPIO_INT	The GPIO interrupt. Individual lines must be masked before this interrupt can be cleared.
3	UART_INT	The UART interrupt. UART interrupt registers must be read before this interrupt can be cleared.
4	WATCHDOG_ INT	The Watchdog Timer interrupt. This interrupt is generated when the Watchdog Timer reaches zero and the Watchdog Configuration register is configured to generate a general-purpose interrupt.
7:5	RES	Reserved. Must be written with zero. Contains zeros when read.
8	TIMER1_INT	The interrupt corresponding to General Purpose Timer1. This bit has been cleared after being read. The timer will be immediately reloaded from the General Timer Reload register.
9	TIMER2_INT	The interrupt corresponding to General Purpose Timer2. This bit has been cleared after being read. The timer will be immediately reloaded from the General Timer Reload register.
10	TIMER3_INT	The interrupt corresponding to General Purpose Timer3. This bit is cleared after being read. The timer has been immediately reloaded from the General Timer Reload register.
11	RES	Reserved. Must be written with zero. Contains zeros when read.
12	ETH_MAC_INT	The interrupt generated by the Ethernet Switch.
31:13	RES	Reserved. Must be written with zero. Contains zeros when read.

3.5.6 Miscellaneous Interrupt Mask (RST_MISC_INTERRUPT_MASK)

Address: 0x18060014
Access: Read/Write
Reset: 0x0

Enables or disables a propagation of interrupts in the "Miscellaneous Interrupt Status (RST_MISC_INTERRUPT_STATUS)" register.

Bit	Bit Name	Description	
0	TIMER_MASK	Used to enable or disable the TIMER interrupt	
		0	Timer interrupt disabled
		1	Timer interrupt enabled
1	ERROR_MASK	Used to enable or disable the Error interrupt	
		0	Error interrupt disabled
		1	Error interrupt enabled
2	GPIO_MASK	Used to enable or disable the GPIO interrupt	
		0	GPIO interrupt disabled
		1	GPIO interrupt enabled
3	UART_MASK	Used to enable and disable the UART interrupt	
		0	UART interrupt disabled
		1	UART interrupt enabled
4	WATCHDOG_ MASK	Used to enable or disable the Watchdog interrupt	
		0	Watchdog interrupt disabled
		1	Watchdog interrupt enabled
7:5	RES	Reserved. Must be written with zero. Contains zeros when read.	
8	TIMER1_MASK	Used to enable and disable the TIMER1 interrupt	
		0	TIMER1 interrupt disabled
		1	TIMER1 interrupt enabled
9	TIMER2_MASK	Used to enable and disable the TIMER2 interrupt	
		0	TIMER2 interrupt disabled
		1	TIMER2 interrupt enabled
10	TIMER3_MASK	Used to enable and disable the TIMER3 interrupt	
		0	TIMER3 interrupt disabled
		1	TIMER3 interrupt enabled
11	RES	Reserved. Must be written with zero. Contains zeros when read.	
12	ETH_MAC_INT_MASK	Enables the interrupt generated ny the Ethernet Switch.	
31:11	RES	Reserved. Must be written with zero. Contains zeros when read.	

3.5.7 Global Interrupt Status (RST_GLOBAL_INTERRUPT_STATUS)

Address: 0x18060018
Access: Read-Only
Reset: 0x0

A duplication of the CPU Cause Register. During normal operations, it should be not used by software. Software can force interrupts for testing by writing bits into this register.

Bit	Bit Name	Description
0	PCIE_INT	The interrupt corresponding to PCIE. This bit is cleared after read.
1	USB_INT	The interrupt corresponding to USB. This bit is cleared after read.
2	GE0_INT	The interrupt corresponding to Ethernet 0. This bit is cleared after read.
3	GE1_INT	The interrupt corresponding to Ethernet 1. This bit is cleared after read.
4	MISC_INT	The Misc interrupt. This bit is cleared after being read.
5	TIMER_INT	The interrupt corresponding to the internal count/compare timer; cleared after read.
31:6	RES	Reserved. Must be written with zero. Contains zeros when read.

3.5.8 Reset (RST_RESET)

Address: 0x1806001C
Access: Read/Write
Reset: See field description

This register individually controls the reset to each of the chip's submodules.

Bit	Bit Name	Reset	Description
2:0	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
3	USB_OHCI_DLL_ RESET	0x1	Used to reset the Open Host Controller Interface
4	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
5	USB_HOST_RESET	0x1	Used to reset the USB Host Controller
6	PCIE_RESET	0x1	Used to reset the PCIE Host Controller. This bit will reset the Endpoint as well.
7	PCIE_PHY_RESET	0x1	Used to reset the PCIE Host Controller
8	ETH_SWITCH_ RESET	0x1	Resets the Ethernet Switch
9	GE0_MAC_RESET	0x1	Asserts the GE0 MAC reset
10	PCIE_PHY_SERIAL_ RESET	0x1	Resets the PCIE PHY Shift reset
12:11	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
13	GE1_MAC_RESET	0x1	Used to reset the GE1 MAC
15:14	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
16	DDR_RESET	0x0	Used to reset the DDR controller
19:17	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
20	CPU_COLD_RESET	0x0	Used to cold reset the CPU. Always zero when read.
21	CPU_NMI	0x0	Used to send an NMI to the CPU. Always zero when read.
23:22	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
24	FULL_CHIP_RESET	0x0	Used to command a full chip reset. This is the software equivalent of pulling the reset pin. The system will reboot with PLL disabled. Always zero when read.
27:25	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
28	EXTERNAL_RESET	0x0	Commands an external reset (SYS_RST_L pin); inverted before being sent to the pin.
31:29	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.5.9 Chip Revision ID (RST_REVISION_ID)

Address: 0x18060090
Access: Read-Only
Reset: See field description

This register is the revision ID for the chip.

Bit	Bit Name	Reset	Description
3:0	MINOR	0x0	Minor revision ID
7:4	MAJOR	0xC	Major revision ID
31:8	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.6 PCIE Local Registers

Table 3-7 summarizes the AR7240 PCIE local registers.

Table 3-7. **PCIE Local Registers Summary**

Address	Name	Description	Page
0x180F0000	PCIE_APP	PCIE Application Control	page 54
0x180F0004	PCIE_AER	PCIE Interrupt and Error	page 54
0x180F0008	PCIE_PWR_MGMT	PCIE Power Management	page 55
0x180F0010	PCIE_CFG	PCIE Configuration	page 55
0x180F0014	PCIE_RX_CNTL	PCIE Receive Completion	page 56
0x180F0018	PCIE_RESET	PCIE Reset	page 56
0x180F001C	PCIE_DEBUG	PCIE Debug Register	page 57
0x180F0024	PCIE_PHY_RW_DATA	PCIE PHY Serial Interface Read/Write Data	page 57
0x180F0028	PCIE_PHY_TRG_RD_LOAD	PCIE PHY Serial Interface Trigger Read or Load	page 58
0x180F002C	PCIE_PHY_CFG_DATA	PCIE PHY Configuration Data	page 58
0x180F0030	PCIE_MAC_PHY	PCIE MAC-PHY Interface Signals	page 58
0x180F0034	PCIE_PHY_MAC	PCIE PHY-MAC Interface Signals	page 59
0x180F0038	PCIE_SIDEBAND1	PCIE Sideband Bus 1	page 59
0x180F003C	PCIE_SIDEBAND2	PCIE Sideband Bus 2	page 59
0x180F0040	PCIE_SPARE	PCIE Spare Bits	page 60
0x180F0044	PCIE_MSI_ADDR	PCIE MSI Lower Address Register	page 60
0x180F0048	PCIE_MSI_DATA	PCIE MSI Data Value	page 60
0x180F004C	PCIE_INT_STATUS	PCIE Interrupt Status Register	page 61
0x180F0050	PCIE_INT_MASK	PCIE Interrupt Mask Register	page 61

3.6.1 PCIE Application Control (PCIE_APP)

Address: 0x180F0000
Access: Read/Write
Reset: See field description

This register is used to map error responses and generate unlock messages.

Bit	Bit Name	Reset	Description
0	LTSSM_ENABLE	0x0	Application signal to enable the LTSSM. If set to zero, it indicates that the application is not ready.
1	UNLOCK_MSG	0x0	Application signal to generate unlock message. This is to support legacy PCI Lock transactions. If the RC has sent a lock transaction it would need to assert this signal to unlock the path through the PCIE fabric which is locked.
2	PM_XMT_TURN OFF	0x0	Application signal to generate PM turnoff messages for power management
3	INIT_RST	0x0	Application request to initiate a training reset
5:4	MSTR_RESP_ERR _MAP	0x0	AHB master response error map. This signal allows the application to select a master response error report mechanism received from an AHB response channel to the CPL status of native PCIE core transmissions. MSB is not currently used. ■ When the LSB is set to 1, it will set an AHB response error to a UR of a PCIE completion. ■ When the LSB is set to 0, it will set an AHB response error to a CA of a PCIE completion: 2 bits == {decerr, slverr}
			0 — ERR goes to completed aborts
			1 — ERR goes to unsupported requests
11:6	SLV_RESP_ERR_ MAP	0x3F	AHB slave response error map**.** This signal allows the application to select a slave response error report mechanism received from a PCIE completion. There are six kinds of PCIE completion errors that the core can report to the AHB interface. The application can choose to not assert the AHB response error as a slave. 6 bits == {completion_tlp_abort, completion_ecrc, completion_ep, completion_crs, completion_ca, completion_ur}, where:
			1'b0 — SLVERR
			1'b1 — DECERR
31:12	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.6.2 PCIE Interrupt and Error (PCIE_AER)

Address: 0x180F0004
Access: Read-Only
Reset: 0x0

This register is used to set the advanced error interrupt message number.

Bit	Bit Name	Description
4:0	INT_MSG_NUM	Advanced error interrupt message number. Used when the message signalled interrupts or extended MSI is enabled
31:5	RES	Reserved. Must be written with zero. Contains zeros when read.

3.6.3 PCIE Power Management (PCIE_PWR_MGMT)

Address: 0x180F0008
Access: Read/Write
Reset: See field description

This register is used to set the configurations for the PCIE power.

Bit	Bit Name	Description
0	AUX_PWR_DET	Auxiliary power detected. Used to indicate that the auxiliary power is present
1	REQ_ENTRY_L1	The capability for applications to request the PM state to enter L1. This bit is only effective when the ASPM of L1 is enabled.
2	REQ_EXIT_L1	The request from the application to exit ASPM state L1. This bit is only effective if L1 is enabled.
3	READY_ENTR_ L23	The indication from the application that it is ready to enter the L23 state
4	AUX_PM_EN	Auxiliary power PM enable. Setting this bit enables the device to draw auxiliary power independent of the PME AUX power
31:5	RES	Reserved. Must be written with zero. Contains zeros when read.

3.6.4 PCIE Configuration (PCIE_CFG)

Address: 0x180F0010
Access: Read-Only
Reset: See field description

This register is used to denote various function settings of the PCIE device control.

Bit	Bit Name	Description
0	BUS_MASTER_ EN	Bus master enable. This bit denotes the state of the Bus Master Enable bit in the PCI-compatible Command register in the PCIE RC.
1	MEM_SPACE_EN	Memory space enable. This bit denotes the state of the Memory Space Enable bit in the PCI-compatible Command register in the PCIE RC.
4:2	MAX_RDREQ_ SIZE	The maximum read request size. This bit denotes the value of the MAX_READ_REQUEST_SIZE field in the Device Control register in the PCIE RC.
7:5	MAX_PAYLOAD_SIZE	The maximum payload size. This bit denotes the value of the MAX_PAYLOAD_SIZE field in the Device Control register in the PCIE RC.
8	RCB	The read completion boundary (RCB). This bit denotes the value of the RCB bit in the Link Control register in the PCIE RC.
16:9	PBUS_NUM	The configured primary bus number. These bits denote the primary bus number assigned to the device.
21:17	PBUS_DEV_NUM	The configured device number. These bits denotes the device number assigned to the device.
23:22	ATTEN_IND	The attention indicator control. These bits control the system attention indicator (from bits [7:6] of the Slot Control Register in the PCIE RC).
24	PWR_CTRLER_ CTRL	The power controller control. This bit controls the system power controller (from bit [10] of the Slot Control Register in the PCIE RC).
25	EML_CONTROL	The electromechanical interlock control. This bit denotes the state of the Electromechanical Interlock Control bit in the Slot Control Register.
31:26	RES	Reserved. Must be written with zero. Contains zeros when read.

3.6.5 PCIE Receive Completion (PCIE_RX_CNTL)

Address: 0x180F0014
Access: Read-Only
Reset: 0x0

This register is used to denote the field values related to the completion timeout of the PCIE.

Bit	Bit Name	Description
0	CPL_TIMEOUT	The completion timeout. This bit indicates that the completion TLP for a request has not been received within the expected time window.
3:1	TIMEOUT_FN_ NUM	The function number of the timed out completion. This bit is valid when the PCIE core Rx timeout signal is asserted.
6:4	TIMEOUT_CPL_ TC	The traffic class of the timed out completion. This bit is valid when the PCIE core Rx timeout signal is asserted.
8:7	TIMEOUT_CPL _ATTR	The attributes field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted.
20:9	TIMEOUT_CPL_ LEN	The length field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted.
28:21	TIMEOUT_CPL_ TAG	The tag field of the timed out completion. This bit is only valid when the PCIE core Rx timeout signal is asserted
31:29	RES	Reserved. Must be written with zero. Contains zeros when read.

3.6.6 PCIE Reset (PCIE_RESET)

Address: 0x180F0018
Access: Read/Write
Reset: See field description

This register is used to set the bits for the PCIE reset.

Bit	Bit Name	Reset	Description	
0	LINK_UP	0x0	Indicates if the PHY link is up or down	
			0	Link is down
			1	Link is up
1	LINK_REQ_ RESET	0x0	The reset request due to a Link down status. A high-to-low transition indicates that the RC Core is requesting external logic to reset the RC Core because the PHY link is down.	
2	EP_RESET_L	0x1	The reset bit for indicating an endpoint reset through the PCIE PHY	
31:3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	

3.6.7 PCIE Debug Register (PCIE_DEBUG)

Address: 0x180F001C
Access: See field description
Reset: See field description

This register is used to configure the debug parameters of the PCIE.

Bit	Bit Name	Type	Reset	Description
0	RDLH_LINK_UP	RO	0x0	The Data Link Layer up/down indicator. This bit indicates that the flow control has been initialized and the Data Link Layer is ready to transmit and receive packets
				0 Link is down
				1 Link is up
3:1	PM_CURNT_ STATE	RO	0x0	Current power state
8:4	XMLH_LTSSM_ STATE	RO	0x0	Current LTSSM state
11:9	PM_DSTATE	RO	0x0	Current power management D-state of the function.
12	PM_PME_EN	RO	0x0	Power Management Event Enable. The PME enable bit in the PMCSR.
13	PM_STATUS	RO	0x0	The Power Management status. The PME Status bit in the PMCSR.
14	BYTESWAP	RW	0x1	AHB slave byte swap configuration. AHB is Big Endian, PCIE core is Little Endian. If the endpoint is Little Endian, this bit must be set.
15	RES	RO	0x1	Reserved. Always equal to 0x1.
16	PCIE_PHY_ READY	RO	0x0	The ready signal of the PCIE PHY
31:17	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.6.8 PCIE PHY Serial Interface Read/Write Data (PCIE_PHY_RW_DATA)

Address: 0x180F0024
Access: Read/Write
Reset: See field description

This register is used to move IP data.

Bit	Bit Name	Description
31:0	PHY_DATA	Data returned by the PHY or data to be shifted into the PHY. A write to this register would trigger the data written into this register to be shifted into the serial shift register of the PHY, and simultaneously this register is updated with the data shifted out of the PHY.

3.6.9 PCIE PHY Serial Interface Trigger Read or Load

Address: 0x180F0028
Access: Read/Write
Reset: 0x0

This register is used to set the bits for the PCIE PHY Serial Interface Trigger.

Bit	Bit Name	Description
0	PARALLEL_ LOAD	Setting this bit triggers a parallel load into the PCIE PHY. This bit will be cleared when the operation is complete
30:1	RES	Reserved. Must be written with zero. Contains zeros when read.
31	OP_DONE	This bit indicates that the previous operation has been completed. The read/ write/load will be cleared if bit [0] is set.

3.6.10 PCIE PHY Configuration Data (PCIE_PHY_CFG_DATA)

Address: 0x180F002C
Access: Read/Write
Reset: See field description

This register holds the PCIE PHY configuration data.

Bit	Bit Name	Type	Reset	Description
31:0	PHY_CFG_DATA	RW	0x5	The PCIE PHY configuration data

3.6.11 PCIE MAC_PHY Interface Signals (PCIE_MAC_PHY)

Address: 0x180F0030
Access: Read-Only
Reset: See field description

This register is used to denote the interface signals for the MAC-PHY interface.

Bit	Bit Name	Description	
15:0	TXDATA	The parallel data for transmission. Bits [7:0] correspond to the first symbol of Lane 0. Bits [15:8] correspond to the second symbol of Lane 0. (16-bit PHY interface)	
17:16	TXDATAK	The control indicator for the transmit data	
18	TXDETRX_ LOOPBACK	The combined loopback and transmit detection control	
19	TXELECIDLE	The electrical idle transmit. This bit forces the transmit output to Electrical Idle for each Lane on which is it asserted.	
20	TXCOMPLIANCE	The transmit compliance pattern. This bit sets the running disparity to negative. This is used when the transmitting compliance is patterned.	
21	RXPOLARITY	Inverted polarity on receive. This bit directs the PHY to perform a polarity inversion on the received data on the specified Lanes.	
23:22	PWRDOWN	The power control. Power control bits to the PHY. The MAC_PHY_POWERDOWN is a 2-bit signal that is shared by all Lanes.	
		00	P0 (L0: normal)
		01	P0s (L0s: Low recovery time, power saving)
		10	P1 (L1: longer recovery time, additional power saving)
		11	P2 (L2: lowest power state)
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.	

3.6.12 PCIE PHY-MAC Interface Signals

Address: 0x180F0034
Access: Read-Only
Reset: 0x0

This register is used to denote the interface signals for the PHY-MAC interface.

Bit	Bit Name	Description	
15:0	RXDATA	The parallel receive data. Bits [7:0] correspond to the first symbol of Lane 0. Bits [15:8] correspond to the second symbol of Lane 0. (16-bit PHY interface)	
17:16	RXDATAK	The control indicator for the receive data.	
18	RXELECIDLE	Electrical Idle Receive. This bit indicates the receiver detection of an electrical idle for each lane	
21:19	RXSTATUS	The receive status and error codes for each lane	
		000	Received data OK
		001	1 SKP added
		010	1 SKP removed
		011	Receiver detected
		100	8b/10b decode error
		101	Elastic buffer overflow
		110	Elastic buffer underflow
		111	Receive disparity error
22	PHYSTATUS	The PHY status. This bit communicates completion of the PHY functions including power management transitions and receiver detection	
23	RXVALID	Receive data invalid. Indicates the symbol lock and valid data for each lane.	
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.	

3.6.13 PCIE Sideband Bus 1 (PCIE_SIDEBAND1)

Address: 0x180F0038
Access: Read-Only
Reset: 0x0

This register is used to control additional PHY purposes.

Bit	Bit Name	Description
31:0	CFG_PHY_ CONTROL	The output bus that can be used for additional PHY control purposes. The CFG_PHY_CONTROL bus maps to the PHY Control register.

3.6.14 PCIE Sideband Bus 2 (PCIE_SIDEBAND2)

Address: 0x180F003C
Access: Read-Only
Reset: 0x0

This register is used to read the PHY status from the PCIE-PHY.

Bit	Bit Name	Description
31:0	PHY_CFG_ STATUS	Used to read the PHY status from the PCIE-PHY. The PHY_CFG_STATUS bus maps to the PHY Status register.

3.6.15 PCIE Spare Bits (PCIE_SPARE)

Address: 0x180F0040
Access: Read/Write
Reset: 0x0

This register holds the spare bits for the PCIE.

Bit	Bit Name	Description
31:0	BITS	The spare bits for the PCIE

3.6.16 PCIE MSI Lower Address Register (PCIE_MSI_ADDR)

Address: 0x180F0044
Access: Read/Write
Reset: 0x0

This register holds the lower address for the MSI.

Bit	Bit Name	Description
31:0	LADDR	The lower address register for the MSI

3.6.17 PCIE MSI Data Value (PCIE_MSI_DATA)

Address: 0x180F0048
Access: Read/Write
Reset: 0x0

This register is used to hold the data for the MSI including vector.

Bit	Bit Name	Description
15:0	VALUE	These bits hold the data for the MSI including vector [4:0]. The pattern assigned by the system software.
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.

3.6.18 PCIE Interrupt Status Register (PCIE_INT_STATUS)

Address: 0x180F004C
Access: See field description
Reset: 0x0

This register is used to generate interrupts from PCIE functions or errors.

Bit	Bit Name	Type	Description
0	CORR_ERR	RW	The received correctable error message. One clock cycle pulse that indicates that the RC core received an ERR_COR message.
1	NONFATAL_ERR	RW	The received non-fatal error message. One clock cycle pulse that indicates that the RC core received an ERR_NONFATAL message
2	FATAL_ERR	RW	The received fatal error message. One clock cycle pulse that indicates that the RC core received an ERR_FATAL message
3	GM_COMP_ LOOKUP_ERR	RW	GM response composer TAG lookup error. This is a fatal error condition.
4	RADMX_COMP_ LOOKUP_ERR	RW	The RADMX response composer TAG lookup error. This is a fatal error condition.
5	INTA	RW	The edge-triggered INTA virtual wire used for PCI 3.0 compatible INTx emulation
6	INTB	RW	The edge-triggered INTB virtual wire used for the PCI 3.0 compatible INTx emulation
7	INTC	RW	The edge-triggered INTC virtual wire used for the PCI 3.0 compatible INTx emulation
8	INTD	RW	The edge-triggered INTD virtual wire used for the PCI 3.0 compatible INTx emulation
9	MSI	RW	The interrupt caused by the MSI
10	MSI_ERR	RW	The interrupt generated by an MSI error
11	AER_INT	RW	The AER interrupt
12	AER_MSI_INT	RW	AER MSI interrupt; set if MSI interrupt is enabled and an AER occurs
13	SYS_ERR	RW	A system error. The RC Core asserts CFG_SYS_ERR_RC if any device in the hierarchy reports any of the following errors and the associated enable bit is set in the Root Control register: ERR_COR, ERR_FATAL, ERR_NONFATAL.
14	INTAL	RO	The level triggered assertion and deassertion of INTA virtual wire used for PCI 3.0 compatible INTx
15	INTBL	RO	The level triggered assertion and deassertion of INTB virtual wire used for PCI 3.0 compatible INTx
16	INTCL	RO	The level triggered assertion and deassertion of INTC virtual wire used for PCI 3.0 compatible INTx
17	INTDL	RO	The level triggered assertion and deassertion of INTD virtual wire used for PCI 3.0 compatible INTx
18	CPU_INTA	RO	The status bit to indicate that an INTA assertion has occurred and the client needs to send a deassert interrupt
19	CPU_INTB	RO	The status bit to indicate that an INTB assertion has occurred and the client needs to send a deassert interrupt
20	CPU_INTC	RO	The status bit to indicate that an INTC assertion has occurred and the client needs to send a deassert interrupt
21	CPU_INTD	RO	The status bit to indicate that an INTD assertion has occurred and the client needs to send a deassert interrupt
31:22	RES	RO	Reserved. Must be written with zero. Contains zeros when read.

3.6.19 PCIE Interrupt Mask Register

This register is used to selectively enable or disable propagation of interrupts.

Address: 0x180F0050
Access: See field description
Reset: 0x0

Bit	Bit Name	Type	Description
0	CORR_ERR	RW	The received correctable error message. One clock cycle pulse that indicates that the RC core received an ERR_COR message.
1	NONFATAL_ERR	RW	The received non-fatal error message. One clock cycle pulse that indicates that the RC core received an ERR_NONFATAL message
2	FATAL_ERR	RW	The received fatal error message. One clock cycle pulse that indicates that the RC core received an ERR_FATAL message
3	GM_COMP_ LOOKUP_ERR	RW	GM response composer TAG lookup error. This is a fatal error condition.
4	RADMX_COMP_ LOOKUP_ERR	RW	The RADMX response composer TAG lookup error. This is a fatal error condition.
5	INTA	RW	The edge-triggered INTA virtual wire used for PCI 3.0 compatible INTx emulation
6	INTB	RW	The edge-triggered INTB virtual wire used for the PCI 3.0 compatible INTx emulation
7	INTC	RW	The edge-triggered INTC virtual wire used for the PCI 3.0 compatible INTx emulation
8	INTD	RW	The edge-triggered INTD virtual wire used for the PCI 3.0 compatible INTx emulation
9	MSI	RW	The interrupt caused by the MSI
10	MSI_ERR	RW	The interrupt generated by an MSI error
11	AER_INT	RW	The AER interrupt
12	AER_MSI	RW	AER MSI interrupt
13	SYS_ERR	RW	A system error. The RC Core asserts CFG_SYS_ERR_RC if any device in the hierarchy reports any of the following errors and the associated enable bit is set in the Root Control register: ERR_COR, ERR_FATAL, ERR_NONFATAL.
14	INTAL	RO	The level triggered assertion and deassertion of INTA virtual wire used for PCI 3.0 compatible INTx
15	INTBL	RO	The level triggered assertion and deassertion of INTB virtual wire used for PCI 3.0 compatible INTx
16	INTCL	RO	The level triggered assertion and deassertion of INTC virtual wire used for PCI 3.0 compatible INTx
17	INTDL	RO	The level triggered assertion and deassertion of INTD virtual wire used for PCI 3.0 compatible INTx
31:22	RES	RO	Reserved. Must be written with zero. Contains zeros when read.

3.7 Ethernet Registers

Table 3-8 summarizes the Ethernet registers for the AR7240.

Table 3-8. **Ethernet Registers Summary**

GE0 Address	GE1 Address	Description		Page
0x19000000	0x1A000000	MAC Configuration 1		page 66
0x19000004	0x1A000004	MAC Configuration 2		page 67
0x19000008	0x1A000008	IPG/IFG		page 67
0x1900000C	0x1A00000C	Half-Duplex		page 68
0x19000010	0x1A000010	Maximum Frame Length		page 68
0x19000020	0x1A100020	MII Configuration		page 69
0x19000024	0x1A000024	MII Command		page 70
0x19000028	—	MII Address		page 70
0x1900002C	—	MII Control		page 70
0x19000030	—	MII Status		page 71
0x19000034	—	MII Indicators		page 71
0x19000038	0x1A000038	Interface Control		page 72
0x1900003C	0x1A00003C	Interface Status		page 73
0x19000040	0x1A000040	STA Address 1		page 74
0x19000044	0x1A000044	STA Address 2		page 74
0x19000048	0x1A000048	ETH Configuration 0		page 75
0x1900004C	0x1A00004C	ETH Configuration 1		page 76
0x19000050	0x1A000050	ETH Configuration 2		page 76
0x19000054	0x1A000054	ETH Configuration 3		page 77
0x19000058	0x1A000058	ETH Configuration 4		page 77
0x1900005C	0x1A00005C	ETH Configuration 5		page 78
0x19000060	0x1A000060	ETH_FIFO RAM Access 0		page 79
0x19000064	0x1A000064	ETH_FIFO RAM Access 1		page 79
0x19000068	0x1A000068	ETH_FIFO RAM Access 2		page 80
0x1900006C	0x1A00006C	ETH_FIFO RAM Access 3		page 80
0x19000070	0x1A000070	ETH_FIFO RAM Access 4		page 81
0x19000074	0x1A000074	ETH_FIFO RAM Access 5		page 81
0x19000078	0x1A000078	ETH_FIFO RAM Access 6		page 82
0x1900007C	0x1A00007C	ETH_FIFO RAM Access 7		page 82
0x19000180	0x1A000180	DMATXCNTRL_Q0	DMA Transfer Control for Queue 0	page 83
0x19000184	0x1A000184	DMATXDESCR_Q0	Descriptor Address for Queue 0 Tx	page 83
0x19000188	0x1A000188	DMA Tx Status		page 83
0x1900018C	0x1A00018C	DMARXCTRL	Rx Control	page 84
0x19000190	0x1A000190	DMARXDESCR	Pointer to Rx Descriptor	page 84
0x19000194	0x1A000194	DMARXSTATUS	Rx Status	page 84
0x19000198	0x1A000198	DMAINTRMASK	Interrupt Mask	page 85
0x1900019C	0x1A00019C	Interrupts		page 86
0x190001A4	0x1A0001A4	ETH_TXFIFO_TH	Ethernet Tx FIFO Max and Min Threshold	page 87
0x190001A8	0x1A0001A8	ETH_XFIFO_DEPTH	Current Tx and Rx FIFO Depth	page 87
0x190001AC	0x1A0001AC	ETH_RXFIFO_TH	Ethernet Rx FIFO	page 87
0x190001B0	0x1A0001B0	ETH_RXFSM	Ethernet Rx State	page 87
0x190001B4	0x1A0001B4	ETH_TXFSM	Ethernet Tx State	page 88

Table 3-8. **Ethernet Registers Summary (continued)**

GE0 Address	GE1 Address	Description		Page
0x190001B8	0x1A0001B8	ETH_FREE_TIMER	Ethernet Free Timer	page 88
0x190001C0	0x1A0001C0	DMATXCNTRL_Q1	DMA Transfer Control for Queue 1	page 88
0x190001C4	0x1A0001C4	DMATXDESCR_Q1	Descriptor Address for Queue 1 Tx	page 89
0x190001C8	0x1A0001C8	DMATXCNTRL_Q2	DMA Transfer Control for Queue 2	page 89
0x190001CC	0x1A0001CC	DMATXDESCR_Q2	Descriptor Address for Queue 2 Tx	page 89
0x190001D0	0x1A0001D0	DMATXCNTRL_Q3	DMA Transfer Control for Queue 3	page 90
0x190001D4	0x1A0001D4	DMATXDESCR_Q3	Descriptor Address for Queue 3 Tx	page 90
0x190001D8	0x1A0001D8	DMATXARBCFG	DMA Tx Arbitration Configuration	page 90

Combined Tx/Rx Counters

Table 3-9 summarizes the combined Tx/Rx Ethernet registers for the AR7240.

Table 3-9. **Combined Tx/Rx Registers Summary**

GE0 Address	GE1 Address	Name	Description	Page
0x19000200	0x1A000200	TR64	Tx/Rx 64 Byte Frame Counter	page 90
0x19000204	0x1A000204	TR127	Tx/Rx 65-127 Byte Frame Counter	page 91
0x19000208	0x1A000208	TR255	Tx/Rx 128-255 Byte Frame Counter	page 91
0x1900020C	0x1A00020C	TR511	Tx/Rx 256-511 Byte Frame Counter	page 91
0x19000210	0x1A000210	TR1K	Tx/Rx 512-1023 Byte Frame Counter	page 91
0x19000214	0x1A000214	TRMAX	Tx/Rx 1024-1518 Byte Frame Counter	page 92
0x19000218	0x1A000218	TRMGV	Tx/Rx 1519-1522 Byte VLAN Frame Counter	page 92
0x1900021C	0x1A00021C	RBYT	Receive Byte Counter	page 92
0x19000220	0x1A000220	RPKT	Receive Packet Counter	page 92
0x19000224	0x1A000224	RFCS	Receive FCS Error Counter	page 93
0x19000228	0x1A000228	RMCA	Receive Multicast Packet Counter	page 93
0x1900022C	0x1A00022C	RBCA	Receive Broadcast Packet Counter	page 93
0x19000230	0x1A000230	RXCF	Receive Control Frame Packet Counter	page 93
0x19000234	0x1A000234	RXPF	Receive Pause Frame Packet Counter	page 94
0x19000238	0x1A000238	RXUO	Receive Unknown OPCode Packet Counter	page 94
0x1900023C	0x1A00023C	RALN	Receive Alignment Error Counter	page 94
0x19000240	0x1A000240	RFLR	Receive Frame Length Error Counter	page 94
0x19000244	0x1A000244	RCDE	Receive Code Error Counter	page 95
0x19000248	0x1A000248	RCSE	Receive Carrier Sense Error Counter	page 95
0x1900024C	0x1A00024C	RUND	Receive Undersize Packet Counter	page 95
0x19000250	0x1A000250	ROVR	Receive Oversize Packet Counter	page 95
0x19000254	0x1A000254	RFRG	Receive Fragments Counter	page 96
0x19000258	0x1A000258	RJBR	Receive Jabber Counter	page 96
0x1900025C	0x1A00025C	RDRP	Receive Dropped Packet Counter	page 96

Table 3-9. **Combined Tx/Rx Registers Summary (continued)**

GE0 Address	GE1 Address	Name	Description	Page
0x19000260	0x1A000260	TBYT	Transmit Byte Counter	page 96
0x19000264	0x1A000264	TPKT	Transmit Packet Counter	page 97
0x19000268	0x1A000268	TMCA	Transmit Multicast Packet Counter	page 97
0x1900026C	0x1A00026C	TBCA	Transmit Broadcast Packet Counter	page 97
0x19000270	0x1A000270	TXPF	Transmit Pause Control Frame Counter	page 97
0x19000274	0x1A000274	TDFR	Transmit Deferral Packet Counter	page 98
0x19000278	0x1A000278	TEDF	Transmit Excessive Deferral Packet Counter	page 98
0x1900027C	0x1A00027C	TSCL	Transmit Single Collision Packet Counter	page 98
0x19000280	0x1A000280	TMCL	Transmit Multiple Collision Packet	page 98
0x19000284	0x1A000284	TLCL	Transmit Late Collision Packet Counter	page 99
0x19000288	0x1A000288	TXCL	Transmit Excessive Collision Packet Counter	page 99
0x1900028C	0x1A00028C	TNCL	Transmit Total Collision Counter	page 99
0x19000290	0x1A000290	TPFH	Transmit Pause Frames Honored Counter	page 99
0x19000294	0x1A000294	TDRP	Transmit Drop Frame Counter	page 100
0x19000298	0x1A000298	TJBR	Transmit Jabber Frame Counter	page 100
0x1900029C	0x1A00029C	TFCS	Transmit FCS Error Counter	page 100
0x190002A0	0x1A0002A0	TXCF	Transmit Control Frame Counter	page 100
0x190002A4	0x1A0002A4	TOVR	Transmit Oversize Frame Counter	page 101
0x190002A8	0x1A0002A8	TUND	Transmit Undersize Frame Counter	page 101
0x190002AC	0x1A0002AC	TFRG	Transmit Fragment Counter	page 101
0x190002B0	0x1A0002B0	CAR1	Carry Register 1	page 102
0x190002B4	0x1A0002B4	CAR2	Carry Register 2	page 103
0x190002B8	0x1A0002B8	CAM1	Carry Mask Register 1	page 104
0x190002BC	0x1A0002BC	CAM2	Carry Mask Register 2	page 105

3.7.1 MAC Configuration 1

GE0 Address: 0x19000000
GE1 Address: 0x1A000000
Access: See field description
Reset: See field description

This register is used to set the actions for transmitting and receiving frames.

Bit	Bit Name	Type	Reset	Description
0	TX_ENABLE	RW	0x0	Allows the MAC to transmit frames from the system. Clearing this bit will prevent the transmission of frames.
1	SYNCHRONIZED_TX	RO	0x0	Tx enable synchronized to the Tx stream
2	RX_ENABLE	RW	0x0	Setting this bit will allow the MAC to receive frames from the PHY. Clearing this bit will prevent the reception of frames.
3	SYNCHRONIZED_RX	RO	0x0	Rx enable synchronized to the receive stream
4	TX_FLOW_ CONTROL	RW	0x0	Setting this bit causes the Tx MAC control to send requested flow control frames. Clearing this bit prevents the MAC from sending flow control frames. The default is 0.
5	RX_FLOW _CONTROL	RW	0x0	Setting this bit causes the Rx MAC control to detect and act on pause flow control frames.
7:6	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
8	LOOP_BACK	RW	0x0	Setting this bit causes MAC Rx outputs to loop back to the MAC Rx inputs. Clearing this bit results in normal operation.
15:9	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
16	RESET_TX_ FUNCTION	RW	0x0	Resets the Tx function
17	RESET_RX_ FUNCTION	RW	0x0	Resets the Rx function
18	RESET_TX_MAC_ CONTROL	RW	0x0	Resets the transmit (Tx) MAC control
19	RESET_RX_MAC_ CONTROL	RW	0x0	Resets the receive (Rx) MAC control block
29:20	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
30	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
31	SOFT_RESET	RW	0x1	Setting this bit resets all modules except the host interface. The host interface is reset via HRST.

3.7.2 MAC Configuration 2

GE0 Address: 0x19000004
GE1 Address: 0x1A000004
Access: Read/Write
Reset: See field description

This register is used to set the parameters relating to the MAC, including duplex, CRC, and oversized frames.

Bit	Bit Name	Reset	Description
0	FULL_DUPLEX	0x0	Setting this bit configures the MAC to operate in full-duplex mode. Clearing this bit configures the MAC to operate in half-duplex mode only.
1	CRC_ENABLE	0x0	Set this bit to have the MAC append a CRC to all frames. Clear this bit if frames presented to the MAC have a valid length and contain a valid CRC.
2	PAD/CRC ENABLE	0x0	Set this bit to have the MAC pad all short frames and append a CRC to every frame whether or not padding was required. Clear this bit if frames presented to the MAC have a valid length and contain a CRC.
3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
4	LENGTH_FIELD	0x0	Set this bit to cause the MAC to check the frame's length field to ensure it matches the actual data field length. Clear this bit if no length field checking is desired.
5	HUGE_FRAME	0x0	Set this bit to allow frames longer than the MAXIMUM FRAME LENGTH to be transmitted and received. Clear this bit to have the MAC limit the length of frames at the MAXIMUM FRAME LENGTH value, which is contained in the "Maximum Frame Length" register.
7:6	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
9:8	INTERFACE_ MODE	0x0	Determines the type of interface to which the MAC is connected.

Interface Mode	Bit [9]	Bit [8]
RESERVED	0	0
Nibble Mode (10/100 Mbps MII/RMII/SMII...)	0	1
RESERVED	1	0
RESERVED	1	1

11:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:12	PREAMBLE_ LENGTH	0x7	Determines the length of the preamble field of the packet, in bytes.
31:16	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.7.3 IPG/IFG

GE0 Address: 0x19000008
GE1 Address: 0x1A000008
Access: Read/Write
Reset: See field description

This register is used to configure settings for the inter-packet gap and the inter-frame gap.

Bit	Bit Name	Reset	Description
6:0	BACK-TO-BACK INTER-PACKET_GAP	0x60	This programmable field represents the IPG between back-to-back packets (expressed in bit times). This IPG parameter is used in full-duplex mode when two Tx packets are sent back-to-back. Set this field to the desired number of bits.
7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:8	MINIMUM_IFG_ ENFORCEMENT	0x50	This programmable field represents the minimum IFG size to enforce between frames (expressed in bit times). Frames whose IFG is less than that programmed, are dropped.
22:16	NON BACK-TO-BACK INTER-PACKET GAP 2	0x60	This programmable field represents the non-back-to-back inter-packet gap in bit times
23	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
30:24	NON BACK-TO-BACK INTER-PACKET GAP 1	0x40	This programmable field represents the carrier sense window. If a carrier is detected, the MAC will defer to the carrier. If, however, the carrier becomes active, the MAC will continue timing and transmission, knowingly causing a collision and ensuring fair access to the medium.
31	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.7.4 Half-Duplex

GE0 Address: 0x1900000C
GE1 Address: 0x1A00000C
Access: Read/Write
Reset: See field description

This register is used to configure the settings for half-duplex, including backpressure, excessive defer and collisions.

Bit	Bit Name	Reset	Description
9:0	COLLISION_ WINDOW	0x37	This programmable field represents the slot time or collision window during which collisions might occur in a properly configured network. Since the collision window starts at the beginning of a transmission, the preamble and SFD are included. The reset value (0x37) corresponds to the count of frame bytes at the end of the window. If the value is larger than 0x3F the TPST single will no longer work correctly.
11:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:12	RETRANSMISSION _MAXIMUM	0xF	This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The maximum number of attempts is defined by 802.11 standards as 0xF.
16	EXCESSIVE_ DEFER	0x1	Setting this bit will configure the Tx MAC to allow the transmission of a packet that has been excessively deferred. Clearing this bit will cause the Tx MAC to abort the transmission of a packet that has been excessively deferred.
17	NO_BACKOFF	0x0	Setting this bit will configure the Tx MAC to immediately retransmit following a collision. Clearing this bit will cause the Tx MAC to follow the binary exponential backoff rule.
18	BACKPRESSURE_N O_BACKOFF	0x0	Setting this bit will configure the Tx MAC to immediately retransmit following a collision during backpressure operation. Clearing this bit will cause the Tx MAC to follow the binary exponential backoff rule.
19	ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE	0x0	Setting this bit will configure the Tx MAC to use the setting of bits [23:20] instead of the tenth collision. Clearing this bit will cause the TX MAC to follow the standard binary exponential backoff rule, which specifies that any collision after the tenth uses 210-1 as the maximum backoff time.
23:20	ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION	0xA	Used when bit [19] is set. The value programmed is substituted for the Ethernet standard value of ten.
31:24	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.7.5 Maximum Frame Length

GE0 Address: 0x19000010
GE1 Address: 0x1A000010
Access: Read/Write
Reset: 0x600

This register is used to set the maximum allowable frame length.

Bit	Bit Name	Description
15:0	MAX_FRAME _LENGTH	This programmable field sets the maximum frame size in both the Tx and Rx directions
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.6 MII Configuration

GE0 Address: 0x19000020
GE1 Address: 0x1A000020
Access: Read/Write
Reset: 0x0

This register is used to set the MII management parameters.

Bit	Bit Name	Description				
3:0	MGMT_CLOCK_ SELECT	This field determines the clock frequency of the management clock (MDC).				
		Management Clock Select	**3**	**2**	**1**	**0**
		Source clock divided by 2	0	0	0	0
		Source clock divided by 2	0	0	0	1
		Source clock divided by 4	0	0	1	0
		Source clock divided by 6	0	0	1	1
		Source clock divided by 8	0	1	0	0
		Source clock divided by 12	0	1	0	1
		Source clock divided by 18	0	1	1	0
		Source clock divided by 26	0	1	1	1
		Source clock divided by 32	1	0	0	0
		Source clock divided by 40	1	0	0	1
		Source clock divided by 48	1	0	1	0
		Source clock divided by 56	1	0	1	1
		Source clock divided by 62	1	1	0	0
		Source clock divided by 70	1	1	0	1
		Source clock divided by 78	1	1	1	0
		Source clock divided by 96	1	1	1	1
4	PREAMBLE_ SUPRESSION	Setting this bit causes MII Management to suppress preamble generation and reduce the management cycle from 64 clocks to 32 clocks. Clearing this bit causes MII Management to perform Management read/write cycles with the 64 clocks of preamble.				
5	SCAN_AUTO_ INCREMENT	Setting this bit causes MII Management to continually read from a set of contiguous PHYs. The starting address of the PHY is specified by the PHY address field recorded in the MII Address register. The next PHY to be read will be PHY address + 1. The last PHY to be queried in this read sequence will be the one residing at address 0x31, after which the read sequence will return to the PHY specified by the PHY address field.				
30:6	RES	Reserved. Must be written with zero. Contains zeros when read.				
31	RESET_MII_ MGMT	Setting this bit resets the MII Management. Clearing this bit allows MII Management to perform management read/write cycles as requested by the Host interface.				

3.7.7 MII Command

GE0 Address: 0x19000024
GE1 Address: 0x1A000024
Access: Read/Write
Reset: 0x0

This register is used to cause MII management to perform read cycles.

Bit	Bit Name	Description
0	READ_CYCLE	Causes MII management to perform a single read cycle.
1	SCAN_CYCLE	Causes MII management to perform read cycles continuously (e.g. to monitor link fail).
31:2	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.8 MII Address

GE0 Address: 0x19000028
Access: Read/Write
Reset: 0x0

All switch registers are accessed via the MII address and MII control registers of GE0 only. GE1 MII address and control registers are not used. The details of the Ethernet Switch that are accessible through the MAC 0 MII address.

Bit	Bit Name	Description
4:0	REGISTER ADDRESS	Represents the five-bit register address field used in management cycles. Up to 32 registers can be accessed.
7:5	RES	Reserved. Must be written with zero. Contains zeros when read.
12:8	PHY_ADDRESS	Represents the five-bit PHY address field used in management cycles. Up to 31 PHYs can be addressed (0 is reserved).
31:13	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.9 MII Control

GE0 Address: 0x1900002C
Access: Write-Only
Reset: 0x0

All switch registers are accessed via the MII Address and MII Control registers.

This register is used to perform write cycles using the information in the MII Address register.

Bit	Bit Name	Description
15:0	MII_MGMT_ CONTROL	When written, an MII management write cycle is performed using the 16-bit data and the pre-configured PHY and register addresses from ""MII Address"" (0x0A).
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.10 MII Status

GE0 Address: 0x19000030
Access: Read-Only
Reset: 0x0

This register is used to read information following an MII management read cycle.

Bit	Bit Name	Description
15:0	MII_MGMT_ STATUS	Following an MII management read cycle, 16-bit data can be read from this register.
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.11 MII Indicators

GE0 Address: 0x19000034
Access: Read-Only
Reset: 0x0

This register is used indicate various functions of the MII management are currently being performed.

Bit	Bit Name	Description
0	BUSY	When a 1 is returned, this bit indicates that the MII management block is currently performing an MII management read or write cycle
1	SCANNING	When a 1 is returned, this bit indicates that a scan operation (continuous MII management read cycles) is in progress
2	NOT_VALID	When a 1 is returned, this bit indicates that the MII management read cycle has not yet completed and that the read data is not yet valid
31:3	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.12 Interface Control

MAC 0 Address: 0x19000038
MAC 1 Address: 0x1A000038
Access: Read/Write
Reset: 0x0

This register is used to configure and set the interface modules.

Bit	Bit Name	Description	
0	ENABLE_ JABBER_ PROTECTION	This bit enables the Jabber Protection logic within the PE10T in ENDEC mode. Jabber is the condition where a transmitter is on for longer than 50 ms preventing other stations from transmitting. Affects PE10T module only.	
6:1	RES	Reserved. Must be written with zero. Contains zeros when read.	
7	RESET GPSI	This bit resets the PE10T module which converts MII nibble streams to the serial bit stream of ENDEC PHYs. Affects PE10T module only.	
8	DISABLE_LINK_ FAIL	Affects PE100X module only.	
		0	Normal Operation
		1	Disables the 330-ms link fail timer, allowing shorter simulations. Removes the 330-ms link-up time before stream reception is allowed.
9	NO_CIPHER	Affects PE100X module only.	
		0	Normal ciphering occurs
		1	The raw transmit 5B symbols are transmitting without ciphering
10	FORCE_QUIET	Affects PE100X module only.	
		0	Normal operation
		1	Tx data is quiet, allowing the contents of the cipher to be output
14:11	RES	Reserved. Must be written with zero. Contains zeros when read.	
15	RESET_PE100X	This bit resets the PE100X module, which contains the 4B/5B symbol encipher/ decipher code.	
16	SPEED	This bit configures the reduced MII module with the current operating speed.	
		0	Selects 10 Mbps mode
		1	Selects 100 Mbps mode
22:17	RES	Reserved. Must be written with zero. Contains zeros when read.	
23	RESET_PERMII	Setting this bit resets the PERMII module. Clearing this bit allows for normal operation.	
24	PHY_MODE	Setting this bit configures the serial MII module to be in PHY Mode. Link characteristics are taken directly from the RX segments supplied by the PHY.	
25	LHDMODE	Setting this bit configures the A-RGMII module to expect 10 or 100 Mbps half-duplex MII at the GMII interface and will enable the use of CRS and COL signals. This bit should not be asserted unless this mode is being used.	
26	GHDMODE	Setting this bit configures the A-RGMII to expect half-duplex at the GMII interface. It also enables the use of CRS and COL signals.	
27	TBIMODE	Setting this bit configures the A-RGMII module to expect TBI signals at the GMII interface. This bit should not be asserted unless this mode is being used.	
30:28	RES	Reserved. Must be written with zero. Contains zeros when read.	
31	RESET_ INTERFACE_ MODULE	Setting this bit resets the interface module. Clearing this bit allows for normal operation. This bit can be used in place of bits [23], [15] and [7] when any interface module is connected.	

3.7.13 Interface Status

GE0 Address: 0x1900003C
GE1 Address: 0x1A00003C
Access: Read-Only
Reset: 0x0

Identifies the interface statuses. The range of bits that are active are dependant upon the optional interfaces connected at the time.

Bit	Bit Name	Description	
0	JABBER	0	Has not detected a Jabber condition. Latches high.
		1	Has detected a Jabber condition
1	SQE_ERROR	0	Has not detected an SQE error. Latches high.
		1	Has detected an SQE error.
2	CARRIER_LOSS	Carrier status. This bit latches high.	
		0	No carrier loss detection
		1	Loss of carrier detection
3	LINK_FAIL	Used to read the PHY link fail register. For asynchronous host accesses, this bit must be read at least once every scan read cycle of the PHY.	
		0	The MII management module has read the PHY link fail register to be 0
		1	The MII management module has read the PHY link fail register to be 1
4	SPEED	Used to identify the current running speed of the serial MII PHY	
		0	10 Mbps
		1	100 Mbps
5	FULL_DUPLEX	Used to identify the current duplex of the serial MII PHY	
		0	Half-duplex
		1	Full-duplex
6	LINK_OK	Used to identify the validity of a serial MII PHY link	
		0	No valid link detected
		1	Valid link detected
7	JABBER	Used to identify a jabber condition as detected by the serial MII PHY	
		0	No jabber condition detected
		1	Jabber condition detected
8	CLASH	Used to identify the serial MII module mode	
		0	In PHY mode or in a properly configured MAC to MAC mode
		1	MAC to MAC mode with the partner in 10 Mbps and/or half-duplex mode indicative of a configuration error
9	EXCESS_DEFER	This bit sets when the MAC excessively defers a transmission. It clears when read. This bit latches high.	
31:10	RES	Reserved. Must be written with zero. Contains zeros when read.	

3.7.14 STA Address 1

GE0 Address: 0x19000040
GE1 Address: 0x1A000040
Access: Read/Write
Reset: 0x0

This register holds the first four octets of the station address.

Bit	Bit Name	Description
7:0	STATION_ ADDRESS_4	This field holds the fourth octet of the station address
15:8	STATION_ ADDRESS_3	This field holds the third octet of the station address
23:16	STATION_ ADDRESS_2	This field holds the second octet of the station address
31:24	STATION_ ADDRESS_1	This field holds the first octet of the station address

3.7.15 STA Address 2

GE0 Address: 0x19000044
GE1 Address: 0x1A000044
Access: Read/Write
Reset: 0x0

This register holds the last two octets of the station address.

Bit	Bit Name	Description
15:0	RES	Reserved
23:16	STATION_ ADDRESS_6	This field holds the sixth octet of the station address
31:24	STATION_ ADDRESS_5	This field holds the fifth octet of the station address

3.7.16 ETH_FIFO RAM Configuration 0

GE0 Address: 0x19000048
GE1 Address: 0x1A000048
Access: See field description
Reset: 0x0

This register is used to assert and negate functions concerning the ETH module.

Bit	Bit Name	Access	Description	
0	HSTRSTWT	RW	When asserted, this bit places the eth_wtm module in reset	
1	HSTRSTSR	RW	When asserted, this bit places the eth_sys module in reset	
2	HSTRSTFR	RW	When asserted, this bit places the eth_fab module in reset	
3	HSTRSTST	RW	When asserted, this bit places the eth_sys module in reset	
4	HSTRSTFT	RW	When asserted, this bit places the eth_fab module in reset	
7:5	RES	RW	Reserved. Must be written with zero. Contains zeros when read.	
8	WTMENREQ	RW	Asserted	Requests enabling of the eth_wtm module
			Negated	Requests disabling of the eth_wtm module
9	SRFENREQ	RW	Asserted	Requests enabling of the eth_sys module
			Negated	Requests disabling of the eth_sys module
10	FRFENREQ	RW	Asserted	Requests enabling of the eth_fab module
			Negated	Requests disabling of the eth_fab module
11	STFENREQ	RW	Asserted	Requests enabling of the eth_sys module
			Negated	Requests disabling of the eth_sys module
12	FTFENREQ	RW	Asserted	Requests enabling of the eth_fab module
			Negated	Requests disabling of the eth_fab module
15:13	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
16	WTMENRPLY	RO	Asserted	The eth_wtm module is enabled
			Negated	The eth_wtm module is disabled
17	SRFENRPLY	RO	Asserted	The eth_sys module is enabled
			Negated	The eth_sys module is disabled
18	FRFENRPLY	RO	Asserted	The eth_fab module is enabled
			Negated	The eth_fab module is disabled
19	STFENRPLY	RO	Asserted	The eth_sys module is enabled
			Negated	The eth_sys module is disabled
20	FTFENRPLY	RO	Asserted	The eth_fab module is enabled
			Negated	The eth_fab module is disabled
31:21	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	

3.7.17 ETH Configuration 1

GE0 Address: 0x1900004C
GE1 Address: 0x1A00004C
Access: Read/Write
Reset: See field description

This register is used to configure the ETH storage area.

Bit	Bit Name	Reset	Description
15:0	CFGXOFFRTX	0xFFFF	This hexadecimal value represents the number of pause quanta (64-bit times) after an XOFF pause frame has been acknowledged until the ETH reasserts TCRQ if the ETH receive storage level has remained higher than the low watermark.
27:16	CFGFRTH [11:0]	0xFFFF	This hex value represents the minimum number of 4-byte locations to store simultaneously in the receive RAM, relative to the beginning of the frame being input, before FRRDY may be asserted. Note that FRRDY will be latent a certain amount of time due to fabric transmit clock to system transmit clock time domain crossing, and conditional on FRACPT assertion. When set to the maximum value, FRRD may be asserted only after the completion of the input frame. The value of this register must be greater than 18D when HSTDRPLT64 is asserted.
31:28	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.7.18 ETH Configuration 2

MAC 0 Address: 0x19000050
MAC 1 Address: 0x1A000050
Access: Read/Write
Reset: See field description

This register is used to number the minimum amount of 8-byte words in the Rx RAM before pause frames are transmitted.

Bit	Bit Name	Reset	Description
12:0	CFGLWM [12:0]	0x555	This hex value represents the minimum number of 8-byte words to store simultaneously in the Rx RAM before TCRQ and PSVAL facilitate an XON pause control frame in response to a previously transmitted XOFF pause control frame.
15:13	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
28:16	CFGHWM [12:0]	0xAAA	This hex value represents the maximum number of 8-byte words to store simultaneously in the Rx RAM before TCRQ and PSVAL facilitates an XOFF pause control frame.
31:29	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.7.19 ETH Configuration 3

GE0 Address: 0x19000054
GE1 Address: 0x1A000054
Access: Read/Write
Reset: See field description

This register is used denote the minimum number of 4-byte locations to simultaneously store in the Tx RAM before assertion.

Bit	Bit Name	Type	Reset	Description
11:0	CFGFTTTH [11:0]	RW	0xFFF	This hex value represents the minimum number of 4-byte locations to store simultaneously in the Tx RAM, relative to the beginning of the frame being input, before TPSF is asserted. Note that TPSF is latent for a certain amount of time due to fabric Tx clock system Tx clock time domain crossing. When set to the maximum value, TPSF asserts only after the completion of the input frame.
15:12	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
27:16	CFGHWMFT [11:0]	RW	0x555	This hex value represents the maximum number of 4-byte locations to store simultaneously in the Tx RAM before FTHWM is asserted. Note that FTHWM has two FTCLK clock periods of latency before assertion or negation, as should be considered when calculating headroom required for maximum size packets.
31:28	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.7.20 ETH Configuration 4

GE0 Address: 0x19000058
GE1 Address: 0x1A000058
Access: Read/Write
Reset: 0x0

This register is used to signal drop frame conditions internal to the Ethernet.

Bit	Bit Name	Description
17:0	HSTFLTRFRM	These configurations bits are used to signal drop frame conditions internal to the ETH. The bits correspond to the Rx statistics vector (RSV) on a one-per-one basis. E.g., bit [0] corresponds to RSV [16], and bit [1] corresponds to RSV [17]. When these bits compare and the do not care is not asserted, the frame will be dropped. The setting of these bits, along with their do not care values in the HSTFLTRFRMDC configuration registers, create the filter to assert the SRDRPFRM output of the Rx frame does not pass the acceptable conditions and should be dropped by the system. E.g., if it is desired to drop a frame that contains an FCS Error, bit [4] would be set and all Rx frames with RSV [20] asserted would be dropped.
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.21 ETH Configuration 5

GE0 Address: 0x1900005C
GE1 Address: 0x1A00005C
Access: Read/Write
Reset: See field description

This register is used to assert or negate bits of the ETH component.

Bit	Bit Name	Reset	Description
17:0	HSTFLTRFRMDC [17:0]	0x3FFFF	These configuration bits indicate which RSV are "do not cares" for the ETH frame drop circuitry. The bits correspond to the RSV on a one-per-one basis. For example, bit [0] corresponds to RSV [16], and bit [1] corresponds to RSV [17]. Setting a HSTFLTRFRMDC bit indicates a "do not care" for that RSV bit. Clearing the bit looks for a matching level on the corresponding HSTFLTRFRM bit. If a match is made, the frame is dropped. All bits should be set when CFGFRTH bits are not set.
18	HSTDRPLT64	0x0	Setting this bit will cause the frame to be dropped if an Rx frame is less than 64 bytes in length. This bit should not be asserted if CFGFRTH is less than 0x12.
19	CFGBYTMODE	0x0	This bit should be asserted when data is transferred at the TPD and RPD bus at a rate of one byte per qualified clock. This bit should be negated when data is transferred at the TPD and RPD bus at a rate of one nibble per qualified clock. This bit should therefore be set to 1 for GE0 or set to 0 for GE1.
20	HSTSRFULLCLR	0x0	This bit should be written asserted when it is desired to clear the SRFULL indicator bit. After HSTFULLCLR should then be written unasserted for the indicator to become operational again.
21	SRFULL	0x0	Assertion of this bit indicates that the maximum capacity of the Rx FIFO storage has been met or exceeded. If the CFGFRTH bits are not all set, exceeding the FIFO storage capacity may result in data frame truncation as opposed to full frame deletion.
31:22	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.7.22 ETH_FIFO RAM Access 0

GE0 Address: 0x19000060
GE1 Address: 0x1A000060
Access: See field description
Reset: 0x0

Bit	Bit Name	Type	Description
12:0	HSTTRAMWADX	RW	Host Tx RAM write address. This field has different functionality based on the value of hsttramwadx[12] and whether the ETH_FIFO RAM access register 0 is being written to or read from. When read from, the hsttramwadx[11:0] field contains the actual write pointer value of the eth_fab module. When written to the hsttramwadx register will be loaded. If hsttramwadx[12] is low, hsttramwadx[10:0] will be the transmit RAM address which hsttramwdat is written to. If hsttramwadx[12] is high, hsttramwadx[11:0] contains the pointer value that will be written to the eth_fab module.
15:13	RES	RO	Reserved. Must be written with zero. Contains zeros when read.
23:16	HSTTRAMWDAT [39:32]	RW	The host Tx RAM write data; the upper byte of the Tx FIFO RAM data to write at the address of HSTTRAMWADX [10:0] if HSTTRAMWADX [12] is negated and HSTTRAMWREQ is asserted. This part of the Tx FIFO RAM contains control information for the frame as follows:
			HSTTRAMWDAT [39] — FTCFRM
			HSTTRAMWDAT [38:37] — FTPPPADMODE [1:0]
			HSTTRAMWDAT [36] — FTPPEN
			HSTTRAMWDAT [35] — FTPPGENFCS
			HSTTRAMWDAT [34] — FTEOF
			HSTTRAMWDAT [33:32] — FTDATNVLD [1:0]
29:24	RES	RO	Reserved. Must be written with zero. Contains zeros when read.
30	HSTTRAMWACK	RO	The host Tx RAM write acknowledge. This signifies the acceptance of the HSTTRAMWDAT and HSTTRAMWADX values to the Tx FIFO RAM or ETH_FAB module; will only be asserted or negated following assertion or negation of HSTTRAMWREQ. Writes to this bit have no effect.
31	HSTTRAMWREQ	RW	The host Tx RAM write request. This bit requests the handshake of the HSTTRAMWDAT and HSTTRAMWDAX values to the Tx FIFO RAM. Should only be asserted while HSTTRAMWACK is negated and while the TX data path is disabled from receiving data and is in a steady state. It should only be negated after receiving an asserted HSTTRAMWACK.

3.7.23 ETH_FIFO RAM Access 1

GE0 Address: 0x19000064
GE1 Address: 0x1A000064
Access: Read/Write
Reset: 0x0

This register is used to hold the Tx RAM write data.

Bit	Bit Name	Description
31:0	HSTTRAMWDAT [31:0]	The host Tx RAM write data; the lower 4 bytes of Tx FIFO RAM data to write at the address of HSTTRAMWADX [10:0] if HSTTRAMWADX [12] is negated and HSTTRAMWREQ is asserted.

3.7.24 ETH_FIFO RAM Access 2

GE0 Address: 0x19000068
GE1 Address: 0x1A000068
Access: Read/Write
Reset: 0x0

This register is used to configure actions for the host Tx RAM.

Bit	Bit Name	Description	
12:0	HSTTRAMRADX [12:0]	The host Tx RAM read request. If HSTTRAMRADX [12] is written low, HSTTRAMRADX [10:0] is the Tx FIFO RAM address that HSTTRAMRDAT is read from. If HSTTRAMRADX [12] is written high, HSTTRAMRADX [11:0] contains the pointer value read from the ETH module.	
15:13	RES	Reserved. Must be written with zero. Contains zeros when read.	
23:16	HSTTRAMRDAT [39:32]	The host Tx RAM read data; the upper byte of Tx FIFO RAM data that was read at the address of HSTTRAMWADX [10:0] if HSTTRAMWADX [12] is negated and HSTTRAMWREQ is asserted. This part of the Tx FIFO RAM contains control information for the frame as follows:	
		HSTTRAMRDAT [39]	FTCFRM
		HSTTRAMRDAT [38:37]	FTPPPADMODE [1:0]
		HSTTRAMRDAT [36]	FTPPEN
		HSTTRAMRDAT [35]	FTPPGENFCS
		HSTTRAMRDAT [34]	FTEOF
		HSTTRAMRDAT [33:32]	FTDATNVLD [1:0]
29:24	RES	Reserved. Must be written with zero. Contains zeros when read.	
30	HSTTRAMRACK	The host Tx RAM read acknowledge. Signifies the acceptance of HSTTRAMRADX values to the Tx FIFO RAM and reception of HSTTRAMRDAT from the Tx FIFO RAM location addressed; only asserted or negated following assertion or negation of HSTTRAMRREQ. Writes to this bit have no effect.	
31	HSTTRAMRREQ	The host Tx RAM read request. Requests the handshake of HSTTRAMRADX values to the Tx FIFO RAM and HSTTRAMRDAT from the Tx FIFO RAM. This bit should only be asserted while HSTTRAMRACK is negated and while the Tx data path is disabled from receiving data in a steady state. It should only be negated after receiving an asserted HSTTRAMRACK.	

3.7.25 ETH_FIFO RAM Access 3

GE0 Address: 0x1900006C
GE1 Address: 0x1A00006C
Access: Read-Only
Reset: 0x0

This register is used to hold the host Tx RAM read data.

Bit	Bit Name	Description
31:0	HSTTRAMRDAT [31:0]	The host Tx RAM read data; the lower 4 bytes of Tx FIFO RAM data read at the address of HSTTRAMWADX [10:0] if HSTTRAMWADX [12] is negated and HSTTRAMWREQ is asserted. Writes have no effect on this field.

3.7.26 ETH_FIFO RAM Access 4

GE0 Address: 0x19000070
GE1 Address: 0x1A000070
Access: See field description
Reset: See field description

This register is used to configure the host Rx RAM.

Bit	Bit Name	Type	Reset	Description
13:0	HSTTRAMWADX [13.:0]	RW	0x0	The host Rx RAM write address. This field has different functionality based on the value of HSTRRAMWADX [13] and whether this register is written to or read from. When read from, the HSTRRAMWADX [12] field contains the actual write pointer value of the ETH_SYS module. when written to, the HSTTRAMWADX register will be loaded. If HSTRRAMWADX [13] is low, HSTRRAMWADX [11:0] will be the Rx FIFO RAM address that HSTRRAMWDAT is written to. If HSTRRAMWADX is high, HSTRRAMWADX [12:0] contains the pointer value written to the ETH_SYS.
15:13	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
23:16	HSTTRAMWDAT [39:32]	RW	0x0	The host Rx RAM write data; the upper byte of the receive FIFO RAM data to write at the address of HSTRRAMWADX [11:0] if HSTTRAMWADX [13] is negated and HSTRRAMWREQ is asserted. This part of the Rx FIFO RAM contains control information for the frame as follows.
				HSTTRAMWDAT [39:35] — Unused
				HSTTRAMWDAT [34] — RPEF
				HSTRRAMWDAT [33:32] — SRDATNVLD [1:0]
29:24	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
30	HSTTRAMWACK	RO	0x0	Host Rx RAM write acknowledge. Signifies the acceptance of HSTRRAMWDAT and HSTRRAMWADX values to the Rx FIFO RAM or AMCXRFIF_SYS module. Only asserted or negated following assertion or negation of HSTTTAMWREQ. Writes to this bit have no effect.
31	HSTTRAMWREQ	RW	0x0	The host Rx RAM write request. This bit requests the handshake of HSTRRAMWDAT and HSTRRAMWDAX values to the Rx FIFO RAM. This bit should only be asserted while HSTTRAMWACK is negated and while the Rx data path is disabled from receiving data and is in a steady state. It should only be negated after receiving an asserted HSTRRAMWACK.

3.7.27 ETH_FIFO RAM Access 5

GE0 Address: 0x19000074
GE1 Address: 0x1A000074
Access: Read/Write
Reset: 0x0

This register is used to hold the Rx RAM write data.

Bit	Bit Name	Description
31:0	HSTTRAMWDAT [31:0]	The host Rx RAM write data; the lower 4 bytes of Rx FIFO RAM data to write at the address of HSTRRAMWADX [11:0] if HSTRRAMWADX [13] is negated and HSTRRAMWREQ is asserted.

3.7.28 ETH_FIFO RAM Access 6

GE0 Address: 0x19000078
GE1 Address: 0x1A000078
Access: See field description
Reset: 0x0

This register is used to configure settings for the host Rx RAM read address.

Bit	Bit Name	Access	Description
13:0	HSTRRAMRADX [12:0]	RW	The host Rx RAM read address. If HSTRRAMRADX [13] is written low, HSTRRAMRADX [11:0] is the Rx FIFO RAM address that HSTRRAMDAT is read from. If HSTRRAMRADX [13] is written high, HSTRRAMRADX [12:0] contains the pointer value read from AMCXRFIF_FAB module.
15:14	RES	RO	Reserved. Must be written with zero. Contains zeros when read.
23:16	HSTRRAMRDAT [39:32]	RO	The host Rx RAM read data; the upper byte of Rx FIFO RAM data that was read at the address of HSTRRAMWADX [10:0]TRRAMWADX [13] is negated and HSTRRAMWREQ is asserted. This part of the Rx FIFO RAM contains control information for the frame as follows:
			HSTRRAMWDAT [39:35] — Unused
			HSTRRAMWDAT [34] — RPEF
			HSTRRAMWDAT [33:32] — STDATNVLD [1:0]
29:24	RES	RO	Reserved. Must be written with zero. Contains zeros when read.
30	HSTRRAMRACK	RO	The host Rx RAM read acknowledge. This bit signifies the acceptance of HSTRRAMRADX values to the Rx FIFO RAM and reception of HSTRRAMRDAT from the Rx FIFO RAM location addressed. Only asserted or negated following assertion or negation of HSTRRAMRREQ. Writes to this bit have no effect.
31	HSTRRANRREQ	RW	The host Rx RAM read request. This bit requests the handshake of HSTRRAMRADX values to the RX FIFO RAM and HSTRRAMRDAT from the Rx FIFO RAM. This bit should only be asserted while HSTRRAMRACK is negated and while the Rx data path is disabled from receiving data and is in a steady state. It should only be negated after receiving an asserted HSTRRAMRACK.

3.7.29 ETH_FIFO RAM Access 7

GE0 Address: 0x1900007C
GE1 Address: 0x1A00007C
Access: Read-Only
Reset: 0x0

This register is used to hold the host Rx RAm data for eventual reading.

Bit	Bit Name	Description
31:0	HSTRRAMRDAT [31:0]	The host Rx RAM read data; the lower four bytes of Rx FIFO RAM data read at the address of HSTRRAMRADX [11:0] if HSTRRAMRADX [13] is negated and HSTRRAMWREQ is asserted. Writes to this field have no effect.

3.7.30 DMA Transfer Control for Queue 0 (DMATXCNTRL_Q0)

GE0 Address: 0x19000080
GE1 Address: 0x1A000080
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
0	TX_ENABLE	Enables queue 0
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.31 Descriptor Address for Queue 0 Tx (DMATXDESCR_Q0)

GE0 Address: 0x19000184
GE1 Address: 0x1A000184
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 0

3.7.32 Transmit Status (DMATXSTATUS)

GE0 Address: 0x19000188
GE1 Address: 0x1A000188
Access: Read/Write
Reset: 0x0

This register is used to set the bits and flags regarding the DMA controller and its transferring status.

Bit	Bit Name	Description
0	TXPKTSENT	Indicates that one or more packets transferred successfully. This bit is cleared when TXPKTCOUNT (bits [23:16]) is zero. Writing a 1 to this bit reduces TXPKTCOUNT by one.
1	TXUNDERRUN_Q0	This bit is set when the DMA controller reads a set (”1”) Empty Flag in the descriptor it is processing
2	RES	Reserved. Must be written with zero. Contains zeros when read.
3	BUS_ERROR	Indicates that the DMA controller received a host/slave split, error, or retry response
8:4	RES	Reserved. Must be written with zero. Contains zeros when read.
9	TX_UNDERRUN_Q1	Indicates TXUNDERRUN_Q1 as an interrupt source
10	TX_UNDERRUN_Q2	Indicates TXUNDERRUN_Q2 as an interrupt source
11	TX_UNDERRUN_Q3	Indicates TXUNDERRUN_Q3 as an interrupt source
15:12	RES	Reserved.
23:16	TXPKTCOUNT	This 8-bit TX packet counter increments when the DMA controller transfers a packet successfully, and decrements when the host writes a 1 to TX_PKT_SENT (bit [0]).
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.33 Receive Control (DMARXCTRL)

GE0 Address: 0x1900018C
GE1 Address: 0x1A00018C
Access: Read/Write
Reset: 0x0

This register is used to enable the DMA to receive packets.

Bit	Bit Name	Description
0	RXENABLE	Allows the DMA to receive packet transfers. When set, the built-in DMA controller begins receiving packets as the FIFO indicates they are available (FRSOF asserted). The DMA controller clears this bit when it encounters an RX overflow or bus error state.
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.34 Pointer to Receive Descriptor (DMARXDESCR)

GE0 Address: 0x19000190
GE1 Address: 0x1A000190
Access: Read/Write
Reset: 0x0

This register is used to find the location of the first TX packet descriptor in the memory.

Bit	Bit Name	Description
1:0	RES	Ignored by the DMA controller, because it is a requirement of the system that all descriptors are 32-bit aligned in the host memory.
31:2	DESCRIPTOR_ ADDRESS	The descriptor address. When the RXENABLE (bit [0] of the "Receive Control (DMARXCTRL)" register) is set by the host, the DMA controller reads this register to find the host memory location of the first receive packet descriptor.

3.7.35 Receive Status (DMARXSTATUS)

GE0 Address: 0x19000194
GE1 Address: 0x1A000194
Access: Read/Write
Reset: 0x0

This register is used to set the bits and flags regarding the DMA controller and its receiving status.

Bit	Bit Name	Description
0	RXPKT RECEIVED	Indicates that one or more packets were received successfully. This bit is cleared when the RXPKTCOUNT (bits [23:16]) is zero. Writing a 1 to this bit reduces RXPKTCOUNT by one.
1	RXOVERFLOW	This bit is set when the DMA controller reads a set empty flag in the descriptor it is processing
2	RES	Reserved. Must be written with zero. Contains zeros when read.
3	BUSERROR	Indicates that the DMA controller received a host/slave split, error, or retry response
15:4	RES	Reserved. Must be written with zero. Contains zeros when read.
23:16	RXPKTCOUNT	This 8-bit receive packet counter increments when the DMA controller transfers a packet successfully, and decrements when the host writes a 1 to RXPKTRECEIVED (bit [0]).
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.36 Interrupt Mask (DMAINTRMASK)

GE0 Address: 0x19000198
GE1 Address: 0x1A000198
Access: Read/Write
Reset: 0x0

This register is used to configure interrupt masks for the DMA. Setting a bit to 1 enables the corresponding status signal as an interrupt source. The register "DMA Interrupts" is the AND of DMA status bits with this register.

Bit	Bit Name	Description
0	TXPKTSENT_MASK	Setting this bit to 1 enables TXPKTSENT (bit [0] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
1	TX_UNDERRUN_Q0_MASK	Setting this bit 1 enables TXUNDERRUN_Q0 (bit [1] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
2	RES	Reserved. Must be written with zero. Contains zeros when read.
3	BUSERROR_MASK	Setting this bit to 1 enables BUSERROR (bit [3] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
4	RXPKTRECEIVED_MASK	Enables RXPKTRECEIVED (bit [0] in the "Receive Status (DMARXSTATUS)" register) as an interrupt source
5	RES	Reserved. Must be written with zero. Contains zeros when read.
6	RX_OVERFLOW_MASK	Setting this bit to 1 enables RXOVERFLOW (bit [1] in the "Receive Status (DMARXSTATUS)" register) as in interrupt source
7	BUS_ERROR_MASK	Setting this bit to 1 enables BUSERROR (bit [3] in the "Receive Status (DMARXSTATUS)" register) as an interrupt source
8	RES	Reserved. Must be written with zero. Contains zeros when read.
9	TX_UNDERRUN_Q1_MASK	Setting this bit 1 enables TXUNDERRUN_Q1 (bit [9] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
10	TX_UNDERRUN_Q2_MASK	Setting this bit 1 enables TXUNDERRUN_Q2 (bit [10] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
11	TX_UNDERRUN_Q3_MASK	Setting this bit 1 enables TXUNDERRUN_Q3(bit [11] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.37 Interrupts (DMAINTERRUPT)

GE0 Address: 0x1900019C
GE1 Address: 0x1A00019C
Access: Read/Write
Reset: 0x0

This register is used to configure interrupts for the DMA. Flags in this register clear when their corresponding Status bit is cleared.

Bit	Bit Name	Description
0	TXPKTSENT	Set this bit to 1 enables TXPKTSENT (bit [0] in the "Transmit Status (DMATXSTATUS)" register) and TXPKTSENT_MASK (bit [0] of the "Interrupt Mask (DMAINTRMASK)" register) are both set
1	TX_UNDERRUN_Q0	Setting this bit to 1 enables TX_UNDERRUN (bit [1] in the "Transmit Status (DMATXSTATUS)" register) and TX_UNDERRUN_MASK (bit [1] of the "Interrupt Mask (DMAINTRMASK)" register) are both set
2	RES	Reserved. Must be written with zero. Contains zeros when read.
3	BUS_ERROR	Setting this bit to 1 enables BUSERROR (bit [3] in the "Transmit Status (DMATXSTATUS)" register) and BUSERROR_MASK (bit [3] of the "Interrupt Mask (DMAINTRMASK)" register) are both set
4	RXPKT_RECEIVED_MASK	Records a RX_PKT_RECEIVED error interrupt when RX_PKT_RECEIVED (bit [0] in the "Receive Status (DMARXSTATUS)" register) and RXPKT_RECEIVED_MASK (bit [4] of the "Interrupt Mask (DMAINTRMASK)" register) are both set
5	RES	Reserved. Must be written with zero. Contains zeros when read.
6	RX_OVERFLOW_MASK	Setting this bit to 1 records an Rx overflow error interrupt when RX_OVERFLOW (bit [1] in the "Receive Status (DMARXSTATUS)" register) and RX_OVERFLOW_MASK (bit [6] of the "Interrupt Mask (DMAINTRMASK)" register) are both set
7	BUS_ERROR_MASK	Setting this bit to 1 records an Rx bus error interrupt when BUS_ERROR (bit [3] in the "Receive Status (DMARXSTATUS)" register) and BUS_ERROR_MASK (bit [7] of the "Interrupt Mask (DMAINTRMASK)" register) are both set
8	RES	Reserved. Must be written with zero. Contains zeros when read.
9	TX_UNDERRUN_Q1	Setting this bit 1 enables TXUNDERRUN_Q1 (bit [9] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
10	TX_UNDERRUN_Q2	Setting this bit 1 enables TXUNDERRUN_Q2 (bit [10] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
11	TX_UNDERRUN_Q3	Setting this bit 1 enables TXUNDERRUN_Q3(bit [11] in the "Transmit Status (DMATXSTATUS)" register) as an interrupt source
31:8	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.38 Current Tx and Rx FIFO Depth (ETH_XFIFO_DEPTH)

GE0 Address: 0x190001A8
GE1Address: 0x1A0001A8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
9:0	CURRENT_TX_FIFO_DEPTH	Current Tx FIFO depth
15:10	RES	Reserved
25:16	CURRENT_RX_FIFO_DEPTH	Current Rx FIFO depth
31:26	RES	Reserved

3.7.39 Ethernet Transmit FIFO Throughput (ETH_TXFIFO_TH)

GE0 Address: 0x190001A4
GE1 Address: 0x1A0001A4
Access: Read/Write
Reset: See field description

This Ethernet register has a 2 KB Tx FIFO. It is use to determine the minimum and maximum levels of the transfer FIFO and correspondingly keep the transmit levels within the range to keep a continuous data transfer flowing.

Bit	Bit Name	Reset	Description
9:0	TXFIFO_MINTH	0x160	This bit specifies the minimum number of double words in the Tx FIFO, and if it is less than this value, this bit needs to be asserted.
15:10	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
25:16	TXFIFO_MAXTH	0x1D8	This bit represents the maximum number of double words in the Tx FIFO, and once this limit is surpassed, this bit should be de-asserted
31:26	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.7.40 Ethernet Receive FIFO Threshold (ETH_RXFIFO_TH)

GE0 Address: 0x190001AC
GE1 Address: 0x1A0001AC
Access: Read/Write
Reset: See field description

This Ethernet register has a 2 KB Rx FIFO. It is used to determine the minimum and maximum levels of the transfer FIFO and correspondingly keep the transmit levels within the range to keep a continuous data transfer flowing.

Bit	Bit Name	Reset	Description
9:0	RCVFIFO_MINTH	0x0	The minimum number of double words in the receive FIFO. Once this number is reached, this bit needs to be asserted.
31:10	SCRATCHREG_0	0x28	This bit is a pure scratch pad register that can be used by the CPU for any general purpose.

3.7.41 Ethernet Receive State (ETH_RXFSM)

GE0 Address: 0x190001B0
GE1 Address: 0x1A0001B0
Access: See field description
Reset: 0x0

This register reflects certain signals of the receive state machine for debugging purposes.

Bit	Bit Name	Type	Description	
1:0	RCVDMASTATE	RO	This bit reflects the DMA State variable	
3:2	RES	RO	Reserved	
5:4	RCVAHBSTATE	RO	This bit reflects the AHB State variable.	
6	RES	RO	Reserved	
7	RFDGT_MINTH	RO	This bit represents the receive FIFO depth greater than the minimum specified.	
8	RES	RO	Reserved	
9	AHB_GRANT_RX	RO	0	Receive requestor does not have the grant
			1	Receive requestor has the grant
19:10	MAX_RCV_FIFO_DEPTH	RO	Maximum depth of the receive FIFO that was hit	
30:20	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
31	CLR_RCV_MAX_FIFODEPTH	WO	Writing to this bit clears the max_rx_fifo_depth variable	

3.7.42 Ethernet Transmit Status (ETH_TXFSM)

GE0 Address: 0x190001B4
GE1 Address: 0x1A0001B4
Access: See field description
Reset: 0x0

This register reflects certain signals of the transmit state machine for debugging purposes.

Bit	Bit Name	Type	Description	
1:0	TXDMASTATE	RO	Reflects the DMA state variable	
3:2	RES	RO	Reserved	
5:4	TXAHBSTATE	RO	Reflects the AHB state variable	
6	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
7	TXFIFO_LT_MINTH	RO	The transmit FIFO depth is less than the minimum threshold specified	
8	TXFIFO_GT_MAXTH	RO	The transmit FIFO depth is less than the maximum threshold specified	
9	AHB_GRANT_TX	RO	0	Transmit requestor does not have the grant
			1	Transmit requestor has the grant
19:10	MAX_TX_FIFO_DEPTH	RO	The maximum depth of the transmit FIFO that was hit	
30:20	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
31	CLR_TX_MAX_FIFODEPTH	WO	Writing to this register with this bit set clears the max_rcv_fifo_depth variable	

3.7.43 Ethernet Free Timer

GE0 Address: 0x190001B8
GE1 Address: 0x1A0001B8
Access: Read/Write
Reset: See field description

This register updates the Ethernet descriptors with time stamps

Bit	Bit Name	Reset	Description	
20:0	FREE_TIMER	0x1FFFFF	Free timer	
30:21	SCRATCHREG_1	0x0	The pure general purpose register for use by the CPU	
31	TIMER_UPDATE	0x1	0	Timer update at the AHB_CLK
			1	Free timer at the AHB_CLK/4

3.7.44 DMA Transfer Control for Queue 1 (DMATXCNTRL_Q1)

GE0 Address: 0x190001C0
GE1 Address: 0x1A0001C0
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
0	TX_ENABLE	Enables queue 1
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.45 Descriptor Address for Queue 1 Tx (DMATXDESCR_Q1)

GE0 Address: 0x190001C4
GE1 Address: 0x1A0001C4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 1

3.7.46 DMA Transfer Control for Queue 2 (DMATXCNTRL_Q2)

GE0 Address: 0x190001C8
GE1 Address: 0x1A0001C8
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
0	TX_ENABLE	Enables queue 2
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.47 Descriptor Address for Queue 2 Tx (DMATXDESCR_Q2)

GE0 Address: 0x190001CC
GE1 Address: 0x1A0001CC
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 2

3.7.48 DMA Transfer Control for Queue 3 (DMATXCNTRL_Q3)

GE0 Address: 0x190001D0
GE1 Address: 0x1A0001D0 Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
0	TX_ENABLE	Enables queue 3
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.49 Descriptor Address for Queue 3 Tx (DMATXDESCR_Q3)

GE0 Address: 0x190001D4
GE1 Address: 0x1A0001D4
Access: Read/Write
Reset: 0x0

Bit	Bit Name	Description
1:0	RES	Reserved. Must be written with zero. Contains zeros when read.
31:2	DESCR_ ADDR	The descriptor address to be fetched for queue 3

3.7.50 DMA Transfer Arbitration Configuration (DMATXARBCFG)

GE0 Address: 0x190001D8
GE1 Address: 0x1A0001D8
Access: Read/Write
Reset: See field description

This register is used to select the type of arbitration used for the QoS feature and the weight to be assigned to a particular queue. Note that a weight of zero is not permitted and causes the hardware to misbehave.

Bit	Bit Name	Reset	Description	
0	RRMODE	0x1	Round robin mode	
			0	Simple priority (Q0 highest priority)
			1	Weighted round robin (WRR)
7:1	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
13:8	WGT0	0x8	The weight for Queue 0, if WRR has been selected	
19:4	WGT1	0x4	The weight for Queue 1, if WRR has been selected	
25:20	WGT2	0x2	The weight for Queue 2, if WRR has been selected	
31:26	WGT3	0x1	The weight for Queue 3, if WRR has been selected	

3.7.51 Tx/Rx 64 Byte Frame Counter (TR64)

GE0 Address: 0x19000200
GE1 Address: 0x1A000200
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were up to 64 bytes in length.

Bit	Bit Name	Description
17:0	TR64	The transmit and receive 64 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which is 64 bytes in length inclusive (excluding framing bits but including FCS bytes).
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.52 Tx/Rx 65-127 Byte Frame Counter (TR127)

GE0 Address: 0x19000204
GE1 Address: 0x1A000204
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 65–127 bytes in length.

Bit	Bit Name	Description
17:0	TR127	The transmit and receive 65–127 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 65-127 bytes in length inclusive (excluding framing bits but including FCS bytes).
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.53 Tx/Rx 128-255 Byte Frame Counter (TR255)

GE0 Address: 0x19000208
GE1 Address: 0x1A000208
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 128–255 bytes in length.

Bit	Bit Name	Description
17:0	TR255	The transmit and receive 128-255 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 128-255 bytes in length inclusive (excluding framing bits but including FCS bytes).
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.54 Tx/Rx 256-511 Byte Frame Counter (TR511)

GE0 Address: 0x1900020C
GE1 Address: 0x1A00020C
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 256–511 bytes in length.

Bit	Bit Name	Description
17:0	TR511	The transmit and receive 256–511 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 256–511 bytes in length inclusive (excluding framing bits but including FCS bytes).
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.55 Tx/Rx 512-1023 Byte Frame Counter (TR1K)

GE0 Address: 0x19000210
GE1 Address: 0x1A000210
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 512–1023 bytes in length.

Bit	Bit Name	Description
17:0	TR1K	The transmit and receive 512–1023 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 512–1023 bytes in length inclusive (excluding framing bits but including FCS bytes).
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.56 Tx/Rx 1024-1518 Byte Frame Counter (TRMAX)

GE0 Address: 0x19000214
GE1 Address: 0x1A000214
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 1024–1518 bytes in length.

Bit	Bit Name	Description
17:0	TRMAX	The transmit and receive 1024-1518 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 1024-1518 bytes in length inclusive (excluding framing bits but including FCS bytes).
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.57 Tx/Rx 1519-1522 Byte VLAN Frame Counter (TRMGV)

GE0 Address: 0x19000218
GE1 Address: 0x1A000218
Access: Read/Write
Reset: 0x0

This register is used to count frames transmitted or received that were between 1519–1522 bytes in length.

Bit	Bit Name	Description
17:0	TRMGV	The transmit and receive 1519–1522 byte frame counter. This bit is incremented for each good or bad frame transmitted and received which between 1519–1522 bytes in length inclusive (excluding framing bits but including FCS bytes).
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.58 Receive Byte Counter (RYBT)

GE0 Address: 0x1900021C
GE1 Address: 0x1A00021C
Access: Read/Write
Reset: 0x0

This register is used to count incoming frames and then increment this register accordingly.

Bit	Bit Name	Description
23:0	RBYT	The receive byte counter. This statistic count register is incremented by the byte count of all frames received, including bad packets but excluding framing bits but including FCS bytes.
31:23	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.59 Receive Packet Counter (RPKT)

GE0 Address: 0x19000220
GE1 Address: 0x1A000220

Access: Read/Write
Reset: 0x0

This register is used to count packets received.

Bit	Bit Name	Description
17:0	RPKT	The receive packet counter. This register is incremented for each received packet (including bad packets, all Unicast, broadcast and Multicast packets).
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.60 Receive FCS Error Counter (RFCS)

GE0 Address: 0x19000224
GE1 Address: 0x1A000224
Access: Read/Write
Reset: 0x0

This register is used to count frames received between 64–1518 in length and has a FCS error.

Bit	Bit Name	Description
11:0	RFCS	The received FCS error counter. This register is incremented for each frame received that has an integral 64–1518 length and contains a frame check sequence error.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.61 Receive Multicast Packet Counter (RMCA)

GE0 Address: 0x19000228
GE1 Address: 0x1A000228
Access: Read/Write
Reset: 0x0

This register is used to count received good standard multicast packets.

Bit	Bit Name	Description
17:0	RMCA	The receive multicast packet counter. This register is incremented for each multicast good frame of lengths smaller than 1518 (non-VLAN) or 1522 (VLAN) excluding broadcast frames. This does not include range/length errors.
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.62 Receive Broadcast Packet Counter (RBCA)

GE0 Address: 0x1900022C
GE1 Address: 0x1A00022C
Access: Read/Write
Reset: 0x0

This register is used to count received good broadcast frames.

Bit	Bit Name	Description
21:0	RBCA	The receive broadcast packet counter. This register is incremented for each broadcast good frame of lengths smaller than 1518 (non-VLAN) or 1522 (VLAN) excluding multicast frames. This does not include range or length errors.
31:22	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.63 Receive Control Frame Packet Counter (RXCF)

GE0 Address: 0x19000230
GE1 Address: 0x1A000230
Access: Read/Write
Reset: 0x0

This register is used to count received MAC control frames.

Bit	Bit Name	Description
17:0	RXCF	The receive control frame packet counter. This register is incremented for each MAC control frame received (pause and unsupported).
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.64 Receive Pause Frame Packet Counter (RXPF)

GE0 Address: 0x19000234
GE1 Address: 0x1A000234
Access: Read/Write
Reset: 0x0

This register is used to count received pause frame packets.

Bit	Bit Name	Description
11:0	RXPF	The receive pause frame packet counter. This register is incremented each time a valid pause MAC control frame is received.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.65 Receive Unknown OPCode Packet Counter (RXUO)

GE0 Address: 0x19000238
GE1 Address: 0x1A000238
Access: Read/Write
Reset: 0x0

This register is used to count received MAC control frames that contain an opcode.

Bit	Bit Name	Description
11:0	RXUO	The receive unknown OPcode counter. This bit is incremented each time a MAC control frame is received which contains an opcode other than a pause.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.66 Receive Alignment Error Counter (RALN)

GE0 Address: 0x1900023C
GE1 Address: 0x1A00023C
Access: Read/Write
Reset: 0x0

This register is used to count received packets with an alignment error.

Bit	Bit Name	Description
11:0	RALN	The receive alignment error counter. This register is incremented for each received frame from 64–1518 bytes that contains an invalid FCS and is not an integral number of bytes.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.67 Receive Frame Length Error Counter (RFLR)

GE0 Address: 0x19000240
GE1 Address: 0x1A000240
Access: Read/Write
Reset: 0x0

This register is used to count received frames that have a length error.

Bit	Bit Name	Description
15:0	RFLR	The received frame length error counter. this register is incremented for each received frame in which the 802.3 length field did not match the number of data bytes actually received (46–1500 bytes). The counter is not incremented if the length field is not a valid 802.3 length, such as an EtherType value.
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.68 Receive Code Error Counter (RCDE)

GE0 Address: 0x19000244
GE1 Address: 0x1A000244
Access: Read/Write
Reset: 0x0

This register is used to count the number of received frames that had a code error counter.

Bit	Bit Name	Description
11:0	RCDE	The receive code error counter. This register is incremented each time a valid carrier was present and at least one invalid data symbol was detected.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.69 Receive Carrier Sense Error Counter (RCSE)

GE0 Address: 0x19000248
GE1 Address: 0x1A000248
Access: Read/Write
Reset: 0x0

This register is used to count the number of frames received that had a false carrier.

Bit	Bit Name	Description
11:0	RCSE	The receive false carrier counter. This register is incremented each time a false carrier is detected during idle, as defined by a 1 on RX_ER and an 0xE on RXD. This event is reported along with the statistics generated on the next received frame. Only one false carrier condition can be detected and logged between frames.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.70 Receive Undersize Packet Counter (RUND)

GE0 Address: 0x1900024C
GE1 Address: 0x1A00024C
Access: Read/Write
Reset: 0x0

This register is used to count the number of received packets that were undersized.

Bit	Bit Name	Description
11:0	RUND	The receive undersize packet counter. This register is incremented each time a frame is received which is less than 64 bytes in length and contains a valid FCS and were otherwise well formed. This does not include Range Length errors
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.71 Receive Oversize Packet Counter (ROVR)

GE0 Address: 0x19000250
GE1 Address: 0x1A000250
Access: Read/Write
Reset: 0x0

This register is used to count received packets that were oversized.

Bit	Bit Name	Description
11:0	ROVR	The receive oversize packet counter., This register is incremented each time a frame is received which exceeded 1518 (non-VLAN) or 1522 (VLAN) and contains a valid FCS and were otherwise well formed. This does not include Range Length errors.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.72 Receive Fragments Counter (RFRG)

GE0 Address: 0x19000254
GE1 Address: 0x1A000254
Access: Read/Write
Reset: 0x0

This register is used to count received fragmented frames.

Bit	Bit Name	Description
11:0	RFRG	The receive fragments counter. This register is incremented for each frame received which is less than 64 bytes in length and contains an invalid FCS. This includes integral and non-integral lengths.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.73 Receive Jabber Counter (RJBR)

GE0 Address: 0x19000258
GE1 Address: 0x1A000258
Access: Read/Write
Reset: 0x0

This register is used to count received jabber frames.

Bit	Bit Name	Description
11:0	RJBR	The received jabber counter. This register is incremented for frames which exceed 1518 (non-VLAN) or 1522 (VLAN) bytes and contains an invalid FCS, including alignment errors.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.74 Receive Dropped Packet Counter (RDRP)

GE0 Address: 0x1900025C
GE1 Address: 0x1A00025C
Access: Read/Write
Reset: 0x0

This register is used to count received dropped packets.

Bit	Bit Name	Description
11:0	RDRP	The received dropped packets counter. this register is incremented for frames received which are streamed to the system but are later dropped due to a lack of system resources.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.75 Transmit Byte Counter (TBYT)

GE0 Address: 0x19000260
GE1 Address: 0x1A000260
Access: Read/Write
Reset: 0x0

This register is used to count transmitted bytes.

Bit	Bit Name	Description
23:0	TYBT	The transmit byte counter. This register is incremented by the number of bytes that were put on the wire including fragments of frames that were involved with collisions. This count does not include preamble/SFD or jam bytes.
31:24	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.76 Transmit Packet Counter (TPKT)

GE0 Address: 0x19000264
GE1 Address: 0x1A000264
Access: Read/Write
Reset: 0x0

This register is used to count transmitted packets.

Bit	Bit Name	Description
17:0	TPKT	The transmit packet counter. This register is incremented for each transmitted packet (including bad packets, excessive deferred packets, excessive collision packets, late collision packets, all Unicast, Broadcast and Multicast packets.
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.77 Transmit Multicast Packet Counter (TMCA)

GE0 Address: 0x19000268
GE1 Address: 0x1A000268
Access: Read/Write
Reset: 0x0

This register is used to count transmitted multicast packets.

Bit	Bit Name	Description
17:0	TMCA	Transmit multicast packet counter. Incremented for each multicast valid frame transmitted (excluding broadcast frames).
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.78 Transmit Broadcast Packet Counter (TBCA)

GE0 Address: 0x1900026C
GE1 Address: 0x1A00026C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted broadcast packets.

Bit	Bit Name	Description
17:0	TBCA	Transmit broadcast packet counter. Incremented for each broadcast frame transmitted (excluding multicast frames).
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.79 Transmit Pause Control Frame Counter (TXPF)

GE0 Address: 0x19000270
GE1 Address: 0x1A000270
Access: Read/Write
Reset: 0x0

This register is used to count transmitted pause control frames.

Bit	Bit Name	Description
11:0	TXPF	Transmit pause frame packet counter. Incremented each time a valid pause MAC control frame is transmitted.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.80 Transmit Deferral Packet Counter (TDFR)

GE0 Address: 0x19000274
GE1 Address: 0x1A000274
Access: Read/Write
Reset: 0x0

This register is used to count transmitted deferral packets.

Bit	Bit Name	Description
11:0	TDFR	Transmit deferral packet counter. Incremented for each frame that was deferred on its first transmission attempt. Does not include frames involved in collisions.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.81 Transmit Excessive Deferral Packet Counter (TEDF)

GE0 Address: 0x19000278
GE1 Address: 0x1A000278
Access: Read/Write
Reset: 0x0

This register is used to count excessive transmitted deferral packets.

Bit	Bit Name	Description
11:0	TEDF	Transmit excessive deferral packet counter. Incremented for frames aborted that were deferred for an excessive period of time (3036 byte times).
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.82 Transmit Single Collision Packet Counter (TSCL)

GE0 Address: 0x1900027C
GE1 Address: 0x1A00027C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted single collision packets.

Bit	Bit Name	Description
11:0	TSCL	Transmit single collision packet counter. Incremented for each frame transmitted that experienced exactly one collision during transmission.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.83 Transmit Multiple Collision Packet (TMCL)

GE0 Address: 0x19000280
GE1 Address: 0x1A000280
Access: Read/Write
Reset: 0x0

This register is used to count transmitted multiple collision packets.

Bit	Bit Name	Description
11:0	TMCL	Transmit multiple collision packet counter. Incremented for each frame transmitted that experienced 2–15 collisions (including any late collisions) during transmission as defined using the RETRY[3:0] field of the Tx function control register.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.84 Transmit Late Collision Packet Counter (TLCL)

GE0 Address: 0x19000284
GE1 Address: 0x1A000284
Access: Read/Write
Reset: 0x0

This register is used to count transmitted late collision packets.

Bit	Bit Name	Description
11:0	TLCL	Transmit late collision packet counter. Incremented for each frame transmitted that experienced a late collision during a transmission attempt. Late collisions are defined using the LCOL[5:0] field of the Tx function control register.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.85 Transmit Excessive Collision Packet Counter (TXCL)

GE0 Address: 0x19000288
GE1 Address: 0x1A000288
Access: Read/Write
Reset: 0x0

This register is used to count excessive transmitted collision packets.

Bit	Bit Name	Description
11:0	TXCL	Transmit excessive collision packet counter. Incremented for each frame that experienced 16 collisions during transmission and was aborted.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.86 Transmit Total Collision Counter (TNCL)

GE0 Address: 0x1900028C
GE1 Address: 0x1A00028C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted total collision packets.

Bit	Bit Name	Description
12:0	TNCL	Transmit total collision counter. Incremented by the number of collisions experienced during the transmission of a frame as defined as the simultaneous presence of signals on the DO and RD circuits (i.e., transmitting and receiving at the same time). Note, this register does not include collisions that result in an excessive collision condition).
31:13	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.87 Transmit Pause Frames Honored Counter (TPFH)

GE0 Address: 0x19000290
GE1 Address: 0x1A000290
Access: Read/Write
Reset: 0x0

This register is used to count honored transmitted pause frames.

Bit	Bit Name	Description
11:0	TPFH	Transmit pause frames honored counter. Incremented each time a valid pause MAC control frame is transmitted and honored.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.88 Transmit Drop Frame Counter (TDRP)

GE0 Address: 0x19000294
GE1 Address: 0x1A000294
Access: Read/Write
Reset: 0x0

This register is used to count transmitted drop frames.

Bit	Bit Name	Description
11:0	TDRP	Transmit drop frame counter. Incremented each time input PFH is asserted.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.89 Transmit Jabber Frame Counter (TJBR)

GE0 Address: 0x19000298
GE1 Address: 0x1A000298
Access: Read/Write
Reset: 0x0

This register is used to count transmitted jabber frames.

Bit	Bit Name	Description
11:0	TJBR	Transmit jabber frame counter. Incremented for each oversized transmitted frame with an incorrect FCS value.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.90 Transmit FCS Error Counter (TFCS)

GE0 Address: 0x1900029C
GE1 Address: 0x1A00029C
Access: Read/Write
Reset: 0x0

This register is used to count transmitted FCS errors.

Bit	Bit Name	Description
11:0	TFCS	Transmit FCS error counter. Incremented for every valid sized packet with an incorrect FCS value.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.91 Transmit Control Frame Counter (TXCF)

GE0 Address: 0x190002A0
GE1 Address: 0x1A0002A0
Access: Read/Write
Reset: 0x0

This register is used to count transmitted control frames.

Bit	Bit Name	Description
11:0	TXCF	Transmit control frame counter. Incremented for every valid size frame with a type field signifying a control frame.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.92 Transmit Oversize Frame Counter (TOVR)

GE0 Address: 0x190002A4
GE1 Address: 0x1A0002A4
Access: Read/Write
Reset: 0x0

This register is used to count transmitted oversize frames.

Bit	Bit Name	Description
11:0	TOVR	Transmit oversize frame counter. Incremented for each oversized transmitted frame with an correct FCS value.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.93 Transmit Undersize Frame Counter (TUND)

GE0 Address: 0x190002A8
GE1 Address: 0x1A0002A8
Access: Read/Write
Reset: 0x0

This register is used to count transmitted undersize frames.

Bit	Bit Name	Description
11:0	TUND	Transmit undersize frame counter. Incremented for every frame less then 64 bytes, with a correct FCS value.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.94 Transmit Fragment Counter (TFRG)

GE0 Address: 0x190002AC
GE1 Address: 0x1A0002AC
Access: Read/Write
Reset: 0x0

This register is used to count transmitted fragments.

Bit	Bit Name	Description
11:0	TFRG	Transmit fragment counter. Incremented for every frame less then 64 bytes, with an incorrect FCS value.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.95 Carry Register 1 (CAR1)

GE0 Address: 0x190002B0
GE1 Address: 0x1A0002B0
Access: Read-Only
Reset: 0x0

Carry register bits are cleared on carry register write while the respective bit is asserted.

Bit	Bit Name	Description
0	C1_RDR	Carry register 1 RDRP counter carry bit
1	C1_RJB	Carry register 1 RJBR counter carry bit
2	C1_RFR	Carry register 1 RFRG counter carry bit
3	C1_ROV	Carry register 1 ROVR counter carry bit
4	C1_RUN	Carry register 1 RUND counter carry bit
5	C1_RCS	Carry register 1 RCSE counter carry bit
6	C1_RCD	Carry register 1 RCDE counter carry bit
7	C1_RFL	Carry register 1 RFLR counter carry bit
8	C1_RAL	Carry register 1 RALN counter carry bit
9	C1_RXU	Carry register 1 RXUO counter carry bit
10	C1_RXP	Carry register 1 RXPF counter carry bit
11	C1_RXC	Carry register 1 RXCF counter carry bit
12	C1_RBC	Carry register 1 RBCA counter carry bit
13	C1_RMC	Carry register 1 RMCA counter carry bit
14	C1_RFC	Carry register 1 RFCS counter carry bit
15	C1_RPK	Carry register 1 RPKT counter carry bit
16	C1_RBY	Carry register 1 RBYT counter carry bit
24:17	RES	Reserved. Must be written with zero. Contains zeros when read.
25	C1_MGV	Carry register 1 TRMGV counter carry bit
26	C1_MAX	Carry register 1 TRMAX counter carry bit
27	C1_1K	Carry register 1 TR1K counter carry bit
28	C1_511	Carry register 1 TR511 counter carry bit
29	C1_255	Carry register 1 TR255 counter carry bit
30	C1_127	Carry register 1 TR127 counter carry bit
31	C1_64	Carry register 1 TR64 counter carry bit

3.7.96 Carry Register 2 (CAR2)

GE0 Address: 0x190002B4
GE1 Address: 0x1A0002B4
Access: Read-Only
Reset: 0x0

Carry register bits are cleared on carry register write while the respective bit is asserted.

Bit	Bit Name	Description
0	C2_TDP	Carry register 2 TDRP counter carry bit
1	C2_TPH	Carry register 2 TPFH counter carry bit
2	C2_TNC	Carry register 2 TNCL counter carry bit
3	C2_TXC	Carry register 2 TXCL counter carry bit
4	C2_TLC	Carry register 2 TLCL counter carry bit
5	C2_TMA	Carry register 2 TMCL counter carry bit
6	C2_TSC	Carry register 2 TSCL counter carry bit
7	C2_TED	Carry register 2 TEDF counter carry bit
8	C2_TDF	Carry register 2 TDFR counter carry bit
9	C2_TPF	Carry register 2 TXPF counter carry bit
10	C2_TBC	Carry register 2 TBCA counter carry bit
11	C2_TMC	Carry register 2 TMCA counter carry bit
12	C2_TPK	Carry register 2 TPKT counter carry bit
13	C2_TBY	Carry register 2 TBYT counter carry bit
14	C2_TFG	Carry register 2 TFRG counter carry bit
15	C2_TUN	Carry register 2 TUND counter carry bit
16	C2_TOV	Carry register 2 TOVR counter carry bit
17	C2_TCF	Carry register 2 TXCF counter carry bit
18	C2_TFC	Carry register 2 TFCS counter carry bit
19	C2_TJB	Carry register 2 TJBR counter carry bit
31:20	RES	Reserved. Must be written with zero. Contains zeros when read.

3.7.97 Carry Mask Register 1 (CAM1)

GE0 Address: 0x190002B8
GE1 Address: 0x1A0002B8
Access: Read/Write
Reset: 0x1

When one of these mask bits is set to zero, the corresponding interrupt bit is allowed to cause interrupt indications on output CARRY.

Bit	Bit NaM1e	Description
0	M1_RDR	Mask register 1 RDRP counter carry bit
1	M1_RJB	Mask register 1 RJBR counter carry bit
2	M1_RFR	Mask register 1 RFRG counter carry bit
3	M1_ROV	Mask register 1 ROVR counter carry bit
4	M1_RUN	Mask register 1 RUND counter carry bit
5	M1_RCS	Mask register 1 RCSE counter carry bit
6	M1_RCD	Mask register 1 RCDE counter carry bit
7	M1_RFL	Mask register 1 RFLR counter carry bit
8	M1_RAL	Mask register 1 RALN counter carry bit
9	M1_RXU	Mask register 1 RXUO counter carry bit
10	M1_RXP	Mask register 1 RXPF counter carry bit
11	M1_RXC	Mask register 1 RXCF counter carry bit
12	M1_RBC	Mask register 1 RBCA counter carry bit
13	M1_RMC	Mask register 1 RMCA counter carry bit
14	M1_RFC	Mask register 1 RFCS counter carry bit
15	M1_RPK	Mask register 1 RPKT counter carry bit
16	M1_RBY	Mask register 1 RBYT counter carry bit
24:17	RES	Reserved. Must be written with zero. Contains zeros when read.
25	M1_MGV	Mask register 1 TRMGV counter carry bit
26	M1_MAX	Mask register 1 TRMAX counter carry bit
27	M1_1K	Mask register 1 TR1K counter carry bit
28	M1_511	Mask register 1 TR511 counter carry bit
29	M1_255	Mask register 1 TR255 counter carry bit
30	M1_127	Mask register 1 TR127 counter carry bit
31	M1_64	Mask register 1 TR64 counter carry bit

3.7.98 Carry Mask Register 2 (CAM2)

GE0 Address: 0x190002BC
GE1 Address: 0x1A0002BC
Access: Read/Write
Reset: 0x1

When one of these mask bits is set to zero, the corresponding interrupt bit is allowed to cause interrupt indications on output CARRY.

Bit	Bit Name	Description
0	M2_TDP	Mask register 2 TDRP counter carry bit
1	M2_TPH	Mask register 2 TPFH counter carry bit
2	M2_TNC	Mask register 2 TNCL counter carry bit
3	M2_TXC	Mask register 2 TXCL counter carry bit
4	M2_TLC	Mask register 2 TLCL counter carry bit
5	M2_TMA	Mask register 2 TMCL counter carry bit
6	M2_TSC	Mask register 2 TSCL counter carry bit
7	M2_TED	Mask register 2 TEDF counter carry bit
8	M2_TDF	Mask register 2 TDFR counter carry bit
9	M2_TPF	Mask register 2 TXPF counter carry bit
10	M2_TBC	Mask register 2 TBCA counter carry bit
11	M2_TMC	Mask register 2 TMCA counter carry bit
12	M2_TPK	Mask register 2 TPKT counter carry bit
13	M2_TBY	Mask register 2 TBYT counter carry bit
14	M2_TFG	Mask register 2 TFRG counter carry bit
15	M2_TUN	Mask register 2 TUND counter carry bit
16	M2_TOV	Mask register 2 TOVR counter carry bit
17	M2_TCF	Mask register 2 TXCF counter carry bit
18	M2_TFC	Mask register 2 TFCS counter carry bit
19	M2_TJB	Mask register 2 TJBR counter carry bit
31:20	RES	Reserved. Must be written with zero. Contains zeros when read.

3.8 USB Registers

Table shows the USB registers for the AR7240.

Table 3-10. **USB Registers**

Offset	Register	Page
0x1B000000	HC Revision	page 106
0x1B000004	HC Control	page 107
0x1B000008	HC Command Status	page 108
0x1B00000C	HC Interrupt Status	page 108
0x1B000010	HC Interrupt Enable	page 109
0x1B000014	HC Interrupt Disable	page 110
0x1B000018	HC HCCA	page 110
0x1B00001C	HC Period Current Endpoint Descriptor	page 111
0x1B000020	HC Period Head Endpoint Descriptor	page 111
0x1B000024	HC Control Current Endpoint Descriptor	page 111
0x1B000028	HC Bulk Head Endpoint Descriptor	page 111
0x1B00002C	HC Bulk Current Endpoint Descriptor	page 112
0x1B000030	HC Done Head	page 112
0x1B000034	HC FM Interval	page 112
0x1B000038	HC FM Remaining	page 113
0x1B00003C	HC FM Number	page 113
0x1B000040	HC Periodic Start	page 113
0x1B000044	HC LS Threshold	page 113
0x1B000048	HC Root Hub Descriptor A	page 114
0x1B00004C	HC Root Hub Descriptor B	page 115
0x1B000050	HC Root Hub Status	page 115
0x1B000054	HC Root Hub Port Status	page 116

3.8.1 HC Revision

Address: 0x1B000000
Access: Read-Only
Reset: See field description

This register denotes the HCI version specified by the host controller.

Bit	Bit Name	Reset	Description
7:0	REV	0x10	Contains the BCD representation of the version of the HCI specification that is implemented by the host controller
31:8	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.8.2 HC Control

Address: 0x1B000004
Access: Read/Write
Reset: 0x0

This register is used to define the operating modes for the host controller.

Bit	Bit Name	Description
1:0	CBSR	Control Bulk Service Ratio. These bits specify the service ratio between Control and bulk endpoint descriptors.

CBSR	Number of Control Endpoint Descriptors Over Bulk Endpoint Descriptors Served
0	1:1
1	2:1
2	3:1
3	4:1

Bit	Bit Name	Description
2	PLE	Periodic List Enable. Setting this bit enables the periodic list to be produced in the next frame.
3	IE	Isochronous Enable. This bit enables the host controller to process isochronous endpoint descriptors, when the host controller processes a periodic list in a frame
4	CLE	Control List Enable. Setting this bit enables the processing of the Control list in the next frame.
5	BLE	Bulk List Enable. Setting this bit enables processing of the Bulk list in the next frame.
7:6	HCFS	Host Controller Functional State. These bits set the host controller state for the USB.

00	USB Reset
01	USB Resume
10	USB Operational
11	USB Suspend

Bit	Bit Name	Description
8	IR	Interrupt Routing. These bits determine the routing of interrupts generated by events registered in the HC Interrupt Status. If cleared, interrupts are routed to the normal host bus interrupt mechanism. If set, all interrupts are routed to the System Management Interrupt (SMI).
9	RWC	Remote Wakeup Connected. This bit indicates whether the host controller supports remote wakeup signaling.
10	RWE	Remote Wakeup Enable. This bit is used by the host controller driver to enable or disable the remote wakeup feature upon detection of an upstream resume signaling. When this bit is set, and the Resume Detected bit in the HC Interrupt Status Register is set, a remote wakeup is signalled to the host system.
31:11	RES	Reserved. Must be written with zero. Contains zeros when read.

3.8.3 HC Command Status

Address: 0x1B000008
Access: Read/Write
Reset: 0x0

This register is used by the host controller to receive commands issued by the host controller driver, as well as reflecting the current status of the host controller.

Bit	Bit Name	Description
0	HCR	Host Controller Reset. This bit is set by the host controller driver to initiate a software reset of the host controller which must be completed within 10 µs. This bit is cleared by the host controller when the reset has completed.
1	CLF	Control List Filled. This bit indicates whether there are any transfer descriptors on the control list. When a transfer descriptor is added to an endpoint descriptor in the control list, this bit is set by the host controller driver.
2	BLF	Bulk List Filled. This bit is used to indicate whether there are any transfer descriptors on the bulk list. This bit is set when the HCD adds a transfer descriptor to an endpoint descriptor in the bulk list.
3	OCR	Ownership Change Request. This bit is set by an OS host controller driver to request a change of control of the host controller. When set, the host controller will set the Ownership Change field in the HC Interrupt Status Register.
15:4	RES	Reserved. Must be written with zero. Contains zeros when read.
17:16	SOC	Scheduling Overrun Count. This bit is incremented on each scheduling overrun error occurrence.
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.8.4 HC Interrupt Status

Address: 0x1B00000C
Access: Read/Write
Reset: 0x0

This register provides status on various events that cause hardware interrupts. When an interrupt occurs, the host controller sets the corresponding bits in this register.

Bit	Bit Name	Description
0	SO	The Scheduling Overrun. This bit is set when the USB update schedule for the current frame overruns. It is also set after an update of the HccaFrameNumber.
1	WDH	Writeback Done Head. This bit is set after the host controller has written the host controller Done Head to the host controller communication area Done Head bit.
2	SF	Start of Frame. Set by the host controller at the start of each frame and after the Frame Number bit has been updates.
3	RD	Resume Detected. This bit is set when the host controller detects that a device on the USB is trying to resume signaling.
4	UE	Unrecoverable Error. This bit is set when the host controller detects a system error not related to the USB. This bit is cleared by the host controller driver after the host controller has been reset.
5	FNO	Frame Number Overflow. This bit is set when the bit 15 of the HC FM Number (bit 15) register changes its value, or the host controller communication area Frame Number has been updated.
6	RHSC	Root Hub Status Change. Set when the content of the host controller RH Status or RH Port Status has changed.
29:7	RES	Reserved. Must be written with zero. Contains zeros when read.
30	OC	Ownership Change. Set by the host controller when the host controller driver sets the Ownership Change Request field in the "HC Command Status" on page 108. This event, unmasked, generates a System Management Interrupt (SMI).
31	RES	Reserved. Must be written with zero. Contains zeros when read.

3.8.5 HC Interrupt Enable

Address: 0xB000010
Access: Read/Write
Rest: 0x0

This register is used to control which events generate a hardware interrupt when a bit is set in this register, the corresponding bit in the HC Interrupt Status Register and the Master Interrupt Enable Register.

Bit	Bit Name	Description	
0	SO	0	Ignore
		1	Enable interrupt generation due to Scheduling Overrun
1	WDH	0	Ignore
		1	Enable interrupt generation due to HC Done Head Writeback
2	SF	0	Ignore
		1	Enable interrupt generation due to Start of Frame
3	RD	0	Ignore
		1	Enable interrupt generation due to Resume Detect
4	UE	0	Ignore
		1	Enable interrupt generation due to Unrecoverable Error
5	FNO	0	Ignore
		1	Enable interrupt generation due to Frame Number Overflow
6	RHSC	0	Ignore
		1	Enable interrupt generation due to Root Hub Status Change
29:7	RES	Reserved. Must be written with zero. Contains zeros when read.	
30	OC	0	Ignore
		1	Enable interrupt generation due to Ownership Change
31	MIE	0	Ignore
		1	Enables an interrupt generation due to events specified in other bits of this register. Used as a Master Interrupt Enable by the host controller driver.

3.8.6 HC Interrupt Disable

Address: 0xB000014
Access: Read/Write
Rest: 0x0

Bit	Bit Name	Description	
0	SO	0	Ignore
		1	Disable interrupt generation due to Scheduling Overrun
1	WDH	0	Ignore
		1	Disable interrupt generation due to HC Done Head Writeback
2	SF	0	Ignore
		1	Disable interrupt generation due to Start of Frame
3	RD	0	Ignore
		1	Disable interrupt generation due to Resume Detect
4	UE	0	Ignore
		1	Disable interrupt generation due to Unrecoverable Error
5	FNO	0	Ignore
		1	Disable interrupt generation due to Frame Number Overflow
6	RHSC	0	Ignore
		1	Disable interrupt generation due to Root Hub Status Change
29:7	RES	Reserved. Must be written with zero. Contains zeros when read.	
30	OC	0	Ignore
		1	Disable interrupt generation due to Ownership Change
31	MIE	0	Ignore
		1	Disables an interrupt generation due to events specified in other bits of this register. Used as a Master Interrupt Enable by the host controller driver.

3.8.7 HC HCCA Register

Address: 0x1B000018
Access: Read/Write
Reset: 0x0

This register contains the physical address of the Host Controller Communication area, the control structures and the Interrupt table that are accessed by both the host controller and its corresponding driver.

Bit	Bit Name	Description
7:0	RES	Reserved. Must be written with zero. Contains zeros when read.
31:8	HCCA	The base address of the Host Controller Communication Area

3.8.8 HC Period Current ED

Address: 0x1B00001C
Access: Read/Write
Reset: 0x0

This register contains the physical address of the current Isochronous or Interrupt Endpoint Descriptor.

Bit	Bit Name	Description
3:0	RES	Reserved. Must be written with zero. Contains zeros when read.
31:4	PCED	Period Current Endpoint Descriptor. Used by the host controller to point to the head of one of the periodic lists which will be processed in the current frame. Updated by the host controller after a periodic endpoint descriptor has been processed.

3.8.9 HC Control Head Endpoint Descriptor

Address: 0x1B000020
Access: Read/Write
Reset: 0x0

This register contains the physical address of the first Endpoint Descriptor of the control list.

Bit	Bit Name	Description
3:0	RES	Reserved. Must be written with zero. Contains zeros when read.
31:4	CHED	Control Head Endpoint Descriptor. The host controller crosses the control list starting with this register's pointer.

3.8.10 HC Control Current Endpoint Descriptor

Address: 0x1B000024
Access: Read/Write
Reset: 0x0

This register contains the physical address of the current endpoint descriptor of the control list.

Bit	Bit Name	Description
3:0	RES	Reserved. Must be written with zero. Contains zeros when read.
31:4	CCED	Control Current Endpoint Descriptor. Advances the pointer to the next endpoint descriptor after serving the present one.

3.8.11 HC Bulk Head Endpoint Descriptor

Address: 0x1B000028
Access: Read/Write
Reset: 0x0

This register contains the physical address of the first endpoint descriptor of the bulk list.

Bit	Bit Name	Description
3:0	RES	Reserved. Must be written with zero. Contains zeros when read.
31:4	BHED	Bulk Head Endpoint Descriptor. The host controller goes through the bulk list starting with this register.

3.8.12 HC Bulk Current Endpoint Descriptor

Address: 0x1B00002C
Access: Read/Write
Reset: 0x0

This register contains the physical address of the current endpoint descriptor of the bulk list. Done in round-robin ordering, the endpoints will be ordered according to their insertion in the list.

Bit	Bit Name	Description
3:0	RES	Reserved. Must be written with zero. Contains zeros when read.
31:4	BCED	Bulk Current Endpoint Descriptor. The host controller advances the pointer to the next endpoint descriptor after the present one has been served. This process continues from where it left off in the last frame.

3.8.13 HC Done Head

Address: 0x1B000030
Access: Read/Write
Reset: 0x0

This register contains the physical address of the last completed transfer descriptor that was added to the done queue.

Bit	Bit Name	Description
3:0	RES	Reserved. Must be written with zero. Contains zeros when read.
31:4	DH	Done Head. When a transfer descriptor has completed, the host controller writes the contents of this register to the NEXT TD field of the transfer descriptor, and then overwrites the transfer descriptor address to this field. It also sets the Write Back Done Head of the "HC Interrupt Status" on page 108.

3.8.14 HC FM Interval

Address: 0x1B000034
Access: Read/Write
Reset: See field description

This register contains a 14-bit value which indicates the bit time interval in a frame, and a 15-bit value indicating the full speed maximum packet size that the host controller may transmit or receive without causing a scheduling overrun.

Bit	Bit Name	Reset	Description
13:0	FI	0x2EDF	Frame Interval. Specifies the interval between two consecutive SOFs in bit times. The nominal value is set to 11,999.
15:14	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
30:16	FSMPS	TBD	FS Largest Data Packet. This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame, which is calculated by the host controller driver. The counter value represents the largest amount of data in bits which can be sent or received by the host controller in a single transaction at any given time without causing a scheduling overrun.
31	FIT	0x0	Frame Interval Toggle. The host controller driver togglers this bit whenever it loads a new value into the Frame Interval.

3.8.15 HC FM Remaining

Address: 0x1B000038
Access: Read/Write
Reset: 0x0

This register is a 14-bit down counter showing the bit time remaining in the current frame.

Bit	Bit Name	Description
13:0	FR	Frame Remaining. This counter is decremented at each bit time and when it reaches zero, it is reset by loading the Frame Interval value specified in the register "HC FM Interval" on page 112, at the next boundary. When entering the USB operational state, the host controller reloads the content with the Frame Interval value and uses the updated value from the next start of frame packet.
30:14	RES	Reserved. Must be written with zero. Contains zeros when read.
31	FRT	Frame Remaining Toggle. This bit is loaded from the Frame Interval Toggle field of the register "HC FM Interval" on page 112 whenever the FR bit reaches zero.

3.8.16 HC FM Number

Address: 0x1B00003C
Access: Read/Write
Reset: 0x0

This 16-bit counter provides a timing reference among events happening in the host controller and the host controller driver.

Bit	Bit Name	Description
15:0	FN	Frame Number. Incremented when the register "HC FM Remaining" on page 113 is reloaded. This bit will be automatically incremented when entering the USB operational state.
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.

3.8.17 HC Periodic Start

Address: 0x1B000040
Access: Read/Write
Reset: 0x0

This register has a 14-bit programmable value which determines when is the earliest time the host controller should start processing the periodic list.

Bit	Bit Name	Description
13:0	RES	Reserved. Must be written with zero. Contains zeros when read.
31:14	PS	Periodic Start. The value written to this field by the host controller driver is roughly 10% off from the "HC FM Interval" on page 112. (typical value is 0x3E67) After reaching this value, processing of the periodic lists will have priority over control or bulk processing.

3.8.18 HC LS Threshold

Address: 0x1B000044
Access: Read/Write
Reset: See field description

This 11-bit value is used by the host controller to determine whether to commit to the transfer of a maximum of 8-byte LS packet before the end of frame packet is issued.

Bit	Bit Name	Description
11:0	LST	Low Speed Threshold. The value of this field is compared to the Frame Remaining field and if it is found to be less than or equal to this field, the transaction commences.
31:12	RES	Reserved. Must be written with zero. Contains zeros when read.

3.8.19 HC Root Hub Descriptor A

Address: 0x1B000048
Access: Read/Write
Reset: See field description

This register, and the following "HC Root Hub Descriptor B" are used to describe the characteristics of the Root Hub.

Bit	Bit Name	Reset	Description	
7:0	NDP	See note [1]	Number Downstream Ports. Used to specify the number of downstream ports supported by the root hub, and is dependant on the implementation. the minimum number of ports is 1 and the maximum is 15.	
8	PSM	See note [1]	Power Switching Mode. Used to specify how the power switching method of the Root Hub is controlled, which is dependant on the implementation.	
			0	All ports are powered at the same time
			1	Each port is powered individually, which may be controlled by the global switch or per-port switching. If the Port Power Control Mask bit is set, the port responds only to port power commands. If cleared, then it is controlled by the global switch.
9	NPS	See note [1]	No Power Switching. Used to specify whether power switching is supported or if ports are always powered, and is dependant on the implementation.	
			0	Ports are power switched
			1	Ports are always powered when the host controller is powered on
10	DT	0x0	Device Type. Specifies that the Root Hub is not a compound device. Since the Root Hub is not permitted to be a compound device, this bit should always be written as zero.	
11	OCPM	See note [1]	Over Current Protection Mode. This bit describes the reporting method for an overcurrent status for the Root Hub.	
			0	Overcurrent status is reported collectively for all downstream ports
			1	Overcurrent status is reported on a per-port basis
12	NOCP	See note [1]	No overcurrent protection. This bit describes how the overcurrent status for the root hub is reported.	
			0	Overcurrent status is reported collectively for all downstream ports
			1	No overcurrent protection supported
23:13	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
31:24	POTPGT	See note [1]	Power on to Power Good Time. Specifies the duration the host controller driver must wait before accessing a powered-on port of the Root Hub, based on implementation. The unit of time is 2 ms. The duration is calculated as POTPGT x 2 ms.	

[1] Represents an implementation-specific reset value.

3.8.20 HC Root Hub Descriptor B

Address: 0x1B00004C
Access: Read/Write
Reset: See field description

This register This register, and the preceding "HC Root Hub Descriptor A" are used to describe the characteristics of the Root Hub.

Bit	Bit Name	Reset	Description
15:0	DR	See note [1]	Device Removable. Each bit is dedicated to a port of the root hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit [0] is reserved and each bit corresponds to a device attached to that port number. (e.g., if bit [1] is set, there is a device attached to port 1, if bit [2] is set, there is a device attached to port 2 and so on through bit [15]).
31:16	PPCM	See note [1]	Port Power Control Mask. Each bit indicates if a port is affected by a global power control command when the power switching mode bit in the preceding register is set. When set, the port's power state is only affected by per-port power control. When cleared, the port is controlled by the global power switch. If the device is configured to the global switching mode, this field is not valid. Bit [0] is reserved but each following bit corresponds to a ganged-power mask on that port. (e.g., if bit [1] is set, there is a ganged-power mask on port 1. If bit [2] is set, there is a ganged-power mask on port 2, and so on through bit [15]).

[1] Represents an implementation-specific reset value.

3.8.21 HC Root Hub Status

Address: 0x1B000050
Access: Read/Write
Reset: See field description

This register is divided into two parts. The lower word of a Dword represents the HUB Status field while the upper word represents the hub status change field.

Bit	Bit Name	Description		
0	LPS	Read	Local Power Status. The root hub does not support the local power status feature and therefore this bit is already read as 0.	
		Write	Clear global power. In global power mode (power switch mode = 0), this bit is written to 1 to turn off all power. In per-port power mode, it clears the Port Power Status only on ports whose Port Power control Mask bit is not set.	
1	OCI	Over Current Indicator. Represents the overcurrent conditions when global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port over current protection is implemented, this bit always reads 0.		
14:2	RES	Reserved. Must be written with zero. Contains zeros when read.		
15	DRWE	Read	Device remote wakeup enable. This bit enables a connect status change bit as a resume event, causing a USB suspend to USB resume state transition and setting the resume detected interrupt.	
			0	Connect Status Change is not a remote wakeup event
			1	Connect Status change is a remote wakeup event.
		Write	Set remote wakeup enable. Writing a 1 sets the Device Remote Wakeup Event while writing a 0 has no effect.	
16	LPSC	Read	Local Power Status Change. The root hub does not support the local power status feature and therefore, this bit always reads 0	
		Write	Set global power. In global power mode (power switching mode = 0), this bit is written to 1 to turn on power to all ports. In per-port power mode, it sets the port power status only on ports whose port power control mask bit is not set. Writing a 0 has no effect.	
17	OCIC	Over Current Indicator Change. Set by hardware, this bit indicates when a change has occurred to the OCI field of this register. The host controller driver clears this bit by writing a 1. Writing a 0 has no effect.		
30:18	RES	Reserved. Must be written with zero. Contains zeros when read.		
31	CRWE	Clear Remote Wakeup Enable. Writing a 1 by the host controller clears the device remote wakeup enable. Writing a 0 has no effect.		

3.8.22 HC Root Hub Port Status

Address: 0x1B000054
Access: Read/Write
Reset: 0x0

This register is used to control and report port events on a per-port basis. The lower word is used to reflect the port status, whereas the upper word reflects the status change bits.

Bit	Bit Name	Description		
0	CCS	Read	Current connect status. This bit reflects the current state of the downstream port.	
			0	No device connected
			1	Device connected
		Write	Clear port enable. The host controller driver writes a 1 to this bit to clear the Port Enable Status bit. Writing a 0 has no effect. This bit is always read 1 when the attached device is nonremovable (Device removable [NDP])	
1	PES	Read	Port enable status. Indicates whether the port is enabled or disabled.	
			0	Port is disabled
			1	Port is enabled
		Write	Set port enable. This bit sets a port as enabled. If the Current Connect Status is cleared, this write does not set the Port Enable Status, but instead sets the Connect Status Change. This informs the driver that it attempted to enable a disconnected port.	
2	PSS	Read	Port suspend status. This bit indicates that the port is suspended or in the resume sequence.	
			0	Port is not suspended
			1	Port is suspended
		Write	Set port suspend. This bit suspends a disconnected port. If the Current Connect Status is cleared, this write does not set the Port Enable Status, but instead sets the Connect Status Change. This informs the driver that it attempted to enable a disconnected port.	
3	POCI	Read	Port over current indicator. This bit is only valid when the Root Hub is configured such that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0.If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on the this port.	
			0	No overcurrent condition
			1	Overcurrent condition detected
		Write	Clear suspend status. The host controller driver will write a 1 to initiate a resume, initiated only if the Port Suspend Status is set.	
4	PRS	Read	Port reset status. When set, this bit signals a port reset to be asserted.	
			0	Port reset signal is not active
			1	Port reset signal is active
		Write	Set port reset. The host controller driver sets the port reset signaling by writing a 1 to this bit, thus informing the driver that it attempted to reset a disconnected port.	
7:5	RES	Reserved. Must be written with zero. Contains zeros when read.		

8	PPS	Read	Port power status. This bit represents the power status of the port. This bit is cleared if an overcurrent condition is detected.	
			0	Port power is off
			1	Port power is on
		Write	Set port power. The host controller driver writes a 1 to set this bit. This bit always read 1 if power switching is not supported.	
9	LSDA	Read	Low speed device attached. This bit indicates the speed of the device attached to this port.	
			0	Full speed device attached
			1	Low speed device attached
		Write	Clear port power. The host controller driver clears the Port Power Status bit by writing a 1 to this bit.	
15:10	RES	Reserved. Must be written with zero. Contains zeros when read.		
16	CSC	Connect status change. This bit is set whenever a connect or disconnect event occurs. Setting this bit forces the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected.		
		0	No change in the current connect status	
		1	Change in the current connect status	
17	PESC	Port enable status change. This bit is set when the hardware events cause the Port Enable Status bit to be cleared		
		0	No change in port enable status	
		1	Change in the port enable status	
18	PSSC	Port suspend status change. This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3 ms resynchronization delay.		
		0	Resume is not completed	
		1	Resume completed	
19	OCIC	Port overcurrent indicator change. This bit is valid only if the overcurrent conditions are reported on a per-port basis.		
		0	No change in the port overcurrent indicator	
		1	Port Overcurrent indicator has changed	
20	PRSC	Port reset status change. this bit is set at the end of the 10 ms port reset signal.		
		0	Port reset is not complete	
		1	Port reset is complete	
31:21	RES	Reserved. Must be written with zero. Contains zeros when read.		

3.9 Serial Flash Registers

Table 3-11 shows the serial flash registers for the AR7240.

Table 3-11. **Serial Flash Registers**

Offset	Name	Description	Page
0x1F000000	SPI_FUNCTION_SELECT	SPI Function Select Register	page 118
0x1F000004	SPI_CONTROL	SPI Control Register	page 118
0x1F000008	SPI_IO_CONTROL	SPI IO Control	page 119
0x1F00000C	SPI_READ_DATA	SPI Read Data	page 119

3.9.1 SPI Function Select (SPI_FUNC_SELECT)

Address: 0x1F000000
Access: Write-Only
Reset: 0x0

This register is used to enable or disable the SPI.

Bit	Bit Name	Description
0	FUNCTION_SELECT	Setting this bit to 0 enables the SPI functional block. Setting this bit to 1 makes the rest of the registers visible and this register becomes Read/Write accessible.
31:1	RES	Reserved. Must be written with zero. Contains zeros when read.

3.9.2 SPI Control (SPI_CONTROL)

Address: 0x1F000004
Access: Read/Write
Reset: See field description

This register is used to set the functions for the SPI control.

Bit	Bit Name	Reset	Description
5:0	CLOCK_DIVIDER	0x8	Specifies the clock divider setting. Actual clock frequency would be (AHB_CLK/((CLOCK_DIVIDER+1)*2)). Therefore by default, if the AHB_CLK is 200 MHz, this would give 200/18 = ~11MHz.
6	REMAP_DISABLE	0x0	Remaps 4 MB space over unless explicitly disabled by setting this bit to 1. If set to 1, 16 MB is accessible.
31:7	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.9.3 SPI I/O Control (SPI_IO_CONTROL)

Address: 0x1F000008
Access: Read/Write
Reset: 0x0

This register is used to configure the in/out bits for the SPI.

Bit	Bit Name	Description
0	IO_DO	The data bit to be output
7:1	RES	Reserved. Must be written with zero. Contains zeros when read.
8	IO_CLOCK	The clock bit to be output
15:9	RES	Reserved. Must be written with zero. Contains zeros when read.
16	IO_CS_0	The chip select 0 bit to be output
17	IO_CS_1	The chip select 1 bit to be output
18	IO_CS_2	The chip select 2 bit to be output
31:19	RES	Reserved. Must be written with zero. Contains zeros when read.

3.9.4 SPI Read Data (SPI_READ_DATA)

Address: 0x1F00000C
Access: Read-Only
Reset: 0x0

This register is used to return the data read from the flash device with bits sampled after every clock.

Bit	Bit Name	Type	Reset	Description
31:0	READ_DATA	RO	0x0	The read data sampled in every clock

3.10 Ethernet Switch Registers

This section describes the internal registers of the Ethernet Switch registers. Table 3-12 summarizes the Ethernet registers for the Ethernet Switch.

Table 3-12. **Ethernet Switch Registers Summary**

Address	Description	Page
0x0000–0x0098	Global Control Registers	page 121
0x0100–0x0120	Port0 Control Registers	page 133
0x0200–0x0220	Port1 Control Registers	
0x0300–0x0320	Port2 Control Registers	
0x0400–0x0420	Port3 Control Registers	
0x0500–0x0520	Port4 Control Registers	
0x20000–0x200A4	Port0 Statistics Counters	page 142
0x20100–0x201A4	Port1 Statistics Counters	
0x20200–0x202A4	Port2 Statistics Counters	
0x20300–0x203A4	Port3 Statistics Counters	
0x20400–0x204A4	Port4 Statistics Counters	

These registers are accessed by the CPU through the GE0 "MII Address" and "MII Control" registers. GE0 has a MDIO master, while the Ethernet Switch has a MDIO slave.

The MDC/MDIO interface allows users to access the switch internal registers and the MII registers. The format required to access the MII registers in the embedded PHY for a PHY_ADDR from 0x00 to 0x04 is:

start	OP	2'b0	Phy_Addr [2:0]	Reg_Addr [4:0]	TA [1:0]	Data [15:0]

The Op code "10" indicates the read command and "01" is the write command.

The switch internal registers are 32-bits wide, but the MDIO access is only 16-bits wide, so two access cycles are required to access all 32 bits of the internal registers. Moreover, address spacing is more than the 10 bits supported by MDIO, so the upper address bits must be written to internal registers, similar to the page mode access method.

For example, the register address bits [18:9] are treated as a page address and are written out first as High_Addr[9:0]:

start	OP	2'b11	8'b0	6'b0	High_Addr [9:0]

Then the register would be accessed via:

start	OP	2'b10	Low_Addr [7:0]	TA [1:0]	Data [15:0]

Where:

- Low_Addr[7:1] is the address bit [8:2] of the register AND Low_Addr[0] is 0 for Data[15:0]

or

- Low_Addr[0] is 1 for Data[31:16]

3.10.1 Global Control Registers

Table 3-13 summarizes the global control registers for the AR7240.

Table 3-13. **Global Control Registers Summary**

Offset	Register	Page
0x0000	Global Mask Control	page 121
0x0010	Global Interrupt	page 122
0x0014	Global Interrupt Mask	page 123
0x0020	Global MAC Address 0	page 124
0x0024	Global MAC Address 1	page 123
0x002C	Flood Mask	page 124
0x0030	Global Control	page 125
0x0040	VLAN Table Function 0	page 125
0x0044	VLAN Table Function 1	page 126
0x0050	Address Table Function 0	page 126
0x0054	Address Table Function 1	page 127
0x0058	Address Table Function 2	page 127
0x005C	Address Table Control	page 128
0x0060	IP Priority Mapping 0	page 128
0x0064	IP Priority Mapping 1	page 129
0x0068	IP Priority Mapping 2	page 129
0x006C	IP Priority Mapping 3	page 130
0x0070	Tag Priority Mapping	page 130
0x0074	Service Tag	page 131
0x0078	CPU Port	page 131
0x0080	MIB Function0	page 132
0x0098	MDIO Control	page 132

3.10.1.1Global Mask Control

Address: 0x0000
Access: Read/Write
Reset: See field description

This register is used for soft resets.

Bit	Bit Name	Type	Reset	Description
30:0	RES	RO	0x0	Reserved.
31	SOFT_RET	WO	0x0	Software reset. This bit is set by software to initialize the hardware, and should be self-cleared by hardware after the initialization is done.

3.10.1.2 Global Interrupt

Address: 0x0010
Access: Read/Write
Reset: 0x0

This register provides the status of various interrupts based global parameters. Interrupts are only generated when the corresponding bits of the following "Global Interrupt Mask" are set.

Bit	Bit Name	Description
1:0	RES	Reserved
2	PHY_INT	Generates an interrupt originating from the physical layer
3	MDIO_DONE_ INT	Generates an interrupt when the MDIO access switch register is done
4	ARL_DONE_ INT	This bit generates and interrupt when the address resolution table was accessed and the process has completed
5	ARL_FULL_INT	This bit generates an interrupt when there is an address attempting to be added to the address resolution table, yet the table is full
6	AT_INI_INT	Generates an interrupt when the address table initialization has completed
7	QM_INI_INT	Generates an interrupt after the QM memory initialization is completed
8	VT_DONE_INT	This bit generates an interrupt after completing an access to the VLAN table by the CPU
9	VT_MEM_VIO_INT	This bit generates an interrupt when a VID is located in the VLAN table, yet the source port is not a member of the VID
10	VT_MISS_VIO_ INT	This bit generates an interrupt when a VID is not located in the VLAN table
11	RES	Reserved
12	MIB_DONE_ INT	This bit generates an interrupt when the CPU has completed accessing the MIB
13	MIB_INI_INT	This bit generates an interrupt when the MIB memory initialization has completed
14	HARDWARE_ INI_DONE	This bit generates an interrupt when the hardware memory initialization has completed
15	RES	Reserved. Must be written with zero. Contains zeros when read.
16	QM_ERR_INT	This bit generates an interrupt when the QM detects an error
17	LOOKUP_ERR_INT	Generates an interrupt when there is an error detected during a lookup
31:18	RES	Reserved. Must be written with zero. Contains zeros when read.

3.10.1.3 Global Interrupt Mask

Address: 0x0014
Access: Read/Write
Reset: See field description

This register controls various interrupts based global parameters. Interrupts are only generated when the bits of this register are set.

Bit	Bit Name	Reset	Description
1:0	RES	0x0	Reserved
2	PHY_INT_EN	0x0	Enables an interrupt originating from the physical layer
3	MDIO_DONE_ INT_EN	0x0	Enables an interrupt when the MDIO access switch register is done
4	ARL_DONE_ INT_EN	0x0	Enables interrupt when the address resolution table was accessed and the process has completed
5	ARL_FULL_INT_EN	0x0	Enables an interrupt when there is an address attempting to be added to the address resolution table, yet the table is full
6	AT_INI_INT_ EN	0x0	Enables an interrupt when the address table initialization has completed
7	QM_INI_INT_ EN	0x0	Enables an interrupt after the QM memory initialization has been completed
8	VT_DONE_INT_EN	0x0	Enables an interrupt after completing an access to the VLAN table by the CPU
9	VT_MEM_VIO_INT_ EN	0x0	Enables an interrupt when a VID is located in the VLAN table, yet the source port is not a member of the VID
10	VT_MISS_VIO_ INT_EN	0x0	Enables an interrupt when a VID is not located in the VLAN table
11	RES	0x0	Reserved
12	MIB_DONE_ INT_EN	0x0	Enables an interrupt when the CPU is finished accessing the MIB
13	MIB_INI_INT_ EN	0x0	Enables an interrupt when the MIB memory initialization has completed
14	HARDWARE_ INI_DONE_EN	0x0	Enables an interrupt when the hardware memory initialization has completed
15	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
16	QM_ERR_INT_EN	0x0	Enables an interrupt when the QM detects an error
17	LOOKUP_ERR_INT_ EN	0x0	Enables an interrupt when there is an error detected during a lookup
31:18	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.10.1.4 Global MAC Address 1

Address: 0x0020
Access: Read/Write
Reset: See field description

This register, along with the preceding "Global MAC Address 2", are used to identify the station address of the switch.

Bit	Bit Name	Reset	Description
7:0	MAC_ADDR_ BYTE5	0x01	These bits represent the station address of the switch which is used as a source address in pause frames or other management frames
15:8	MAC_ADDR_ BYTE4	0x0	
31:16	RES	0x0	Reserved

3.10.1.5 Global MAC Address 2

Address: 0x0024
Access: Read/Write
Reset: 0x0

This register, along with the following "Global MAC Address 1", are used to identify the station address of the switch.

Bit	Bit Name	Description
7:0	MAC_ADDR_ BYTE3	These bits represent the station address of the switch, which is used as a source address in pause frames or other management frames
15:8	MAC_ADDR_ BYTE2	
23:16	MAC_ADDR_ BYTE1	
31:24	MAC_ADDR_ BYTE0	

3.10.1.6 Flood Mask

Address: 0x002C
Access: Read/Write
Reset: See field description

This register is used to allocate broadcast, multicast and unicast frames.

Bit	Bit Name	Reset		Description
5:0	UNI_FLOOD_ DP	0x3F		These bits are used to find a destination port for a unknown unicast frame received by the MAC, within which the destination address is not contained in the address resolution table (ARL)
15:6	RES	0x0		Reserved. Must be written with zero. Contains zeros when read.
21:16	MULTI_FLOOD _DP	0x3F		These bits are used to find a destination port for a unknown multicast frame received by the MAC, within which the destination address is not contained in the address resolution table (ARL)
23:22	RES	0x0		Reserved. Must be written with zero. Contains zeros when read.
24	ARL_UNI_ LEAKY_EN	0x0	0	Ignores the LEAKY_EN bit in the ARL table to control unicast frame leaky VLAN. Uses only port-base UNI_LEAKY_EN to control the unicast frame leaky VLAN.
			1	Uses the LEAKY_EN bit in the ARL table to control unicast frame leaky VLANs and ignore the UNI_LEAKY_EN
25	ARL_MULTI_ LEAKY_EN	0x0	0	Ignores the LEAKY_EN bit in the ARL table to control multicast frame leaky VLANs. Uses only port-base MULTI_LEAKY_EN to control the frame leaky VLAN.
			1	Uses the LEAKY_EN bit in the ARL table to control multicast frame leaky VLANs and ignore the MULTI_LEAKY_EN
26	BROAD_TO_ CPU_EN	0x0	0	Broadcast frames cannot be transmitted to the CPU port
			1	Broadcast frames can be transmitted to the CPU port
31:27	RES	0x0		Reserved. Must be written with zero. Contains zeros when read.

3.10.1.7 Global Control

Address: 0x0030
Access: Read/Write
Reset: See field description

Bit	Bit Name	Reset	Description	
13:0	MAX_FRAME_SIZE	0x5EE	Max frame size can be received and transmitted by the MAC. The MAC drops any packet sized larger than MAX_FRAME_SIZE. The value is for normal packets; the MAC adds 4 if it supports VLAN, it adds 8 for double VLAN, and adds 2 for some headers.	
26:14	RES	0x0	Reserved	
27:24	RES	0xF	Reserved	
28	MIX_WEIGHT_PRIORITY	0x0	0	Use the 8, 4, 2, 1 weighted fair queueing scheme when the WEIGHT_PRIORITY bit is set to 1
			1	Strict priority and weight priority mix mode. The highest priority uses strict priority, other priorities use a 4, 2, 1 weighted fair queueing scheme when the WEIGHT_PRIORITY bit is set as 1.
30:29	RES	0x3	Reserved	
31	WEIGHT_PRIORITY	0x0	0	Use strict priority for egress
			1	If MIX_WEIGHT_PRIORITY = 0, use an 8, 4, 2, 1 weighted fair queueing scheme, otherwise use mix mode

3.10.1.8 VLAN Table Function 0

Address: 0x0040
Access: Read/Write
Reset: 0x0

This register is used to set the various functions of the VLAN table, such as priority and ports.

Bit	Bit Name	Description	
2:0	VT_FUNC	The VLAN table operating functions	
		000	No operation
		001	Flush all entries in the VLAN table
		010	The CPU wants to load an entry into other VLAN table
		011	Used to purge an entry from the VLAN table
		100	Used to identify a port to be removed from the VLAN table. This port is indicated in the VT_PORT_NUM bit
		101	Used to get the next entry in the VLAN table
		If the VID is 0 and VT_BUSY is set by the software, the hardware should search for the first valid entry in the VLAN table. If the VID is 0 and the VT_BUSY is reset by the hardware, there is no valid entry from the VID set by the software.	
3	VT_BUSY	The VLAN table is busy. This bit must be set to 1 to start a VLAN table operation and cleared to zero after the operation has completed. If this bit is set to 1, the CPU cannot request another operation.	
4	VT_FULL_VIO	This bit is set when there is a violation of the VLAN table. Set to 1 if the VLAN table is full when the CPU wishes to add a new VID to the VLAN table	
7:5	RES	Reserved.	
11:8	VT_PORT_NUM	The port number in the VLAN table	
15:12	RES	Reserved. Must be written with zero. Contains zeros when read.	
27:16	VID	Represents the value of the VLAN ID (VID) to be added or purged	
30:28	VT_PRI	Represents the priority of a VLAN in the VLAN table. VTU [2:0]	
31	VT_PRI_EN	Represents the priority of a VLAN in the VLAN table. VTU [3]	

3.10.1.9 VLAN Table Function 1

Address: 0x0044
Access: Read/Write
Reset: 0x0

This register is used to identify VLAN entries in the VID table.

Bit	Bit Name	Type	Reset	Description
9:0	VID_MEM	RW	0x0	Represents a VID member in the VLAN table. VTU [25:16]
10	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.
11	VT_VALID	RW	0x0	Represents a valid entry in the VLAN table. VTU [15]
31:12	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.10.1.10 Address Table Function 0

Address: 0x0050
Access: Read/Write
Reset: 0x0

This register is used to configure functions of the address resolution (ARL) table.

Bit	Bit Name	Description	
2:0	AT_FUNC	The address table operation functions	
		000	No operation
		001	Flush all entries
		010	Used to load an entry. If these bits are set, the CPU wishes to load an entry into the ARL table
		011	If these bits are set, used by the CPU to purge an entry from the ARL table
		100	Flushes all unlocked entries from the ARL
		101	Flushes the entries of one port from the Address table
		110	Used to get the next valid or static entry in the ARL table
		111	Setting these bits enables a MAC address to be searched
		If the address and the AT_STATUS are both zero, the hardware will search the first valid entry from entry0. If the address is set to zero and the AT_STATUS is not zero, the hardware will discover the next valid entry which has an address of 0x0. If the hardware returns an address and the AT_STATUS is zero, there is no next valid entry in the address table.	
3	AT_BUSY	The address table is busy. Setting this bit to 1 starts an ARL operation and it must be cleared to zero after the operation is complete. If set to 1, the CPU cannot request another operation	
4	FLUSH_STATIC_EN	0	When the AT_FUNC is set to 101, only dynamic entries in the ARL table will be flushed
		1	When the AT_FUNC is set to 101, static entries in the ARL table can be flushed
7:5	RES	Reserved. Must be written with zero. Contains zeros when read.	
11:8	AT_PORT_NUM	The port number to be flushed. If the AT_FUNC is set to 101, the lookup module must flush all unicast entries for the port	
12	AT_FULL_VIO	ARL table full violation. This bit is set to 1 if the ARL table is full when the CPU wishes to add a new entry into the ARL table, and if the ARL table is empty when the CPU wants to purge an entry from the ARL table.	
15:13	RES	Reserved. Must be written with zero. Contains zeros when read.	
23:16	AT_ADDR_BYTES5	The last byte of the address	
31:24	AT_ADDR_BYTES4	The fifth byte of the address	

3.10.1.11 Address Table Function 1

Address: 0x0054
Access: Read/Write
Reset: 0x0

This register holds the address of the ARL table, along with bits [23:16] and [31:24] of the preceding "Address Table Function 0".

Bit	Bit Name	Description
7:0	AT_ADDR_ BYTE3	The fourth byte of the address
15:8	AT_ADDR_ BYTE2	The third byte of the address
23:16	AT_ADDR_ BYTE1	The second byte of the address
31:24	AT_ADDR_ BYTE0	The first byte of the address to operate. This byte is the highest byte of the MAC address for the most significant bit (MSB).

3.10.1.12 Address Table Function 2

Address: 0x0058
Access: Read/Write
Reset: 0x0

This register is used to set parameters for the address resolution table (ARL) such as destination and source address.

Bit	Bit Name	Description
5:0	DES_PORT	The destination port bits for address ATU [53:48]
9:6	RES	Reserved. Must be written with zero. Contains zeros when read.
11:10	AT_PRIORITY	The destination address (DA) priority. ATU [59:58]
12	AT_PRIORITY_EN	Setting this bit to 1 enables the use of a DA priority. ATU [60]
13	MIRROR_EN	Setting this bit to 1 enables the copying of the DA frame to the mirror port. ATU [61]
14	SA_DROP_EN	Source address (SA) drop enable. ATU [62]
15	RES	Reserved. Must be written with zero. Contains zeros when read.
19:16	AT_STATUS	The destination address status. Associated with the "status" bits in the Address Table ATU [67:64]
23:20	RES	Reserved. Must be written with zero. Contains zeros when read.
24	LEAKY_EN	Used to enable the leaky VLAN. ATU [68]
25	REDIRECT_TOCPU	ATU [69]
26	COPY_TO_CPU	ATU [7:0]
31:27	RES	Reserved. Must be written with zero. Contains zeros when read.

3.10.1.13 Address Table Control

Address: 0x005C
Access: Read/Write
Reset: See field description

This register is used to set the parameters of the Address Table Control, including address age out time and MAC address changes.

Bit	Bit Name	Reset	Description	
15:0	AGE_TIME	0x2B	The address table age timer. This determines the time that each entry remains valid in the address table, since it was last accessed. The maximum age time is about 10,000 minutes. The default value of 0x2B is for 5 minutes. If the AGE_EN is set to 1, these bits should not be set to 0.	
16	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
17	AGE_EN	0x1	Enables the age operation. Setting this bit to 1 allows the lookup module that can age the address in the address table.	
18	LEARN_ CHANGE_EN	0x0	MAC address change	
			0	If a hash violation occurs during learning, no new address will be learned in the ARL
			1	Enables a new MAC address change if a hash violation occurs during learning
19	RES	0x1	Reserved.	
20	ARP_EN	0x0	ARP frame acknowledge enable. Setting this bit to 1 is an acknowledgement by the hardware of a received ARP frame and allows it to be copied to the CPU port.	
31:21	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	

3.10.1.14 IP Priority Mapping 0

Address: 0x0x0060
Access: Read/Write
Reset: See field description

This register is used to configure the priority mapping value of IPv4 ToS or IPv6 TC field. Bit [7] to bit [2] are used to map queue priority, but bit [1] and bit [0] are ignored. If ToS [7:2] or TC [7:2] is equal to 0x3C, the queue priority should be mapped to the value of these bits.

Bit	Bit Name	Reset	Description
1:0	IP_MAP	0x0	IP_0x00
3:2	IP_MAP	0x0	IP_0x04
5:4	IP_MAP	0x0	IP_0x08
7:6	IP_MAP	0x0	IP_0x0C
9:8	IP_MAP	0x0	IP_0x10
11:10	IP_MAP	0x0	IP_0x14
13:12	IP_MAP	0x0	IP_0x18
15:14	IP_MAP	0x0	IP_0x1C
17:16	IP_MAP	0x0	IP_0x20
19:18	IP_MAP	0x0	IP_0x24
21:20	IP_MAP	0x0	IP_0x28
23:22	IP_MAP	0x0	IP_0x2C
25:24	IP_MAP	0x0	IP_0x30
27:26	IP_MAP	0x0	IP_0x34
29:28	IP_MAP	0x0	IP_0x38
31:30	IP_MAP	0x0	IP_0x3C

3.10.1.15 IP Priority Mapping 1

Address: 0x0x0064
Access: Read/Write
Reset: See field description

This register is used to configure the priority mapping value of IPv4 ToS or IPv6 TC field. Bit [7] to bit [2] are used to map queue priority, but bit [1] and bit [0] are ignored. If ToS [7:2] or TC [7:2] is equal to 0x3C, the queue priority should be mapped to the value of these bits.

Bit	Bit Name	Reset	Description
1:0	IP_MAP	0x1	IP_0x40
3:2	IP_MAP	0x1	IP_0x44
5:4	IP_MAP	0x1	IP_0x48
7:6	IP_MAP	0x1	IP_0x4C
9:8	IP_MAP	0x1	IP_0x50
11:10	IP_MAP	0x1	IP_0x54
13:12	IP_MAP	0x1	IP_0x58
15:14	IP_MAP	0x1	IP_0x5C
17:16	IP_MAP	0x1	IP_0x60
19:18	IP_MAP	0x1	IP_0x64
21:20	IP_MAP	0x1	IP_0x68
23:22	IP_MAP	0x1	IP_0x6C
25:24	IP_MAP	0x1	IP_0x70
27:26	IP_MAP	0x1	IP_0x74
29:28	IP_MAP	0x1	IP_0x78
31:30	IP_MAP	0x1	IP_0x7C

3.10.1.16 IP Priority Mapping 2

Address: 0x0x0068
Access: Read/Write
Reset: See field description

This register is used to configure the priority mapping value of IPv4 ToS or IPv6 TC field. Bit [7] to bit [2] are used to map queue priority, but bit [1] and bit [0] are ignored. If ToS [7:2] or TC [7:2] is equal to 0x3C, the queue priority should be mapped to the value of these bits.

Bit	Bit Name	Reset	Description
1:0	IP_MAP	0x2	IP_0x80
3:2	IP_MAP	0x2	IP_0x84
5:4	IP_MAP	0x2	IP_0x88
7:6	IP_MAP	0x2	IP_0x8C
9:8	IP_MAP	0x2	IP_0x90
11:10	IP_MAP	0x2	IP_0x94
13:12	IP_MAP	0x2	IP_0x98
15:14	IP_MAP	0x2	IP_0x9C
17:16	IP_MAP	0x2	IP_0xA0
19:18	IP_MAP	0x2	IP_0xA4
21:20	IP_MAP	0x2	IP_0xA8
23:22	IP_MAP	0x2	IP_0xAC
25:24	IP_MAP	0x2	IP_0xB0
27:26	IP_MAP	0x2	IP_0xB4
29:28	IP_MAP	0x2	IP_0xB8
31:30	IP_MAP	0x2	IP_0xBC

3.10.1.17 IP Priority Mapping 3

Address: 0x0x006C
Access: Read/Write
Reset: See field description

This register is used to configure the priority mapping value of IPv4 ToS or IPv6 TC field. Bit [7] to bit [2] are used to map queue priority, but bit [1] and bit [0] are ignored. If ToS [7:2] or TC [7:2] is equal to 0x3C, the queue priority should be mapped to the value of these bits.

Bit	Bit Name	Reset	Description
1:0	IP_MAP	0x3	IP_0xC0
3:2	IP_MAP	0x3	IP_0xC4
5:4	IP_MAP	0x3	IP_0xC8
7:6	IP_MAP	0x3	IP_0xCC
9:8	IP_MAP	0x3	IP_0xD0
11:10	IP_MAP	0x3	IP_0xD4
13:12	IP_MAP	0x3	IP_0xD8
15:14	IP_MAP	0x3	IP_0xDC
17:16	IP_MAP	0x3	IP_0xE0
19:18	IP_MAP	0x3	IP_0xE4
21:20	IP_MAP	0x3	IP_0xE8
23:22	IP_MAP	0x3	IP_0xEC
25:24	IP_MAP	0x3	IP_0xF0
27:26	IP_MAP	0x3	IP_0xF4
29:28	IP_MAP	0x3	IP_0xF8
31:30	IP_MAP	0x3	IP_0xFC

3.10.1.18 Tag Priority Mapping

Address: 0x0070
Access: Read/Write
Reset: See field description

This register is used to map the priority value of TAG. If the pri [2:0] in the tag is equal to 0x07, the queue priority should be mapped to the value of these bits.

Bit	Bit Name	Reset	Description
1:0	TAG0	0x1	The priority mapping value of TAG. TAG_0x00
3:2	TAG1	0x0	The priority mapping value of TAG. TAG_0x01
5:4	TAG2	0x0	The priority mapping value of TAG. TAG_0x02
7:6	TAG3	0x1	The priority mapping value of TAG. TAG_0x03
9:8	TAG4	0x2	The priority mapping value of TAG. TAG_0x04
11:10	TAG5	0x2	The priority mapping value of TAG. TAG_0x05
13:12	TAG6	0x3	The priority mapping value of TAG. TAG_0x06
15:14	TAG7	0x3	The priority mapping value of TAG. TAG_0x07
31:16	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.10.1.19 Service Tag

Address: 0x0074
Access: Read/Write
Reset: 0x0

This register is used to double tag egress packets and recognize double tagged packets at ingress.

Bit	Bit Name	Description
15:0	SERVICE_TAG	The service tag. These bits are used to recognize the double tag at ingress and insert the double tag at egress.
31:16	RES	Reserved. Must be written with zero. Contains zeros when read.

3.10.1.20 CPU Port

Address: 0x0078
Access: Read/Write
Reset: See field description

This register is used to identify CPU connected ports and mirror ports.

Bit	Bit Name	Reset	Description	
3:0	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
7:4	MIRROR_PORT_NUM	0xF	Represents the port number to which packets are to be mirrored. 0x0 is port0, 0x1 is port1 and so on. If this value is more than 5, no mirror port is connected to the switch.	
8	CPU_PORT_EN	0x0	This bit is used to identify ports that are CPU enabled	
			0	No CPU is connected to the switch
			1	CPU is connected to port0
31:9	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	

3.10.1.21 MIB Function0

Address: 0x0080
Access: Read/Write
Reset: 0x0

This register is used to set the MIB functions such as the auto-cast timer and MIB functions.

Bit	Bit Name	Description	
15:0	MIB_TIMER	The MIB auto-cast timer. If set to 0, the MIB will not auto-cast because the timer timed out. This timer is set in periods of 8.4 ms. The recommended value is 0x100. (8.4 ms x 4)	
16	MIB_AT _HALFEN	The MIB auto-cast is enabled due to half flow. If set to one, the MIB will be auto-cast when the highest bit count for any counter is set as 1.	
17	MIB_BUSY	The MIB module status	
		0	The MIB module is currently empty and can access a new command
		1	The MIB module is busy and cannot access a new command
23:18	RES	Reserved. Must be written with zero. Contains zeros when read.	
26:24	MIB_FUNC	The current MIB function	
		000	No Operation
		001	Flush all counters on all ports
		010	Reserved
		011	Capture all counters for all ports and auto-cast to the CPU port
		1xx	Reserved
31:27	RES	Reserved. Must be written with zero. Contains zeros when read.	

3.10.1.22 MDIO Control

Address: 0x0098
Access: Read/Write
Reset: 0x0

This register is used to control the functions of the MDIO interface.

Bit	Bit Name	Description	
15:0	MDIO_DATA	When write, these bits are data written to the PHY register. When read, these bits are read out from the PHY register	
20:16	REG_ADDR	These bits represent the PHY register address	
25:21	PHY_ADDR	These bits represent the PHY address	
26	MDIO_SUP_ PRE	Writing a 1 to this bit enables the supposed preamble	
27	MDIO_CMD	This bit represents the commands given for the MDIO	
		0	Write
		1	Read
29:28	RES	Reserved. Must be written with zero. Contains zeros when read.	
30	MDIO_ MASTER_EN	Writing a 1 to this bit enables the MDIO master which is used to configure the PHY register. MDC should change to the internal MDC to PHY	
31	MDIO_BUSY	Writing a one to this bit represents the internal MDIO interface as busy. This bit should be set when the CPU reads or writes to the PHY register through the internal MDIO interface, and should be cleared after the hardware finishes this command	

3.10.2 Port Control Registers

Table 3-23 summarizes the port control registers for the AR7240.

NOTE: Table 3-23 shows the offset address for Port0. Port0 through Port4 use these offsets:

Port0	0x100
Port1	0x200
Port2	0x300
Port3	0x400
Port4	0x500

Table 3-23. **MAC Control Registers Summary**

Offset[1]	Register	Page
0x0100	Port Status	page 134
0x0104	Port Control	page 134
0x0108	Port Base VLAN	page 136
0x010C	Rate Limit 0	page 137
0x0110	Priority Control	page 137
0x0114	Storm Control	page 138
0x0118	Queue Control	page 139
0x011C	Rate Limit 1	page 141
0x0120	Rate Limit 2	page 141

[1]See Table 3-23.

3.10.2.1Port Status

Address: 0x0100 (See Table 3-23)
Access: See field description
Reset: 0x0

This register denotes the settings for the port including flow control and speed.

Bit	Bit Name	Type	Description	
1:0	SPEED	RW	The speed mode	
			00	10 Mbps
			01	100 Mbps
			10	Reserved
			11	Speed mode error
2	TXMAC_EN	RW	Enables the Tx MAC	
3	RXMAC_EN	RW	Enables the Rx MAC	
4	TX_FLOW_EN	RW	Tx MAC flow control enable	
5	RX_FLOW_EN	RW	Rx MAC flow control enable	
6	DUPLEX_MODE	RW	The duplex mode	
			0	Half-duplex mode
			1	Full-duplex mode
7	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	
8	LINK	RO	The current link status	
			0	PHY link down
			1	PHY link up
9	LINK_EN	RW	This bit is used to enable the PHY link mode	
			0	Allows the MAC to be configured by the software
			1	Enables the use of the PHY link status to configure the MAC
10	LINK_PAUSE_ EN	RO	The link partner support flow control	
11	LINK_ASYN_PAUSE_EN	RO	The link partner supports ASYN flow control	
31:12	RES	RO	Reserved. Must be written with zero. Contains zeros when read.	

3.10.2.2 Port Control

Address: 0x0104 (See Table 3-23)
Access: Read/Write
Reset: See field description

This register is used to configure port functions such as port mirroring and spanning tree.

Bit	Bit Name	Reset	Description	
2:0	PORT_STATE	0x4	Port state. These bits manage the port to determine what kind of frames may enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree.	
			000	Disabled mode. This port cannot send or receive frames.
			001	Blocking mode. The port forwards received management frames to the designed port only. Other frames are not transmitted or received and do not learn source addresses.
			010	Listening mode. The port receives and transmits only management frames without learning the source address. Other frames are not transmitted or received.
			011	Learning mode. The port learns all source addresses and discards all frames except management frames, and management frames can only be transmitted.
			100	Forwarding mode. The port will learn all source addresses and transmit and receive frames normally.

4:3	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
5	LOCK_DROP _ EN	0x0	0	If the source address is not in the ARL table or the port member is not the source port, the packet should be re4directed to the CPU when the PORT_LOCK_EN bit is set to 1.
			1	If the source address is not in the ARL table or if it is there but the port member is not the source port, the packet should be dropped when the PORT_LOCK_EN bit is set to 1.
6	PORT_LOCK_ EN	0x0	When this bit is set to 1, the port lock is enabled. All packets received with the source address not found in the ARL table, or the source address resides in the ARL table but the port member is not the source address, should be redirected to the CPU or dropped, which is controlled by the LOCK_DROP_EN bit.	
7	LEARN_ONE _ LOCK	0x0	0	Normal learning mode
			1	This port should not learn source addresses except from the first packet which will be locked in as a static address
9:8	EG_VLAN_ MODE	0x0	Egress VLAN mode based on the following	
			00	Egress should transmit frames unmodified
			01	Egress should transmit without VLAN
			10	Egress should transmit frames with VLAN
			11	Double tagged. The MAC should add one tag after the source address. This tag will be set in the SERVICE_TAG register
10	IGMP_MLD _EN	0x0	Enables IGMP/MLD Snooping. Setting this bit to one allows the port to examine all received frames and copy or redirect them to the CPU port, based on the IGMP_COPY_EN bit setting.	
11	RES	0x0	Reserved.	
12	MAC_LOOP_ BACK	0x0	Setting this bit to 1 enables the MAC Loop back function on the MII interface	
13	SINGLE _VLAN_EN	0x0	Setting this bit allows the MAC to transmit and receive packets with the single VLAN enabled	
14	LEARN_EN	0x1	Used to enable the learning operation. Setting this bit to 1 will allow the lookup module to learn new addresses to the address table	
15	DOUBLE _TAG_VLAN	0x0	Setting this bit to 1 will enable the double tag where the MAC will check received frames for the service tag and if found, remove it.	
16	EG_MIRROR_ EN	0x0	Setting this bit to 1 enables egress port mirroring where all packets sent out through this port will be copied to a mirror port	
17	ING_MIRROR _EN	0x0	Setting this bit to 1 will enable ingress port mirroring where all packets received on this port will be copied to a mirror port	
31:18	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	

3.10.2.3 Port Base VLAN

Address: 0x0108 (See Table 3-23)
Access: Read/Write
Reset: 0x0

This register is used to configure the bits for the VLANs, including port VIDs and Leaky VLANs.

Bit	Bit Name	Description	
11:0	PORT_VID	The port default VID. Untagged frames transmitted from this port will have the default VID tagged to them	
12	FORCE_ DEFALUT_VID_ EN	0	Received frames will use only the tag set with the received frames for port default VID and priority
		1	When 802.1Q is enabled, the received frames must use the port default VID and priority issued to them by the switch
13	MULTI_LEAKY_ EN	Used to enable Multicast frames for the leaky VLAN. If the MAC receives multicast frames on this port, it should forward them as leaky VLAN frames. These frames may be switched to the destination port defined in the ARL table and then across all VLANs (including port-based and 802.1Q). Users may enable the ARL_MULTI_LEAKY_EN bit and the LEAKY_EN bit the ARL table to control unicast frames for the leaky VLAN. When the ARL_MULTI_LEAKY_EN is set to 0, only the MULTI_LEAKY_EN controls multicast frames for the leaky VLAN. If the ARL_UNI_LEAKY_VLAN bit is set to 1, only frames with the destination address in the ARL table and their LEAKY_EN bit is set to 1 can be forwarded as leaky VLAN frames. This will force the UNI_LEAKY_EN bit to be ignored.	
14	UNI_LEAKY_EN	Used to enable Unicast frames for the leaky VLAN. If the MAC receives unicast frames on this port, it should forward them as leaky VLAN frames. These frames may be switched to the destination port defined in the ARL table and then across all VLANs (including port-based and 802.1Q). Users may enable the ARL_MULTI_LEAKY_EN bit and the LEAKY_EN bit the ARL table to control unicast frames for the leaky VLAN. When the ARL_MULTI_LEAKY_EN is set to 0, only the MULTI_LEAKY_EN controls multicast frames for the leaky VLAN. If the ARL_MULTI_LEAKY_VLAN bit is set to 1, only frames with the destination address in the ARL table and their LEAKY_EN bit is set to 1, can be forwarded as leaky VLAN frames. This will force the MULTI_LEAKY_EN bit to be ignored.	
15	ARP_LEAKY_EN	Setting this bit to 1 allows received frames from this port on the MAC to cross all VLANs (both port-based and 802.1Q)	
25:16	PORT_VID_ MEMBER	Port Base VLAN Member. Each bit restricts which port can send frames to port 0, bit 16 must be set to 1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they are received on.	
26	FORCE_PORT_ VLAN_EN	Setting this bit forces port-based VLANs to be enabled. This uses the port base VLAN and the VLAN table to determine the destination port.	
29:27	ING_PORT_PRI	The port default priority for received frames.	
31:30	8021Q_MODE	Sets the 802.1Q mode for this port	
		00	Disables the 802.1Q VLAN function. Port-based VLAN used only.
		01	Enables 802.1Q for all received frames. If the VID for the received frame is not contained in the VLAN table, port VLANs will be used and ingress membership will not be discarded.
		10	Enables 802.1Q for all received frames. Frames will be discarded only if the VID of the frames are not contained in the VLAN table. Ingress membership will not be discarded.
		11	Enables 802.1Q for all received frames. Frames will be discarded if the VID of the frames are not contained in the VLAN table and ingress membership will be discarded.

3.10.2.4 Rate Limit

Address: 0x0010C (See Table 3-23)
Access: Read/Write
Reset: See field description

This register is used to set rate limits various frame types.

Bit	Bit Name	Reset	Description
14:0	ING_RATE	0x7FFF	The Ingress Rate Limit for all priorities. This rate is limited to multiples of 32kbps. The default of 0x7FFF disables the rate limit for ingress traffic. When these bits are set to 0x0, no frames should be received on the port.
19:15	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
20	INGRESS_MULTI_RATE_EN	0x0	Enables multicast frames to be included in the calculations for the ingress rate limit, if the destination address of those multicast frames is found in the ARL table
21	INGRESS_MANAGE_RATE_EN	0x0	Enables management frames to be included in the calculations for the ingress rate limit
22	EGRESS_MANAGE_RATE_EN	0x0	Enables management frames to be included in the calculations for the egress rate limit
23	EGRESS_RATE_EN	0x0	Enables the port base rate limit. The rate should be set using the EG_PRI3_RATE
31:24	ADD_RATE_BYTE	0x18	The byte number should be added to the frame when calculating the rate limit. The default is 24 bytes for IPG, preamble SFD and CRC.

3.10.2.5 Priority Control

Address: 0x0110 (See Table 3-23)
Access: Read/Write
Reset: See field description

This register is used to set the priority for QoS based on priorities set for other functions like ToS and IP.

Bit	Bit Name	Reset	Description
1:0	PORT_PRI_SEL	0x3	Port-based priority selected level for QoS
3:2	IP_PRI_SEL	0x2	IP priority selected level for QoS
5:4	VLAN_PRI_SEL	0x1	VLAN priority selected level for QoS
7:6	DA_PRI_SEL	0x0	The DA priority selected level for QoS, which has five levels. The highest priority is the one found in the packet header. The other four are selected by these bits. If these bits are set to 0, the destination address priority is selected after the header. If set to n, the destination address priority is selected after the priority is set to n-1.
15:8	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
16	IP_PRI_EN	0x0	Setting this bit to 1 allows the ToS/TC to be used for QoS
17	VLAN_PRI_EN	0x0	Setting this bit to 1 allows the VLAN priority to be used for QoS
18	DA_PRI_EN	0x0	Setting this bit to 1 allows the destination address priority to be used for QoS
19	PORT_PRI_EN	0x1	Setting this bit to 1 allows the port-based priority to be used for QoS
31:20	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.10.2.6 Storm Control

Address: 0x0x0114 (See Table 3-23)
Access: Read/Write
Reset: 0x0

This register sets the rate for the storm control based on incoming broadcast, unicast and multicast frames.

Bit	Bit Name	Type	Reset	Description	
3:0	STORM_RATE	RW	0x0	The storm control rate	
				0x0	Disables storm control
				0x1	Rate set at 1K frames per second
				0x2	Rate set at 2K frames per second
				0x3	Rate set at 4K frames per second
				0x4	Rate set at 8K frames per second
				0x5	Rate set at 16K frames per second
				0x6	Rate set at 32K frames per second
				0x7	Rate set at 64K frames per second
				0x8	Rate set at 128K frames per second
				0x9	Rate set at 256K frames per second
				0xA	Rate set at 512K frames per second
				0xB	Rate set at 1M frames per second
7:4	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	
8	BROAD_STORM_EN	RW	0x0	Setting this bit to 1 enables broadcast frames to be included in the calculations for storm control	
9	UNI_STORM_EN	RW	0x0	Setting this bit to 1 enables unknown unicast frames to be included in the calculations for storm control	
10	MULTI_STORM_EN	RW	0x0	Setting this bit to 1 enables unknown multicast frames to be included in the calculations for storm control	
31:11	RES	RO	0x0	Reserved. Must be written with zero. Contains zeros when read.	

3.10.2.7 Queue Control

Address: 0x0x0118 (See Table 3-23)
Access: Read/Write
Reset: See field description

This register is used to set the buffer controls for QoS queues.

Bit	Bit Name	Reset	Description	
3:0	PRI0_QUEUE_ NUM	0x0	This field sets the limit of the buffer size for QoS priority queue 0. Each bit represents a block of memory x 4, where each block represents 256 bytes. Therefore the maximum amount of memory that this bit can hold in the queue is 1024 bytes. (4x 256 = 1024)	
			0x0	No memory for the queue
			0x1	A maximum of 4 blocks (1024 bytes)
			0x2	A maximum of 8 blocks (2048 bytes)
			0x3	A maximum of 12 blocks (3072 bytes)
			...	...
			0xF	A maximum of 60 blocks (15360 bytes)
			Each successive hex value holds the same formula until 0xF which will be a maximum of 60 blocks (15360 bytes)	
7:4	PRI1_QUEUE_ NUM	0x0	This field sets the limit of the buffer size for QoS priority queue 1. Each bit represents a block of memory x 4, where each block represents 256 bytes. Therefore the maximum amount of memory that this bit can hold in the queue is 1024 bytes. (4x 256 = 1024)	
			0x0	No memory for the queue
			0x1	A maximum of 4 blocks (1024 bytes)
			0x2	A maximum of 8 blocks (2048 bytes)
			0x3	A maximum of 12 blocks (3072 bytes)
			...	...
			0xF	A maximum of 60 blocks (15360 bytes)
			Each successive hex value holds the same formula until 0xF which will be a maximum of 60 blocks (15360 bytes)	
11:8	PRI2_QUEUE_ NUM	0x0	This field sets the limit of the buffer size for QoS priority queue 2. Each bit represents a block of memory x 4, where each block represents 256 bytes. Therefore the maximum amount of memory that this bit can hold in the queue is 1024 bytes. (4x 256 = 1024)	
			0x0	No memory for the queue
			0x1	A maximum of 4 blocks (1024 bytes)
			0x2	A maximum of 8 blocks (2048 bytes)
			0x3	A maximum of 12 blocks (3072 bytes)
			...	...
			0xF	A maximum of 60 blocks (15360 bytes)
			Each successive hex value holds the same formula until 0xF which will be a maximum of 60 blocks (15360 bytes)	

15:12	PRI3_QUEUE_ NUM	0x0	This field sets the limit of the buffer size for QoS priority queue 3. Each bit represents a block of memory x 4, where each block represents 256 bytes. Therefore the maximum amount of memory that this bit can hold in the queue is 1024 bytes. (4x 256 = 1024)	
			0x0	No memory for the queue
			0x1	A maximum of 4 blocks (1024 bytes)
			0x2	A maximum of 8 blocks (2048 bytes)
			0x3	A maximum of 12 blocks (3072 bytes)
			...	...
			0xF	A maximum of 60 blocks (15360 bytes)
			Each successive hex value holds the same formula until 0xF which will be a maximum of 60 blocks (15360 bytes)	
20:16	PRI_QUEUE_ NUM	0x10	This field sets the limit of the buffer size for QoS priority queue. Each bit represents a block of memory x 4, where each block represents 256 bytes. Therefore the maximum amount of memory that this bit can hold in the queue is 1024 bytes. (4x 256 = 1024)	
			0x0	No memory for the queue
			0x1	A maximum of 4 blocks (1024 bytes)
			0x2	A maximum of 8 blocks (2048 bytes)
			0x3	A maximum of 12 blocks (3072 bytes)
			...	...
			0x1F	A maximum of 120 blocks (30720 bytes)
			Each successive hex value holds the same formula until 0x1F which will be a maximum of 120 blocks (30720 bytes)	
23:21	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	
24	PRI_QUEUE_ CTRL_EN	0x0	Setting this bit to 1 enables the memory depth control for this port based on priority	
25	PORT_QUEUE _CTRL_EN	0x1	Setting this bit to 1 enables the specified port to use the memory depth control feature	
31:26	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.	

3.10.2.8 Rate Limit Register 1

Address: 0x011C (See Table 3-23)
Access: Read/Write
Reset: See field description

This register is used to set the rate limits for priority queues.

Bit	Bit Name	Reset	Description
14:0	EG_PRI0_RATE	0x7FFF	The egress rate limit for priority 0. The rate limit is calculated in increments of 32 Kbps. The reset value will disable the rate limit for egress priority 2. If these bits are set to 0 no priority 0 frame will be sent out from this port.
15	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
30:16	EG_PRI1_RATE	0x7FFF	The egress rate limit for priority 1. The rate limit is calculated in increments of 32 Kbps. The reset value will disable the rate limit for egress priority 2. If these bits are set to 0 no priority 1 frame will be sent out from this port.
31	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.10.2.9 Rate Limit Register 2

Address: 0x0120 (See Table 3-23)
Access: Read/Write
Reset: See field description

This register used to set the rate limits for priority queues.

Bit	Bit Name	Reset	Description
14:0	EG_PRI2_RATE	0x7FFF	The egress rate limit for priority 2. The rate limit is calculated in increments of 32 Kbps. The reset value will disable the rate limit for egress priority 2. If these bits are set to 0 no priority 2 frame will be sent out from this port.
15	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.
30:16	EG_PRI3_RATE	0x7FFF	The egress rate limit for priority 3. The rate limit is calculated in increments of 32 Kbps. The reset value will disable the rate limit for egress priority 0. If these bits are set to 1 no priority 3 frame will be sent out from this port.
31	RES	0x0	Reserved. Must be written with zero. Contains zeros when read.

3.10.3 Statistics Counters

Table 3-10 lists the AR7240 statistics counters.

Table 3-10. **Extensive RMON/Statistics Counters**

Name	Description	Port0	Port1	Port2	Port3	Port4
RxBroad	The number of good broadcast frames received	20000	20100	20200	20300	20400
RxPause	The number of pause frames received	20004	20104	20204	20304	20404
RxMulti	The number of good multicast frames received	20008	20108	20208	20308	20408
RxFcsErr	Total frames received with a valid length that have an invalid FCS and an integral number of octets	2000C	2010C	2020C	2030C	2040C
RxAllignErr	Total frames received with a valid length that not have an integral number of octets and invalid FCS	20010	20110	20210	20310	20410
RxRunt	The number of frames received that are less than 64 byte long and good FCS	20014	20114	20214	20314	20414
RxFragment	The number of frames received that are less than 64 byte long and bad FCS	20018	20118	20218	20318	20418
Rx64Byte	The number of frames received that are exactly 64 byte long, including those with errors	2001C	2011C	2021C	2031C	2041C
Rx128Byte	The number of frames received whose length between 65 to 127, including those with errors	20020	20120	20220	20320	20420
Rx256Byte	The number of frames received whose length between 128 to 255, including those with errors	20024	20124	20224	20324	20424
Rx512Byte	The number of frames received whose length between 256 to 511, including those with errors	20028	20120	20228	20328	20428
Rx1024Byte	The number of frames received whose length between 512 to 1023, including those with errors	2002C	2012C	2022C	2032C	2042C
Rx1518Byte	The number of frames received whose length between 1024 to 1518, including those with errors	20030	20130	20230	20330	20430
RxMaxByte	The number of frames received whose length between 1519 to MaxLength, including those with errors (Jumbo)	20034	20134	20234	20334	20434
RxTooLong	The number of frames received whose length exceed MaxLength, including those with FCS errors	20038	20138	20238	20338	20438
RxGoodByte	Total data octets received in frame with a valid FCS; all size frames are included	2003C	2013C	2023C	2033C	2043C
RxBadByte	Total data octets received in frame with a invalid FCS alignment error; all size frames are included and pause frame is included with a valid FCS	20044	20144	20244	20344	20444

Table 3-10. **Extensive RMON/Statistics Counters (continued)**

RxOverFlow	Total valid frames received that are discarded due to lack of buffer space.	2004C	2014C	2024C	2034C	2044C
Filtered	Port disable and unknown VID	20050	20150	20250	20350	20450
TxBroad	Total good frames transmitted with a broadcast destination address	20054	20154	20254	20354	20454
TxPause	Total good PAUSE frames transmitted	20058	20150	20258	20358	20458
TxMulti	Total good frames transmitted with a multicast destination address	2005C	2015C	2025C	2035C	2045C
TxUnderRun	Total valid frames discarded that were not transmitted due to Tx FIFO underflow	20060	20160	20260	20360	20460
Tx64Byte	Total frames transmitted with a length of exactly 64 byte, including errors	20064	20164	20264	20364	20464
Tx128Byte	Total frames transmitted with length between 65 to 127, including errors	20068	20138	20268	20368	20468
Tx256Byte	Total frames transmitted with length between 128 to 255, including errors	2006C	2016C	2026C	2036C	2046C
Tx512Byte	Total frames transmitted with length between 256 to 511, including errors	20070	20170	20270	20370	20470
Tx1024Byte	Total frames transmitted with length between 512 to 1023, including errors	20074	20174	20274	20374	20474
Tx1518Byte	Total frames transmitted with length between 1024 to 1518, including errors	20078	20178	20278	20378	20478
TxMaxByte	Total frames transmitted with length between 1519 to MaxLength, including errors (Jumbo)	2007C	2017C	2027C	2037C	2047C
TxOverSize	Total frames over MaxLength but transmitted truncated with bad FCS	20080	20180	20280	20380	20480
TxByte	Total data octets transmitted from frames counted, included with bad FCS	20084	20184	20284	20384	20484
TxCollision	Total collisions experienced by a port during packet transmissions	2008C	2018C	2028C	2038C	2048C
TxAbortCol	Total number of frames not transmitted because the frame experienced 16 transmission attempts and was discarded	20090	20190	20290	20390	20490
TxMultiCol	Total number of successfully transmitted frames that experienced more than one collision	20094	20194	20294	20394	20494
TxSingalCol	Total number of successfully transmitted frames that experienced exactly one collision	20098	20198	20298	20398	20498
TxExcDefer	The number of frames that deferred for an excessive period of time	2009C	2019C	2029C	2039C	2049C
TxDefer	Total frames whose transmission was delayed on its first attempt because the medium was busy	200A0	201A0	202A0	203A0	204A0
TxLateCol	Total number of times a collision is detected later than 512 bit-times into the transmission of a frame	200A4	201A4	202A4	203A4	204A4

3.11 PCIE Configuration Space Registers

Table 3-11 shows the PCI Express configuration space registers for the AR7240.

Table 3-11. **PCI Configuration Space Registers**

Offset	Description	Page
0x10000000	Vendor ID	page 144
0x10000002	Device ID	page 144
0x10000004	Command	page 145
0x10000006	Status	page 145
0x10000008	Revision ID	page 146
0x10000009	Class Code	page 146
0x1000000C	Cache Line Size	page 146
0x1000000D	Master Latency Timer	page 146
0x1000000E	Header Type	page 146
0x10000010	Base Address 0 (Read-Only)	page 147
0x10000010	BAR0 Mask (Write-Only)	page 147
0x10000018	Bus Number	page 148
0x1000001E	Secondary Status	page 148
0x10000020	Memory Base	page 148
0x10000022	Memory Limit	page 148
0x10000024	Prefetchable Memory Base	page 149
0x10000026	Prefetchable Memory Limit	page 149
0x10000034	Capability Pointer	page 149
0x1000003C	Interrupt Line	page 149
0x1000003D	Interrupt Pin	page 150
0x1000003E	Bridge Control	page 150

3.11.1 Vendor ID

Address: 0x10000000
Access: Read-Only

The default value is the hardware configuration parameter.

Bit	Bit Name	Description
15:0	CX_VENDOR_ID_0	Vendor ID

3.11.2 Device ID

Address: 0x10000002
Access: Read-Only

The default value is the hardware configuration parameters.

Bit	Bit Name	Description
15:0	CX_DEVICE_ID_0	Device ID

3.11.3 Command

Address: 0x10000004
Access: See field description
Reset: 0

Bit	Access	Description
15:11	RO	Reserved
10	R/W	INTx assertion disable
9	RO	Fast back-to-back enable Not applicable for PCIE. Hardwired to 0.
8	R/W	SERR# enable
7	RO	IDSEL stepping/wait cycle control Not applicable for PCIE. Hardwired to 0.
6	R/W	Parity error response
5	RO	VGA palette snoop Not applicable for PCIE. Hardwired to 0.
4	RO	Memory write and invalidate Not applicable for PCIE. Hardwired to 0.
3	RO	Special cycle enable Not applicable for PCIE. Hardwired to 0.
2	R/W	Bus master enable
1	R/W	Memory space enable
0	R/W	I/O space enable

3.11.4 Status

Address: 0x10000006
Access: See field description
Reset: See field description

Bit	Access	Reset	Description
15	RW1C	0	Detected parity error
14	RW1C	0	Signalled system error
13	RW1C	0	Received master abort
12	RW1C	0	Received target abort
11	RW1C	0	Signalled target abort
10:9	RO	0x0	DEVSEL timing; not applicable for PCIE. Hardwired to 0.
8	RW1C	0	Master data parity error
7	RO	0	Fast back-to-back capable; not applicable for PCIE. Hardwired to 0.
6	RO	0	Reserved
5	RO	0	66 MHz capable; not applicable for PCIE. Hardwired to 0.
4	RO	1	Capabilities list Indicates presence of an extended capability item. Hardwired to 1.
3	RO	0	INTx status
2:0	RO	0x0	Reserved

3.11.5 Revision ID

Address: 0x10000008
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
7:0	CX_REVISION_ID_0	Revision ID

3.11.6 Class Code

Address: 0x10000009
Access: Read-Only
Reset: 0x0

Bit	Bit Name	Description
23:16	BASE_CLASS_CODE_0	Base class code
15:8	SUB_CLASS_CODE_0	Sub class code
7:0	IF_CODE_0	Programming interface

3.11.7 Class Line Size

Address: 0x1000000C
Access: Read/Write
Reset: 0x0

Bit	Description
7:0	Cache line size This register is R/W for legacy compatibility purposes and is not applicable to PCI Express device functionality. Writing to the Cache Line Size register does not impact functionality of the RC.

3.11.8 Master Latency Timer

Address: 0x1000000D
Access: Read-Only
Reset: 0x0

Bit	Description
7:0	Master latency timer; not applicable to PCIE. Hardwired to 0.

3.11.9 Header Type

Address: 0x1000000E
Access: Read-Only
Reset: See field descriptions

Bit	Reset	Description
7	0x0	Multi-function device
6:0	0x01	Configuration header format. Hardwired to 0x01.

3.11.10 Base Address 0 (BAR0)

Address: 0x10000010
Access: Read-Only
Reset: See field descriptions

The RC Core provides one 32-bit base address register.

Bit	Reset	Description	
31:4	0x0000000	BAR0 base address bits. The BAR0 mask value determines which address bits are masked.	
3	PREFETCHABLE0_0 for memory BAR	If BAR0 is a memory BAR, indicates if the memory region is prefetchable:	
		0	Non-prefetchable
		1	Prefetchable
2:1	BAR0_TYPE_0 for memory BAR	If BAR 0 is a memory BAR, bits [2:1] determine the BAR type:	
		00	32-bit BAR
		10	Unused
0	MEM0_SPACE _DECODER_0	0	BAR0 is a memory BAR
		1	Unused

3.11.11 BAR0 Mask

Address: 0x10000010 (same as "Base Address 0 (BAR0)"
Access: Write-Only
Reset: See field descriptions

Determines which bits in the BAR are non-writable by host software, which determines the size of the address space claimed by the BAR. This register only exists when the corresponding BAR*n*_MASK_WRITABLE_0 value is 1. Otherwise, the BAR*n*_MASK_0 value sets the BAR Mask value in hardware.

BAR Mask values indicate the range of low-order bits in each implemented BAR to not use for address matching. The BAR Mask value also indicates the range of low-order bits in the BAR that cannot be written from the host. The application can write to all BAR bits to set memory, I/O, and other BAR options. To disable a BAR, the application can write a 0 to bit [0] of the BAR Mask register. To change the BAR Mask value for a disabled BAR, the application must first enable the BAR by writing 1 to bit [0]. After enabling the BAR, the application can write a new value to the BAR Mask register. If the BAR Mask value for a BAR is less than that required for the BAR type, the RC Core uses the minimum BAR type value:

- BAR bits [11:0] are always masked for a memory BAR. The RC Core requires each memory BAR to claim at least 4 KB
- BAR bits [7:0] are always masked for an I/O BAR. The RC Core requires each I/O BAR to claim at least 256 bytes

Bit	Bit Name	Description	
31:1	BAR0 _MASK_0	Indicates which BAR0 bits to mask (make nonwritable) from host software, which in turn determines the size of the BAR. For example, writing 0xFFF to the BAR0 Mask register claims a 4096-byte BAR by masking bits 11:0 of the BAR from writing by host software. Application write access depends on the value of BAR0_MASK_WRITABLE_0: ■ If BAR0_MASK_WRITABLE_0 = 1, the BAR0 Mask register is writable ■ If BAR0_MASK_WRITABLE_0 = 0, BAR0 Mask is not writable	
0	BAR0 _ENABLED _0	BAR0 enable	
		0	BAR0 is disabled
		1	BAR0 is enabled
		Bit [0] is interpreted as BAR enable when writing to the BAR Mask register rather than as a mask bit because bit [0] of a BAR is always masked from writing by host software.	

3.11.12 Bus Number

Address: 0x10000018
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
31:24	RO	Secondary latency timer; not applicable to PCI Express, hardwired to 0x00.
23:16	R/W	Subordinate bus number
15:8	R/W	Secondary bus number
7:0	R/W	Primary bus number

3.11.13 Secondary Status

Address: 0x1000001E
Access: See field descriptions
Reset: 0

Bit	Access	Description
15	RW1C	Detected parity error
14	RW1C	Received system error
13	RW1C	Received master abort
12	RW1C	Received target abort
11	RW1C	Signalled timer abort
10:9	RO	DEVSEL timing; not applicable to PCIE. Hardwired to 0.
8	RW1C	Master data parity error
7	RO	Fast back-to-back capable; not applicable to PCIE. Hardwired to 0.
6	RO	Reserved
5	RO	66 MHz; not applicable to PCIE. Hardwired to 0.
4:0	RO	Reserved

3.11.14 Memory Base

Address: 0x10000020
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
15:4	R/W	Memory base address
3:0	RO	Reserved

3.11.15 Memory Limit

Address: 0x10000022
Access: See field descriptions
Reset: 0x00

Bit	Access	Description
15:5	R/W	Memory limit address
4:0	RO	Reserved

3.11.16 Prefetchable Memory Base

Address: 0x10000024
Access: See field descriptions
Reset: See field descriptions

Bit	Access	Default	Description	
15:4	R/W	0x000	Upper 12 bits of 32-bit prefetchable memory start address	
3:1	RO	0x0	Reserved	
0	RO	MEM_DECODE_64_0	64-bit memory addressing	
			0	32-bit memory addressing
			1	Unused

3.11.17 Prefetchable Memory Limit

Address: 0x10000026
Access: See field descriptions
Reset: See field descriptions

Bit	Access	Default	Description	
15:4	R/W	0x000	Upper 12 bits of 32-bit prefetchable memory end address	
3:1	RO	0x0	Reserved	
0	RO	MEM_DECODE_64_0	64-bit memory addressing	
			0	32-bit memory addressing
			1	Unused

3.11.18 Capability Pointer

Address: 0x10000034
Access: Read-Only
Reset: 0x40

Bit	Description
7:0	First capability pointer Points to power management capability structure by default.

3.11.19 Interrupt Line

Address: 0x1000003C
Access: Read/Write
Reset: 0xFF

Bit	Description
7:0	Interrupt line

3.11.20 Interrupt Pin

Address: 0x1000003D
Access: Read-Only
Reset: 0x1

Bit	Description	
7:0	Interrupt pin. Identifies the legacy interrupt Message that the device uses. Valid values are:	
	00	The device does not use legacy interrupt
	01	The device uses INTA

3.11.21 Bridge Control

Address: 0x1000003E
See field descriptions
Reset: 0x0

Bit	Access	Description
15:12	RO	Reserved
11	RO	Discard timer SERR enable status; not applicable to PCIE. Hardwired to 0.
10	RO	Discard timer status; not applicable to PCIE. Hardwired to 0.
9	RO	Secondary discard timer; not applicable to PCIE. Hardwired to 0.
8	RO	Primary discard timer; not applicable to PCIE. Hardwired to 0.
7	RO	Fast back-to-back transactions enable; not applicable to PCIE. Hardwired to 0.
6	R/W	Secondary bus reset
5	RO	Master abort mode; not applicable to PCIE. Hardwired to 0.
4	R/W	VGA 16-bit decode
3	R/W	VGA enable
2	R/W	ISA enable
1	R/W	SERR enable
0	R/W	Parity error response enable

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 summarizes the absolute maximum ratings and Table 4-2 lists the recommended operating conditions for the AR7240.

Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 4-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max Rating	Unit
V_{dd33}	Supply voltage	–0.3 to 4.0	V
V_{dd25}	Maximum I/O supply voltage	–0.3 to 3.0	V
T_{store}	Storage temperature	–65 to 150	°C
T_j	Junction temperature	125	°C
ESD	Electrostatic discharge tolerance	2000	V

4.2 Recommended Operating Conditions

Table 4-2. **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD33}	Supply voltage	±10%	2.97	3.3	3.63	V
V_{DD25}	I/O supply voltage[1]	—	2.375	2.5	2.65	V
V_{DD12}	Core Voltage[1]	±5%	1.14	1.2	1.26	V
V_{DD12CD}	Core Voltage for CPU/DDR[1]	±5%	1.216	1.28	1.34	V
AV_{DD18}	Voltage for Ethernet PHY[1]	—	1.9	2.0	2.15	V
V_{DD_DDR}	DDR1 I/O Voltage[1]	±5%	2.47	2.6	2.73	V
D_{DR_VREF}	DDR Reference Level for SSTL Signals[2]	—	1.235	1.3	1.365	V
T_{case}	Case temperature	—	0	45	105	°C
Psi_{JT}	Thermal Parameter[3]	—	—	—	3.1	°C/W

[1]Voltage regulated internally by the AR7240. For 400 MHz operation, an external voltage regulator is required for VDD12CD and VDD12. See "External Voltage Regulator With 400 MHz Operation" on page 155 and reference design schematics for more information.
[2]Divide VDD_DDR voltage by two externally, see reference design schematic
[3]For 14x14 mm LQFP package.

4.3 General DC Electrical Characteristics

Table 4-3 lists the general DC electrical characteristics. These conditions apply to all DC characteristics unless otherwise specified:

T_{amb} = 25 °C, V_{dd25} = 2.5 V

Table 4-3. **General DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	2.0	—	2.8	V
V_{IL}	Low Level Input Voltage	—	–0.3	—	0.4	V
I_{IL}	Input Leakage Current	With pull down	—	26	—	µA
V_{OH}	High Level Output Voltage	I_o = 1 mA	2.2	—	2.8	V
V_{OL}	Low Level Output Voltage	I_o = 1 mA	0	—	0.4	V
I_O	Output Current	V_o = 0 to V_{dd}	—	1	—	mA
	GPIO_13 to GPIO_17 when used as LED_0 to LED_4	V_o = 0 to V_{dd}	—	10	—	mA
C_{IN}	Input Capacitance	—	—	3	—	pF

Table 4-4 lists the DDR1 DC electrical characteristics:

T_{amb} = 25 °C, V_{DD_DDR} = 2.6 V

Table 4-4. **DDR1 Interface DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	1.48	—	2.9	V
V_{IL}	Low Level Input Voltage	—	–0.3	—	1.12	V
V_{OH}	High Level Output Voltage	I_o = 1 mA	2.2	—	2.8	V
V_{OL}	Low Level Output Voltage	I_o = 1 mA	–0.3	—	0.4	V

Table 4-5 lists the EJTAG and LDO DC electrical characteristics:

T_{amb} = 25 °C, V_{DD}= 2.5 V

Table 4-5. **EJTAG and LDO DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage (EJTAG_SEL, TRST_L, TCK, LDO_DDR_SEL)	—	2	—	3.6	V
V_{IL}	Low Level Input Voltage (EJTAG_SEL, TRST_L, TCK, LDO_DDR_SEL)	—	–0.3	—	0.4	V
V_{IH}	High Level Input Voltage (TMS, TDI)	—	2	—	2.8	V
V_{IL}	Low Level Input Voltage (TMS, TDI)	—	–0.3	—	0.4	V
V_{OH}	High Level Output Voltage (TDO)	—	2.2	—	2.8	V
V_{OL}	Low Level Output Voltage (TDO)	—	0	—	0.4	V

4.4 40 MHz Clock Characteristics

The 40 MHz reference clock can be AC coupled sine wave or square wave. An external 100 pF capacitor should connect between REFCLKIN and the clock source. See Table 4-6 and Table 4-7 for more information.

Table 4-6. **40 MHz Clock Sine Wave Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{Ampl}	Peak-to-Peak Amplitude	—	0.6	—	1.4	V

Table 4-7. **40 MHz Clock SquareWave Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{Ampl}	Peak-to-Peak Amplitude	—	0.6	—	1.2	V
T_{DCycle}	Duty Cycle	—	40	50	60	%
T_{Rise}	Rise Time	—	—	—	3	ns
T_{Fall}	Fall Time	—	—	—	3	ns

4.5 Power Consumption

Primary voltage supply of the AR7240 is provided by the VDD33, pins 71 and 117. The VDD33 is regulated by the internal LDOs to supply power to the external DDR memory, and magnetics of the Ethernet ports.

Figure 4-1 depicts the output voltages regulated by the AR7240. Refer to the reference design schematics for details. Table 4-8 shows the typical power consumption for the AR7240 operating at 350 MHz with internal 5-port Ethernet Switch, PCIE interface in operating mode.

Table 4-8. **Power Consumption**

Symbol	Voltage (V)	Current (mA)[1]
V_{DD33}	3.3	689

[1]Current consumption without magnetics

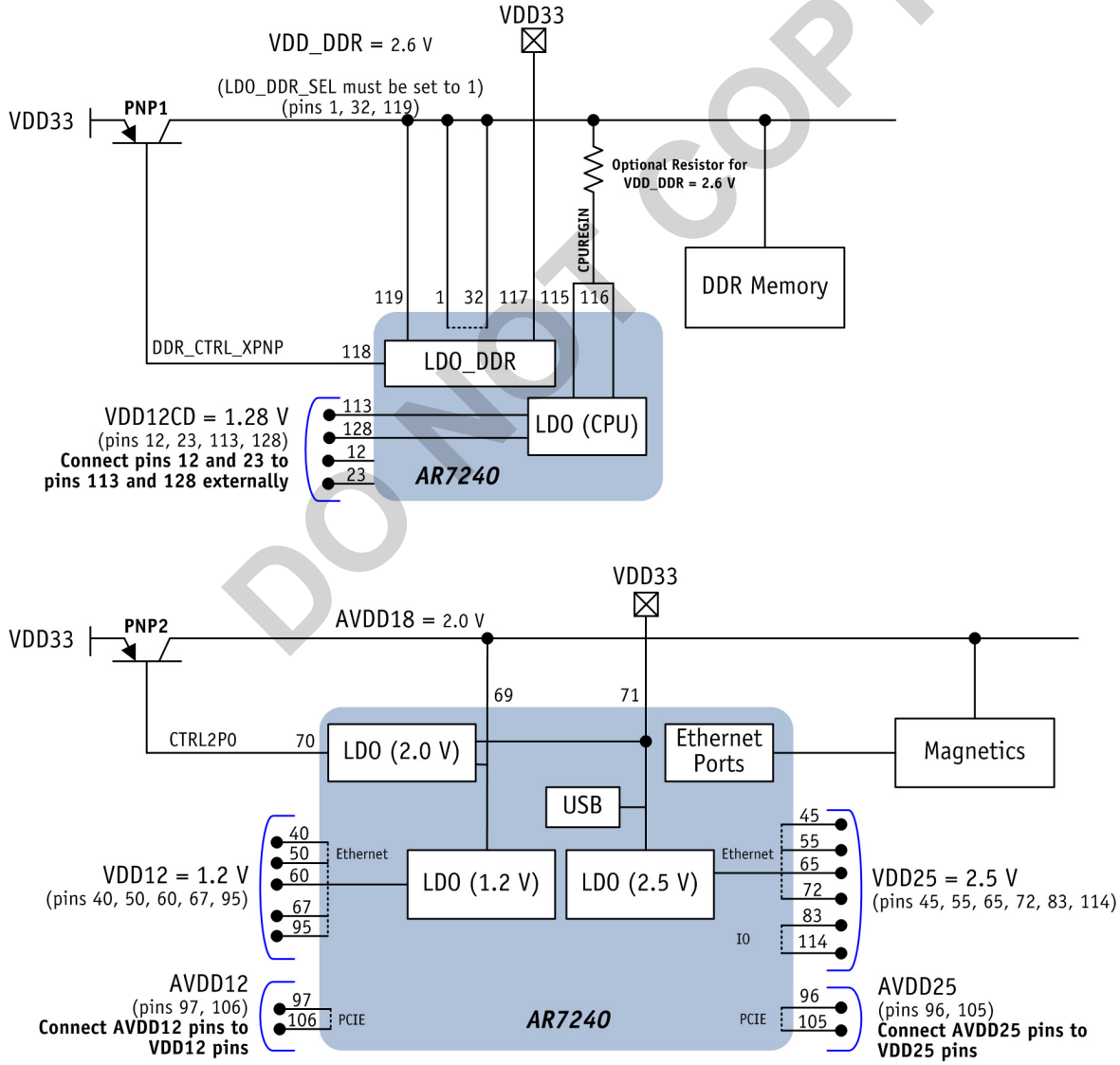


Figure 4-1. **Output Voltages Regulated by the AR7240**

4.6 External Voltage Regulator With 400 MHz Operation

When operating the AR7240 at 400 MHz, an external voltage regulator is required for VDD12CD and VDD12. Input to this regulator is 3.3 V and output should be 1.3 V ±2%.

Table 4-9. **Recommended External Voltage Regulator Operating Conditions**

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage	±10%	2.97	3.3	3.63	V
Output Voltage	±2%	1.274	1.3	1.326	V

Figure 4-2 depicts the output voltages regulated by the AR7240 (except for VDD12CD and VDD12). Refer to the reference design schematics for details.

Table 4-10 shows the typical power consumption for the AR7240 operating at 400 MHz with internal 5-port Ethernet Switch, PCIE interface in this operating mode.

Table 4-10. **Power Consumption With External Voltage Regulator**

Symbol	Voltage (V)	Current (mA)[1]
V_{DD33}	3.3	305
V_{DD12CD}[2]	1.3	527

[1]Current consumption without magnetics
[2]Current consumption includes V_{DD12}

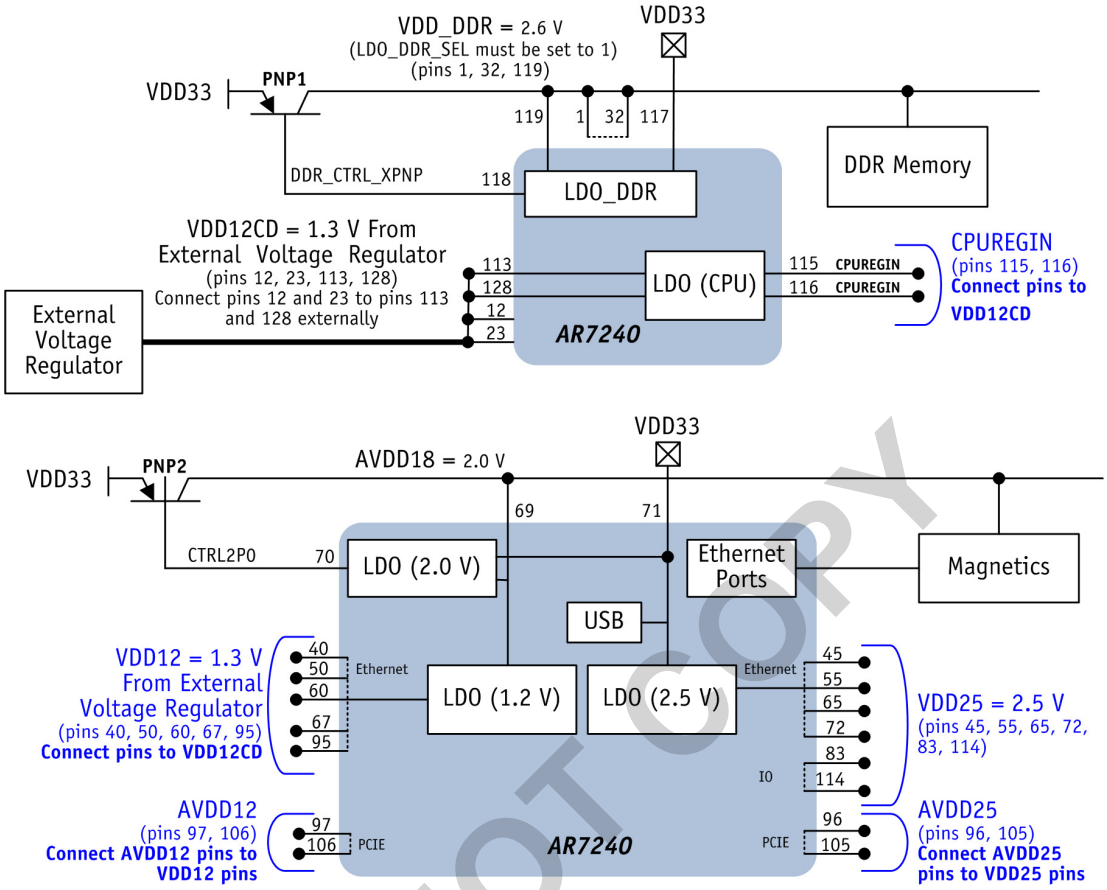


Figure 4-2. **Output Voltages Regulated by the AR7240 and External 1.3 V Voltage Regulator Connection**

5. AC Specifications

5.1 DDR Interface Timing

Figure 5-1 shows the DDR output timing. See Table 5-1 for timing values.

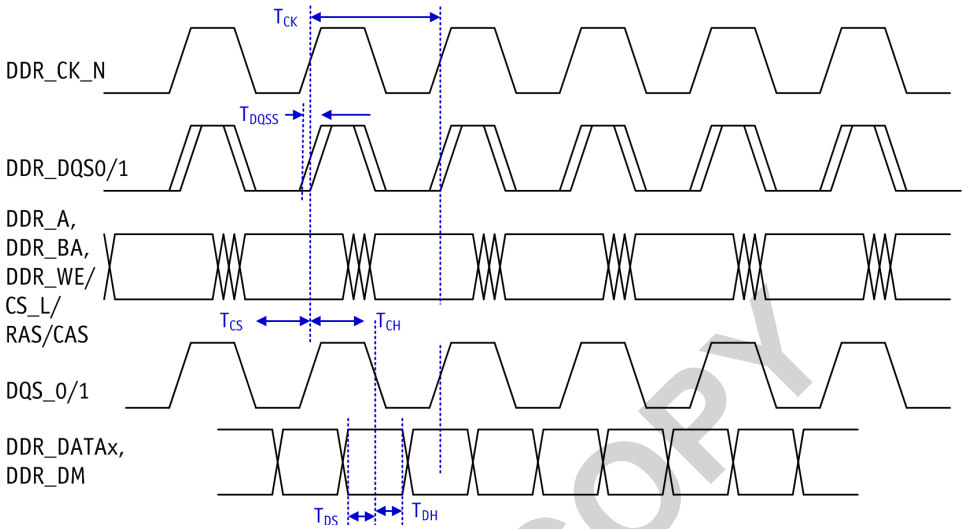


Figure 5-1. **DDR Output Timing**

Table 5-1. **DDR Output Timing Values[1]**

Parameter	Reference Signal	Min	Max	Comments
T_{CK}	—	—	5.0 ns	Normal period of CK_P clock output signal
T_{CS}	DDR_CK_P	2.0 ns	—	Control signals output setup time
T_{CH}	DDR_CK_P	2.0 ns	—	—
T_{DQSS}	DDR_CK_P	—	0.4 ns	Maximum skew between edge of CK_P and DQS with respect to either edge of CK_P
T_{DS}	DDR_DQS_0/1	1.0 ns	—	DDR data/mask signal setup time
T_{DH}	DDR_DQS_0/1	0.8 ns	—	DDR data/mask signal hold time

[1]These numbers assume a 400 MHz DDR_CLK frequency. Control signals include all address, bank address, RAS, CAS, CS_L, and CKE WE_L signals. Data signals include data and data mask signals.

Figure 5-2 shows the DDR input timing. See Table 5-2 for timing values.

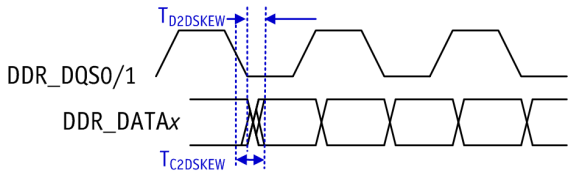


Figure 5-2. **DDR Controller Interface Input Timing**

Table 5-2. **DDR Controller Interface Input Timing Values**

Parameter	Reference Signal	Min	Max	Comments
$T_{C2DSKEW}$	DDR_DQS_0, DDR_DQS_1	—	0.4 ns	Maximum skew from DQS to DQ being stable from memory
$T_{D2DSKEW}$	—	—	0.2 ns	Maximum skew along data lines

5.2 Reset Timing

Internal reset of the AR7240 is held low until the VDD12 and VDD12CD voltages are up and RST_L pin (with internal pull-up) is deasserted. VDD12CD is generated from VDD_DDR, which is the last voltage domain to come up. The actual timing between the de-assertion of these signals is not critical. See Figure 5-3, the conceptual power up sequence.

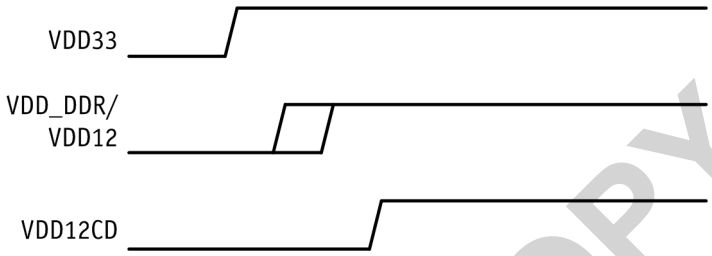


Figure 5-3. **Conceptual Power-Up Sequence**

Immediately after power on reset, the CPU boots up with the reference clock, then programs the PLL and releases all the interface resets, which causes the SYS_RST_OUT_L pin to be de-asserted. The time from internal reset de-asserted to the SYS_RST_OUT_L pin de-asserted is approximately 5 ms based on the 40 MHz reference clock. Figure 5-4 shows a conceptual reset timing diagram.

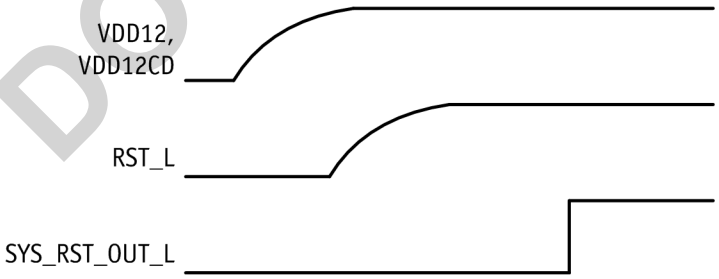


Figure 5-4. **Reset Timing**

5.3 SPI Serial Flash Interface Timing

Figure 5-5 shows the SPI serial flash interface timing.

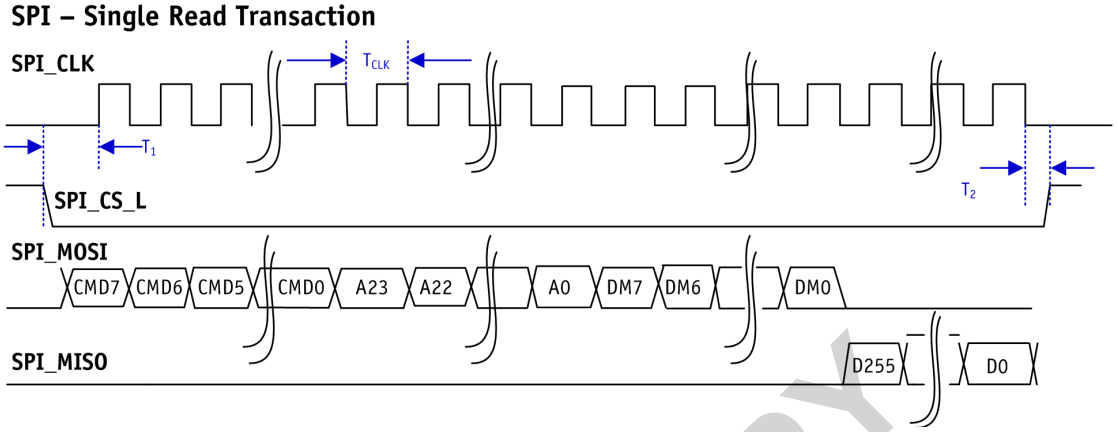


Figure 5-5. **SPI Serial Flash Interface Timing**

Table 5-3. **SPI Serial Flash Timing Values**

Symbol	Parameter
T_1	(3 + CLK_DIV) AHB_CLK Cycles
T_2	1 AHB_CLK
T_{CLK}	AHB_CLK/(CLK_DIV + 1) * 2

Figure 5-6 shows the SPI setup and hold timing.

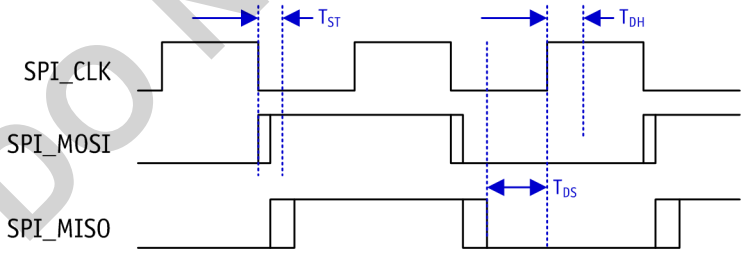


Figure 5-6. **SPI Setup and Hold Timing**

Table 5-4. **SPI Setup and Hold Timing Values**

Symbol	Minimum	Maximum	Comments
T_{DS}	3.0 ns	—	Minimum needed by the AR7240
T_{ST}	—	0.8 ns	Maximum time by which data is available
T_{DH}	0.5 ns	—	Minimum hold duration

6. Package Dimensions

The AR7240 LQFP-128 package drawings and dimensions are provided in Figure 6-1, Table 6-1, and Table 6-2.

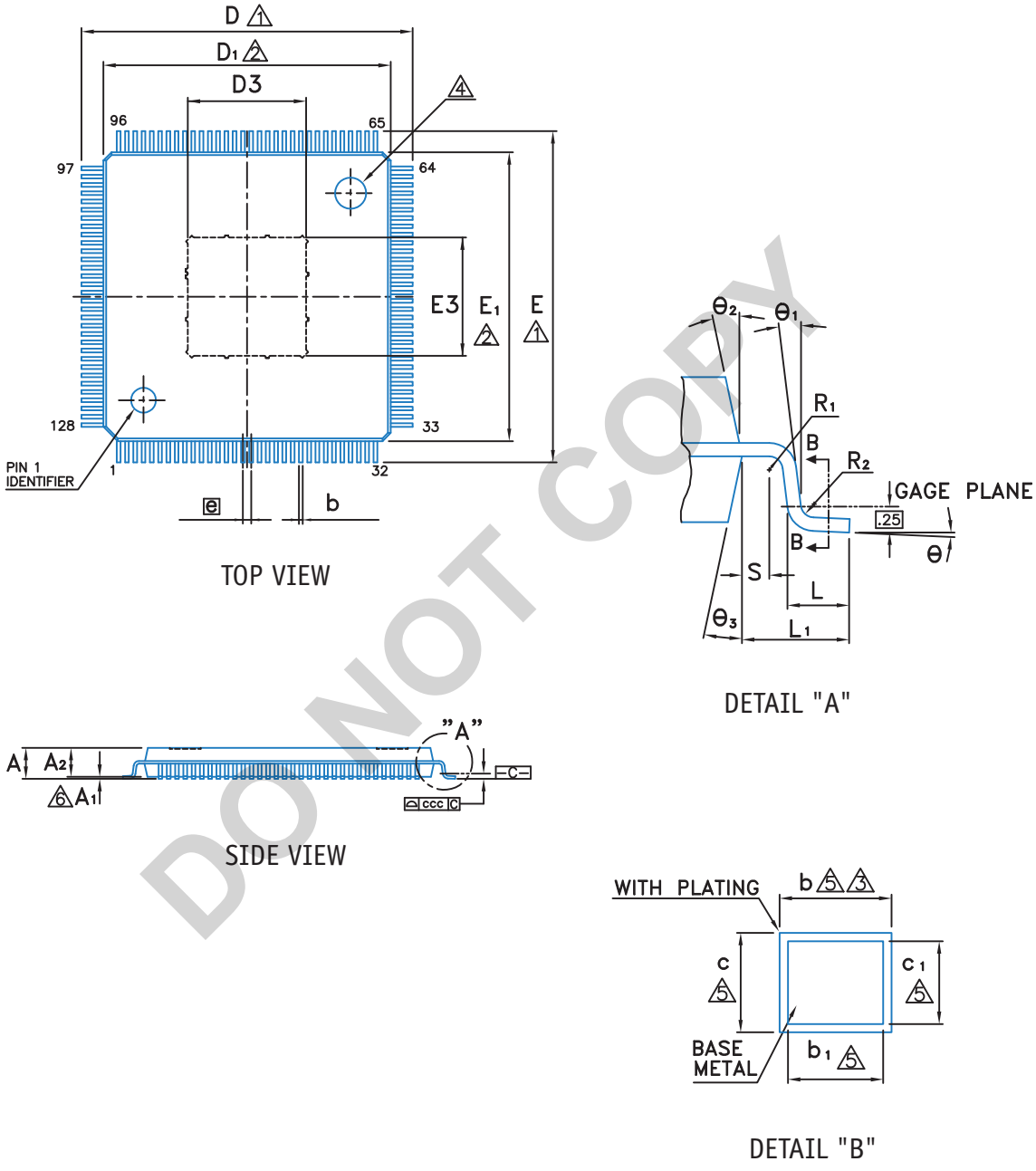


Figure 6-1. **Package Details**

Table 6-1. **Package Dimensions**

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	—	—	1.60	mm	—	—	0.063	inches
A1	0.05	—	—	mm	0.002	—	—	inches
A2	1.35	1.40	1.45	mm	0.053	0.055	0.057	inches
b	0.13	0.18	0.23	mm	0.005	0.007	0.009	inches
b1	0.13	0.16	0.19	mm	0.005	0.006	0.007	inches
c	0.009	—	0.20	mm	0.004	—	0.006	inches
c1	0.09	—	0.16	mm	0.004	—	0.006	inches
D	15.85	16.00	16.15	mm	0.624	0.630	0.636	inches
D1	13.90	14.00	14.10	mm	0.547	0.551	0.555	inches
E	15.85	16.00	16.15	mm	0.624	0.630	0.636	inches
E1	13.90	14.00	14.10	mm	0.547	0.551	0.555	inches
e	0.40 BSC			mm	0.016 BSC			inches
L	0.45	0.60	0.75	mm	0.018	0.024	0.030	inches
L1	1.00 REF			mm	0.039 REF			inches
R1	0.08	—	—	mm	0.003	—	—	inches
R2	0.08	—	0.20	mm	0.003	—	0.008	inches
S	0.20	—	—	mm	0.008	—	—	inches
θ	0	3.5	7	°	0	3.5	7	—
θ1	0	—	—	°	0	—	—	°
θ2/θ3	12° TYP				12° TYP			
ccc	0.08			mm	0.003			inches

[1] To be determined at seating plane C.
[2] Dimensions D1 and E1 do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
[3] Dimension b does not include dambar protrusion. Dambar can not be located on the lower radius of the foot.
[4] Exact shape of each corner is optional.
[5] These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
[6] A1 is defined as the distance from the seating plane to the lowest point of the package body.
[7] Controlling dimension: Millimeters.
[8] Reference document: JEDEC MS-026.
[9] Special characteristics C class: ccc.

Table 6-2. **Exposed Pad Size**

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
D3/E3	5.60/5.20 REF			mm	0.221/0.205 REF			inches

7. Ordering Information

The order number AR7240-AH1A specifies a LQFP lead-free standard-temperature version of the AR7240.

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