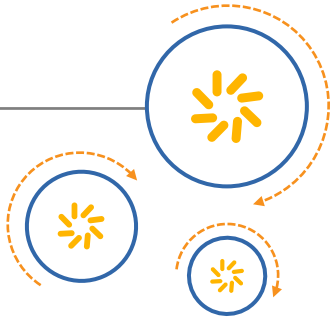
NOTICE REGARDING QUALCOMM ATHEROS, INC.

Effective June 2016, Qualcomm Atheros, Inc. (QCA) transferred certain of its assets, including substantially all of its products and services, to its parent corporation, Qualcomm Technologies, Inc. Qualcomm Technologies, Inc. is a wholly-owned subsidiary of Qualcomm Incorporated. Accordingly, references in this document to Qualcomm Atheros, Inc., Qualcomm Atheros, Atheros, QCA or similar references, should properly reference, and shall be read to reference, Qualcomm Technologies, Inc.

Qualcomm Atheros, Inc.



IPQ4018/IPQ4028 AP.DK01

Hardware Reference Guide

80-Y9700-1 Rev. E

May 16, 2016

Qualcomm Atheros, Inc.
1700 Technology Drive
San Jose, CA 95110
U.S.A.

Revision history

Revision	Date	Description
A	July 2015	Initial release

B	September 2015	▪ Section 1.1, Additional resources: Updated the Design Package doc numbers for IPQ4018 and IPQ4028
		▪ Section 2.1, AP.DK01 block diagram:
		  ▫ Updated the clock frequency from 600 MHz to 626 MHz.
		  ▫ Add the feature support for Single SPI NAND Flash.
		  ▫ Update Figure 2-1.
		▪ Section 3.1, Clock: Added Items of “Nominal Frequency, Drive Level and Equivalent Series Resistance” to Table 3-2.
		▪ Section 3.2, Reset: Updated the resistor and capacitor value for A92.
		▪ Section 3.5.1, PSGMII: Add additional guidelines for Length and System in Table 3 9.
		▪ Section 3.5.2, MDIO: Add 10 pF to MDIO in Table 3 11.
		▪ Section 3.12, GPIOs, in Table 3-21:
		  ▫ Updated the Table heading for column 2.
		  ▫ Add additional description for GPIO[62].
		  ▫ Updated description for GPIO[58, 59, 63].
		▪ Section 4.2, Internal regulators in IPQ4018/IPQ4028: Updated VTT LDO current value
		▪ Section 6.1, AP.DK01 RF block description:
		  ▫ Updated the RF parts and Figure 6-1.
		  ▫ Updated section 6.1.2 to section 6.1.6.
		▪ Section 6.2, RF layout guidelines:
		  ▫ Updated section 6.2.1 and section 6.2.2.
		  ▫ Added section 6.2.3 to section 6.2.8.
		▪ Section 7.3, Power: Highlighted 0.1 µF for pins A55 and A58 on the same side with chip in Table 7-1.
		▪ Section 7.5, Boot configuration: Added Figure 7-5 and Figure 7-6.

C	November 2015	▪ Section 1.1, Additional resources: Updated the Design Package doc numbers for IPQ4018 and IPQ4028
		▪ Section 2.1, AP.DK01 block diagram: Updated the AP.DK01 memory components.
		▪ Section 3.1, Clock: Updated description for Grounding and Routing.
		▪ Section 3.8, SPI: Updated Table 3-16 SPI flash memory used in AP.DK01.
		▪ Section 3.10, DDR3L DRAM: Update Table 3-18 DDR3L memory used in AP.DK01.
		▪ Removed section 4.5 Power consumption.
		▪ Updated Section 5.2, System thermal characteristics:
		  ▫ Added sections 5.2.1, 5.2.2, and 5.2.3.
		▪ Section 6, RF design:
		  ▫ Updated sections 6.1.3, 6.1.4, 6.2.1, 6.2.7, 6.2.8, and 6.3.
		  ▫ Removed section 6.1.6 Antenna and added section 6.1.6.
		  ▫ Added section 6.2.6.
		▪ Updated section 7.7, QCA8075 layout guidelines.
		▪ Updated A, Performance Characteristics.

Revision	Date	Description
D	November 2015	Section 2.1, AP.DK01 block diagram: Updated the clock frequency from 626 MHz to 710 MHz.
E	May 2016	▪ Section 2.1, AP.DK01 block diagram: Updated the clock frequency from 626 MHz to 716.8 MHz and DDR frequency from 533 to 537.6 MHz. ▪ Section 3.10, DDR3L DRAM: Updated the DDR frequency from 533 to 537.6 MHz.

Contents

Figures

Tables

1 Introduction

This document provides design guidelines for an AP.DK01 reference design based on IPQ4018/IPQ4028. The design is mainly targeting the low to medium end AP market. The IPQ4018/IPQ4028 is a single chip AP solution that can support 2.4 GHz and 5 GHz Wi-Fi simultaneously.

1.1 Additional resources

This document assumes that the reader is familiar with the *IEEE 802.11a/b/g/n and 802.11ac specifications.*

For topics that are not addressed in this document, see:

- IPQ4018 Access Point SoC Device Specification (80-Y9347-18)
- IPQ4028 Access Point SoC Device Specification (80-Y9347-28)
- QCA8075 Five-Port 10/100/1000 Mbps Ethernet Transceiver Device Specification (80-Y9112-1)
- IPQ4018.AP.DK01.1, 2X2 11AC DBDC FEM (RFMD/SKY/RFAXIS) 5GE 2USB RET QFN, Reference Design Schematic, Layout, and BOM (DP25-YB021-2)
- IPQ4028.AP.DK01.2, 2X2 11AC DBDC FEM (RFMD/SKY/RFAXIS) 5GE 2USB ENT QFN, Reference Design Schematic, Layout, and BOM (DP25-YB021-4)

2 AP.DK01 Overview

AP.DK01 is a low to medium end AP reference design. The AP.DK01 reference design has the following chip solution:

- IPQ4018/IPQ4028 is a highly integrated system-on-chip (SoC) designed for high-performance, power efficient, and cost-effective 2×2, 802.11ac, dual-band concurrent access point applications. The SoC incorporates a quad-core ARM Cortex A7 processor, two dual-band, concurrent 802.11ac Wave-2 Wi-Fi subsystems, and a five-port Gigabit Ethernet Layer2/3/4 multilayer switch supporting line rate network address translation (NAT). It supports one USB3.0 and one USB2.0.
- QCA8075 Ethernet transceiver is a 5-port, 10/100/1000 Mbps tri-speed Ethernet PHY. The QCA8075 Ethernet transceiver provides physical layer functions for half/full-duplex 10BASE-Te, 100BASE-TX, and full-duplex 1000BASE-T Ethernet to transmit and receive data over standard Category 5 (CAT-5) unshielded twisted pair cable. QCA8075 is connected to the PSGMII interface of IPQ4018/IPQ4028.

2.1 AP.DK01 block diagram

The AP.DK01 reference design consists of the following functional blocks:

- IPQ4018/IPQ4028 has a quad-core ARM Cortex A7 processors which operates at a clock frequency of 716.8 MHz, 32 KB instruction cache and 32 KB data cache per core, 256 KB L2 cache (shared)
- IPQ4018/IPQ4028 on-chip dual-band concurrent (DBDC) 2×2 2.4 GHz 802.11n (256QAM) and 2×2 5 GHz 802.11ac, two dedicated CPUs for Wi-Fi offloading and feature growth. Cooperates with RFMD/SKY/RFAXIS front-end chips.
- A QCA8075 five-port, 10/100/1000 Mbps tri-speed Ethernet PHY connected to the PSGMII of IPQ4018/IPQ4028, to provide LAN/WAN network connectivity.
- One USB3.0 connector and one USB2.0 connector which operate in the host mode.
- The AP.DK01 reference design comprises of three memory components:
  - Single 32MByte SPI NOR Flash
  - 16-bit maximum of 256MByte capacity low power DDR3 memory, implemented in a single rank configuration running at 537.6 MHz clock speed and 1075.2 MT/s data rate
  - 2MB SPI NOR + 128MB SPI NAND Flash
- DC/DC switching regulators to provide the different DC voltage levels for main chip usage.
- Single 48 MHz crystal for IPQ4018/IPQ4028
- JTAG interface and UART interface for CPU debugging

- LEDs

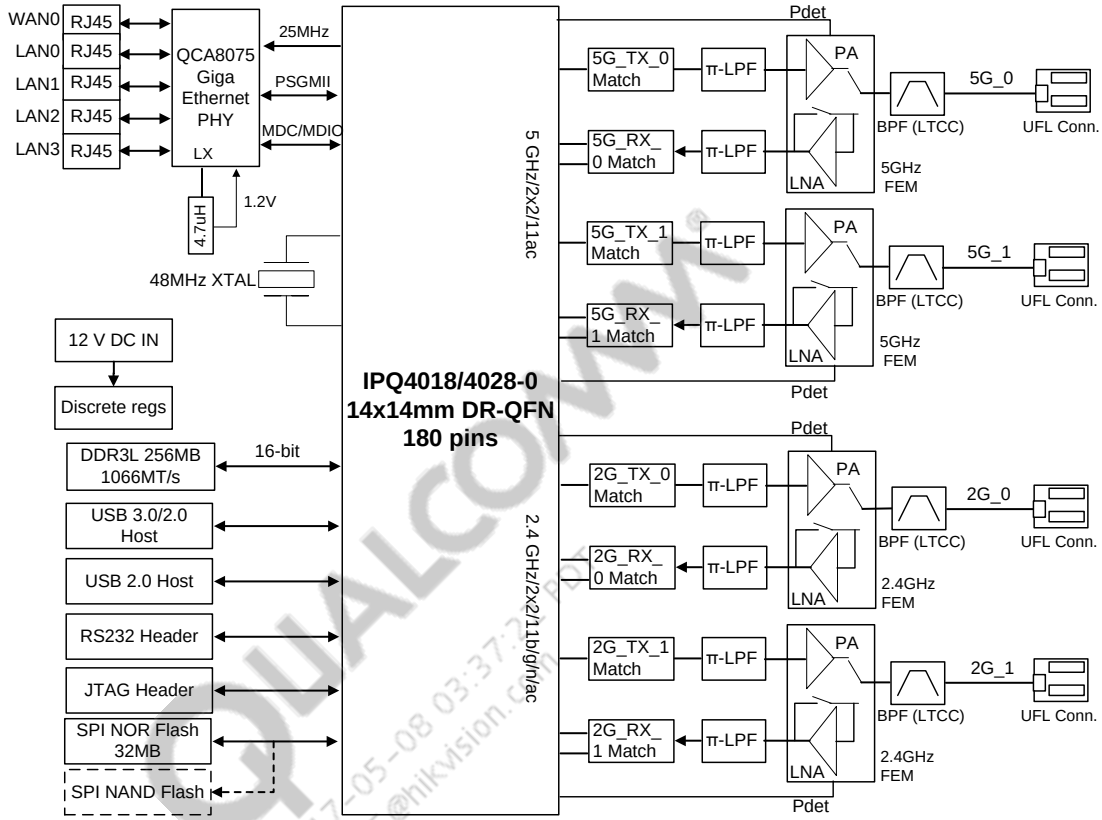


Figure 2-1 AP.DK01 hardware block diagram

3 Board Design Guidelines

3.1 Clock

The 48 MHz crystal attached to IPQ4018/IPQ4028, internally forming an oscillator, provides the core clock for the IPQ4018/IPQ4028. The IPQ4018/IPQ4028 provides the output of the oscillator to its internal frequency synthesizer and all digital PLLs.

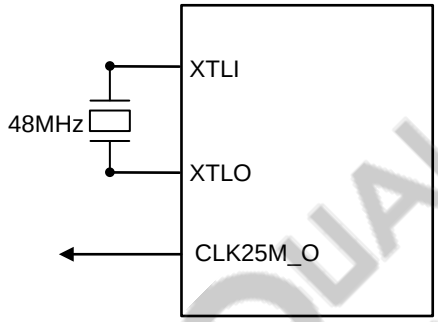


Figure 3-1 IPQ4018/IPQ4028 clock diagram

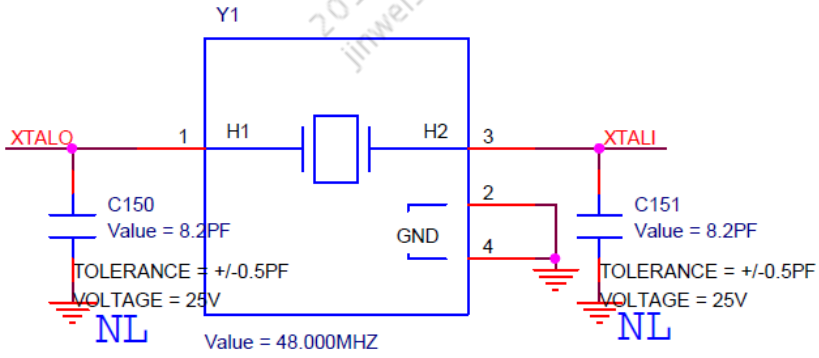


Figure 3-2 Schematic implementation

Table 3-1 Crystal used in AP.DK01

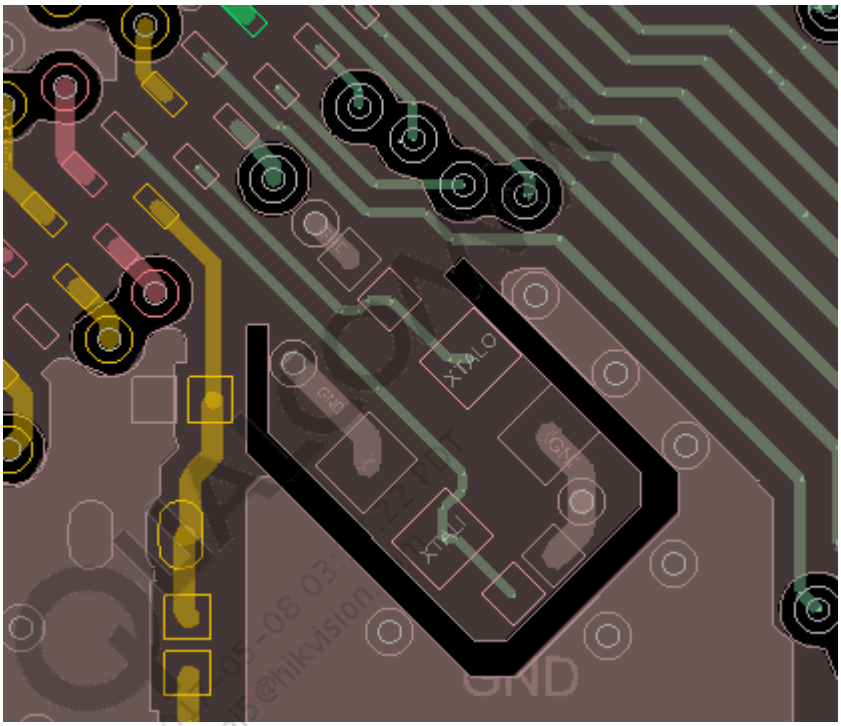
Company	Device
KYOCERA	CX2016DB48000E0DLFA1

Table 3-2 Crystal specifications

Items	Electrical specification				Test condition
	Min	Typ.	Max	Unit	
Nominal Frequency		48		MHz	
Load Capacitance	–	9.0	–	pF	Network Analyzer E5100A
	–	11.1	–	pF	Network Analyzer 250B
Frequency Tolerance	-8.0	–	+8.0	ppm	Network Analyzer E5100A
Frequency Temperature characteristics	-10.0	–	+10.0	ppm	-30 to +85 °C Network Analyzer E5100A
Drive Level (Pd)	10		100	µW	
Equivalent Series Resistance (ESR)			22	Ω	Network Analyzer E5100A

Table 3-3 Crystal design guidelines

Category	Guideline
Component	48 MHz crystal An SMD package is recommended.
Placement	Place the crystal and tuning capacitors close to the IPQ4018/IPQ4028 on the top side with sufficient isolation.
Spacing	Maintain >2 W spacing for these traces. An isolated GND pour is recommended around the crystal that nets to a GND moat below it.

Category	Guideline
Grounding	An isolated GND pour is recommended around the crystal esp for the two GND pins and covering the XTAL XIN/XOUT pins. Connect to the second layer GND by several vias.For better isolation, create a moat around the crystal GND as shown below; include the crystal and its associate components within the moat and run the separation around this block. No other signal via should transit this moat and no other GND connection should be made into it. 
Routing	Route wide short traces from the crystal pins to the IPQ4018/IPQ4028. Limit the PCB routing parasitic to less than 500fF per line. Route in as straight line as possible and follow the order of the XTAL foot print so as not to swap the PCB routing.

The IPQ4018/IPQ4028 also generates clock output for system application to save cost. Refer to pin CLK25M_O which is 25 MHz clock for Ethernet PHY QCA8075.

Table 3-4 IPQ4018/IPQ4028 clock output pin

Pin number	Pin name	Description and guidelines
B46	CLK25M_O	25 MHz clock output at 1.1V levels This clock can be used to feed external Ethernet device. The trace must be as short as possible. Maintain a separation (2 W) from neighboring traces. It is recommended to provide for a series damping resistor at the source pin (populated with 0 Ω).

3.2 Reset

The IPQ4018/IPQ4028 reset signals should be handled as shown in Table 3-5.

Table 3-5 IPQ4018/IPQ4028 reset signals

Pin number	Pin name	Description and guidelines
A92	CHIP_PWD_L	Fundamental reset input Recommended RC circuit is 10K pull-up with 1 µF pull-down.
A68	SYS_RST_L	GPIO62 default function is system reset output (SYS_RST_L). It can be used as hardware reset input for other system chips. Following verified HDK reset design to avoid any driver modification is recommended.

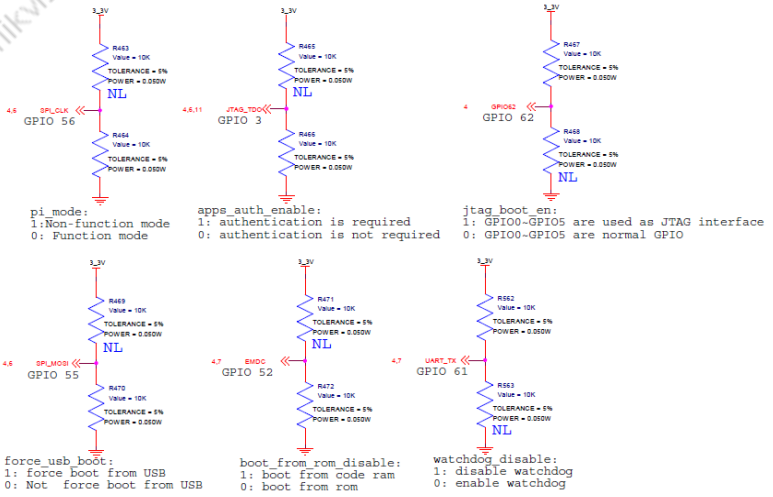
3.3 Boot configuration straps

At hardware reset, several IPQ4018/IPQ4028 GPIO pins are default as input to sense boot configuration settings.

The configuration straps are described in the device documentation; see the device specification for more details. Note that all options listed therein may not be supported in the reference design and software releases.

Table 3-6 IPQ4018/IPQ4028 boot configuration pins

Pin number	Pin name	Alt function	Configuration implementation
A64	GPIO56	pi_mode: 1 = Non-function mode 0 = Function mode	Schematic implementation as recommended. Their recommended value for pull-up or pull-down is 10k.
A90	GPIO3	apps_auth_enable: 1 = authentication is required 0 = authentication is not required	
A68	GPIO62	jtag_boot_en: 1 = GPIO0~GPIO5 are used as JTAG interface 0 = GPIO0~GPIO5 are normal GPIO	
A63	GPIO55	1 = Reserved 0 = Normal boot	
B49	GPIO52	boot_from_rom_disable: 1 = boot from code RAM 0 = boot from SPI NOR	
B55	GPIO61	watchdog_disable: 1 = disable watchdog 0 = enable watchdog	



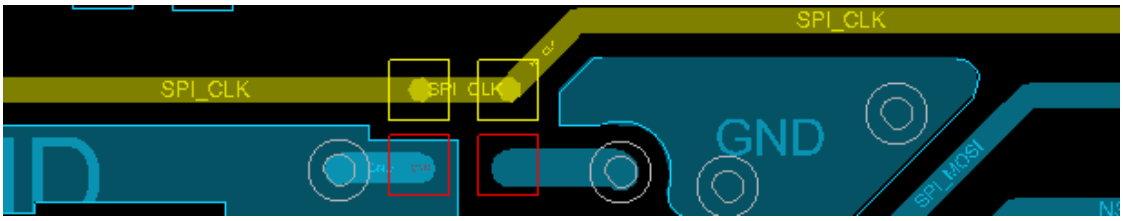


Figure 3-3 Configuration strap layout

Minimize stubs routing of the configuration straps to the IPQ4018/IPQ4028 lines.

3.4 Reference resistors

The IPQ4018/IPQ4028 uses one reference resistor. This section describes the designated value and design guidelines.

Table 3-7 IPQ4018/IPQ4028 reference resistors

Pin number	Pin name	Value
A56	RBIAS	5.9 K 1%

Table 3-8 Reference resistors design guidelines

Category	Guidelines/Remarks
Signals/ Groups	Reference resistors as per Table 3-7.
Placement	Place these resistors as close as possible to the IPQ4018/IPQ4028 device. Route them with wide traces within 200 mils.
Spacing	Provide as much spacing from these traces/ resistors to neighboring board features as practically possible (at least 2 W).
Routing and Other	Connect the other end of these resistors directly to GND with dedicated vias. Avoid sharing vias on the return path as this can cause noise pickup from the other elements tied to the GND trace.

3.5 Ethernet interfaces

3.5.1 PSGMII

One PSGMII is available on the IPQ4018/IPQ4028 which is used to connect with QCA8075.

Table 3-9 shows the routing guidelines for these interfaces.

Table 3-9 PSGMII interface routing guidelines

Category	Guidelines/Remarks
Groups	PSGMII Tx, PSGMII Rx
Route type	Differential pair, 100 Ω impedance
Length	< 5 inches (< 1 inch is recommended for 2.4 GHz noise floor improvement)
Length match within pair	±5 mils (refer to Table 3-10)

Category	Guidelines/Remarks
Length match across pairs	There is no requirement to length match the Tx and Rx pairs.
Spacing requirements	3 W spacing between pairs and to other signals
Vias/ layer transitions	Minimize layer transitions; where necessary limit to 2 vias per signal trace. Provide return vias interconnecting the GNDs in the immediate vicinity of the signal vias.
AC coupling	Use 0.1 µF capacitors on each signal line; place them symmetrically at the same point on the pair; it is preferable to locate the capacitors close to the Rx or receiver pads.
System	▪ Route the PSGMII signal far away from the RF area. ▪ Add shielding-case foot-print for PSGMII trace.

Chip internal delay should be taken into consideration for length control.

Table 3-10 Internal length of IPQ4018/IPQ4028 QFN chip − PSGMII

PSGMII	Internal wire (mm)
PSGMII_SIP	1.34721
PSGMII_SIN	1.39433
PSGMII_SOP	1.37797
PSGMII_SON	1.34058

NOTE: QCA8075 length control of PSGMII differential pair can refer to the edge of the QFN package.

Figure 3-4 shows a reference implementation of the PSGMII layout.

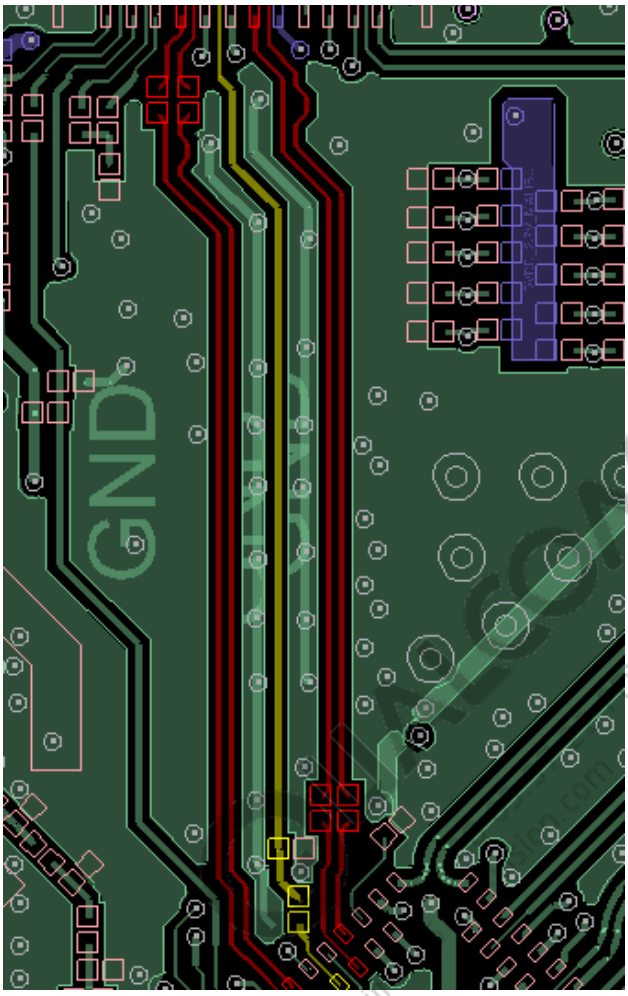


Figure 3-4 PSGMII routing

3.5.2 MDIO

NOTE: The MDIO and MDC signals used to communicate with and control the external Ethernet devices (QCA8075) are de-multiplexed out on the GPIO[53] (MDIO), GPIO[52] (MDC).

The reference designs implemented shown in Table 3-11.

Table 3-11 MDIO interface routing guidelines

Category	Guidelines/remarks
Signal/group	EMDIO, EMDC
Spacing	Because open drain signaling is used by MDIO, these signals are susceptible to crosstalk from strongly driven aggressors. A spacing of 2 W is recommended at a minimum from other signals for both MDIO and MDC.
Loading	Run the traces short to the devices and reduce capacitive load.
Voltage	MDC is 3.3V push-pull output. MDIO is od-gate and requires an external pull-up. The reference design requires an external pull-up to QCA8075 2.7V.
System	Add shunt 10 pF on EMDIO net for 2.4 GHz noise floor improvement.

3.6 USB

IPQ4018/IPQ4028 device has two USB host ports. One of them J16 supports USB3.0 (with both SS and HS PHY). The other J22 only supports USB2.0 with HS PHY. Implement the design guidelines shown in Table 3-12 and Table 3-13.

Table 3-12 USB 3.0 design guidelines

Category	Guidelines/Remarks
Groups	(USB1_TXP, USB1_TXN), (USB1_RXP, USB1_RXN)
Route type	Differential pair, 90 Ω impedance for the super speed pairs
Return path	Ensure continuous and unbroken return path without voids
Length	< 5 inches
Length match within pair	±5 mils
Length match across pairs	There is no requirement to length match the Tx and Rx pairs
Spacing requirements	3 W spacing between pairs and to other signals after the breakout from the BGA
Vias/ layer transitions	Avoid layer transitions; the reference design has been routed without vias on this interface with the signals traversing on top layer throughout. It is recommended to follow this layout.
AC coupling	Use 0.1 µF capacitors on each signal line of the Tx pair from IPQ4018/IPQ4028; place them symmetrically at the same point on the pair; it is preferable to locate the capacitors close to the Rx or receiver pads.
Other	Clear the GND pour under the signal pads of the connector where SMD connectors are used.

Table 3-13 USB 2.0 design guidelines

Category	Guidelines/Remarks
Groups	(USB2_DP, USB2_DM), (USB1_DP, USB1_DM)
Route type	Differential pair, 90 Ω impedance for the USB2.0 pair
Return path	Ensure continuous and unbroken return path without voids
Length	< 5 inches
Length match within pair	±5 mils
Length match across pairs	Not applicable.
Spacing requirements	3 W spacing between pairs and to other signals after the breakout from the package
Vias/ layer transitions	Avoid layer transitions; the reference design has been routed without vias on this interface with the signals traversing on top layer throughout and it is recommended to follow this layout over continuous GND return path.
AC coupling	Not applicable; the lines must be DC connected.
Other	Clear the GND pour under the signal pads of the connector where SMD connectors are used.

Chip internal delay must be take into consideration for length control.

Table 3-14 Internal length of IPQ4018/IPQ4028 chip − USB

USB	Internal wire (mm)
USB2.0 port	
USB2_DM	1.56185
USB2_DP	1.5813
USB3.0 port	
USB1 _DM	2.68963
USB1 _DP	2.7111
USB1_ RXN	2.25251
USB1_ RXP	2.18477
USB1_ TXN	1.7222
USB1_ TXP	1.68946

The layout has been implemented in the reference designs as shown in Figure 3-5 and Figure 3-6.

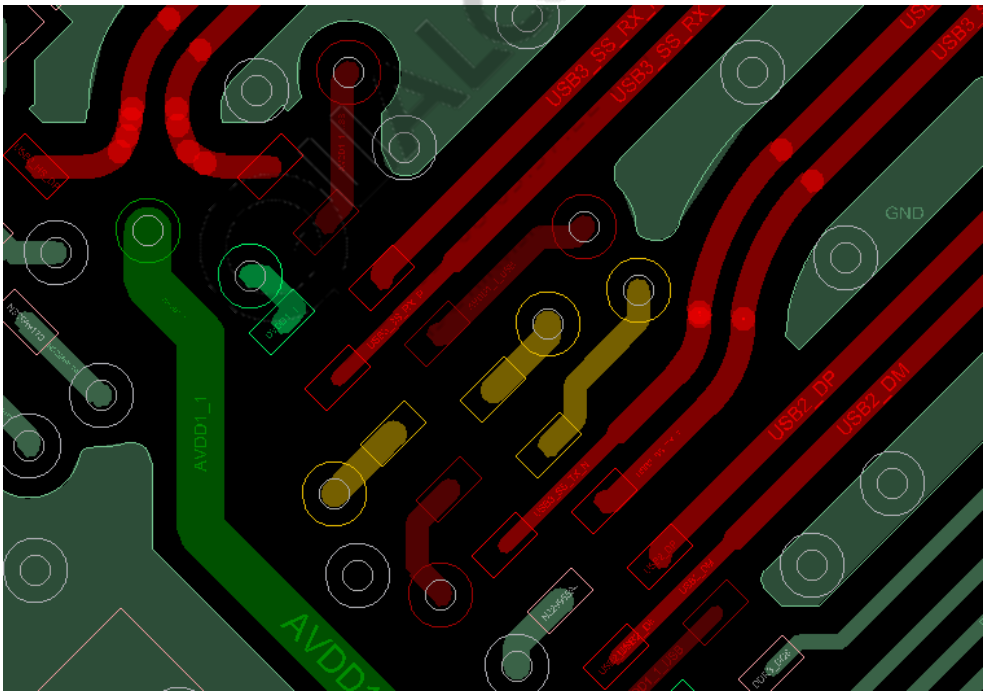


Figure 3-5 USB trace breakout at the IPQ4018/IPQ4028

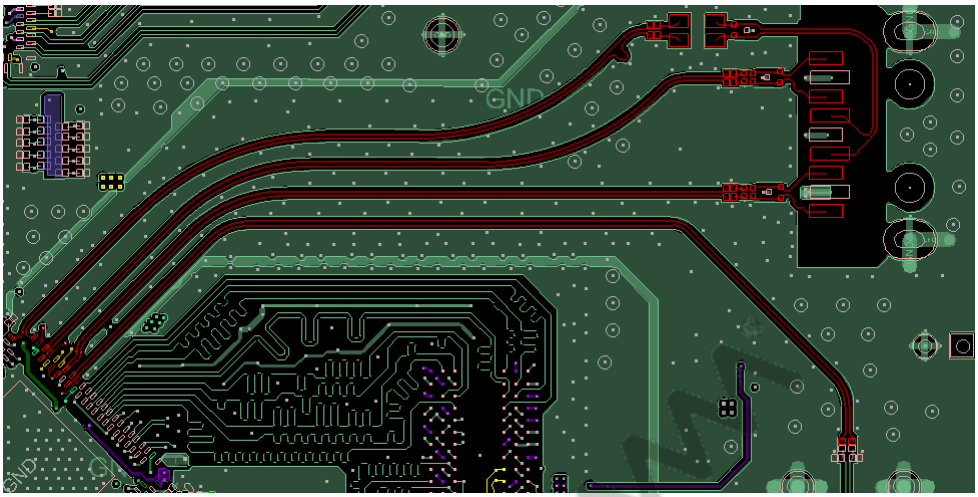


Figure 3-6 USB routing overview

The signals are routed without vias in the top layer end-to-end and the super-speed Tx pair is routed around the connector to the pins to avoid transitions.

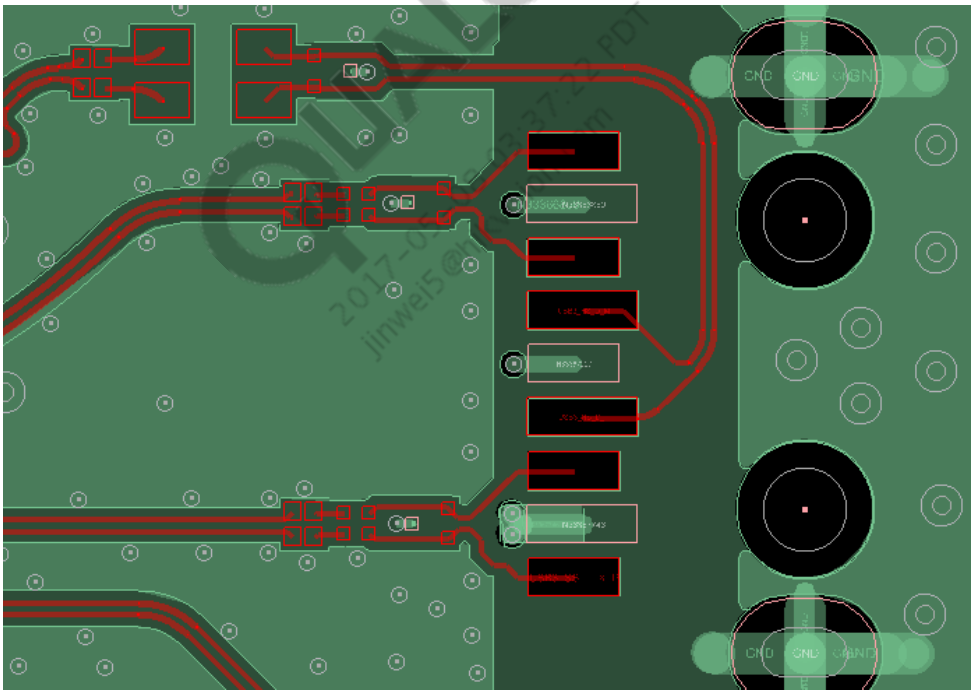


Figure 3-7 USB routing at connectors showing cutouts under SMD signal pads

NOTE: In implementations of designs with radio or WLAN modules, it is recommended to maximize the separation of the USB 3.0 routing from these sections. Adverse co-location of these interfaces has been seen to elevate the noise floor of the radio spectrum in the 2.4 GHz band.

Layout rules

- Spatial isolation of the USB connector and device from the antennas significantly mitigates the issue. This can be implemented by careful placement of the USB and the RF circuitry and antennas relative to each other.
- Merging Chassis GND to digital GND significantly mitigates the issue.
- Pour GND between the USB connectors as well and ensure good isolation to the super speed lines.
- The use of SMD connectors has considerable impact.
- Use of common-mode chokes on the USB lines has some impact.
- Routing the antenna connectors/cables for antennas should be optimal.
- Where required, covering/enclosing the USB connector especially with absorptive material mitigates the issue. Use of shielded connectors may be considered.

3.7 I²C

The I²C port is optional designed on GPIO[1:0] and used for interfacing to EEPROM as with the reference design. No other connectivity has been provided in the reference design.

NOTE:

The I²C function can be enabled by either of the following ways:

- Configure GPIO[1:0] as normal GPIO function. The I²C is simulated by software.
- GPIO[59:58] provides the I²C controller function. If these two GPIOs are not used, the I²C function can be enabled.

Table 3-15 I²C design guidelines

Category	Guidelines/Remarks
Signal/group	I2C_SDA, I2C_SCL
Spacing	As open drain signaling is used by the interface these signals are susceptible to crosstalk from strongly driven aggressors. A spacing of 2W is recommended at a minimum from other signals.
Loading	Run the traces short to the devices and reduce capacitive load.
Voltage	3.3V logic

3.8 SPI

The AP.DK01 reference design implements a dual footprint flash memory interface that supports both an 8-pin and 16-pin SO package. The SPI controller operates at 25 MHz on this interface. The flash used on the reference design by default is a 32 MByte part in the 16-pin SO footprint. AP.DK01 boot from this SPI memory for which suitable bootstraps need to be selected.

The recommended SPI Flash memory is stated in table below.

Table 3-16 SPI flash memory used in AP.DK01

Company	Device
Winbond	W25Q256FVFG
Macronix	MX25L25635FMI

The GPIO[57:54] is connected to an SPI NOR/NAND Flash in the reference design.

Table 3-17 SPI design guidelines

Category	Guidelines/Remarks
Signal/group	SPI_MOSI, SPI_MISO, SPI_CLK, SPI_CS
Route type	Single-ended 50 Ω Z controlled trace.
Spacing	2 W spacing is recommended especially for SPI_CLK
Length	Run the traces short to the devices; keep within 5 inches
Length match	Overall length match between the group (MISO, MOSI, CLK and CS) is recommended to be within 500 mils
Voltage	3.3V logic
Other	A moderate pull-up is recommended on the chip select line SPI_CS at the flash device

3.9 UART

AP.DK01 implements a UART console with GPIO[61](RXD), GPIO[60](TXD).

3.3V interface 12-pin connector at J19.

3.10 DDR3L DRAM

IPQ4018/IPQ4028 supports a 16-bit DDR3L memory interface with the memory capacity up to 256 Mbytes. AP.DK01 implements a DDR3L memory with speed of 1075.2 MT/s data rate and 537.6 MHz clock rate. The DDR3L interface is implemented using the devices listed in Table 3-18.

Table 3-18 DDR3L memory used in AP.DK01

Company	Device
Micron	MT41K128M16JT-125 256MB
EtronTech	EM6HD16EWXC-15H 256MB
Winbond	W632GU6KB-12 256MB

The command address (CA) bus and data bus are routed in point-to-point topology, as shown in Figure 3-8. VTT terminations are used for CA lines.

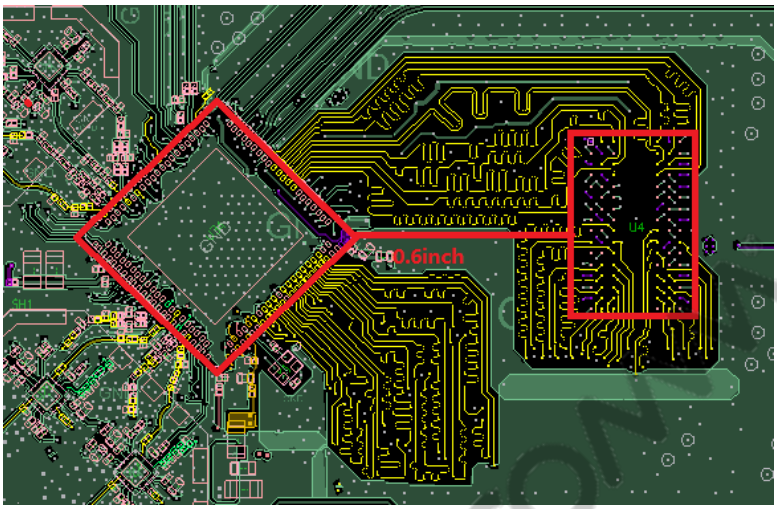


Figure 3-8 DDR3L routing topology

The design guidelines are summarized in Table 3-19.

Table 3-19 DDR3L DRAM design guidelines

<table>
<tr><th>Category</th><th colspan="3">Guidelines/Remarks</th></tr>
<tr><td rowspan="8">Groups</td><td>Group</td><td colspan="2">Signals</td></tr>
<tr><td colspan="3">Differential pairs</td></tr>
<tr><td>Clock</td><td colspan="2">DDR3_CLK_N, DDR3_CLK</td></tr>
<tr><td>DQS0</td><td colspan="2">DDR_DQS_0, DDR_DQS_N_0</td></tr>
<tr><td>DQS1</td><td colspan="2">DDR_DQS_1, DDR_DQS_N_1</td></tr>
<tr><td colspan="3">Single-ended</td></tr>
<tr><td>DDR_CA group</td><td colspan="2">DDR_ADDR_[13:0], DDR_BA_[2:0], DDR_CAS_N, DDR_WE_N, DDR_ODT, DDR_RAS_N, DDR_RST_N</td></tr>
<tr><td>DDR_DQ byte0</td><td colspan="2">DDR_DQ_[7:0], DDR_DQM_0</td></tr>
<tr><td>DDR_DQ byte1</td><td colspan="2">DDR_DQ_[15:8], DDR_DQM_1</td></tr>
<tr><td>Route type</td><td colspan="3">Differential pairs: 100 Ω differential impedance
Single-ended signals: 60 Ω impedance</td></tr>
<tr><td>Return path</td><td colspan="3">Ensure continuous and unbroken return path without voids</td></tr>
<tr><td>Length</td><td colspan="3">It is recommended to keep the routed length to within 3 inches for the CA group.
It is recommended to route DQ lanes as short as possible and keep within 2 inches.</td></tr>
<tr><td rowspan="8">Length match rules</td><td colspan="3">Use the following length match per group:</td></tr>
<tr><td colspan="2">Signal type</td><td>Length-match within</td></tr>
<tr><td colspan="2">DQ,DM,DQS (within group)</td><td>±50 mils</td></tr>
<tr><td colspan="2">DQS-to-DQSB (intra-pair)</td><td>±5 mils</td></tr>
<tr><td colspan="2">CA-to-CK</td><td>400 mils</td></tr>
<tr><td colspan="2">CK-to-CKB (intra-pair)</td><td>±5 mils</td></tr>
<tr><td colspan="2">DQS-to-CK</td><td>≤ 600 mils</td></tr>
<tr><td colspan="3">Note: The length match includes via lengths in the trace match. The groups should be formed with vias accounted for.</td></tr>
<tr><td>Vias/layer transitions</td><td colspan="3">Minimize layer transitions where necessary limit to 2 vias per signal trace.</td></tr>
<tr><td>VREF</td><td colspan="3">▪ Use a 1 K 1% resistor divider with accompanying 0.1 µF filter to each rail, collocated with a small copper pour. Route thick short trace from this island to the VREF pins
▪ Keep a 2 w spacing from the trace to its neighbors
▪ Separate dividers can be used, one close to the IPQ4018/IPQ4028 device; one close to DDR_VREFCA; one close to DDR VREF_DQ.</td></tr>
<tr><td>ZQ/Cal resistors</td><td colspan="3">For DDR devices it is recommended to place the 240 Ω resistor close to the device ball and route to GND with a 2 W separation.</td></tr>
<tr><td>Decoupling and power layout</td><td colspan="3">▪ Provide individual 0201 capacitors per pin for the VDDQ and VDDL close to the pins
▪ Connect them up with minimal inductance on both Vdd and GND paths
▪ Provide one bulk capacitor of 10uF at least</td></tr>
<tr><td>Voltage</td><td colspan="3">1.35 V
The reference design is currently populated and validated with DDR3L devices.</td></tr>
</table>

Chip internal wire length must be take into consideration for PCB length match.

DDR ADD/CMD	Internal wire (mm)
DDR_A_0 [ADD/CMD]	2.94978
DDR_A_1 [ADD/CMD]	2.15036
DDR_A_2 [ADD/CMD]	2.17391
DDR_A_3 [ADD/CMD]	2.30093
DDR_A_4 [ADD/CMD]	2.76054
DDR_A_5 [ADD/CMD]	2.21861
DDR_A_6 [ADD/CMD]	2.64558
DDR_A_7 [ADD/CMD]	1.98181
DDR_A_8 [ADD/CMD]	1.91783
DDR_A_9 [ADD/CMD]	2.58019
DDR_A_10 [ADD/CMD]	2.58019
DDR_A_11 [ADD/CMD]	2.68464
DDR_A_12 [ADD/CMD]	2.12251
DDR_A_13 [ADD/CMD]	2.5994
DDR_BA_0 [ADD/CMD]	2.23048
DDR_BA_1 [ADD/CMD]	3.15108
DDR_BA_2 [ADD/CMD]	2.43637
DDR_CAS_N [ADD/CMD]	2.44316
DDR_CKE_M [ADD/CMD]	2.99166
DDR_CK_N [ADD/CMD]	2.56815
DDR_CK_P [ADD/CMD]	2.20831
DDR_ODT [ADD/CMD]	2.98912
DDR_RAS_N [ADD/CMD]	2.88528
DDR_WE_N [ADD/CMD]	2.72825
DATA0	
DDR_DM_0 [DATA0]	2.00851
DDR_DQSN_0 [DATA0]	1.97762
DDR_DQS_0 [DATA0]	2.01239
DDR_DQ_0 [DATA0]	1.98664
DDR_DQ_1 [DATA0]	1.97075
DDR_DQ_2 [DATA0]	1.95946
DDR_DQ_3 [DATA0]	1.95983
DDR_DQ_4 [DATA0]	2.06326
DDR_DQ_5 [DATA0]	2.1291
DDR_DQ_6 [DATA0]	2.20855
DDR_DQ_7 [DATA0]	2.30021
DATA1	
DDR_DM_1 [DATA1]	2.08664
DDR_DQSN_1 [DATA1]	2.51423

DDR ADD/CMD	Internal wire (mm)
DDR_DQS_1 [DATA1]	2.63445
DDR_DQ_8 [DATA1]	2.13185
DDR_DQ_9 [DATA1]	2.20825
DDR_DQ_10 [DATA1]	2.29987
DDR_DQ_11 [DATA1]	2.4023
DDR_DQ_12 [DATA1]	2.76187
DDR_DQ_13 [DATA1]	2.89554
DDR_DQ_14 [DATA1]	3.03464
DDR_DQ_15 [DATA1]	3.21673

3.11 JTAG interface

AP.DK01 uses a 20-pin header J21 to connect ICE (Lauterbach©) to debug ARM CPU. Note: The JTAG connector of the debug cable is not suitable for hot plug-in.

Table 3-20 JTAG debug interface design guidelines

Category	Guidelines/Remarks
Signals/Group	JTAG_TRST_N, JTAG_TDI, JTAG_TDO, JTAG_TMS, JTAG_TCK, JTAG_RST_N (SRST)
Mechanical	Ensure sufficient clearance for placement of debug headers
Spacing	2 W spacing is desirable
Routing	Route short (<5 inch) and direct traces with impedance control
Length match	No critical requirement; it is recommended to keep the signals matched within 500 mils
Voltage	Operates at 3.3 V; the PowerTrace debugger can be connected directly

3.12 GPIOs

The IPQ4018/IPQ4028 has a total of 18 GPIO pins. Many of these GPIOs are multiplexed with other functionality as described in Table 3-21, such as JTAG, MDIO/MDC, SPI and UART.

There are no critical guidelines for routing generic GPIO signals that connect to switches, LEDs, interrupts, and so on.

Table 3-21 GPIO function description

GPIO	AP.DK01 default configuration	Default configurable function description
0	TDI	JTAG TDI
1	TCK	JTAG TCK
2	TMS	JTAG TMS
3	TDO	JTAG TDO
4	JTAG_RST_N	JTAG SRST
5	JTAG_TRST_N	JTAG TRST
52	MDC	SMI MDC

GPIO	AP.DK01 default configuration	Default configurable function description
53	MDIO	SMI MDIO
54	SPI_CS	SPI CS
55	SPI_MOSI	SPI MOSI
56	SPI_CLK	SPI CLK
57	SPI_MISO	SPI MISO
58	WIFI LED	GPIO
59	QCA8075 reset	GPIO
60	RXD	UART RXD
61	TXD	UART TXD
62	SYS_RST_L	Chip reset out for 32MB NOR Flash reset
63	CHIP_IRP_IN	GPIO button input

4 Power

4.1 Power rails

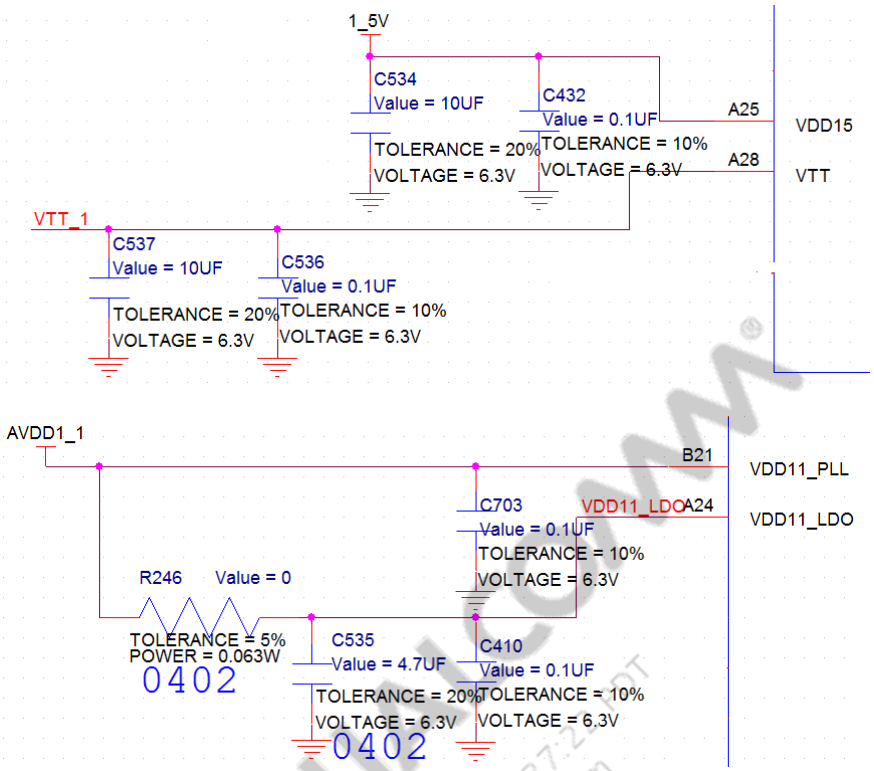
There are four low power rails in AP.DK01:

- 12V to 5V for USB operation
- 12V to 1.35V for IPQ4018/IPQ4028 1.35V DDR3L
- 12V to 3.3V for IPQ4018/IPQ4028 VDD33, 2.4 GHz and 5 GHz FEM, and QCA8075
- 12V to 1.1V for IPQ4018/IPQ4028 2.4 GHz and 5 GHz radio

Refer to HDK for detailed power rail and regulator design.

4.2 Internal regulators in IPQ4018/IPQ4028

- One VTT LDO, 120mA, providing common mode voltage for DDR3 CA pads
- PLL LDO provides 1.1V power for PLLs, including PSGMIIPLL_AVDD/USB1_PLL/USB1_AVDD11_RX/USB1_AVDD11_TXCLK/AVDD_PLL/AVDDVCO, drivability is 130mA
- 2.7V LDO, 20mA, only for BIAS generator



4.3 Power sequencing

The IPQ4018/IPQ4028 devices must be powered up in a definite sequence to ensure safe and reliable operation. Figure 4-1 shows the details on power sequencing for an IPQ4018/IPQ4028 system.

- The power rails must follow the sequence: VDD33 > VDD135 > VDD11 ≥ AVDD11.
- Keep asserting CHIP_PWD_L low for at least 10ms to get reliable warm hardware reset.

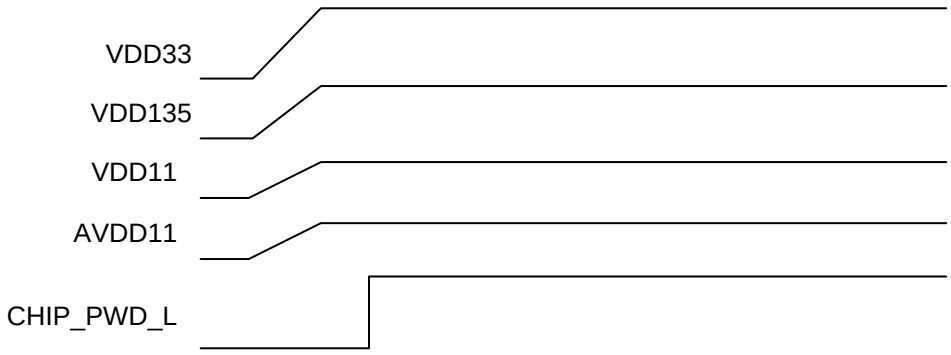


Figure 4-1 Power sequencing for an IPQ4018/IPQ4028 system

A power up RC (10k/1uF) circuit is suggested as shown in Figure 4-2.

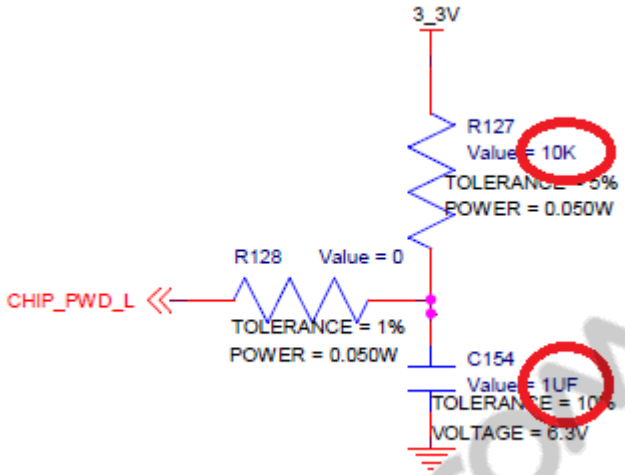


Figure 4-2 Recommended power-up RC circuit

NOTE: It is acceptable to power down the system without a particular sequence. However, ensure a reasonable time to the next power-on to verify that the rails have drained so the subsequent power-on will not violate the power sequence.

It is recommended to keep the power off for a few seconds for this purpose.

4.4 Qualcomm® Internet Processor (IPQ) decoupling

Table 4-1 shows the recommended IPQ4018/IPQ4028 decoupling values.

Table 4-1 Recommended IPQ4018/IPQ4028 decoupling values

IQP rail	Voltage (nominal)(V)	Capacitance value	Quantity
VDD11	1.1	10 uF	1
		4.7 uF	2
		0.1 uF	11
USB1_AVDD11_TXCLK USB1_PLL USB1_AVDD11_RX	1.1	0.1 uF 0.1 uF 0.1 uF	1 1 1
VDD11_ADDAC	1.1	4.7 uF	1
		0.1 uF	1
		1 nF	1
VDD11_BB	1.1	4.7 uF	1
		0.01 uF	1
VDD11_BIAS	1.1	0.01 uF	1
VDD11_CLKBUF	1.1	47 uF	2
		0.1uF	1
VDD11_LO	1.1	10 uF	1
		4.7 uF	1
		0.01 uF	1
		10 pF	1
VDD11_ADDAC_R1	1.1	4.7 uF	1
		0.1uF	1
		1nF	1
VDD11_BB_R1	1.1	0.01uF	1
VDD11_BIAS_R1	1.1	0.01uF	1
VDD11_LO_R1	1.1	4.7 uF	1
		0.01 uF	1
		10 pF	1
VDD11_PLL	1.1	0.1 uF	1
VDD11_LDO	1.1	4.7 uF	1
		0.1 uF	1
VDD11_T/RX_CH0 VDD11_T/RX_CH1	1.1	1 uF	1
		0.01 uF	4
VDD11_T/RX_CH2 VDD11_T/RX_CH3	1.1	0.01 uF	4
VDDIO	3.3	1 uF	1
		0.01 uF	1
VDD15	1.5	10 uF	1
		0.1 uF	1
VTT	0.75	10 uF	1

IQP rail	Voltage (nominal)(V)	Capacitance value	Quantity
		0.1 uF	1
VDD33_BB VDD33_PMU	3.3	10 uF	1
		0.1 uF	1
VDD33_PLL	3.3	0.1 uF	1
		10 pF	1
VDD33_SYN	3.3	0.1 uF	1
VDD33_VCO	3.3	4.7 uF	1
		0.01 uF	1
		10 pF	1
VDD33_BB_R1	3.3	0.01 uF	1
VDD33_PLL_R1	3.3	2.2 uF	1
		0.1 uF	1
VDD33_SYN_R1	3.3	10 pF	1
VDD33_VCO_R1	3.3	4.7 uF	1
		0.01 uF	1
		10 pF	1
VDD33_XO	3.3	0.01 uF	1
DDR_VDDQ	1.5	10 uF	1
		0.1 uF	5
VDDIO	3.3	0.1 uF	2
AVDD_PLL	1.1	0.1 uF	1
AVDD25_REG	2.62	1 uF	1
		0.1 uF	1
AVDDVCO	1.1	0.1 uF	1
USB1_DVDD11_RX USB1_AVDD11 USB1_AVDD11_TX	1.1	0.1 uF	3
USB1_AVDD11_RX USB1_PLL	1.1	0.1 uF	2
USB1_AVDD33	3.3	0.1 uF	1
USB1_AVDD33	3.3	0.1 uF	1
USB2_AVDD11	1.1	10 uF	1
PSGMIIRX_AVDD PSGMIITX_AVDD	1.1	0.1 uF	3
PSGMIIPLL_AVDD	1.1	0.1 uF	1

NOTE: Detailed configurations will be updated based on final test result.

See Figure 4-3 for the recommended layout for the decap vias: short wide connections to vias as close as possible using a symmetric pattern minimizing the inductance on both power lead and GND lead. Where possible, 0201 components can be inlined with the vias. 0402 components can be placed side-on.

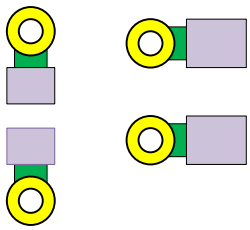


Figure 4-3 Via placement for decaps (0201, 0402)

While it is possible to use multiple vias to reduce inductance, it is not recommended due to the adverse impact on the copper plane area in the inner layers. In severely constrained areas it may even be necessary to share vias across two capacitors.

5 Thermal Considerations

Careful consideration is required of the thermal dissipation on the system board taking the power dissipation of the IPQ4018/IPQ4028 and other system peripherals into account. Thermal simulation is recommended.

5.1 IPQ thermal characteristics

Table 5-1 lists the thermal characteristics of the IPQ4018/IPQ4028.

Table 5-1 IPQ4018/IPQ4028 thermal characteristics

Device	Package configuration	Junction-to-Case thermal resistance θJC (°C/W)	Junction-to-Board thermal resistance θJB (°C/W)	Junction-to-Ambient thermal resistance θJA (°C/W)
IPQ4018/ IPQ4028	180-pin 14*14 DRQFN	4.5	13.3	19.3
		▪ JESD51-7, JESD51-8 ▪ Cu block at top of package maintained at 25C ▪ No thermal vias	▪ JESD51-7, JESD51-8 ▪ Cold plate ring maintained at 25C at top and bottom of PCB	▪ JESD51-2A, JESD51-7

5.2 System thermal characteristics

The thermal dissipation of the system should be budgeted taking into consideration the overall loads including other devices, the board design, and enclosure design and is implementation-specific. Try to keep complete copper plane and enough thermal vias.

Thermal simulation is required. See related Device Specification for chip power consumption data.

Exposed-pad QFN packages conduct approximately 80% of the heat though the bottom of the package and into the PWB. As shown in Figure 5-1, heat flow is from the QFN ground pad > thermal vias > backside ground plane > TIM > heatsink > air.

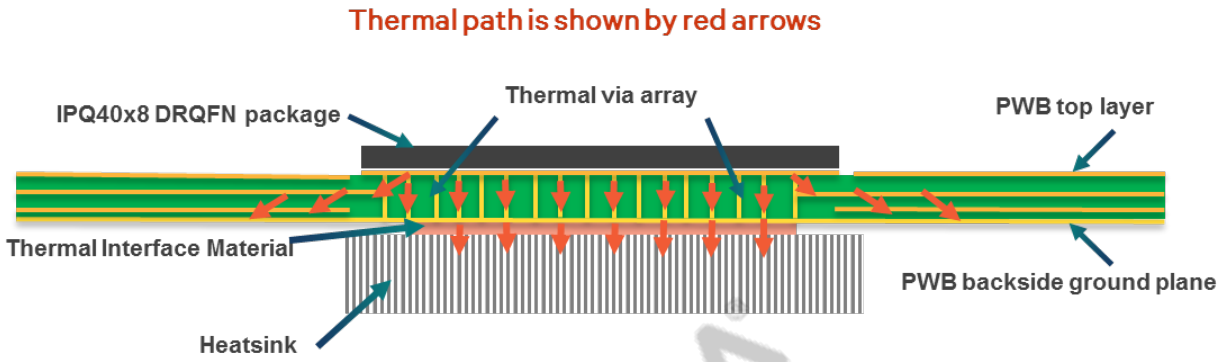


Figure 5-1 IPQ4018/IPQ4028 board cross-section view

5.2.1 Heatsink and thermal interface material (TIM)

- Heatsink increases cooling surface area when connected to the backside of the board.
- TIM ensures proper contact and transfer of heat from board to heatsink.
- Clear the solder resist on bottom layer of PCB to expose copper for better conduction of heat to the TIM.

5.2.2 AP.DK01 thermal solution

- An extruded aluminum heatsink is attached to the bottom of the board with TIM sandwiched between the board and heatsink.
- Heatsink surface area is 175 cm^2, which is used to dissipate about 7 W of power.
- TIM is T-Global 6050 with thermal conductivity of 6 W/m-K.
- TIM can be placed as small blocks under IPQ4018/IPQ4028 and each RFPA.

5.2.3 PWB construction

- The more copper the PWB contains, the better the thermal performance.
- Maximize the size and number of thermal vias under the QFN devices. The AP.DK01 includes many filled vias on the GND pad for IPQ4018/IPQ4028, and puts vias on the GND pad for RF FEM (RFFM8228P and SKY85716).
- Maximize the exposed ground plane area on the back side of the PWB.

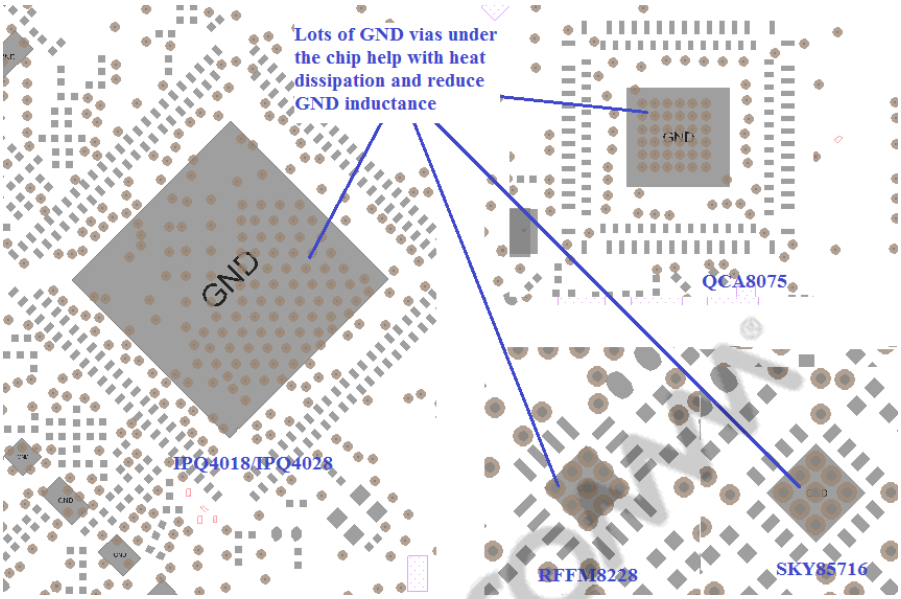


Figure 5-2 AP.DK01 thermal considerations

6 RF design

6.1 AP.DK01 RF block description

AP.DK01 RF front end parts include:

- 2.4 GHz and 5 GHz RF FEM, in this case, the default RF FEM selections are Skyworks SKY85716 for 5 GHz and Qorvo RFFM8228P for 2.4 GHz
- RF filters, including 2.4 GHz RF BPF, 5 GHz RF BPF, and other T or pi networks

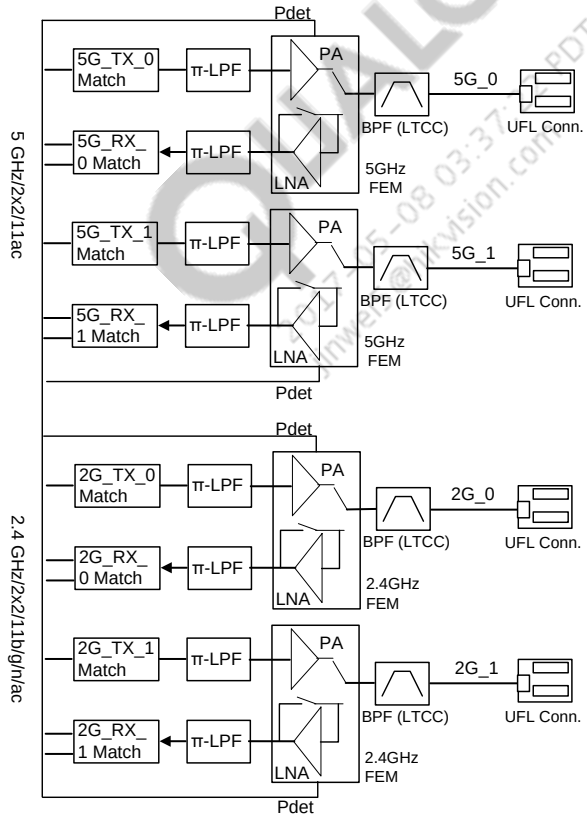


Figure 6-1 AP.DK01 RF block diagram

6.1.1 2.4 GHz external FEM (PA/LNA/SPDT RF switch)

Each transmit radio chain has an external power amplifier (PA) inside FEM to increase WLAN rates over range and WLAN coverage beyond the capabilities of the internal PA. The Qorvo RFFM8228P provides a system mask compliance output power above 20 dBm for HT20/40 rates and can exceed 15 dBm of Tx power for the highest modulation rate of 256 QAM, 5/6 encoding and 40 MHz bandwidth (VHT40 MSC9).

Each receive radio chain has an external LNA inside FEM to increase receive dynamic range and sensitivity beyond the capabilities of the internal LNAs of the IPQ4018/IPQ4028.

The Tx/Rx switch inside FEM is used to toggle the antenna back and forth between transmit and receive. Also, an additional SPDT switch for selection between LNA on and Bypass in Receive mode. All the impedance matching components and DC-block capacitors are integrated to minimize the PCB footprint for system implementation.

RFFM8228P is assembled in an ultra-compact, low-profile 2.3x2.3x0.45mm 16L QFN package and requires minimal external components.

6.1.2 5 GHz external FEM (PA/LNA/SPDT RF switch)

Skyworks SKY85716 is used to serve 5GHz RF operation. SKY85716 is a fully matched, with integrated 5 GHz PA with harmonic, LNA with bypass mode and SPDT switch. This FEM is integrated, positive slope logarithmic power detector. Detector.

- Single 3.3V power supply
- High-power and Power-save modes
- Transmit gain: 30 dB
- Receive gain: 11 dB
- Output power: +17.5 dBm, MCS7, HT20
- Output power: +16 dBm, MCS9, HT80
- Small, QFN (16-pin, 2.3 x 2.3 x 0.33 mm) package

6.1.3 2.4 GHz Band Pass filter

The Murata LFB212G45CN1E205 band pass filter (BPF) is used to filter out the high 2/3 LOs, 4/3 LOs leaked from the IPQ4018/IPQ4028, and to retain some of the spurs that fall in restricted bands below the FCC limit (-41 dBm/MHz in conducted 50 Ω system or 500 µV/m at 3 mts in field strength). This BPF is used to filter out the 5 GHz radio for DBDC.

6.1.4 5 GHz Band Pass filter

The WALSIN RFBPF1608060KC8Q1C band pass filter (BPF) is used to filter out the high 2/3 LOs, 4/3 LOs leaked from the IPQ4018/IPQ4028, and to retain some of the spurs that fall in restricted bands below the FCC limit (-41 dBm/MHz in conducted 50 Ω system or 500 µV/m at 3 mts in field strength). This BPF is used to filter out the 2.4 GHz radio for DBDC.

6.1.5 Power detector on FEM

Vdet of FEM is used for Close-Loop power control (CLPC) operation. Tx power accuracy depends on FEM's Vdet curve, where 250 to 750mV relative linear Vdet curve is expected at input of IPQ40x8 to cover the total expected Tx output power range.

6.1.6 Optimizing Tx EVM by separating AVDD1_1_5G power supply

The MPS MP1498DJ-LF DC regulator is reserved in AP.DK01 design. It is an option to supply the AVDD1_1_5G separately. The 5G's Tx EVM floor can be optimized by this option.

Test results indicate that separating AVDD1_1_5G from other power supplies improves 0.5dB Tx output power@5G with EVM compliant.

BOM changes on AP.DK01 (DP25-YB021-2/DP25-YB021-4) for this modification:

- Load U32, part number: MPS MP1498DJ-LF

  Requirement of Regulator specifications:

  - Switching frequency at least 1.0 MHz
  - Output current at least 2.0 A
- R437 = NL and R487 = 0 ohm

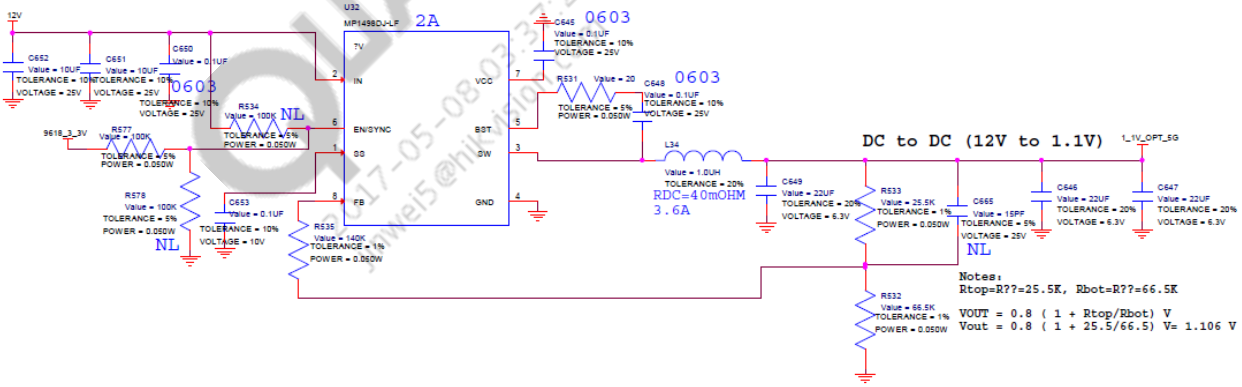


Figure 6-2 AVDD1_1_5G DC regulator

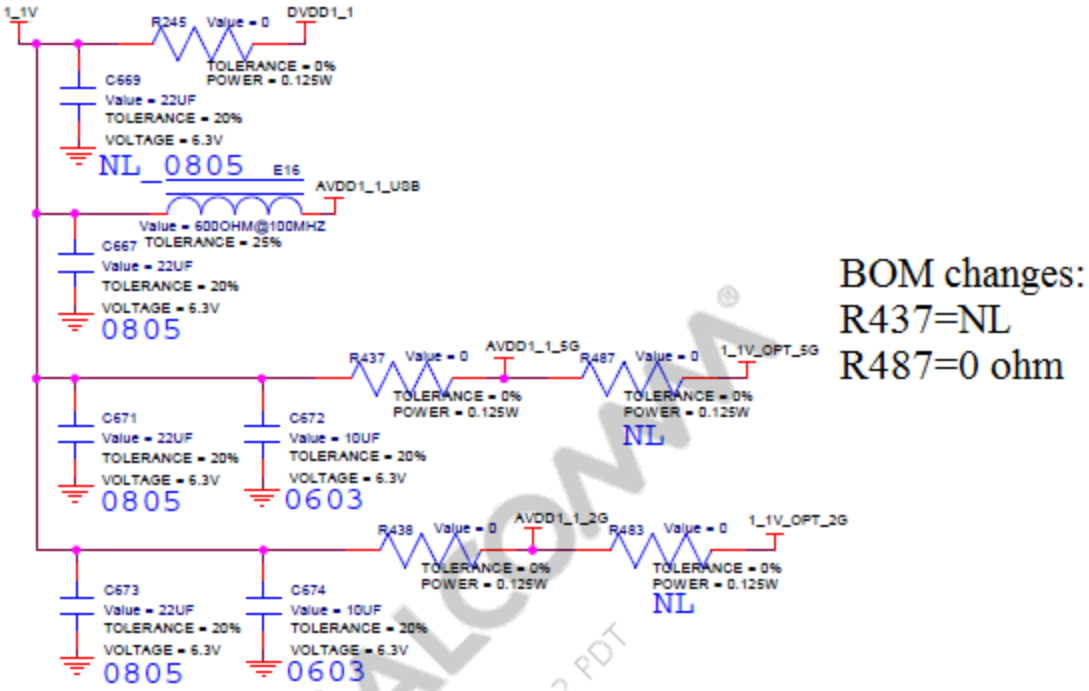


Figure 6-2 BOM changes for applying 1_1V_OPT_5G to AVDD1_1_5G

6.2 RF layout guidelines

6.2.1 RF traces

- All RF, Rx, and Tx traces must be 50 Ω. Qualcomm Atheros recommends all RF components and traces to be on the same side of the board.
- Via should be avoided in the RF traces as much as possible. Do not use any test points on any RF traces or component.
- Place Ground plane with enough asymmetric via close to RF trace.
- Ground via should be close to component pad as possible.
- Minimize the length of all RF traces since FR4 material incurs losses at RF frequencies. Minimizing trace length reduces the overall signal loss.
- With the AP.DK01 stackup, the 50 Ω trace is an 7-mil wide Microstrip on the top layer reference to the GND plane on the second layer and bottom layer reference to the GND plane on the 3rd layer.

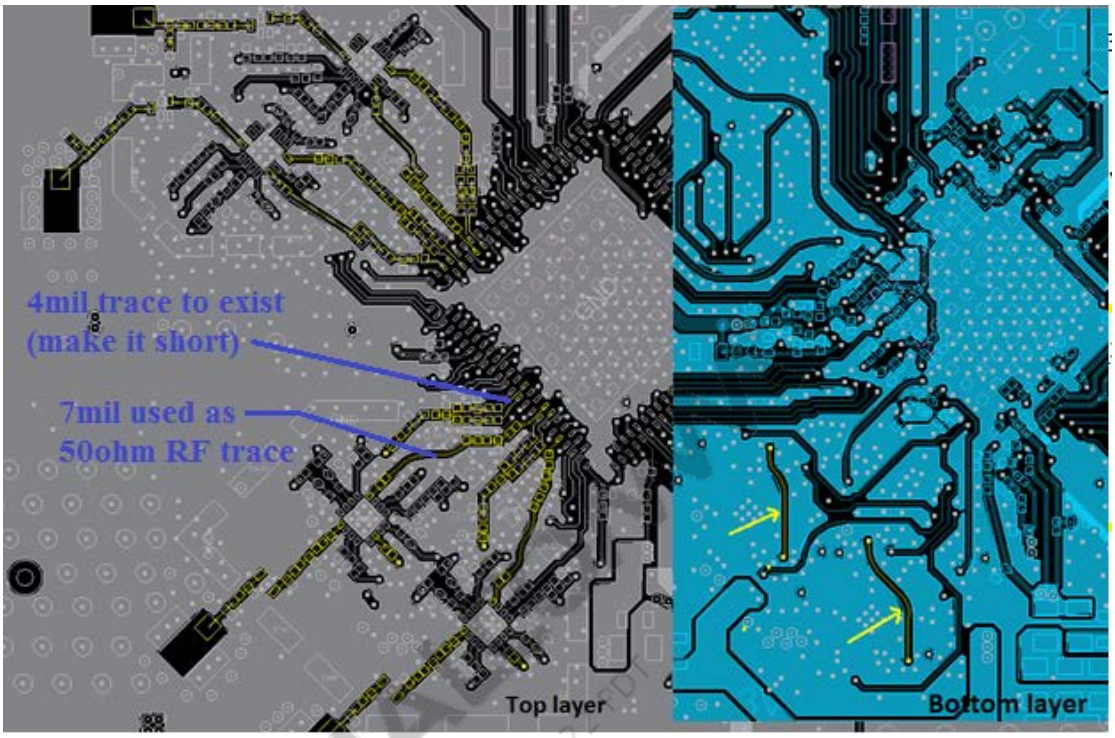


Figure 6-3 AP.DK01 RF traces

6.2.2 RF connector

Because the RF signal passes from an on-board RF trace to the middle pin of RF connector, the diameter of that pin is much thicker than RF trace that requires the reference GND be further away. Do not put metal under the U.FL connectors on layer 1 and 2. Make sure that the ground is present on all other layers of the board.

Do not put metal under the U.FL connectors (J11/J12/J13/J14) on layer 1~2. Make sure that the ground is present on all other layers of the board to keep 50ohm impedance control.

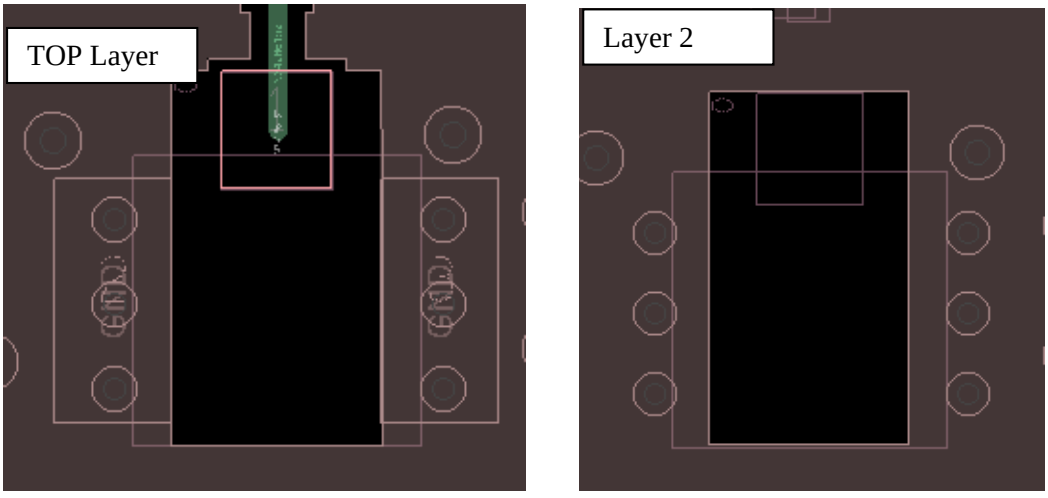


Figure 6-4 AP.DK01 RF connectors

6.2.3 FEM's Power Detector output traces

Treat these Paths as voltage signals. Keep isolation with other signals by Ground and a wider trace width is expected.

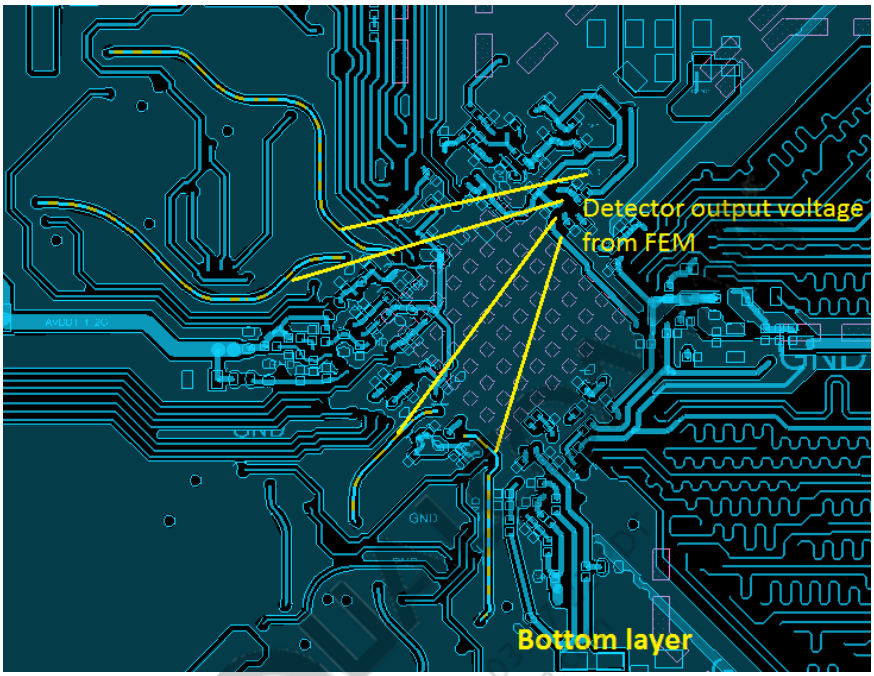


Figure 6-5 FEM's power detector output

6.2.4 Discrete Balun on Rx

The wrong placement of those 6 components can easily degrade Rx performance, thus the best approach is to follow the exact placement from the reference design and keep the whole circuit tight and close to IPQ4018/IPQ4028.

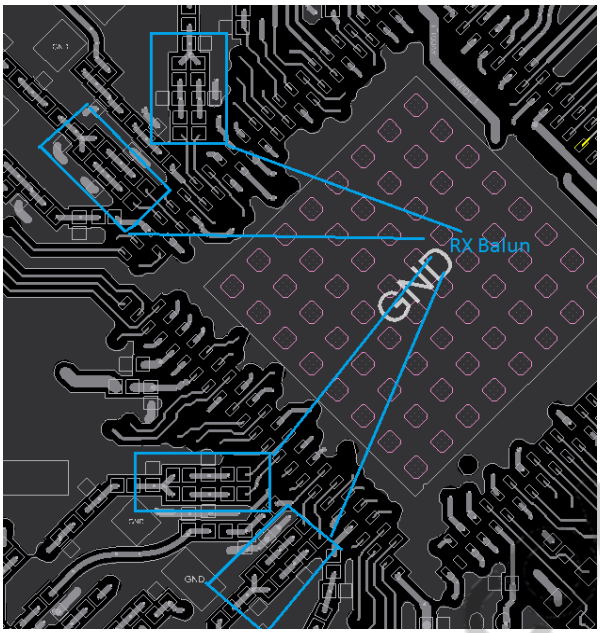


Figure 6-6 Rx balun

6.2.5 Matching circuit on Tx

Place the matching circuit (3 components) tight and close to IPQ4018/IPQ4028 output PINs.

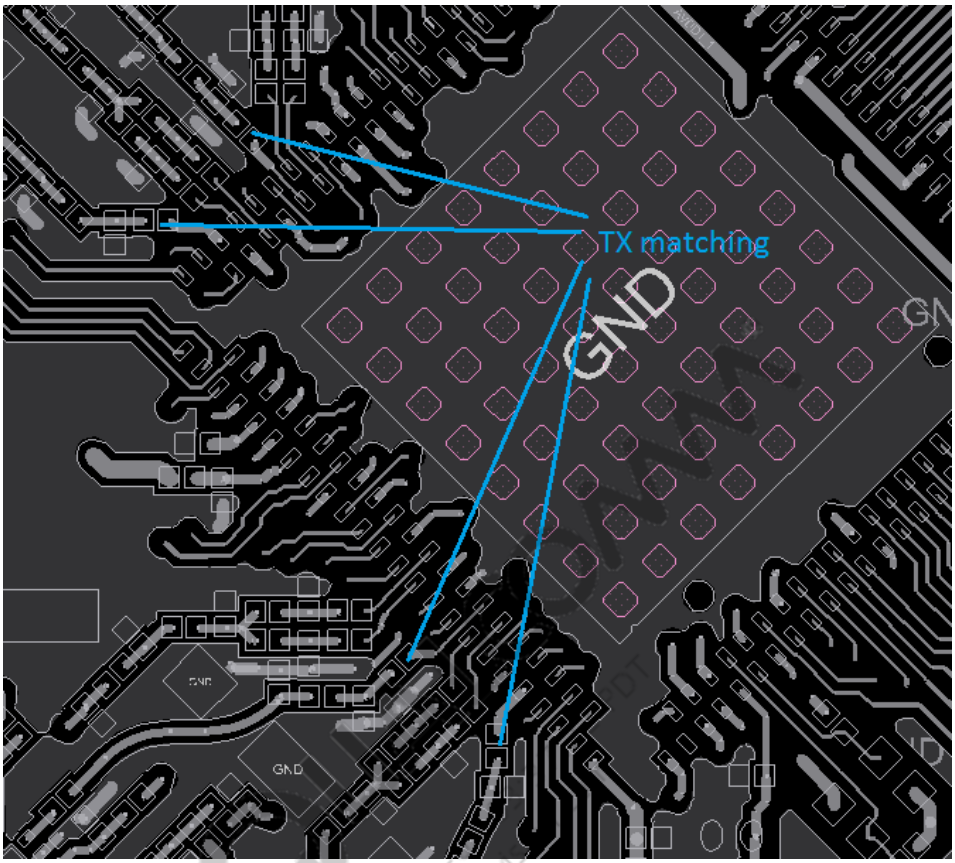


Figure 6-7 Tx matching circuit

6.2.6 Layout guidelines for power supply of IPQ4018/IPQ4028

Route the power supply of AVDD1_1, AVDD1_1_2G, AVDD1_1_5G, AVDD1_1_USB, 3_3V_2G and 3_3V_5G by star topology. The placement of decoupling capacitors follow the AP.DK01 as far as possible. The decoupling capacitor should be placed as close to the power pins as possible and with minimal trace length to avoid inductance. In addition, avoid long GND trace for the decoupling capacitor's GND, and provide quick via to GND plane rather than a long trace.

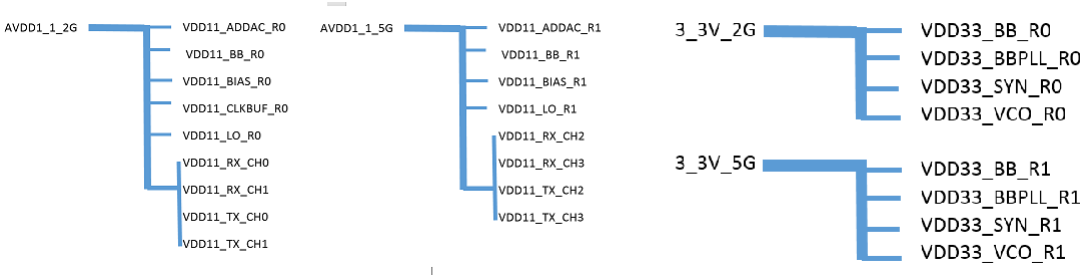


Figure 6-7 Analog power supply on IPQ4018/IPQ4028

The placement priority of decoupling capacitors:

- AVDD1_1
- 3_3V_2G and 3_3V_5G

- DVDD1_1, 9618_3_3V and others

The smaller decoupling capacitors (such as 10 pF) in schematic shall be placed close to IPQ4018/IPQ4028 pins.

Most Power supply are routing on layer 3 and bottom layer, stay away from 48 MHz crystal areas. Only a few power supply domains can be on the top layer; follow AP.DK01 as far as possible.

6.2.7 RF shields

RF shields are required for adequate operation of the AP.DK01 reference design. The shield compartments can prevent radio-to-radio coupling.

Places 5G and 2.4G in difference shields to reduce the coupling between each other.

The number of shield openings must be reduced to a minimum needed, that is, for routing the RF traces to connect to the antenna connector. The shield openings should be as small as possible to reduce leakage.

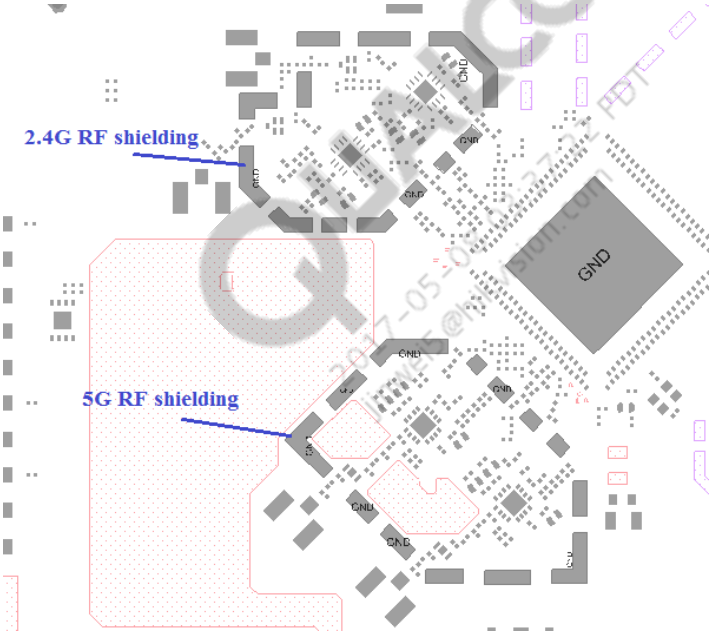


Figure 6-8 Shielding case on AP.DK01

6.2.8 Additional guidelines

- Use at least 0805 size 0-Ω for the AVDD11 and DVDD11 power source.
- Avoid using a thin trace for AVDD11 and DVDD11.
- Avoid an overlap between 3_3V_2G/5G and the AVDD11 power plane.
- Avoid an overlap between VDD11_LDO and the AVDD11 power plane.
- Avoid an overlap between the AVDD11 power plane and all four XLNA_0/1 signal traces on the nearby layers.

- Separate the power source between 3_3V_2G_FEM and 3_3V_5G_FEM. Avoid an overlap between 3_3V_2G_FEM and 3_3V_5G_FEM.
- Avoid the coupling between AVDD11 and IPQ40x8 RF input traces.
- Avoid the coupling between DVDD11 and IPQ40x8 RF input traces.
- Avoid the coupling between XLNA_0/1 lines and IPQ40x8 RF input traces.
- Avoid routing 3_3V_2G_FEM, 3_3V_5G_FEM and VDD11 on top layer or bottom layer.

6.3 Antenna placement on the AP

This section lists the recommendations to optimize antenna performance when using external dual-band dual-feed antennas.

- Maximize physical separation of all antennas.

  The minimum separation distance is 60 mm or 2.5 inches to get the minimum 15-dB isolation. Optimum performance at 2.4 GHz is typically achieved with spacing greater than 90 mm or 3.5 inches.

- Allow the antennas to rotate so they are not all forced to remain vertical.

  Best MIMO performance is typically obtained with some polarization diversity. This frequently occurs with two antennas tilted -45 degrees from vertical and two tilted +45 from vertical.

- Locate the antennas so they are clear of obstructions and not blocked by boards, shields, heat sinks, and so on. Each antenna should have a clear omni-directional path.

- Do not locate all of the antennas in a straight line.

  This typically results in nulls in the MIMO coverage when the line through the antennas points at the client device.

- Locate the antennas away from USB3 interface PWB traces, connectors, or cables.

  Separate by 90 mm or 3.5 inches, if possible. Ideally, the USB port should be located near the center of the rear panel, thus placing the antennas on each of the corners far away from the USB port in the center. A shield cover over the USB3 traces is not required in the most recent Qualcomm Atheros designs.

- Locate the antenna away from PCIE BUS, PCIE traces, and connectors.

  Test results indicate that radiating interference from PCIE 2.0 falls into the 2.4 GHz band and will affect the 2.4 GHz radio.

- Locate the antenna away from QCA8075, PSGMII traces, and connectors.
- Antenna cable routing shall avoid high speed I/O area (PSGMII, USB3.0 PCIe2.0 and DDR).
- Separate the 2.4 GHz and 5 GHz ANT traces to get at least 20 dB isolation for DBDC mode.

7 QCA8075 Five-Port 10/100/1000 Mbps Ethernet Transceiver

The QCA8075 Ethernet transceiver is a 5-port, 10/100/1000 Mbps tri-speed Ethernet PHY.

The QCA8075 includes two SerDes. One can be configured to PSGMII or QSGMII for connection with MAC. The other can be configured to SGMII for connection with MAC or fiber port combined with copper port4 to form a combo port.

AP.DK01 application as shown in Figure 7-1, IPQ4018/IPQ4028 connects with QCA8075 through PSGMII interface which run at 6.25 Gbps.

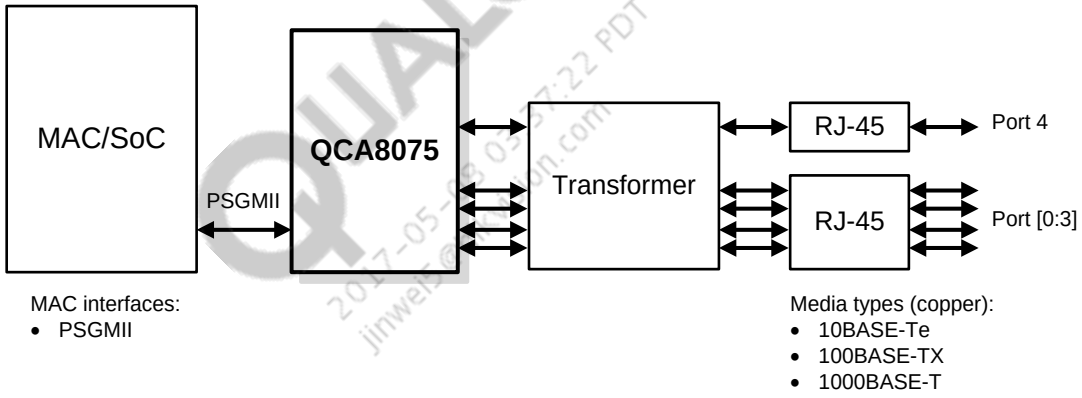


Figure 7-1 PSGMII connection

Besides PSGMII, there is MDC/MDIO, reset and clock connection between the two chips.

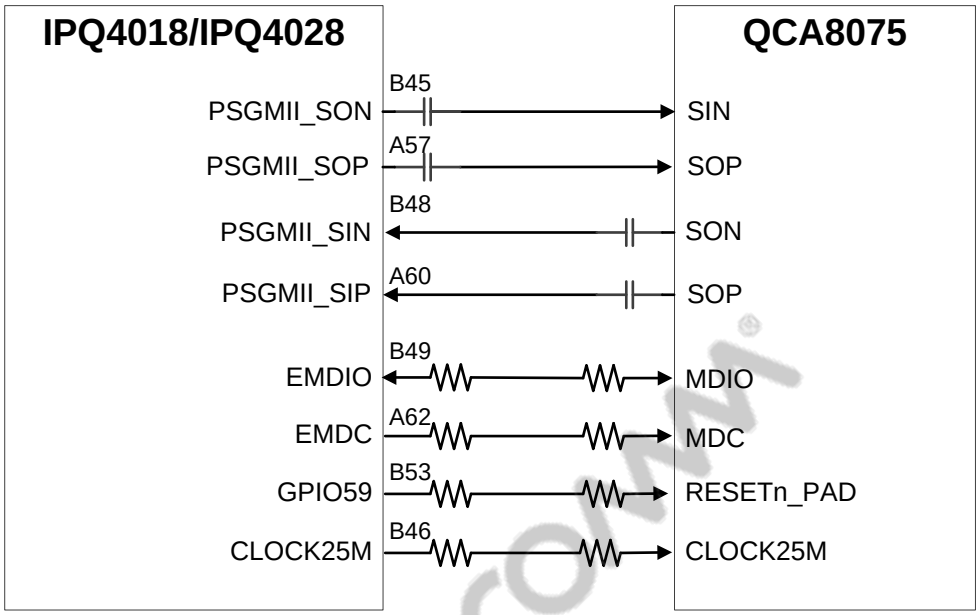


Figure 7-2 MDC/MDIO, reset and clock connection

7.1 Reset

QCA8075 requires reset signal must be asserted and kept low for at least 1ms after 3.3V power and reference clock signals become stable. 3.3V rising duration from 10% to 90% must be larger than 0.5 ms. The subsequent warm hardware reset needs at least 1ms.

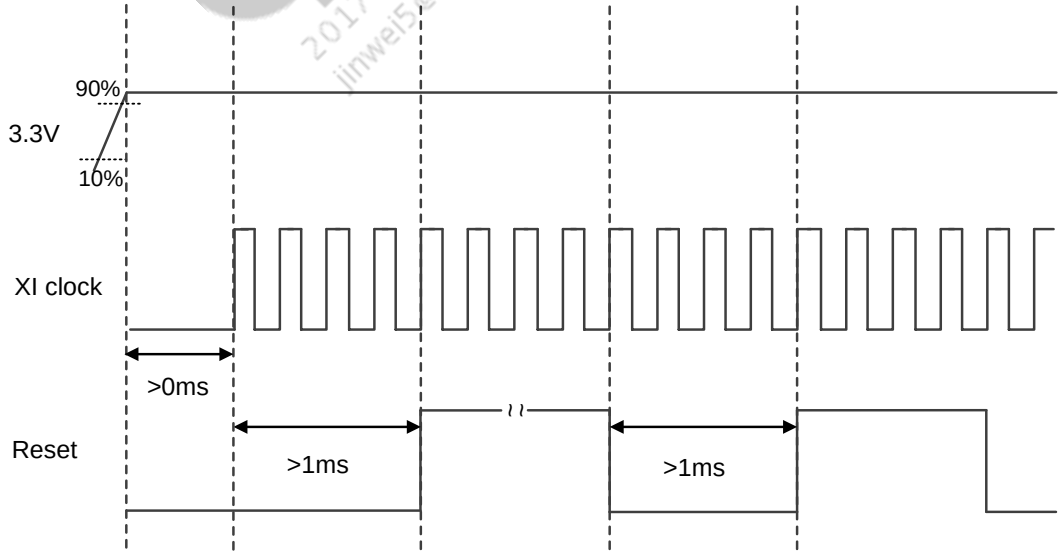


Figure 7-3 QCA8075 reset timing diagram

In AP.DK01 both the reset and clock source are from IPQ4018/IPQ4028, so a long enough power-up reset is required for IPQ4018/IPQ4028. Follow the RC circuit setting.

7.2 Clock

QCA8075 requires an external 25MHz clock input. In AP.DK01 it is sourced by IPQ4018/IPQ4028.

The clock amplitude is limited to 1.2V.

7.3 Power

QCA8075 only requires 3.3V input, all the other power rails are generated by internal regulators.

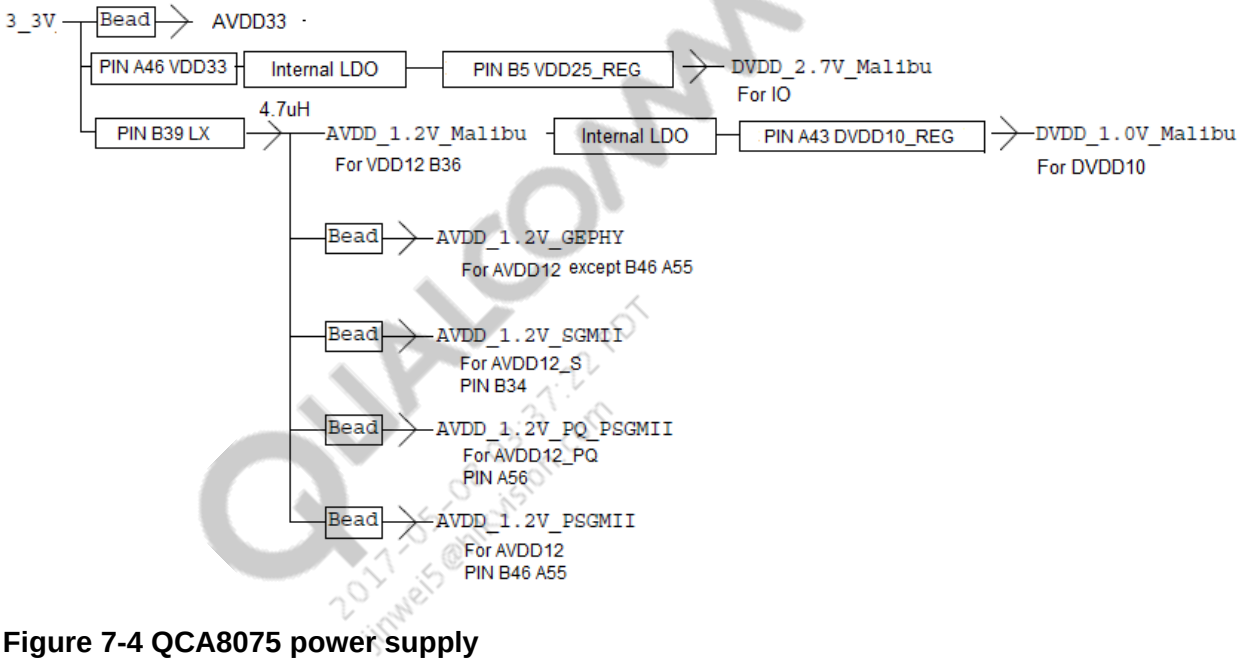


Figure 7-4 QCA8075 power supply

Table 7-1 QCA8075 power description

FILCAP_0	B7	1 µF+0.1 µF
FILCAP_1	A27	1 µF+0.1 µF
AVDD33	B2, B6, B10, A21,A24, B26, A37	3.3 V analog power input, 0.1 µF close to each pin
VDD33	A46	3.3 V digital power input for switch regulator, 22 µF+0.1 µF close to pin
AVDD12	A5, A10, A13, B15, B18, B21, A29, B28, B31, A55, B46, B52	1.2 V analog power input , 0.1 µF close to each pin Note: For A55, place the 0.1 µF and the chip on the same side, and 0.1 µF close to pin A55.
DVDD10	B13, A40	1.0 V digital power input, Connect to pin A43, 0.1 µF close to each pin
VDDIO_25	A58	2.7 V digital I/O power and the power supply for VDD15_REG LDO Note: For A58, place the 0.1 µF and the chip on the same side, and 0.1 µF close to pin A58.

AVDD12_S	B34	1.2 V analog power input for SGMII, Connect to pin B36 with a bead. 0.1 µF close to pin
AVDD12_PQ	A56	1.2 V analog power input for PSGMII/QSGMII Connect to pin B36 with a bead. 0.1 µF close to pin
AVDD25	B23	2.7 V analog power input for bias Connect to pin VDD25_REG. 0.1 µF close to pin
DVDD10_REG	A43	1.0 V regulator output for DVDD10 Connect a 4.7 µF and a 0.1 µF capacitors to stabilize this voltage.
VDD25_REG	B5	2.7 V regulator output Connect a 1 µF and a 0.1 µF capacitors to GND to stabilize this voltage.
VDD12	B36	1.2 V digital power input for 1.0 V LDO input Connect directly to the power inductor of switch regulator. Connect to AVDD12 through a bead. 0.1 µF close to pin.
VDD15_REG	B43	1.5/1.8 V regulator output and the I/O power for the MDC, MDIO, RESETn, INTn, WOL_INTn, and LOS. Connect a 1 µF and a 0.1 µF capacitors to stabilize this voltage.
LX	B39	Inductor pin for 1.2 V switch regulator Connect an external 4.7 µH power inductor to this pin directly. Connect the other end of the inductor to B36 directly. Connect a 10 µF and a 0.1 µF ceramic capacitors to the other end of the inductor to stabilize this power supply.

NOTE: In AP.DK01 the MDC/MDIO/RESETn need to work with 3.3V logic. Short VDD25_REG with VDD15_REG to make the MDC/MDIO/RESETn work at (VDD25_REG) 2.7V rail which can communicate with 3.3V logic.

7.4 MDC/MDIO manage

The IEEE 802.3u clause 22-compliant management interface provides access to the internal registers of the QCA8075 transceiver via the MDC and MDIO pins.

IPQ4018/IPQ4028 use GPIO[53] (MDIO), GPIO[52] (MDC) as MDC/MDIO interface.

The MDIO is an od-gate which requires an external 1.5K pull-up to QCA8075 2.7V rail.

Table 7-2 Management interface frame fields

	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

7.5 Boot configuration

The QCA8075 includes 10 LED pins. During hardware reset, these 10 LED pins are used as input for Power-On Strapping (POS) usage. After hardware reset is released, these 10 LED pins are used as output driven by internal PHY status. The POS functions are listed in Table 7-3.

In AP.DK01 MODE[2:0] must be configure as 3'b111.

The PHY address upper two bits are configured as 2'b00 by default.

Table 7-3 QCA8075 POS configurations

Pin symbol	POS configuration	Description	Default internal weak pull-up/down
LED_100_0	MODE[0]	MODE[2:0] are latched to configure chip operation mode. ▪ 111 = PSGMII ▫ 5 copper ports ▪ 110 = PSGMII ▫ 4 copper ports + 1 COMBO port (copper/fiber) ▪ 101 = QSGMII +SGMII ▫ 5 copper ports ▪ Others = Reserved	pull-up
LED_1000_0	MODE[1]		pull-up
LED_100_1	MODE[2]		pull-up
LED_1000_1	PHYAD3	The upper two bits of the physical address are set by PHYAD[4:3]. The PHYAD[2:0] are fixed to 0-5 for ports 0-4 and PSGMII respectively.	pull-down
LED_100_2	PHYAD4		pull-down
LED_1000_2	CONTROL_DAC0	CONTROL_DAC[2:0] configure power saving scheme in 1000BASE-T mode.	pull-up
LED_100_3	CONTROL_DAC1		pull-up
LED_1000_3	CONTROL_DAC2		pull-up
LED_100_4	AZ_SEL	AZ_SEL is latched to MMD7 register 0x3C bits[2:1] to enable/disable IEEE 802.3 az.	pull-up
LED_1000_4	Reserved	Must be pulled up.	pull-up

NOTE: The active status of LED_100_n and LED_1000_n depends on external pull-up or pull-down. When the LED pin is externally pulled up, it is strapped high and active low; when the LED pin is externally pulled down, it is strapped low and active high.

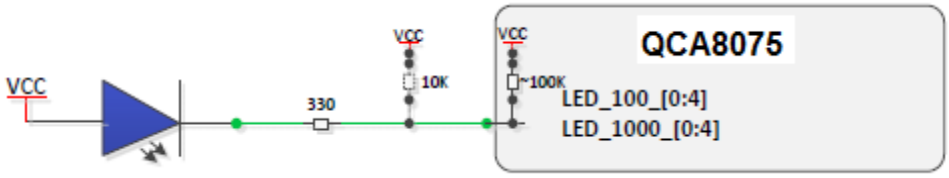


Figure 7-5 Reference design for LED, active low

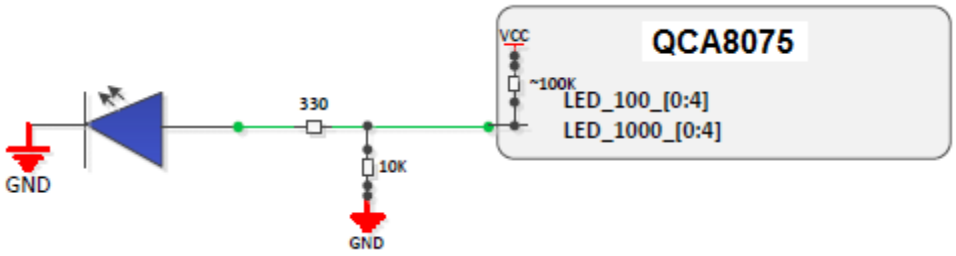


Figure 7-6 Reference design for LED, active high

7.6 MDI connection

The 75 Ω termination resistors and 1 nF/2kV capacitor between the center tap and the chassis ground (Bob Smith termination circuitry) is used to enhance the system EMI and ESD performance.

The 0.1 µF/50 V capacitors between the chassis ground and the system ground are used to enhance EMI performance. The capacitor values can be adjusted to minimize common noise.

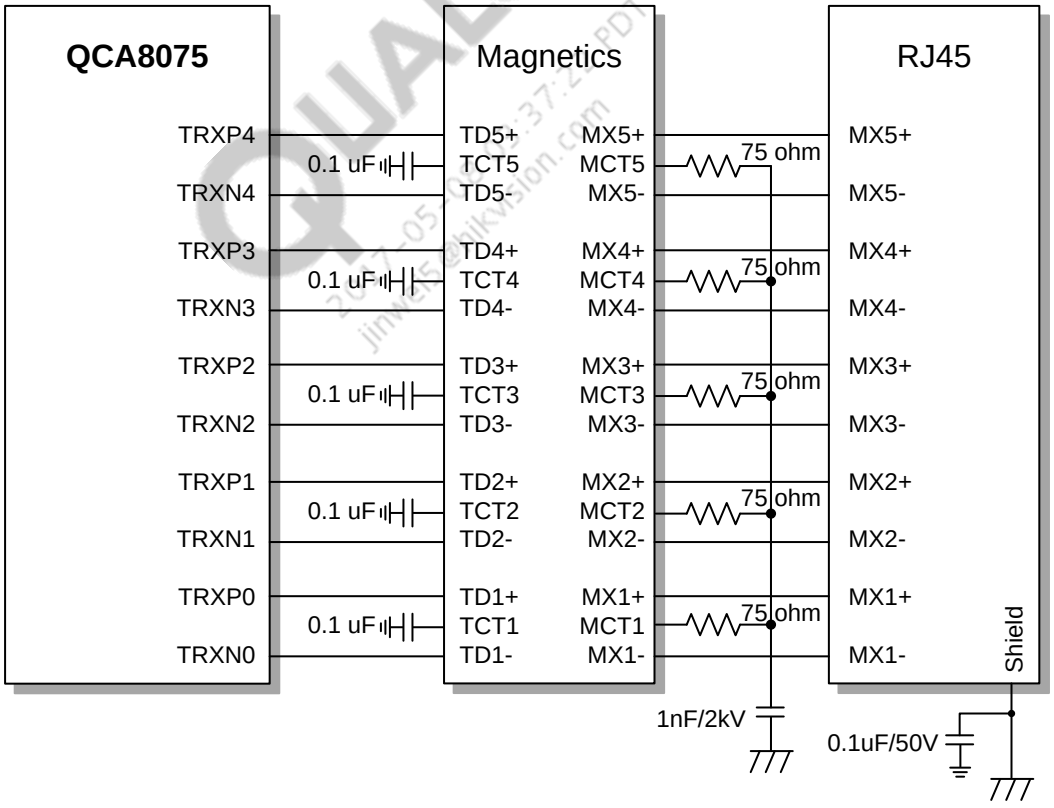
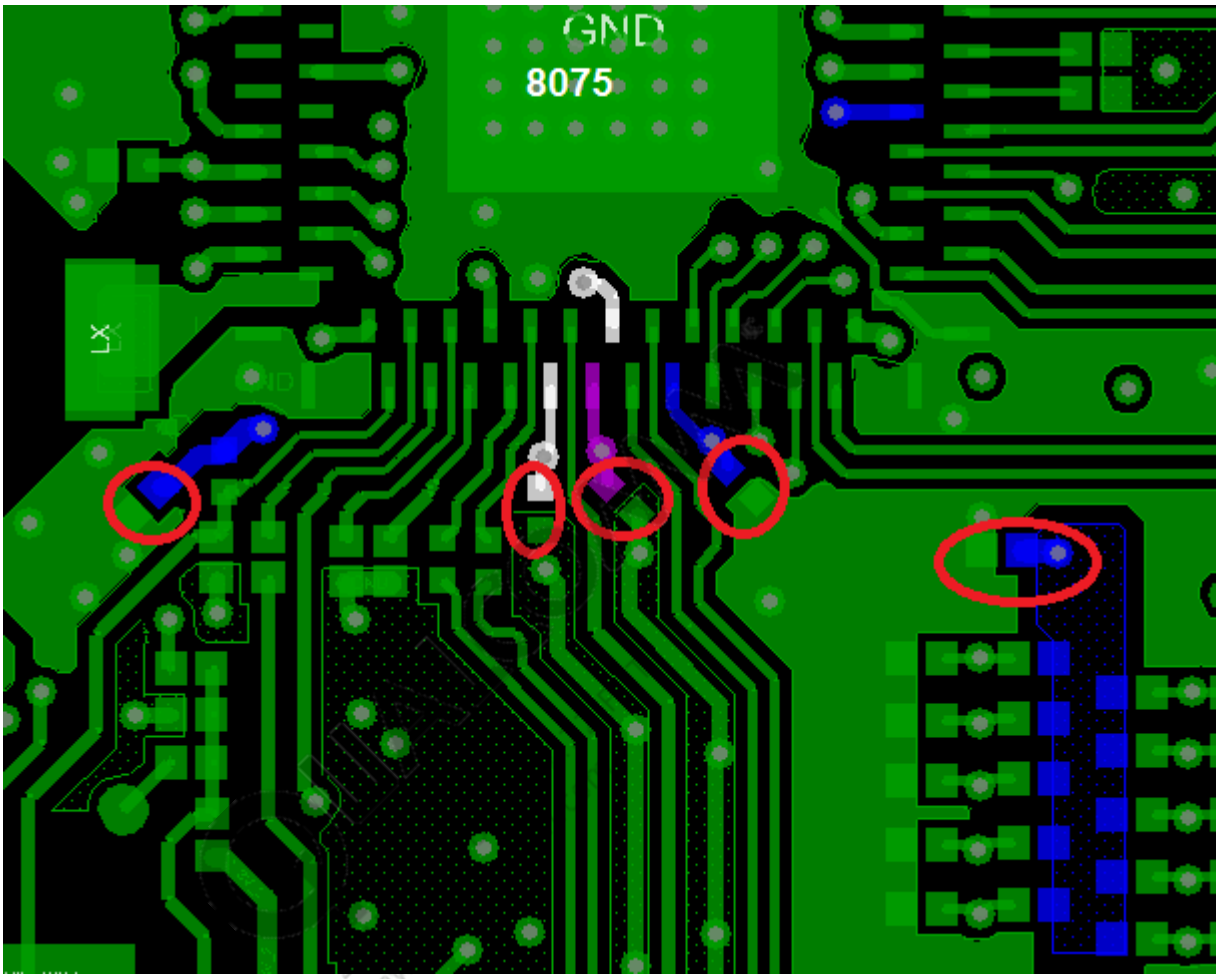


Figure 7-7 QCA8075 MDI connection

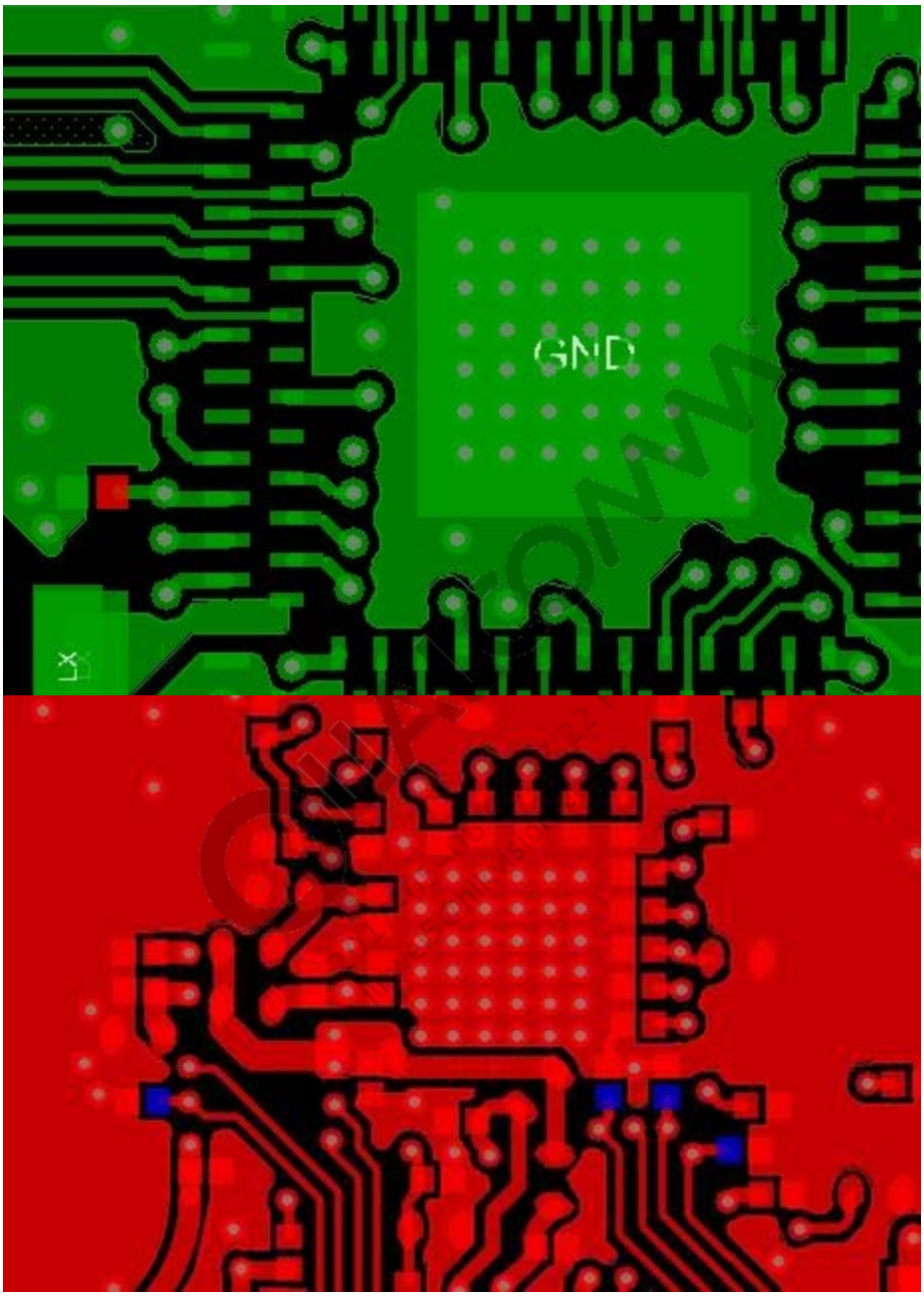
7.7 QCA8075 layout guidelines

- Choose 4.7µH inductor with 2A current capability and low DCR.

- Place the 4.7µH inductor on the same layer with PHY, no via. Close to chip.
- Place the decoupling capacitors for 1.2V on the same layer with inductor.
- The 2nd layer must be solid reference GND layer for PHY. Ensure that the same side pin breakout vias do not cut the ground under the chip.
- The chip and inductor, capacitors must be shielded with GND copper plane.
- 30 or more ground vias for E-pad.
- The length control of high speed differential pair can refer to the edge of the package.
- Control PSGMII/MDI differential impedance 100ohm.
- At least 80mil isolation between magnetic two ends.
- Refer to section 8.3 for DRQFN fan-outs.
- Add decouple capacitors for board 2.4 GHz noise floor improvement.
  - One 4.7 pF (DVDD_2.7V_Malibu to ground), close to QCA8075 reset pull-up resistor.
  - One 4.7 pF (DVDD_2.7V_Malibu to ground), close to boot configure reference rail.
  - One 0.1 µF (A58 to ground) close to A58 of QCA8075 on top layer.
  - One 0.1 µF (A56 to ground) close to A56 of QCA8075 on top layer.
  - One 0.1 µF (A55 to ground) close to A55 of QCA8075 on top layer.



- For each pin of P0_1000_LED/P1_1000_LED/P2_1000_LED/P3_1000_LED/P4_1000_LED, add 10 pF to ground close to QCA8075.



8 Board Stack-up and PCB Rules

The IPQ4018/IPQ4028 device is packaged as a 180-pin 14 x 14 DRQFN. The packaging and pinout have been optimized to implement designs in as few layers as possible; a 4-layer implementation with IPQ4018/IPQ4028 is presented in AP.DK01

8.1 Stack-up

- 4-layer board
- Thickness is 1.6 mm (62.992 mil), 1oz Cu =1.40152mil and 1/2oz Cu =0.7mil.
- Material: FR4 Tg 170

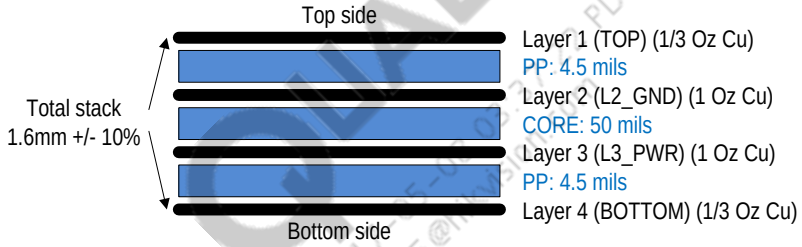


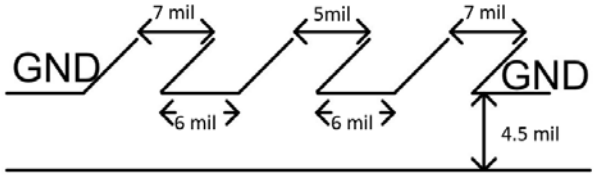
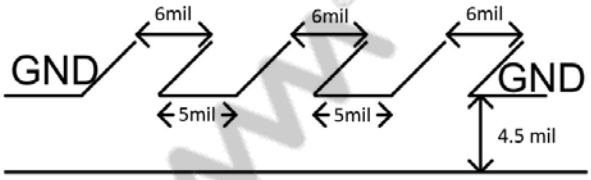
Figure 8-1 Board stack-up

8.2 Routing features

Table 8-1 shows the trace features used for routing (in reference to the stack-up in Figure 8-1). All signal traces routed on this board are micro-strip. The rules can vary by PCB manufacturer; it is more critical to meet the Z targets.

Table 8-1 AP.DK01 routing features

Category	Guideline/Remarks
Single-ended micro-strip trace	The target impedance of 7 mils single-ended traces on layer 1&4 is 50ohm ±10% relative to layer 2&3. The target impedance of 4.5 mils single-ended traces on layer 1&4 is 60ohm ±10% relative to layer 2&3.

Category	Guideline/Remarks
Micro-strip differential pair	▪ The USB target impedance is 90ohm ±10%.  ▪ The DDR3, Ethernet differential pair and PSGMII target impedance is 100ohm ±10%. 
Via/Drill	Blind and buried vias are not used
Other notes	It is key to suppress unused pads in inner layers to obtain more space for any inner layer routing/copper. It is acceptable to neck down the traces to 4 mils wide to exit the dual row QFN packages.

8.3 DRQFN fan-outs

Figure 8-2 shows the exit routing for IPQ4018/IPQ4028.

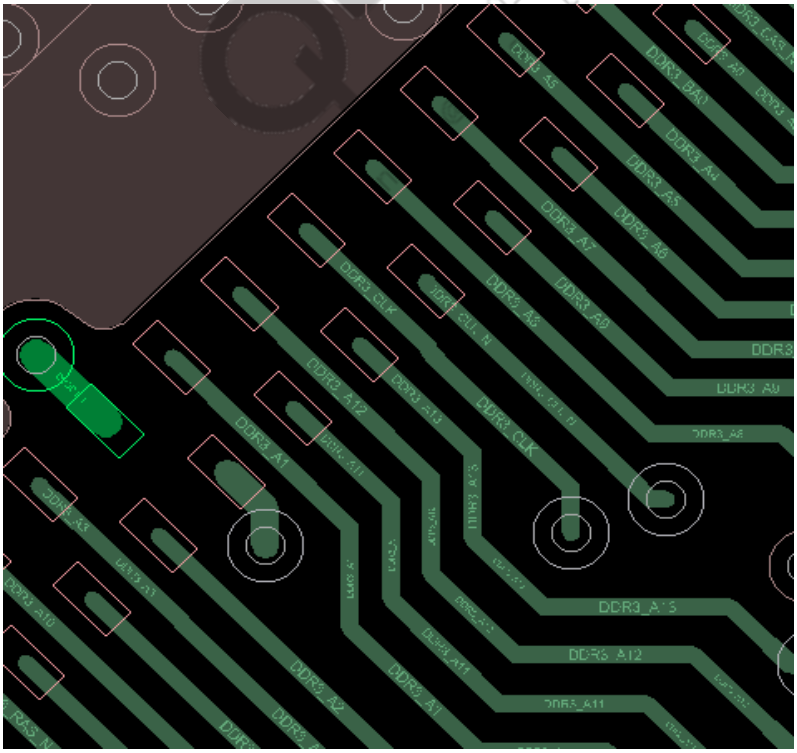
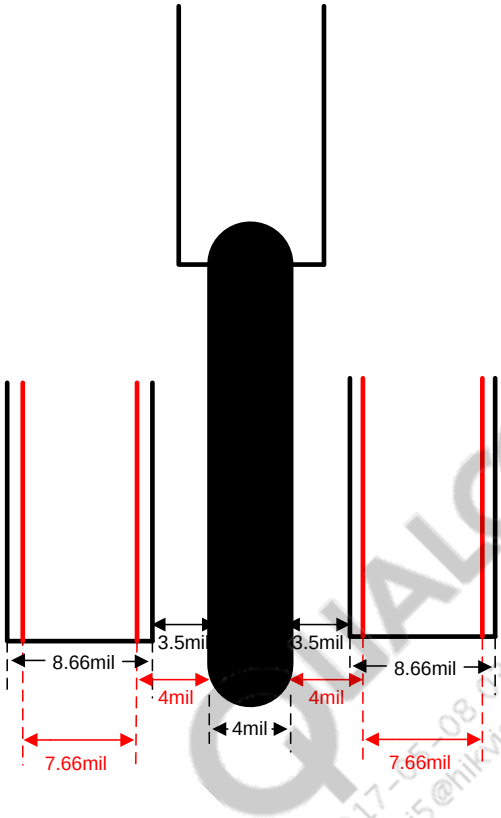


Figure 8-2 DRQFN exits and routing for IPQ4018/IPQ4028

It is acceptable to neck down the traces at the DRQFN breakouts to 4 mils wide, to obtain sufficient clearance. The pad dimension requires to adjust to get 4 mils clearance between trace and pad (see Figure 8-3).



Chip Dimensions:
Center Distance of Pin is 0.5mm (19.68mil)
Width of Pin is 0.22mm (8.66mil)

Pad Dimensions Guide:
Center Distance of PAD is 0.5mm (19.68mil)
Width of PAD is 0.195mm (7.66mil)
Width of Trace is 0.1mm (4mil)

Length of PAD equal to the chip package size

All of PAD follow the above size

Figure 8-3 Pad dimensions guide

A Performance Characteristics

This section provides example RF performance characteristics for AP.DK01 reference design based on the IPQ4018/IPQ4028 chips.

A.1 Tx power for UNII bands

Table A-1 Tx power (2.4 GHz)

	Each Chain	Tx Power (dBm)	
802.11b	1L	20	
802.11g	6 Mbps	19	
	54 Mbps	14	
802.11ac 20/40 MHz	MCS0	19	18
	MCS7 (EVM: -32 dB HO)	13	13
	MCS9 (EVM: -36 dB HO)	N/A	11

Table A-2 Tx power (5 GHz)

		Tx Power (dBm)			
	Each Chain	**Unii1 (5.15-5.25 GHz)**	**Unii2 (5.25-5.35 GHz)**	**Unii2ext (5.47-5.725 GHz)**	**Unii3 (5.725-5.875 GHz)**
802.11a	6 Mbps	17.5	17.5	17.5	17.5
	54 Mbps	13	13	13	13
802.11ac 20/40/80 MHz	MCS0	17.5/17/16.5	17.5/17/16.5	17.5/17/16.5	17.5/17/16.5
	MCS7 (EVM: -32 dB HO)	12/12/12	12/12/12	12/12/12	12/12/12
	MCS9 (EVM: -36 dB HO)	NA/10/10	NA/10/10	NA/10/10	NA/10/10

A.2 Rx sensitivity

Table A-3 Rx sensitivity (2.4 GHz)

	Each Chain	Rx Power (dBm)	
802.11b	1L (8% PER)	-97	N/A
802.11g	6 Mbps (10% PER)	-92.5	N/A
	54 Mbps (10% PER)	-75.5	N/A
802.11n 20/40 MHz	MCS0 (10% PER)	-92	-89.5
	MCS7 (10% PER)	-73.5	-71

	Each Chain	Rx Power (dBm)	
256-QAM 20/40 MHz	MCS9 (10% PER)	N/A	-65

Table A-4 Rx sensitivity (5 GHz)

	Each Chain (10% PER)	Rx Power (dBm)		
802.11g	6 Mbps	-90		
	54 Mbps	-74		
802.11ac 20/40/80 MHz	MCS0	-87	-85	-82
	MCS7	-71	-68.5	-64.5
	MCS8	-67	-63.5	-60.5
	MCS9	N/A	-61.5	-58.5