QCA9887 5-GHz 1x1 802.11a/n/ac WLAN SoC

Device Specification

80-Y0962-3 Rev. B

October 31, 2014

Confidential and Proprietary - Qualcomm Atheros, Inc.

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Revision history

Revision	Date	Description
A	August 2014	Initial version
B	October 2014	1. Global: Change package designation from “LPCC” to “MQFN”. 2. Global: Clarification that this device supports 5-GHz WLAN only 3. Section 3 “Electrical Characteristics”: Updated in many places. 4. Section 4.1 “Device Physical Dimensions”: Added specs for “E” package. 5. Table 4-4 “QCA9887 Order Numbers”: Updated for revision “02”. 6. Section 4.5 “Thermal characteristics”: New. 7. Section 6 “PCB Mounting Guidelines”: New. 8. Section 7 “Part Reliability”: New.

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1 Introduction

1.1 General Description

The Qualcomm Atheros QCA9887 is a highly integrated wireless local area network (WLAN) system-on-chip (SoC) for 5-GHz 802.11a/n/ac WLAN applications. The QCA9887 integrates an on-board CPU for low-level setup of WLAN physical layer (PHY) and RF to off-load the host processor for other tasks. It enables high-performance 1x1 with a single spatial stream for wireless applications demanding the highest robust link quality and maximum throughput and range. The QCA9887 integrates a multi-protocol MAC, PHY, analog-to-digital/digital-to-analog converters (ADC/DAC), 1x1 radio transceivers, and PCI Express interface in an all-CMOS device for low power consumption and small form-factor applications.

The QCA9887 implements half-duplex OFDM, and DSSS PHY, supporting 433 Mbps for 802.11ac 80-MHz channel operation. It supports 802.11n up to 72.2 Mbps for 20-MHz and 150 Mbps for 40-MHz channel operations, and IEEE 802.11a data rates. Additional features include Low-Density Parity Check (LDPC) and Space Time Block Code (STBC) for receive. The QCA9887 supports 802.11 wireless MAC protocol, 802.11i security, Rx/Tx filtering, error recovery, and 802.11e quality of service (QoS).

The QCA9887 supports a single traffic stream integrating one Tx and one Rx chain for high throughput and extended coverage. Tx chains combine PHY in-phase (I) and quadrature (Q) signals, convert them to the desired frequency, and drive the RF signal to an antenna. An Rx chain use an integrated architecture. The frequency synthesizer supports 1-MHz steps to match frequencies defined by IEEE 802.11a/n specifications.The QCA9887 supports frame data transfer to and from the host using a PCIE interface providing interrupt generation and reporting, power save, and status reporting. Other external interfaces include EEPROM and GPIOs.

1.2 Features

- WLAN CPU supports low-level setup of PHY and RF to off-load the host processor for other tasks
- Dynamic frequency selection (DFS) in required 5-GHz bands when used as an AP
- Supports low-density parity check (LDPC) for transmit and receive, Space Time Block Code (STBC) for receiver
- Integrated 1.2 V switching regulator
- Data rates of up to 433 Mbps in 802.11ac 80 MHz channels
- Data rates of up to 72.2 Mbps for 20 MHz channels and 150 Mbps for 40 MHz channels using reduced (short) guard interval in 802.11n mode
- Supports 20/40/80 MHz at 5 GHz
- Support for IEEE 802.11d, e, h, i, k, r, v time stamp, and w standards
- WEP, TKIP, AES, and WAPI hardware encryption
- PCI Express 1.1 interface
- 20 and 40 MHz channelization
- Frame aggregation, block ACK
- 802.11e-compatible bursting
- 68-pin, 8 mm x 8 mm MQFN package

1.3 System Diagram

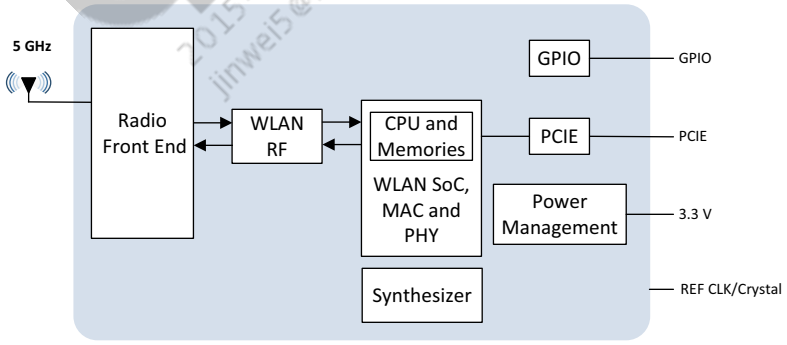


Figure 1-1 QCA9887 System Diagram

1.4 Functional Specification

1.4.1 Functional block diagram

Figure 1-2 illustrates the QCA9887 functional block diagram.

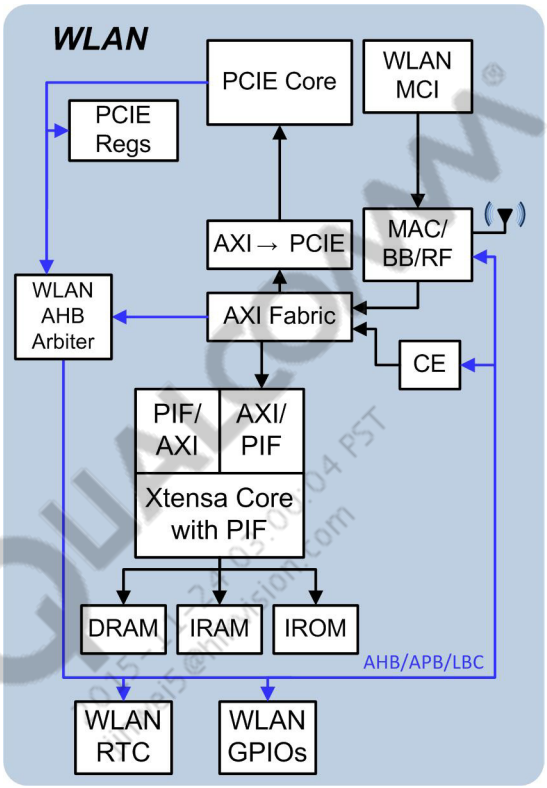


Figure 1-2 QCA9887 functional block diagram

The QCA9887 is comprised of several internal functional blocks, as summarized in Table 1-1.

Table 1-1 Functional blocks

Block	Description
AXI	The AXI bus is accessed simultaneously by multiple masters in the PCIE host memory, CPU memory, and all programmable registers. The WLAN portion of the AXI fabric supports split transactions to achieve higher utilization on the PCIE bus. All register access from the CPU route through the AXI fabric. A bridge converts AXI requests to AHB requests, and the AHB arbiter selects between PCIE register access requests and CPU register access requests on a round-robin basis. All register accesses for all modules including the MAC, CE, and blocks such as GPIOs, or RTC use the APB protocol. A bridge converts AHB requests into APB. It must be noted here that the entire AXI fabric, AHB, and APB interfaces all run synchronously on the SoC clock domain. See AXI.
CE	The copy engine (CE) establishes a communication channel between the firmware and the host. It performs a DMA copy from one memory location (source memory) to another memory location (destination memory), and it can perform this DMA copy operation in a batch, under control of software. A copy involves a read operation from the source memory, followed by a write operation to the destination memory.
WLAN Clocking	The MAC/baseband clock domain runs off of the WLAN PLL. The PLL runs at either at 160 MHz or 176 MHz. The CPU/SoC clock domain runs off of the CPU PLL. The AXI fabric together with the AHB and APB buses typically run at either half or quarter CPU clock. The PCIE clock domain runs at 125 MHz.
CPU Core and Memory Controller	The CPU is a Tensilica XTENSA 7.0 processor with a hardware abstraction layer (HAL) to support low level WLAN activity with minimal support from the PCIE host. The CPU is configured with a peripheral interface (PIF). The outbound PIF is used by the CPU for register access. The inbound PIF is used by the other AXI masters (MAC and CE) to access the data memory (DMEM) connected to the CPU.
MAC/Baseband/RF	The integrated 5-GHz 802.11ac MAC/baseband/radio includes low-density parity check (LDPC) for transmit and receive, Space Time Block Code (STBC) for receive, an off-load engine (OLE) block responsible for A-MSDU scatter and gather, L2 header encapsulation and decapsulation, IP/TCP/UDP checksum, and Rx classification.
PCIE Core	All programmable registers can be accessed by either the PCIE host or by the internal CPU. The PCIE core provides a simple proprietary low-bandwidth controller (LBC) interface for register accesses.
PCIE Configuration Space Registers	The QCA9887 PCIE configuration space maps to the host memory space. All programmable registers can be accessed either by the PCIE host or by the internal CPU. The PCIE core provides a simple proprietary low-bandwidth controller (LBC) interface for register accesses. A bridge converts this LBC interface into standard AHB. An AHB-AHB bridge synchronizes the clock domain from the PCIE clock domain to the SoC clock domain. Some additional registers are accessible only by the PCIE host. These registers run on the PCIE clock domain and are not routed through the main AHB arbiter. They allow the PCIE host to determine the sleep status of the SoC and to wake up the SoC if needed. See PCIE configuration space register descriptions.
WLAN AHB Arbiter	Selects between the PCIE register access requests and CPU register access requests on a round-robin basis.
WLAN GPIOs	All digital pins map to 18 GPIOs. These GPIOs are used for a variety of purposes such as UART, I^2C, SPI, or JTAG. Another set of digital outputs are the four antenna switches used as scan outputs during ATPG testing. See GPIO.
WLAN RTC	The RTC block controls the clocks and power going to other modules within the chip. Its inputs consist of sleep requests from these modules and its outputs consists of clock enable signals used to gate the clocks going to these modules. The RTC block also manages resets going to other modules within the device.

1.4.2 AXI

Figure 1-3 diagrams the AXI fabric.

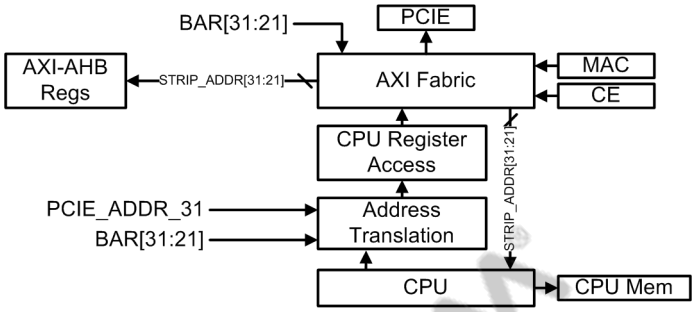


Figure 1-3 AXI fabric diagram

Because PCIE host memory, CPU memory, and all programmable registers can all be accessed simultaneously by multiple masters in the AXI bus, it is important to ensure that no address-related conflicts arise. Upon booting, the PCIE host provides a unique base address (BAR) to all devices. BAR location always aligns to the space requested by each device; in the QCA9887, it is 2 MBytes of space, thus the BAR aligns to 2 MBytes, and only bits [31:21] are non-zero. AXI fabric uses these bits as input to steer incoming AXI requests to the appropriate slave. Note that BAR input to the AXI fabric is not directly connected to the BAR value programmed by the PCIE host, but comes from a programmable register. AXI fabric looks for BAR bits [31:21] for all incoming transfers. See Table 1-2.

Table 1-2 Address decoding logic

Address Bits [31:21]	Address Bits [20:0]	AXI Slave Decode
BAR not matching	—	PCIE
BAR matching	< 0x100000	AXI-AHB (register access)
	≥ 0x100000	For the CPU, address bits [31:20] are replaced with the programmable register CPU_ADDR_MSB_V, which is set by default to 4 to indicate a 4-Mbyte address range matching with the CPU's DMEM address space.

The Xtensa CPU memory address location must be in fixed address ranges: instruction memory (IMEM) must be 8-12 MBytes (0x800000-0xBFFFFF) and data memory (DMEM) 4-8 MBytes (0x400000-0x7FFFFF). Because these fixed address ranges could conflict with PCIE host memory allocation, the an address translation mechanism is used for all CPU access. See Figure 1-4.

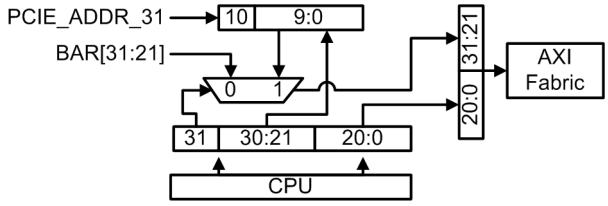


Figure 1-4 CPU address translation mechanism

All outbound transfers from the CPU pass through the address translation logic, which looks at the MSB of the address (bit [31]). If this bit is low, the transfer is deemed to be a register access and bits [31:21] of the address are appended with the BAR value. The AXI fabric steers the transfer to the AXI-AHB bridge as indicated in Table 1-2. If bit [31] is high, the transfer is deemed as intended to access PCIE memory, thus all but the MSB (bits [30:0]) must contain the intended address in PCIE host memory. The programmable register PCIE_ADDR_31 contains the MSB of the PCIE host memory location appended to the original address.

1.4.3 GPIO

The QCA9887 provides 18 configurable bidirectional general purpose I/O ports and three configurable input-only ports. Each GPIO port can be configured independently as input or output using the GPIO control registers. The GPIOs are used for a variety of purposes such as UART, I^2C, SPI, JTAG, and so on. Another set of digital outputs are the five antenna switches used as scan outputs during ATPG testing.

Most GPIOs have a normal mode functionality as well as a test-mode functionality. The mapping of the GPIOs is shown in Table 1-3. On reset all GPIOs are inputs and the bootstrap values are sampled. The global test mode is on GPIO4. If this pin is sampled high during initialization, then the chip enters test mode.

Table 1-3 Multiplexed pins

GPIO Pin	Pin	Description
GPIO0	36	WLAN_DISABLE
GPIO1	37	WLAN_LED
GPIO2	5	Reserved
GPIO3	6	Reserved
GPIO4	7	WLAN_ACTIVE
GPIO5	9	I2C_SDA
GPIO6	33	UART_RXD
GPIO7	35	UART_TXD
GPIO8	68	ANTA
GPIO9	2	ANTB
GPIO10	3	ANTC
GPIO11	4	ANTD
GPIO12	11	TMS
GPIO13	12	TCK
GPIO14	13	TDI
GPIO15	14	TDO
GPIO16	32	Reserved
GPIO17	10	I2C_SCK

2 Pin Descriptions

This section contains a package pinout (see Figure 2-1 and Table 2-1) and a tabular listing of the signal descriptions.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

I	Digital input signal
I/O	A digital bidirectional signal
IA	Analog input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
O	A digital output signal
OA	An analog output signal
OD	A digital output signal with open drain
P	A power or ground signal

Figure 2-1 shows the MQFN-68 package pinout.

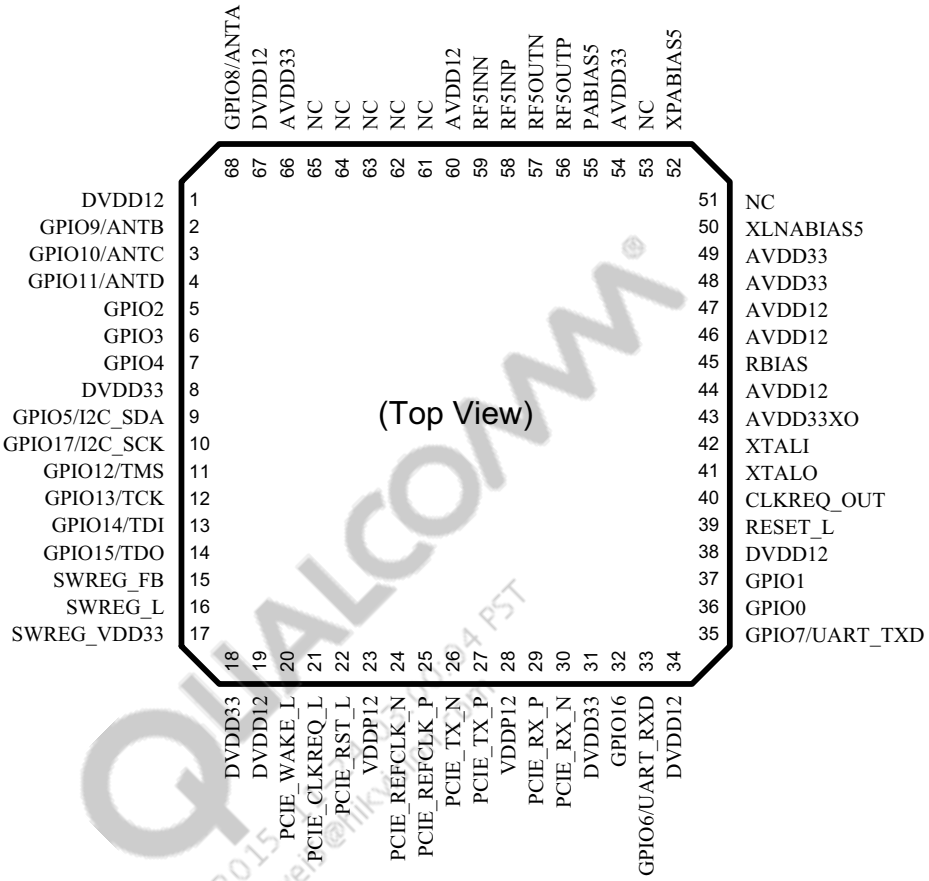


Figure 2-1 MQFN-68 Package Pinout

Table 2-1 Signal-to-Pin Relationships and Descriptions

Symbol	Pin	Type	Description
PCI Express			
PCIE_CLKREQ_L	21	OD	Reference clock request, open drain
PCIE_REFCLK_N	24	IA	Differential reference clock (100 MHz)
PCIE_REFCLK_P	25	IA	
PCIE_RST_L	22	IL	PCI Express reset with weak pull-down
PCIE_RX_N	30	IA	Differential receive
PCIE_RX_P	29	IA	
PCIE_TX_N	26	OA	Differential transmit
PCIE_TX_P	27	OA	
PCIE_WAKE_L	20	OD	Request to service a function-initiated wake event, open drain
Radio			
RF5INN	59	IA	Differential RF input at 5 GHz; use one side for single-ended input
RF5INP	58	IA	
RF5OUTN	57	OA	Differential 5-GHz RF power amplifier output
RF5OUTP	56	OA	
Analog Interface			
PABIAS5	55	P	External bias for 5 GHz
RBIAS	45	IA	BIAS for radio
XLNABIAS5	50	OA	External LNA Bias for 5 GHz
XPABIAS5	52	OA	External PA bias for 5 GHz
Internal Voltage Regulator			
SWREG_FB	15	I	1.2 V feedback to the internal switching regulator[1]
SWREG_L	16	P	1.2 V output from the internal switching regulator[1]
SWREG_VDD33	17	P	3.3 V input to the internal switching regulator
General			
CLKREQ_OUT	40	OD	40 MHz clock output
RESET_L	39	IH	Reset with weak pull-up for the QCA9887
XTALI	42	I	40 MHz crystal
XTALO	41	I/O	

Table 2-1 Signal-to-Pin Relationships and Descriptions (cont.)

Symbol	Pin	Type	Description
GPIO			
GPIO0	36	I/O	General purpose input/output pins The GPIOs are used for a variety of purposes such as I^2C, SPI, JTAG, etc.
GPIO1	37	I/O	
GPIO2	5	I/O	
GPIO3	6	I/O	
GPIO4	7	I/O	
GPIO5/I2C_SDA	9	I/O	
GPIO6/UART_RXD	33	I/O	
GPIO7/UART_TXD	35	I/O	
GPIO8/ANTA	68	I/O	
GPIO9/ANTB	2	I/O	
GPIO10/ANTC	3	I/O	
GPIO11/ANTD	4	I/O	
GPIO12/TMS	11	I/O	
GPIO13/TCK	12	I/O	
GPIO14/TDI	13	I/O	
GPIO15/TDO	14	I/O	
GPIO16/EJTAG_RESET	32	I/O	
GPIO17/I2C_SCK	10	I/O	

1. An LC circuit is required off-chip between the SWREG_OUT and SWREG_FB. See Figure 3-2.

Symbol	Pin	Description
Power		
AVDD12	44, 46, 47, 60	Analog 1.2 V power supply[1]
AVDD33	48, 49, 54, 66	Analog 3.3 V power supply
AVDD33XO	43	Analog 3.3 V power supply
DVDD12	1, 19, 34, 38, 67	Digital 1.2 V power supply[1]
DVDD33	8, 18, 31	Digital 3.3 V power supply
VDDP12	23, 28	PCIE 1.2 V power supply[1]
Ground Pad		
Exposed Ground Pad		Tied to GND (see Device Physical Dimensions)
No-Connect (NC)		
	51, 53, 61, 62, 63, 64, 65	Leave disconnected.

1. All 1.2 V supplies need to be connected to the SWREG_FB pin. See Figure 3-2.

3 Electrical Characteristics

3.1 Absolute maximum ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the QCA9887.

Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document is not recommended.

Table 3-1 Absolute maximum ratings

Symbol	Parameter	Max Rating	Unit
V_{DD12}	Supply voltage	-0.3 to 1.32	V
V_{DD33}	Maximum I/O supply voltage	-0.3 to 3.6	V
RF_{in}	Maximum RF input (reference to 50 Ω)	+10	dBm
T_{store}	Storage temperature	-60 to 150	°C
T_J	Junction temperature	125	°C
ESD	Electrostatic discharge tolerance		
	PABIAS5, RF5OUTN and RF5OUTP	1500	V
	All other pins	2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AV_{DD12}	External regulator voltage	±3%	1.14	1.20	1.26	V
D_{VDD12}	Internal regulator voltage	—	—	1.20	—	V
V_{DD33}	I/O voltage	±5%	3.135	3.3	3.465	V
T_{case}	Case temperature	—	0	—	110	°C
Psi_{JT}	Junction-to-top-center of the package thermal resistance	—	—	—	2.6	°C/W

3.3 40-MHz clock characteristics

TCXO clock is not supported by the QCA9887; a 40 MHz crystal with no less than 12 pF loading must be used.

3.4 GPIO DC electrical characteristics

Table 3-3 lists the GPIO DC electrical characteristics, with:

T_{amb} = 25 °C

Table 3-3 General DC electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	0.7 * V_{DD33}	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	0.3 * V_{DD33}	V
V_{OH}	High Level Output Voltage	—	0.9 * V_{DD33}	—	—	V
V_{OL}	Low Level Output Voltage	—	0	—	0.1 * V_{DD33}	V

3.5 PCIE pin characteristics

Table 3-4 shows the QCA9887 PCIE interface pin characteristics.

Table 3-4 PCIE interface DC electrical characteristics

Signal Name	Pin	Type	Drive	PU/PD Resistance
RESET_L	15	IH	—	—
PCIE_RST_L	26	IL	—	150 KΩ
PCIE_WAKE_L	22	OD	90 mA	—
PCIE_CLKREQ_L	24	OD	90 mA	—
PCIE_REFCLK_N	29	IA	—	—
PCIE_REFCLK_P	30	IA	—	—
PCIE_TX_N	31	OA	—	—
PCIE_TX_P	32	OA	—	—
PCIE_RX_N	34	IA	—	—
PCIE_RX_P	33	IA	—	—
GPIO0	17	IO	90 mA	—
GPIO1	18	IO	27 mA	—
GPIO2	19	IO	90 mA	—
GPIO3	20	IO	90 mA	—
GPIO4	23	IO	27 mA	—
GPIO5	25	IO	90 mA	—
GPIO6	40	IO	90 mA	—
GPIO7	41	IO	27 mA	—
GPIO8	42	IO	27 mA	—
GPIO9	43	IO	27 mA	—
GPIO10	44	IO	90 mA	—
GPIO11	46	IO	90 mA	—
GPIO12	47	IO	90 mA	—
GPIO13	48	IO	27 mA	—
GPIO14	49	IO	27 mA	—
GPIO15	50	IO	27 mA	—
GPIO16	57	IO	90 mA	—
GPIO17	58	IO	27 mA	—

3.6 Power up sequencing

Figure 3-1 depicts the required reset sequence for the QCA9887 PCIE interface. Table 3-5 shows the QCA9887 PCIE interface timing parameters.

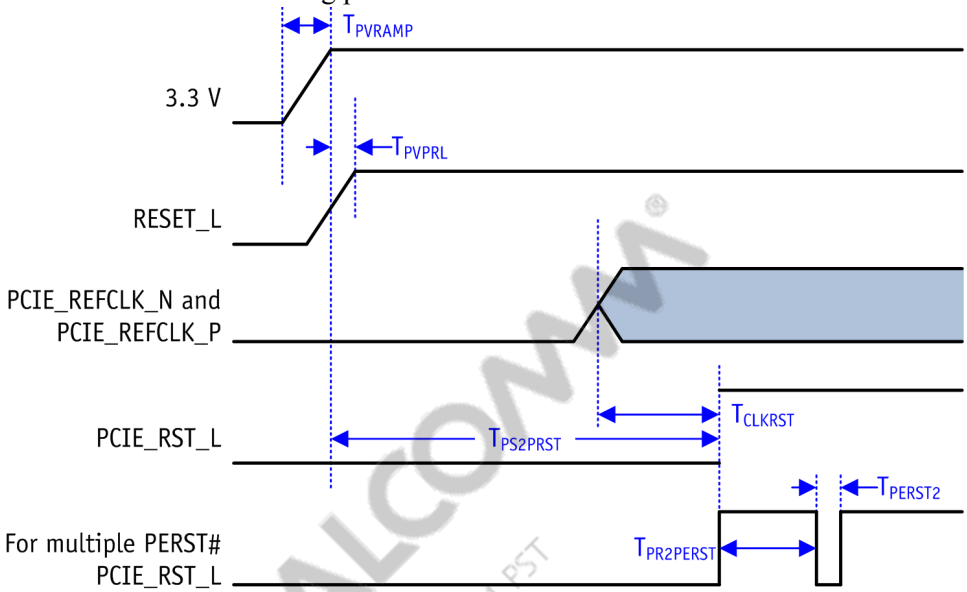


Figure 3-1 QCA9887 power up sequencing

Table 3-5 PCIE interface timing parameters

Symbol	Parameter	Min	Max	Unit
T_{PVRAMP}	Power supply ramp on 3.3 V	—	25	ms
T_{PVPRL}	Power valid to RESET_L asserted	0[1]	—	µs
T_{PRCLK}	RESET_L deasserted to PCIE_REFCLK_N and PCIE_REFCLK_P stable	100	—	µs
T_{CLKRST}	PCIE_REFCLK_N and PCIE_REFCLK_P stable to PCIE_RST_L deasserted	100[2]	—	µs
$T_{PS2PRST}$	Power supply stable to PCIE_RST_L deassert	10[3]	—	ms
$T_{PR2PERST}$	Initial PCIE_RST_L deassert to subsequent multiple PCIE_RST_L	40	—	ms
T_{PERST2}	Subsequent PCIE_RST_L asserted for multiple PCIE_RST_L	1	—	ms

1. It is recommended to leave the RST_L pin floating. At power up, internal power-on reset signal derived from 1.2 V and 3.3 V supply will ensure correct functionality.
2. This timing depends on hardware interface designs, such as Express Card, PCIE Mini Card, or PCIE desktop applications. The system must follow PCIE specifications, as well as TCLKRST.
3. $T_{PS2PRST}$ minimum timing must be observed.

3.7 Internal voltage regulators

Figure 3-2 depicts the voltages regulated by the QCA9887. Refer to the reference design schematics for details.

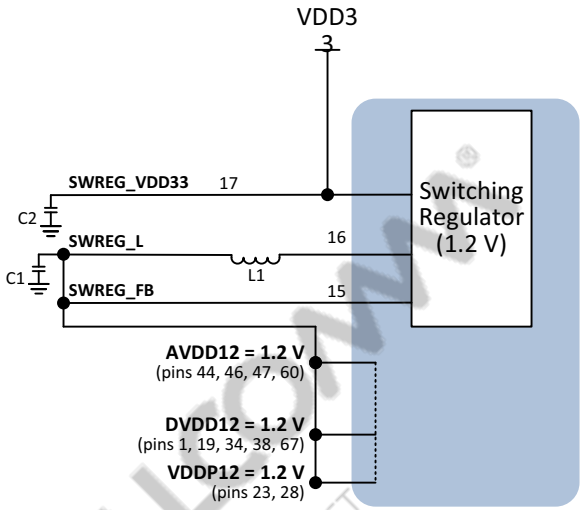


Figure 3-2 Output voltages regulated by the QCA9887

3.8 Radio characteristics

The following conditions apply to the typical per chain characteristics unless otherwise specified:

V_{DD12} = 1.2V
V_{DD33} = 3.3V, T_{amb} = 25 °C

3.8.1 Receiver characteristics

See Table 3-6 for the QCA9887 receiver characteristics:

Table 3-6 Rx Characteristics for 5-GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range	5 MHz center frequency	5.18	—	5.825	GHz
NF	Receive chain noise figure (max gain)	See Note 1	—	6.5	—	dB
S_{rf}	Sensitivity					
	OFDM, 6 Mbps	See Note 2	-82	-91	—	dBm
	OFDM, 54 Mbps		-65	-75	—	
	HT20, MCS0, 1 stream, 1 Tx, 1 Rx		-82	-91	—	
	HT20, MCS7, 1 stream, 1 Tx, 1 Rx		-64	-73	—	
	HT40, MCS0, 1 stream, 1 Tx, 1 Rx		-79	-89	—	
	HT40, MCS7, 1 stream, 1 Tx, 1 Rx		-61	-70	—	
	VHT20, MCS0, 1 stream, 1 Tx, 1 Rx		-82	-91	—	
	VHT20, MCS8, 1 stream, 1 Tx, 1 Rx		-59	-69	—	
	VHT40, MCS0, 1 stream, 1 Tx, 1 Rx		-79	-88	—	
	VHT40, MCS9, 1 stream, 1 Tx, 1 Rx		-54	-64	—	
	VHT80, MCS0, 1 stream, 1 Tx, 1 Rx		-76	-86	—	
	VHT80, MCS9, 1 stream, 1 Tx, 1 Rx		-51	-60	—	
IP1dB	Input 1 dB compression (min. gain)	—	—	2.5	—	dBm
IIP3	Input third intercept point (min. gain)	—	—	13	—	dBm
Z_{RFin_input}	Recommended LNA single-ended drive impedance	—	—	12.88 + j51	—	Ω
R_{adj}	Adjacent channel rejection					
	11a OFDM, 6 Mbps	See Note 3	16	21	—	dB
	11a OFDM, 54 Mbps		-1	5	—	
	HT20, MCS0		16	24	—	dB
	HT20, MCS15		-2	5	—	
	HT40, MCS0		16	26	—	dB
	HT40, MCS15		-2	8	—	
	VHT20, MCS0, 1 stream		16	23	—	dB
	VHT20, MCS15, 2 stream		-9	-0	—	
	VHT40, MCS0, 1 stream		16	22	—	dB
	VHT40, MCS15, 2 stream		-9	2	—	
	VHT80, MCS0, 1 stream		16	22	—	dB
	VHT80, MCS9, 2 stream		-9	0	—	

1. For improved sensitivity performance, an external LNA may be used.
2. Sensitivity performance based on Qualcomm Atheros reference design, which includes Tx/Rx antenna switch, xLNA, and diplexer with LDPC enabled. Minimum values based on IEEE 802.11 specifications.
3. Typical values measured with reference design. Minimum values based on IEEE 802.11 specifications.

3.8.2 Transmitter characteristics

See these tables for the QCA9887 transmitter characteristics:

Table	Transmit Characteristics for:
Table 3-7	5 GHz Operation with Internal PA
Table 3-8	5 GHz Operation with External PA

Table 3-7 Tx Characteristics for 5-GHz Operation with Internal PA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	20 MHz center frequency	5.18	—	5.825	GHz
P_{out}	Mask compliant output power					
	6M	See Note [1]	—	15	—	dBm
	VHT20 MCS0		—	15	—	dBm
	VHT40 MCS0		—	15	—	dBm
	VHT80 MCS0		—	14	—	dBm
	EVM compliant output power					
	802.11a, 54 Mbps - single Tx chain	See Note [1]	—	12	—	dBm
	802.11ac, MCS7, VHT20 - single Tx chain		—	11	—	dBm
	802.11ac, MCS7, VHT40 - single Tx chain		—	11	—	dBm
	802.11ac, MCS7, VHT80 - single Tx chain		—	11	—	dBm
	802.11ac, MCS8, VHT20 - single Tx chain		—	11	—	dBm
	802.11ac, MCS8, VHT40 - single Tx chain		—	10	—	dBm
	802.11ac, MCS8, VHT80 - single Tx chain		—	10	—	dBm
	802.11ac, MCS9, VHT40 - single Tx chain		—	10	—	dBm
	802.11ac, MCS9, VHT80 - single Tx chain		—	10	—	dBm
SP_{gain}	PA gain step	See Note [2]	—	0.25	—	dB
A_{pl}	Accuracy of power leveling loop	See Note [3]	—	±2	—	dB
Z_{RFout_load}	Output Impedance	See Note [4]	—	15.58 + j121	—	Ω
SS	Sideband suppression	—	—	-40	—	dBc
LO_{leak}	LO leakage: at 2/3 of the RF output					
	@ RF=5.15-5.35 GHz (FCC)	—	—	-32	—	dBm
	@ RF=5.35-5.725 GHz (ETSI)			-36	—	dBm
	@ RF=5.725-5.825 GHz (FCC)			-30	—	dBm
RS	Synthesizer reference spur	—	—	-68	—	dBc

Table 3-7 Tx Characteristics for 5-GHz Operation with Internal PA (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EVM		Tx Power (dBm)[5]				
	802.11n, MCS9, VHT80:1 Tx Chain	-15	—	-40	—	dB
		-13	—	-39.5	—	
		-10	—	-39.5	—	
		-8	—	-39.5	—	
		-7	—	-39.4	—	
		-5	—	-39	—	
		-3	—	-38.8	—	
		-1	—	-38	—	
		1	—	-37	—	
		3	—	-36	—	
		5	—	-35	—	
		7	—	-35	—	
		9	—	-34	—	
		11	—	-33	—	
		13	—	-31	—	
		15	—	-26	—	
		17	—	-25	—	

1. Measured with reference design including switch, filter, and diplexer.
2. Guaranteed by design.
3. Manufacturing calibration required.
4. See the sample impedance matching circuit in the Qualcomm Atheros reference design schematics. To achieve good RF performance, it is strongly recommended not to alter the RF portion of the Qualcomm Atheros reference design for different matching networks.
5. Measured at the RF connector's output.

Table 3-8 Tx Characteristics for 5-GHz Operation with External PA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	20 MHz center frequency	5.18	—	5.825	GHz
P_{out}	Mask compliant output power					
	6 Mbps	See Note 1	—	20.5	—	dBm
	VHT20, MCS0		—	20.5	—	
	VHT40, MCS0		—	20	—	
	VHT80, MCS0		—	19.5	—	

Table 3-8 Tx Characteristics for 5-GHz Operation with External PA (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_{out} (cont.)	EVM compliant output power					
	802.11ac, 54 Mbps: 1 Tx Chain	See Note 1	—	17	—	dBm
	802.11ac, MCS7, VHT20: 1 Tx Chain		—	17	—	
	802.11ac, MCS7, VHT40: 1 Tx Chain		—	17	—	
	802.11ac, MCS7, VHT80: 1 Tx Chain		—	17	—	
	802.11ac, MCS8, VHT20: 1 Tx Chain		—	15	—	
	802.11ac, MCS8, VHT40: 1 Tx Chain		—	15	—	
	802.11ac, MCS8, VHT80: 1 Tx Chain		—	15	—	
	802.11ac, MCS9, VHT40: 1 Tx Chain		—	14.5	—	
	802.11ac, MCS9, VHT80: 1 Tx Chain		—	14.5	—	
EVM	802.11ac, MCS9, VHT80: 1 Tx Chain	0 dBm	—	-39	—	dB
		1 dBm	—	-39	—	
		2 dBm	—	-39	—	
		3 dBm	—	-39	—	
		4 dBm	—	-39	—	
		5 dBm	—	-38	—	
		6 dBm	—	-38	—	
		7 dBm	—	-38	—	
		8 dBm	—	-38	—	
		9 dBm	—	-38	—	
		10 dBm	—	-37	—	
		11 dBm	—	-37	—	
		12 dBm	—	-37	—	
		13 dBm	—	-37	—	
		14 dBm	—	-36	—	
		15 dBm	—	-35	—	
		16 dBm	—	-33	—	
		17 dBm	—	-31	—	
		18 dBm	—	-28	—	
		19 dBm	—	-26	—	
		20 dBm	—	-22	—	
SP_{gain}	PA gain step	See Note 2	—	0.25	—	dB
A_{pl}	Accuracy of power leveling loop	See Note 3	—	±2	—	dB
Z_{RFout_load}	Output Impedance	See Note 4	—	15.58 + j121	—	Ω
SS	Sideband suppression	—	—	-40	—	dBc
LO_{leak}	LO leakage: at 2/3 of the RF output					
	@ RF=5.15-5.35 GHz (FCC)	—	—	-32	—	dBm
	@ RF=5.35-5.725 GHz (ETSI)			-36	—	
	@ RF=5.725-5.825 GHz (FCC)			-30	—	
RS	Synthesizer reference spur	—	—	-68	—	dBc

1. Measured at antenna port.
2. Guaranteed by design (5G FEM: SKY85703-11).
3. Manufacturing calibration required.
4. See the sample impedance matching circuit in the Qualcomm Atheros reference design schematics. To achieve good RF performance, it is strongly recommended not to alter the RF portion of the Qualcomm Atheros reference design for different matching networks.

3.8.3 Synthesizer characteristics

Table 3-9 summarizes the synthesizer characteristics for the QCA9887.

Table 3-9 Synthesizer Composite Characteristics for 5-GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pn	Phase noise (at Tx_Out)					
	At 30 KHz offset	—	—	-97	—	dBc/Hz
	At 100 KHz offset		—	-98	—	
	At 500 KHz offset		—	-103	—	
	At 1 MHz offset		—	-112	—	
F_C	Center channel frequency	Center frequency at 5 MHz spacing[1]	5.18	—	5.825	GHz
F_{ref}	Reference oscillator frequency	± 20 ppm[2]	—	40	—	MHz

1. Frequency is measured at the Tx output.
2. Over temperature variation and aging.

3.9 Power consumption parameters

These conditions apply to the typical characteristics unless otherwise specified:
V_{DD33} = 3.3V, T_{amb} = 25 °C

Table 3-10 through Table 3-12 show typical power consumption as a function of operating mode.

Table 3-10 Power consumption for 5 GHz operation (VHT20)[1]

Operating Mode	AVDD33	DVDD33	AVDD12	DVDD12	Unit
Tx (One-Chain[2]) with Internal PA	145	83	100	63	mA
Rx (Two-Chain)	46	27	95	69	mA

1. MCS8
2. Tx output power of 11 dBm

Table 3-11 Power consumption for 5 GHz operation (VHT40)[1]

Operating Mode	AVDD33	DVDD33	AVDD12	DVDD12	Unit
Tx (One-Chain[2]) with Internal PA	126	72	104	70	mA
Rx (One-Chain)	49	28	97	76	mA

1. MCS9
2. Tx output power of 10 dBm

Table 3-12 Power consumption for 5 GHz operation (VHT80)[1]

Operating Mode	AVDD33	DVDD33	AVDD12	DVDD12	Unit
Tx (One-Chain[2]) with Internal PA	114	65	126	82	mA
Rx (One-Chain)	52	30	126	87	mA

1. MCS9
2. Tx output power of 10 dBm

4 Mechanical Specifications

4.1 Device Physical Dimensions

Refer to the package specifications that correspond to the product's assembly site code.

Assembly site code (A)[1]	Package drawings and dimensions
E	Figure 4-1 and Table 4-1
K	Figure 4-2 and Table 4-2

1. Refer to Section 4.2 for the location of the assembly site code on the package

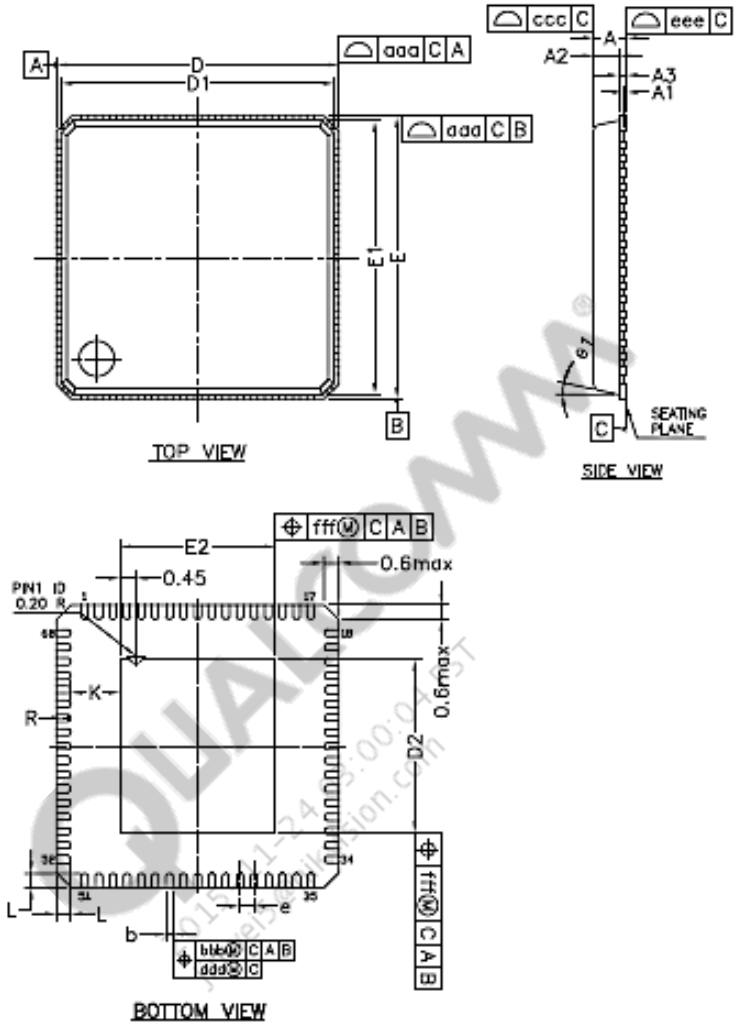


Figure 4-1 QCA9887 package details (assembly site E)

Table 4-1 Package Dimensions (assembly site E)

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm	0.031	0.033	0.035	inches
A1	0.00	0.02	0.05	mm	0.000	0.001	0.002	inches
A2	0.60	0.65	0.70	mm	0.024	0.026	0.028	inches
A3		0.20 REF		mm		0.008 REF		inches
b	0.15	0.20	0.25	mm	0.006	0.008	0.010	inches
D/E	7.90	8.00	8.10	mm	0.311	0.315	0.319	inches
D1/E1		7.75 BSC		mm		0.305 BSC		inches
D2	4.80	4.90	5.00	mm	0.189	0.193	0.197	inches
E2	4.30	4.40	4.50	mm	0.169	0.173	0.177	inches
e		0.40 BSC		mm		0.016 BSC		inches
L	0.30	0.40	0.50	mm	0.012	0.016	0.020	inches
θ	0°	—	14°	degrees	0°	—	14°	degrees
R	0.075	—	0.125	mm	0.003	—	0.005	inches
K	0.20	—	—	mm	0.008	—	—	inches
aaa		0.10		mm		0.004		inches
bbb		0.07		mm		0.003		inches
ccc		0.10		mm		0.004		inches
ddd		0.05		mm		0.002		inches
eee		0.08		mm		0.003		inches
fff		0.10		mm		0.004		inches

[1] Controlling dimension: Millimeters
[2] Reference Document: JEDEC MO-220

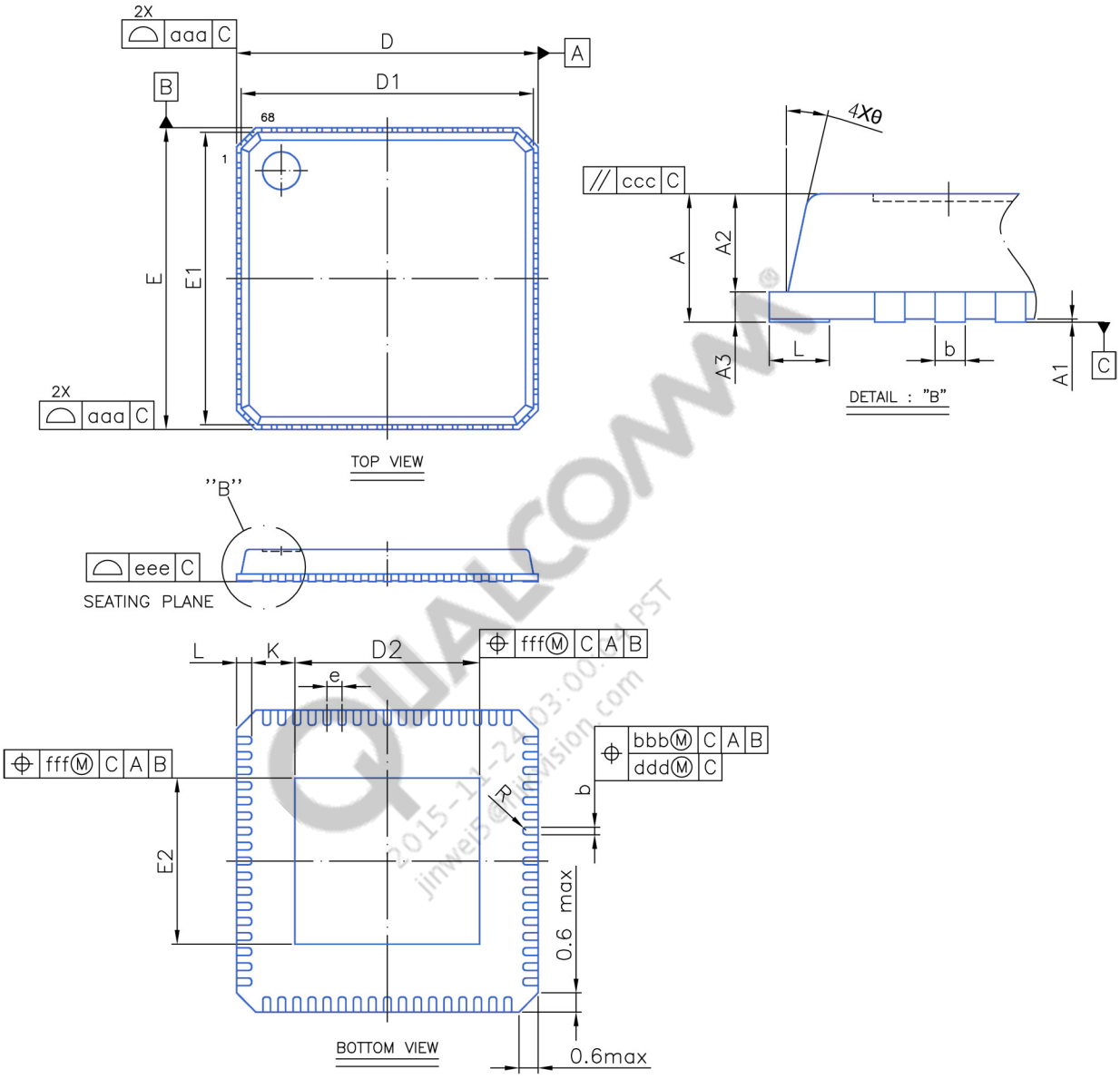


Figure 4-2 QCA9887 package details (assembly site K)

Table 4-2 Package Dimensions (assembly site K)

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm	0.031	0.033	0.035	inches
A1	0.00	0.02	0.05	mm	0.000	0.001	0.002	inches
A2	0.60	0.65	0.70	mm	0.024	0.026	0.028	inches
A3		0.20 REF		mm		0.008 REF		inches
b	0.15	0.20	0.25	mm	0.006	0.008	0.010	inches
D/E	7.90	8.00	8.10	mm	0.311	0.315	0.319	inches
D1/E1		7.75 BSC		mm		0.305 BSC		inches
D2	4.80	4.90	5.00	mm	0.189	0.193	0.197	inches
E2	4.30	4.40	4.50	mm	0.169	0.173	0.177	inches
e		0.40 BSC		mm		0.016 BSC		inches
L	0.30	0.40	0.50	mm	0.012	0.016	0.020	inches
θ	0°	—	14°	degrees	0°	—	14°	degrees
R	0.075	—	0.125	mm	0.003	—	0.005	inches
K	0.20	—	—	mm	0.008	—	—	inches
aaa		0.10		mm		0.004		inches
bbb		0.07		mm		0.003		inches
ccc		0.10		mm		0.004		inches
ddd		0.05		mm		0.002		inches
eee		0.08		mm		0.003		inches
fff		0.10		mm		0.004		inches

[1] Controlling dimension: Millimeters
[2] Reference Document: JEDEC MO-220

4.2 Part marking

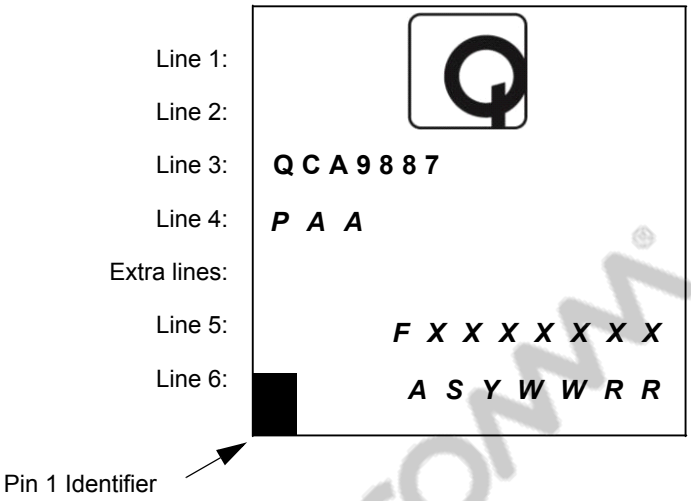


Figure 4-3 QCA9887 marking (top view, not to scale)

Table 4-3 QCA9887 marking line definitions

Line	Marking	Description
1 and 2	QUALCOMM	Qualcomm name or logo
3	QCA9887	Qualcomm product name
4	*PAA*	P = product configuration code AA = product feature code
5	*FXXXXXXX*	F = fab code XXXXXXX = traceability number
6	*ASYWWRR*	A = assembly site code S = assembly sequence number Y = single, last digit of year WW = work week (based on calendar year) RR = product revision
Additional lines may appear on the part marking for some samples; this is manufacturing information that is only relevant to Qualcomm and Qualcomm suppliers.		

4.3 Ordering Information

Order numbers have the form shown in Figure 4-4.

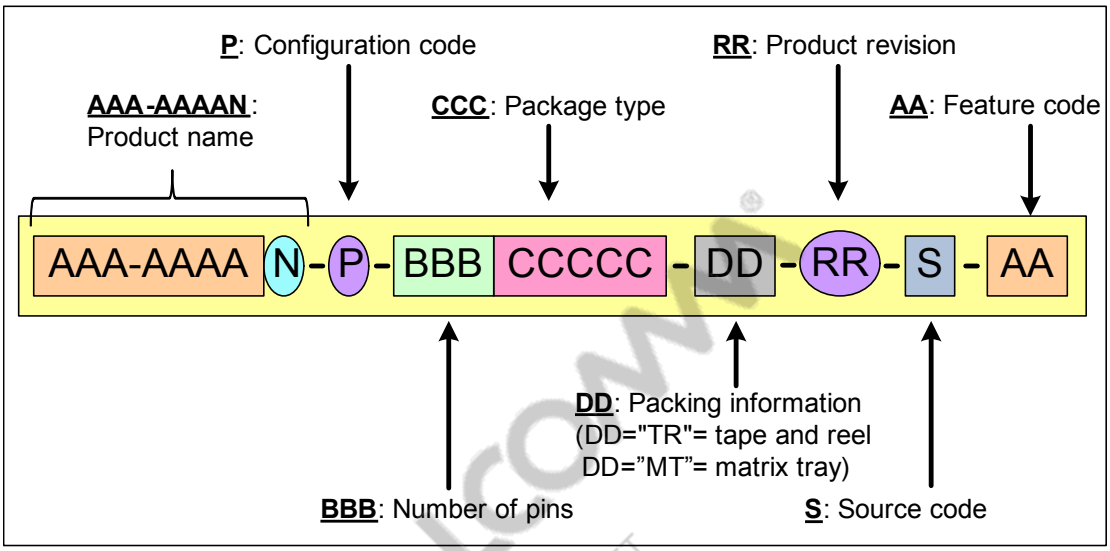


Figure 4-4 Device identification code

Table 4-4 shows the available order numbers.

Table 4-4 QCA9887 Order Numbers

Order Number	Description
QCA-9887-0-68BMQFN-MT-02-0	RoHS and BrCl-free
QCA-9887-0-68BMQFN-TR-02-0	RoHS and BrCl-free

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. Qualcomm follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. The QCA9887 is classified as MSL3; the qualification temperature was 255ºC.

4.5 Thermal characteristics

Table 4-5 Thermal Resistance

Parameter		Comment	Typical	Unit
θ_{JA}	Junction-to-Ambient	■ With 30 thermal vias ■ Jedec JESD51-2A ■ Jedec JESD51-5	28.15	°C/W
θ_{JB}	Junction-to-Board	■ With no thermal vias ■ Jedec JESD51-7 ■ Jedec JESD51-8	9.2	°C/W
θ_{JC}	Junction-to-Case	■ With no thermal vias ■ Jedec JESD51-7 ■ Jedec JESD51-8	5.83	°C/W

5 Carrier, Storage, and Handling

5.1 Carrier

5.1.1 Tape and reel information

Carrier tape system conforms to EIA-481 standards.

Simplified sketches of the QCA9887 tape carrier is shown in Figure 5-1 and Figure 5-2, including the part orientation. Tape and reel details for the QCA9887 are as follows:

- Reel diameter: 330 mm
- Hub size: 102 mm
- Tape width: 16 mm
- Tape pocket pitch: 12 mm
- Feed: Single
- Units per reel: 4000

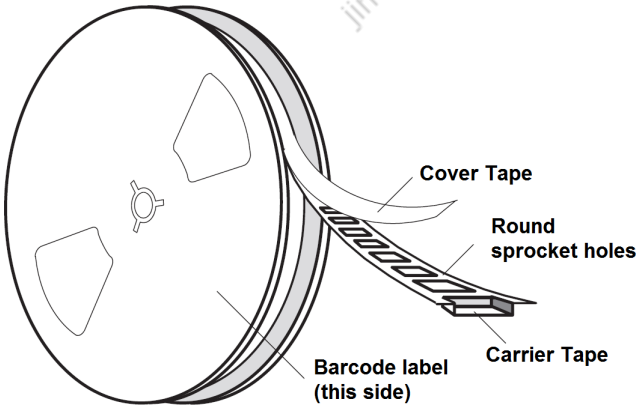


Figure 5-1 Tape orientation on reel

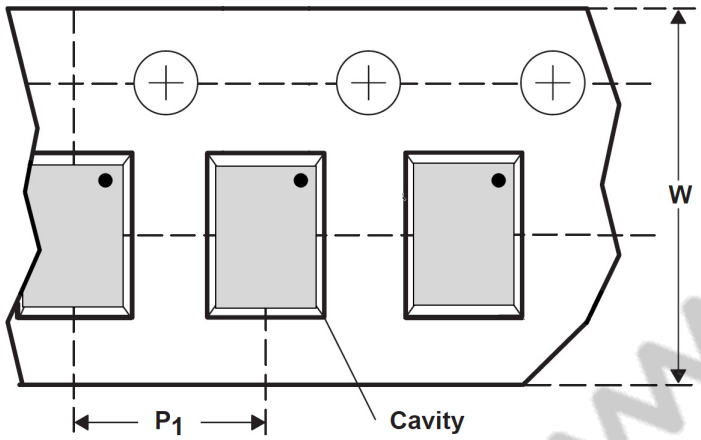
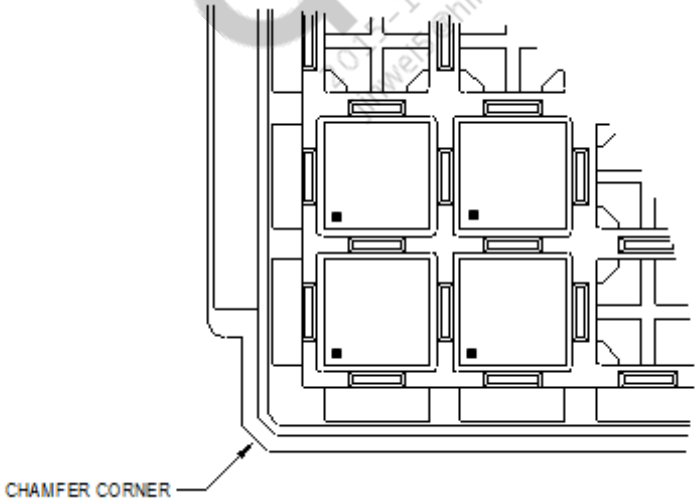


Figure 5-2 Part orientation in tape

5.1.2 Matrix tray information

Matrix tray carriers confirm to JEDEC standards. The device pin 1 is oriented to the chamfered corner of the matrix tray. Each tray of QCA9887 contains up to 260 devices. See Figure 5-3 for matrix-tray key attributes and dimensions.



Key dimensions	
Array	10 × 26 = 260
M	10.35 mm
M1	10.00 mm
M2	11.80 mm
M3	12.80 mm

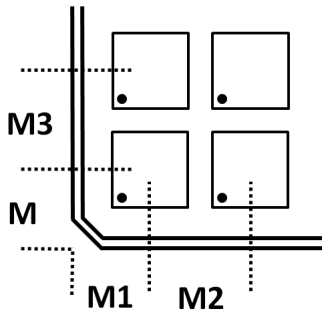


Figure 5-3 Matrix tray part orientation

5.2 Storage

5.2.1 Bagged storage conditions

QCA9887 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling is described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

It is **not necessary** to bake the QCA9887 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the QCA9887 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see *ASIC Packing Methods and Materials Specification* (80-VK055-1) for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Barcode label and packing for shipment

Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

6 PCB Mounting Guidelines

Guidelines for mounting the QCA9887 device onto a PCB are presented in this chapter, including land pad and stencil design details, surface mount technology (SMT) process characterization, and SMT process verification.

6.1 RoHS compliance

The QCA9887 device is externally lead-free and RoHS-compliant. Qualcomm defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products. A Product Material Declaration (PMD), which provides RoHS and other product environmental governance information, is available. Refer to *Product Material Declaration QCA9887* (80-Y0137-227D).

6.2 SMT parameters

This section describes board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

Qualcomm recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil-pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability. Review the land pattern and stencil pattern design recommendations as a guide for characterization:

PCB Land and Stencil Design Guide (LS90-NG134-1).

6.2.2 Reflow profile

Reflow profile conditions typically used by Qualcomm for lead-free systems are listed in Table 6-1 and are shown in Figure 6-1.

Table 6-1 Typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Dry-out and flux activation	150 to 190°C	60 to 120sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C. This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

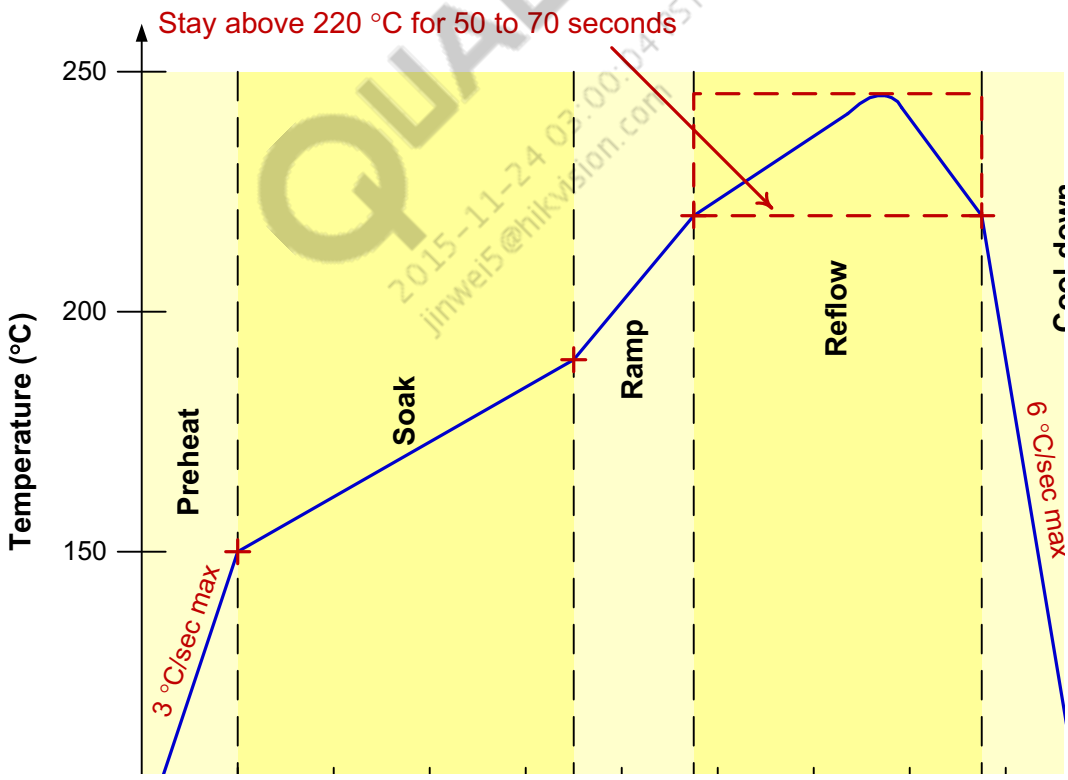


Figure 6-1 Typical SMT reflow profile

6.2.3 SMT peak package-body temperature

During a production board's reflow process, the temperature seen by the package must be controlled. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more). Although the solder-paste manufacturer's recommendations for optimum temperature and duration for solder reflow must be followed, the Qualcomm recommended limits must not be exceeded.

6.2.4 SMT process verification

Qualcomm recommends verification of the SMT process prior to high-volume board assembly, including:

- Electrical continuity
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume

6.3 Board-level reliability

Qualcomm conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

For board-level reliability data, refer to *Board-Level Reliability DRQFN/mQFN* (BR80-NT096-1).

7 Part Reliability

7.1 Reliability qualification summary

QCA9887 reliability evaluation report.

Table 7-1 Reliability Evaluation Results

Tests, standards, and conditions	Sample Size	Result
Average failure rate (AFR, λ) in FIT Failure in billion device-hours Functional HTOL: JESD22-A108	231	λ = 51 FIT[1]
Mean time to failure (MTTF, million hours) t = 1/λ	231	19.6
ESD - Human-body model (HBM) rating JESD22-A114	3	PASS[2]
ESD - Charge-device model (CDM) rating JESD22-C101-D	3	PASS[3]
Latch-up (I-test): EIA/JESD 78D Trigger current: ±100 mA; temperature: 85°C	6	PASS
Latch-up (Vsupply overvoltage): EIA/JESD 78D Trigger voltage: 1.5×; temperature: 85°C	6	PASS
Moisture resistance test (MRT): MSL 3, J-STD-020D 30C/60%RH, 192 hrs, 3xIR@260°C	1078	PASS
Temperature cycle: JESD22-A104 Temperature: -60°C to +150°C Number of cycles: 1000 Min soak time at min/max temperature: 5 minutes Cycle rate: 2 cycles per hour (cph) Preconditioning: JESD22-A113 MSL: 3; (30C/60%RH, 192 hrs, 3xIR@260°C)	462	PASS
Biased highly accelerated stress test (BHAST): JESD22-A110 Preconditioning: JESD22-A113 MSL: 3; (30C/60%RH, 192 hrs,3xIR@260°C)	77	PASS
Unbiased Highly Accelerated Stress Test (UHAST): JESD22-A118 Preconditioning: JESD22-A113 MSL: 3; (30C/60%RH, 192 hrs, 3xIR@260°C)	462	PASS

Table 7-1 Reliability Evaluation Results (cont.)

Tests, standards, and conditions	Sample Size	Result
High-Temperature Storage Life: JESD22-A103 Temperature 150°C, 1000 hours duration	462	PASS
Physical dimensions: JESD22-B100 Package outline drawing in Section 4.1	30	PASS
Solder ball shear stress test: JESD22-B117	N/A	N/A

1. Interim result. Final result to be updated when all data are available
2. ±2000 V. All pins except pins 55/56/57 and 63/64/65 pass ±1500 V
3. ±500 V. All pins

7.2 Qualification sample description

Table 7-2 QCA9887 characteristics

Device name	QCA9887
Package type	68 MQFN
Package body size	8 mm × 8 mm × 0.9 mm
Pin count	68
Pin composition	Sn
Process	55 nm