

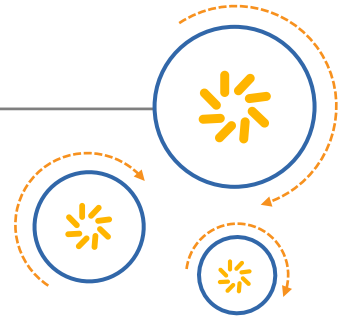
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QFE1922 2 GHz WLAN Front End

Device Specification

80-Y8641-2 Rev. H

February 18, 2016

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Revision history

Revision	Date	Description
A	August 2014	Initial release
B	August 2014	<ul style="list-style-type: none"> ■ Section 4 “Mechanical information”: Improved package description. ■ Table 4-2 “QFE1922 order numbers ”: Specified order numbers. ■ Section 5.1.2 “Matrix Tray Information”: New. ■ Section 5.3.2 “Electrostatic discharge”: Added preliminary test results.
C	October 2014	<ul style="list-style-type: none"> ■ Section 6 “PCB Mounting Guidelines”: New. ■ Table 2-2 “Pin descriptions”: IO Type of pin #20 is “Supply”.
D	December 2014	<ul style="list-style-type: none"> ■ Section 3.2 “Transmit Parameters”: Updated many parameters. ■ Section 3.3 “Receive Parameters”: Updated many parameters. ■ Section 5.3.2 “Electrostatic discharge”: Passes HBM. ■ Section 6.1 “RoHS Compliance”: Standardized wording.
E	March 2015	<ul style="list-style-type: none"> ■ Section 1.2 “QFE1922 features”: Supply voltage 3.5 V. ■ Figure 2-1 “Pin Map”: Pin 5 is NC. Supply voltage 3.5 V. ■ Table 2-2 “Pin Descriptions”: Pin 5 should be grounded. ■ Section 3.1 “Recommended operating conditions”: Operating temp. ■ Table 3-2 “Tx Parameters”: Several refinements to parameters. ■ Table 3-3 “Rx Parameters”: Several refinements to parameters. ■ Section 7 “Part Reliability”: New.
F	March 2015	<ul style="list-style-type: none"> ■ Section 3.1 “Recommended operating conditions”: Added T_{CASE}
G	September 2015	<ul style="list-style-type: none"> ■ Table 3-1 “Recommended operating conditions” and Table 3-2 “Tx Parameters”: Expanded operating temperature range.
H	February 2016	<ul style="list-style-type: none"> ■ Minor updates to Section 1.1 and Section 1.2 ■ Updated Table 3-1 “Recommended operating conditions” ■ Updated Table 3-3 “Rx parameters”

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1 Introduction

1.1 QFE1922 introduction

The QFE1922 is a fully integrated, single chip front end (FE) solution that supports 802.11 WLAN operation delivering high power, high linearity and high receiver sensitivity. Figure 1-1 provides a functional view of the chip architecture. QFE1922 integrates a power amplifier (PA), low noise amplifier (LNA), and transmit receive switch (TRSW) supporting 802.11 b/g/n/ac DBDC/DBS. QFE1922 has a dual channel feature to support band simultaneous (DBS) or dual band concurrency (DBC). The level of feature integration for this Si based device makes it an ideal solution for 4 x 4 MIMO access point (AP) applications.

The QFE1922 has mobile industry processor interface (MIPI) to communicate Wi-Fi SoC-to-program and optimize performance depending on the customers system implementation. MIPI in the QFE1922 configures this FE for high power mode (HPM) and mid-power mode (MPM) and is easily programmed through software.

Paired with Qualcomm's Wi-Fi SoC, the QFE1922 has digital predistortion (DPD) calibration to improve linearity of the FE on platform.

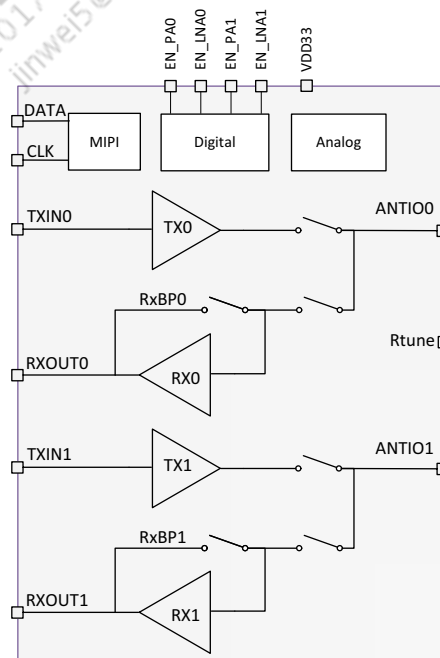


Figure 1-1 QFE1922 functional block diagram

1.2 QFE1922 features

- 2.4 GHz ISM band support
- Single chip RF front end for 802.11 b/g/n/ac (20/40 MHz)
- Integrates PA, LNA, TRSW
- Highest output power (23.5dBm for 802.11ac MCS0 HT20)
- Highest output power for MCS9 HT40 (16.5dBm, HO EVM = -40 dB)
- Supports high-power mode and mid-power mode Tx
- Supports high-gain mode and bypass mode for Rx
- Dual chain in a single package
- Single 3.3V supply
- Supports MIMO platform
- Supports dual band simultaneous (DBS) or dual band dual concurrency (DBDC)
- No external matching components required
- DC decoupled RF ports
- All ESD protected pins
- Supports MIPI v1 standard
- 50-ohm matched RF ports
- $3.5 \times 3.5 \text{ mm}^2$ 24-QFN package with exposed ground paddle
- SOI process for low cost

1.3 Terms and abbreviations

Table 1-1 defines terms, abbreviations, and acronyms commonly used throughout this document.

Table 1-1 Terms and abbreviations

Term	Definition
ANT	Antenna
CDM	Charge-device model
CW	Continuous wave
DBDC	Dual-band, dual-concurrent
DBS	Dual band simultaneous
DPD	Digital predistortion
ESD	Electrostatic discharge
EVM	Error vector magnitude
FE	Front end

Table 1-1 Terms and abbreviations (cont.)

Term	Definition
HPF	High-pass filter
ISM	Industrial, scientific, and medical (band)
LNA	Low-noise amplifier
LPF	Low-pass filter
MCS	Modulation and coding scheme
MIMO	Multiple-input and multiple-output
MIPI	Mobile industry processor interface
MSL	Moisture sensitivity level
MU	Multiuser
NF	Noise figure
PA	Power amplifier
RF	Radio frequency
SMT	Surface mount technology
SOI	Silicon on insulator
SU	Single user
TRSW	Transmit-receive switch
VHT80	80 MHz very high throughput

1.4 Special marks

Table 1-2 defines special marks used in this document.

Table 1-2 Special marks

Mark	Definition
0x0000	Hexadecimal numbers are identified with an x in the number, for example, 0x0000. All numbers are decimal (base 10), unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number, for example, 0011 (binary).
	A vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin Definitions

2.1 QFE1922 Pin map

Figure 2-1 shows a high-level view of the pin assignments.

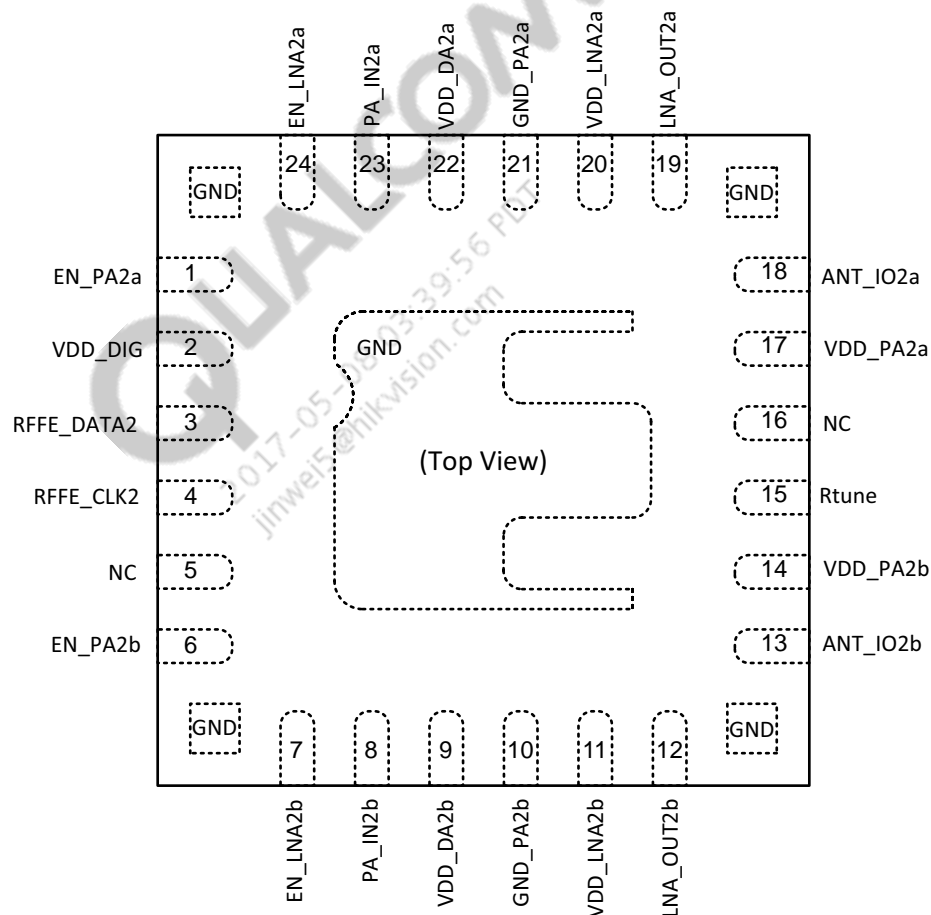


Figure 2-1 QFE1922 pin map

2.2 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Analog	
Digital	
GND	
NC	not used
RF IN	RF input
RF Out	RF output

2.3 Pin descriptions

Descriptions of pins are presented in [Table 2-2](#).

Table 2-2 QFE1922 pin descriptions

Pin #	Pin Name	IO Type	Functional Description
1	EN_PA2a	Digital	Enable PA for chain A
2	VDD_DIG	Supply	Supply for digital block (3.3 V)
3	RFFE_DATA2	Digital	MIPI data
4	RFFE_CLK2	Digital	MIPI clock
5	NC	NC	Only used for production test. Should be connected to ground.
6	EN_PA2b	Digital	Enable PA for chain B
7	EN_LNA2b	Digital	Enable LNA for chain B
8	PA_IN2b	RF IN	RF input for chain B
9	VDD_DA2b	Supply	3.3 V supply
10	GND_PA2b	GND	PA ground for PCB
11	VDD_LNA2b	Supply	3.3 V supply for LNA
12	LNA_OUT2b	RF Out	Rx output
13	ANT_IO2b	RF Out	RF chip output to Antenna
14	VDD_PA2b	Supply	3.3 V supply
15	Rtune	Analog	Connect high precision R for bias
16	NC	NC	not used
17	VDD_PA2a	Supply	3.3 V supply
18	ANT_IO2a	RF Out	RF chip output to antenna
19	LNA_OUT2a	Supply	Rx output

Table 2-2 QFE1922 pin descriptions

Pin #	Pin Name	IO Type	Functional Description
20	VDD_LNA2a	Supply	3.3 V supply for LNA
21	GND_PA2a	GND	PA ground for PCB
22	VDD_DA2a	Supply	3.3 V supply
23	PA_IN5a	RF IN	RF input for chain A
24	EN_LNA2a	Digital	Enable LNA for chain A

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3 Electrical Specifications

3.1 Recommended operating conditions

Operating the QFE1922 under conditions beyond its absolute maximum ratings (listed in [Table 3.1](#)) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, are not guaranteed or implied. Exposure may affect device reliability.

Table 3-1 Recommended operating conditions

Parameter	Min	Typ	Max	Unit	Comment
Operating temperature	-40	25	85	°C	Ambient temperature measured in still air inside test chamber
Maximum case temperature ¹	—	—	120	°C	T _{CASE}
Supply Voltage	3.1	3.3	3.5	V	Gain and EVM spec to meet
Operating frequency range	2.4	—	2.5	GHz	

1. Running two PAs at the same time for an hour under 45°C ambient with Qualcomm reference platform.

3.2 Transmit Parameters

Table 3-2 Tx Parameters

VDD = 3.3 V, room temperature (typical), over all frequencies unless specified

Parameters	Conditions	Min	Typ	Max	Units
Gain inband (high power)	Measured at MCS0 and MCS9 Pout	—	29.5	—	dB
Gain inband (medium power)	Measured at MCS0 and MCS9 Pout	—	24.0	—	dB
Gain flatness	For any 80MHz bandwidth (for 11ac VHT80 signals) over operating frequency range	—	±0.25	—	dB
NF		—	8.0	—	dB
EVM @ 1 Mbps (high power)	24.5 dBm (with DPD)	—	-21.0	—	dB
EVM @ 11 Mbps (high power)	24.5 dBm (with DPD)	—	-21.0	—	dB
EVM @ MCS0 (high power) HT20	23.5 dBm (with DPD)	—	-25.0	—	dB
EVM @ MCS7 (high power) HT20	18.5 dBm (with DPD)	—	-38.0	—	dB
EVM @ MCS9 (high power) HT20	17.5 dBm (with DPD)	—	-41.0	—	dB
EVM @ MCS0 (high power) HT40	22.5 dBm (with DPD)	—	-25.0	—	dB

Table 3-2 Tx Parameters (cont.)

VDD = 3.3 V, room temperature (typical), over all frequencies unless specified

Parameters	Conditions	Min	Typ	Max	Units
EVM @ MCS7 (high power) HT40	18.5 dBm (with DPD)	—	-38.0	—	dB
EVM @ MCS9 (high power) HT40	16.5 dBm (with DPD)	—	-41.0	—	dB
EVM @ MCS9 (high power) HT40 at -40°C and 85°C	14.0 dBm (with DPD)	—	-41.0	—	dB
EVM @ MCS0 (medium power) HT20	17.5 dBm (with DPD)	—	-25.0	—	dB
EVM @ MCS7 (medium power) HT20	12.5 dBm (with DPD)	—	-38.0	—	dB
EVM @ MCS9 (medium power) HT20	11.5 dBm (with DPD)	—	-41.0	—	dB
EVM @ MCS0 (medium power) HT40	16.5 dBm (with DPD)	—	-25.0	—	dB
EVM @ MCS7 (medium power) HT40	12.5 dBm (with DPD)	—	-38.0	—	dB
EVM @ MCS9 (medium power) HT40	10.5 dBm. (with DPD)	—	-41.0	—	dB
EVM @ MCS9 (low power) HT20 HT40	2.5 dBm. (with DPD)	—	-42.0	—	dB
2H	HT20 MCS0. Test case: 11b 1 Mbps and HT20 MCS0 max Pout	—	—	-19.0	dBm/1 MHz
3H	HT20 MCS0. As above.	—	—	-19.0	dBm/1 MHz
Supply Current	P _{OUT} = 24.5 dBm, 11b	—	397	—	mA
Supply Current	P _{OUT} = 23.5 dBm, MCS0	—	366	—	mA
Supply Current	P _{OUT} = 18.5 dBm, MCS7	—	270	—	mA
Supply Current	P _{OUT} = 17.5 dBm, MCS9	—	258	—	mA
Supply Current	P _{OUT} = 17.5 dBm, MCS0	—	165	—	mA
Supply Current	P _{OUT} = 2.5 dBm, MCS9	—	110	—	mA
Tx Enable/Disable Time	Timing relative to control signals	—	—	0.4	μs
Ruggedness	P _{IN} = -1 dBm, 10:1 VSWR, CW	No permanent damage			
Stability	P _{IN} = -1 dBm, 6:1 VSWR, CW, 1 MHz ~ 6 GHz,	All non-harmonic related spurs below -45 dBc/100 KHz			

3.3 Receive Parameters

Table 3-3 Rx Parameters

VDD = 3.3 V, room temperature (typical), over all frequencies unless specified

Parameters	Conditions	Min	Typ	Max	Units	Notes
NF	High gain mode	—	2.4	—	dB	
Gain	High gain mode	—	14.5	—	dB	
Gain flatness	For any 40 MHz bandwidth (for 11ac HT40 signals) over operating frequency range	—	±0.25	—	dB	
IIP3	High gain mode. Test case (input referred): inband 2-tone signal, each tone J = -25 dBm, IM3 = 3*J - 2*IIP3 = -85 dBm	—	6.0	—	dBm	
NF	Low gain mode	—	5.5	—	dB	
Gain	Low gain mode	—	-5.5	—	dB	1
Switching time	Timing relative to control signals	—		180.0	nS	2
		—		300.0	nS	3
IIP3	Low gain mode. Test case (input referred): inband 2-tone signal, each tone J = -5 dBm, IM3 = 3*J - 2*IIP3 = -67 dBm	—	35.0	—	dBm	4
Gain loss relative to inband f < 2170 MHz	Test case: CW signal sweep over frequency, power decreasing relative to in-band power	—	-1.3	—	dB	5
Gain loss relative to inband 2620 MHz - 2690 MHz		—	-1.5	—	dB	
Gain loss relative to inband 3400 MHz - 3800 MHz		—	-16.5	—	dB	
Gain loss relative to inband 4900 MHz - 5925 MHz		—	-40	—	dB	
Supply current (High Gain)		—	17.5	—	mA	
Supply current (Low Gain)		—	—	0.75	mA	

1. LNA bypass mode.
2. Rx switching time from High to Low Gain mode and back: from 90% RF to 10% RF and from 10% RF to 90% RF.
3. From Tx to Rx (high or low gain) and back: from 90% RF to 10% RF and from 10% RF to 90% RF.
4. LNA bypass mode.
5. Without external coex filter.

3.4 Mode Logic

Table 3-4 Mode Logic Table¹

EN_PA2x ²	EN_LNA2x ²	Operating condition	Comments
1	0	Normal Tx mode / DPD cal	Default setting is HPM. MPM can be set through MIPI software
0	1	Rx high-gain mode	
0	0	Rx bypass mode	
1	1	Beam forming cal	

1. Logic high (1) is 3.0 V or greater
2. "x" means either chain A or chain B

4 Mechanical Information

The QFE1922 uses 24-pin micro-quad-flat no-leads (24MQFN) package technology (see [Figure 4-1](#)). The 24MQFN package includes an exposed copper die pad for good grounding and thermal continuity.

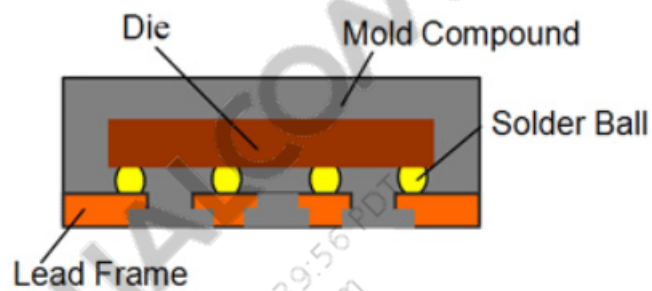
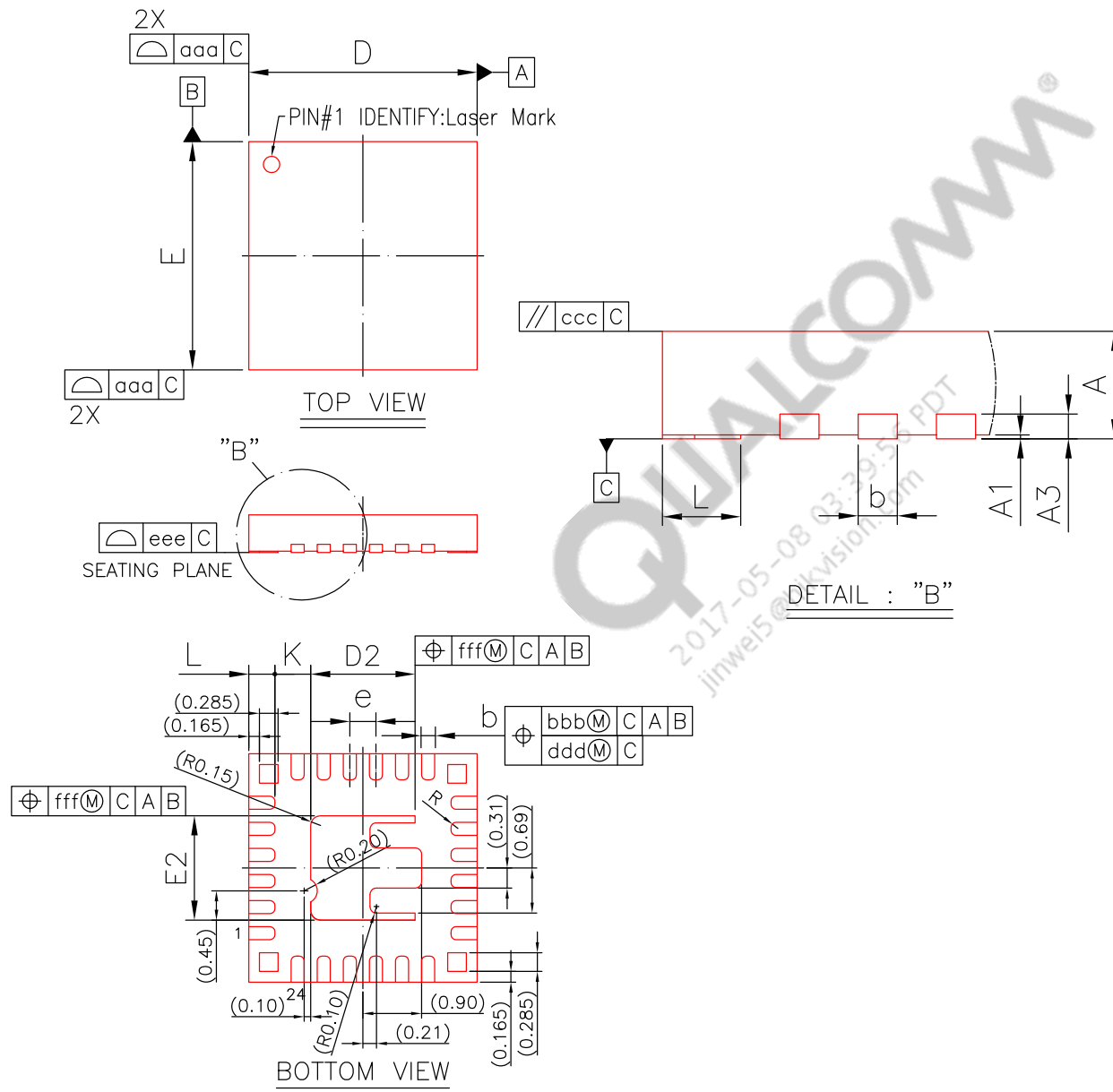


Figure 4-1 MQFN cut-away diagram

4.1 Device physical dimensions

[Figure 4-2](#) shows the package drawing and dimensions.



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.527	0.577	0.627	0.021	0.023	0.025
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.127 REF			0.005 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	3.40	3.50	3.60	0.134	0.138	0.142
E	3.40	3.50	3.60	0.134	0.138	0.142
D2	1.50	1.60	1.70	0.059	0.063	0.067
E2	1.50	1.60	1.70	0.059	0.063	0.067
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	0.125	0.003	---	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 4-2 QFE1922 24MQFN package details

4.2 Part marking

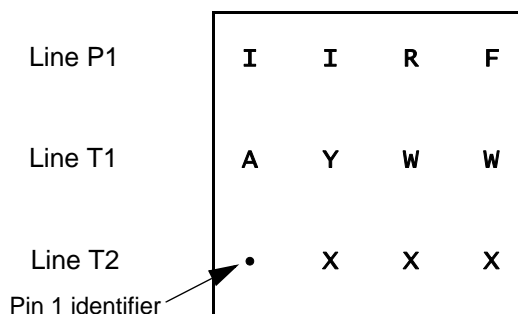


Figure 4-3 QFE1922 marking (top view, not to scale)

Table 4-1 QFE1922 marking line definitions

Line	Marking	Description
P1	IIRF	IIR = product code F = fab code
T1	AYWW	A = assembly site code Y = single, last digit of year WW = work week (based on calendar year)
T2	XXX	XXX = traceability number

4.3 Device ordering information

Order numbers have the form shown in Figure 4-4.

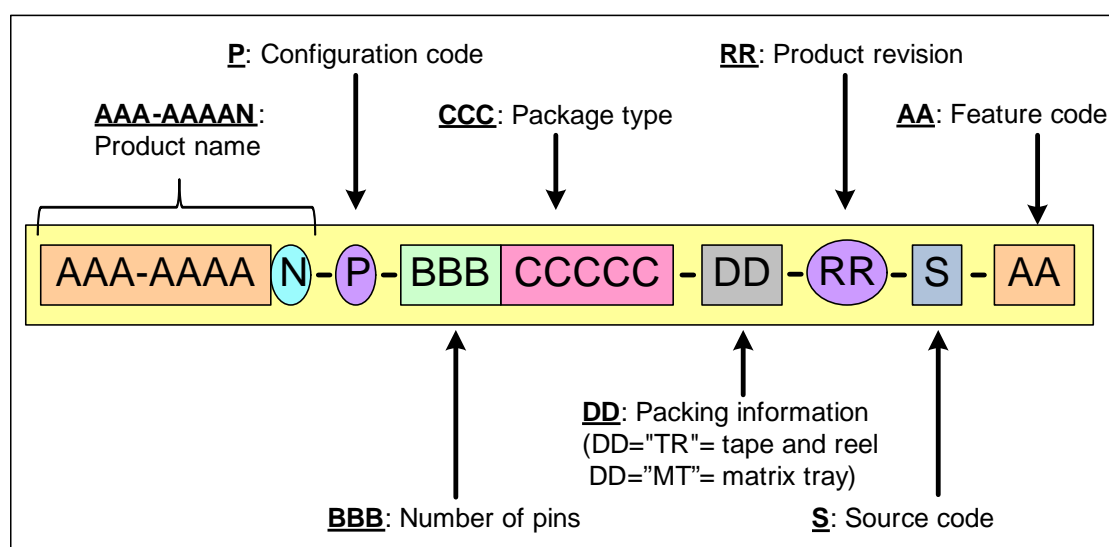


Figure 4-4 Device identification code

Table 4-2 shows the available order numbers.

Table 4-2 QFE1922 order numbers

Order number	Description
QFE-1922-0-24MQFN-MT-55-0	RoHS & BrCl-free
QFE-1922-0-24MQFN-TR-55-0	RoHS & BrCl-free

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. Qualcomm follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. The QFE1922 is classified as MSL3; the qualification temperature was 255°C.

5 Carrier, Storage, and Handling

5.1 Carrier

5.1.1 Tape and reel information

The carrier tape system conforms to EIA-481 standards.

Simplified sketches of the QFE1922 tape carrier are shown in [Figure 5-1](#) and [Figure 5-2](#), including the part orientation. Tape and reel details for the QFE1922 are as follows:

- Reel diameter: 330 mm
- Hub size: 178 mm
- Tape width: 12 mm
- Tape pocket pitch: 8 mm
- Feed: Single
- Units per reel: 4000

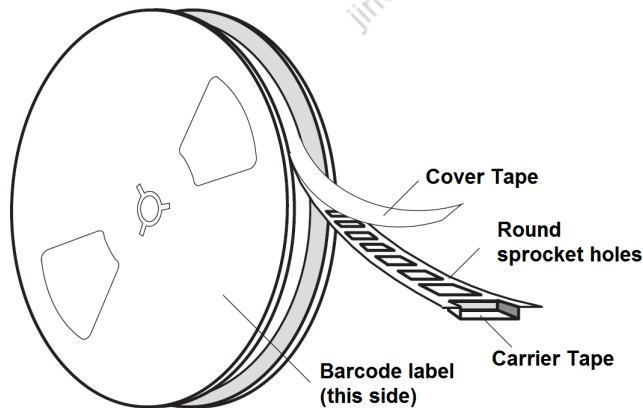


Figure 5-1 Tape orientation on reel

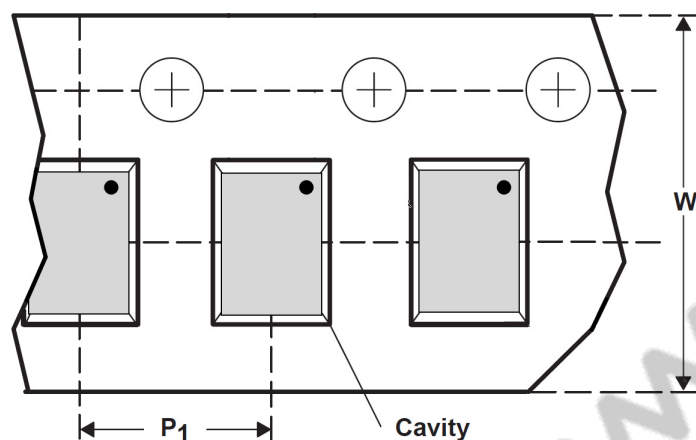


Figure 5-2 Part orientation in tape

5.1.2 Matrix tray information

Matrix tray carriers conform to JEDEC standards. The device pin 1 is oriented to the chamfered corner of the matrix tray. Each tray of QFE1922 contains up to 490 devices. See Figure 5-3 for matrix-tray key attributes and dimensions.

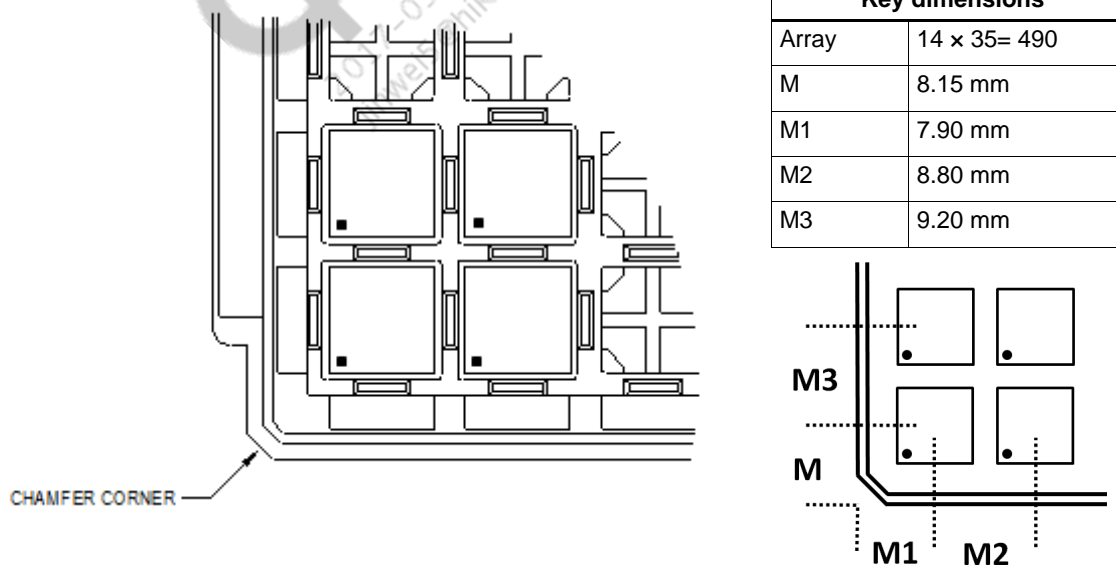


Figure 5-3 Matrix tray part orientation

5.2 Storage

5.2.1 Bagged storage conditions

QFE1922 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in [Section 4.4](#).

5.3 Handling

Tape handling is described in [Section 5.1.1](#). Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

It is **not necessary** to bake the QFE1922 if the conditions specified in [Section 5.2.1](#) and [Section 5.2.2](#) have **not been exceeded**.

It is **necessary** to bake the QFE1922 if any condition specified in [Section 5.2.1](#) or [Section 5.2.2](#) has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see *ASIC Packing Methods and Materials Specification* (80-VK055-1) for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

Current ESD performance for QFE1922 is:

- QFE1922 passes 500V charged device model (CDM) conditions.
- QFE1922 passes 2000 V human-body model (HBM) conditions for all pins.

5.4 Barcode label and packing for shipment

Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

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6 PCB Mounting Guidelines

Guidelines for mounting the QFE1922 device onto a PCB are presented in this chapter, including land pad and stencil design details, surface mount technology (SMT) process characterization, and SMT process verification.

6.1 RoHS compliance

The QFE1922 device is externally lead-free and RoHS-compliant. Qualcomm defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products.

6.2 SMT parameters

This section describes board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

Qualcomm recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil-pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability. Review the land pattern and stencil pattern design recommendations as a guide for characterization:

PCB Land and Stencil Design Guide (LS90-NG134-1).

6.2.2 Reflow profile

Reflow profile conditions typically used by Qualcomm for lead-free systems are listed in [Table 6-1](#) and are shown in [Figure 6-1](#).

Table 6-1 Typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Dry-out and flux activation	150 to 190°C	60 to 120sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C ¹	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C. This temperature should not be confused with the peak temperature reached during MSL testing, as described in [Section 6.2.3](#).

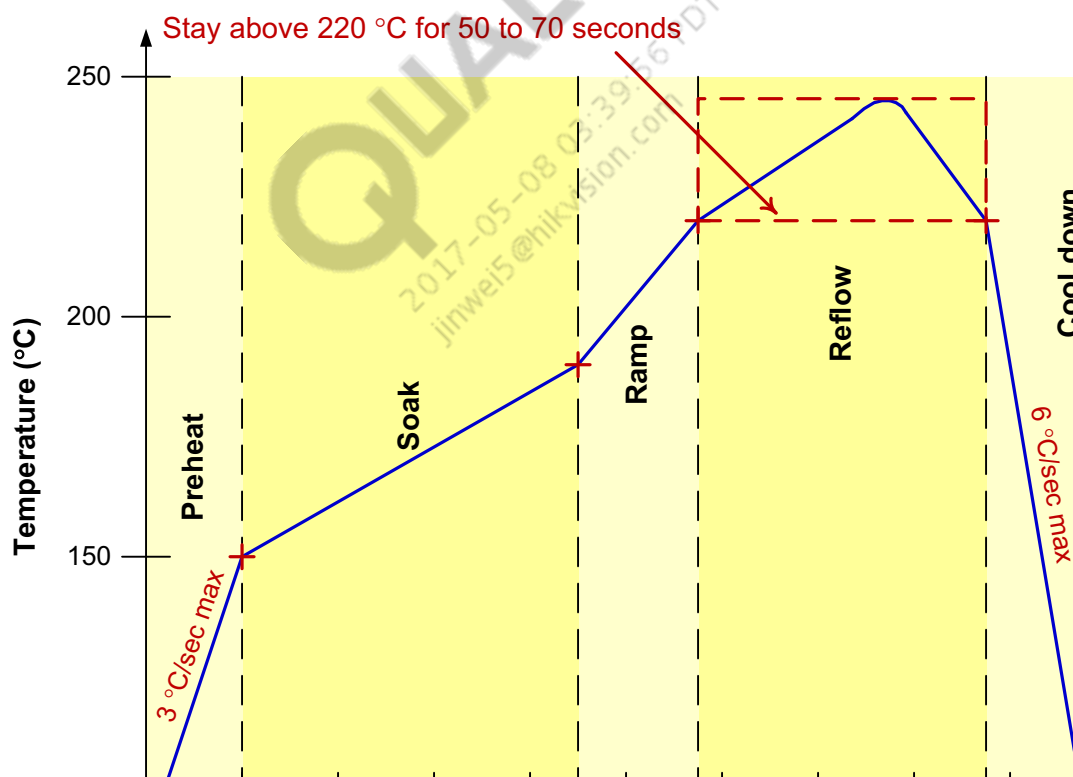


Figure 6-1 Typical SMT reflow profile

6.2.3 SMT peak package-body temperature

During a production board's reflow process, the temperature seen by the package must be controlled. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more). Although the solder-paste manufacturer's recommendations for optimum temperature and duration for solder reflow must be followed, the Qualcomm recommended limits must not be exceeded.

6.2.4 SMT process verification

Qualcomm recommends verification of the SMT process prior to high-volume board assembly, including:

- Electrical continuity
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume

6.3 Board-level reliability

Qualcomm conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

For board-level reliability data, refer to *Board-Level Reliability DRQFN/mQFN* (BR80-NT096-1).

7 Part Reliability

7.1 Reliability qualification summary

QFE1922 reliability evaluation report.

Table 7-1 Silicon Reliability Results

Tests, Standards and Conditions	Sample Size	Result
Average Failure Rate (AFR) in FIT (λ , Failure in billion device-hours) Dynamic HTOL: JESD22-A108-A	231	$\lambda = 95$ FIT, Pass Reachout ~ 10.5 yrs
Mean Time To Failure (MTTF) $t = 1/\lambda$ (Million Hours)	231	10.5 yrs
ESD – Human-Body Model (HBM) Rating; JESD22-A114-B	6	± 2 KV, all pins
ESD – Charge Device Model (CDM) Rating; JESD22-C101-D	6	500 V, All Pins
Latch-up (I-test): EIA/JESD 78 Trigger current: ± 100 ma; Temperature: 85°C	NA	
Latch-Up (V-supply Overvoltage): EIA/JESD78 Trigger voltage: $1.5 \times V_{dd}$; Temperature: 85°C	NA	

Table 7-2 Package Reliability Results

Tests, Standards and Conditions	Sample Size	Result
Moisture Resistance Test (MRT): MSL3; J-STD-020 3 × Reflow Cycles @ 255C +5/-0 °C 100% CSAM Delamination Inspection	960	Pass
Temperature Cycle: JESD22-A104 Temperature: -55C to +125C; Number of cycles: 1000 Soak time at min/max temperature: 20 minutes Cycle rate: 2 cycles per hour (cph) Preconditioning: MSL3; JESD22-A113 Reflow temperature: 255C +5/-0 °C	480	Pass
Unbiased Highly Accelerated Stress Test (UHAST) JESD22-A118 Preconditioning: MSL3; JESD22-A113 Reflow temperature: 255C +5/-0 °C	480	Pass
High Temperature Storage Life (HTS): JESD22-A103 Temperature = 150 °C, 1000 hours	480	Pass
Physical Dimensions: JESD22-B100-A Case Outline Drawing: BL90-Y6949/ BL90-Y6950	15	Pass
Die shear MIL-STD-883E, Method 2019	15	Pass

7.2 Qualification sample description

Table 7-3 QFE1922 characteristics

Device name	QFE1922
Package type	24MQFN
Package body size	3.5 mm × 3.5 mm × 0.627 mm
Pin count	24
Pin composition	Matte tin
Process	.18 μm
Pin pitch	0.40 mm