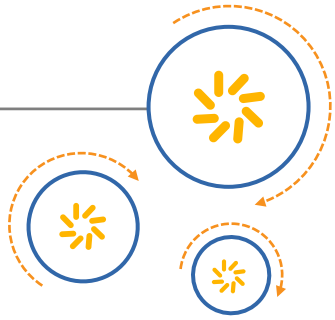
Qualcomm Atheros, Inc.



QFE1952 5 GHz WLAN Front End

Device Specification

80-Y8641-5 Rev. J

October 10, 2016

Qualcomm Atheros, Inc.
1700 Technology Drive
San Jose, CA 95110
U.S.A.

Revision history

Revision	Date	Description
A	August 2014	Initial release
B	August 2014	■ Section 4 “Mechanical Information”: Improved package description. ■ Table 4-2 “QFE1952 order numbers ”: Specified order numbers. ■ Section 5.1.2 “Matrix tray information”: New. ■ Section 5.3.2 “Electrostatic discharge”: Added preliminary test results.
C	October 2014	■ Section 6 “PCB Mounting Guidelines”: New. ■ Table 2-2 “Pin descriptions”: IO Type of pin #21 is “Supply”.
D	December 2014	■ Section 3.2 “Transmit Parameters”: Updated many parameters. ■ Section 3.3 “Receive Parameters”: Updated many parameters. ■ Section 5.3.2 “Electrostatic discharge”: Passes HBM ■ Section 6.1 “RoHS Compliance”: Standardized wording.
E	March 2015	■ Section 1.2 “QFE1952 features”: Supply voltage 3.5 V. ■ Figure 2-1 “QFE1952 pin map”: Pin #5 is NC. ■ Figure 2-2 “QFE1952 pin descriptions”: Pin #5 should be grounded. Supply voltage 3.5 V. ■ Section 3 “Electrical Specifications”: Many refinements. ■ Table 4-2 “QFE1952 order numbers”: Updated. ■ Section 5.3.2 “Electrostatic discharge”: Pin #5 conditions. ■ Section 7 “Part Reliability”: New.
F	September 2015	■ Table 3-1 “Recommended operating conditions”. Expanded operating temperature range. ■ Table 3-2 “Tx Parameters”: Refined EVM characteristics.
G	February 12, 2016	■ Minor updates to Section 1.1 and Section 1.2 ■ Updated Table 3-1 “Recommended operating conditions” ■ Updated Table 3-3 “Rx parameters”
H	February 29, 2016	■ Updated Section 1.2 QFE1952 features ■ Updated Table 2-2 QFE1952 pin descriptions
J	October 2016	■ Updated Table 3-2 Tx Parameters

Contents

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Tables

1 Introduction

1.1 QFE1952 introduction

The QFE1952 is a is a fully integrated, single chip front end (FE) solution that supports 802.11 WLAN operation delivering high power, high linearity and high receiver sensitivity. Figure 1-1 provides a functional view of the chip architecture. QFE1952 integrates a power amplifier (PA), low noise amplifier (LNA), transmit receive switch (TRSW), low pass filter (LPF), high pass filter (HPF) and coupler supporting 802.11 a/g/n/ac DBDC/DBS. QFE1952 has a dual channel feature to support dual band simultaneous (DBS) or dual band concurrency (DBC). The level of feature integration for this Si based device makes it an ideal solution for 4 x 4 MIMO access point (AP) applications.

The QFE1952 implements MIPI (Mobile Industry Processor Interface) to communicate Wi-Fi SoC parameters to software, enabling customization of performance and features depending on system implementation. MIPI in QFE1952 configures this FE for high power mode (HPM) and mid-power mode (MPM) and is easily programmed through software.

Paired with Qualcomm's Wi-Fi SoC, the QFE1952 has DPD (digital predistortion) calibration to improve linearity of the FE on platform.

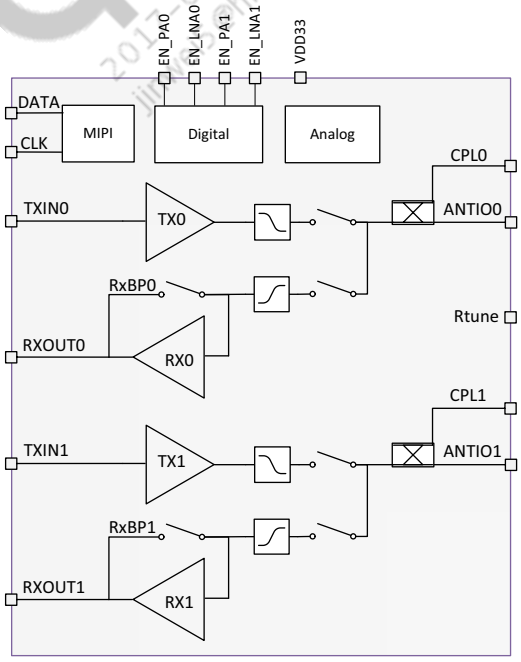


Figure 1-1 QFE1952 functional block diagram

1.2 QFE1952 features

- 5 GHz ISM band support
- Single chip RF front end for 802.11 a/g/n/ac (20/40/80 MHz BW)
- Integrates PA, LNA, TRSW, LPF (Tx), HPF (Rx), and Coupler
- Highest output power (22.5 dBm for 802.11ac MCS0 HT20)
- Highest output power for MCS9 HT80 (14.5 dBm, header only EVM = -41dB)
- Supports high-power mode and mid-power mode Tx
- Supports high-gain mode and bypass mode for Rx
- Dual chain in a single package
- 3.5V supply for analog block, 3.3V/3.5V supply for digital block
- Supports MIMO platform
- Supports DBS (dual band simultaneous) or DBDC (dual band dual concurrency)
- No external matching components required
- DC decoupled RF ports
- All ESD protected pins
- Supports MIPI v1 standard
- 3.9 × 3.5 mm^2 26-QFN package with exposed ground paddle

1.3 Terms and abbreviations

Table 1-1 defines terms, abbreviations, and acronyms commonly used throughout this document.

Table 1-1 Terms and abbreviations

Term	Definition
ANT	Antenna
CDM	Charge-device model
CW	Continuous wave
DBDC	Dual-band, dual-concurrent
DBS	Dual band simultaneous
DPD	Digital predistortion
ESD	Electrostatic discharge
EVM	Error vector magnitude
FE	Front end
HPF	High-pass filter
ISM	Industrial, scientific, and medical (band)

Table 1-1 Terms and abbreviations (cont.)

Term	Definition
LNA	Low-noise amplifier
LPF	Low-pass filter
MCS	Modulation and coding scheme
MIMO	Multiple-input and multiple-output
MIPI	Mobile industry processor interface
MSL	Moisture sensitivity level
MU	Multiuser
NF	Noise figure
PA	Power amplifier
RF	Radio frequency
SMT	Surface mount technology
SOI	Silicon on insulator
SU	Single user
TRSW	Transmit-receive switch
VHT80	80 MHz very high throughput

1.4 Special marks

Table 1-2 defines special marks used in this document.

Table 1-2 Special marks

Mark	Definition
0x0000	Hexadecimal numbers are identified with an x in the number, for example, 0x0000. All numbers are decimal (base 10), unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number, for example, 0011 (binary).
|	A vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin Definitions

2.1 QFE1952 pin map

Figure 2-1 shows a high-level view of the pin assignments.

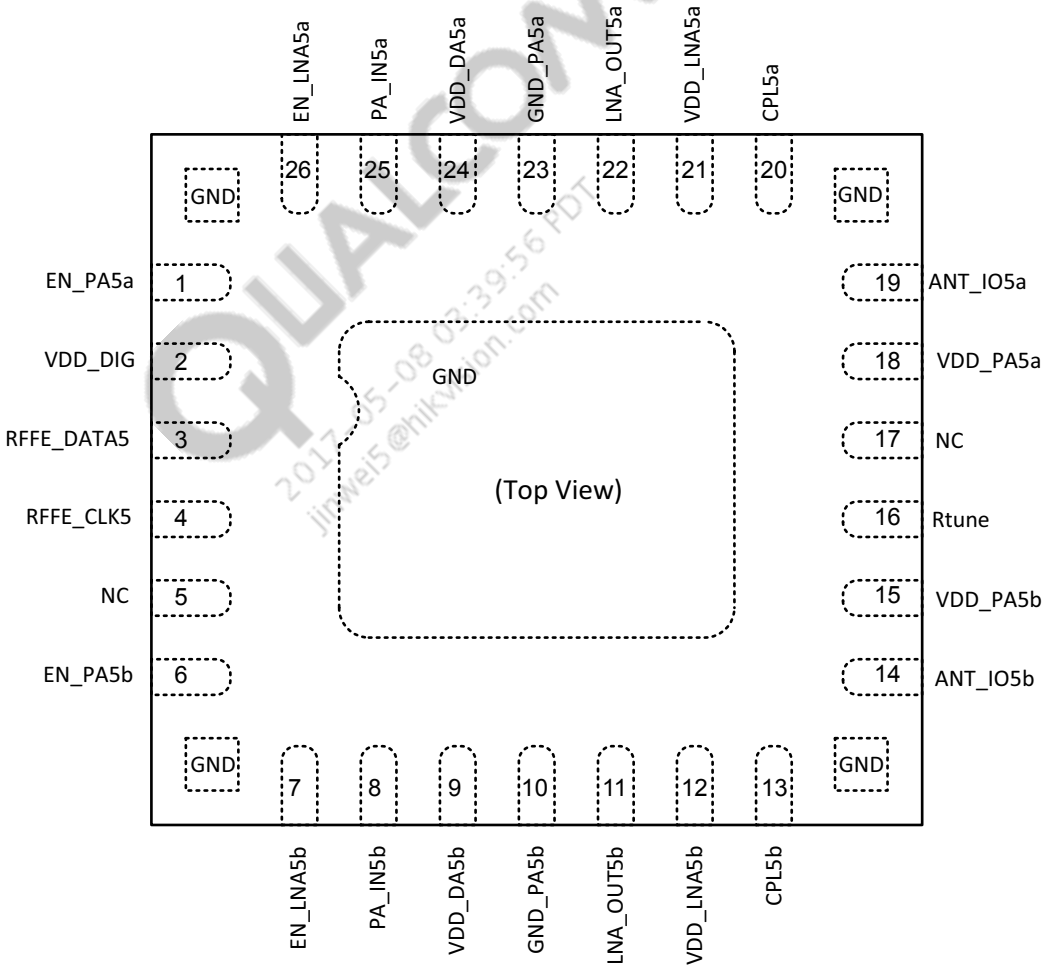


Figure 2-1 QFE1952 pin map

2.2 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Analog	
Digital	
GND	
NC	not used
RF IN	RF input
RF Out	RF output

2.3 Pin descriptions

Descriptions of pins are presented in Table 2-2.

Table 2-2 QFE1952 pin descriptions

Pin #	Pin Name	IO Type	Functional Description
1	EN_PA5a	Digital	Enable PA for chain A
2	VDD_DIG	Digital Supply	3.3 V or 3.5 V for digital block
3	RFFE_DATA5	Digital	MIPI data
4	RFFE_CLK5	Digital	MIPI clock
5	NC	NC	Only used for production test; should be connected to ground
6	EN_PA5b	Digital	Enable PA for chain B
7	EN_LNA5b	Digital	Enable LNA for chain B
8	PA_IN5b	RF IN	RF input
9	VDD_DA5b	Analog Supply	3.5 V supply
10	GND_PA5b	GND	PA ground for pcb
11	LNA_OUT5b	Analog Supply	Rx output
12	VDD_LNA5b	RF Out	3.5V supply for LNA
13	CPL5b	RF Out	Coupler output
14	ANT_IO5b	RF Out	RF chip output to antenna
15	VDD_PA5b	Analog Supply	3.5V supply
16	Rtune	Analog	Connect high precision R for bias
17	NC	NC	not used
18	VDD_PA5a	Analog Supply	3.5V supply
19	ANT_IO5a	RF Out	RF chip output to antenna
20	CPL5a	RF Out	Coupler output
21	VDD_LNA5a	Analog Supply	3.5V supply for LNA
22	LNA_OUT5a	Analog Supply	Rx output
23	GND_PA5a	GND	PA ground for pcb
24	VDD_DA5a	Analog Supply	3.5V supply
25	PA_IN5a	RF IN	RF input
26	EN_LNA5a	Digital	Enable LNA for chain A

3 Electrical Specifications

3.1 Recommended operating conditions

Operating the QFE1952 in conditions beyond its absolute maximum ratings (listed in Table 3-1) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, are not guaranteed or implied. Exposure may affect device reliability.

Table 3-1 Recommended operating conditions

Parameter	Min.	Typ.	Max.	Unit	Comment
Operating temperature	-40	25	85	°C	Ambient temperature measured in still air inside test chamber
Max case temperature[1]	—	—	120	°C	T_{CASE}
Supply Voltage	3.3	3.5	3.7	V	Gain and EVM spec to meet
Operating frequency range	4.9	—	5.9	GHz	

1. Running two PAs at the same time for an hour under 45°C ambient with Qualcomm reference platform.

3.2 Transmit parameters

Table 3-2 Tx Parameters

VDD = 3.5 V, room temperature (typical), over all frequencies unless specified

Parameters	Conditions	Min	Typ	Max	Units	Notes
Gain in-band (high power)	Measured at MCS0 and MCS9 Pout	—	25.5	—	dB	
Gain in-band (medium power)	Measured at MCS0 and MCS9 Pout	—	20.5	—	dB	
Gain flatness	For any 80MHz bandwidth (for 11ac VHT80 signals) over operating frequency range	—	±0.3	—	dB	
NF		—	8.0	—	dB	
EVM @ MCS0 (high power) HT20	22.5 dBm (with DPD)	—	-23.0	—	dB	1
EVM @ MCS7 (high power) HT20	17.5 dBm (with DPD)	—	-38.0	—	dB	
EVM @ MCS9 (high power) HT20	16.5 dBm (with DPD)	—	-40.0	—	dB	

Table 3-2 Tx Parameters (cont.)

VDD = 3.5 V, room temperature (typical), over all frequencies unless specified

Parameters	Conditions	Min	Typ	Max	Units	Notes
EVM @ MCS0 (high power) HT40	21.5 dBm (with DPD)	—	-25.0	—	dB	
EVM @ MCS7 (high power) HT40	17.5 dBm (with DPD)	—	-38.0	—	dB	
EVM @ MCS9 (high power) HT40	15.5 dBm (with DPD)	—	-40.0	—	dB	
EVM @ MCS0 (high power) HT80	20.5 dBm (with DPD)	—	-25.0	—	dB	1
EVM @ MCS7 (high power) HT80	17.5 dBm (with DPD)	—	-38.0	—	dB	
EVM @ MCS9 (high power) HT80	14.5 dBm (with DPD) (SU MIMO)	—	-39.5	—	dB	
	13.5 dBm (with DPD) (MU MIMO)	—		—		
EVM @ MCS9 (high power) HT80 at -40°C and 85°C	12.0 dBm (with DPD)	—	-39.5	—		1,2
EVM @ MCS0 (medium power) HT20	16.5 dBm (with DPD)	—	-25.0	—	dB	1
EVM @ MCS7 (medium power) HT20	11.5 dBm (with DPD)	—	-38.0	—	dB	
EVM @ MCS9 (medium power) HT20	10.5 dBm (with DPD)	—	-40.0	—	dB	
EVM @ MCS0 (medium power) HT40	15.5 dBm (with DPD)	—	-25.0	—	dB	
EVM @ MCS7 (medium power) HT40	11.5 dBm (with DPD)	—	-38.0	—	dB	
EVM @ MCS9 (medium power) HT40	9.5 dBm (with DPD)	—	-40.0	—	dB	
EVM @ MCS0 (medium power) HT80	14.5 dBm (with DPD)	—	-25.0	—	dB	
EVM @ MCS7 (medium power) HT80	11.5 dBm (with DPD)	—	-38.0	—	dB	
EVM @ MCS9 (medium power) HT80	8.5 dBm (with DPD)	—	-39.5	—	dB	
EVM @ MCS9 (low power) HT20 HT40 HT80	1.5 dBm (with DPD)	—	-40.0	—	dB	
2H	HT20 MCS0	—	-25.0	—	dBm/ 1MHz	3
3H	HT20 MCS0	—	-45.0	—	dBm/ 1MHz	
Supply Current	P_{OUT} = 22.5 dBm, MCS0	—	420	—	mA	4
Supply Current	P_{OUT} = 17.5 dBm, MCS7	—	285	—	mA	
Supply Current	P_{OUT} = 16.5 dBm, MCS9	—	270	—	mA	
Supply Current	P_{OUT} = 16.5 dBm, MCS0	—	240	—	mA	5
Supply Current	P_{OUT} = 1.5 dBm, MCS9	—	130	—	mA	
Tx Enable/Disable Time	Timing relative to control signals	—		0.4	uS	6
Ruggedness	P_{IN} = -3 dBm, 8:1 VSWR, CW	No permanent damage				
Stability	P_{IN} = -3 dBm, 4:1 VSWR, CW, 1 MHz ~ 10 GHz	All non-harmonic related spurs below -42 dBc/100 kHz				

1. Header Only (HO) Dynamic EVM (64uS 90% duty cycle)
2. For -40°C and 85°C, output power is backed off by 2.5 dBm to have same EVM performance
3. Pmax, all channels
4. High power
5. Medium power
6. To 90% of P_{NOM} to 10% of P_{NOM}

3.3 Receive parameters

Table 3-3 Rx Parameters

VDD = 3.5 V, room temperature (typical), over all frequencies unless specified

Parameters	Conditions	Min	Typ	Max	Units	Notes
NF	High gain mode	—	3.3	—	dB	
Gain	High gain mode	—	13	—	dB	
Gain flatness	For any 80 MHz bandwidth (for 11ac VHT80 signals) over operating frequency range	—	0.3	—	dB	
IIP3	High gain mode. Test case (input referred): inband 2-tone signal, each tone J = -25 dBm, measured IM3 = 3*J - 2*IIP3 = -87 dBm	-3	—	—	dBm	
NF	Low gain mode	—	6	—	dB	
Gain	Low gain mode	—	-6	—	dB	1
IIP3	Low gain mode. Test case (input referred): inband 2-tone signal, each tone J = -5 dBm, measured IM3 = 3*J - 2*IIP3 = -67 dBm	—	22.0	—	dBm	
Switching time	Timing relative to control signals	—	—	180.0	nS	2
		—	—	300.0	nS	3
LNA block out of band IIP2	For 2400 < f < 2484 MHz. Test case: (input referred): 2G CW signal, tone J = -10 dBm, measured in 5 G band; IM2 = 2*J - IIP2 - 3 = -47 dBm	55.5	—		dBm	4
Gain loss relative to in-band f < 3800 MHz	Test case: CW signal sweep over frequency, power decreasing relative to in-band power	—	—	-5	dB	5
Gain loss relative to in-band f < 2.7 GHz		—	—	-26	dB	
Gain loss relative to in-band f < 2.5 GHz		—	—	-30	dB	
Supply current (High Gain)		—	16.0	—	mA	
Supply current (Low Gain)		—	1.5	—	mA	

1. LNA bypass mode.
2. Rx switching time from High to Low Gain mode and back: from 90% RF to 10% RF and from 10% RF to 90% RF. LNA_EN toggling only, PA_EN=0.
3. From Tx to Rx (High Gain) and back (from High or Low Gain): from 90% RF to 10% RF and from 10% RF to 90% RF. PA_EN and LNA_EN are toggled.
4. Including LNA matching circuits, including integrated 5 G coex filter. Normal Rx mode for high mode.
5. Including integrated 5 G coex filter.

3.4 Mode logic

Table 3-4 Mode Logic Table[1]

EN_PA5x[2]	EN_LNA5x[2]	Operating condition	Comments
1	0	Normal Tx mode / DPD cal	Default setting is HPM. MPM can be set through MIPI software
0	1	Rx High gain mode	
0	0	Rx Bypass mode	
1	1	Beam forming cal	

1. Logic high (1) is 3.0 V or greater
2. “x” means either chain A or chain B

4 Mechanical Information

The QFE1952 uses 26-pin micro-quad-flat no-leads (26MQFN) package technology (see Figure 4-1). The 26MQFN package includes an exposed copper die pad for good grounding and thermal continuity.

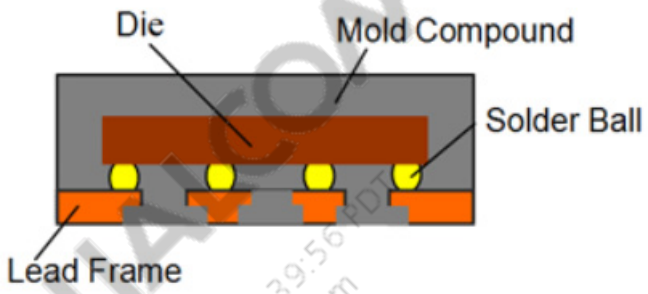
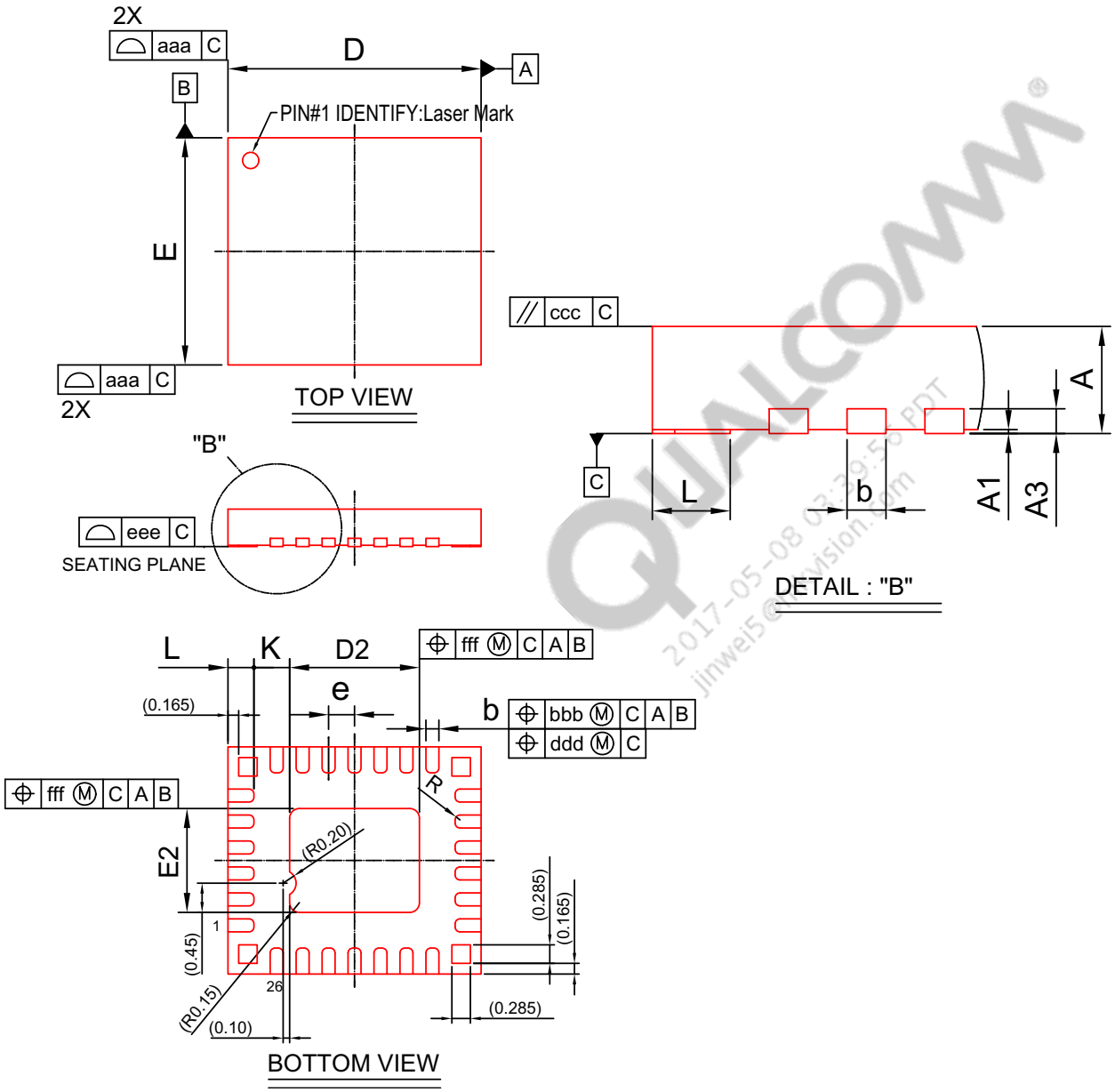


Figure 4-1 MQFN cut-away diagram

4.1 Device physical dimensions

Figure 4-2 shows the package drawing and dimensions.



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.527	0.577	0.627	0.021	0.023	0.025
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.127 REF			0.005 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	3.80	3.90	4.00	0.150	0.154	0.157
E	3.40	3.50	3.60	0.134	0.138	0.142
D2	1.90	2.00	2.10	0.075	0.079	0.083
E2	1.50	1.60	1.70	0.059	0.063	0.067
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	0.125	0.003	---	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 4-2 QFE1952 26MQFN package details

4.2 Part marking

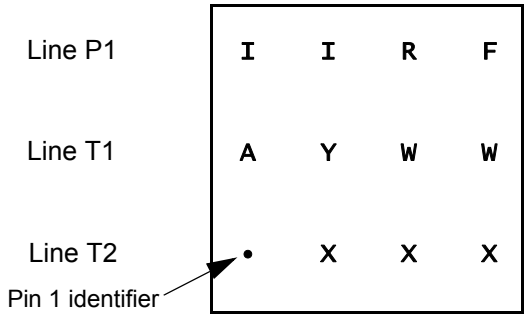


Figure 4-3 QFE1952 marking (top view, not to scale)

Table 4-1 QFE1952 marking line definitions

Line	Marking	Description
P1	*IIRF*	IIR = product code F = fab code
T1	*AYWW*	A = assembly site code Y = single, last digit of year WW = work week (based on calendar year)
T2	*XXX*	XXX = traceability number

4.3 Device ordering information

Order numbers have the form shown in Figure 4-4.

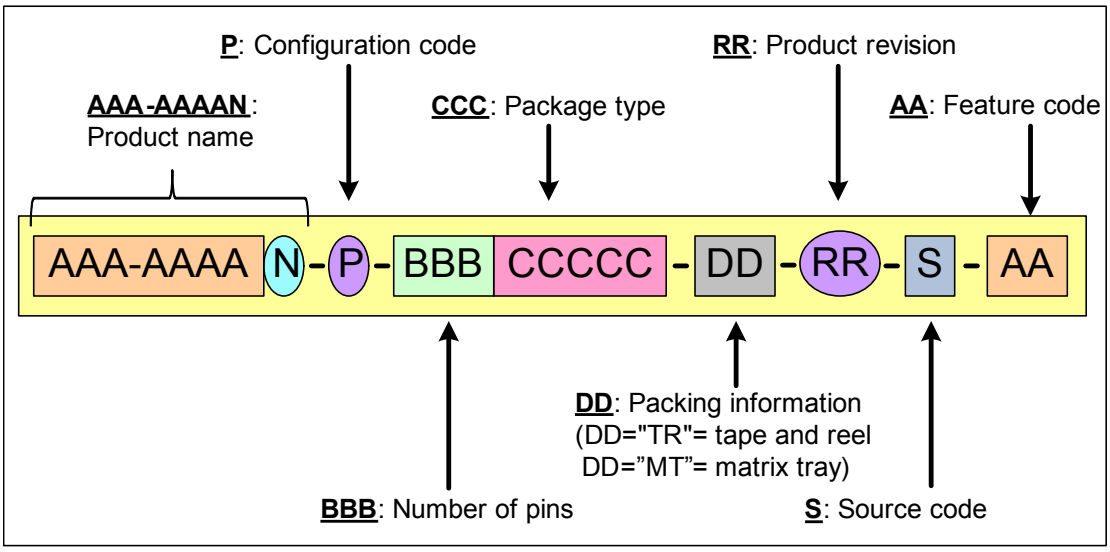


Figure 4-4 Device identification code

Table 4-2 shows the available order numbers.

Table 4-2 QFE1952 order numbers

Order number	Description
QFE-1952-0-26MQFN-MT-65-0	RoHS & BrCl-free
QFE-1952-0-26MQFN-TR-65-0	RoHS & BrCl-free

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. Qualcomm follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. The QFE1952 is classified as MSL3; the qualification temperature was 255ºC.

5 Carrier, Storage, and Handling

5.1 Carrier

5.1.1 Tape and reel information

The carrier tape system conforms to EIA-481 standards.

A simplified sketches of the QFE1952 tape carrier are shown in Figure 5-1 and Figure 5-2, including the part orientation. Tape and reel details for the QFE1952 are as follows:

- Reel diameter: 330 mm
- Hub size: 178 mm
- Tape width: 12 mm
- Tape pocket pitch: 8 mm
- Feed: Single
- Units per reel: 4000

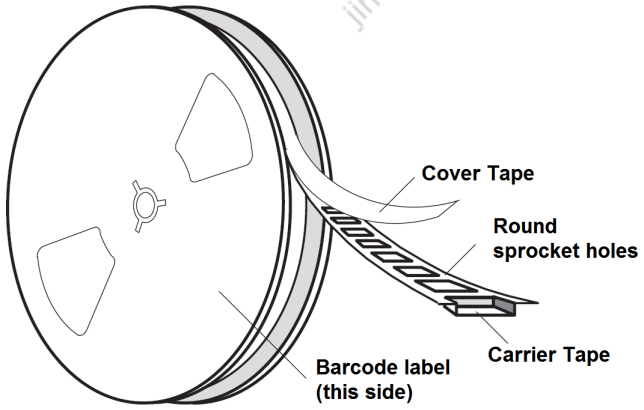


Figure 5-1 Tape orientation on reel

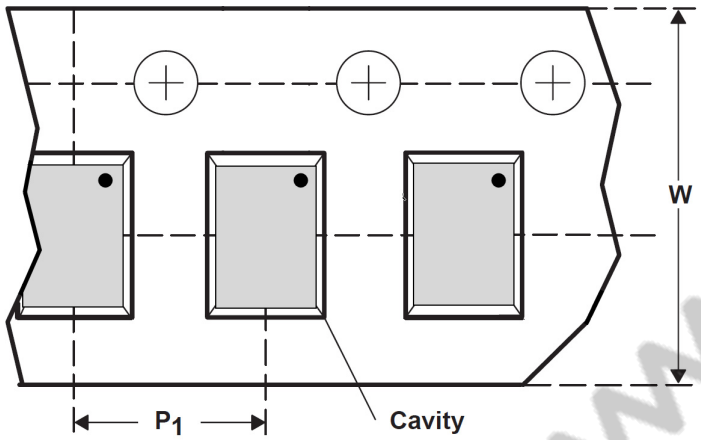
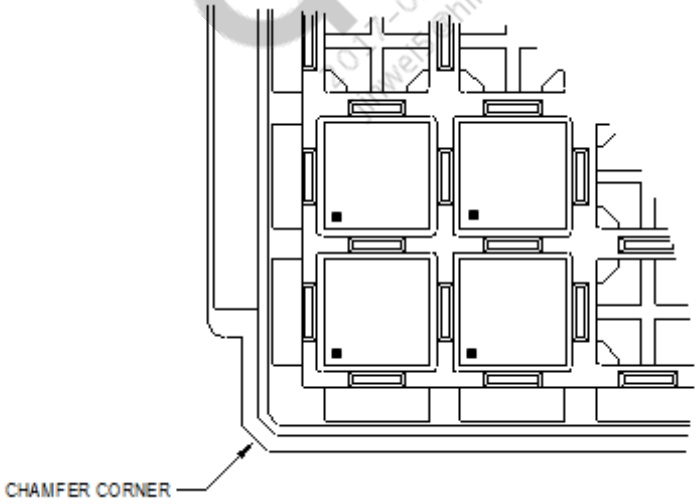


Figure 5-2 Part orientation in tape

5.1.2 Matrix tray information

Matrix tray carriers confirm to JEDEC standards. The device pin 1 is oriented to the chamfered corner of the matrix tray. Each tray of QFE1952 contains up to 490 devices. See Figure 5-3 for matrix-tray key attributes and dimensions.



Key dimensions	
Array	14 × 35= 490
M	8.15 mm
M1	7.90 mm
M2	8.80 mm
M3	9.20 mm

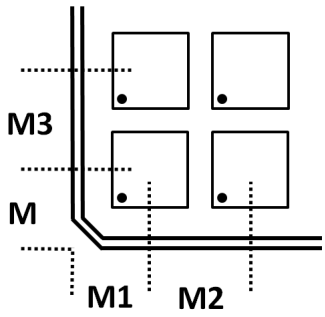


Figure 5-3 Matrix tray part orientation

5.2 Storage

5.2.1 Bagged storage conditions

QFE1952 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling is described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

It is **not necessary** to bake the QFE1952 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the QFE1952 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see *ASIC Packing Methods and Materials Specification* (80-VK055-1) for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

Current preliminary ESD performance for QFE1952 is:

- QFE1952 passes 500 V charged device model (CDM) conditions.
- QFE1952 passes 2000 V human-body model (HBM) conditions for all pins except pin #5 (NC).
  - Pin #5 passes ±1.5 KV HBM conditions.
  - By connecting pin #5 to solid ground on the board, it passes ±2 KV HBM.
  - More data is available upon request.

5.4 Barcode label and packing for shipment

Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

6 PCB Mounting Guidelines

Guidelines for mounting the QFE1952 device onto a PCB are presented in this chapter, including land pad and stencil design details, surface mount technology (SMT) process characterization, and SMT process verification.

6.1 RoHS compliance

The QFE1952 device is externally lead-free and RoHS-compliant. Qualcomm defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products.

6.2 SMT parameters

This section describes board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

Qualcomm recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil-pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability. Review the land pattern and stencil pattern design recommendations as a guide for characterization:

PCB Land and Stencil Design Guide (LS90-NG134-1).

6.2.2 Reflow profile

Reflow profile conditions typically used by Qualcomm for lead-free systems are listed in Table 6-1 and are shown in Figure 6-1.

Table 6-1 Typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Dry-out and flux activation	150 to 190°C	60 to 120sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C. This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

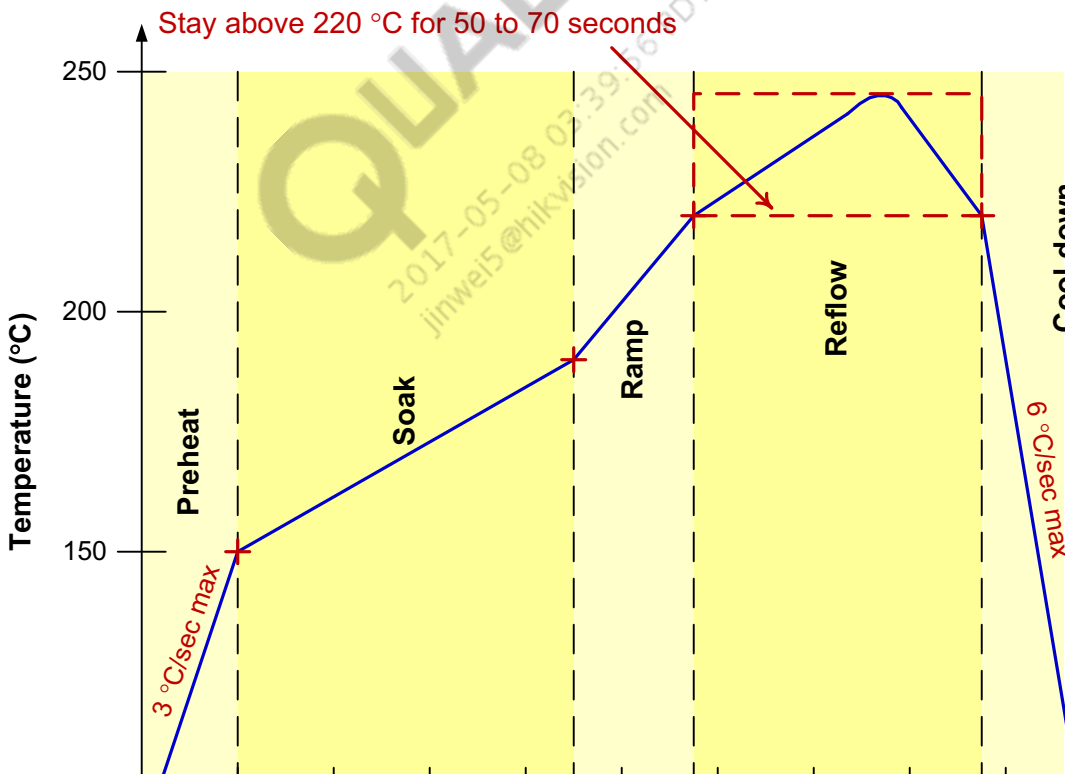


Figure 6-1 Typical SMT reflow profile

6.2.3 SMT peak package-body temperature

During a production board's reflow process, the temperature seen by the package must be controlled. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more). Although the solder-paste manufacturer's recommendations for optimum temperature and duration for solder reflow must be followed, the Qualcomm recommended limits must not be exceeded.

6.2.4 SMT process verification

Qualcomm recommends verification of the SMT process prior to high-volume board assembly, including:

- Electrical continuity
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume

6.3 Board-level reliability

Qualcomm conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

For board-level reliability data, refer to *Board-Level Reliability DRQFN/mQFN* (BR80-NT096-1).

7 Part Reliability

7.1 Reliability qualification summary

QFE1952 reliability evaluation report.

Table 7-1 Silicon Reliability Results

Tests, Standards and Conditions	Sample Size	Result
Average Failure Rate (AFR) in FIT (λ, Failure in billion device-hours) Dynamic HTOL: JESD22-A108-A	231	λ = 95 FIT, Pass Reachout ~ 10.5 yrs
Mean Time To Failure (MTTF) t = 1/λ (Million Hours)	231	10.5 yrs
ESD – Human-Body Model (HBM) Rating; JESD22-A114-B	6	±2 KV, all pins except #5. Pin #5 passed ±1.5 KV)
ESD – Charge Device Model (CDM) Rating; JESD22-C101-D	6	500 V, All Pins
Latch-up (I-test): EIA/JESD 78 Trigger current: ±100 ma; Temperature: 85°C	NA	
Latch-Up (V-supply Overvoltage): EIA/JESD78 Trigger voltage: 1.5 × Vdd; Temperature: 85°C	NA	

Table 7-2 Package Reliability Results

Tests, Standards and Conditions	Sample Size	Result
Moisture Resistance Test (MRT): MSL3; J-STD-020 3 × Reflow Cycles @ 255C +5/-0 °C 100% CSAM Delamination Inspection	960	Pass
Temperature Cycle: JESD22-A104 Temperature: -55C to +125C; Number of cycles: 1000 Soak time at min/max temperature: 20 minutes Cycle rate: 2 cycles per hour (cph) **Preconditioning: MSL3;** JESD22-A113 Reflow temperature: 255C +5/-0 °C	480	Pass
Unbiased Highly Accelerated Stress Test (UHAST) JESD22-A118 **Preconditioning: MSL3;** JESD22-A113 Reflow temperature: 255C +5/-0 °C	480	Pass
High Temperature Storage Life (HTS): JESD22-A103 Temperature = 150 °C, 1000 hours	480	Pass
Physical Dimensions: JESD22-B100-A Case Outline Drawing: BL90-Y6949/ BL90-Y6950	15	Pass
Die shear MIL-STD-883E, Method 2019	15	Pass

7.2 Qualification sample description

Table 7-3 QFE1952 characteristics

Device name	QFE1952
Package type	26MQFN
Package body size	3.5 mm × 3.9 mm × 0.627 mm
Pin count	26
Pin composition	Matte tin
Process	.18 µm
Pin pitch	0.40 mm