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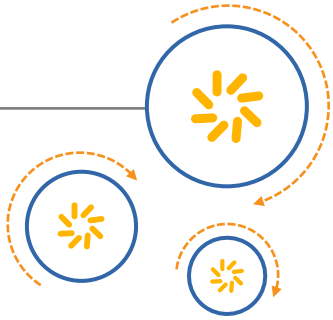

QCA99XX Board Data File Structure

Application Note

80-Y8050-6 Rev. G

January 22, 2016

For additional information or to submit technical questions go to https://createpoint.qti.qualcomm.com/

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Revision history

Revision	Date	Description
A	September 2014	Initial release
B	November 2014	Table 2-1 BDF layout ▫ Change section “5G power calibration data and target power/CTL table” to “5G power calibration data and target power table”. ▫ Add “Rx calibration” and “5G power CTL table” sections. ▫ Change “TOTAL SIZE” to 13280. ▫ Add 2.8.1 2 GHz target power. ▫ Add 2.6.2 “2” GHz CTL power. Change Table 2-10 ▫ Add “targetPower2G SU12,VHT20, G”, “targetPower2G SU34, MU, VHT20, G”, “ctlIndex2G_11b”, ‘ctlFreqbin2G _11b”, “ctlData2G_11b”, “ctlIndex2G_ HT20/VHT20”, “ctlFreqbin2G_ HT20/VHT20”, “ctlData2G_ HT20/VHT20”, “ctlIndex2G_ HT40/VHT40”, “ctlFreqbin2G_ HT40/VHT40”, and “ctlData2G_ HT40/VHT40” fields. Change 2.9 heading title to 5 GHz calibration. ▫ Add 2.7.1 “5” GHz target power. ▫ Add 2.7.2 “5” GHz CTL power. Change Table 2-12 ▫ Add “targetPower5G SU12,VHT20, G”, “targetPower5G SU34, MU, VHT20, G”, “Sticky write to set register”, “Rx Gain Cal”, “ctl5GFuture1”, “ctlIndex5G_11a”, “ctlFreqbin5G _11a”, “Padding”, “ctlData5G_11a”, “ctlIndex5G_ HT20/VHT20”, “ctlFreqbin5G_ HT20/VHT20”, “ctlData5G_ HT20/VHT20”, “ctlIndex5G_ HT40/VHT40”, “ctlFreqbin5G_ HT40/VHT40”, “ctlData5G_ HT40/VHT40”, “ctlIndex5G_VHT80”, “ctlFreqbin5G_VHT80”, “ctlData5G_VHT80”, and “@G CTL spare” fields. Update sections: ▫ Add 2.10.1 Rx Gain Cal 5G 96 Bytes. ▫ Add 0 ▫ ▫ Rx Gain Cal 2G 96 Bytes.
C	December 2014	Added Section B, Related Documentation
D	February 2015	Add smartAn tennaEnabl e field in Table 2-2. Update 2.8.1 2 GHz target power and 2.9.1 5 GHz target power.
E	November 2015	Updated for 160 MHz and latest fields available in board data file; changes throughout document
F	December 2015	Added description of new fields paprdShortCal, and nonLinearTxFir and new flag WHAL_FLAG3_OVERRIDE_SWTBLCOM
G	January 2015	▪ EEPROM is now referred to as the board data file (BDF) ▪ Added 160 and 80p80 CTL fields ▪ GLUT Offset Table Updates

Applicable Chips

Chip Number
QCA9980, QCA9981, QCA9990, QCA9982, QCA9983, and QCA9992
QCA9984 and QCA9994

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1 Overview

The board data file (BDF) structure identifies all the BDF fields and their values. Some fields' values cannot be changed or are reserved for future use.

2 QCA99XX BDF Layout

Table 2-1 BDF layout

Section	Size
Base BDF header	200
Bimodal BDF header (2 GHz/5 GHz)	528
Frequency modal BDF header	148
Spur mitigation	136
2 GHz power calibration data and target power/CTL table	3234
5 GHz power calibration data and target power table	6882
Sticky write table	508
Rx calibration	192
5 GHz power CTL table	1024
Chip calibration data	36
ATE data	144
TOTAL SIZE	**13280**

2.1 Base BDF header

Table 2-2 Base header

Field Name	Bytes	Description	Bit Num	Bit Definition
length	2	Overall BDF file size based on the .bin file selected	[16:0]	Value
checksum	2	BDF file checksum	[16:0]	Value
eeprom version	1	Version control	[7:0]	Value
template version	1	Template version control (some boards have special template define field)	[7:0]	Value
macAddr	6	WLAN MAC Address	[47:0]	WLAN MAC Address
regDmn	4	Determines regulatory domain, country code	[31:16]	Reserved
			[15]	COUNTRY_OR_DOMAIN_FLAG
			[14]	WORLD_WIDE_ROAMING_FLAG
			[11:0]	COUNTRY_OR_DOMAIN_CODE
opCapBrdFlags	16	Determines device operation mode (detail in BDF FLAGS page)	[95:0]	Refer to BDF flags
binBuildNumber	4	Includes 4 fields:	[31:24]	boardDataRev
			[23:16]	projectId
			[15:8]	customerId
			[7:0]	refDesignId

txrxMask	1	Tx and Rx Mask bit to identify MIMO configuration	[7:4]	Rx Mask	
				0x1	RF Chain 0
				0x2	RF Chain 1
				0x3	RF Chain 0 && 1
			[3:0]	Tx Mask	
				0x1	RF Chain 0
				0x2	RF Chain 1
				0x3	RF Chain 0 && 1
rfSilent	1	Reserved for RFSilent pin config	[7:0]	Reserved	
wlanLedGpio	1	Reserved for LED pin config	[7:0]	Reserved	
swreg	1	Reserved for control internal switching regulator register	[7:0]	Reserved	
deltaCck	1	Compensate all CCK rates for any delta from calibration	[7:0]	Signed compensation value in 1/8th dB steps - Positive values specify the amount removed, negative values the amount to be added	
delta20	1	Compensate all 20 MHz rates for any delta from calibration (e.g. between 1-chain calibration and 4-chain op)	[7:0]	Signed compensation value in 1/8th dB steps - Positive values specify the amount removed, negative values the amount to be added	
delta40	1	Compensate all 40 MHz rates for any delta from calibration	[7:0]	Signed compensation value in 1/8th dB steps - Positive values specify the amount removed, negative values the amount to be added	
delta80	1	Compensate all 80 MHz rates for any delta from calibration	[7:0]	Signed compensation value in 1/8th dB steps - Positive values specify the amount removed, negative values the amount to be added	
custData	20	Space for customer to write info	[159:0]	N/A	
param_for_tuning_caps	1	Value of XTAL_CAPOUTDAC	[7:0]	Value of XTAL_CAPOUTDAC	
param_for_tuning_caps_1	1	Value of XTAL_CAPINDAC	[7:0]	Value of XTAL_CAPINDAC	
tpc_flag	1	Reserved for future use		Reserved	
dpdRfbMode	1	DPD GLUT selection index	[7:0]	Number of GLUTs used in a current reference design (3 or 4 depending upon the ref design)	
				0x1	Enable 3 GLUT
				0x4	Enable 4 GLUT
dpdTrainingSample	2	Reserved for DPD configuration	[15:0]	N/A	
dpdHeavyClipEnable	2	Reserved for DPD configuration	[15:0]	N/A	
dpdQuickDrop	1	Reserved for DPD configuration	[7:0]	N/A	
dpdTargetLvlHi	1	Reserved for DPD configuration	[7:0]	N/A	
dpdTargetLvlLow	1	Reserved for DPD configuration	[7:0]	N/A	
dpdTargetLvlWeak	1	Reserved for DPD configuration	[7:0]	N/A	
dpdPwrHi	1	Reserved for DPD configuration	[7:0]	N/A	
dpdPwrLow	1	Reserved for DPD configuration	[7:0]	N/A	
dpdEnable	1	Enable DPD	[7:0]	1	Enable
				0	Disable
dpdSqLimit	1	Maximum DPD training quality limit	[7:0]	Limit set at 60	
dpdSqBestLimit	1	Best DPD training quality limit	[7:0]	Best training quality set at 20	
dpdCorexRange	1	DPD timing search window	[7:0]	Current algorithm search window fixed at 6	

dpdForceClock_TxRadioBW	1	Reserved for DPD configuration	[7:0]	N/A	
dpdAm2PmMask	4	DPD enable mask for MCS9 ~ MCS0 for Nss=1/2/3(4)	[31:0]	1	Enable
				0	Disable
dpdHt40Mask	4	DPD enable mask HT40 for MCS9 ~ MCS0 for Nss=1/2/3(4)	[31:0]	1	Enable
				0	Disable
dpdTrainingBW	1	DPD training bandwidth	[7:0]	7	50 MHz+RC47.5
				6	50 MHz+RC25
				5	120 MHz+RC25 (20 MHz)
				4	120 MHz+RC47.5, (40 MHz)
				3	140 MHz, (80 MHz)
				2	12.5 MHz+RC25
				1	120 MHz
				0	50 MHz
dpdAgc2Settling	1	Reserved for DPD configuration	[7:0]	N/A	
dpdXpaOn	1	Turn on all external PAs during DPD Calibration	[7:0]	1	Enable
				0	Disable
xtal_temp_comp	40	XTAL calibration temperature compensation	[319:0]	Repeated over 10 temperature sets	
				deltaCapin (between room and each temp)	
				deltaCapout (btw. room and each temp)	
				Temperature for each capin/capout delta	
baseFuture1	12	Reserved for future use	[95:0]	Reserved	
clpc_error	2	Reserved for future use	[15:0]	Reserved	
clpcFlag	1	Reserved for CLPC debug	[7:0]	Reserved	
tempSlopeCharacterized	1	Populated from on chip values	[7:0]	Do not set	
xtal_cap_interval	4	Crystal capacitor parameter	[31:0]		
xtal_cap_offset	4	Crystal capacitor parameter	[31:0]		
pefFlag	1	Reserved for future use	[7:0]	Reserved	
pefCalMax	1	Reserved for future use	[7:0]	Reserved	
pefCalMin	1	Reserved for future use	[7:0]	Reserved	
pefCalStep	1	Reserved for future use	[7:0]	Reserved	
pefMaxCalAtt	1	Reserved for future use	[7:0]	Reserved	
pefMaxCalBw	1	Reserved for future use	[7:0]	Reserved	
pefMagSel	1	Reserved for future use	[7:0]	Reserved	
pefLbSel	1	Reserved for future use	[7:0]	Reserved	
checkTrainingStatusDelay	2	Training sequence delay status	[15:0]		
dpdLNASETTING	4	Reserved for DPD LNA setting	[31:0]	N/A	
nvMacFlag	1	NV MAC flag	[7:0]	Set if MAC address or CAL info saved to NVM	
mipiPowerMode	1	MIPI interface power mode	[7:0]	1	Medium power mode
				0	High power mode
				Other values reserved	
pefMask	4	Reserved for future use	[31:0]	Reserved	
sensitivityAdjustment	1	Set a new sensitivity level	[7:0]	Sensitivity value in range -10 to NF (~-90)	
smartAntennaEnable	1	Enable smart antenna	[7:0]		
ccaThresh	1	Set CCA threshold	[7:0]	CCA value in range -10 to NF (~-90)	
packageType	1	Chip package type	[7:0]	1	BGA
				0	QFN

paBiasSetting	4	Bias setting for PA	[31:0]	Four CUS238/CUS240 specific values set by Qualcomm Atheros
refDesignIdForFilename	1	One new BDF file additions use this ID to match ID in filename	[7:0]	Enter ID in the BDF files in hexadecimal, filename ID should be decimal
paprdShortCal	1	Enable PA Pre-distortion Short calibration	[7:0]	Set to 1 to enable PA pre-distortion short calibration
nonLinearTxFir	1	Enable TxFir for improved Tx mask performance	[7:0]	Set to 1 to enable TxFir. Aids Tx mask perf and must be set in conjunction with updated heavy clip parameters.
ThermOffset	1	Reserved for future use	[7:0]	Reserved
baseFuture	24	Reserved for future use	[199:0]	Reserved

2.2 BDF flags

Table 2-3 BDF flags

Field Name	Bytes	Description	Bit Num	Bit Definition	
opFlags	1	Determines the operation mode of the device	[7:0]	Enable flags for the following modes:	
				WHAL_OPFLAGS_11A	= 0x01
				WHAL_OPFLAGS_11G	= 0x02
				WHAL_OPFLAGS_5G_HT40	= 0x04
				WHAL_OPFLAGS_2G_HT40	= 0x08
				WHAL_OPFLAGS_5G_HT20	= 0x10
				WHAL_OPFLAGS_2G_HT20	= 0x20
featureEnable	1	Some features enable/disable	[7:0]	tempComp	= 0x01
				Enable temperature compensation table for power	
				voltComp	= 0x02
				Enable voltage compensate table for power	
				Reserved	= 0x04
				Reserved	= 0x08
				Reserved	= 0x10
				override_heavy_clip	= 0x20
				Use common heavy clip values for all bandwidths (see section 2.6)	
				tuning_caps	= 0x40
				Use longshift to update CAPINDAC/CAPOUTDAC	
				override_heavy_clip_perbw	= 0x80
				Use per bandwidth heavy clip values (see section 2.6)	
miscConfiguration	1	Taken from previous chipsets, reserved for future cfg setting flag	[7:0]	Reserved	
flag1	1	Some flags for set change to setting analog register	[7:0]	Reserved	
boardFlags	4	Boards flags to enable/disable features	[31:0]	Reserved for future use	
				WHAL_BOARD_SELLNA	= 0x001
				WHAL_BOARD_ZERO_DBM	= 0x002
				WHAL_BOARD_USE_OTP_XTALCAPS	= 0x040

Field Name	Bytes	Description	Bit Num	Bit Definition	
				WHAL_BOARD_TXGAIN_TBL	= 0x008
				WHAL_BOARD_ANTDIVERSITY	= 0x010
				WHAL_BOARD_TEMP_SENSOR	= 0x020
				WHAL_BOARD_SHARED_RX	= 0x080
				WHAL_BOARD_BT_SIGNAL_PRESENT	= 0x100
				WHAL_BOARD_USE_XPA	= 0x200
				WHAL_BOARD_PMU_BYPASS_SW	= 0x400
				WHAL_BOARD_PMU_BYPASS_PA	= 0x800
				WHAL_BOARD_PAPRD_2G_DISABLE	= 0x2000
				WHAL_BOARD_PAPRD_5G_DISABLE	= 0x4000
				WHAL_BOARD_0CAL_ENABLED	= 0x8000
				WHAL_BOARD_TXGAINTBL_EEP_ENA	= 0x10000
				WHAL_BOARD_TXGAINTBL_SCHEME	= 0x20000
				WHAL_BOARD_ENABLE_XPA_BIAS_2G	= 0x40000
				WHAL_BOARD_ENABLE_XPA_BIAS_5G	= 0x80000
opFlags2	1	Extend part of opFlags	[7:0]	Enable flags for the following modes:	
				WHAL_OPFLAGS2_5G_VHT20	= 0x01
				WHAL_OPFLAGS2_2G_VHT20	= 0x02
				WHAL_OPFLAGS2_5G_VHT40	= 0x04
				WHAL_OPFLAGS2_2G_VHT40	= 0x08
				WHAL_OPFLAGS2_5G_VHT80	= 0x10
				WHAL_OPFLAGS2_5G_VHT160	= 0x20
				WHAL_OPFLAGS2_5G_VHT80P80	= 0x40
flag2	1	Additional feature guidance flags – typically used to keep backward compatibility with previous board data files when new fields are added	[7:0]	WHAL_FLAG2_CTLS_VALID = 0x01	
				Set when the CTL portion of BDF has been properly populated	
				WHAL_FLAG2_ALT_TGT_PWR_LAYOUT	= 0x02
				Always set to 1 in current BDF	
				WHAL_FLAG2_MINCCA_THR_FROM_MODAL	= 0x04
				Set to apply min CCA from modal section of BDF file (minCCAPwrThresh)	
				WHAL_FLAG2_MINCCA_THR_FROM_RXGAIN	= 0x08
				Set to apply min CCA from receive gain calibration	
				WHAL_FLAG2_IBF_CAL	= 0x10
				Set to use Implicit beam forming	
				WHAL_FLAG2_TPC_CAL_TGT_PWR_GUIDE	= 0x20
				Set when TPC power guidance has been supplied (calDataTgtPwr) in BDF – this guidance is given to test equipment during TPC	
				WHAL_FLAG2_OVERRIDE_PAPRD_BW	= 0x40
				Use dpdTrainingBW field for PAPRD training bandwidth	
				WHAL_FLAG2_XTAL_TEMP_COMP_ENABLE	= 0x80
				Set when the XTAL temp compensation table has been supplied in BDF in the xtal_temp_comp section	
flag3	1		[7:0]	WHAL_FLAG3_PA_BIAS_OVERRIDE	= 0x01
				Set when the PA Bias current (paBiasSetting) is set via the BDF	
				WHAL_FLAG3_ENABLE_160_TARGET_PWR	= 0x02

Field Name	Bytes	Description	Bit Num	Bit Definition
				Set when the 160 MHz target powers have been populated in the bdf file. If not set, 80MHz target powers will be used
				WHAL_FLAG3_OVERRIDE_SWTBLCOM = 0x20
				When set, the parameters of antCtrlCommon and antCtrlCommon2 are used from the BDF; otherwise value from software will be used
				WHAL_FLAG3_160_CTL_valid = 0x40
				Set when the CTL sections for 160 and 80p80 sections are populated; otherwise if clear, the 80 MHz CTL is applied for 160 and 80plus80 modes
secGlutCalFlag	1	Flag for GLUT calibration of secondary 80MHz channel	[7:0]	Set to 0x1 when secondary channel GLUT has been calibrated or when the secondChannelGLUTOffset N/Atable is valid
boardFlagsExt	4	Reserved for coex and other future flags	[31:0]	N/A

2.3 Bimodal BDF header

Table 2-4 Modal section

Field Name	Bytes	Description	Bit Num	Bit Definition
voltSlope	4	Reserved	[31:0]	Reserved
biModal_resv1	2	Adding for byte alignment	[15:0]	N/A
xpaBiasLvl	1	Reserved for external PA bias level voltage level	[7:0]	Value
antennaGainCh	1	Reserved for ANT gain calculation	[7:0]	Value
antCtrlCommon	4	Sets switch_table during Tx states; see BB_SWITCH_TABLE_COM1 (Section A.1)	[31:0]	Value. Note that WHAL_FLAG3_OVERRIDE_SWTBLCOM needs to be set for this value to apply from board data file
antCtrlCommon2	4	Sets ANT switch_table in Rx states; see BB_SWITCH_TABLE_COM2 (Section A.2)	[31:0]	Value. Note that WHAL_FLAG3_OVERRIDE_SWTBLCOM needs to be set for this value to apply from board data file
antCtrlChain	8	Sets XLNA control lines in any state; see BB_SWITCH_TABLE_CHN_B0 (Section A.3)	[15:0]	Value of chain 1, 2, 3
			[15:0]	Value of chain 0
fem_xpa_set	1	FEM control xpa set enable_xpab/xpaa[3:2] xpab/xpaa_active_high[1:0]	[7:0]	Value
rxFilterCap	1	Adjust Rx filter bandwidth	[7:0]	Value
rxGainCap	1	Limit max RF gain (in Rx gain table)	[7:0]	Value
txrxgain	1	Tx and Rx gain table index SW fills the INI tables to use based on Tx and Rx gain index (in code arxxx_ini.c)	[7:4]	Tx gain table index index 0 for xpa, indx1 for ipa
			[3:0]	Rx gain table index index 0 for xpa, indx1 for ipa
dpdCtrl	2	Reserved for DPD configuration	[15:0]	N/A

Field Name	Bytes	Description	Bit Num	Bit Definition	
dpdTxFirCoeffSel	1	Reserved for DPD configuration	[7:0]	N/A	
dpdInitRxBbGain	1	Reserved for DPD configuration	[7:0]	N/A	
dpdVht80Mask	4	DPD enable mask HT40 for MCS9 ~ MCS0 for Nss=1/2/3(4)	[31:0]	Bit [1]	Enable
				Bit [0]	Disable
dpdInitRxBbGainLow	1	Reserved for DPD configuration	[7:0]	N/A	
dpdInitRxBbGainHi	1	Reserved for DPD configuration	[7:0]	N/A	
dpdMaxIndexRef	1	Reserved for DPD configuration	[7:0]	N/A	
dpdTrainPwrInc_t7	1	Reserved for DPD configuration	[7:0]	N/A	
dpdNoiseRatio	1	configuration for no of noise bins	[7:0]	Ranging from 25 to 30	
dpdStartCoarseIdx	1	DPD loopback timing index, considering all 4 chains	[7:0]	Ranging from 10 to 23	
unUsed	2	Reserved for future use	[7:0]	Reserved	
dpdTxFirCoeffMem	1	Reserved for DPD configuration	[7:0]	N/A	
clpcAttenTargetPwrChain0	1	Reserved for future use	[7:0]	Reserved	
clpcAttenTargetPwrChain1	1	Reserved for future use	[7:0]	Reserved	
clpcPdetTiaGain	1	Reserved for future use	[7:0]	Reserved	
clpcSensitivePdadc	1	Reserved for future use	[7:0]	Reserved	
thermal_interval	1	Reserved for future use	[7:0]	Reserved	
thermal_interval_lowTemp	1	Reserved for future use	[7:0]	Reserved	
calPowerOffset	1	Reserved for future use	[7:0]	Reserved	
clpcLpfHighLowTiaHighGain	1	Reserved for future use	[7:0]	Reserved	
clpcSqGain	1	Reserved for future use	[7:0]	Reserved	
dpdTargetPwrMax	1	Maximum DPD operational range	[7:0]	Unit half dB step	
dpdTargetPwrMin	1	Minimum DPD operational range	[7:0]	Unit half dB step	
paprdAttenTable	20	DPD configurations	[159:0]		
minCCAPwrThresh	2	Minimum CCA threshold value; applied when WHAL_FLAG2_MINCCA_THR_FROM_MODAL is set	[15:0]		
TxIQCalMaxTxGain	1	Reserved for future use	[7:0]	Reserved	
minPwr4TPCErrCorr	1	It means if transmit power is lower than this value will disable CLPC error correction	[7:0]	Value in half dB step	
startChannel	1	Used to limit range of frequencies supported by hw – start frequency of range	[7:0]	2GHz: value + 2300 = channel frequency in MHz 5GHz: Value*5 + 4800 = channel frequency in MHz	
endChannel	1	Used to limit range of frequencies supported by hw – start frequency of range	[7:0]	2GHz: value + 2300 = channel frequency in MHz 5GHz: Value*5 + 4800 = channel frequency in MHz	
tempSlopeGLUTShift	1	Reserved for future use	[7:0]	Reserved	
futureBiModal	37	Reserved	[295:0]	Reserved	

2.4 Frequency modal BDF header

Table 2-5 Frequency modal BDF header

Field Name	Bytes	Description	Bit Num	Bit Definition
xatten1DB	16	2 chains Attenuation is in dB, provided by switch (first stage of attenuation). Detail in BB_ext_atten_switch_ctl_bx (See Section A.4)	[7:0]	value2G
			[7:0]	value5GLow freqs = 5180-5500
			[7:0]	value5GMid freqs = 5500-5785
			[7:0]	value5GHigh freqs = 5785-
			[7:0]	value2G
			[7:0]	value5GLow freqs = 5180-5500
			[7:0]	value5GMid freqs = 5500-5785
			[7:0]	value5GHigh freqs = 5785-
xatten1Margin	16	3 chains Margin is to maximum receiver gain in dB, before acting first stage of switch attenuation Detail in BB_ext_atten_switch_ctl_bx (See Section A.4)	[7:0]	value2G
			[7:0]	value5GLow freqs = 5180-5500
			[7:0]	value5GMid freqs = 5500-5785
			[7:0]	value5GHigh freqs = 5785-
			[7:0]	value2G
			[7:0]	value5GLow freqs = 5180-5500
			[7:0]	value5GMid freqs = 5500-5785
			[7:0]	value5GHigh freqs = 5785-
xatten1Hyst	16	3 chains Margin is to maximum receiver gain in dB, before acting first stage of switch attenuation Detail in BB_ext_atten_switch_ctl_bx (See Section A.4)	[7:0]	value2G
			[7:0]	value5GLow freqs = 5180-5500
			[7:0]	value5GMid freqs = 5500-5785
			[7:0]	value5GHigh freqs = 5785-
			[7:0]	value2G
			[7:0]	value5GLow freqs = 5180-5500
			[7:0]	value5GMid freqs = 5500-5785
			[7:0]	value5GHigh freqs = 5785-
xatten1HystHT40	16	3 chains Margin is to maximum receiver gain in dB, before acting first stage of switch attenuation Detail in BB_ext_atten_switch_ctl_bx (See Section A.4)	[7:0]	value2G
			[7:0]	value5GLow freqs = 5180-5500
			[7:0]	value5GMid freqs = 5500-5785
			[7:0]	value5GHigh freqs = 5785-
			[7:0]	value2G
			[7:0]	value5GLow freqs = 5180-5500
			[7:0]	value5GMid freqs = 5500-5785
			[7:0]	value5GHigh freqs = 5785-
xatten1HystHT80	16	3 chains Margin is to maximum receiver gain in dB, before acting first stage of switch attenuation Detail in BB_ext_atten_switch_ctl_bx (See Section A.4)	[7:0]	value2G
			[7:0]	value5GLow freqs = 5180-5500
			[7:0]	value5GMid freqs = 5500-5785
			[7:0]	value5GHigh freqs = 5785-
			[7:0]	value2G
			[7:0]	value5GLow freqs = 5180-5500
			[7:0]	value5GMid freqs = 5500-5785
			[7:0]	value5GHigh freqs = 5785-
xlnaGain	4	xlnaGain	[31:0]	xlnaGain for 4 chains
Reserved	64	Reserved	[511:0]	Reserved

2.5 Spur mitigation

Table 2-6 Spur mitigation

Field Name	Bytes	Description	Bit Num	Bit Definition	
spurRssiThresh	1	RSSI Threshold to enable spur	Decimal Value	The RSSI threshold to enable the spur mitigation. Spur mitigation is disabled above this RSSI threshold.	
spurRssiThreshCCK	1	RSSI Threshold to enable spur in CCK mode	Decimal Value	Value is in decimal as -94.	
spurMitFlag	1	Additional flag to control spur mitigation behavior	[7:1]	Reserved	
			[0]	0x01	Enable spur mitigation for noise floor calibration
				0x02	Spur mitigation mask override
				0x04	Set when populating the spurThreshold fields
spurMitFreqMax	1	Number of frequencies applying spur mitigation	[7:0]	Up to 8	
spurChans_CCK	6	Spur channels in usual fbin coding format: spurChan spurABChoose spurA_PrimSecChoose spurB_PrimSecChoose reserved[4]	[47:0]	Decimal + 2300 = Channel Frequency in MHz	
spurChans_2G	8	spur channels in usual fbin coding format: spurChan spurABChoose spurA_PrimSecChoose spurB_PrimSecChoose reserved[4]	[63:0]	Value + 2300 = Channel Frequency in MHz	
spurStr_2G	8	Spur strength of the corresponding 2GHz frequency	[63:0]	Spur strength	
spurChans_5G	64	spur channels in usual fbin coding format; spurChan spurABChoose spurA_PrimSecChoose spurB_PrimSecChoose reserved[4]	[511:0]	Value*5 + 4800 = Channel Frequency in MHz	
spurStr_5G	32	Spur strength of the corresponding 5 GHz frequency	[255:0]	Spur strength	
spur_config_reserve	3	Spur configurations	[23:0]	Spur configurations	
spurThreshold	5	Spur configurations	[39:0]	Used to override the following thresholds: SPUR_THRESHOLD_AGC SPUR_THRESHOLD_SELFCOR SPUR_THRESHOLD_DATA_TD SPUR_THRESHOLD_DATA_FD SPUR_THRESHOLD_CCK	
spurPuncMask	1	Spur configurations	[7:0]	Spur configurations	
spurPilotMask	1	Spur configurations	[7:0]	Spur configurations	
spurChanMask	1	Spur configurations	[7:0]	Spur configurations	

2.6 Heavy Clip Configuration

Table 2-7 Heavy clip configuration

Field Name	Bytes	Description	Bit Num	Bit Definition
heavyClipFactorQam	10	Per MCS heavy clip factor for 20MHz if override_heavy_clip_perbw is set or all bandwidths if override_heavy_clip is set	[79:0]	MCS0 -> byte 0 … MCS9 -> byte 9
heavyClipCompFactorQam	10	Corresponding compensation factor for 20 MHz or all bandwidths (as above)	[79:0]	MCS0 -> byte 0 … MCS9 -> byte 9
heavyClipFactorQamNonHtDup40	10	Per MCS heavy clip factor for 40 MHz non-HT duplicate	[79:0]	MCS0 -> byte 0 … MCS9 -> byte 9
heavyClipCompFactorQamNonHtDup40	10	Corresponding compensation factor for 40 MHz non-HT duplicate	[79:0]	MCS0 -> byte 0 … MCS9 -> byte 9
heavyClipFactorQamNonHtDup80	10	Per MCS heavy clip factor for 80MHz non-HT duplicate	[79:0]	MCS0 -> byte 0 … MCS9 -> byte 9
heavyClipCompFactorQamNonHtDup80	10	Corresponding compensation factor for 80 MHz non-HT duplicate	[79:0]	MCS0 -> byte 0 … MCS9 -> byte 9
heavyClipEnableBitMap	2	Enables which rates apply heavy clip; only these rates apply heavy clip regardless of how many rates have factor values supplied	[15:0]	MCS0 -> bit 0 … MCS9 -> bit 9
heavyClipUsePreEmp	1	Enable the Frequency-Domain pre-emphasis	[7:0]	
heavyClipBackoffPwr2x	1	Power back off for 3 and 4 stream SU target powers in ½-dB step size	[7:0]	
heavyClipFactorQam_40Mhz	10	Per MCS heavy clip factor for 40 MHz if override_heavy_clip_perbw is set	[79:0]	MCS0 -> byte 0 … MCS9 -> byte 9
heavyClipCompFactorQam_40Mhz	10	Corresponding compensation factor for 40 MHz	[79:0]	MCS0 -> byte 0 … MCS9 -> byte 9
heavyClipFactorQam_80Mhz	10	Per MCS heavy clip factor for 80 MHz if override_heavy_clip_perbw is set	[79:0]	MCS0 -> byte 0 … MCS9 -> byte 9
heavyClipCompFactorQam_80Mhz	10	Corresponding compensation factor for 80 MHz	[79:0]	MCS0 -> byte 0 … MCS9 -> byte 9
powerOffset_HT20	10	Per MCS power compensation deltas due to heavy clip for 20 MHz rates	[79:0]	MCS0 -> byte 0 … MCS9 -> byte 9 Signed value added to or subtracted from HW requested power
powerOffset_HT40	10	Per MCS power compensation deltas due to heavy clip for 40 MHz rates	[79:0]	MCS0 -> byte 0 … MCS9 -> byte 9 Signed value added to or subtracted from HW requested power
powerOffset_HT80	10	Per MCS power compensation deltas due to heavy clip for 80 MHz rates	[79:0]	MCS0 -> byte 0 … MCS9 -> byte 9 Signed value added to or subtracted from HW requested power

2.7 Secondary segment GLUT offset table

The secondary segment GLUT offset table is used in 160 MHz or 80 plus 80 MHz modes. The RF parameters are tuned for power accuracy at the primary 80 MHz segment. Table 2-8 specifies how much the Gain Look Up Table (GLUT) should be shifted for the secondary segment. The table below show an example of the gain shift based on primary and secondary segment's frequencies

Table 2-8 Secondary segment GLUT offset table

tx gain index bias	5210	5290	5530	5610	5690	5775
Primary freq@5210	0	0	2	3	4	4
Primary freq @5290	1	0	3	3	4	4
Primary freq @5530	6	4	0	0	0	0
Primary freq @5610	7	7	1	0	0	0
Primary freq @5690	7	7	1	2	0	0
Primary freq @5775	7	7	5	4	2	0

This is represented in the board data file with these fields (two tables, one for each of the two chains):

Chain	Field Name	Bytes	Description	Bit Num	Bit Definition
0	secondChannelGLUTOffset_0_A_0_0	6	Secondary channel GLUT offsets from primary frequency 5210	[47:0]	Offsets for secondary channels 5210, 5290, 5530, 5610, 5690 and 5775
	secondChannelGLUTOffset_1_A_0_0	6	Secondary channel GLUT offsets from primary frequency 5290	[47:0]	Offsets for secondary channels 5210, 5290, 5530, 5610, 5690 and 5775
	secondChannelGLUTOffset_2_A_0_0	6	Secondary channel GLUT offsets from primary frequency 5530	[47:0]	Offsets for secondary channels 5210, 5290, 5530, 5610, 5690 and 5775
	secondChannelGLUTOffset_3_A_0_0	6	Secondary channel GLUT offsets from primary frequency 5610	[47:0]	Offsets for secondary channels 5210, 5290, 5530, 5610, 5690 and 5775
	secondChannelGLUTOffset_4_A_0_0	6	Secondary channel GLUT offsets from primary frequency 5690	[47:0]	Offsets for secondary channels 5210, 5290, 5530, 5610, 5690 and 5775
	secondChannelGLUTOffset_5_A_0_0	6	Secondary channel GLUT offsets from primary frequency 5775	[47:0]	Offsets for secondary channels 5210, 5290, 5530, 5610, 5690 and 5775
1	secondChannelGLUTOffset_0_A_0_1	6	Secondary channel GLUT offsets from primary frequency 5210	[47:0]	Offsets for secondary channels 5210, 5290, 5530, 5610, 5690 and 5775
	secondChannelGLUTOffset_1_A_0_1	6	Secondary channel GLUT offsets from primary frequency 5290	[47:0]	Offsets for secondary channels 5210, 5290, 5530, 5610, 5690 and 5775
	secondChannelGLUTOffset_2_A_0_1	6	Secondary channel GLUT offsets from primary frequency 5530	[47:0]	Offsets for secondary channels 5210, 5290, 5530, 5610, 5690 and 5775
	secondChannelGLUTOffset_3_A_0_1	6	Secondary channel GLUT offsets from primary frequency 5610	[47:0]	Offsets for secondary channels 5210, 5290, 5530, 5610, 5690 and 5775
	secondChannelGLUTOffset_4_A_0_1	6	Secondary channel GLUT offsets from primary frequency 5690	[47:0]	Offsets for secondary channels 5210, 5290, 5530, 5610, 5690 and 5775
	secondChannelGLUTOffset_5_A_0_1	6	Secondary channel GLUT offsets from primary frequency 5775	[47:0]	Offsets for secondary channels 5210, 5290, 5530, 5610, 5690 and 5775

2.8 2.4 GHz calibration

- 14 piers in board data
- Only 3 piers in OTP
- OLPC
  49*14 Piers = 686 Bytes (Can be optimized if increments and not absolute values are stored)
- CLPC
  40*14 Piers = 560 Bytes (Can be optimized if increments and not absolute values are stored)

2.8.1 2 GHz target power

NSS	Number of spatial streams
SU	Target powers for SU all NSS
MU	Target powers for MU all NSS
VHT20	Legacy/HT20/VHT20
VHT40	HT40/VHT40
VHT80	VHT80
VHT160	VHT160
G_0_0	<Band (G/A)> _<Chain>_<freq index>

tgtPow2xNss_SU_VHT<20/40/80>_<G/A>_0_0 44 44 44 44 42 42 40 38 30 30
tgtPow2xNss_MU_VHT<20/40/80>_<G/A>_0_0 44 44 44 44 42 42 40 38 30 30

The target powers are stored in the board data file in steps of 0.5 dB; the values from l-r are:

Table 2-9 2-GHz target powers in the board data file

Location	0	1	2	3	4	5	6	7	8	9
Legacy	6/9	12	18	24	36	48	54	NA	NA	NA
HT	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	NA	NA
VHT	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8	MCS9
e.g.	22 dBm	22 dBm	22 dBm	22 dBm	21 dBm	21 dBm	22 dBm	19 dbm	15 dBm	15 dBm

A power backoff field heavyClipBackoffPwr can back off power for SU NSS 3 and 4 for MCS0-3 by the value in heavyClipBackoffPwr2x (in steps of 0.5 dB), as shown:

MCS	SU_12	MU	SU_34
0	From BDF	From BDF	SU_12 – heavyClipBackoffPwr2x
1	From BDF	From BDF	SU_12 – heavyClipBackoffPwr2x
2	From BDF	From BDF	SU_12 – heavyClipBackoffPwr2x
3	From BDF	From BDF	SU_12 – heavyClipBackoffPwr2x
4	From BDF	From BDF	SU_12
5	From BDF	From BDF	SU_12
6	From BDF	From BDF	SU_12
7	From BDF	From BDF	SU_12
8	From BDF	From BDF	SU_12
9	From BDF	From BDF	SU_12

2.8.2 2 GHz CTL power

The general structure of each of the areas is the same, and consists of these components:

CTL Index	Describes the regulatory body, mode, number of chains, number of streams and beamforming status of each CTL being stored
Frequency list	Describes the frequencies to apply to the CTL
Power values	One power for each frequency and mode stored. Also there is an in-band flag to indicate whether power should apply for the current channel or all channels until the next frequency

Table 2-10 2.4 GHz calibration, target, and CTL power

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/ Field Description	Bit Num	Bit Definition
calFreqPier2G	calFreqPier2G	16	2 GHz channels that are calibrated; e.g: Decimal + 2300Hz = Channel Frequency	[127:0]	1 byte per channel (Max 16 channel)
	calFreqPier2G _ext	16	Extend for channel calibrated flag	[127:0]	
calPierData2G (OLPC/CLPC) = calibration data stored per point per channel per RF chain. (NumOfChain*10B(calPerPoint) + 4B(dacGain)+ 5B(therm/vol)) * NumOfChannels (4*10+9)*14= 686 Bytes	calPerPoint (per chain)	1	txgainIdx cal point 1	[7:3]	value of cal gain index
			pasetting cal point 1	[2:0]	value of cal pasetting
		1	meas_pwr cal point 1	[7:0]	value of measured power
		1	txgainIdx cal point 2	[7:3]	value of cal gain index
			pasetting cal point 2	[2:0]	value of cal pasetting
		1	meas_pwr cal point 2	[7:0]	value of measured power
		1	txgainIdx cal point 3	[7:3]	value of cal gain index
			pasetting cal point 3	[2:0]	value of cal pasetting
		1	meas_pwr cal point 3	[7:0]	value of measured power
		1	txgainIdx cal point 4	[7:3]	value of cal gain index
			pasetting cal point 4	[2:0]	value of cal pasetting
		1	meas_pwr cal point 4	[7:0]	value of measured power
		1	txgainIdx cal point 5	[7:3]	value of cal gain index
			pasetting cal point 5	[2:0]	value of cal pasetting
		1	meas_pwr cal point 5	[7:0]	value of measured power
	dacGain (per chain)	1	dacGain of glut gain setting	[7:0]	Value
	thermCalVal (per chain)	1	therm_cal_value not per chain	[7:0]	Value
	voltCalVal	1	volt_cal_value not per chain	[7:0]	Value
pad0	pad0	63	Pad0		
calData2G_PLUT_Future	calData2G_PLUT_Future	44	N/A	[351:0]	N/A
pad1	pad1	5	N/A	[39:0]	N/A
powerOffset2G	powerOffset2G	128	Used for power offset for CCK/OFDM 20/40/80 16 channels; 4chains	[1023:0]	Reserved
calPierData2G_CLPC (5points*2B*4Chains)*14 Piers = 560 Bytes	pdadc_read	1	Pdadc value for each CAL point	[7:0]	Pdadc value for each CAL point
	meas_pwr	1	Measured power value for each CAL point	[7:0]	Measured power value for each CAL point

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/ Field Description	Bit Num	Bit Definition
calData2GFuture	calData2GFuture	560	N/A	[4479:0]	N/A
alutFuture2G	alutFuture2G	92	N/A	[735:0]	N/A
extTPow2xDelta2G	extTPow2xDelta2G	24	Extend target power delta from 4bit to 5bit. Here is the all rates 5th bit.	[192:0]	5th bits of target power delta
Target powers for channels	calTargetFreqbinCck	2	802.11b Target powers for the following channels Ex: Decimal + 2300Hz = Channel Frequency	[15:0]	1 byte per channel (Max 2 channel)
	calTargetFreqbin2G	3	802.11g Target powers for the following channels Ex: Decimal + 2300Hz = Channel Frequency	[23:0]	1 byte per channel (Max 3 channel)
	pad11	3	Reserved space for byte alignment	[23:0]	Reserved
	targetFreqbin2GVHT20	4	HT20/VHT20 Target powers for the following channels Ex: Decimal + 2300Hz = Channel Frequency	[31:0]	1 byte per channel (Max 4 channel)
	targetFreqbin2GVHT40	4	HT40/VHT40 Target powers for the following channels Ex: Decimal + 2300Hz = Channel Frequency	[31:0]	1 byte per channel (Max 4 channel)
pad2	pad2	4		[31:0]	
Target power for DSSS && HR/DSSS rates. 4 bytes per channel * 2 channels = 8 Bytes	targetPowerCck	4	Target powers for 802.11b rates Ex: Decimal/2 = Power level [dBm]	[31:24]	11(S) Mbps
				[23:16]	11(L) Mbps
				[15:8]	5.5(S) Mbps
				[7:0]	1 Mbps -5.5(L) Mbps
Target power for 2GHz VHT 11AC, 11n, Legacy, 2xNSS SU12	targetPower2G SU12,VHT20, G	10	Target powers for SU12_VHT20_G Ex: Decimal/2 = Power level [dBm]	[79:72]	MSC9/NA/NA
				[71:64]	MSC8/NA/NA
				[63:56]	MSC7/MCS7/NA
				[55:48]	MSC6/MCS6/54
				[47:40]	MSC5/MCS5/48
				[39:32]	MSC4/MCS4/36
				[31:24]	MSC3/MCS3/24
				[23:16]	MSC2/MCS2/18
				[15:8]	MSC1/MCS1/12
				[7:0]	MSC0/MCS0/6 or 9
Target power for 2GHz VHT 11AC, 11n, Legacy, 2xNSS SU34 MU	targetPower2G SU34, MU, VHT20, G		Target powers for SU34_MU__VHT20_G Ex: Decimal/2 = Power level [dBm]	[79:72]	MSC9/NA/NA
				[71:64]	MSC8/NA/NA
				[63:56]	MSC7/MCS7/NA
				[55:48]	MSC6/MCS6/54
				[47:40]	MSC5/MCS5/48
				[39:32]	MSC4/MCS4/36
				[31:24]	MSC3/MCS3/24
				[23:16]	MSC2/MCS2/18
				[15:8]	MSC1/MCS1/12
				[7:0]	MSC0/MCS0/6 or 9

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/ Field Description	Bit Num	Bit Definition
[2G CTL 11b Index	ctlIndex2G_11b	12	6 indexes, each index 2 bytes 2 modes, 3 regulatory domains	[15:12]	SS mask
				[11:8]	Chain mask stream
				[7:4]	REG DOMN
				[3]	BF
				[2:0]	MODE
2G CTL 11b Frequency bin	ctlFreqbin2G_11b	27	(Frequency_in_MHz – 2300) 9 Channels 3 domains FCC, MKK, ETSI	[3:0]	Freq
Padding		1			
2G CTL 11b data Bin	ctlData2G_11b	54	1 pwr val for frequency and mode 2 modes, 9 channels, 3 reg dmn	[3:0]	dbm
2G CTL HT20/VHT20 index	ctlIndex2G_HT20/VHT20	60	30 indexes, each index 2 bytes 10 modes, 3 regulatory domains	[15:12]	SS mask
				[11:8]	chain mask stream
				[7:4]	REG DOMN
				[3]	BF
				[2:0]	MODE
2G CTL HT20/VHT20 Frequency Bin	ctlFreqbin2G_HT20/VHT20	33	(Frequency_in_MHz – 2300) 11 Channels 3 domains FCC, MKK, ETSI	[3:0]	Freq
Padding		1			
2G CTL HT20/VHT20 data Bin	ctlData2G_HT20/VHT20	330	1 pwr val for frequency and mode 10 modes, 11 channels, 3 reg dmn	[3:0]	dbm
2G CTL HT40/VHT40 index	ctlIndex2G_HT40/VHT40	36	18 indexes, each index 2 bytes 6 modes, 3 regulatory domains 3 domains FCC, MKK, ETSI	[15:12]	SS mask
				[11:8]	chain mask stream
				[7:4]	REG DOMN
				[3]	BF
				[2:0]	MODE
2G CTL HT40/VHT40 Frequency Bin	ctlFreqbin2G_HT40/VHT40	18	(Frequency_in_MHz – 2300) 6 Channels 3 domains FCC, MKK, ETSI	[3:0]	Freq
2G CTL HT40/VHT40 data bin	ctlData2G_HT40/VHT40	108	1 pwr val for frequency and mode 6 modes, 6 channels, 3 reg dmn	[3:0]	dbm
@G CTL spare		4			
Alpha thermal channel 4 bytes per chain * 4 RF chains = 16 Bytes	tempCompChans2G	4	Alpha thermal channel index Ex: Decimal + 2300Hz = Channel frequency	[31:0]	1 byte per channel (Max 4 channel)
Alpha thermal table 4 bytes per chain * 4 channels * 4 RF chains = 32 Bytes	tempComp2G	4	Alpha thermal table	[31:24]	85
				[23:16]	45
				[15:8]	-10
				[7:0]	-40

2.9 5 GHz calibration

- 32 piers in board data
- Only 8 piers in OTP
- OLPC
  49*32 Piers = 1568 Bytes (Can be optimized if increments and not absolute values are stored)
- CLPC
  5points*2B*4Chains*32 Piers = 1280 Bytes (Can be optimized if increments and not absolute values are stored)

2.9.1 5 GHz target power

NSS	Number of spatial streams
SU	Target powers for SU all NSS
MU	Target powers for MU all NSS
VHT20	Legacy/HT20/VHT20
VHT40	HT40/VHT40
VHT80	VHT80
VHT160	VHT160
G_0_0	<Band (G/A)> _<Chain>_<freq index>

tgtPow2xNss_SU_VHT<20/40/80>_<G/A>_0_0 44 44 44 44 42 42 40 38 30 30
tgtPow2xNss_MU_VHT<20/40/80>_<G/A>_0_0 44 44 44 44 42 42 40 38 30 30

The target powers are stored in the board data file in steps of 0.5 dB; the values from l-r are:

Table 2-11 5-GHz target powers in the board data file

Location	0	1	2	3	4	5	6	7	8	9
Legacy	6/9	12	18	24	36	48	54	NA	NA	NA
HT	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	NA	NA
VHT	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7	MCS8	MCS9
e.g	22 dBm	22 dBm	22 dBm	22 dBm	21 dBm	21 dBm	22 dBm	19 dbm	15 dBm	15 dBm

A power backoff field heavyClipBackoffPwr can back off power for SU NSS 3 and 4 for MCS0-3 by the value in heavyClipBackoffPwr2x (in steps of 0.5dB). Illustrated in table below.

MCS	SU_12	MU	SU_34
0	From BDF	From BDF	SU_12 – heavyClipBackoffPwr2x
1	From BDF	From BDF	SU_12 – heavyClipBackoffPwr2x
2	From BDF	From BDF	SU_12 – heavyClipBackoffPwr2x
3	From BDF	From BDF	SU_12 – heavyClipBackoffPwr2x
4	From BDF	From BDF	SU_12
5	From BDF	From BDF	SU_12
6	From BDF	From BDF	SU_12
7	From BDF	From BDF	SU_12
8	From BDF	From BDF	SU_12
9	From BDF	From BDF	SU_12

2.9.2 5 GHz CTL power

The general structure of each of the areas is the same, and consists of these components:

CTL Index	Describes the regulatory body, mode, number of chains, number of streams and beamforming status of each CTL being stored
Frequency list	Describes the frequencies to apply to the CTL
Power values	One power for each frequency and mode stored. Also there is an in-band flag to indicate whether power should apply for the current channel or all channels until the next frequency

Table 2-12 5 GHz calibration, target and CTL power

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/Field Description	Bit Num	Bit Definition
calFreqPier5G	calFreqPier5G	32	5GHz channels that are calibrated Ex: (Decimal*5) + 4800Hz = Channel frequency	[255:0]	1 byte per channel (Max 32 channel)
	calFreqPier5G_ext	32	Extend for channel calibrated flag	[255:0]	
calPierData5G(OLPC) - calibration data stored per point per channel per RF chain. (NumOfChain*11B + 4(therm)+1vol))* 32 channels=(4*11B+5B)* 32= 1568 Bytes	calPerPoint	1	txgainIdx cal point 1	[7:3]	value of cal gain index
			pasetting cal point 1	[2:0]	value of cal pasetting
		1	meas_pwr cal point 1	[7:0]	value of measured power
		1	txgainIdx cal point 2	[7:3]	value of cal gain index
			pasetting cal point 2	[2:0]	value of cal pasetting
		1	meas_pwr cal point 2	[7:0]	value of measured power
		1	txgainIdx cal point 3	[7:3]	value of cal gain index
			pasetting cal point 3	[2:0]	value of cal pasetting
		1	meas_pwr cal point 3	[7:0]	value of measured power
		1	txgainIdx cal point 4	[7:3]	value of cal gain index
			pasetting cal point 4	[2:0]	value of cal pasetting
		1	meas_pwr cal point 4	[7:0]	value of measured power
		1	txgainIdx cal point 5	[7:3]	value of cal gain index
			pasetting cal point 5	[2:0]	value of cal pasetting
		1	meas_pwr cal point 5	[7:0]	value of measured power
	dacGain (Per Chain)	1	dacGain of glut gain setting	[7:0]	Value
	thermCalVal (Per Chain)	1	therm_cal_value	[7:0]	Value
	voltCalVal	1	volt_cal_value	[7:0]	Value
pad30	Padding	32	padding	[255:0]	N/A
calData5G_PLUT_Future	calData5G_PLUT_Future	92	calData5G_PLUT_Future	[735:0]	Reserved
Pad31	Padding	2	padding	[15:0]	N/A
powerOffset5G	powerOffset5G	256	Used for power offset for CCK/ OFDM20/40/80 32 channels; 4chains	[2047:0]	Reserved

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/Field Description	Bit Num	Bit Definition
calPierData5G_CLPC (5points*2B*4Chains)* 32 Piers = 1280 Bytes	pdadc_read	1	Pdadc value for each CAL point	[7:0]	Pdadc value for each CAL point
	meas_pwr	1	Measured power value for each CAL point	[7:0]	Measured power value for each CAL point
calData5G_plut_future	calData5G_plut_future	1280	Reserved for additional channels plut: 5point*2data*4chains* 32channels =1280	[10239:0]	Reserved
	alutFuture	72	N/A	[375:0]	N/A
	extTPow2xDelta5G	72	Extend target power delta from 4bit to 5 bit. Here is the all rates 5th bit	[375:0]	5th bits of target power delta
Target powers for channels	targetFreqbin5G	8	11a target powers for these channels Ex: (Decimal*5) + 4800Hz = Channel Frequency	[47:0]	1 byte per channel (Max 6 channel)
	targetFreqbin5GVHT20	8	HT20/VHT20 target powers for these channels Ex: (Decimal*5) + 4800Hz = Channel Frequency	[47:0]	1 byte per channel (Max 6 channel)
	targetFreqbin5GVHT40	8	HT40/VHT40 Target powers for these channels Ex: (Decimal*5) + 4800Hz = Channel Frequency	[47:0]	1 byte per channel (Max 6 channel)
	targetFreqbin5GVHT80	8	VHT80 Target powers for these channels Ex: (Decimal*5) + 4800Hz = Channel Frequency	[47:0]	1 byte per channel (Max 6 channel)
Target power for 5GHz 802.11a rates. 4 bytes per channel * 8 channels = 32 Bytes	targetPower5G	4	Target powers for 802.11a rates Ex: Decimal/2 = Power level [dBm]	[31:24]	54 Mbps
				[23:16]	48 Mbps
				[15:8]	36 Mbps
				[7:0]	6 Mbps - 24 Mbps
Target power for 5GHz VHT 11AC, 11n, Legacy, 2xNSS SU12	targetPower5G SU12,VHT20, G	10	Target powers for SU12_VHT20_G Ex: Decimal/2 = Power level [dBm]	[79:72]	MSC9/NA/NA
				[71:64]	MSC8/NA/NA
				[63:56]	MSC7/MCS7/NA
				[55:48]	MSC6/MCS6/54
				[47:40]	MSC5/MCS5/48
				[39:32]	MSC4/MCS4/36
				[31:24]	MSC3/MCS3/24
				[23:16]	MSC2/MCS2/18
				[15:8]	MSC1/MCS1/12
				[7:0]	MSC0/MCS0/6 or 9
Target power for 5GHz VHT 11AC, 11n, Legacy, 2xNSS SU34 MU	targetPowr5G SU34, MU, VHT20, G		Target powers for SU34_MU__VHT20_G Ex: Decimal/2 = Power level [dBm]	[79:72]	MSC9/NA/NA
				[71:64]	MSC8/NA/NA
				[63:56]	MSC7/MCS7/NA
				[55:48]	MSC6/MCS6/54
				[47:40]	MSC5/MCS5/48
				[39:32]	MSC4/MCS4/36
				[31:24]	MSC3/MCS3/24
				[23:16]	MSC2/MCS2/18
				[15:8]	MSC1/MCS1/12
				[7:0]	MSC0/MCS0/6 or 9

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/Field Description	Bit Num	Bit Definition
RATE_TPC_PA_BW		60		[479:0]	
Sticky write to set register		652		[63:32]	Value
				[31:0]	Address
Rx Gain Cal		192	See Section 2.10	[159:0]	
	ctl5GFuture1	68	Reserved	[5043:0]	Reserved
Alpha thermal table 4 bytes per chain * 8 channels * 4 RF chains = 128 Bytes	alphaThermTbl	4	Alpha thermal table	[31:24]	85
				[23:16]	45
				[15:8]	-10
				[7:0]	-40
5G CTL 11a Index	ctlIndex5G_11a	18	9 indexes, each index 2 bytes 3 modes, 3 regulatory domains	[15:12]	SS mask
				[11:8]	chain mask stream
				[7:4]	REG DOMN
				[3]	BF
				[2:0]	MODE
5G CTL 11a Frequency bin	ctlFreqbin5G_11a	75	((Frequency_in_MHz – 4800)/5) 25 channels; 3 domains; FCC, MKK, ETSI	[7:0]	Freq
Padding		1			
5G CTL 11a data Bin	ctlData5G_11a	225	1 pwr val for frequency and mode 3 modes, 25 channels, 3 reg dmn	[7]	In band flag
				[6:0]	Power in dbm
Padding		1			
5G CTL HT20/VHT20 index	ctlIndex5G_ HT20/VHT20	48	8 indexes, each index 2 bytes 8 modes, 3 regulatory domains	[15:12]	SS mask
				[11:8]	chain mask stream
				[7:4]	REG DOMN
				[3]	BF
				[2:0]	MODE
5G CTL HT20/VHT20 Frequency Bin	ctlFreqbin5G_ HT20/VHT20	75	((Frequency_in_MHz – 4800)/5) 25 Channels; 3 domains FCC, MKK, ETSI	[7:0]	Freq
Padding		1			
5G CTL HT20/VHT20 data Bin	ctlData5G_ HT20/VHT20	600	1 pwr val for frequency and mode 8 modes, 25 channels, 3 reg dmn	[7]	In band flag
				[6:0]	Power in dbm
5G CTL HT40/VHT40 index	ctlIndex5G_ HT40/VHT40	36	18 indexes, each index 2 bytes 6 modes, 3 regulatory domains 3 domains FCC, MKK, ETSI	[15:12]	SS mask
				[11:8]	chain mask stream
				[7:4]	REG DOMN
				[3]	BF
				[2:0]	MODE
5G CTL HT40/VHT40 Frequency Bin	ctlFreqbin5G_ HT40/VHT40	36	((Frequency_in_MHz – 4800)/5) 12 Channels; 3 domains FCC, MKK, ETSI	[7:0]	Freq
5G CTL HT40/VHT40 data bin	ctlData5G_ HT40/VHT40	216	1 pwr val for frequency and mode 6 modes, 12 channels, 3 reg dmn	[7]	In band flag
				[6:0]	Power in dbm

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/Field Description	Bit Num	Bit Definition
5G CTL VHT80 index	ctlIndex5G_VHT80	36	18 indexes, each index 2 bytes 6 modes, 3 regulatory domains 3 domains FCC, MKK, ETSI	[15:12]	SS mask
				[11:8]	chain mask stream
				[7:4]	REG DOMN
				3	BF
				[0:2]	MODE
5G CTL VHT80 Frequency Bin	ctlFreqbin5G_VHT80	18	((Frequency_in_MHz – 4800)/5) 6 Channels; 3 domains FCC, MKK, ETSI	[7:0]	Freq
5G CTL VHT80 data bin	ctlData5G_VHT80	108	1 pwr val for frequency and mode 6 modes, 6 channels, 3 reg dmn	[7]	In band flag
				[6:0]	Power in dBm
5G CTL VHT160 index	ctlIndex5G_HT160	18	9 indexes, each 2 bytes 3 modes, 3 regulatory domains 3 domains FCC, MKK, ETSI	[15:12]	SS mask
				[11:8]	chain mask stream
				[7:4]	REG DOMN
				[3]	BF
				[0:2]	MODE
				[7:0]	Freq
5G CTL VHT160 Frequency Bin	ctlFreqbin5G_HT160	6	((Frequency_in_MHz – 4800)/5) 2 Channels; 3 domains FCC, MKK, ETSI	[7]	In band flag
5G CTL VHT160 data bin	ctlData5G_HT160	18	1 pwr val for frequency and mode 3 modes, 2 channels, 3 reg dmn	[6:0]	Power in dBm
				[15:12]	SS mask
5G CTL VHT80p80 index (freqPri < freqSec)	ctlIndex5G_HT80p80_Primary_lower_freq	18	9 indexes, each 2 bytes 3 modes, 3 regulatory domains 3 domains FCC, MKK, ETSI	[11:8]	chain mask stream
				[7:4]	REG DOMN
				3	BF
				[0:2]	MODE
				[7:0]	MODE (when > 3 bits)
5G CTL VHT80p80 mode extension (freqPri < freqSec)	ctlModeExt_HT80p80_Primary_lower_freq	9	3 modes, 3 regulatory domains 3 domains FCC, MKK, ETSI	[7:0]	Freq
Padding		1		[7]	In band flag
5G CTL VHT80p80 Frequency Bin (freqPri < freqSec)	ctlFreqbin5G_HT80p80_Primary_lower_freq	18	((Frequency_in_MHz – 4800)/5) 6 Channels; 3 domains FCC, MKK, ETSI	[6:0]	Power in dBm
5G CTL VHT80p80 data bin (freqPri < freqSec)	ctlData5G_HT80p80_Primary_lower_freq	54	1 pwr val for frequency and mode 3 modes, 6 channels, 3 reg dmn	[15:12]	SS mask
				[11:8]	chain mask stream
5G CTL VHT80p80 index (freqPri > freqSec)	ctlIndex5G_HT80p80_Primary_higher_freq	18	9 indexes, each 2 bytes 3 modes, 3 regulatory domains 3 domains FCC, MKK, ETSI	[7:4]	REG DOMN
				3	BF
				[0:2]	MODE
				[7:0]	MODE (when > 3 bits)
				[7:0]	Freq
5G CTL VHT80p80 mode extension (freqPri > freqSec)	ctlModeExt_HT80p80_Primary_higher_freq	9	3 modes, 3 regulatory domains 3 domains FCC, MKK, ETSI	[7]	In band flag
Padding		1		[6:0]	Power in dBm

Structure Description	Structure Name/Field Name	Bytes	Structure Detail/Field Description	Bit Num	Bit Definition
5G CTL VHT80p80 Frequency Bin (freqPri > freqSec)	ctlFreqbin5G_HT80p80_Primary_higher_freq	18	((Frequency_in_MHz – 4800)/5) 6 Channels; 3 domains FCC, MKK, ETSI		
5G CTL VHT80p80 data bin (freqPri > freqSec)	ctlData5G_HT80p80_Primary_higher_freq	54	1 pwr val for frequency and mode 3 modes, 6 channels, 3 reg dmn		

NOTE: Note that TPC calibration is also guided by some parameters in board data file. Details on these can be found in the *QCA99xx Power Calibration Application Note* (80-Y8050-20).

2.10 Rx Gain Cal

2.10.1 Rx Gain Cal 5G 96 Bytes

Table 2-13 rxGainCalCfg – Configuration for Rx Gain CAL

Field Name	Bytes	Description	Bit Num	Bit Definition
bandMask	1	Mask for 2G/5G	[7:0]	Value = FF enabled
refISS	1	Reference signal from tester	[7:0]	dbm
rate	1	Rate used for cal	[7:0]	The rate used
bandWidth	1	BW used for Cal	[7:0]	20, 40, 80
numChan	1	Number of channels	[7:0]	
numChain	1	Number of chains	[7:0]	
numPkts	2	Number of packets	[7:0]	Packets used
chans	4	List of channels to be calibrated	[31:0]	List channels; If number of channels is 2, then the two channels are listed here.
chainMasks	4	List of chains to be calibrated	[31:0]	Same for chain masks

Table 2-14 rxGainCalResult– Results for Rx gain CAL for each channel

Field Name	Bytes	Description
rxNFCalPowerDBr	4	Resulting NF for each chain in dBr
rxNFCalPowerDBm	4	Resulting NF for each chain in dBm
rxTempMeas	4	Measured temp for each chain during cal
rxNFThermCalSlope	4	Bench characterized NF Cal slope for each chain
minCcaThreshold	4	Calculated Min CCA threshold for each chain based on calibration

2.10.2 Rx Gain Cal 2G 96 Bytes

Table 2-15 rxGainCalCfg – Configuration for Rx Gain Cal

Field Name	Bytes	Description	Bit Num	Bit Definition
bandMask	1	Mask for 5G	[7:0]	Value = FF
refISS	1	Desired reference signal from tester	[7:0]	Value in dBm
rate	1	Rate to be used for cal	[7:0]	Rate used
bandWidth	1	BW to use for Cal	[7:0]	Enter 20, 40 or 80
numChan	1	Number of channels	[7:0]	Max of 4 channels
numChain	1	Number of chains	[7:0]	Max of 4 chains
numPkts	2	Number of packets	[7:0]	Packets to use
chans	4	List of channels to be calibrated	[31:0]	Cal pier formula up to numChan
chainMasks	4	List of chains to be calibrated	[31:0]	

Table 2-16 rxGainCalResult– Results for Rx Gain Cal for each Channel

Field Name	Bytes	Description	Bit Num	Bit Definition
rxNFCalPowerDBr	4	Result NF for each chain in dBr		
rxNFCalPowerDBm	4	Result NF for each chain in dBm		
rxTempMeas	4	Measured temp for each chain during cal		
rxNFThermCalSlope	4	NF Cal slope for each chain		
minCcaThreshold	4	Min CCA threshold for each chain		

2.11 Calibration data per chip

Table 2-17 Thermal and ATE fields

Field Name	Bytes	Description	Bit Num	Bit Definition
thermAdcScaledGain	2	thermometer ADC scaled gain correction factor (unsigned) for chain0	[15:9]	Reserved
			[8:0]	ADC scaled gain correction
thermAdcOffset	1	thermometer ADC offset correction factor (signed) for chain0	[7:0]	ADC offset correction
rbias	1	Reserved for analog rbias register setting value	[8:0]	Value
thermAdcScaledGain1	2	thermometer ADC scaled gain correction factor (unsigned) for chain1	[15:9]	Reserved
			[8:0]	ADC scaled gain correction
thermAdcOffset1	1	thermometer ADC offset correction factor (signed) for chain1	[7:0]	ADC offset correction
thermAdcScaledGain2	2	thermometer ADC scaled gain correction factor (unsigned) for chain2	[15:9]	Reserved
			[8:0]	ADC scaled gain correction
thermAdcOffset2	1	thermometer ADC offset correction factor (signed) for chain2	[7:0]	ADC offset correction
thermAdcScaledGain3	2	thermometer ADC scaled gain correction factor (unsigned) for chain3	[15:9]	Reserved
			[8:0]	ADC scaled gain correction
thermAdcOffset3	1	thermometer ADC offset correction factor (signed) for chain3	[7:0]	ADC offset correction
configFlag	1	Enable thermal Compensation	[8:0]	Value
ateCALTemp	4	all ATE temp values (ATE_CAL_TEMP, CODE0, Code1)	[31:0]	OTP ATE DATA for chain0-1
ateCALTemp1	4	all ATE temp values (ATE_CAL_TEMP, CODE2, Code3)	[31:0]	OTP ATE DATA for chain2-3
Reserved	14	Reserved	[111:0]	Value

Table 2-18 ATE fields

Structure Description	Field Name	Bytes	Description	Bit Num	Bit Definition
TPC attenuator ATE calibration	tpc_attenuatior	120	5bit (step size) for each calibration point, 15 cal points, internal/external coupler, 2 freq band, 2 chain 5*15*2*2*2 = 600 bits = 75 bytes, to facilitate save/store, use 15*2*2*2=120bytes.	[959:0]	Value
Reserved	Reserved	24	Reserved	[192:0]	Value

A Baseband Registers

A.1 BB_switch_table_com1 register

Table A-1 BB_switch_table_com1 register

Name	BB_switch_table_com1
Prop name	BB_switch_table_com1
Address	0x10688
Description	Common switch table(1) (for all chains, driving SWCOM[x:0] pins of chip). pcu_ant[1] controls lna1/lna2. pcu_ant[0] controls ant1/ant2.
Reset signal	rst_cold_l [rst_cold_l]
Reset value	where U or S respectively represent a bit that Undefined or Signal controlled

Table A-2 BB_switch_table_com1 bit description

Bit	SW	Name	Description	Reset
31:28	R/W	switch_table_com_tx_1chn	When wlan tx on 1 un-shared chain. Rec setting = n/a	4'd0
27:22	R/W	switch_table_com_idle_alt	When idle and OTP_SWCOM_IDLE_MODE is 1'b1. Rec setting = n/a	6'b001010
21:16	R/W	switch_table_com_b	When BlueTooth Rec setting = n/a	6'd0
15:12	R/W	switch_table_com_t2	When tx ant2. Rec setting = n/a	4'd0
11:6	R/W	switch_table_com_t1	When tx ant1. Rec setting = n/a	6'd0
5:0	R/W	switch_table_com_idle	When idle and OTP_SWCOM_IDLE_MODE is 1'b0. Rec setting = n/a	6'b000000

A.2 BB_switch_table_com2 register

Table A-3 BB_switch_table_com2 register

Name	BB_switch_table_com2
Prop name	BB_switch_table_com2
Address	0x1068c
Description	Common switch table (2) (for all chains, driving SWCOM[x:0] pins of chip). pcu_ant[1] controls lna1/lna2. pcu_ant[0] controls ant1/ant2.
Reset signal	rst_cold_l [rst_cold_l]
Reset value	where U or S respectively represent a bit that Undefined or Signal controlled

Table A-4 BB_switch_table_com2 bit description

Bit	SW	Name	Description	Reset
31:22	R	RSVD	RSVD	10'h000
21:18	R/W	switch_table_com_ra12	When rx ant1&2, and lna1&2 combining. Rec setting = n/a	4'd0
17:14	R/W	switch_table_com_ra2l2	When rx ant2, lna2. Rec setting = n/a	4'd0
13:10	R/W	switch_table_com_ra1l2	When rx ant1, lna2. Rec setting = n/a	4'd0
9:6	R/W	switch_table_com_ra2l1	When rx ant2, lna1. Rec setting = n/a	4'd0
5:0	R/W	switch_table_com_ra1l1	When rx ant1, lna1. Rec setting = n/a	6'd0

A.3 BB_switch_table_chn_b0 register

Table A-5 BB_switch_table_chn_b0 register

Name	BB_switch_table_chn_b0
Prop name	BB_switch_table_chn_b0
Address	0x10684
Description	chain 0 switch table (driving XLNAs via radio)
Reset signal	rst_cold_l [rst_cold_l]
Reset value	where U or S respectively represent a bit that Undefined or Signal controlled

Table A-6 BB_switch_table_chn_b0 bit description

Bit	SW	Name	Description	Reset
31	R/W	enable_bt_override	This is to enable override for BT which is needed for QCA9880, but not QCA6174.	1'b0
30	R/W	bt_in_tx_xlna_override	Enable bt_in_tx (BT in high-priority-Tx) to control xlna bias. Protection for QCA6164 FEM control limitation.	1'b1
29:12	R	Reserved	Reserved	18'h00000
11:10	R/W	switch_table_b_0	When Blue Tooth (banked). Rec setting = n/a	2'd0
9:8	R/W	switch_table_rx12_0	When rx ant, xatten1&2 asserted (banked). Rec setting = n/a	2'd0
7:6	R/W	switch_table_rx1_0	When rx ant, xatten1 asserted (banked). Rec setting = n/a	2'd0
5:4	R/W	switch_table_r_0	When rx ant (banked). Rec setting = n/a	2'd0
3:2	R/W	switch_table_t_0	When tx ant (banked). Rec setting = n/a	2'd0
1:0	R/W	switch_table_idle_0	When idle (banked). Rec setting = n/a	2'd0

A.4 BB_ext_atten_switch_ctl_b0 register

Table A-7 BB_ext_atten_switch_ctl_b0 register

Name	BB_ext_atten_switch_ctl_b0
Prop name	BB_ext_atten_switch_ctl_b0
Address	0x10018
Description	External attenuator controls
Reset signal	rst_cold_l [rst_cold_l]
Reset value	where U or S respectively represent a bit that Undefined or Signal controlled

Table A-8 BB_ext_atten_switch_ctl_b0 bit description

Bit	SW	Name	Description	Reset
31:29	R	RSVD	RSVD	3'h0
28:24	R/W	xlna_gain_db_0	External LNA gain used to offset the rf_ref gain table (unsigned dB steps)(banked). Rec setting = 0	5'd0
23:18	R/W	xatten2_margin_0	dB above min on-chip gain (0 dB) to switch open the 2nd attenuation switch (unsigned dB steps)(banked). Rec setting = 0	6'd0
17:12	R/W	xatten1_margin_0	dB above min on-chip gain (0 dB) to switch open the 1st attenuation switch (unsigned dB steps)(banked). Rec setting = 50	6'd0
11:6	R/W	xatten2_db_0	Expected attenuation of 2nd external switch (unsigned dB steps)(banked). Rec setting = 18	6'd0
5:0	R/W	xatten1_db_0	Expected attenuation of 1st external switch (unsigned dB steps)(banked). Rec setting = 15	6'd0

B Related Documentation

Doc Number	Title
80-Y8050-1	QDART-Connectivity User Guide
80-Y8050-3	Preserving Test Trees and Configuration Files When Upgrading the QDART-Connectivity Package
80-Y8050-4	Loop Setup and Chain Selection Application Note
80-Y8050-5	QCA99xx Utilities Application Note
80-Y8050-6	QCA99xx BDF Structure Application Note
80-Y8050-8	Up and Running with QLINE Application Notes
80-Y8050-10	ATLV Commands
80-Y8050-11	QCA99xx FTM API WLAN Non-Signaling Commands
80-Y8050-12	QCA99xx Target Power
80-Y8050-13	QCA9990 Rx Noise Floor and Rx Gain Calibration Implementation Overview
80-Y8050-14	Porting QCMBR to Non-Win7 OS Platforms
80-Y8050-16	QCA99xx Target and Control Power Modification Application Note
80-Y8050-17	QDART-Connectivity Laptop Setup and Checklist
80-Y8050-18	QCA9900 Crystal Calibration Algorithm Application Note
80-Y8050-19	QCA9900 QSPR Calibration Process Application Note
80-Y8050-20	QCA9900 Power Calibration Application Note
80-Y8050-21	QCA99xx QLIB WLAN Commands
80-Y8050-27	QCA99xx CTL Power Layout
80-Y8050-28	QCA99xx CTL Power and Utilities Application Note
80-Y8924-1	QCA99xx QDART Plus Testing Training
VD80-NT271-1	Video: Introduction to QDTA-QMINE