



88E1111 Product Brief




**Integrated 10/100/1000 Ultra
Gigabit Ethernet Transceiver**

Doc. No. MV-S105540-00, Rev. A

October 10, 2013

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Document Conventions

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OVERVIEW

The Alaska[®] Ultra 88E1111 Gigabit Ethernet Transceiver is a physical layer device for Ethernet 1000BASE-T, 100BASE-TX, and 10BASE-T applications. It is manufactured using standard digital CMOS process and contains all the active circuitry required to implement the physical layer functions to transmit and receive data on standard CAT 5 unshielded twisted pair.

The 88E1111 device incorporates the Marvell Virtual Cable Tester[®] (VCT[™]) feature, which uses Time Domain Reflectometry (TDR) technology for the remote identification of potential cable malfunctions, thus reducing equipment returns and service calls. Using VCT, the Alaska 88E1111 device detects and reports potential cabling issues such as pair swaps, pair polarity and excessive pair skew. The device will also detect cable opens, shorts or any impedance mismatch in the cable and report accurately within one meter the distance to the fault.

The 88E1111 device supports the Gigabit Media Independent Interface (GMII), Reduced GMII (RGMII), Serial Gigabit Media Independent Interface (SGMII), the Ten-Bit Interface (TBI), and Reduced TBI (RTBI) for direct connection to a MAC/Switch port.

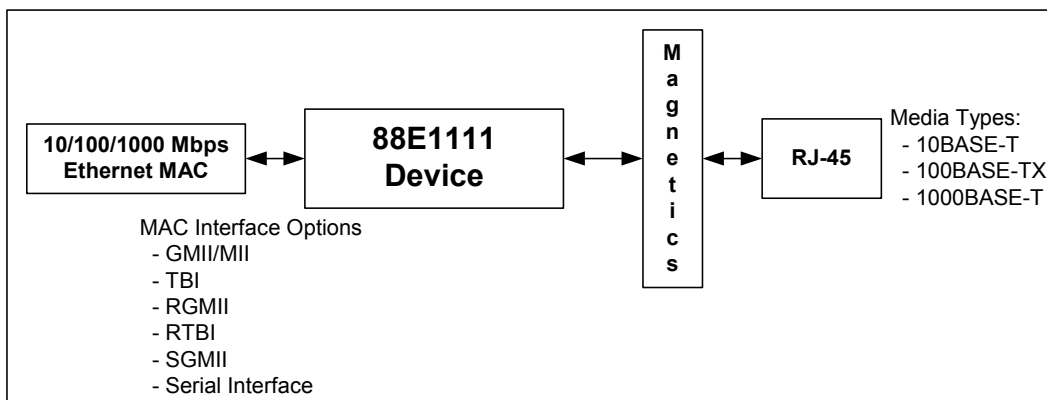
The 88E1111 device incorporates an optional 1.25 GHz SERDES (Serializer/Deserializer). The serial interface may be connected directly to a fiber-optic transceiver for 1000BASE-T/1000BASE-X media conversion applications. Additionally, the 88E1111 device may be used to implement 1000BASE-T Gigabit Interface Converter (GBIC) or Small Form Factor Pluggable (SFP) modules.

The 88E1111 device uses advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a gigabit per second data rate. The device achieves robust performance in noisy environments with very low power dissipation.

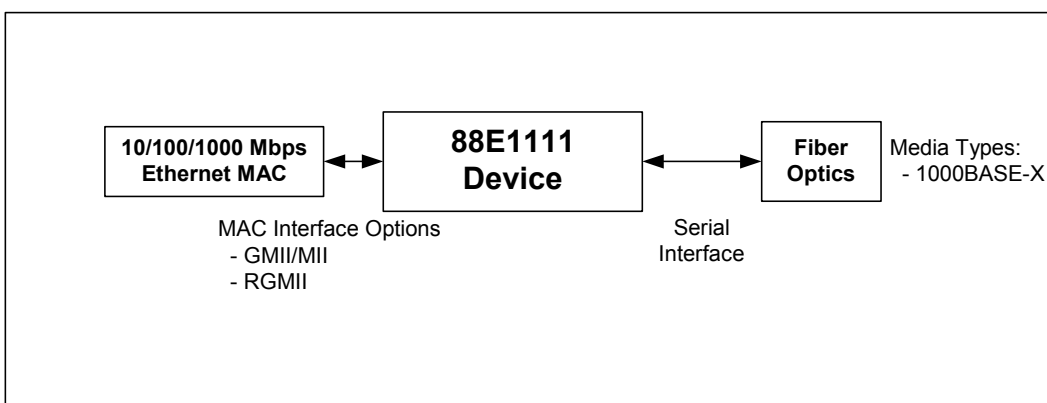
The 88E1111 device is offered in three different package options including a 117-Pin TFBGA, a 96-pin aQFN featuring a body size of only 9 x 9 mm, and a 128 PQFP package.

FEATURES

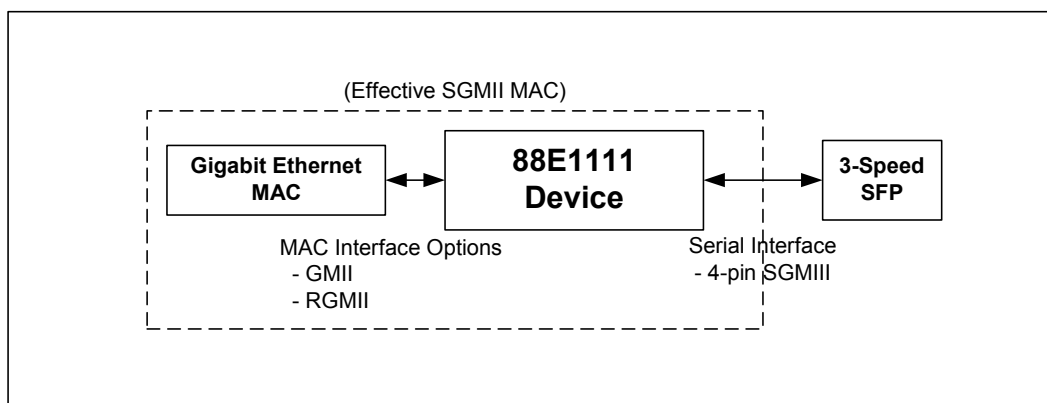
- 10/100/1000BASE-T IEEE 802.3 compliant
- Supports GMII, TBI, reduced pin count GMII (RGMII), reduced pin count TBI (RTBI), and serial GMII (SGMII) interfaces
- Integrated 1.25 GHz SERDES for 1000BASE-X fiber applications
- Four RGMII timing modes
- Energy Detect and Energy Detect+ low power modes
- Three loopback modes for diagnostics
- "Downshift" mode for two-pair cable installations
- Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers
- Advanced digital baseline wander correction
- Automatic MDI/MDIX crossover at all speeds of operation
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Software programmable LED modes including LED testing
- Automatic detection of fiber or copper operation
- Supports IEEE 1149.1 JTAG
- Two-Wire Serial Interface (TWSI) and MDC/MDIO
- CRC checker, packet counter
- Packet generation
- Virtual Cable Tester (VCT)
- Auto-Calibration for MAC Interface outputs
- Requires only two supplies: 2.5V and 1.0V (with 1.2V option for the 1.0V supply)
- I/Os are 3.3V tolerant
- Low power dissipation Pave = 0.75W
- 117-Pin TFBGA, 96-Pin aQFN, and 128 PQFP package options (NOTE: The 96-Pin BCC package is obsolete and is no longer available. The 96-Pin aQFN package is a pin compatible replacement for the 96-Pin BCC package. See Product Change Notification 1210066 and [Table 20](#) for details.)
- 117-Pin TFBGA and 96-Pin aQFN packages available in Commercial or Industrial grade
- RoHS 6/6 compliant packages available



88E1111 Device used in Copper Application



88E1111 Device used in Fiber Application



88E1111 RGMII/GMII MAC to SGMII MAC Conversion

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Section 1. Signal Description

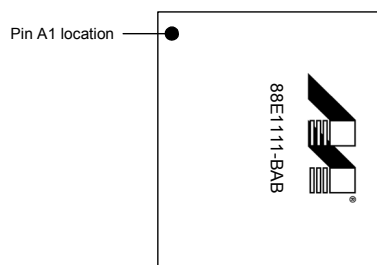
The 88E1111 device is a 10/100/1000BASE-T/1000BASE-X Gigabit Ethernet transceiver.

1.1 117-Pin TFBGA Package

Figure 1: 88E1111 Device 117-Pin TFBGA Package (Top View)

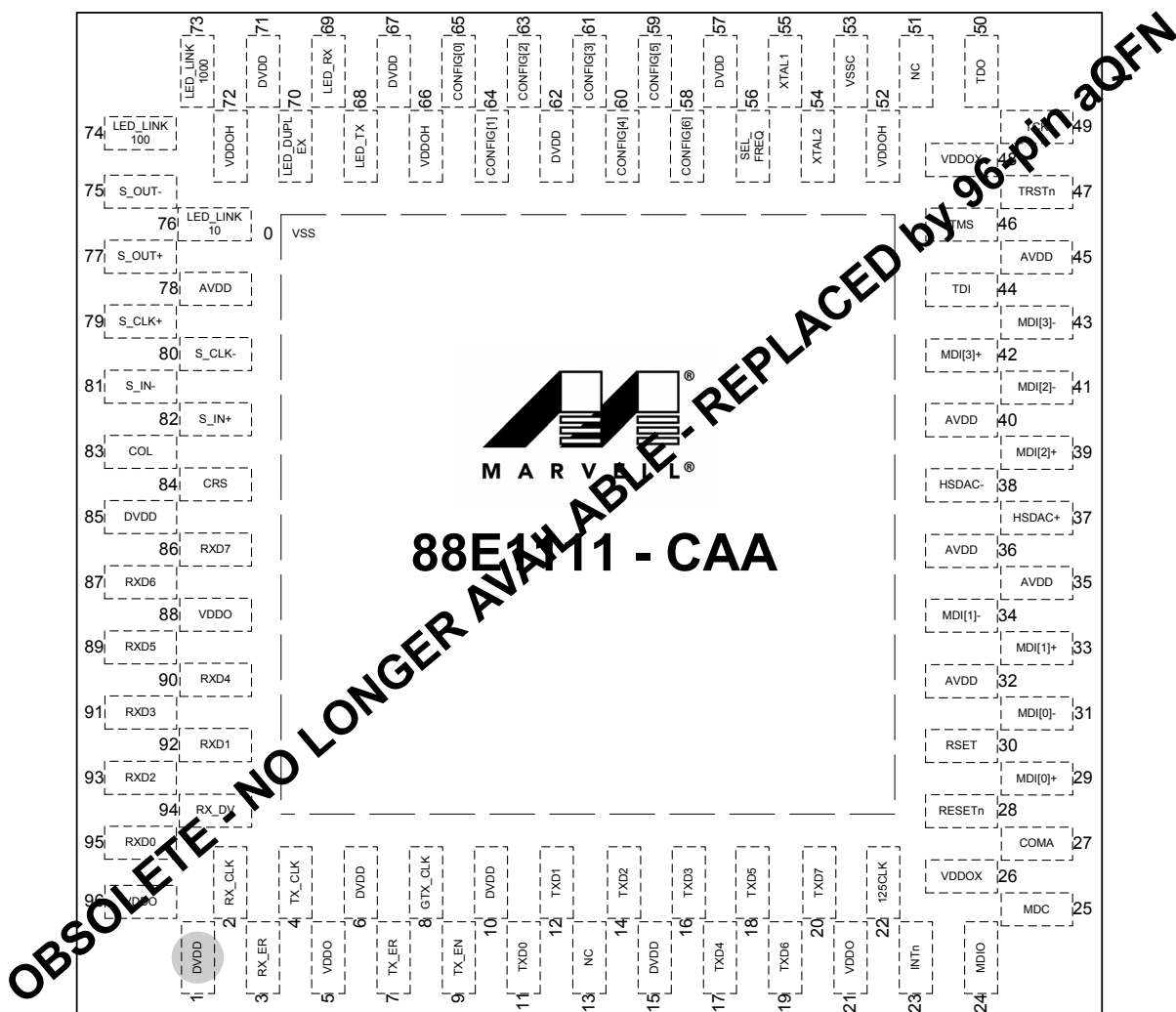
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |
|---|---------|---------|---------|---------|--------|---------|-----------|-------------|--------------|---|
| A | RXD5 | RXD6 | S_IN+ | S_IN- | S_CLK+ | S_CLK- | S_OUT+ | S_OUT- | LED_LINK1000 | A |
| B | RX_DV | RXD0 | RXD3 | VDDO | CRS | COL | AVDD | LED_LINK100 | VDDOH | B |
| C | RX_CLK | VDDO | RXD2 | RXD4 | RXD7 | DVDD | DVDD | LED_LINK10 | LED_RX | C |
| D | TX_CLK | RX_ER | RXD1 | VSS | VSS | VSS | DVDD | CONFIG[0] | LED_TX | D |
| E | TX_EN | GTX_CLK | DVDD | VSS | VSS | VSS | DVDD | LED_DUPLEX | CONFIG[1] | E |
| F | TXD0 | TX_ER | DVDD | VSS | VSS | VSS | VDDOH | CONFIG[2] | CONFIG[4] | F |
| G | NC | TXD1 | TXD2 | VSS | VSS | VSS | CONFIG[3] | CONFIG[6] | CONFIG[5] | G |
| H | TXD4 | TXD3 | TXD5 | VSS | VSS | VSS | VSSC | SEL_FREQ | XTAL1 | H |
| J | TXD6 | TXD7 | DVDD | VSS | VSS | VSS | DVDD | VDDOH | XTAL2 | J |
| K | VDDO | 125CLK | RESETn | VSS | VSS | VSS | NC | TDO | VDDOX | K |
| L | INTn | VDDOX | MDC | COMA | VSS | VSS | TDI | TMS | TCK | L |
| M | MDIO | RSET | AVDD | AVDD | HSDAC+ | HSDAC- | AVDD | AVDD | TRSTn | M |
| N | MDI[0]+ | MDI[0]- | MDI[1]+ | MDI[1]- | AVDD | MDI[2]+ | MDI[2]- | MDI[3]+ | MDI[3]- | N |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |

Figure 2: Pin A1 Location



1.2 96-Pin aQFN Package

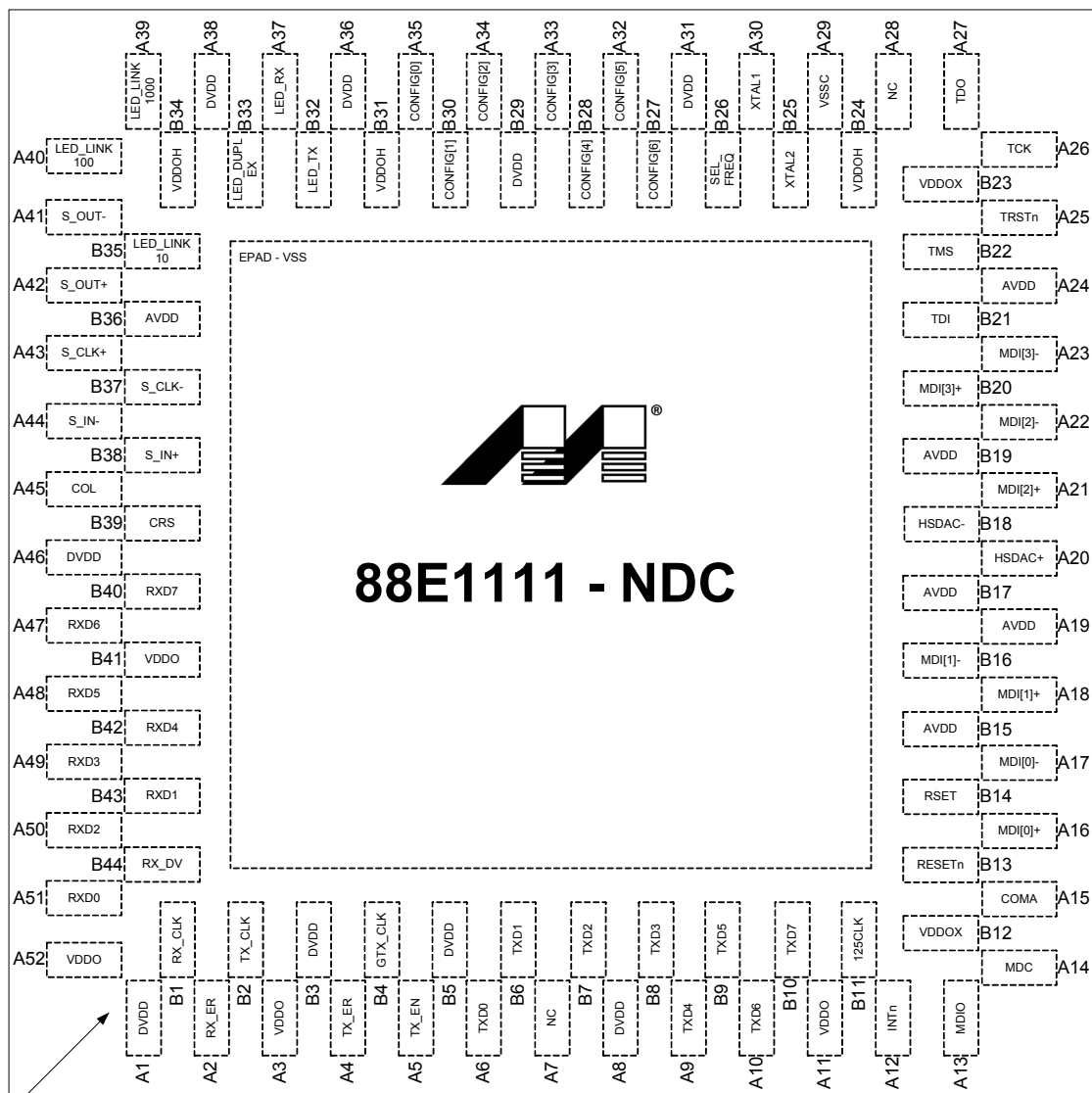
Figure 3: 88E1111 Device 96-Pin BCC Package (Top View) - (OBSOLETE - No Longer Available - Replaced by 96-Pin aQFN Package)



Note

The 96-Pin aQFN package is a pin compatible replacement for the 96-Pin BCC package. See Product Change Notification 1210066 and [Table 20](#) for details.

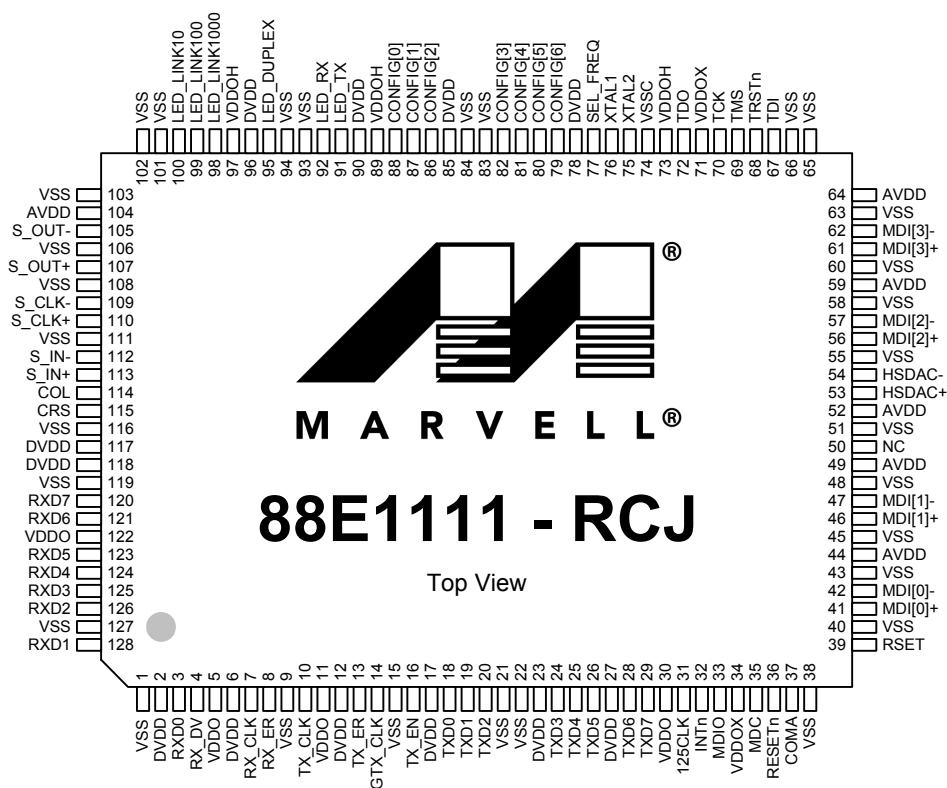
Figure 4: 88E1111 Device 96-Pin aQFN Package (Top View)



Pin 1 Corner

1.3 128-Pin PQFP Package

Figure 5: 88E1111 Device 128-Pin PQFP Package (Top View)



1.4 Pin Description

1.4.1 Pin Type Definitions

| Pin Type | Definition |
|-----------------|-----------------------|
| H | Input with hysteresis |
| I/O | Input and output |
| I | Input only |
| O | Output only |
| PU | Internal pull up |
| PD | Internal pull down |
| D | Open drain output |
| Z | Tri-state output |
| mA | DC sink capability |

Table 1: Media Dependent Interface

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|----------------------------|--------------------------|---------------------------|--------------------|-----------------|--|
| N1 N2 | A16 A17 | 41 42 | MDI[0]+ MDI[0]- | I/O, D | Media Dependent Interface[0]. In 1000BASE-T mode in MDI configuration, MDI[0]± correspond to BI_DA±. In MDIX configuration, MDI[0]± correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDI[0]± are used for the transmit pair. In MDIX configuration, MDI[0]± are used for the receive pair. MDI[0]± should be tied to ground if not used. |
| N3 N4 | A18 B16 | 46 47 | MDI[1]+ MDI[1]- | I/O, D | Media Dependent Interface[1]. In 1000BASE-T mode in MDI configuration, MDI[1]± correspond to BI_DB±. In MDIX configuration, MDI[1]± correspond to BI_DA±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDI[1]± are used for the receive pair. In MDIX configuration, MDI[1]± are used for the transmit pair. MDI[1]± should be tied to ground if not used. |

Table 1: Media Dependent Interface (Continued)

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|----------------------------|--------------------------|---------------------------|-------------------|-----------------|--|
| N6 N7 | A21 A22 | 56 57 | MDI[2] MDI[2]- | I/O, D | Media Dependent Interface[2]. In 1000BASE-T mode in MDI configuration, MDI[2] \pm correspond to BI_DC \pm . In MDIX configuration, MDI[2] \pm corresponds to BI_DD \pm . In 100BASE-TX and 10BASE-T modes, MDI[2] \pm are not used. MDI[2] \pm should be tied to ground if not used. |
| N8 N9 | B20 A23 | 61 62 | MDI[3] MDI[3]- | I/O, D | Media Dependent Interface[3]. In 1000BASE-T mode in MDI configuration, MDI[3] \pm correspond to BI_DD \pm . In MDIX configuration, MDI[3] \pm correspond to BI_DC \pm . In 100BASE-TX and 10BASE-T modes, MDI[3] \pm are not used. MDI[3] \pm should be tied to ground if not used. |

The GMII interface supports both 1000BASE-T and 1000BASE-X modes of operation. The GMII interface pins are also used for the TBI interface. See [Table 3](#) for TBI pin definitions. The MAC interface pins are 3.3V tolerant.

Table 2: GMII/MII Interfaces

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|--------------------|------------------|-------------------|----------|----------|---|
| E2 | B4 | 14 | GTX_CLK | I | GMII Transmit Clock. GTX_CLK provides a 125 MHz clock reference for TX_EN, TX_ER, and TXD[7:0]. This clock can be stopped when the device is in 10/100BASE-T modes, and also during Auto-Negotiation. |
| D1 | B2 | 10 | TX_CLK | O, Z | <p>MII Transmit Clock. TX_CLK provides a 25 MHz clock reference for TX_EN, TX_ER, and TXD[3:0] in 100BASE-TX mode, and a 2.5 MHz clock reference in 10BASE-T mode.</p> <p>TX_CLK provides a 25 MHz, 2.5 MHz, or 0 MHz clock during 1000 Mbps Good Link, Auto-Negotiation, and Link Lost states depending on the setting of register 20.6:4.</p> <p>The 2.5 MHz clock is the default rate, which may be programmed to another frequency by writing to register 20.6:4.</p> |
| E1 | A5 | 16 | TX_EN | I | <p>GMII and MII Transmit Enable. In GMII/MII mode when TX_EN is asserted, data on TXD[7:0] along with TX_ER is encoded and transmitted onto the cable.</p> <p>TX_EN is synchronous to GTX_CLK, and synchronous to TX_CLK in 100BASE-TX and 10BASE-T modes.</p> |
| F2 | A4 | 13 | TX_ER | I | <p>GMII and MII Transmit Error. In GMII/MII mode when TX_ER and TX_EN are both asserted, the transmit error symbol is transmitted onto the cable. When TX_ER is asserted with TX_EN de-asserted, carrier extension symbol is transmitted onto the cable.</p> <p>TX_ER is synchronous to GTX_CLK, and synchronous to TX_CLK in 100BASE-TX and 10BASE-T modes.</p> |

Table 2: GMII/MII Interfaces (Continued)

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|--|--|--|--|-----------------|---|
| J2 J1 H3 H1 H2 G3 G2 F1 | B10 A10 B9 A9 B8 B7 B6 A6 | 29 28 26 25 24 20 19 18 | TXD[7] TXD[6] TXD[5] TXD[4] TXD[3]/TXD[3] TXD[2]/TXD[2] TXD[1]/TXD[1] TXD[0]/TXD[0] | I | <p>GMII and MII Transmit Data. In GMII mode, TXD[7:0] present the data byte to be transmitted onto the cable in 1000BASE-T mode.</p> <p>In MII mode, TXD[3:0] present the data nibble to be transmitted onto the cable in 100BASE-TX and 10BASE-T modes. TXD[7:4] are ignored in these modes, but should be driven either high or low. These pins must not float.</p> <p>TXD[7:0] are synchronous to GTX_CLK, and synchronous to TX_CLK in 100BASE-TX and 10BASE-T modes.</p> <p>Inputs TXD[7:4] should be tied low if not used (e.g., RGMII mode).</p> |
| C1 | B1 | 7 | RX_CLK | O, Z | <p>GMII and MII Receive Clock. RX_CLK provides a 125 MHz clock reference for RX_DV, RX_ER, and RXD[7:0] in 1000BASE-T mode, a 25 MHz clock reference in 100BASE-TX mode, and a 2.5 MHz clock reference in 10BASE-T mode.</p> <p>TX_TCLK comes from the RX_CLK pins used in jitter testing. Refer to Register 9 for jitter test modes.</p> |
| B1 | B44 | 4 | RX_DV | O, Z | <p>GMII and MII Receive Data Valid. When RX_DV is asserted, data received on the cable is decoded and presented on RXD[7:0] and RX_ER.</p> <p>RX_DV is synchronous to RX_CLK.</p> |
| D2 | A2 | 8 | RX_ER | O, Z | <p>GMII and MII Receive Error. When RX_ER and RX_DV are both asserted, the signals indicate an error symbol is detected on the cable.</p> <p>When RX_ER is asserted with RX_DV deasserted, a false carrier or carrier extension symbol is detected on the cable.</p> <p>RX_ER is synchronous to RX_CLK.</p> |

Table 2: GMII/MII Interfaces (Continued)

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|--|--|--|--|-----------------|--|
| C5 A2 A1 C4 B3 C3 D3 B2 | B40 A47 A48 B42 A49 A50 B43 A51 | 120 121 123 124 125 126 128 3 | RXD[7] RXD[6] RXD[5] RXD[4] RXD[3]/RXD[3] RXD[2]/RXD[2] RXD[1]/RXD[1] RXD[0]/RXD[0] | O, Z | <p>GMII and MII Receive Data. Symbols received on the cable are decoded and presented on RXD[7:0] in 1000BASE-T mode.</p> <p>In MII mode, RXD[3:0] are used in 100BASE-TX and 10BASE-T modes. In MII mode, RXD[7:4] are driven low.</p> <p>RXD[7:0] is synchronous to RX_CLK.</p> |
| B5 | B39 | 115 | CRS | O, Z | <p>GMII and MII Carrier Sense. CRS asserts when the receive medium is non-idle. In half-duplex mode, CRS is also asserted during transmission. CRS assertion during half-duplex transmit can be disabled by programming register 16.11 to 0.</p> <p>CRS is asynchronous to RX_CLK, GTX_CLK, and TX_CLK.</p> |
| B6 | A45 | 114 | COL | O, Z | <p>GMII and MII Collision. In 10/100/1000BASE-T full-duplex modes, COL is always low. In 10/100/1000BASE-T half-duplex modes, COL asserts only when both the transmit and receive media are non-idle.</p> <p>In 10BASE-T half-duplex mode, COL is asserted to indicate signal quality error (SQE). SQE can be disabled by clearing register 16.2 to zero.</p> <p>COL is asynchronous to RX_CLK, GTX_CLK, and TX_CLK.</p> |

The TBI interface supports 1000BASE-T mode of operation. The TBI interface uses the same pins as the GMII interface. The MAC interface pins are 3.3V tolerant.

Table 3: TBI Interface

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|--|--|--|--|----------|---|
| E2 | B4 | 14 | GTX_CLK/ TBI_TXCLK | I | TBI Transmit Clock. In TBI mode, GTX_CLK is used as TBI_TXCLK. TBI_TXCLK is a 125 MHz transmit clock. TBI_TXCLK provides a 125 MHz clock reference for TX_EN, TX_ER, and TXD[7:0]. |
| D1 | B2 | 10 | TX_CLK/RCLK1 | O, Z | TBI 62.5 MHz Receive Clock- even code group. In TBI mode, TX_CLK is used as RCLK1. |
| J2 J1 H3 H1 H2 G3 G2 F1 | B10 A10 B9 A9 B8 B7 B6 A6 | 29 28 26 25 24 20 19 18 | TXD[7] TXD[6] TXD[5] TXD[4] TXD[3] TXD[2] TXD[1] TXD[0] | I | TBI Transmit Data. TXD[7:0] presents the data byte to be transmitted onto the cable. TXD[9:0] are synchronous to GTX_CLK. Inputs TXD[7:4] should be tied low if not used (e.g., RTBI mode). |
| E1 | A5 | 16 | TX_EN/ TXD8 | I | TBI Transmit Data. In TBI mode, TX_EN is used as TXD8. TXD[9:0] are synchronous to GTX_CLK. |
| F2 | A4 | 13 | TX_ER/ TXD9 | I | TBI Transmit Data. In TBI mode, TX_ER is used as TXD9. TXD[9:0] are synchronous to GTX_CLK. TX_ER should be tied low if not used (e.g., RTBI mode). |
| C1 | B1 | 7 | RX_CLK/ RCLK0 | O, Z | TBI 62.5 MHz Receive Clock- odd code group. In the TBI mode, RX_CLK is used as RCLK0. |
| C5 A2 A1 C4 B3 C3 D3 B2 | B40 A47 A48 B42 A49 A50 B43 A51 | 120 121 123 124 125 126 128 3 | RXD[7] RXD[6] RXD[5] RXD[4] RXD[3] RXD[2] RXD[1] RXD[0] | O, Z | TBI Receive Data code group [7:0]. In the TBI mode, RXD[7:0] present the data byte to be transmitted to the MAC. Symbols received on the cable are decoded and presented on RXD[7:0]. RXD[7:0] are synchronous to RCLK0 and RCLK1. |
| B1 | B44 | 4 | RX_DV/ RXD8 | O, Z | TBI Receive Data code group bit 8. In the TBI mode, RX_DV is used as RXD8. RXD[9:0] are synchronous to RCLK0 and RCLK1. |

Table 3: TBI Interface (Continued)

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|----------------------------|--------------------------|---------------------------|-----------------|-----------------|--|
| D2 | A2 | 8 | RX_ER/ RXD9 | O, Z | TBI Receive Data code group bit 9. In the TBI mode, RX_ER is used as RXD9. RXD[9:0] are synchronous to RCLK0 and RCLK1. |
| B5 | B39 | 115 | CRS/ COMMA | O, Z | TBI Valid Comma Detect. In the TBI mode, CRS is used as COMMA. |
| B6 | A45 | 114 | COL/LPBK | I | TBI Mode Loopback. In the TBI mode, COL is used to indicate loopback on the TBI. When a "0 - 1" transition is sampled on this pin, bit 0.14 is set to 1. When a "1 - 0" is sampled on this pin, bit 0.14 is reset to 0. If this feature is not used, the COL pin should be driven low on the board. This pin should not be left floating in TBI mode. |

The RGMII interface supports 10/100/1000BASE-T and 1000BASE-X modes of operation. The RGMII interface pins are also used for the RTBI interface. See [Table 5](#) for RTBI pin definitions. The MAC interface pins are 3.3V tolerant.

Table 4: RGMII Interface

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|----------------------|----------------------|----------------------|--|----------|--|
| E2 | B4 | 14 | GTX_CLK/ TXC | I | RGMII Transmit Clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock with ± 50 ppm tolerance depending on speed. In RGMII mode, GTX_CLK is used as TXC. |
| H2 G3 G2 F1 | B8 B7 B6 A6 | 24 20 19 18 | TXD[3]/TD[3] TXD[2]/TD[2] TXD[1]/TD[1] TXD[0]/TD[0] | I | RGMII Transmit Data. In RGMII mode, TXD[3:0] are used as TD[3:0]. In RGMII mode, TXD[3:0] run at double data rate with bits [3:0] presented on the rising edge of GTX_CLK, and bits [7:4] presented on the falling edge of GTX_CLK. In this mode, TXD[7:4] are ignored. In RGMII 10/100BASE-T modes, the transmit data nibble is presented on TXD[3:0] on the rising edge of GTX_CLK. |
| E1 | A5 | 16 | TX_EN/ TX_CTL | I | RGMII Transmit Control. In RGMII mode, TX_EN is used as TX_CTL. TX_EN is presented on the rising edge of GTX_CLK. A logical derivative of TX_EN and TX_ER is presented on the falling edge of GTX_CLK. |
| C1 | B1 | 7 | RX_CLK/ RXC | O, Z | RGMII Receive Clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock with ± 50 ppm tolerance derived from the received data stream depending on speed. In RGMII mode, RX_CLK is used as RXC. |

Table 4: RGMII Interface (Continued)

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|----------------------------|--------------------------|---------------------------|--|-----------------|--|
| B1 | B44 | 4 | RX_DV/ RX_CTL | O, Z | <p>RGMII Receive Control. In RGMII mode, RX_DV is used as RX_CTL. RX_DV is presented on the rising edge of RX_CLK.</p> <p>A logical derivative of RX_DV and RX_ER is presented on the falling edge of RX_CLK.</p> |
| B3 C3 D3 B2 | A49 A50 B43 A51 | 125 126 128 3 | RXD[3]/RD[3] RXD[2]/RD[2] RXD[1]/RD[1] RXD[0]/RD[0] | O, Z | <p>RGMII Receive Data. In RGMII mode, RXD[3:0] are used as RD[3:0]. In RGMII mode, RXD[3:0] run at double data rate with bits [3:0] presented on the rising edge of RX_CLK, and bits [7:4] presented on the falling edge of RX_CLK. In this mode, RXD[7:4] are ignored.</p> <p>In RGMII 10/100BASE-T modes, the receive data nibble is presented on RXD[3:0] on the rising edge of RX_CLK. RXD[3:0] are synchronous to RX_CLK.</p> |

The RTBI interface supports 1000BASE-T mode of operation. The RTBI interface uses the same pins as the RGMII interface. The MAC interface pins are 3.3V tolerant.

Table 5: RTBI Interface

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|----------------------|-------------------------|------------------------|--|----------|--|
| E2 | B4 | 14 | GTX_CLK/ TXC | I | RGMII Transmit Clock provides a 125 MHz reference clock with ± 50 ppm tolerance. In RTBI mode, GTX_CLK is used as TXC. |
| H2 G3 G2 F1 | B8 B7 B6 A6 | 24 20 19 18 | TXD[3]/TD[3] TXD[2]/TD[2] TXD[1]/TD[1] TXD[0]/TD[0] | I | RTBI Transmit Data. In RTBI mode, TXD[3:0] are used as TD[3:0]. TD[3:0] run at double data rate with bits [3:0] presented on the rising edge of GTX_CLK, and bits [8:5] presented on the falling edge of GTX_CLK. In this mode, TXD[7:4] are ignored. |
| E1 | A5 | 16 | TX_EN/ TD4_TD9 | I | RTBI Transmit Data. In RTBI mode, TX_EN is used as TD4_TD9. TD4_TD9 runs at a double data rate with bit 4 presented on the rising edge of GTX_CLK, and bit 9 presented on the falling edge of GTX_CLK. |
| C1 | B1 | 7 | RX_CLK/ RXC | O, Z | RTBI Receive Clock provides a 125 MHz reference clock with ± 50 ppm tolerance derived from the received data stream. In RTBI mode, RX_CLK is used as RXC. |
| B3 C3 D3 B2 | 91 A50 B43 A51 | 125 126 128 3 | RXD[3]/RD[3] RXD[2]/RD[2] RXD[1]/RD[1] RXD[0]/RD[0] | O, Z | RTBI Receive Data. In RTBI mode, RXD[3:0] are used as RD[3:0]. RD[3:0] runs at double data rate with bits [3:0] presented on the rising edge of RX_CLK, and bits [8:5] presented on the falling edge of RX_CLK. In this mode, RXD[7:4] are ignored. |
| B1 | B44 | 4 | RX_DV/ RD4_RD9 | O, Z | RTBI Receive Data. In RTBI mode, RX_DV is used as RD4_RD9. RD4_RD9 runs at a double data rate with bit 4 presented on the rising edge of RX_CLK, and bit 9 presented on the falling edge of RX_CLK. |

Table 6: SGMII Interface

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|--------------------|------------------|-------------------|------------------|----------|---|
| A3 A4 | B38 A44 | 113 112 | S_IN+ S_IN- | I | SGMII Transmit Data. 1.25 GBaud input - Positive and Negative. Input impedance on the S_IN± pins may be programmed for 50 ohm or 75 ohm impedance by setting register 26.6. The input impedance default setting is determined by the 75/50 OHM configuration pin. |
| A5 A6 | A43 B37 | 110 109 | S_CLK+ S_CLK- | I/O | SGMII 625 MHz Receive Clock. For Serial Interface modes (HWCFG_MODE[3:0] = 1x00) the S_CLK± pins become Signal Detect± (SD±) inputs. |
| A7 A8 | A42 A41 | 107 105 | S_OUT+ S_OUT- | O, Z | SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output impedance on the S_OUT± pins may be programmed for 50 ohm or 75 ohm impedance by setting register 26.5. Output amplitude can be adjusted via register 26.2:0. The output impedance default setting is determined by the 75/50 OHM configuration pin. |

Table 7: 1.25 GHz Serial High Speed Interface

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|----------------------------|--------------------------|---------------------------|--------------------------|-----------------|---|
| A3 A4 | B38 A44 | 113 112 | S_IN+ S_IN- | I | <p>1.25 GHz input - Positive and Negative. When this interface is used as a MAC interface, the MAC transmitter's positive output connects to the S_IN+. The MAC transmitter's negative output connects to the S_IN-.</p> <p>When this interface is used as a fiber interface, the fiber-optic transceiver's positive output connects to the S_IN+. The fiber-optic transceiver's negative output connects to the S_IN-.</p> <p>Input impedance on the S_IN± pins may be programmed for 50 ohm or 75 ohm impedance by setting register 26.6. The input impedance default setting is determined by the 75/50 OHM configuration pin.</p> |
| A5 A6 | A43 B37 | 110 109 | S_CLK+/SD+ S_CLK-/SD- | I | <p>Signal Detect input.</p> <p>For Serial Interface modes the S_CLK± pins become Signal Detect± (SD±) inputs.</p> |
| A7 A8 | A42 A41 | 107 105 | S_OUT+ S_OUT- | O, Z | <p>1.25 GHz output – Positive and Negative. When this interface is used as a MAC interface, S_OUT+ connects to the MAC receiver's positive input. S_OUT- connects to the MAC receiver's negative input.</p> <p>When this interface is used as a fiber interface, S_OUT+ connects to the fiber-optic transceiver's positive input. S_OUT- connects to the fiber-optic transceiver's negative input.</p> <p>Output impedance on the S_OUT± pins may be programmed for 50 ohm or 75 ohm impedance by setting register 26.5. Output amplitude can be adjusted via register 26.2:0. The output impedance default setting is determined by the 75/50 OHM configuration pin.</p> |

Table 7: 1.25 GHz Serial High Speed Interface (Continued)

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|----------------------------|--------------------------|---------------------------|-----------------|-----------------|--|
| B3 | A49 | 125 | RXD[3] | O, Z | Serial MAC interface Copper Link Status[1] connection. 1 = Copper link up 0 = Copper link down |
| C3 | A50 | 126 | RXD[2] | O, Z | Serial MAC interface Copper Link Status[0] connection. 1 = Copper link down 0 = Copper link up |
| D3 | B43 | 128 | RXD[1] | O, Z | Serial MAC interface PHY_SIGDET[1] connection. 1 = S_OUT± valid code groups according to clause 36. 0 = S_OUT± invalid |
| B2 | A51 | 3 | RXD[0] | O, Z | Serial MAC interface PHY_SIGDET[0] connection. 1 = S_OUT± invalid 0 = S_OUT± valid code groups according to clause 36 |

Table 8: Management Interface and Interrupt

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|--------------------|------------------|-------------------|----------|-------------------------|--|
| L3 | A14 | 35 | MDC | I 3.3V Tolerant | MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 8.3 MHz. |
| M1 | A13 | 33 | MDIO | I/O 3.3V Tolerant | MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm. |
| L1 | A12 | 32 | INTn | D | The polarity of the INTn pin may be programmed at hardware reset by setting the INT_POL bit. Polarity: 0 = Active High 1 = Active Low |

Table 9: Two-Wire Serial Interface

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|--------------------|------------------|-------------------|----------|----------|---|
| L3 | A14 | 35 | MDC/SCL | I | Two-Wire Serial Interface (TWI) serial clock line. When the 88E1111 device is connected to the bus, MDC connects to the serial clock line (SCL). Data is input on the rising edge of SCL, and output on the falling edge. |
| M1 | A13 | 33 | MDIO/SDA | I/O | TWIS serial data line. When the 88E1111 device is connected to the bus, MDIO connects to the serial data line (SDA). This pin is open-drain and may be wire-ORed with any number of open-drain devices. |

Table 10: LED Interface

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|----------------------------|--------------------------|---------------------------|-----------------|-----------------|--|
| C8 | B35 | 100 | LED_LINK10 | O, mA | <p>Parallel LED output for 10BASE-T link or speed. This active low LED pin may be programmed in direct drive or combined LED modes by programming register LED_LINK Control register 24.4:3.</p> <p>In direct drive LED mode, this pin indicates 10 Mbps link up or down.</p> <p>In combined LED mode, the output from LED_LINK10, LED_LINK100, and LED_LINK1000 must be read together to determine link and speed status.</p> <p>LED_LINK10 is a multi-function pin used to configure the 88E1111 device at the de-assertion of hardware reset.</p> |
| B8 | A40 | 99 | LED_LINK100 | O, mA | <p>Parallel LED output for 100BASE-TX link or speed. This active low LED pin may be programmed in direct drive or combined LED modes by programming register LED_LINK Control register 24.4:3.</p> <p>In direct drive LED mode, this pin indicates 100 Mbps link up or down.</p> <p>In combined LED mode, the output from LED_LINK10, LED_LINK100, and LED_LINK1000 must be read together to determine link and speed status.</p> <p>LED_LINK100 is a multi-function pin used to configure the 88E1111 device at the de-assertion of hardware reset.</p> |



Table 10: LED Interface (Continued)

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|--------------------|------------------|-------------------|--------------|-------------|---|
| A9 | A39 | 98 | LED_LINK1000 | O, mA | <p>Parallel LED output for 1000BASE-T link/speed or link indicator. This active low LED pin may be programmed in direct drive or combined LED modes by programming register LED_LINK Control register 24.4:3.</p> <p>In direct drive LED mode, this pin indicates 1000 Mbps link up or down.</p> <p>In combined LED mode, the output from LED_LINK1000 indicates link status.</p> <p>LED_LINK1000 is a multi-function pin used to configure the 88E1111 device at the de-assertion of hardware reset.</p> |
| E8 | B33 | 95 | LED_DUPLEX | O, mA | <p>Parallel LED duplex or duplex/collision modes. The LED_DUPLEX pin may be programmed to Mode 1 or Mode 2 by setting register bit 24.2.</p> <p>Mode 1 Low = Full-duplex High = Half-duplex Blink = Collision</p> <p>Mode 2 Low = Full-duplex High = Half-duplex</p> <p>Mode 3 Low = Fiber Link up High = Fiber Link down</p> <p>LED_DUPLEX is a multi-function pin used to configure the 88E1111 device at the de-assertion of hardware reset.</p> |

Table 10: LED Interface (Continued)

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|----------------------------|--------------------------|---------------------------|-----------------|-----------------|--|
| C9 | A37 | 92 | LED_RX | O, mA | <p>Parallel LED Receive Activity or Receive Activity/Link modes. LED_RX may be programmed to Mode 1 or Mode 2 by setting register bit 24.1.</p> <p>Mode 1 Low = Receiving High = Not receiving</p> <p>Mode 2 Low = Link up High = Link down Blink = Receiving</p> <p>LED_RX is a multi-function pin used to configure the 88E1111 device at the de-assertion of hardware reset.</p> |
| D9 | B32 | 91 | LED_TX | O, mA | <p>Parallel LED Transmit Activity or RX/TX Activity/Link modes. LED_TX may be programmed to Mode 1 or Mode 2 by setting register bit 24.0.</p> <p>Mode 1 Low = Transmitting High = Not transmitting</p> <p>Mode 2 Low = Link up High = Link down Blink = Transmitting or receiving</p> <p>LED_TX is a multi-function pin used to configure the 88E1111 device at the de-assertion of hardware reset.</p> |

Table 11: JTAG Interface

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Type | Pin Name | Description |
|----------------------------|--------------------------|---------------------------|-----------------|-----------------|---|
| L7 | B21 | 67 | TDI | I, PU | Boundary scan test data input. TDI contains an internal 150 kohm pull-up resistor. |
| L8 | B22 | 69 | TMS | I, PU | Boundary scan test mode select input. TMS contains an internal 150 kohm pull-up resistor. |
| L9 | A26 | 70 | TCK | I, PU | Boundary scan test clock input. TCK contains an internal 150 kohm pull-up resistor. |
| M9 | A25 | 68 | TRSTn | I, PU | Boundary scan test reset input. Active low. TRSTn contains an internal 150 kohm pull-up resistor as per the 1149.1 specification. After power up, the JTAG state machine should be reset by applying a low signal on this pin, or by keeping TMS high and applying 5 TCK pulses, or by pulling this pin low by a 4.7 kohm resistor. |
| K8 | A27 | 72 | TDO | O, Z | Boundary scan test data output. |

Table 12: Clock/Configuration/Reset/I/O

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|--------------------|------------------|-------------------|-----------|----------|---|
| K2 | B11 | 31 | 125CLK | O | Clock 125. A generic 125 MHz clock reference generated for use on the MAC device. This output can be disabled via DIS_125 through the CONFIG[3] pin. |
| D8 | A35 | 88 | CONFIG[0] | I | <p>CONFIG[0] pin configures PHY_ADR[2:0] bits of the physical address.</p> <p>Each LED pin is hardwired to a constant value. The values associated to the CONFIG[0] pin are latched at the de-assertion of hardware reset.</p> <p>CONFIG[0] pin must be tied to one of the pins based on the configuration options selected. They should not be left floating.</p> <p>For the Two-Wire Serial Interface (TWSI) device address, the lower 5 bits, which are PHYADR[4:0], are latched during hardware reset, and the device address bits [6:5] are fixed at '10'.</p> |
| E9 | B30 | 87 | CONFIG[1] | I | <p>CONFIG[1] pin configures PHY_ADR[4:3] and ENA_PAUSE options.</p> <p>Each LED pin is hardwired to a constant value. The values associated to the CONFIG[1] pin are latched at the de-assertion of hardware reset.</p> <p>CONFIG[1] pin must be tied to one of the pins based on the configuration options selected. They should not be left floating.</p> <p>For the TWSI device address, the lower 5 bits, which are PHYADR[4:0], are latched during hardware reset, and the device address bits [6:5] are fixed at '10'.</p> |

Table 12: Clock/Configuration/Reset/I/O (Continued)

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|--------------------|------------------|-------------------|-----------|----------|---|
| F8 | A34 | 86 | CONFIG[2] | I | <p>CONFIG[2] pin configures ANEG[3:1] bits.</p> <p>Each LED pin is hardwired to a constant value. The values associated to the CONFIG[2] pin are latched at the de-assertion of hardware reset.</p> <p>CONFIG[2] pin must be tied to one of the pins based on the configuration options selected. They should not be left floating.</p> |
| G7 | A33 | 82 | CONFIG[3] | I | <p>CONFIG[3] pin configures ANEG[0], ENA_XC, and DIS_125 options.</p> <p>Each LED pin is hardwired to a constant value. The values associated to the CONFIG[3] pin are latched at the de-assertion of hardware reset.</p> <p>CONFIG[3] pin must be tied to one of the pins based on the configuration options selected. They should not be left floating.</p> |
| F9 | B28 | 81 | CONFIG[4] | I | CONFIG[4] pin configures HWCFG_MODE[2:0] options. |
| G9 | A32 | 80 | CONFIG[5] | I | CONFIG[5] pin configures DIS_FC, DIS_SLEEP, and HWCFG_MODE[3] options. |
| G8 | B27 | 79 | CONFIG[6] | I | CONFIG[6] pin configures SEL_TWSI, INT_POL, and 75/50 OHM options. |
| H8 | B26 | 77 | SEL_FREQ | | <p>Frequency Selection for XTAL1 input</p> <p>NC = Selects 25 MHz clock input.</p> <p>Tied low = Selects 125 MHz clock input.</p> <p>Internally divided to 25 MHz.</p> <p>SEL_FREQ is internally pulled up.</p> |
| H9 | A30 | 76 | XTAL1 | I | Reference Clock. 25 MHz \pm 50 ppm or 125 MHz \pm 50 ppm oscillator input. PLL clocks are not recommended. |
| J9 | B25 | 75 | XTAL2 | 0 | <p>Reference Clock. 25 MHz \pm 50 ppm tolerance crystal reference. When the XTAL2 pin is not connected, it should be left floating.</p> <p>There is no option for a 125 MHz crystal.</p> <p>See "Crystal Oscillator" Application Note for details.</p> |

Table 12: Clock/Configuration/Reset/I/O (Continued)

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|----------------------------|--------------------------|---------------------------|-----------------|-----------------|--|
| K3 | B13 | 36 | RESETn | I | Hardware reset. Active low. XTAL1 must be active for a minimum of 10 clock cycles before the rising edge of RESETn. RESETn must be pulled high for normal operation. |
| L4 | A15 | 37 | COMA | I | <p>COMA disables all active circuitry to draw absolute minimum power. The COMA power mode can be activated by asserting high on the COMA pin. To deactivate the COMA power mode, tie the COMA pin low. Upon deactivating COMA mode, the 88E1111 device will continue normal operation.</p> <p>The COMA power mode cannot be enabled as long as hardware reset is enabled.</p> <p>In COMA mode, the PHY cannot wake up on its own by detecting activity on the CAT 5 cable.</p> |



Table 13: Test

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|--------------------|------------------|-------------------|------------------|--------------|--|
| M5 M6 | A20 B18 | 53 54 | HSDAC+ HSDAC- | Analog PD | Test pins. These pins should be left floating but brought out for probing. |

Table 14: Control and Reference

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|--------------------|------------------|-------------------|----------|-------------|--|
| M2 | B14 | 39 | RSET | Analog I | Constant voltage reference. External 5.0 kohm 1% resistor connection to VSS required for each pin. |

Table 15: Power & Ground

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|--|---|--|----------|----------|---|
| B7 M3 M4 M7 M8 N5 | B15 A19 B17 B19 A24 B36 | 44 49 52 59 64 104 | AVDD | Power | Analog Power. 2.5V. |
| C6 C7 D7 E3 E7 F3 J3 J7 | A1 B3 B5 A8 A31 B29 A36 A38 A46 | 2 6 12 17 23 27 78 85 90 96 117 118 | DVDD | Power | Digital Power. 1.0V (Instead of 1.0V, 1.2V can be used). |
| B9 F7 J8 | B24 B31 B34 | 73 89 97 | VDDOH | Power | 2.5V Power Supply for LED and CONFIG pins. |
| K9 L2 | B12 B23 | 34 71 | VDDOX | Power | 2.5V Supply for the MDC/MDIO, INTn, 125CLK, RESETn, JTAG pin Power. |
| B4 C2 K1 | A3 A11 B41 A52 | 5 11 30 122 | VDDO | Power | 2.5V I/O supply for the MAC interface pins. |

Table 15: Power & Ground (Continued)

| 117-TFBGA Pin # | 96-aQFN Pin # | 128-PQFP Pin # | Pin Name | Pin Type | Description |
|--|--------------------------|---|-----------------|-----------------|--|
| D4 D5 D6 E4 E5 E6 F4 F5 F6 G4 G5 G6 H4 H5 H6 J4 J5 J6 K4 K5 K6 L5 L6 | EPAD | 1 9 15 21 22 38 40 43 45 48 51 55 58 60 63 65 66 83 84 93 94 101 102 103 106 108 111 116 119 127 | VSS | GND | Global ground |
| H7 | A29 | 74 | VSSC | GND | Ground reference for XTAL1 and XTAL2 pins. This pin must be connected to the ground. |
| G1 K7 | A7 A28 | 50 | NC | NC | No connect. Do not connect these pins to anything |

1.5 I/O State at Various Test or Reset Modes

| Pin(s) | Isolate | Loopback or Normal operation | Software Reset | Hardware Reset | Power Down | Coma | Power Down and Isolate |
|--|--|--|--|----------------|--|--|--|
| MDI[3:0]± | Active | Active | Tri-state | Tri-state | Tri-state | Tri-state | Tri-state |
| TX_CLK | Tri-state | Active | Reg. 16.3 state 0 = Low 1 = Active | Low | Reg. 16.3 state 0 = Low 1 = Active | Reg. 16.3 state 0 = Low 0 = Static but can be either high or low | Tri-state |
| RXD[0], RXD[2] | Tri-state | Active | High | High | High | High | Tri-state |
| RXD[7:3,1], RX_DV, RX_ER, CRS | Tri-state | Active | Low | Low | Low | Low | Tri-state |
| COL | Tri-state | TBI mode - input else -active | Tri-state | Tri-state | TBI mode - input else - low | TBI mode - input else - low | Tri-state |
| RX_CLK | Tri-state | Active | Reg. 16.3 state 0 = Low 1 = Active | Low | Reg. 16.3 state 0 = Low 1 = Active | Reg. 16.3 state 0 = Low 0 = Static but can be either high or low | Tri-state |
| S_CLK± S_OUT± | Active | Active | Tri-state | Tri-state | Reg. 16.3 state 0 = Tri-state 1 = Active | Tri-state | Active |
| MDIO | Active | Active | Active | Tri-state | Active | Tri-state | Active |
| INT | Active | Active | Tri-state | Tri-state | Tri-state | Tri-state | Tri-state |
| LED_*** | Active | Active | High | High | High | High | High |
| TDO | Tri-state | Tri-state | Tri-state | Tri-state | Tri-state | Active | Tri-state |
| 125CLK | Reg. 16.4 state 0 = Toggle 1 = Low | Reg. 16.4 state 0 = Toggle 1 = Low | Reg. 16.4 state 0 = Toggle 1 = Low | Toggle | Reg. 16.4 state 0 = Toggle 1 = Low | Reg. 16.3 state 0 = Static but can be either high or low 0 = Low | Reg. 16.4 state 0 = Toggle 1 = Low |

1.6 117-Pin TFBGA Pin Assignment List - Alphabetical by Signal Name

| Pin # | Pin Name | Pin # | Pin Name |
|-------|-------------|-------|--------------|
| K2 | 125CLK | A9 | LED_LINK1000 |
| B7 | AVDD | C9 | LED_RX |
| M3 | AVDD | D9 | LED_TX |
| M4 | AVDD | L3 | MDC |
| M7 | AVDD | N2 | MDI[0]- |
| M8 | AVDD | N1 | MDI[0]+ |
| N5 | AVDD | N4 | MDI[1]- |
| B6 | COL | N3 | MDI[1]+ |
| L4 | COMA | N7 | MDI[2]- |
| D8 | CONFIG[0] | N6 | MDI[2]+ |
| E9 | CONFIG[1] | N9 | MDI[3]- |
| F8 | CONFIG[2] | N8 | MDI[3]+ |
| G7 | CONFIG[3] | M1 | MDIO |
| F9 | CONFIG[4] | G1 | NC |
| G9 | CONFIG[5] | K7 | NC |
| G8 | CONFIG[6] | K3 | RESETn |
| B5 | CRS | M2 | RSET |
| C6 | DVDD | B2 | RXD0 |
| C7 | DVDD | D3 | RXD1 |
| D7 | DVDD | C3 | RXD2 |
| E3 | DVDD | B3 | RXD3 |
| E7 | DVDD | C4 | RXD4 |
| F3 | DVDD | A1 | RXD5 |
| J3 | DVDD | A2 | RXD6 |
| J7 | DVDD | C5 | RXD7 |
| E2 | GTX_CLK | C1 | RX_CLK |
| M6 | HSDAC- | B1 | RX_DV |
| M5 | HSDAC+ | D2 | RX_ER |
| L1 | INTn | A6 | S_CLK- |
| E8 | LED_DUPLEX | A5 | S_CLK+ |
| C8 | LED_LINK10 | A4 | S_IN- |
| B8 | LED_LINK100 | A3 | S_IN+ |

1.6 117-Pin TFBGA Pin Assignment List - Alphabetical by Signal Name (Continued)

| Pin # | Pin Name | Pin # | Pin Name |
|-------|----------|-------|----------|
| A8 | S_OUT- | D4 | VSS |
| A7 | S_OUT+ | D5 | VSS |
| H8 | SEL_FREQ | D6 | VSS |
| L9 | TCK | E4 | VSS |
| L7 | TDI | E5 | VSS |
| K8 | TDO | E6 | VSS |
| L8 | TMS | F4 | VSS |
| M9 | TRSTn | F5 | VSS |
| F1 | TXD0 | F6 | VSS |
| G2 | TXD1 | G4 | VSS |
| G3 | TXD2 | G5 | VSS |
| H2 | TXD3 | G6 | VSS |
| H1 | TXD4 | H4 | VSS |
| H3 | TXD5 | H5 | VSS |
| J1 | TXD6 | H6 | VSS |
| J2 | TXD7 | J4 | VSS |
| D1 | TX_CLK | J5 | VSS |
| E1 | TX_EN | J6 | VSS |
| F2 | TX_ER | K4 | VSS |
| B4 | VDDO | K5 | VSS |
| C2 | VDDO | K6 | VSS |
| K1 | VDDO | L5 | VSS |
| B9 | VDDOH | L6 | VSS |
| F7 | VDDOH | H7 | VSSC |
| J8 | VDDOH | H9 | XTAL1 |
| K9 | VDDOX | J9 | XTAL2 |
| L2 | VDDOX | | |

1.7 96-Pin aQFN Pin Assignment List - Alphabetical by Signal Name

NOTE: The 96-pin BCC package is obsolete and is no longer available. The 96-Pin aQFN package is a pin compatible replacement for the 96-Pin BCC package.

| 96- Pin BCC Pin # | 96- Pin aQFN Pin # | Pin Name | 96- Pin BCC Pin # | 96- Pin aQFN Pin # | Pin Name |
|----------------------|-----------------------|------------|----------------------|-----------------------|--------------|
| 22 | B11 | 125CLK | 74 | A40 | LED_LINK100 |
| 32 | B15 | AVDD | 73 | A39 | LED_LINK1000 |
| 35 | A19 | AVDD | 69 | A37 | LED_RX |
| 36 | B17 | AVDD | 68 | B32 | LED_TX |
| 40 | B19 | AVDD | 25 | A14 | MDC |
| 45 | A24 | AVDD | 31 | A17 | MDI[0]- |
| 78 | B36 | AVDD | 29 | A16 | MDI[0]+ |
| 83 | A45 | COL | 34 | B16 | MDI[1]- |
| 27 | A15 | COMA | 33 | A18 | MDI[1]+ |
| 65 | A35 | CONFIG[0] | 41 | A22 | MDI[2]- |
| 64 | B30 | CONFIG[1] | 39 | A21 | MDI[2]+ |
| 63 | A34 | CONFIG[2] | 43 | A23 | MDI[3]- |
| 61 | A33 | CONFIG[3] | 42 | B20 | MDI[3]+ |
| 60 | B28 | CONFIG[4] | 24 | A13 | MDIO |
| 59 | A32 | CONFIG[5] | 13 | A7 | NC |
| 58 | B27 | CONFIG[6] | 51 | A28 | NC |
| 84 | B39 | CRS | 28 | B13 | RESETn |
| 1 | A1 | DVDD | 30 | B14 | RSET |
| 6 | B3 | DVDD | 95 | A51 | RXD0 |
| 10 | B5 | DVDD | 92 | B43 | RXD1 |
| 15 | A8 | DVDD | 93 | A50 | RXD2 |
| 57 | A31 | DVDD | 91 | A49 | RXD3 |
| 62 | B29 | DVDD | 90 | B42 | RXD4 |
| 67 | A36 | DVDD | 89 | A48 | RXD5 |
| 71 | A38 | DVDD | 87 | A47 | RXD6 |
| 85 | A46 | DVDD | 86 | B40 | RXD7 |
| 8 | B4 | GTX_CLK | 2 | B1 | RX_CLK |
| 38 | B18 | HSDAC- | 94 | B44 | RX_DV |
| 37 | A20 | HSDAC+ | 3 | A2 | RX_ER |
| 23 | A12 | INTn | 80 | B37 | S_CLK- |
| 70 | B33 | LED_DUPLEX | 79 | A43 | S_CLK+ |
| 76 | B35 | LED_LINK10 | 81 | A44 | S_IN- |

1.7 96-Pin aQFN Pin Assignment List - Alphabetical by Signal Name (Continued)

NOTE: The 96-pin BCC package is obsolete and is no longer available. The 96-Pin aQFN package is a pin compatible replacement for the 96-Pin BCC package.

| 96- Pin BCC Pin # | 96- Pin aQFN Pin # | Pin Name | 96- Pin BCC Pin # | 96- Pin aQFN Pin # | Pin Name |
|----------------------|-----------------------|----------|----------------------|-----------------------|----------|
| 82 | B38 | S_IN+ | 4 | B2 | TX_CLK |
| 75 | A41 | S_OUT- | 9 | A5 | TX_EN |
| 77 | A42 | S_OUT+ | 7 | A4 | TX_ER |
| 56 | B26 | SEL_FREQ | 5 | A3 | VDDO |
| 49 | A26 | TCK | 21 | A11 | VDDO |
| 44 | B21 | TDI | 88 | B41 | VDDO |
| 50 | A27 | TDO | 96 | A52 | VDDO |
| 46 | B22 | TMS | 52 | B24 | VDDOH |
| 47 | A25 | TRSTn | 66 | B31 | VDDOH |
| 11 | A6 | TXD0 | 72 | B34 | VDDOH |
| 12 | B6 | TXD1 | 26 | B12 | VDDOX |
| 14 | B7 | TXD2 | 48 | B23 | VDDOX |
| 16 | B8 | TXD3 | EPAD | EPAD | VSS |
| 17 | A9 | TXD4 | 53 | A29 | VSSC |
| 18 | B9 | TXD5 | 55 | A30 | XTAL1 |
| 19 | A10 | TXD6 | 54 | B25 | XTAL2 |
| 20 | B10 | TXD7 | | | |

1.8 128-Pin PQFP Pin Assignment List - Alphabetical by Signal Name

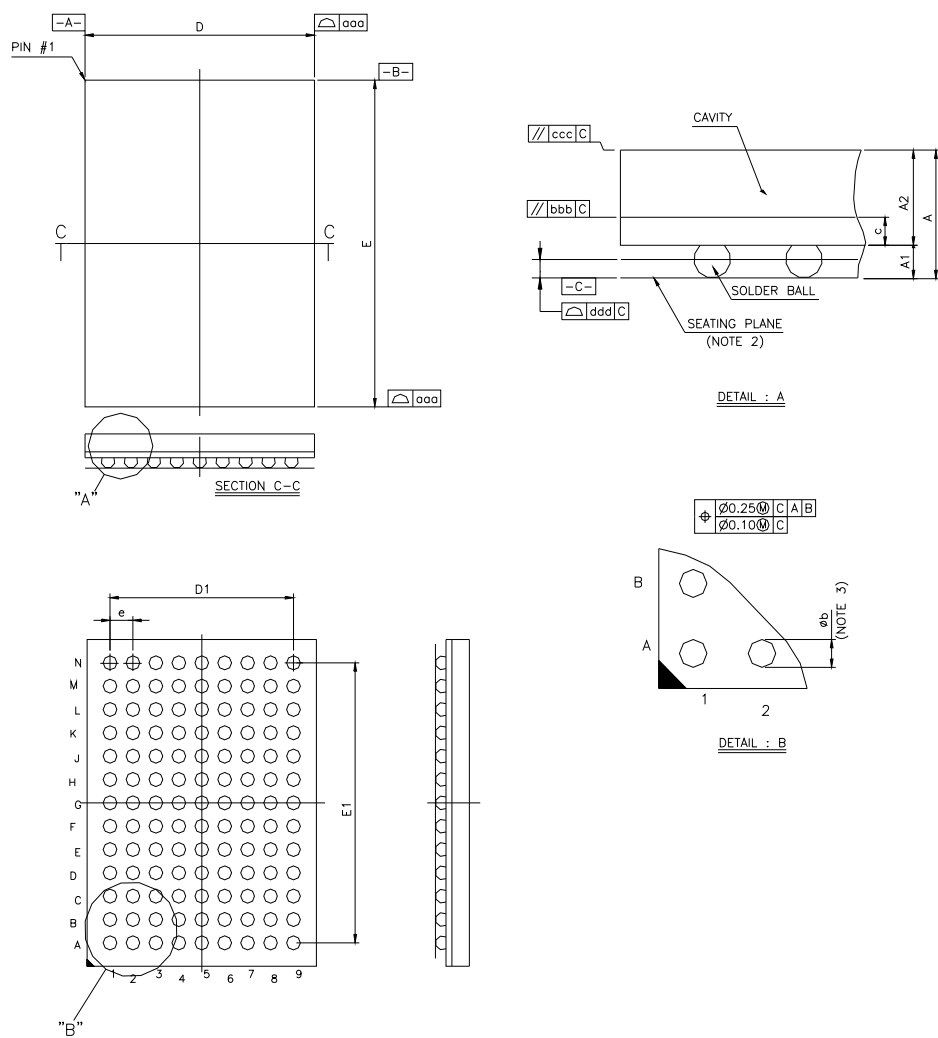
| Pin # | Pin Name | Pin # | Pin Name |
|-------|-----------|-------|--------------|
| 31 | 125CLK | 32 | INTn |
| 44 | AVDD | 95 | LED_DUPLEX |
| 49 | AVDD | 100 | LED_LINK10 |
| 52 | AVDD | 99 | LED_LINK100 |
| 59 | AVDD | 98 | LED_LINK1000 |
| 64 | AVDD | 92 | LED_RX |
| 104 | AVDD | 91 | LED_TX |
| 114 | COL | 35 | MDC |
| 37 | COMA | 41 | MDI[0]+ |
| 88 | CONFIG[0] | 42 | MDI[0]- |
| 87 | CONFIG[1] | 46 | MDI[1]+ |
| 86 | CONFIG[2] | 47 | MDI[1]- |
| 82 | CONFIG[3] | 56 | MDI[2]+ |
| 81 | CONFIG[4] | 57 | MDI[2]- |
| 80 | CONFIG[5] | 61 | MDI[3]+ |
| 79 | CONFIG[6] | 62 | MDI[3]- |
| 115 | CRS | 33 | MDIO |
| 2 | DVDD | 50 | NC |
| 6 | DVDD | 36 | RESETn |
| 12 | DVDD | 39 | RSET |
| 17 | DVDD | 7 | RX_CLK |
| 23 | DVDD | 4 | RX_DV |
| 27 | DVDD | 8 | RX_ER |
| 78 | DVDD | 3 | RXD0 |
| 85 | DVDD | 128 | RXD1 |
| 90 | DVDD | 126 | RXD2 |
| 96 | DVDD | 125 | RXD3 |
| 117 | DVDD | 124 | RXD4 |
| 118 | DVDD | 123 | RXD5 |
| 14 | GTX_CLK | 121 | RXD6 |
| 53 | HSDAC+ | 120 | RXD7 |
| 54 | HSDAC- | 110 | S_CLK+ |

1.8 128-Pin PQFP Pin Assignment List - Alphabetical by Signal Name (Continued)

| Pin # | Pin Name | Pin # | Pin Name |
|-------|----------|-------|----------|
| 109 | S_CLK- | 9 | VSS |
| 113 | S_IN+ | 15 | VSS |
| 112 | S_IN- | 21 | VSS |
| 107 | S_OUT+ | 22 | VSS |
| 105 | S_OUT- | 38 | VSS |
| 77 | SEL_FREQ | 40 | VSS |
| 70 | TCK | 43 | VSS |
| 67 | TDI | 45 | VSS |
| 72 | TDO | 48 | VSS |
| 69 | TMS | 51 | VSS |
| 68 | TRSTn | 55 | VSS |
| 10 | TX_CLK | 58 | VSS |
| 16 | TX_EN | 60 | VSS |
| 13 | TX_ER | 63 | VSS |
| 18 | TXD0 | 65 | VSS |
| 19 | TXD1 | 66 | VSS |
| 20 | TXD2 | 83 | VSS |
| 24 | TXD3 | 84 | VSS |
| 25 | TXD4 | 93 | VSS |
| 26 | TXD5 | 94 | VSS |
| 28 | TXD6 | 101 | VSS |
| 29 | TXD7 | 102 | VSS |
| 5 | VDDO | 103 | VSS |
| 11 | VDDO | 106 | VSS |
| 30 | VDDO | 108 | VSS |
| 122 | VDDO | 111 | VSS |
| 73 | VDDOH | 116 | VSS |
| 89 | VDDOH | 119 | VSS |
| 97 | VDDOH | 127 | VSS |
| 34 | VDDOX | 74 | VSSC |
| 71 | VDDOX | 76 | XTAL1 |
| 1 | VSS | 75 | XTAL2 |

Section 2. Package Mechanical Dimensions

2.1 117-pin TFBGA Package



(All dimensions in mm.)

Table 16: 117-Pin TFBGA Package Dimensions

| Dimensions in mm | | | |
|------------------|-------|-------|-------|
| Symbol | MIN | NOM | MAX |
| A | -- | -- | 1.54 |
| A1 | 0.40 | 0.50 | 0.60 |
| A2 | 0.84 | 0.89 | 0.94 |
| c | 0.32 | 0.36 | 0.40 |
| D | 9.90 | 10.00 | 10.10 |
| E | 13.90 | 14.00 | 14.10 |
| D1 | -- | 8.00 | -- |
| E1 | -- | 12.00 | -- |
| e | -- | 1.00 | -- |
| b | 0.50 | 0.60 | 0.70 |
| aaa | 0.20 | | |
| bbb | 0.25 | | |
| ccc | 0.35 | | |
| ddd | 0.15 | | |
| MD/ME | | | |

NOTE:

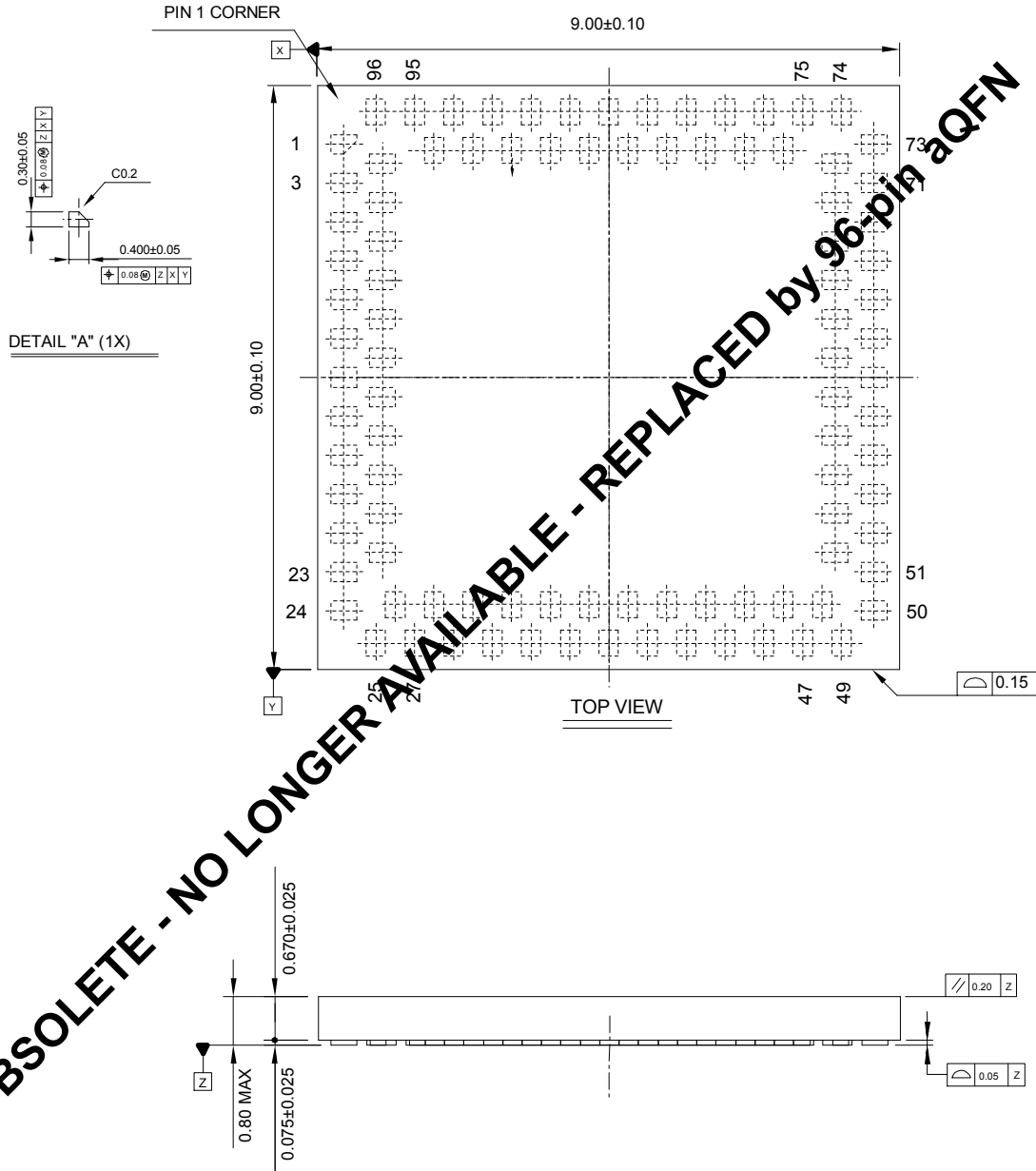
1. CONTROLLING DIMENSION: MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

2.2 96-pin BCC Package - Top View - OBSOLETE - No Longer Available - Replaced by the 96-Pin aQFN Package

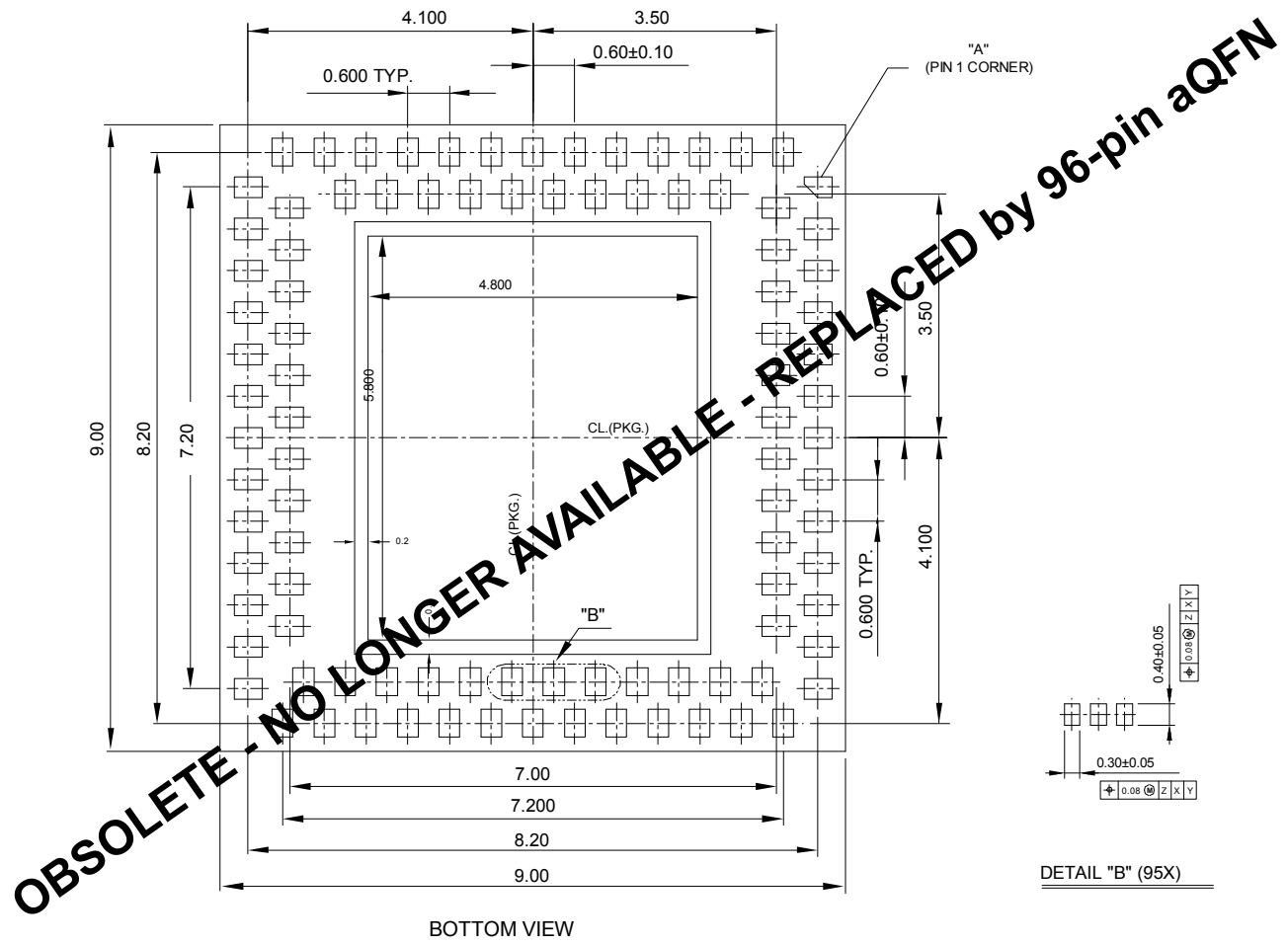


Note

The 96-Pin aQFN package is a pin compatible replacement for the 96-Pin BCC package. See Product Change Notification 1210066 and [Table 20](#) for details.



2.3 96-Pin BCC Package - Bottom View - OBSOLETE - No Longer Available - Replaced by the 96-Pin aQFN Package



2.4 96-pin aQFN Package - Top View

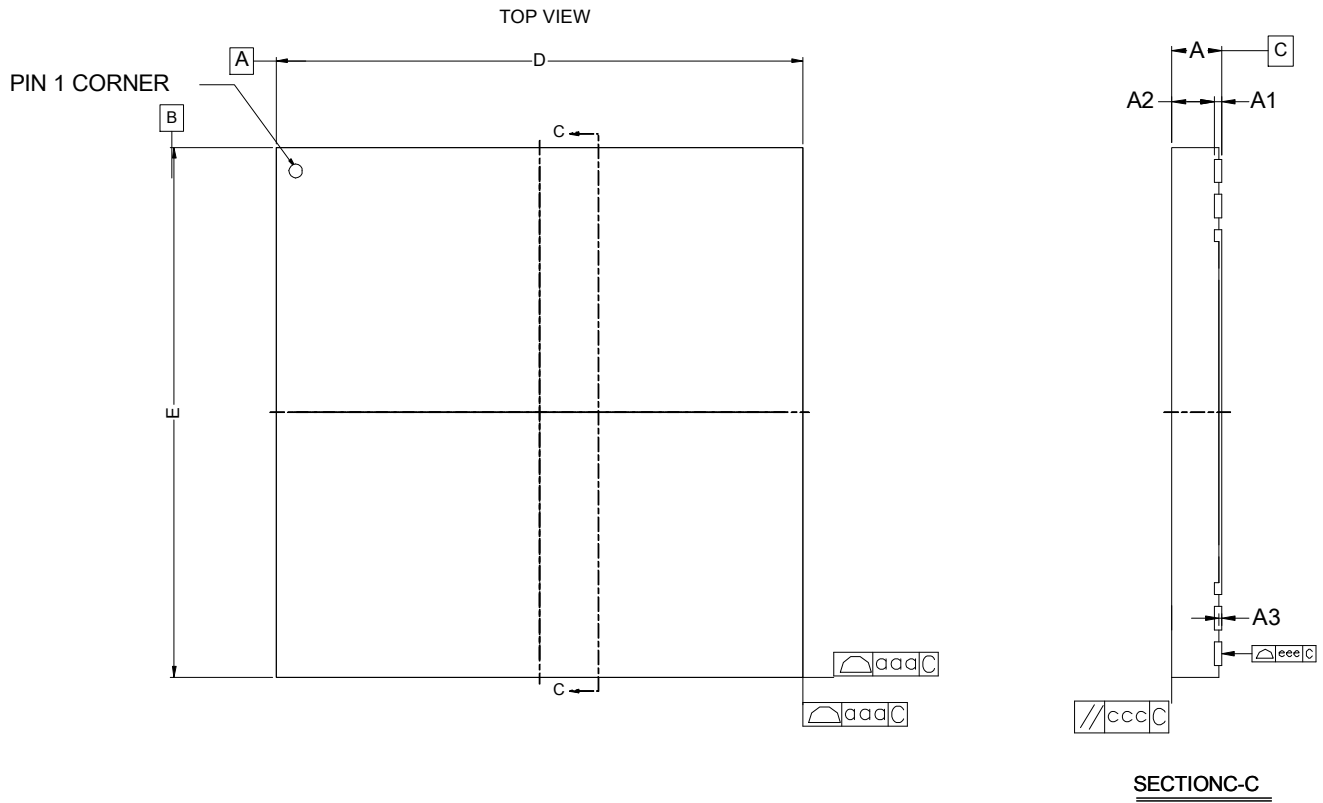
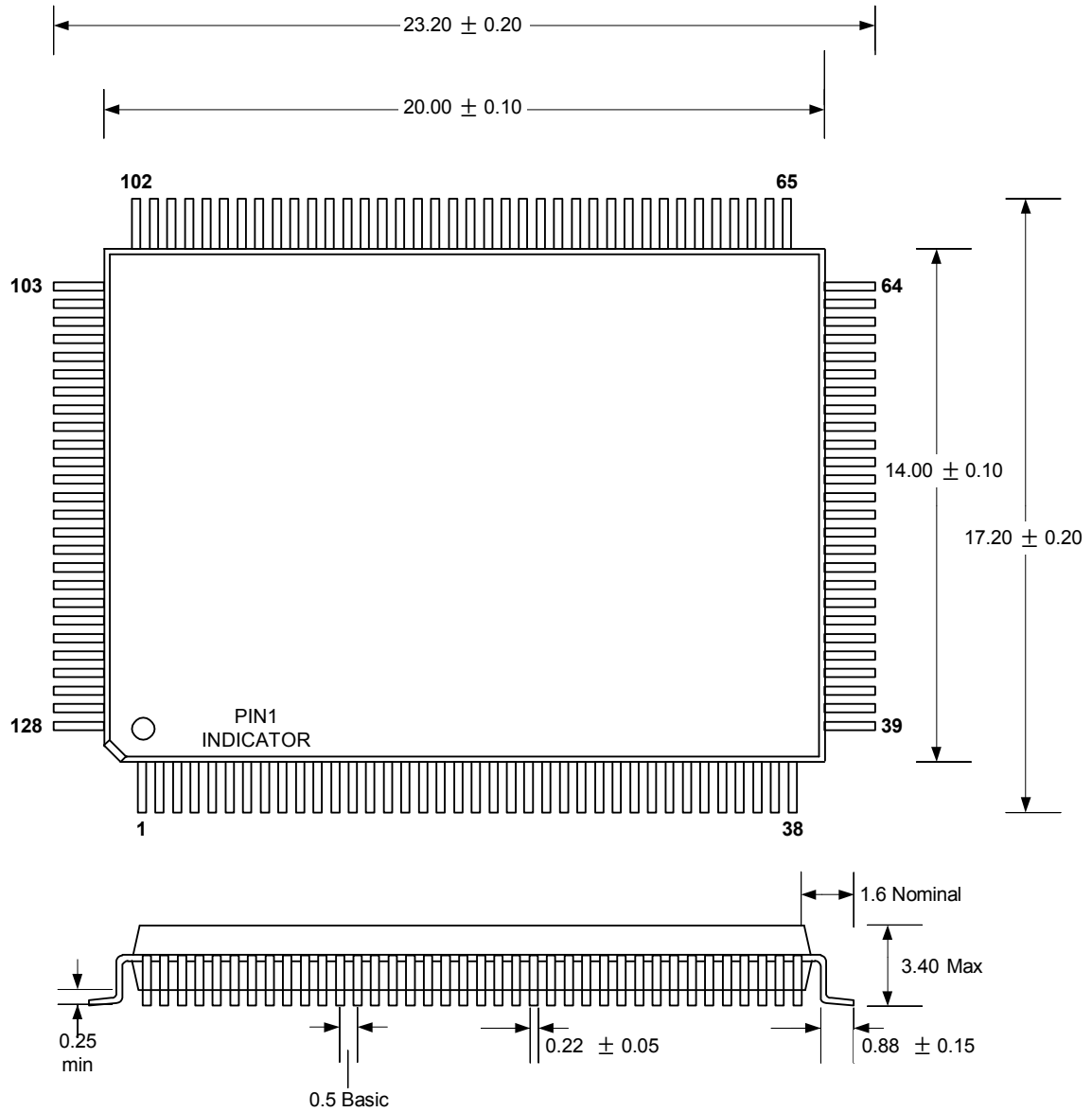


Table 17: 96-Pin aQFN Package Dimensions

| Controlling Dimension: MM | | | |
|--|------------|------------|------------|
| Symbol | MIN | NOM | MAX |
| A | -- | -- | 0.85 |
| A3 | 0.020 | 0.050 | 0.080 |
| A2 | 0.640 | 0.675 | 0.710 |
| A1 | 0.120 | 0.130 | 0.140 |
| b | 0.250 | 0.300 | 0.350 |
| b1 | 0.350 | 0.400 | 0.450 |
| D | 9.00 BSC | | |
| D2 | 4.700 | 4.800 | 4.900 |
| E | 9.00 BSC | | |
| E2 | 5.700 | 5.800 | 5.900 |
| eT | 0.600 | | |
| eR | 0.600 | | |
| K | 0.350 | 0.400 | 0.450 |
| K1 | 0.850 | 0.900 | 0.950 |
| L | 0.150 | 0.200 | 0.250 |
| Tolerances of Form and Position | | | |
| aaa | 0.150 | | |
| bbb | 0.100 | | |
| ddd | 0.050 | | |
| ccc | 0.080 | | |
| eee | 0.080 | | |
| fff | 0.100 | | |

2.6 128-Pin PQFP Package



Section 3. Order Information

3.1 Ordering Part Numbers and Package Markings

Figure 6 shows the ordering part numbering scheme for the 88E1111 devices. Contact Marvell® FAEs or sales representatives for complete ordering information.

Figure 6: Sample Part Number

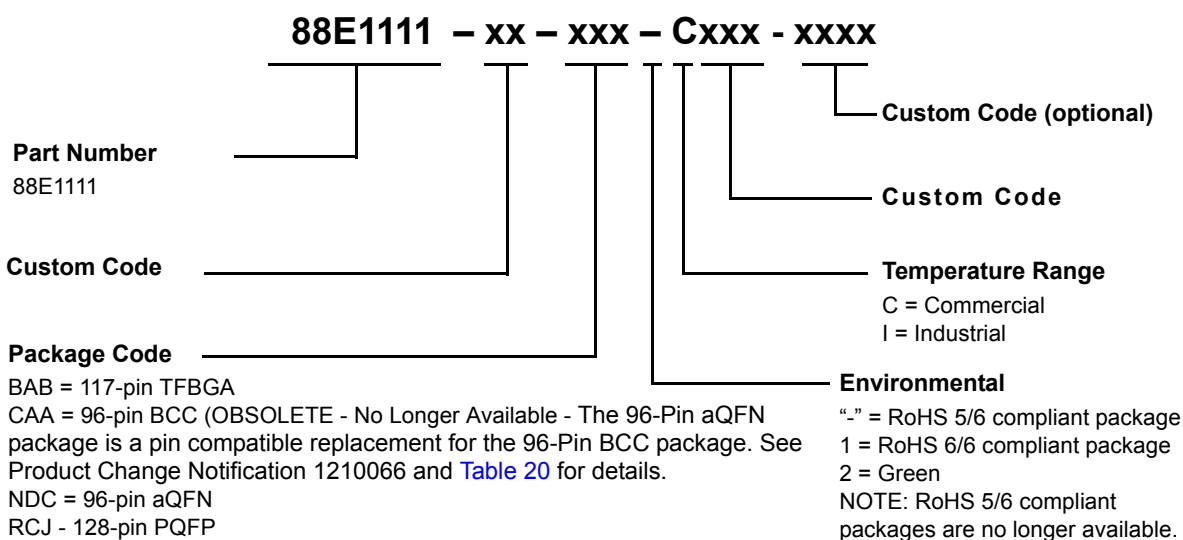


Table 18: 88E1111 Part Order Options - RoHS 6/6 Compliant Package

| Package Type | Part Order Number |
|--|---------------------|
| 88E1111 117-pin TFBGA - Commercial | 88E1111-XX-BAB1C000 |
| 88E1111 117-pin TFBGA - Industrial | 88E1111-XX-BAB1I000 |
| 88E1111 96-pin BCC - Commercial (OBSOLETE - no longer available - replaced by 96-pin aQFN) | 88E1111-XX-CAA1C000 |
| 88E1111 96-pin BCC - Industrial (OBSOLETE - no longer available - replaced by 96-pin aQFN) | 88E1111-XX-CAA1I000 |
| 88E1111 128-pin PQFP - Commercial | 88E1111-XX-RCJ1C000 |

Table 19: 88E1111 Part Order Options - Green Compliant Package

| Package Type | Part Order Number |
|--------------------------------|---------------------|
| 88E1111 96-pin aQFN Commercial | 88E1111-XX-NDC2C000 |
| 88E1111 96-pin aQFN Industrial | 88E1111-XX-NDC2I000 |

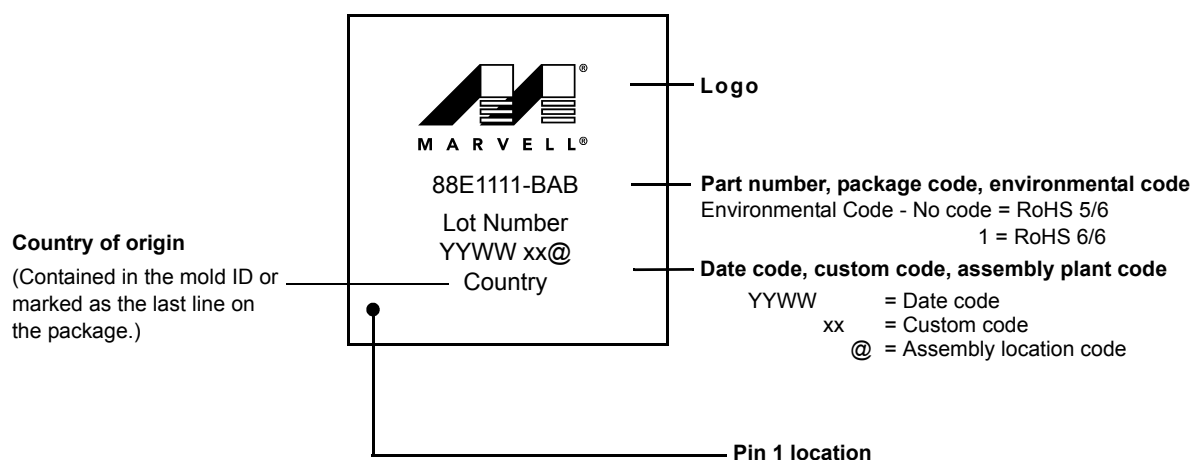
Table 20: 96-pin BCC Package Replacement Part Numbers

| Existing 96-pin BCC Package Part Number | Recommended 96-pin aQFN Package Replacement Part Number |
|---|---|
| 88E1111-B0-CAA-C000 | 88E1111-B0-NDC2C000 |
| 88E1111-B0-CAA1C000 | 88E1111-B0-NDC2C000 |
| 88E1111-B2-CAA-C000 | 88E1111-B2-NDC2C000 |
| 88E1111-B2-CAA-I000 | 88E1111-B2-NDC2I000 |
| 88E1111-B2-CAA1C000 | 88E1111-B2-NDC2C000 |
| 88E1111-B2-CAA1I000 | 88E1111-B2-NDC2I000 |

3.1.1 RoHS 5/6 Compliant Marking Examples

Figure 7 is an example of the package marking and pin 1 location for the 88E1111 117-pin TFBGA commercial RoHS 5/6 compliant package.

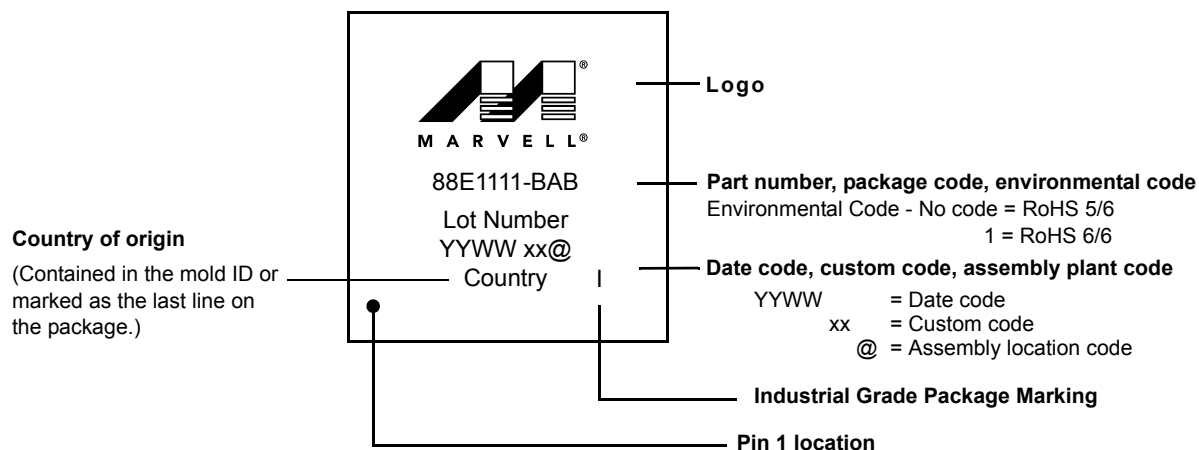
Figure 7: 88E1111 117-pin TFBGA Commercial RoHS 5/6 Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 8 is an example of the package marking and pin 1 location for the 88E1111 117-pin TFBGA Industrial RoHS 5/6 compliant package.

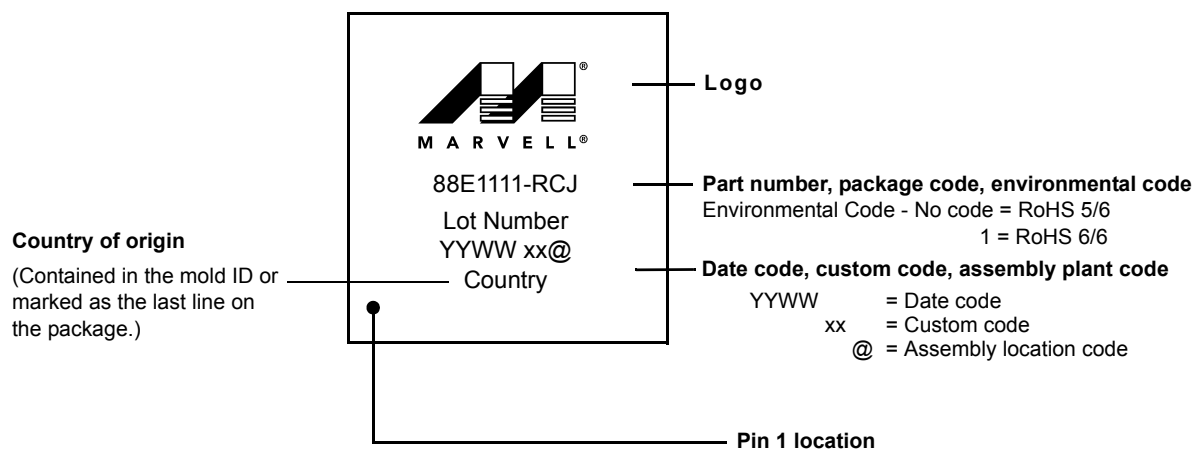
Figure 8: 88E1111 117-pin TFBGA Industrial RoHS 5/6 Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 9 is an example of the package marking and pin 1 location for the 88E1111 128-pin PQFP Commercial RoHS 5/6 compliant package.

Figure 9: 88E1111 128-pin PQFP Commercial RoHS 5/6 Compliant Package Marking and Pin 1 Location

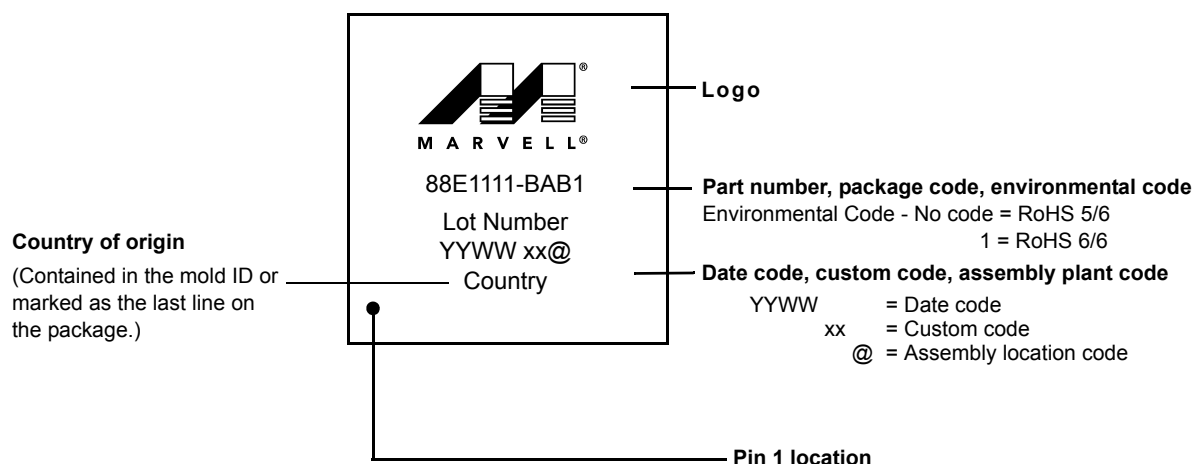


Note: The above example is not drawn to scale. Location of markings is approximate.

3.1.2 RoHS 6/6 Compliant Marking Examples

Figure 10 is an example of the package marking and pin 1 location for the 88E1111 117-pin TFBGA commercial RoHS 6/6 compliant package.

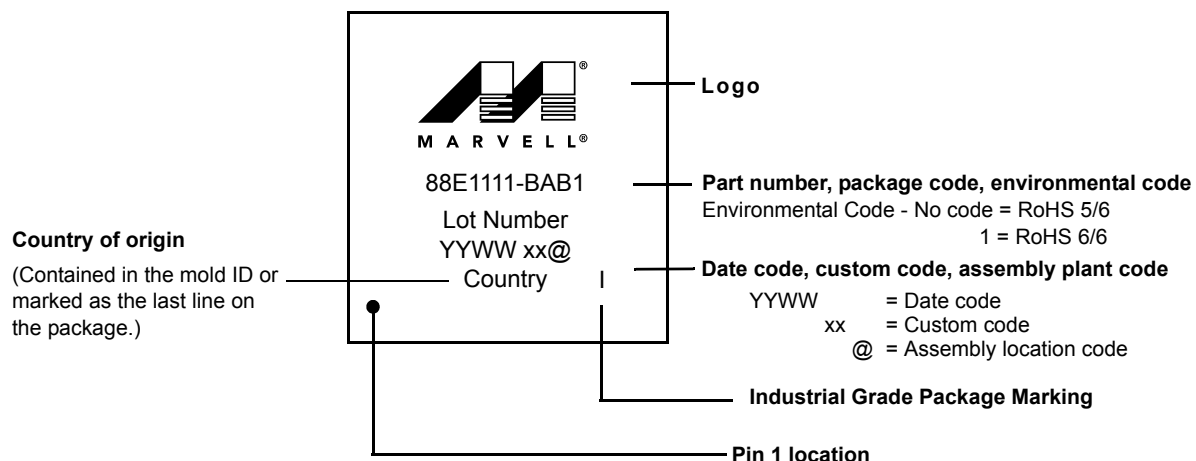
Figure 10: 88E1111 117-pin TFBGA Commercial RoHS 6/6 Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 11 is an example of the package marking and pin 1 location for the 88E1111 117-pin TFBGA industrial RoHS 6/6 compliant package.

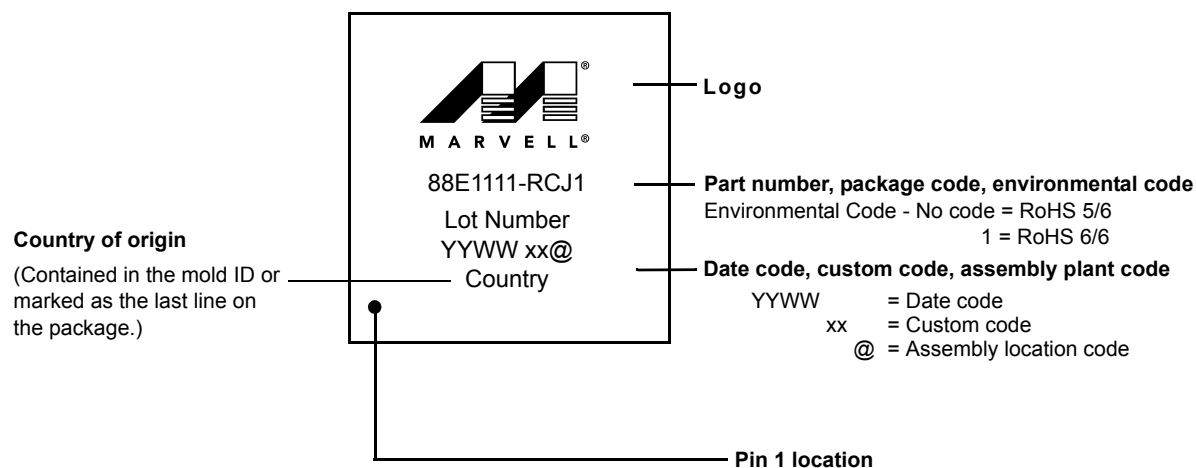
Figure 11: 88E1111 117-pin TFBGA Industrial RoHS 6/6 Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 12 is an example of the package marking and pin 1 location for the 88E1111 128-pin PQFP Commercial RoHS 6/6 compliant package.

Figure 12: 88E1111 128-pin PQFP Commercial RoHS 6/6 Compliant Package Marking and Pin 1 Location

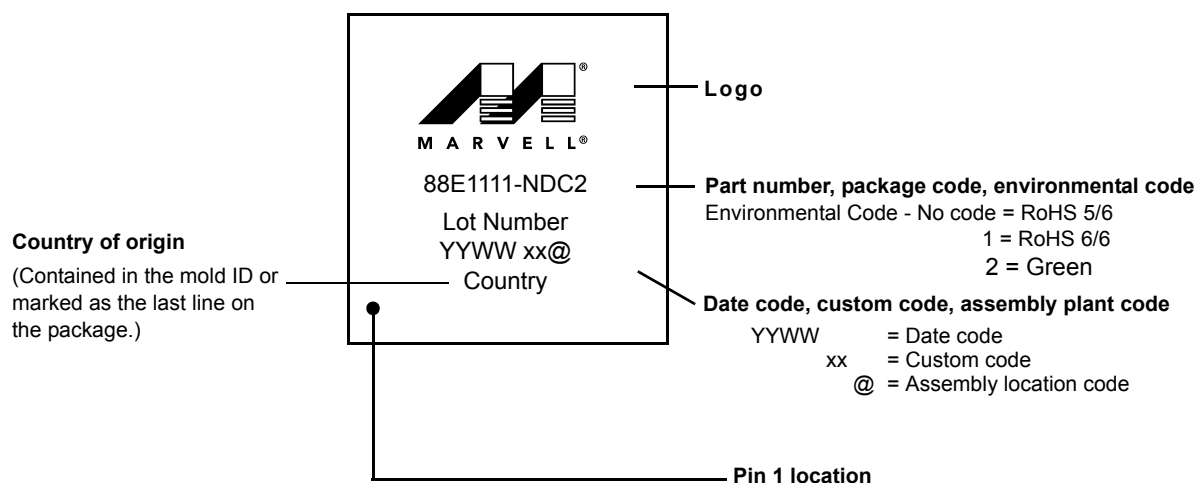


Note: The above example is not drawn to scale. Location of markings is approximate.

3.1.3 Green Compliant Marking Examples

Figure 13 is an example of the package marking and pin 1 location for the 88E1111 96-pin aQFN Commercial Green compliant package.

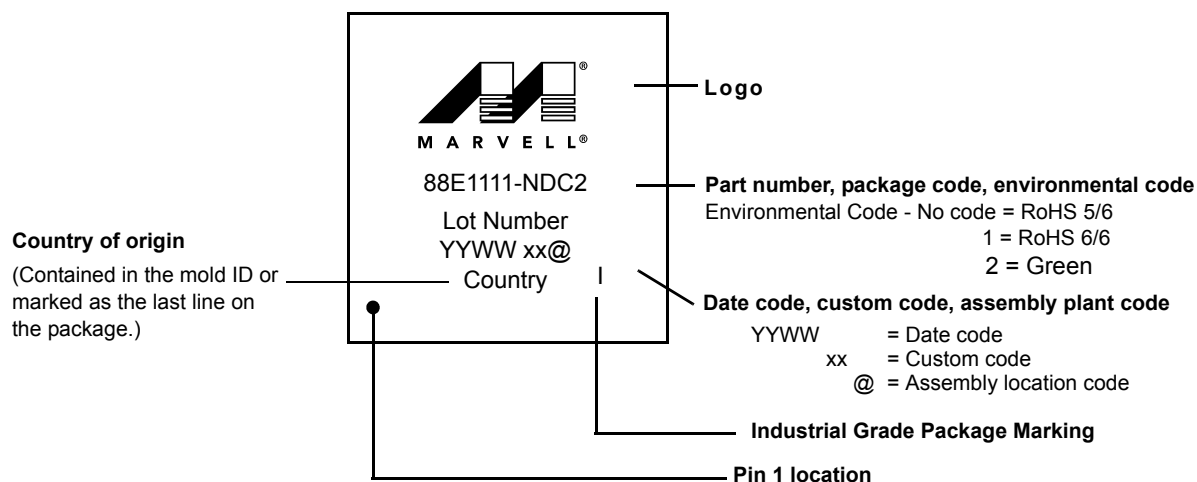
Figure 13: 88E1111 96-pin aQFN Commercial Green Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 14 is an example of the package marking and pin 1 location for the 88E1111 96-pin aQFN Industrial Green compliant package.

Figure 14: 88E1111 96-pin aQFN Industrial Green Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.



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