마이크로콘트롤러
(Micro-controller)

한양대학교 HANYANG UNIVERSITY

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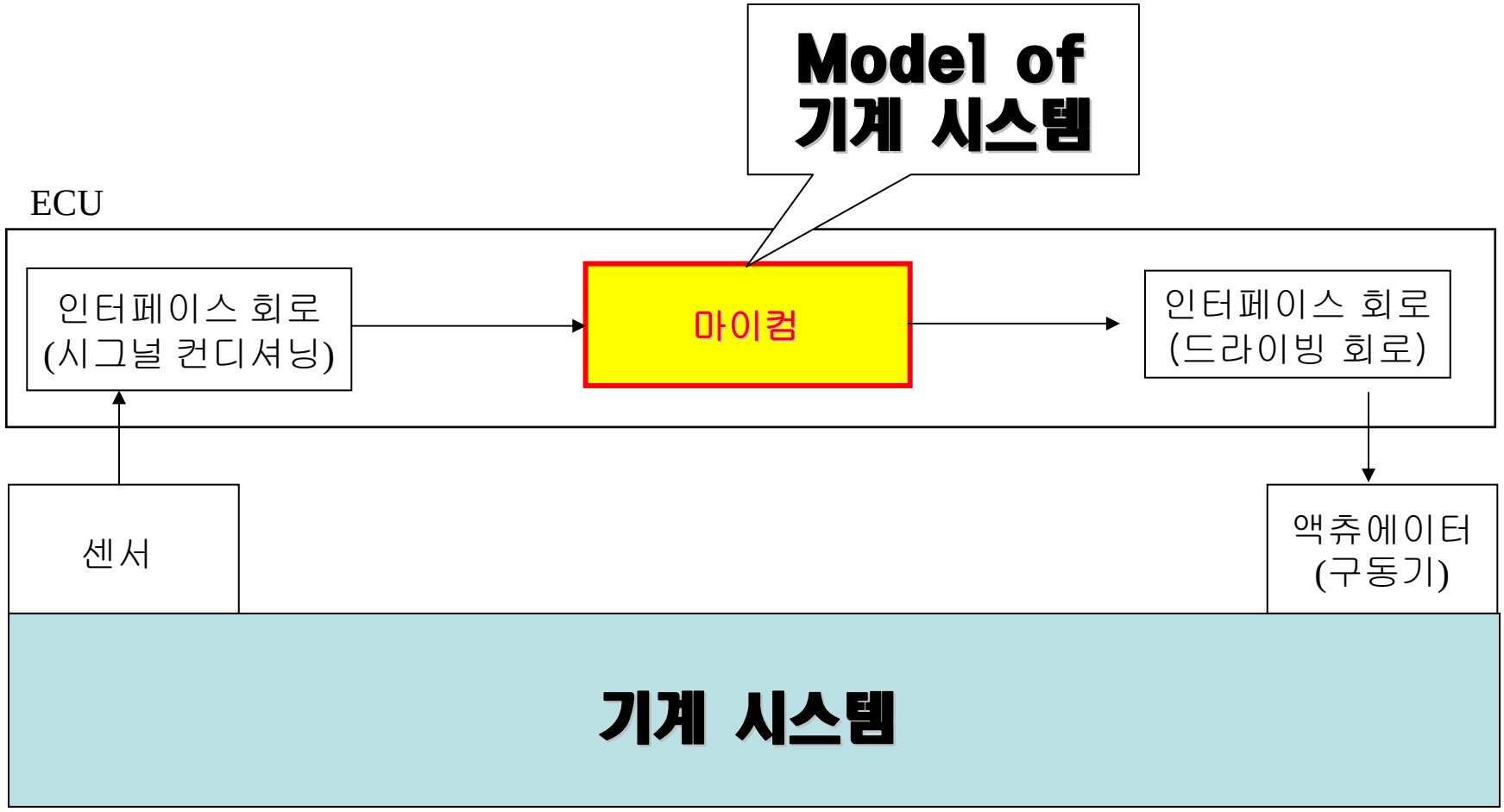
메카트로닉스 시스템의 구성



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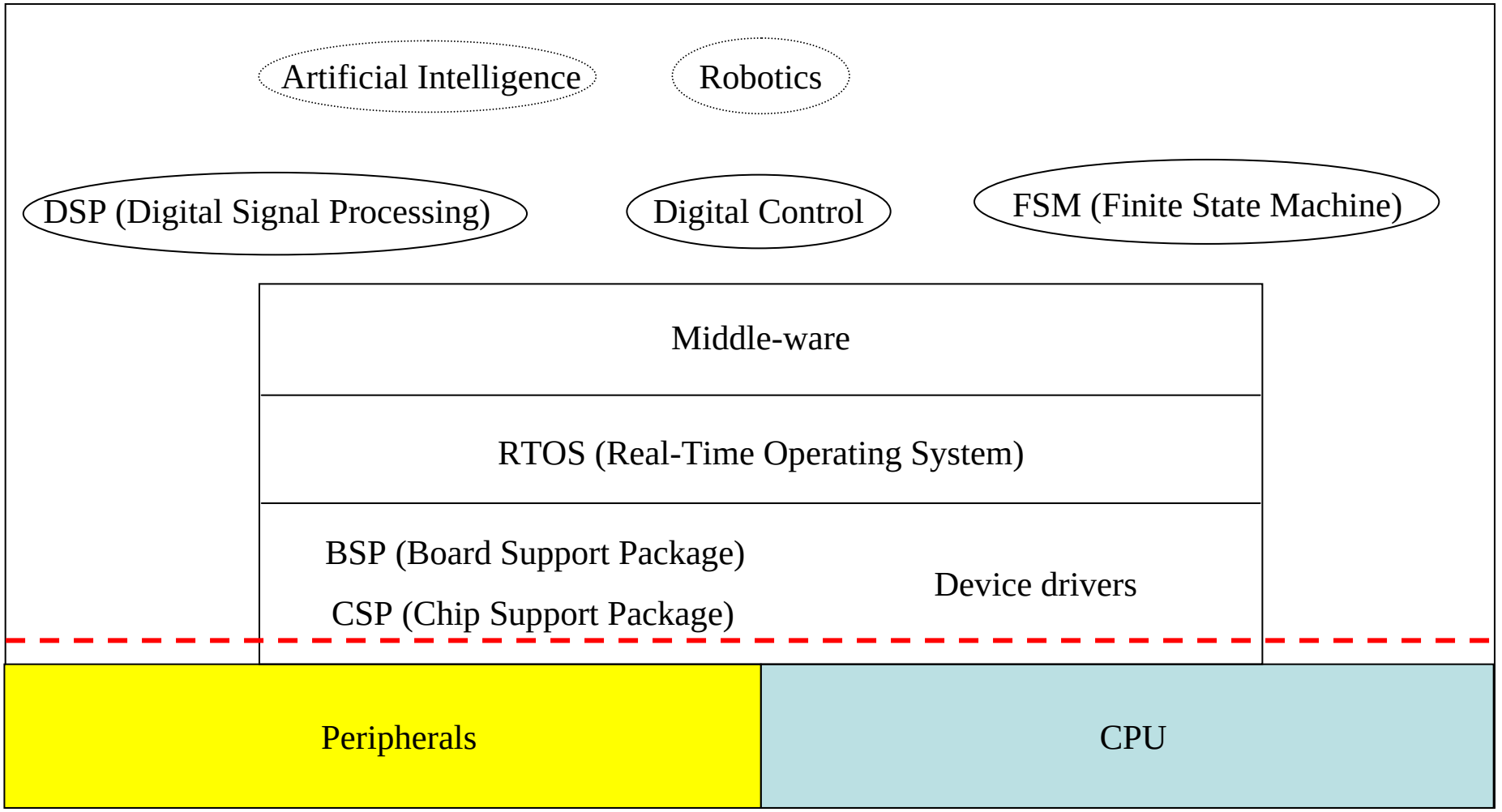
메카트로닉스 시스템의 구성

마이컴



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4.1. 디지털 신호 [1]

4.4.1. 이진수

2진 체계 (binary system): 두 개의 기호(또는 0과 1)로 상태를 표시하는 시스템

- 0과 1은 회로 상에서 0V와 5V 같은 **전압으로** 표시될 수 있다.
- 이 두 상태를 **2진 (binary digits)** 또는 **비트(bits)**라고 한다.
- 각 수의 위치는 가중치를 나타내는데, 우측에서 좌측으로 진행할 때 두 배씩 증가한다.

  $2^3\ 2^2\ 2^1\ 2^0$

  10진수 13 → $1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$ → 2진수 1101

- **워드(word)**: 어떤 수를 표현하기 위한 비트의 조합
- 가장 우측의 비트를 LSB(Least Significant Bit), 가장 좌측의 비트를 MSB(Most Significant Bit)

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5. 디지털 논리 [1]

5.2. 논리 게이트

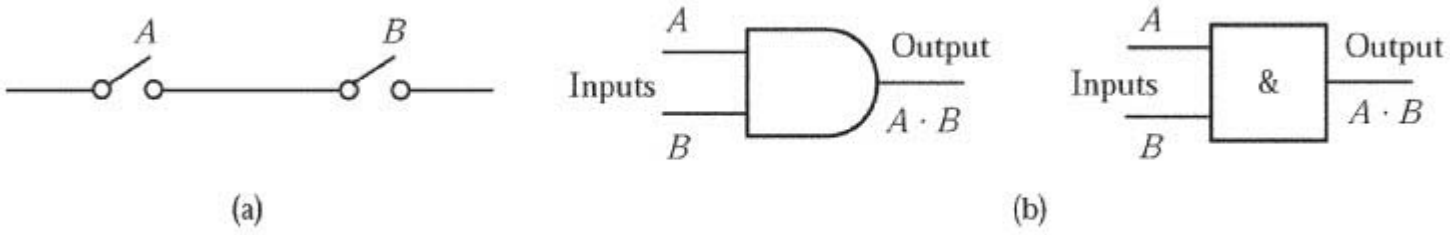

그림 5.1 AND 게이트 (a) 스위치로 표현하는 방식 (b) 표현기호

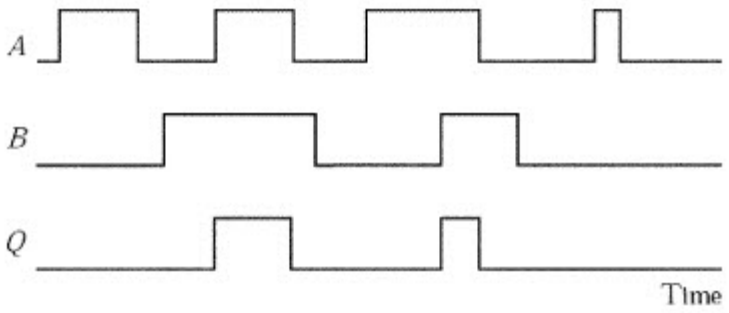

그림 5.2 AND 게이트

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5. 디지털 논리 [1]

5.2. 논리 게이트

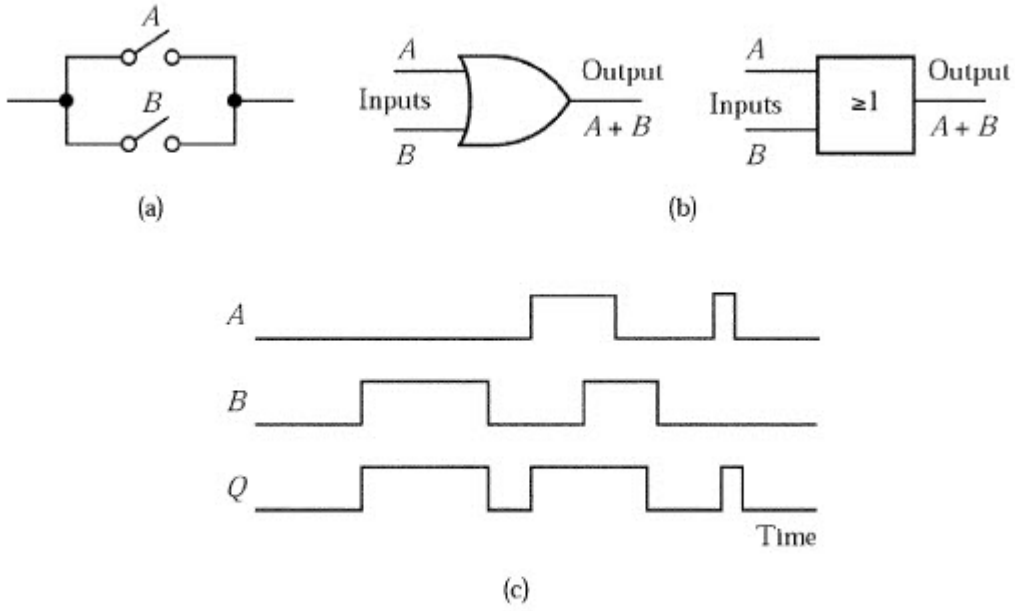

그림 5.3 OR 게이트 (a) 스위치로 표현하는 방식 (b) 표현기호 (c) 타이밍 도

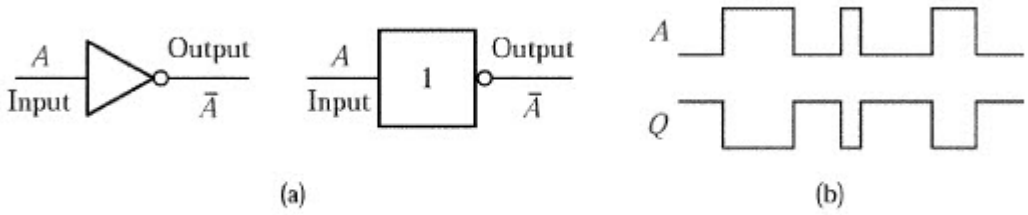

그림 5.4 NOT 게이트

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5. 디지털 논리 [1]

5.2. 논리 게이트

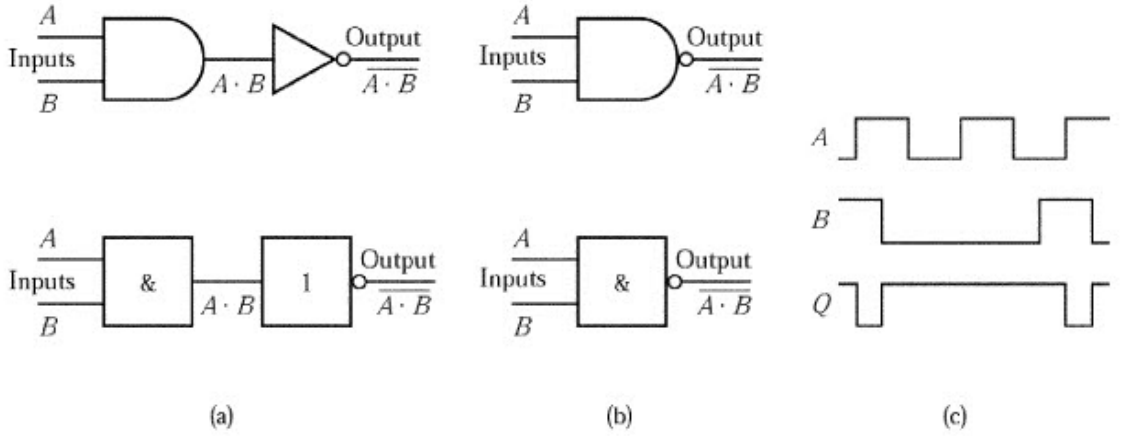

그림 5.5 NAND 게이트

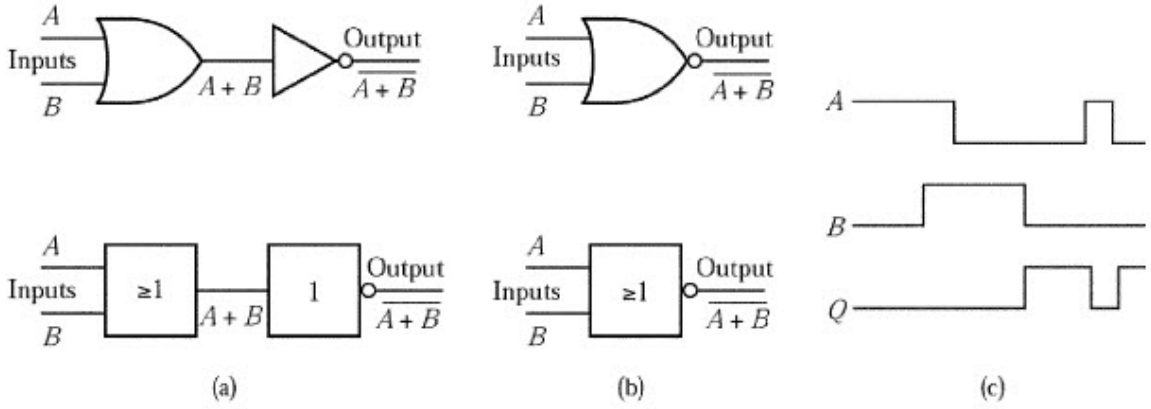

그림 5.6 NOR 게이트

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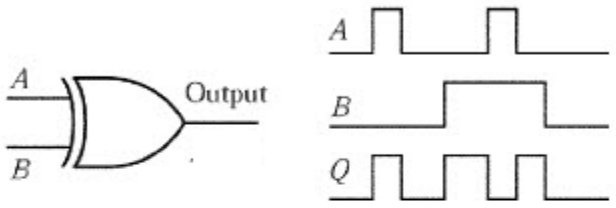
5. 디지털 논리 [1]

5.2. 논리 게이트



(b) (c)

그림 5.7 XOR 게이트

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5. 디지털 논리 [1]

5.3. 논리 게이트의 응용

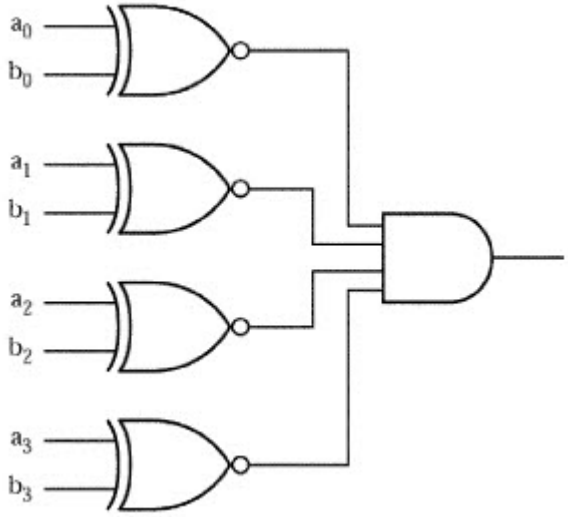

그림 5.12 비교기

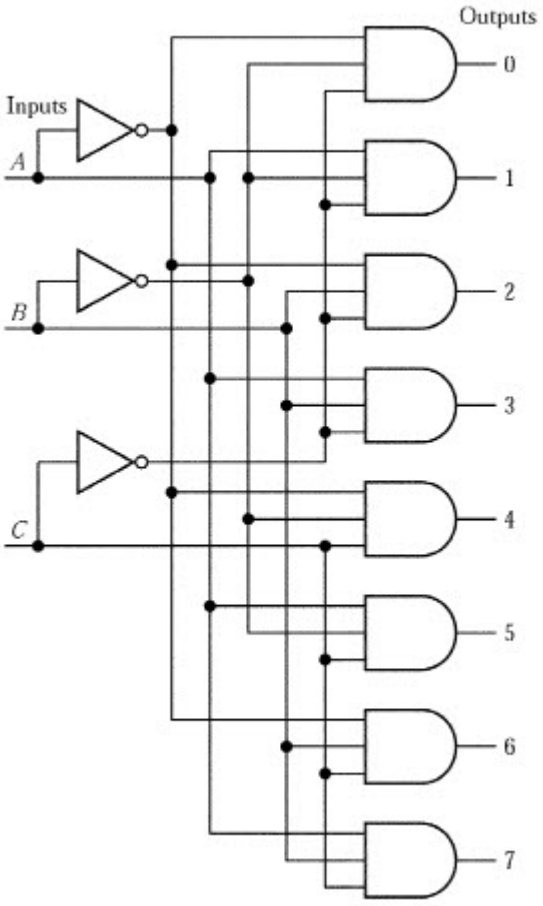

그림 5.16 3라인-8라인 디코더

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5. 디지털 논리 [1]

5.4. 순차 게이트

플립플롭(flip-flop): 논리 게이트의 조합으로 만들어진 기본적인 메모리 요소

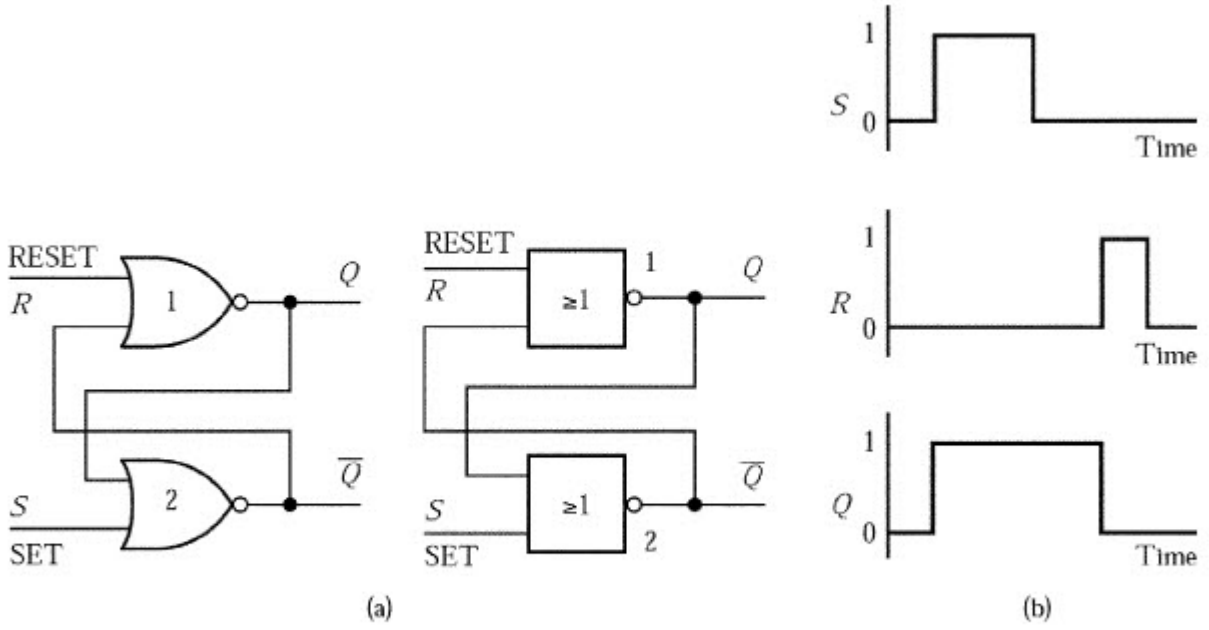

그림 5.20 SR 플립플롭

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5. 디지털 논리 [1]

5.4. 순차 게이트

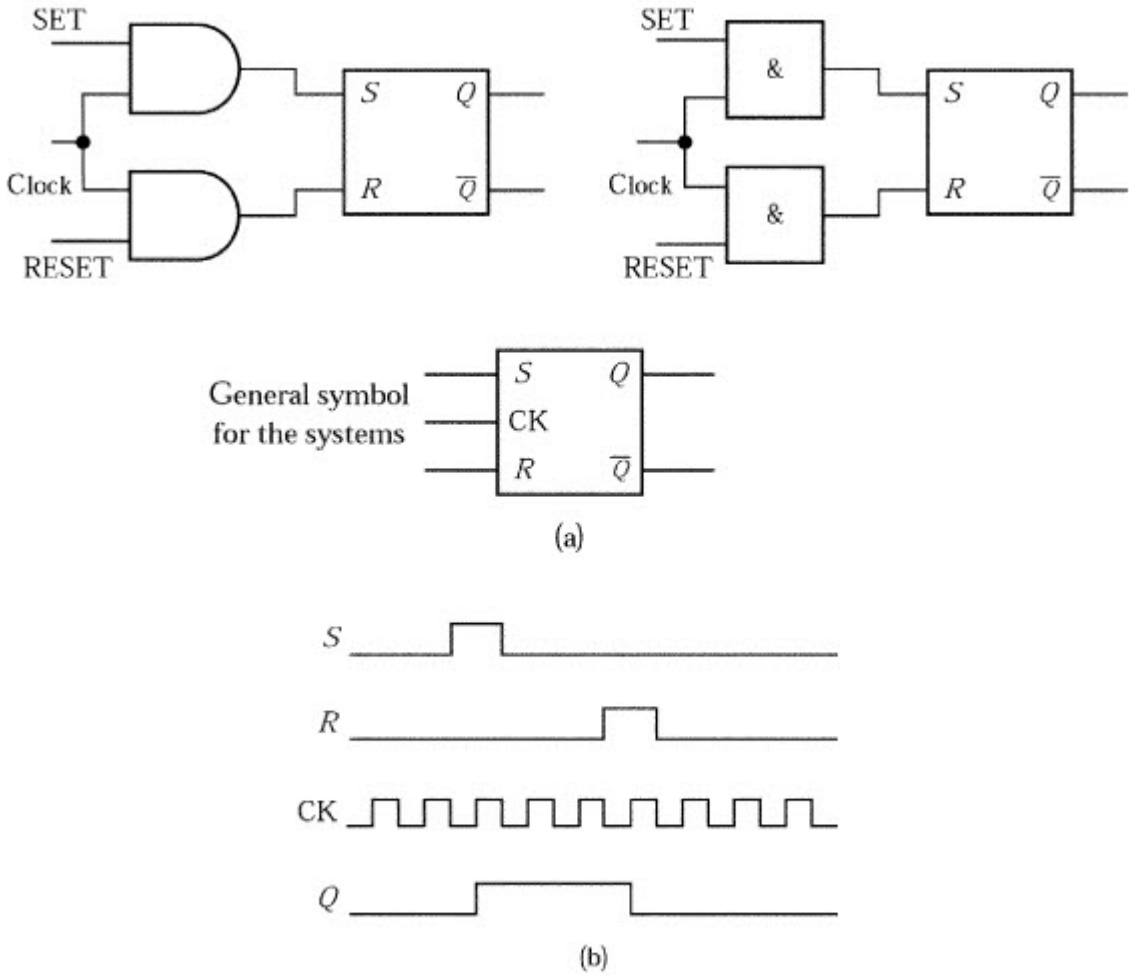

그림 5.23 클록 입력 SR 플립플롭

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5. 디지털 논리 [1]

5.4. 순차 게이트

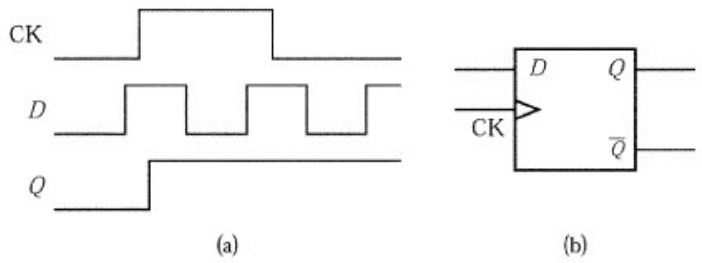

그림 5.26 (a) 양극 에지 – 트리거 (b) 에지 – 트리거 방식 D 플립플롭의 기호

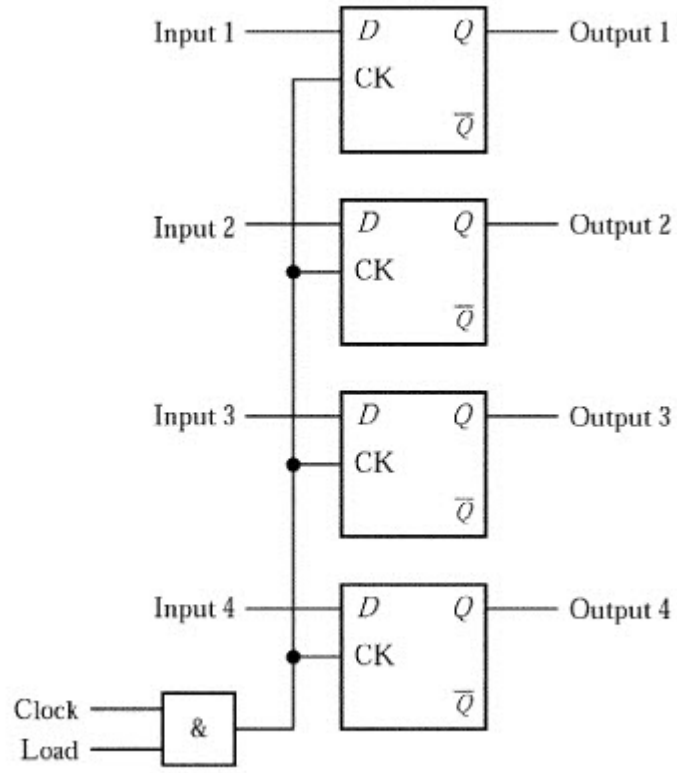

그림 5.28 레지스터

레지스터란 메모리 집합의 한 종류이고 정보가 필요할 때까지 유지하는 데 사용된다,

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17. 마이크로프로세서 시스템

마이크로프로세서를 사용하는 시스템은 기본적으로 다음과 같이 세 부분으로 구성된다.

1) 중앙 처리 장치 (Central Processing Unit, CPU): 프로그램을 인식하고 실행한다.

2) 입출력 인터페이스 (input and output interfaces): 컴퓨터와 외부 사이의 통신을 담당한다.

3) 기억 장치 (memory): 프로그램 명령이나 데이터를 저장한다.

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17. 마이크로프로세서 시스템

디지털 신호는 버스(buses)라고 부르는 통로를 따라 한쪽에서 다른 한쪽으로 이동한다.

데이터 버스, 주소 버스, 제어 버스

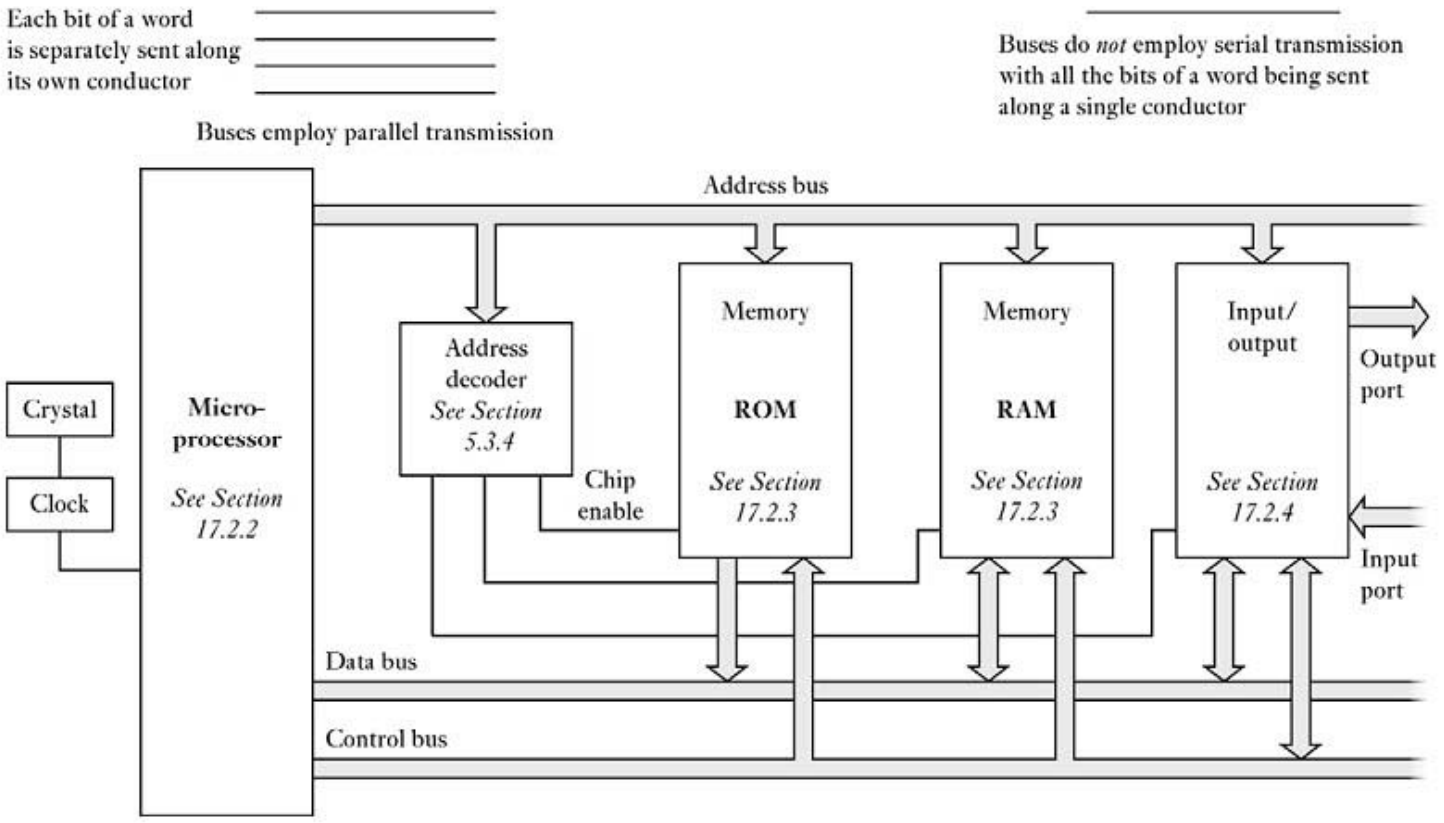

그림 17.1 마이크로 프로세서 시스템과 버스의 일반적인 형태

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17. 마이크로프로세서 시스템

17.2.2. 마이크로프로세서

마이크로프로세서는 일반적으로 중앙 처리 장치(Central Processing Unit, CPU)라고 한다. 이는 데이터를 처리하고 기억 장치로부터 명령어를 불러오고, 명령어를 복호화(decoding)하고 실행한다.

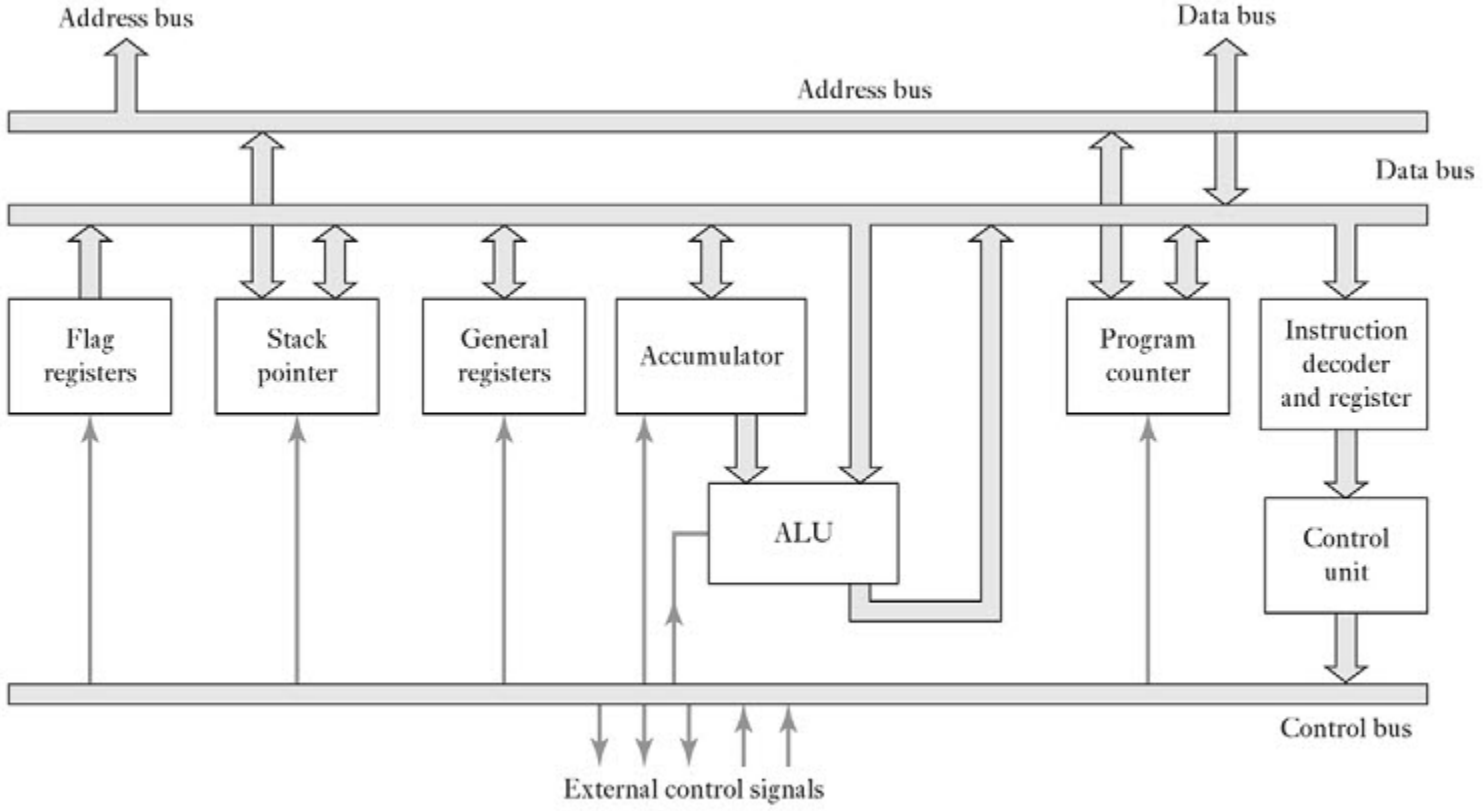

그림 17.2 마이크로 프로세서의 일반적인 내부 구조

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17. 마이크로프로세서 시스템

17.2.2. 마이크로프로세서

마이크로프로세서의 구성요소

1) 산술 논리 연산 장치 (Arithmetic and Logic Unit, ALU)

2) 제어 장치 (control unit): 마이크로프로세서 동작의 타이밍과 순서를 결정한다.

3) 레지스터 (register): CPU가 사용 중인 내부 데이터를 일시적으로 저장하는 장소.

- 누산기 레지스터 (accumulator register): ALU의 입력 또는 출력
- 상태 레지스터 (status register): ALU 최근 처리 결과에 관한 정보.
  각 비트를 플래그(flag)라 하고 고유의 의미를 갖는다.
  (Zero, Negative, Carry, oVerflow, Interruptible 등)
- 프로그램 계수기 레지스터 (program counter register, PC): CPU가 수행하고 있는 프로그램의 위치
- 기억 장치 주소 레지스터 (memory address register, MAR): 액세스할 메모리의 주소
- 명령어 레지스터 (instruction register, IR): 수행할 명령어 저장
- 범용 레지스터 (general purpose register)
- 스택 포이터 레지스터 (stack pointer register, SP): 스택 영역 맨 위쪽의 주소

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17. 마이크로프로세서 시스템

17.2.2. 마이크로프로세서

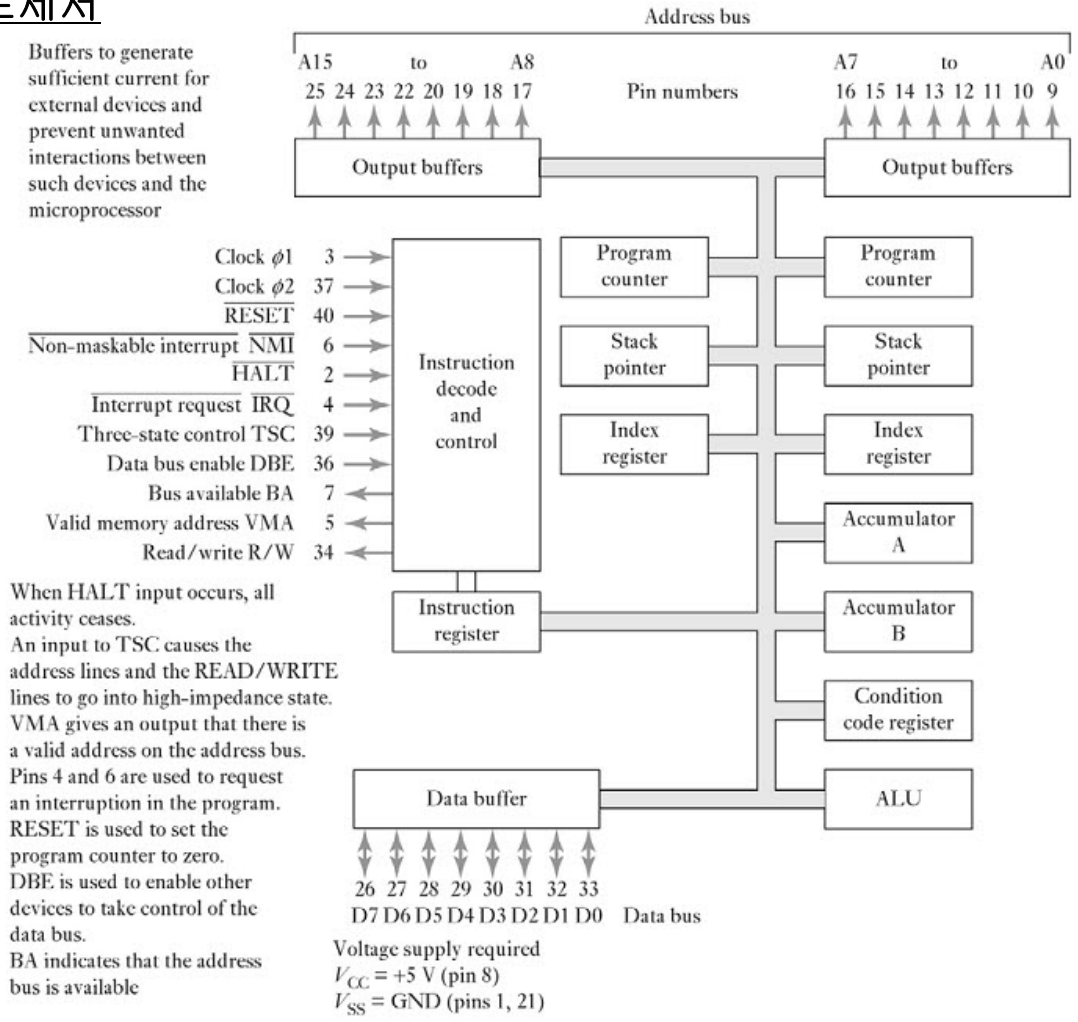

그림 17.3 Motorola 6800 구조

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17. 마이크로프로세서 시스템

17.2.2. 마이크로프로세서

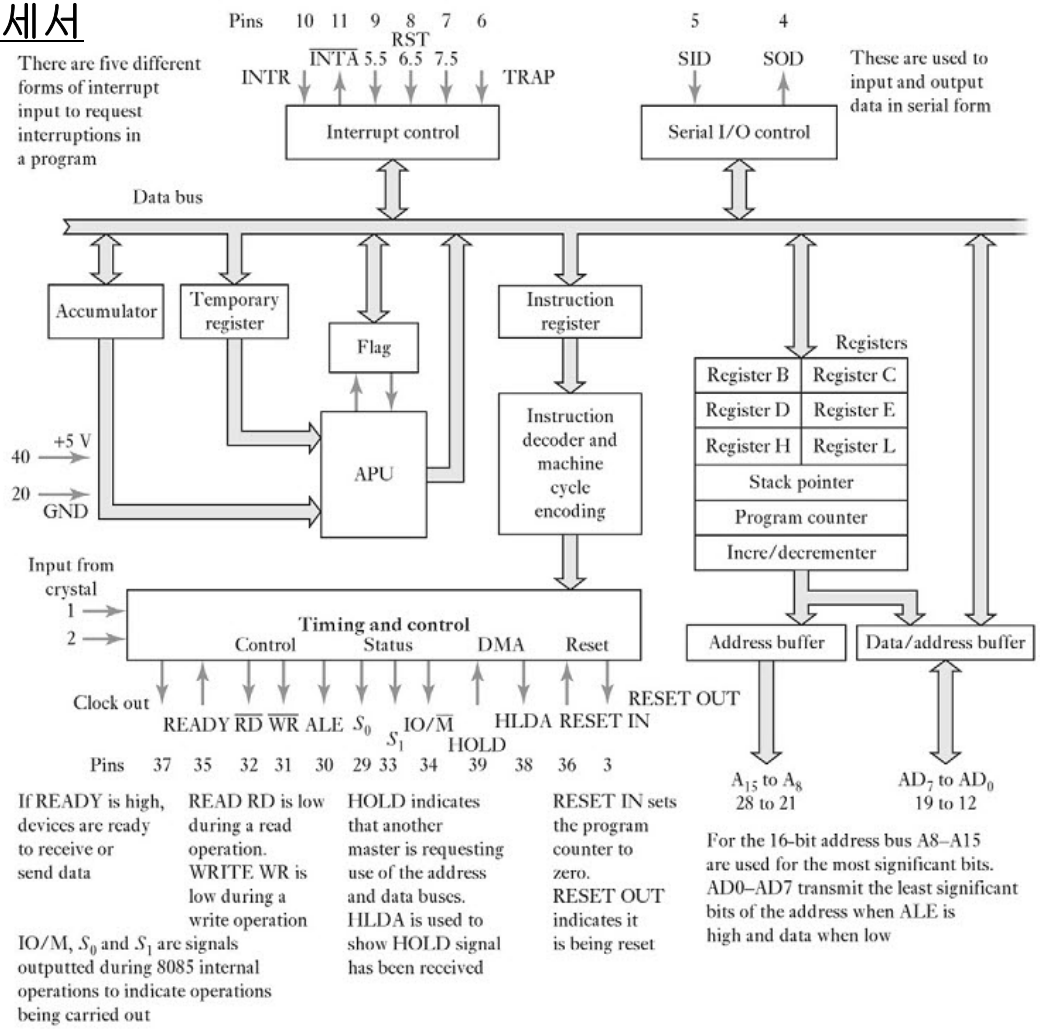

그림 17.4 Intel 8085 구조

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17. 마이크로프로세서 시스템

17.2.3. 기억장치

기억 장치로는 다음과 같이 여러 종류가 있다.

1) 읽기 전용 기억 장치 (Read-Only Memory, ROM)

2) 프로그램 가능 ROM (Programmable ROM, PROM)

3) 소거 가능 PROM (Erasable and Programmable ROM, EPROM)

4) 전기 소거식 PROM (Electrically Erasable PROM, EEPROM)

5) 램 (Random-Access Memory, RAM)

6) 플래시 메모리 (Flash memory)

Flash memory is a non-volatile computer storage chip that can be electrically erased and reprogrammed. It was developed from EEPROM (electrically erasable programmable read-only memory) and must be erased in fairly large blocks before these can be rewritten with new data.

… Although flash memory is technically a type of EEPROM, the term "EEPROM" is generally used to refer specifically to non-flash EEPROM which is erasable in small blocks, typically bytes. Because erase cycles are slow, the large block sizes used in flash memory erasing give it a significant speed advantage over old-style EEPROM when writing large amounts of data. Flash memory now costs far less than byte-programmable EEPROM and has become the dominant memory type wherever a significant amount of non-volatile, solid state storage is needed.

http://en.wikipedia.org/wiki/Flash_memory

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17. 마이크로프로세서 시스템

17.2.3. 기억장치

ALE: Address Latch Enable

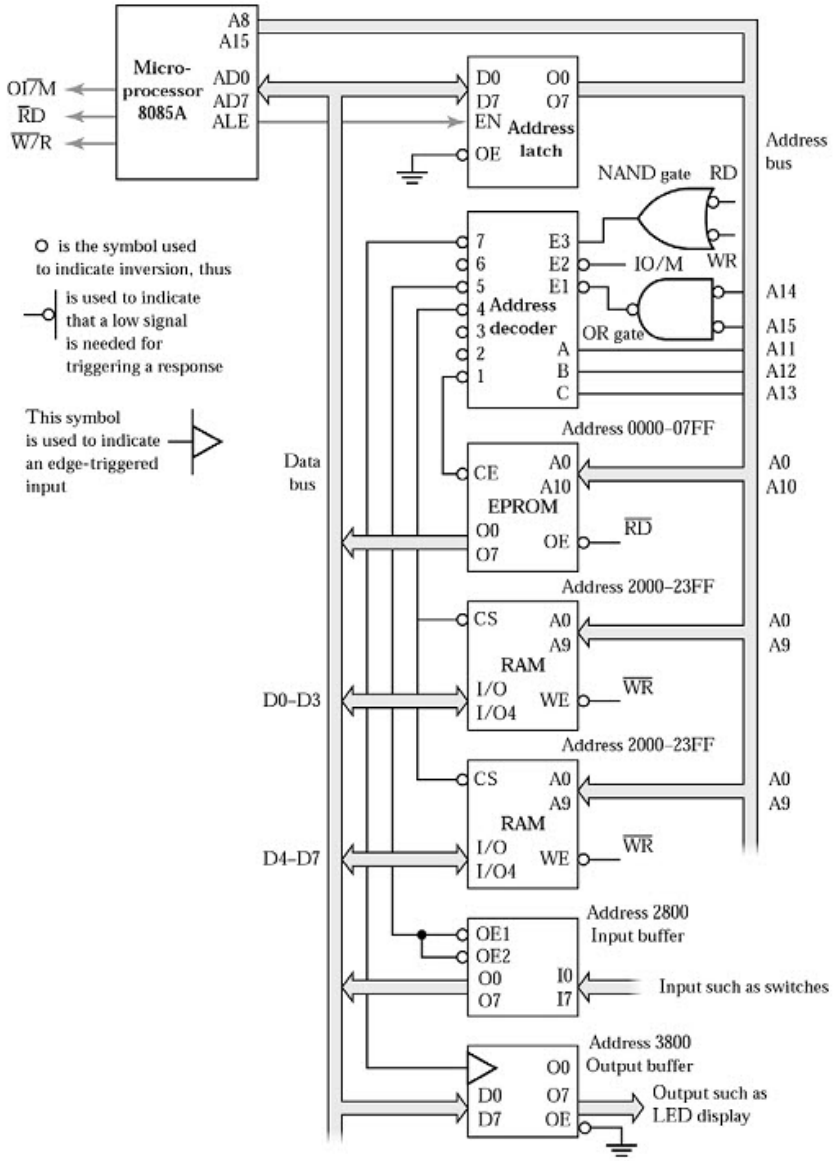

그림 17.7 Intel 8085A 시스템

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17. 마이크로프로세서 시스템

17.2.4. 입력과 출력

입출력 동작은 마이크로프로세서와 외부 간의 데이터 전송에 관계된다. 주변 장치(peripheral devices)는 마이크로프로세서 시스템과 데이터를 교환하는 장치의 일부이다.

데이터 동기 방법

1) 폴링(polling): 마이크로프로세서가 사용 가능한지 여부를 계속 관찰

2) 인터럽트(interrupt): 주변 장치가 사용 가능할 때, 마이크로프로세서에게 통보

Event에 따라 미리 정해진 ISR (Interrupt Service Routine)로 분기

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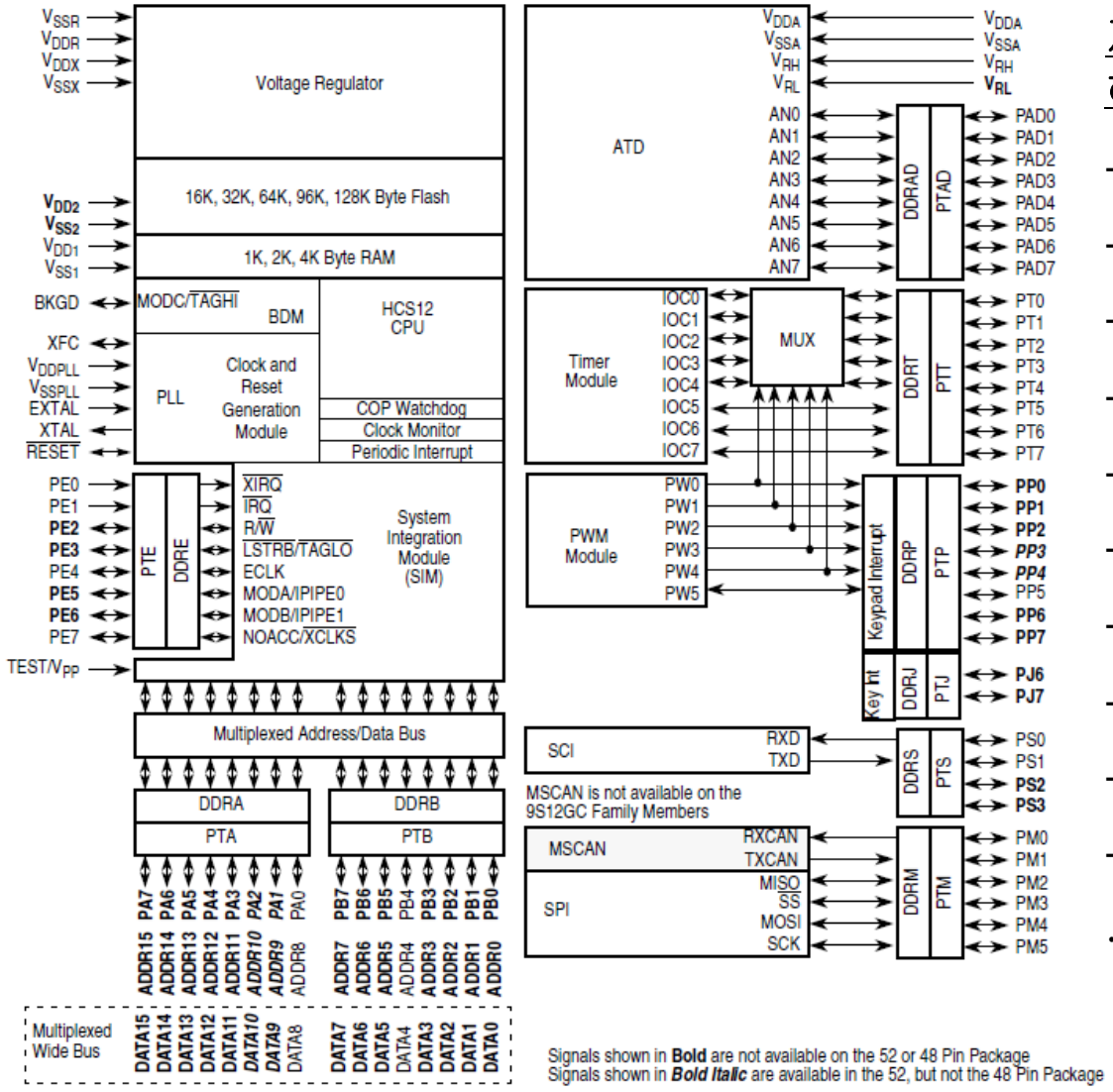
마이크로콘트롤러 [2]



제어시스템 구현에 필요한 모든 요소를 하나의 칩에 내장.

- 마이크로프로세서 (CPU)
- Flash memory
- RAM
- Timer
- ADC (Analog-Digital Converter)
- PWM (Pulse Width Modulation) module
- CAPCOM module
- 통신 (SCI, SPI, CAN, …)
- External interface
- GPIO (General Purpose I/O)

…

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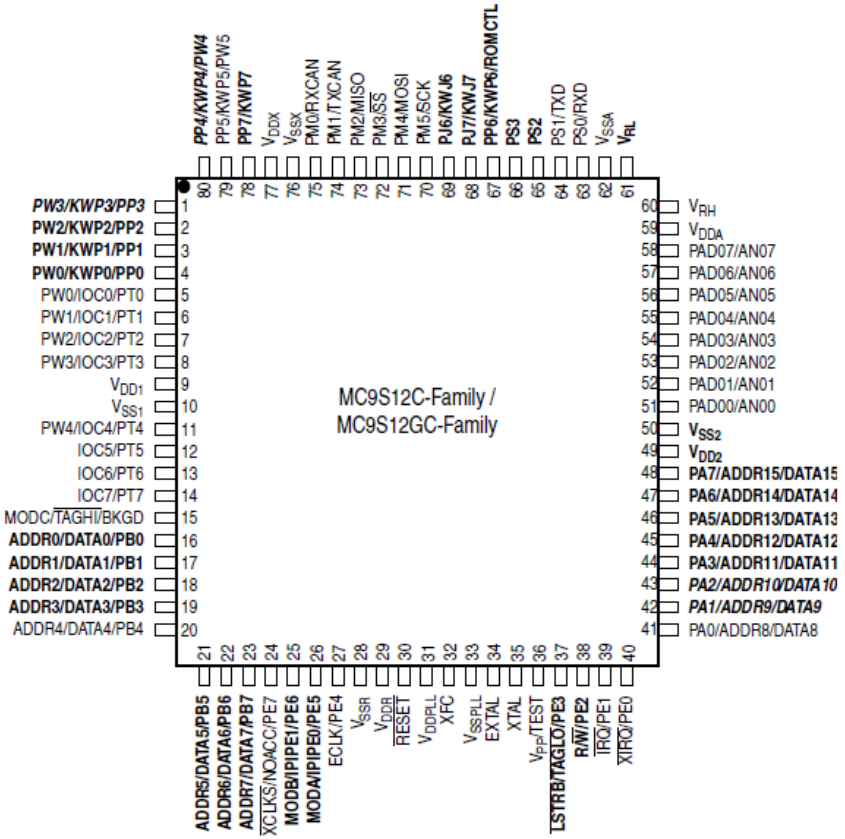
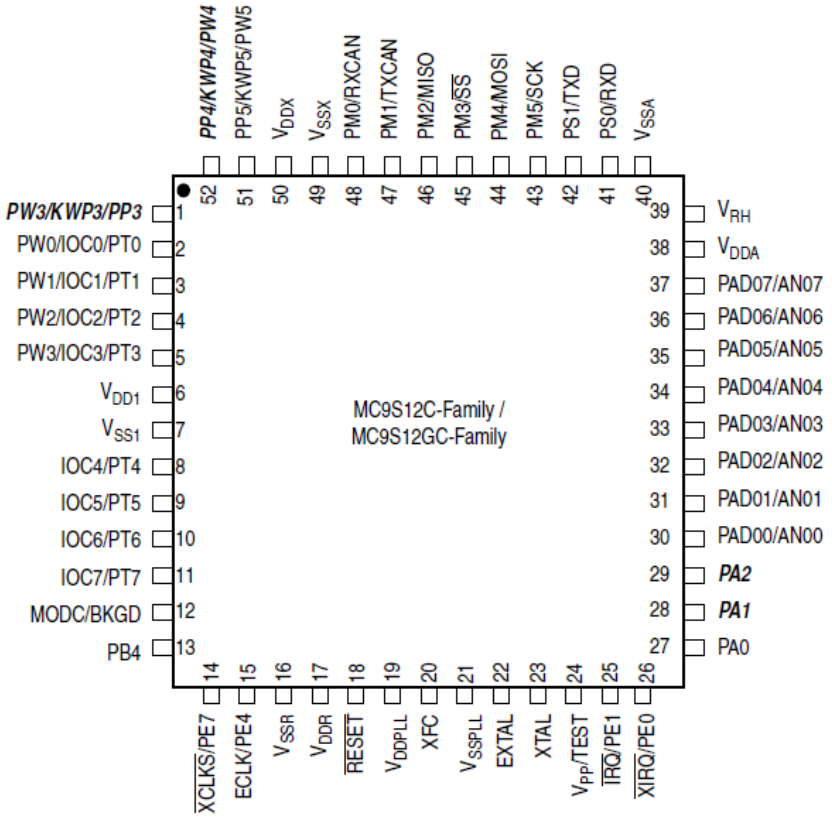
마이크로콘트롤러 [2]

요구 사항에 따라 다양한 패키지로 제작됨.



Signals shown in **Bold** are not available on the 52- or 48-pin package
Signals shown in ***Bold Italic*** are available in the 52-pin, but not the 48-pin package

Figure 1-7. Pin Assignments in 80-Pin QFP



* Signals shown in ***Bold italic*** are not available on the 48-pin package

Figure 1-8. Pin Assignments in 52-Pin LQFP

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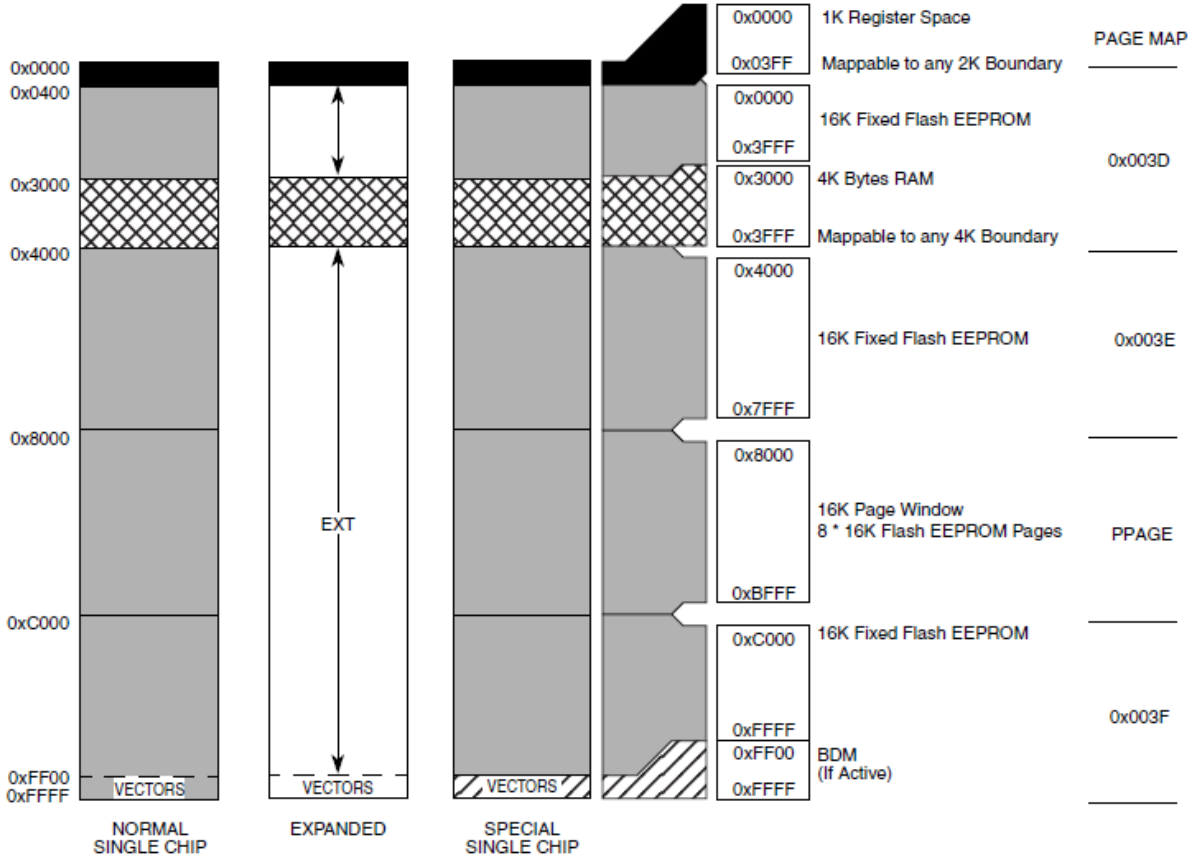
마이크로콘트롤러 [2]

Memory와 peripheral 들은 고유의 주소(address)를 통해 액세스(access)된다.



The figure shows a useful map, which is not the map out of reset. After reset the map is:

0x0000–0x03FF: Register Space

0x0000–0x0FFF: 4K RAM (only 3K visible 0x0400–0x0FFF)

Flash erase sector size is 1024 bytes

Figure 1-2. MC9S12C128 and MC9S12GC128 User Configurable Memory Map

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마이크로콘트롤러 [2]

Memory와 peripheral 들은 고유의 주소(address)를 통해 액세스(access)된다.

Table 1-1. Device Register Map Overview

Address	Module	Size
0x0000–0x0017	Core (ports A, B, E, modes, inits, test)	24
0x0018	Reserved	1
0x0019	Voltage regulator (VREG)	1
0x001A–0x001B	Device ID register	2
0x001C–0x001F	Core (MEMSIZ, IRQ, HPRIO)	4
0x0020–0x002F	Core (DBG)	16
0x0030–0x0033	Core (PPAGE[1])	4
0x0034–0x003F	Clock and reset generator (CRG)	12
0x0040–0x006F	Standard timer module (TIM)	48
0x0070–0x007F	Reserved	16
0x0080–0x009F	Analog-to-digital converter (ATD)	32
0x00A0–0x00C7	Reserved	40
0x00C8–0x00CF	Serial communications interface (SCI)	8
0x00D0–0x00D7	Reserved	8
0x00D8–0x00DF	Serial peripheral interface (SPI)	8
0x00E0–0x00FF	Pulse width modulator (PWM)	32
0x0100–0x010F	Flash control register	16
0x0110–0x013F	Reserved	48
0x0140–0x017F	Scalable controller area network (MSCAN)[2]	64
0x0180–0x023F	Reserved	192
0x0240–0x027F	Port integration module (PIM)	64
0x0280–0x03FF	Reserved	384

1. External memory paging is not supported on this device (Section 1.7.1, "PPAGE").
2. Not available on MC9S12GC Family devices

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마이크로콘트롤러 [2]

Interrupt Vector Table 영역에 ISR의 주소를 기록하여, interrupt 방식 event 처리를 구현할 수 있다.

Table 1-9. Interrupt Vector Locations

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
0xFFFE, 0xFFFF	External reset, power on reset, or low voltage reset (see CRG flags register to determine reset source)	None	None	—
0xFFFC, 0xFFFD	Clock monitor fail reset	None	COPCTL (CME, FCME)	—
0xFFFA, 0xFFFB	COP failure reset	None	COP rate select	—
0xFFF8, 0xFFF9	Unimplemented instruction trap	None	None	—
0xFFF6, 0xFFF7	SWI	None	None	—
0xFFF4, 0xFFF5	XIRQ	X-Bit	None	—
0xFFF2, 0xFFF3	IRQ	I bit	INTCR (IRQEN)	0x00F2
0xFFF0, 0xFFF1	Real time Interrupt	I bit	CRGINT (RTIE)	0x00F0
0xFFEE, 0xFFEF	Standard timer channel 0	I bit	TIE (C0I)	0x00EE
0xFFEC, 0xFFED	Standard timer channel 1	I bit	TIE (C1I)	0x00EC
$FFEE, $FFEF	Reserved			
$FFEC, $FFED	Reserved			
0xFFEA, 0xFFEB	Standard timer channel 2	I bit	TIE (C2I)	0x00EA
0xFFE8, 0xFFE9	Standard timer channel 3	I bit	TIE (C3I)	0x00E8
0xFFE6, 0xFFE7	Standard timer channel 4	I bit	TIE (C4I)	0x00E6
0xFFE4, 0xFFE5	Standard timer channel 5	I bit	TIE (C5I)	0x00E4
0xFFE2, 0xFFE3	Standard timer channel 6	I bit	TIE (C6I)	0x00E2
0xFFE0, 0xFFE1	Standard timer channel 7	I bit	TIE (C7I)	0x00E0

...

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System Clock [2]

Clock Generation

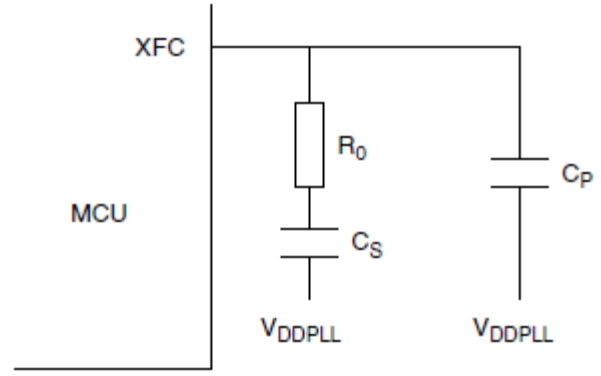
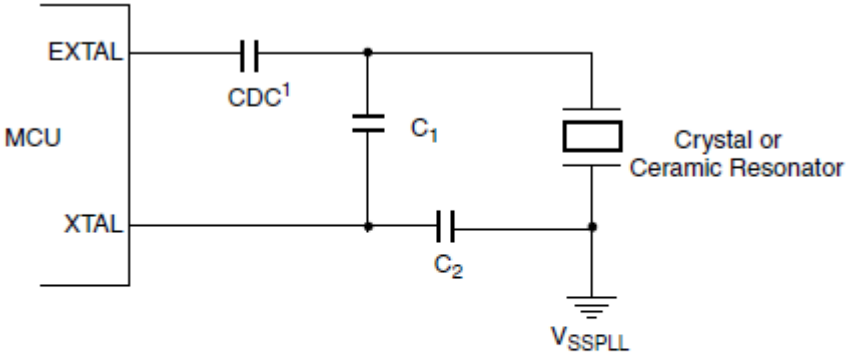
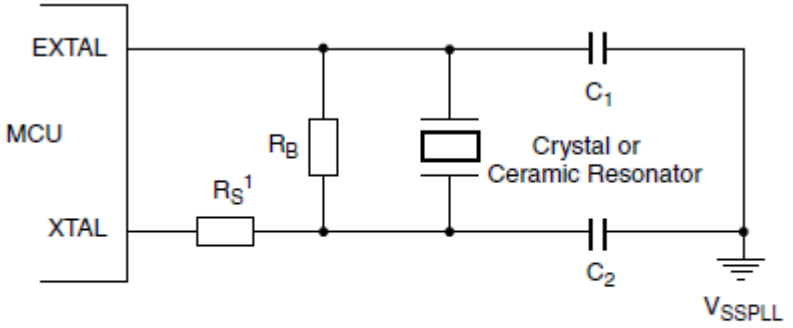


Figure 1-10. PLL Loop Filter Connections



1. Due to the nature of a translated ground Colpitts oscillator a DC voltage bias is applied to the crystal. Please contact the crystal manufacturer for crystal DC.

Figure 1-11. Colpitts Oscillator Connections (PE7 = 1)



1. RS can be zero (shorted) when used with higher frequency crystals, refer to manufacturer's data.

Figure 1-12. Pierce Oscillator Connections (PE7 = 0)

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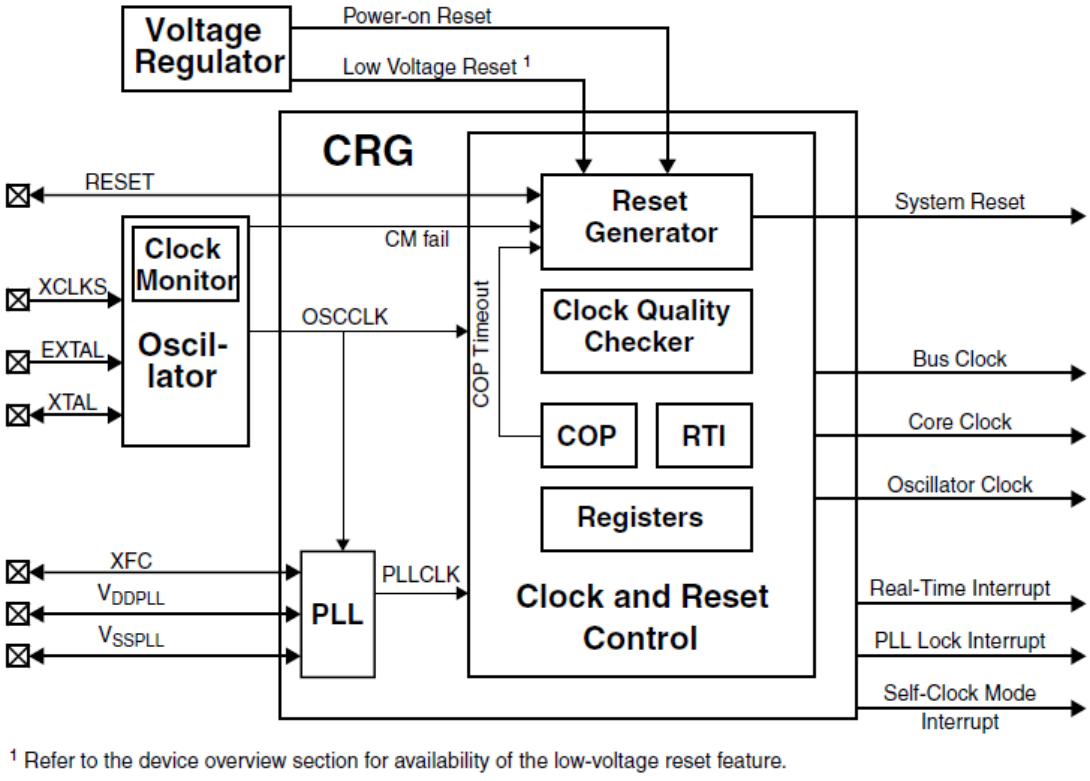
System Clock [2]

Clocks and Reset Generator



1 Refer to the device overview section for availability of the low-voltage reset feature.

Figure 9-1. CRG Block Diagram

COP (Computer Operating Properly) watchdog timer: 일정한 시간마다 체크하지 않으면 리셋.

RTI (Real-Time Interrupt)

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System Clock [2]

System Clock

The clock and reset generator provides the internal clock signals for the core and all peripheral modules.

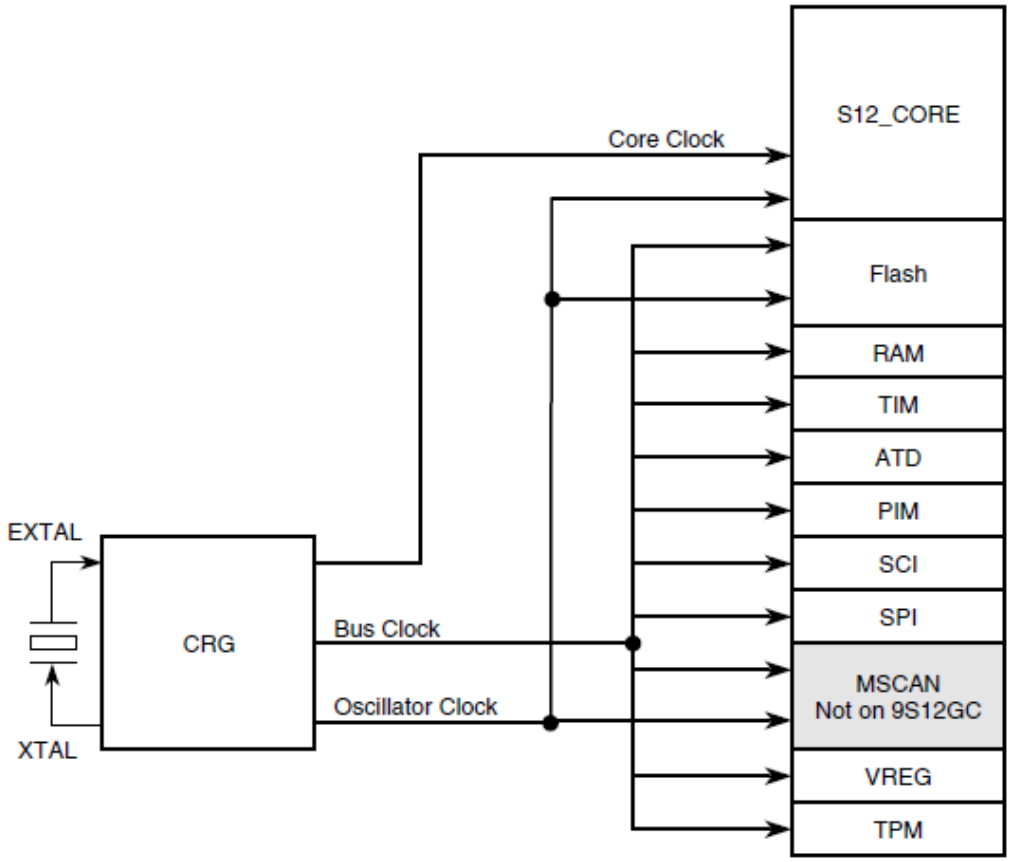

Figure 1-14. Clock Connections

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4.2. 아날로그와 디지털 신호 [1]

아날로그-디지털 변환(Analog-to-Digital Conversion, ADC): 아날로그 신호를 2진 워드로 변환하는 과정

- Clock이 일정한 간격으로 펄스 신호를 발생시키고, 이 펄스가 ADC에 전달될 때마다 아날로그 신호가 샘플(sample)된다.

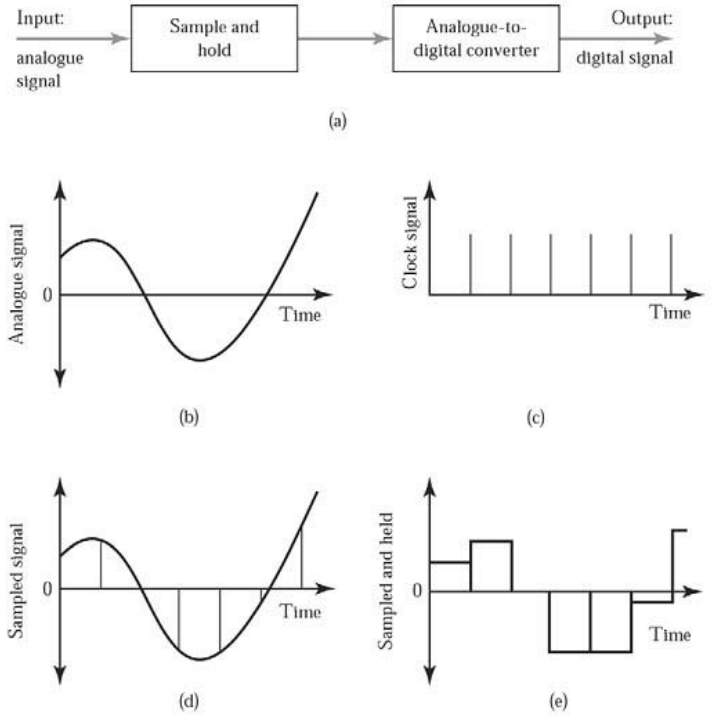

그림 4.1 (a) 아날로그 – 디지털 변환 (b) 아날로그 입력 (c) 클록 신호 (d) 샘플된 신호 (e) 샘플– 홀드 신호

ADC는 유한한 변환시간이 필요하기 때문에 샘플-홀드로 다음 변환까지 값을 유지할 필요가 있다.

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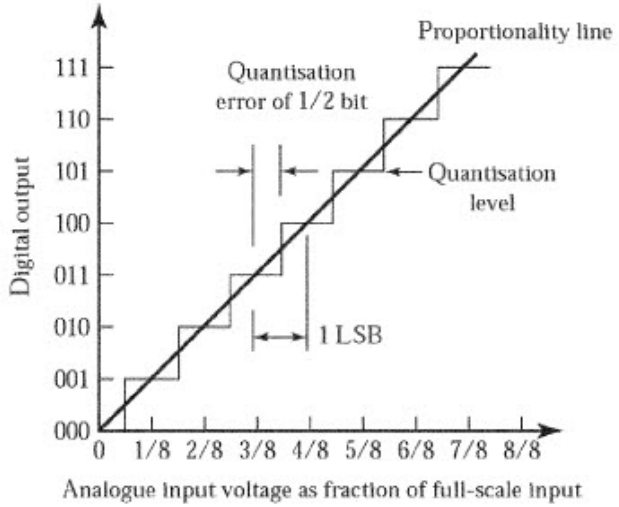
4.2. 아날로그와 디지털 신호 [1]

아날로그-디지털 변환**(Analog-to-Digital Conversion, ADC)**



출력이 3비트로 표현될 때의 입출력 관계 그래프

- 3비트이므로, 2^3=8 단계
- 출력의 변화가 없는 입력의 범위 존재
- 8개의 출력 레벨을 양자화 레벨(quantization level), 두 인접한 양자화 레벨 사이 전압차를 양자화 구간 (quantization interval)이라고 부른다.
- 양자화 오차(quantization error): 디지털 출력과 아날로그 입력 사이 오차
- 분해능 (resolution): 디지털 출력이 표현할 수 있는 최소의 입력 변화량

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4.2. 아날로그와 디지털 신호 [1]

아날로그-디지털 변환**(Analog-to-Digital Conversion, ADC)**

- **분해능 (resolution)**: 디지털 출력이 표현할 수 있는 최소의 입력 변화량

  ADC 출력 워드 비트: n

  Full-scale 아날로그 입력: V_{FS}

  분해능: $V_{FS}/2^n$

- 워드 길이 10비트인 ADC로 10V 레인지의 전압을 입력신호를 양자화하면,

  분해능은 $10V/2^{10}=9.8mV$

- 출력이 0.5mV/˚C 인 열전대, 0˚C ~ 200˚C 범위를 0.5˚C로 계측하고자 할 때, word 길이는?

  (200-0)/0.5=400

  $2^n>=400$, $n>=\log_2 400=8.6439$

  따라서, 최소 9비트 필요

  이때, 분해능은 0.5˚C, 열전대 출력전압의 quantization interval은 0.5mV/˚C x 0.5˚C=0.25mV

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4.2. 아날로그와 디지털 신호 [1]

아날로그-디지털 변환(**Analog-to-Digital Conversion, ADC**)

나이키스트 조건(**Nyquist criterion**) 또는 샤논의 샘플링 정리(**Shannon's sampling theorem**)

신호의 최대 주파수 성분보다 적어도 두 배 이상의 주파수로 샘플해야만 원래 신호의 형태를 잃지 않는다. 샘플링 주파수가 낮을 때 생기는 왜곡을 에일리어싱(aliasing)이라고 하며, 이를 방지하기 위해 ADC 입력단에 설치하는 저역통과필터를 안티 에일리어싱 필터(**anti-aliasing filter**)라 한다.

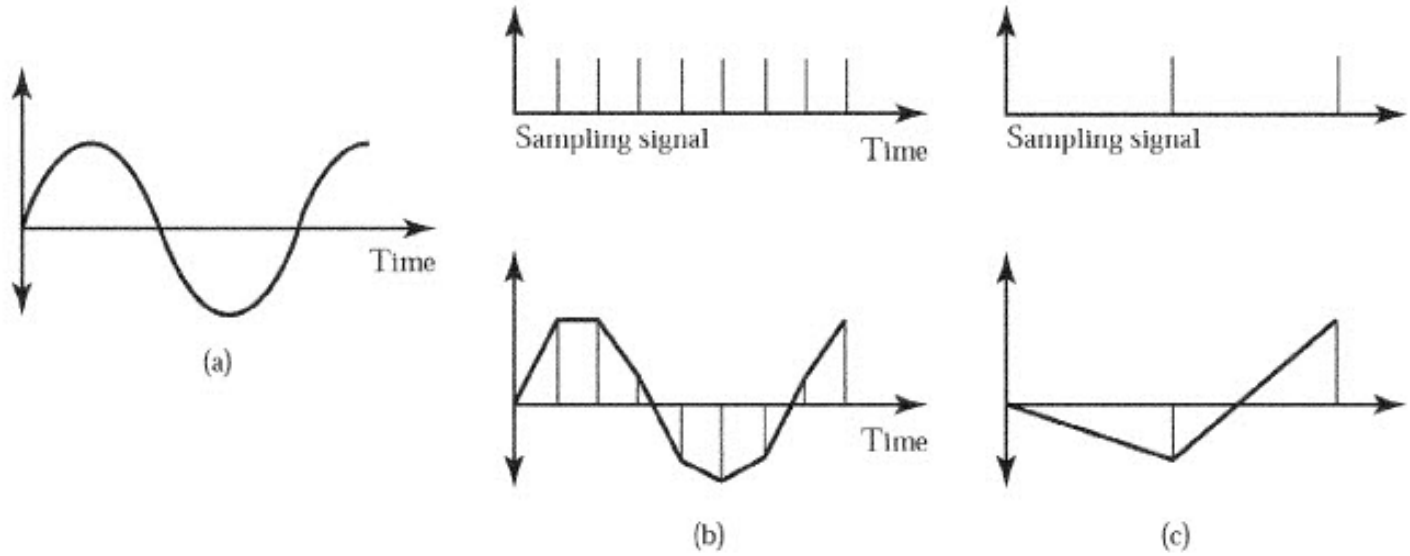

그림 4.3 샘플링 주파수의 영향 : (a) 아날로그 신호 (b) 샘플된 신호 (c) 샘플된 신호

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4.2. 아날로그와 디지털 신호 [1]

디지털-아날로그 변환**(Digital-to-Analog Conversion, DAC)**

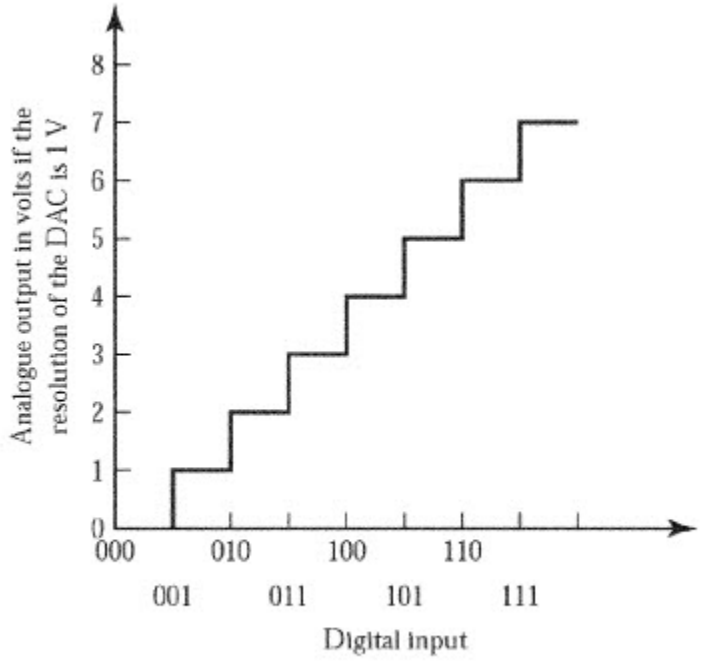

그림 4.4 DAC의 입출력

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4.3. DAC와 ADC 실제 [1]

4.3.1. 디지털-아날로그 변환(Digital-to-Analog Conversion, DAC)

가중저항 네트워크 방식

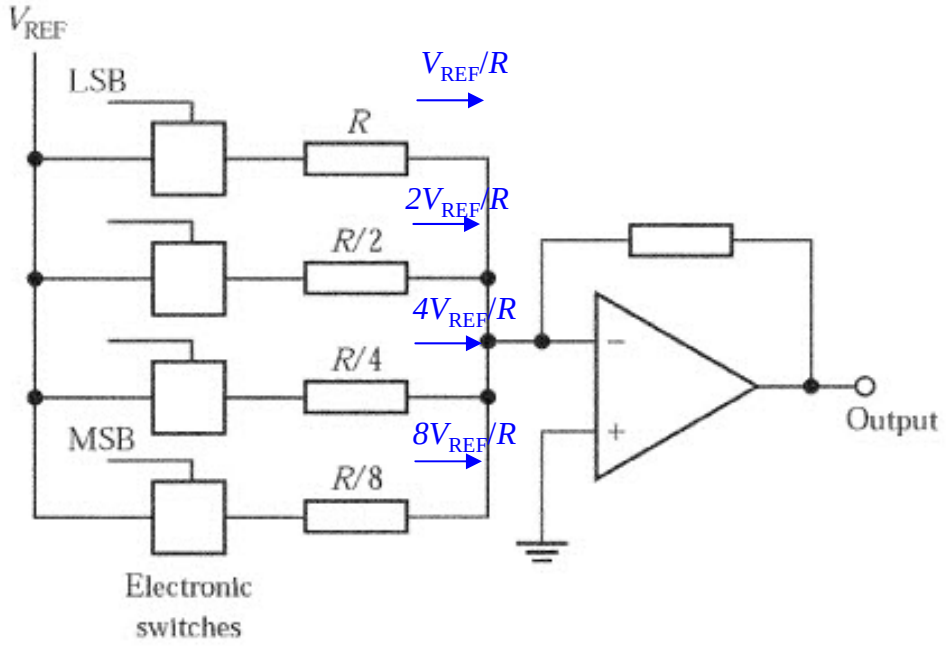

그림 4.5 가중저항 DAC

가중저항 네트워크의 문제점은 ADC의 정밀도가 각 저항들의 정밀도에 좌우되므로 비트 수가 증가할 때 넓은 범위의 정밀한 저항들을 구하는 것이 어렵다는 데 있다.

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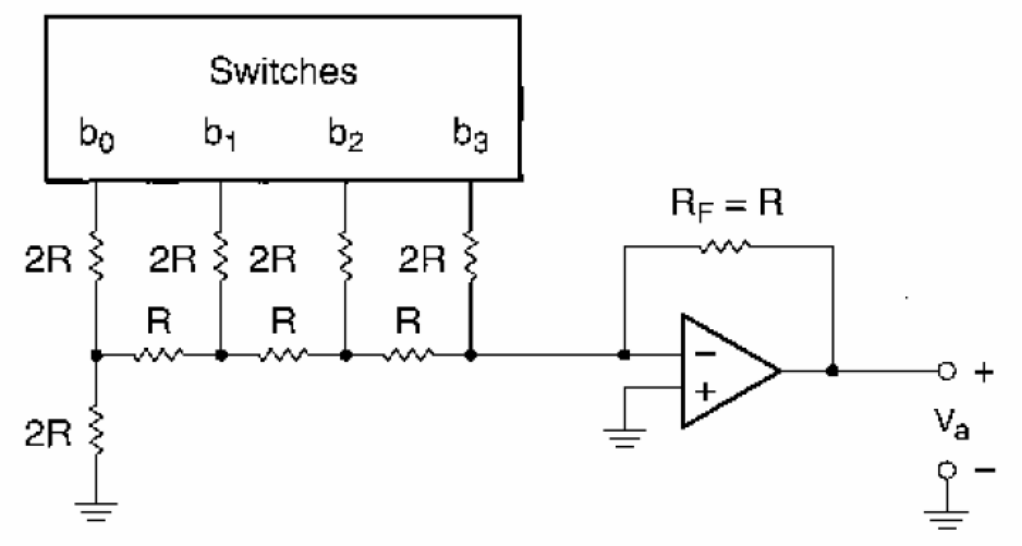
4.3. DAC와 ADC 실제 [1]

4.3.1. 디지털-아날로그 변환(Digital-to-Analog Conversion, DAC)

R-2R 래더(ladder) 네트워크 방식



두 종류의 저항만이 필요하므로 넓은 범위의 정밀저항이 소요되는 문제를 해결했다.

http://home.pcu.ac.kr/_upload/PDSBoard_01/PDSBoardDocs_82/jgjeong/3/Chapter%2012.pdf

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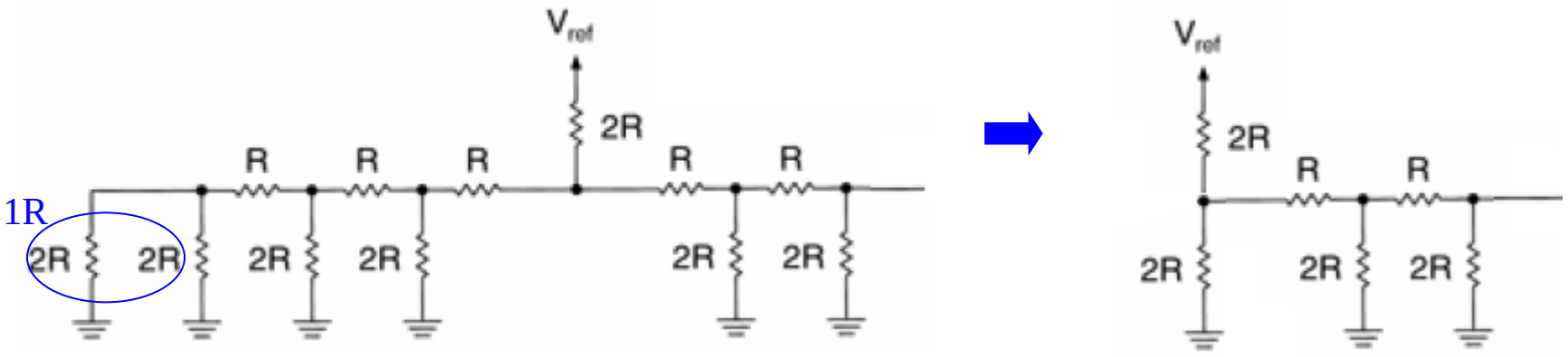
4.3. DAC와 ADC 실제 [1]

4.3.1. 디지털-아날로그 변환(Digital-to-Analog Conversion, DAC)

R-2R 래더(ladder) 네트워크 방식

1) 중첩의 원리

2) 임의의 한 비트만 ON인 경우



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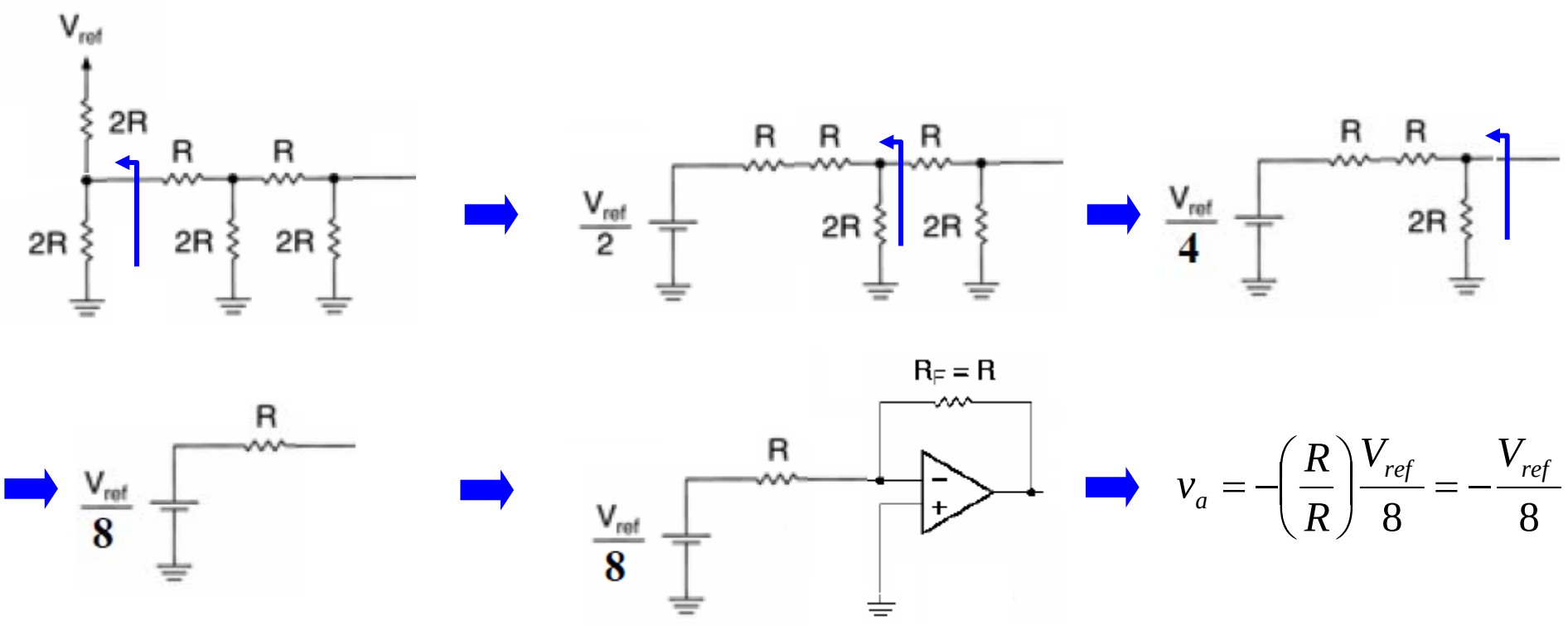
4.3. DAC와 ADC 실제 [1]

4.3.1. 디지털-아날로그 변환(Digital-to-Analog Conversion, DAC)

R-2R 래더(ladder) 네트워크 방식

3) 테브난 등가회로



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4.3. DAC와 ADC 실제 [1]

4.3.2. 아날로그-디지털변환(Analog-to-Digital Conversion, ADC)

램프(ramp) 형

일정한 속도로 증가하는 램프전압이 있고,

이 전압과 입력 전압을 비교하는 비교기.

이 램프전압이 입력전압에 도달하는 시간을 측정.

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4.3. DAC와 ADC 실제 [1]

4.3.2. 아날로그-디지털변환(Analog-to-Digital Conversion, ADC)

연속근사(successive approximation) 법

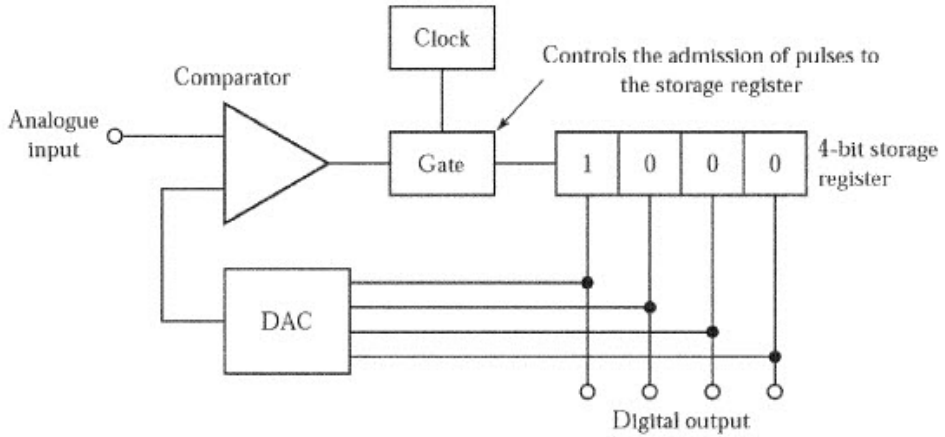

그림 4.9 연속근사법 ADC

연속근가법: MSB부터 LSB쪽으로 비트 결정. DAC 출력 전압이 입력 이하가 되도록.

1000과 비교 → DAC 출력 전압이 작으면 1100과 비교

→ DAC 출력 전압이 크면 0100과 비교 → DAC 출력 전압이 작으면 0110과 비교

→ DAC 출력 전압이 크면 0010과 비교

*n*비트 워드에 대하여 *n*번 시도로 비교를 완수할 수 있다.

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4.3. DAC와 ADC 실제 [1]

4.3.2. 아날로그-디지털변환(Analog-to-Digital Conversion, ADC)

플래시(flash) 법

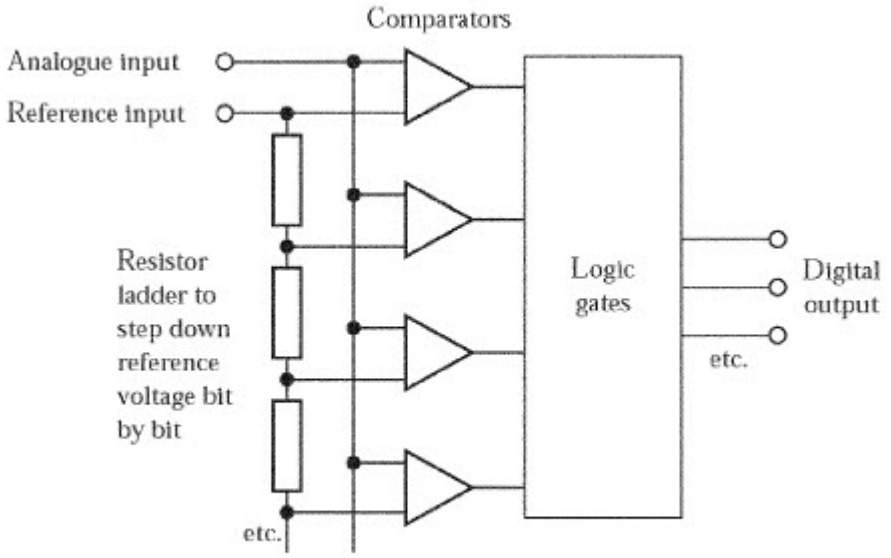

그림 4.14 플래시 ADC

워드 길이가 n일 경우, 아날로그 입력전압이 한 입력단에 공급되는 2^n-1개의 개별적 비교기가 동시에 병렬로 비교된다.

각 비교기엔 저항 래더를 통해 양자화 레벨에 해당하는 기준 전압 공급.

입력 전압이 기준 전압보다 낮으면 low, 높으면 high를 출력 → high를 출력한 비교기 중 가장 높은 기준 전압을 사용한 비교기의 기준 전압을 입력전압으로 인식.

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4.3. DAC와 ADC 실제 [2]

마이컴 ADC 모듈의 예

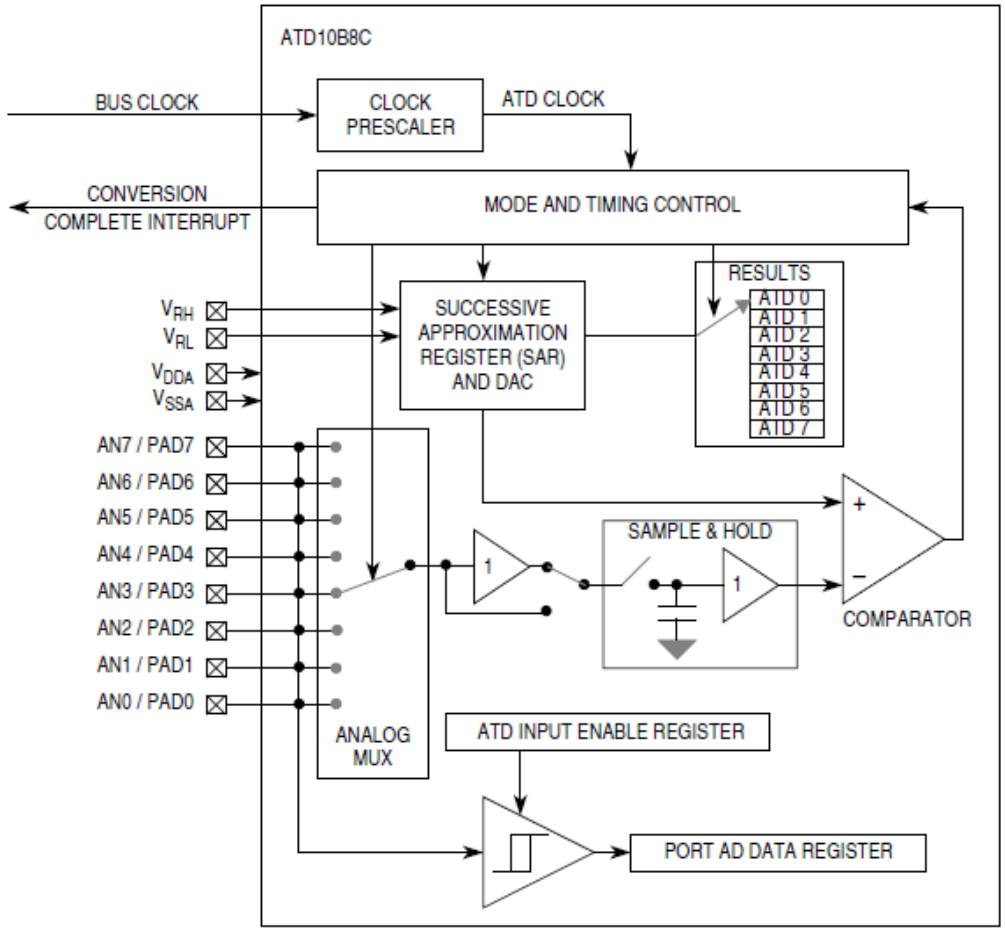

Figure 8-1. ATD10B8C Block Diagram

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PWM Block [2]

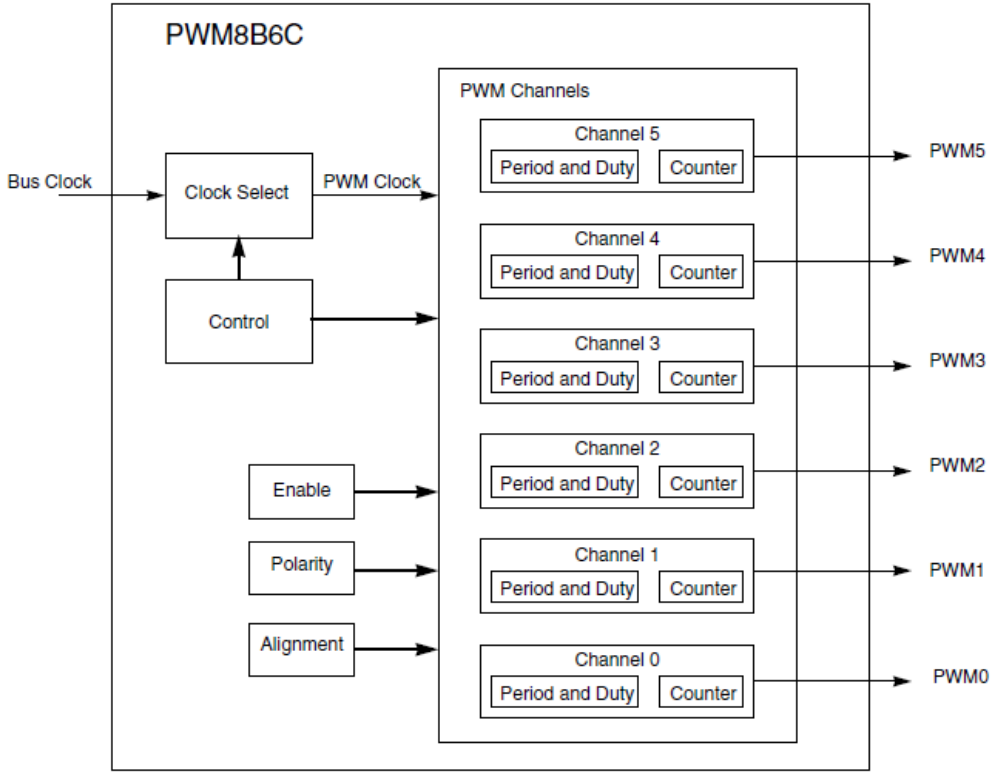

Figure 12-1. PWM8B6CV1 Block Diagram

기준 clock 선택, 극성, alignment 등을 설정한 후,

PWM 채널의 period와 duty 값을 설정하면, 하드웨어적으로 PWM 신호 발생

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PWM Block [2]

Table 12-1. PWM8B6CV1 Memory Map

Address Offset	Register	Access
0x0000	PWM Enable Register (PWME)	R/W
0x0001	PWM Polarity Register (PWMPOL)	R/W
0x0002	PWM Clock Select Register (PWMCLK)	R/W
0x0003	PWM Prescale Clock Select Register (PWMPRCLK)	R/W
0x0004	PWM Center Align Enable Register (PWMCAE)	R/W
0x0005	PWM Control Register (PWMCTL)	R/W
0x0006	PWM Test Register (PWMTST)(1)	R/W
0x0007	PWM Prescale Counter Register (PWMPRSC)(2)	R/W
0x0008	PWM Scale A Register (PWMSCLA)	R/W
0x0009	PWM Scale B Register (PWMSCLB)	R/W
0x000A	PWM Scale A Counter Register (PWMSCNTA)(3)	R/W
0x000B	PWM Scale B Counter Register (PWMSCNTB)(4)	R/W
0x000C	PWM Channel 0 Counter Register (PWMCNT0)	R/W
0x000D	PWM Channel 1 Counter Register (PWMCNT1)	R/W
0x000E	PWM Channel 2 Counter Register (PWMCNT2)	R/W
0x000F	PWM Channel 3 Counter Register (PWMCNT3)	R/W
0x0010	PWM Channel 4 Counter Register (PWMCNT4)	R/W
0x0011	PWM Channel 5 Counter Register (PWMCNT5)	R/W
0x0012	PWM Channel 0 Period Register (PWMPER0)	R/W
0x0013	PWM Channel 1 Period Register (PWMPER1)	R/W
0x0014	PWM Channel 2 Period Register (PWMPER2)	R/W
0x0015	PWM Channel 3 Period Register (PWMPER3)	R/W
0x0016	PWM Channel 4 Period Register (PWMPER4)	R/W
0x0017	PWM Channel 5 Period Register (PWMPER5)	R/W
0x0018	PWM Channel 0 Duty Register (PWMDTY0)	R/W
0x0019	PWM Channel 1 Duty Register (PWMDTY1)	R/W
0x001A	PWM Channel 2 Duty Register (PWMDTY2)	R/W
0x001B	PWM Channel 3 Duty Register (PWMDTY3)	R/W
0x001C	PWM Channel 4 Duty Register (PWMDTY4)	R/W
0x001D	PWM Channel 5 Duty Register (PWMDTY5)	R/W
0x001E	PWM Shutdown Register (PWMSDN)	R/W

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PWM Block [2]

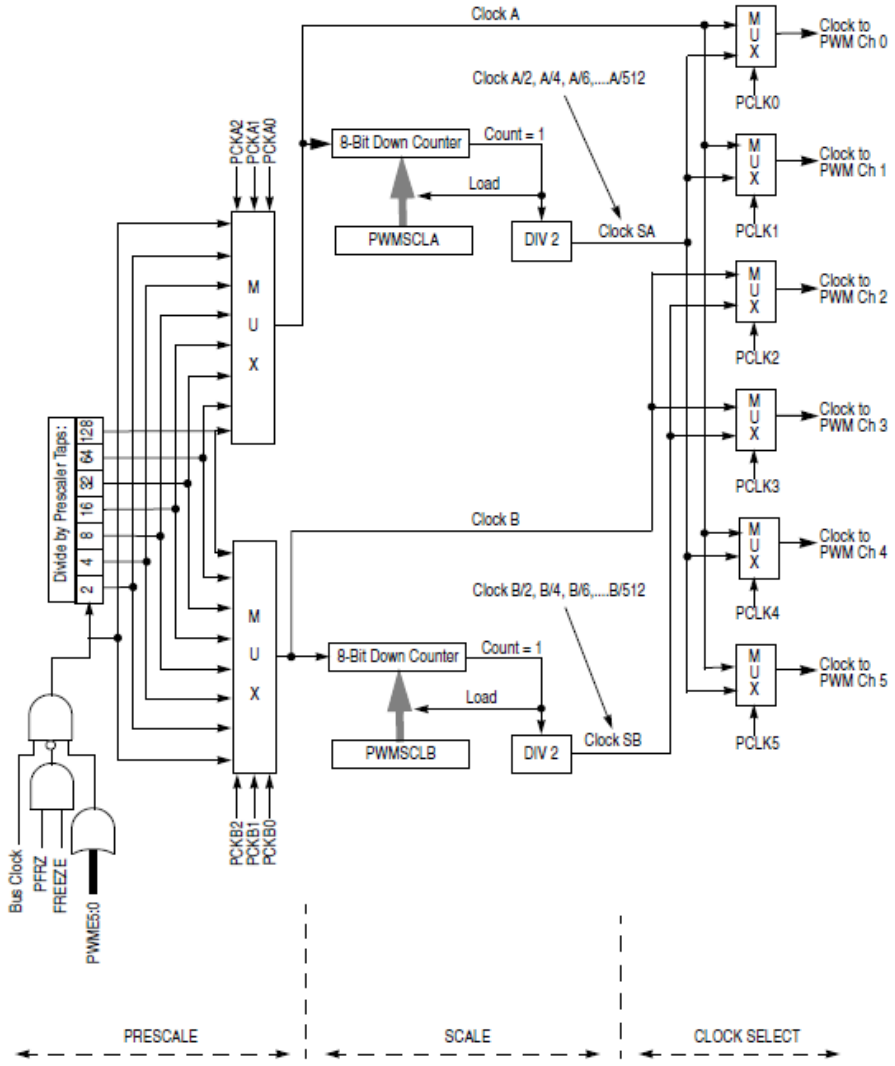

Figure 12-34. PWM Clock Select Block Diagram

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PWM Block [2]

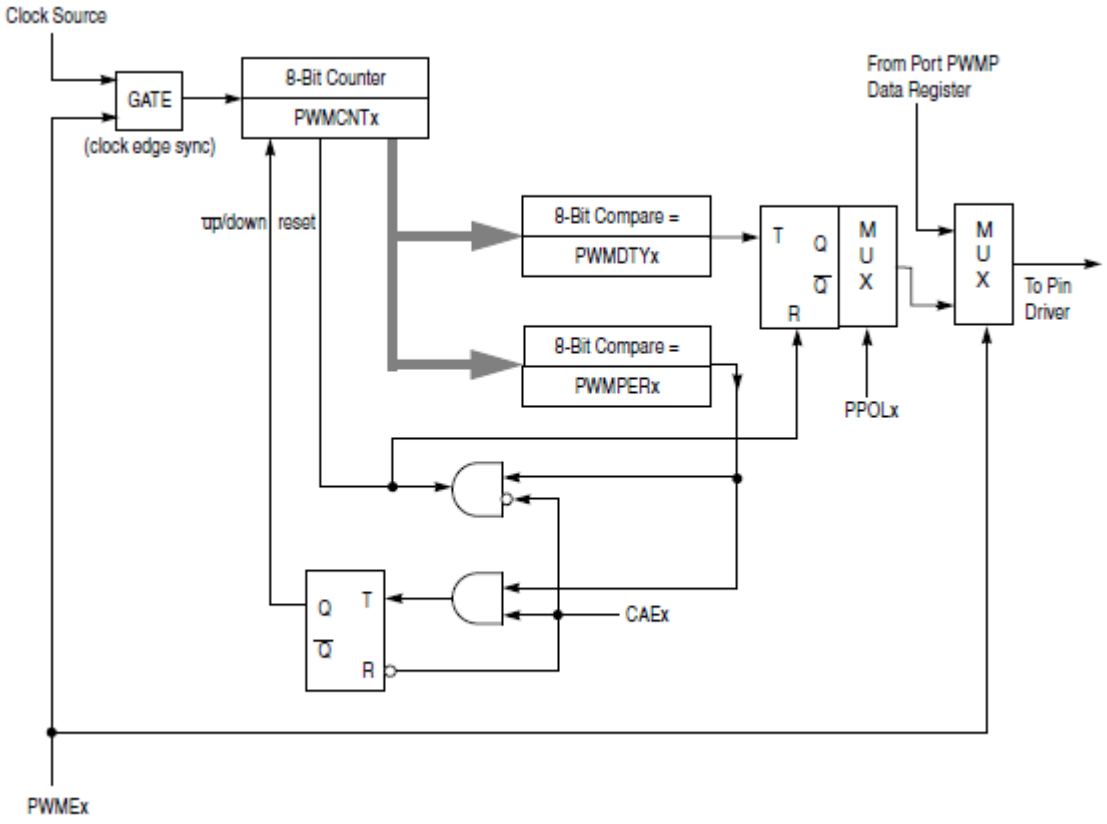

Figure 12-35. PWM Timer Channel Block Diagram

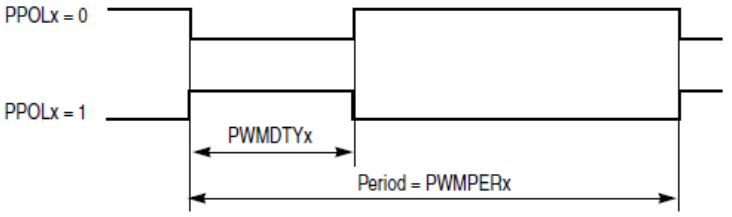

Figure 12-36. PWM Left Aligned Output Waveform

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Timer or CAPCOM Block [2]

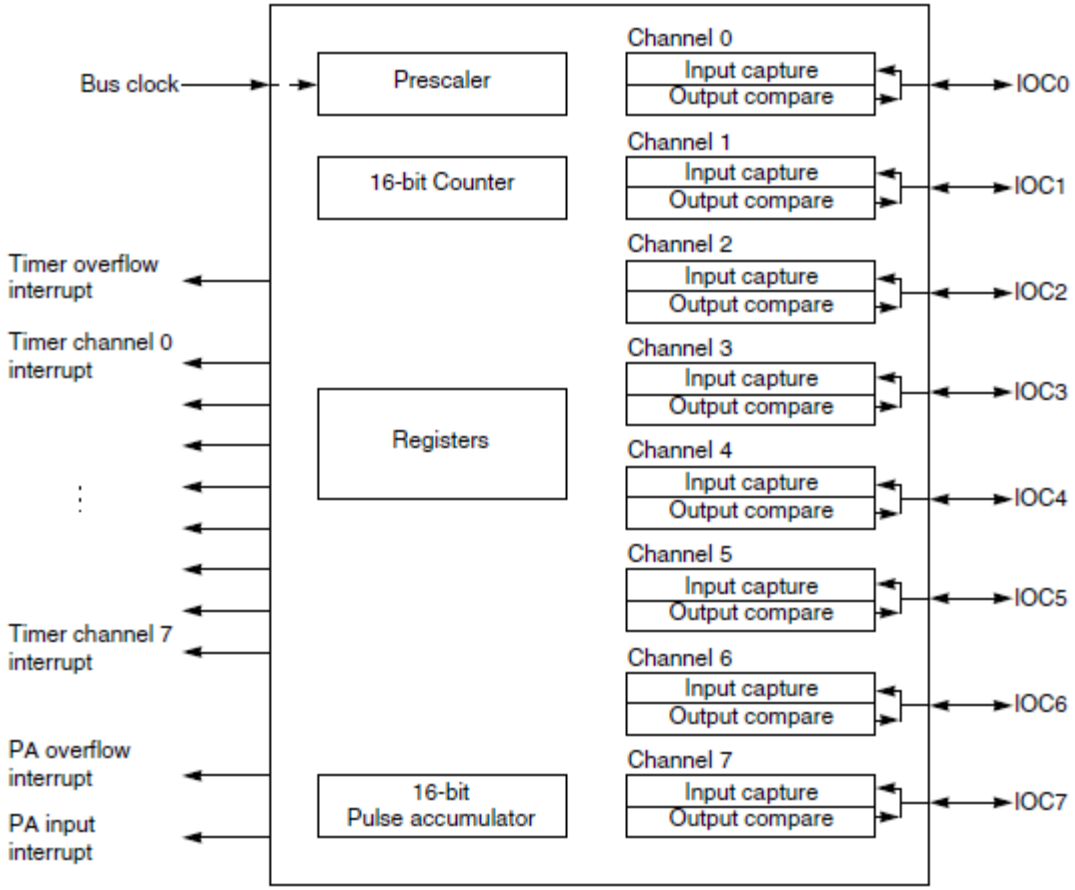

Figure 15-1. TIM16B8CV1 Block Diagram

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Timer or CAPCOM Block [2]

15.4.2 Input Capture

Clearing the I/O (input/output) select bit, IOSx, configures channel x as an input capture channel. The input capture function captures the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the timer transfers the value in the timer counter into the timer channel registers, TCx.

The minimum pulse width for the input capture input is greater than two bus clocks.

An input capture on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests. Timer module must stay enabled (TEN bit of TSCR1 must be set to one) while clearing CxF (writing one to CxF).

15.4.3 Output Compare

Setting the I/O select bit, IOSx, configures channel x as an output compare channel. The output compare function can generate a periodic pulse with a programmable polarity, duration, and frequency. When the timer counter reaches the value in the channel registers of an output compare channel, the timer can set, clear, or toggle the channel pin. An output compare on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests. Timer module must stay enabled (TEN bit of TSCR1 register must be set to one) while clearing CxF (writing one to CxF).

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Timer or CAPCOM Block [2]

15.4.4 Pulse Accumulator

The pulse accumulator (PACNT) is a 16-bit counter that can operate in two modes:

Event counter mode — Counting edges of selected polarity on the pulse accumulator input pin, PAI.

Gated time accumulation mode — Counting pulses from a divide-by-64 clock. The PAMOD bit selects the mode of operation.

The minimum pulse width for the PAI input is greater than two bus clocks.

15.4.5 Event Counter Mode

Clearing the PAMOD bit configures the PACNT for event counter operation. An active edge on the IOC7 pin increments the pulse accumulator counter. The PEDGE bit selects falling edges or rising edges to increment the count.

The Pulse Accumulator counter register reflect the number of active input edges on the PACNT input pin since the last reset.

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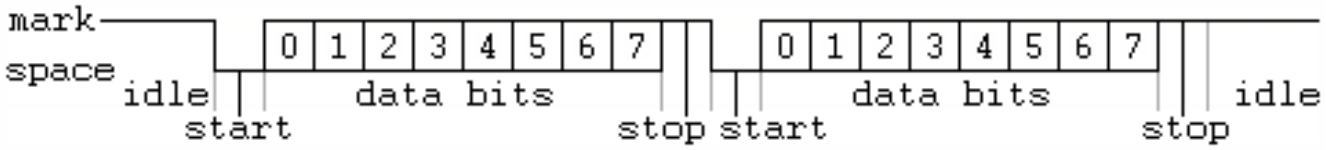
통신

Asynchronous serial communication describes an asynchronous, serial transmission protocol in which **a start signal** is sent prior to each byte, character or code word and **a stop signal** is sent after each code word. The start signal serves to prepare the receiving mechanism for the reception and registration of a symbol and the stop signal serves to bring the receiving mechanism to rest in preparation for the reception of the next symbol. A common kind of start-stop transmission is ASCII over **RS-232**, for example for use in teletypewriter operation.



http://en.wikipedia.org/wiki/Asynchronous_serial_communication

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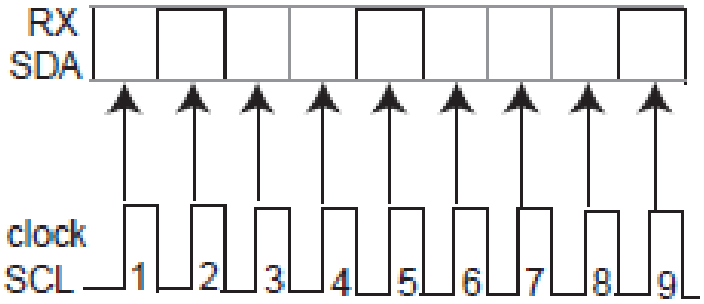
통신

Synchronous serial communications require a separate signal line to carry a **clock pulse** that triggers the arrival of a new data bit. Three common synchronous communication methods are **I^2C**, **SPI**, and Microwire.

I^2C: 2-wire, a serial data line (SDA) and a serial clock line (SCL)

SPI (Serial Peripheral Interface): 4-wire, master out, slave in (MOSI), master in, slave out (MISO), serial clock (SCK), and slave select (SS)



http://www.sampledsystems.com/pdfs/SynchronousComm.pdf

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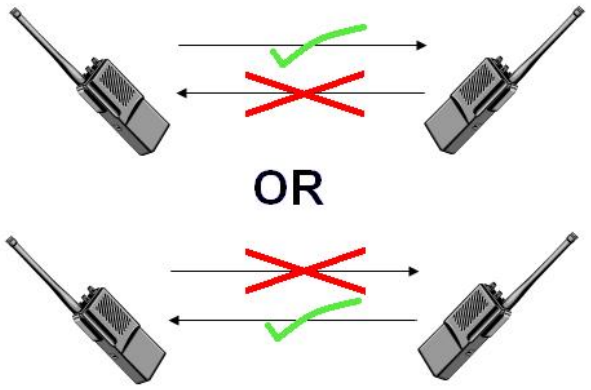
통신

A *half-duplex* (HDX) system provides communication in both directions, but only one direction at a time (not simultaneously). Typically, once a party begins receiving a signal, it must wait for the transmitter to stop transmitting, before replying (antennas are of trans-receiver type in these devices, so as to transmit and receive the signal as well).



A *full-duplex* (FDX), or sometimes *double-duplex* system, allows communication in both directions, and, unlike half-duplex, allows this to happen simultaneously. Land-line telephone networks are full-duplex, since they allow both callers to speak and be heard at the same time. A good analogy for a *full-duplex* system would be a two-lane road with one lane for each direction.

http://en.wikipedia.org/wiki/Duplex_(telecommunications)

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통신 – SCI [2]

SCI (Serial Communication Interface)

The SCI allows **asynchronous** serial communications with peripheral devices and other CPUs.

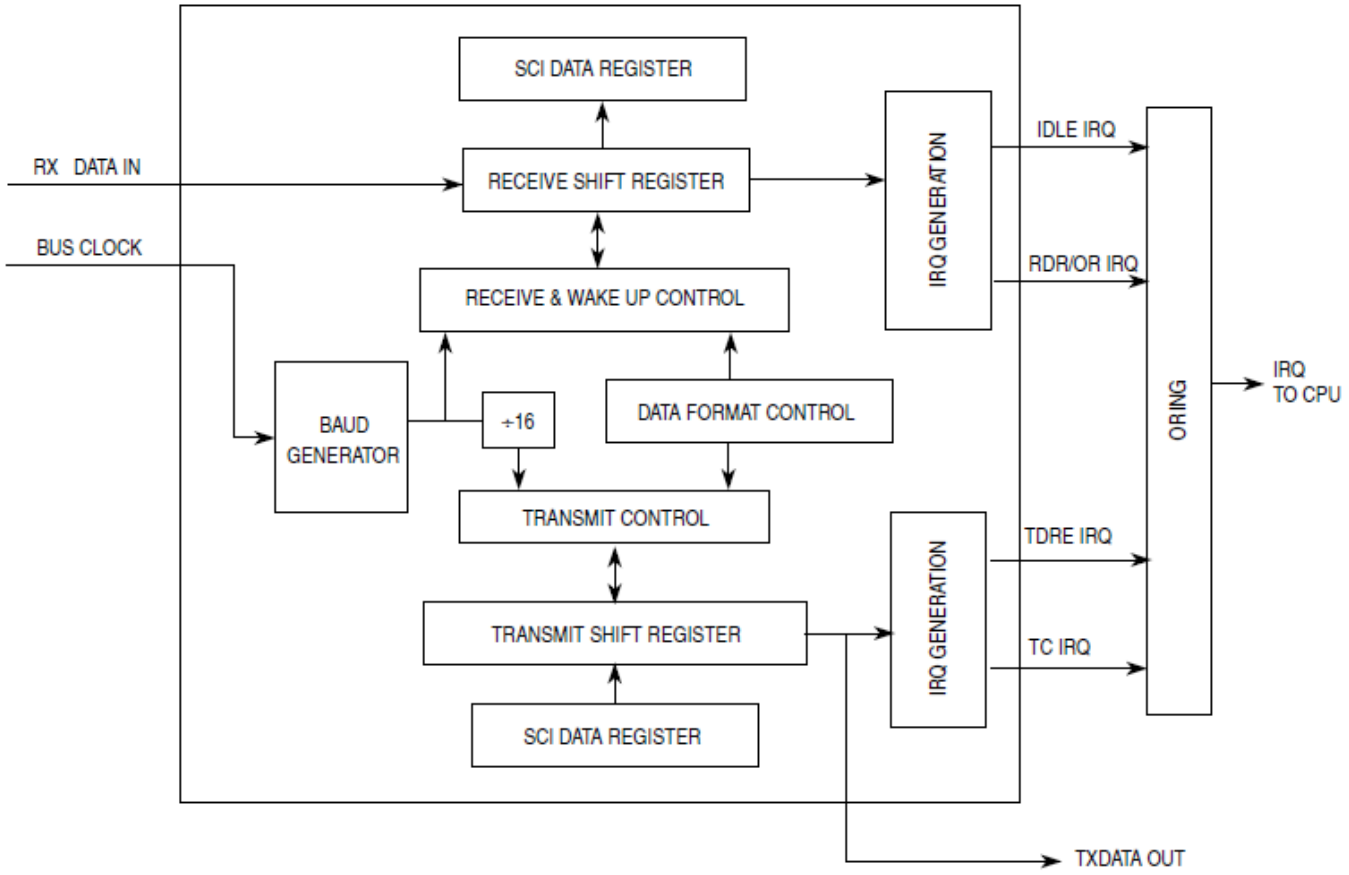

Figure 13-1. SCI Block Diagram

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통신 – SCI [2]

SCI (Serial Communication Interface)

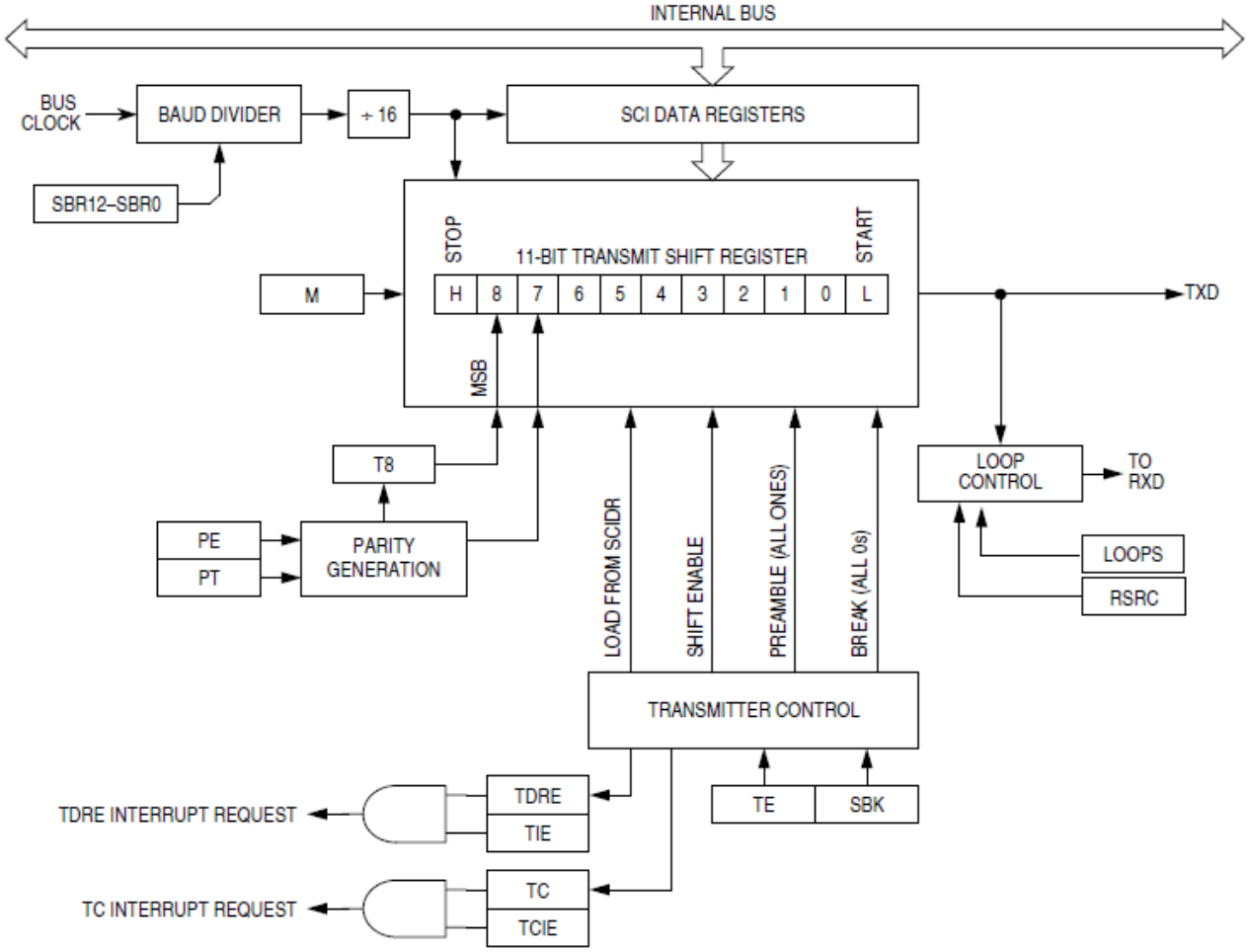

Figure 13-11. Transmitter Block Diagram

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통신 – SCI [2]

SCI (Serial Communication Interface)

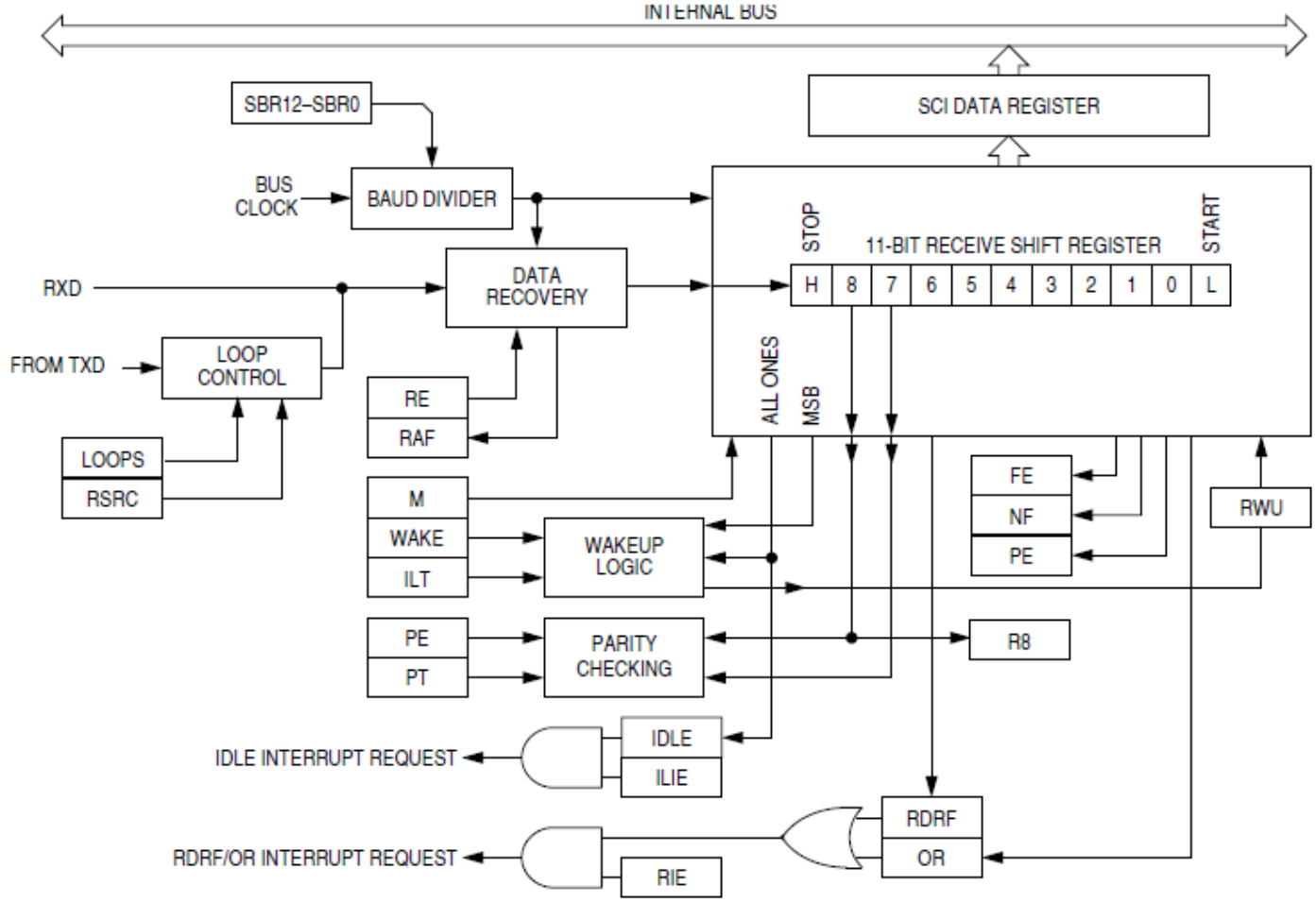

Figure 13-12. SCI Receiver Block Diagram

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통신 – SPI [2]

SPI (Serial Peripheral Interface)

The SPI module allows a duplex, **synchronous**, serial communication between the MCU and peripheral devices.

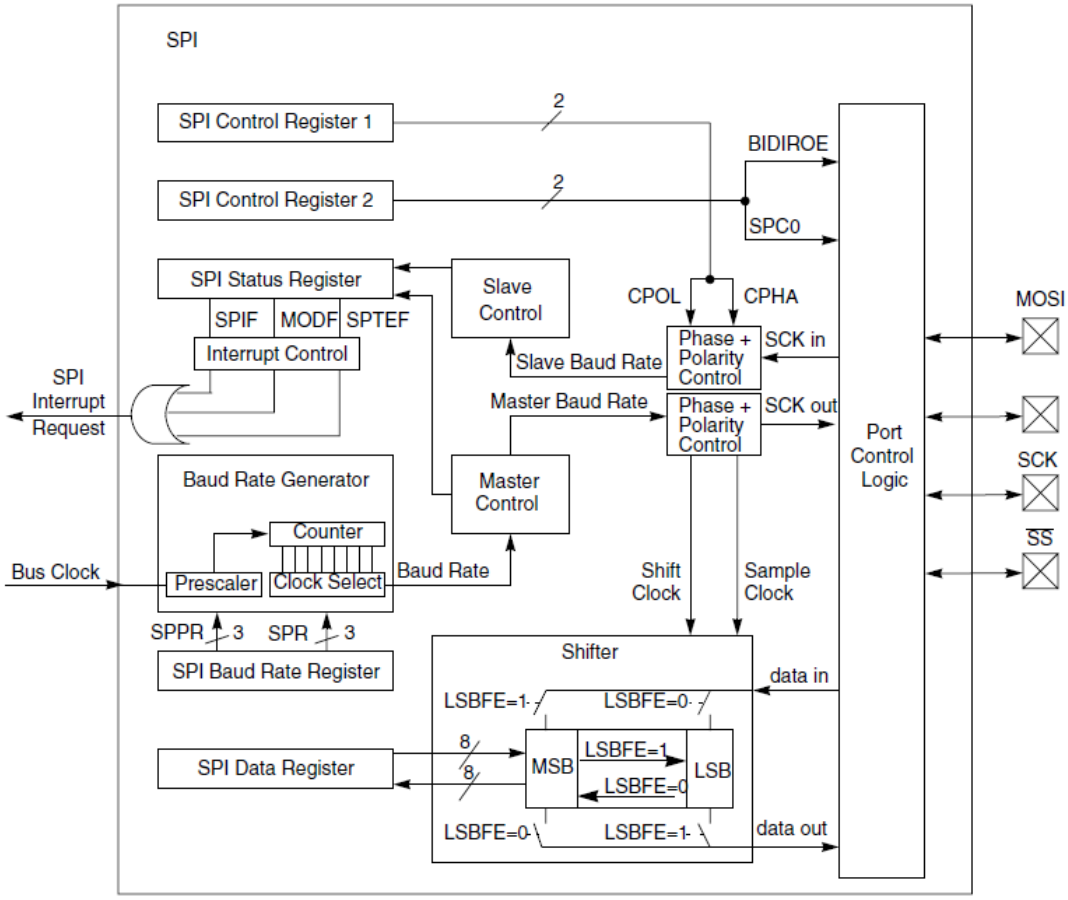

Figure 14-1. SPI Block Diagram

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통신 – SPI [2]

SPI (Serial Peripheral Interface)

During an SPI transmission, data is transmitted (shifted out serially) and received (shifted in serially) simultaneously. The serial clock (SCK) synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows selection of an individual slave SPI device, slave devices that are not selected do not interfere with SPI bus activities. Optionally, on a master SPI device, the slave select line can be used to indicate multiple-master bus contention.

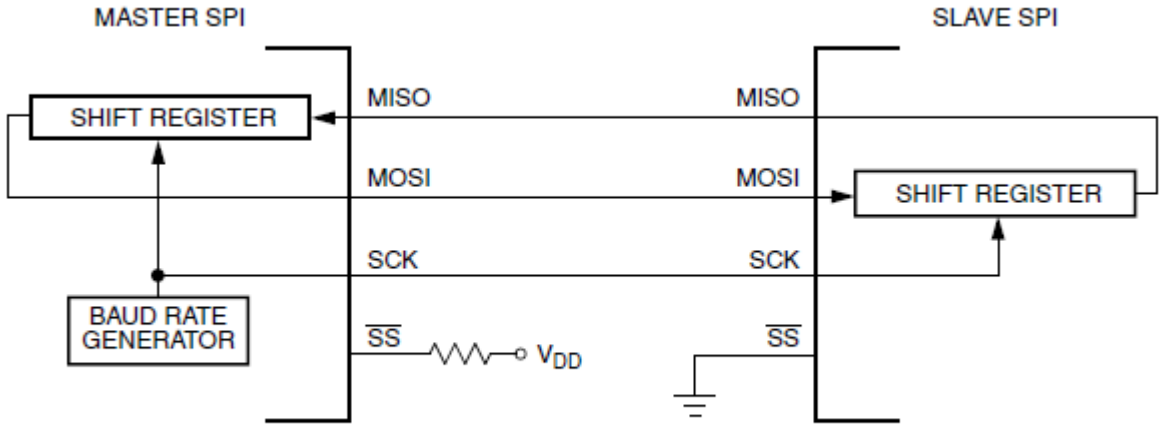

Figure 14-8. Master/Slave Transfer Block Diagram

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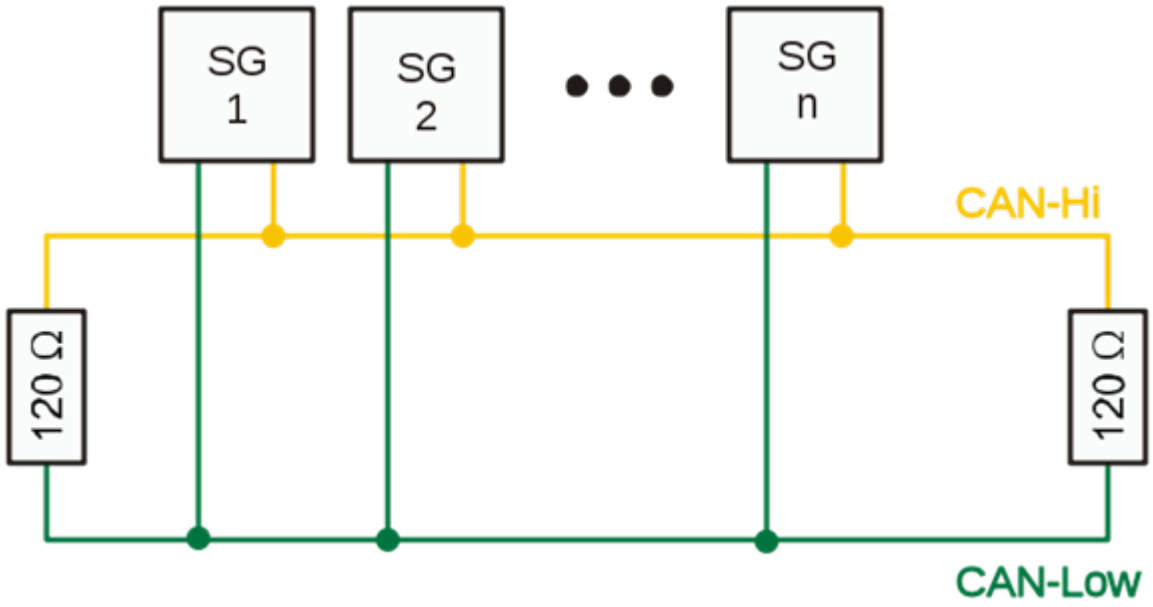
통신 – CAN

CAN (Controller Area Network)

CAN is a **multi-master** broadcast serial bus standard.

Each node is able to send and receive messages, but not simultaneously. A message consists primarily of an **id (identifier)**, which represents the priority of the message, and up to eight data bytes.



http://en.wikipedia.org/wiki/Controller_area_network

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통신 – CAN [2]

CAN (Controller Area Network)

A typical CAN system with MSCAN is shown in Figure 10-2. Each CAN station is connected physically to the CAN bus lines through a **transceiver** device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective stations.

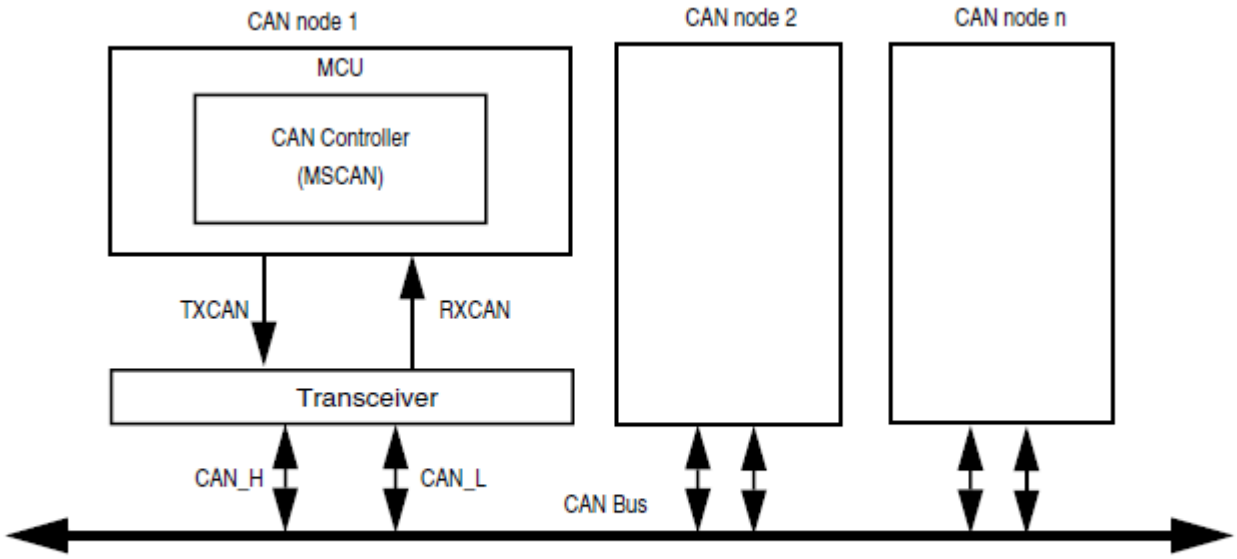

Figure 10-2. CAN System

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통신 – CAN [2]

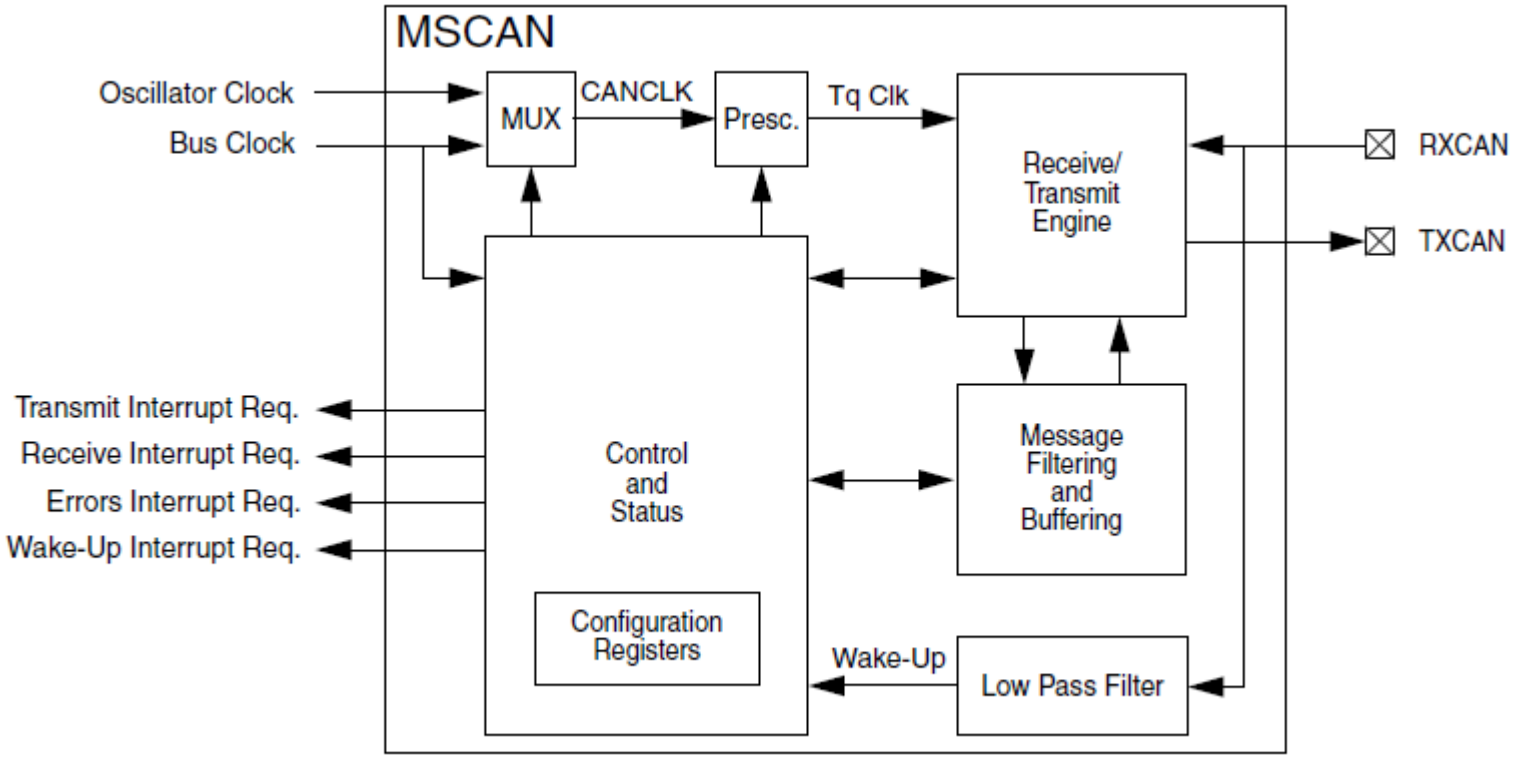

Figure 10-1. MSCAN Block Diagram

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통신 – CAN [2]

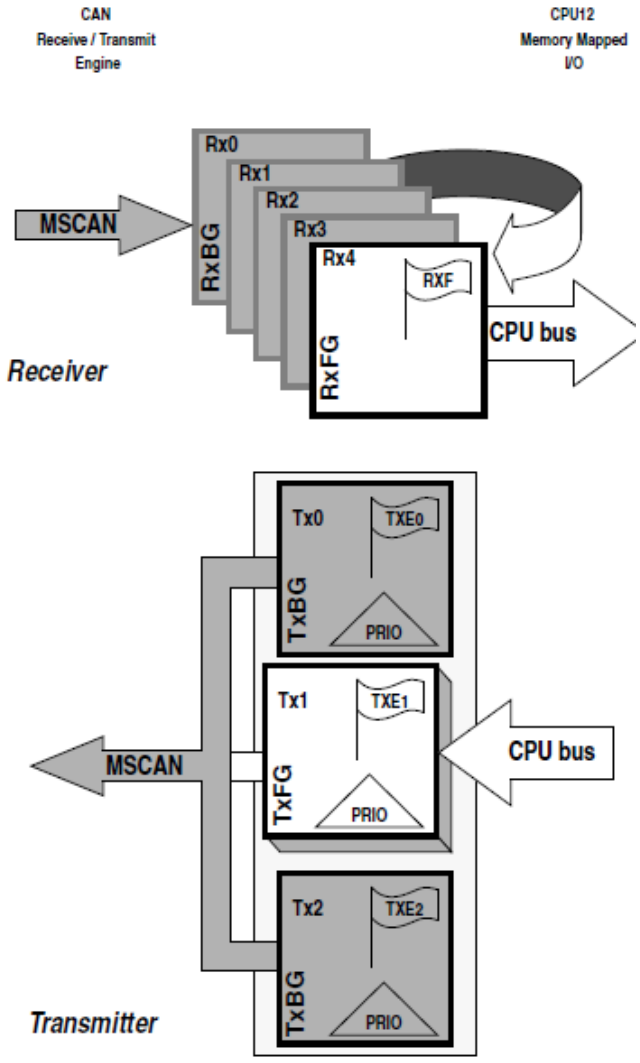

Figure 10-38. User Model for Message Buffer Organization

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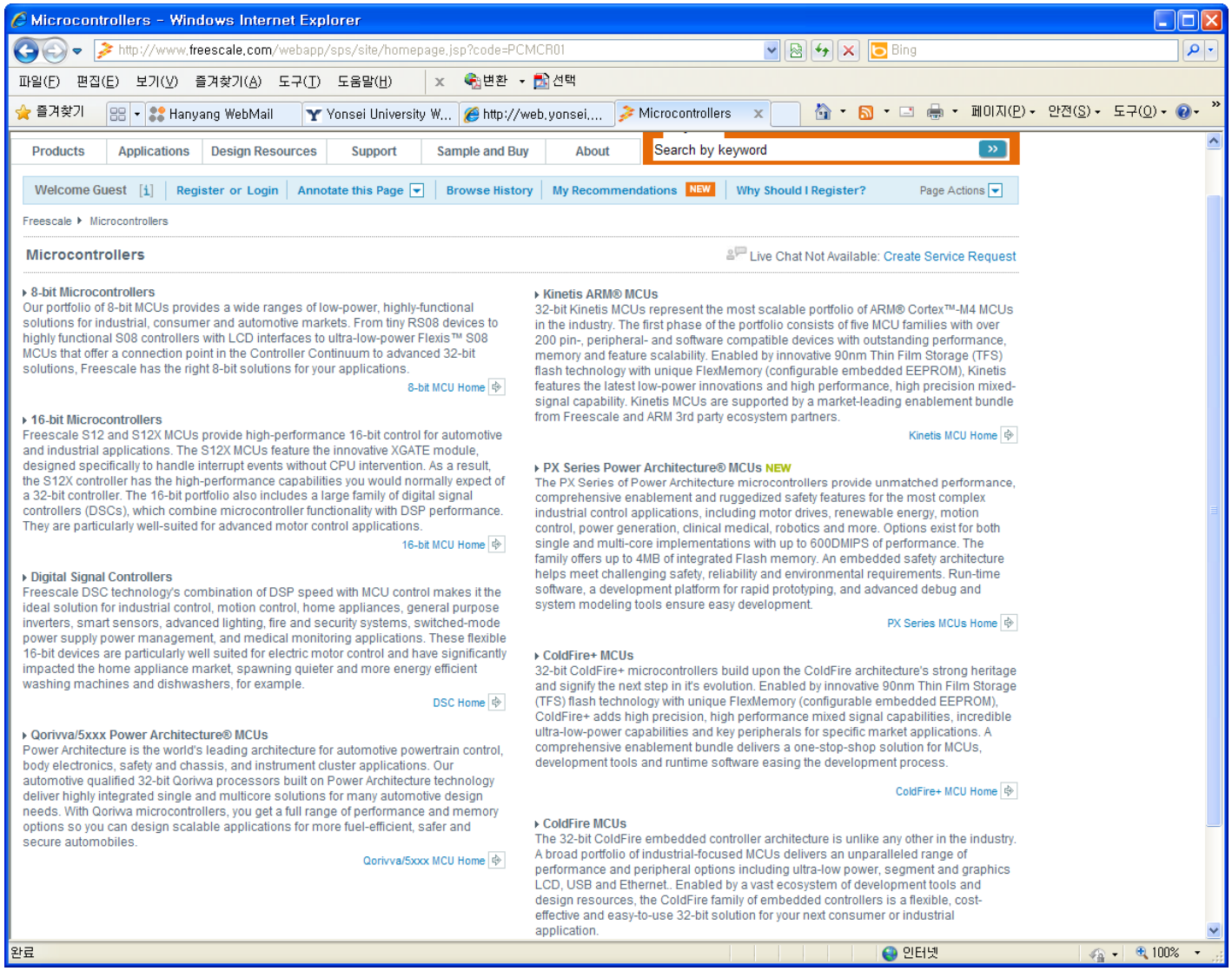

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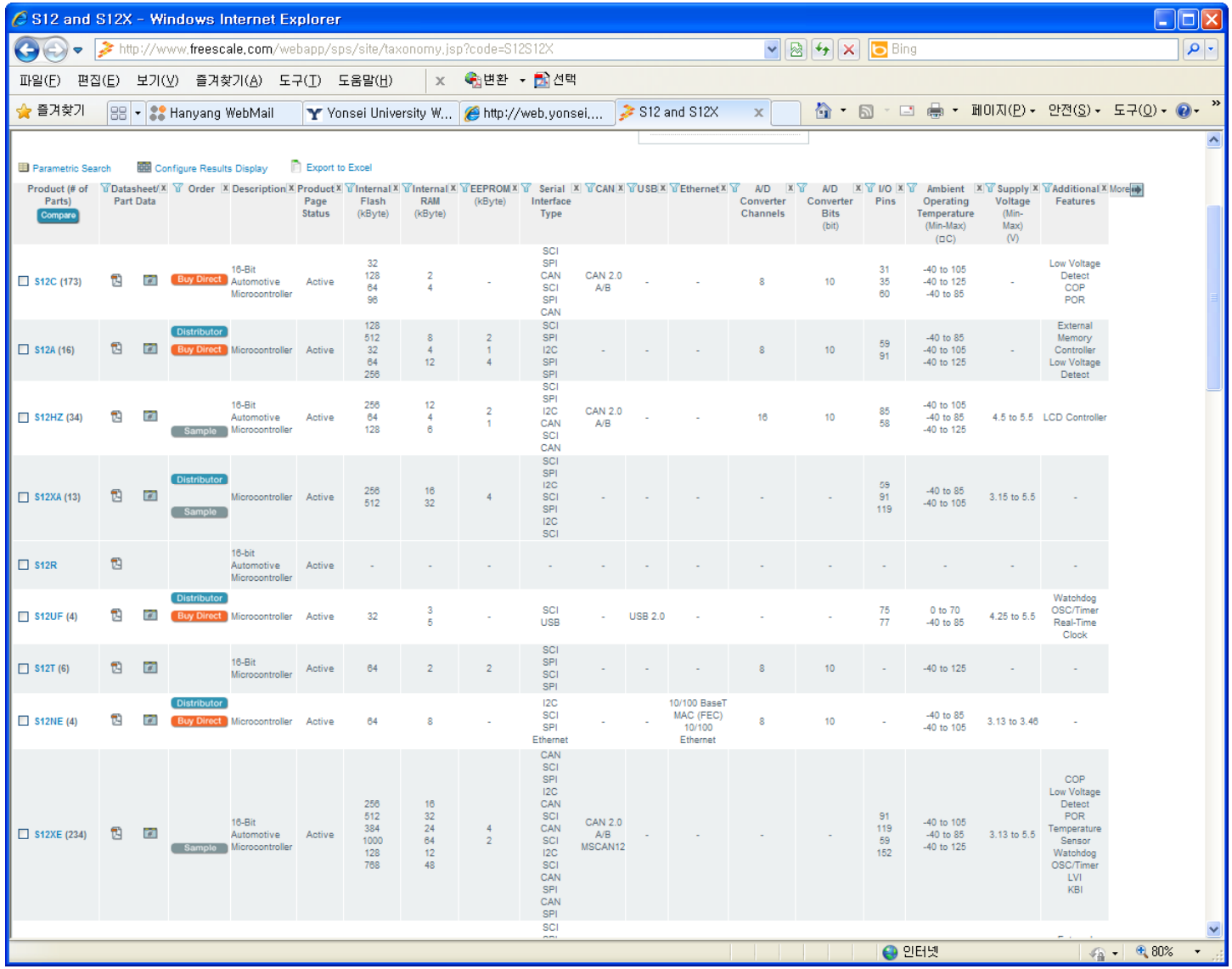
마이크로콘트롤러



Product (# of Parts) Compare	Datasheet/ Part Data	Order	Description	Product Page Status	Internal Flash (kByte)	Internal RAM (kByte)	EEPROM (kByte)	Serial Interface Type	CAN	USB	Ethernet	A/D Converter Channels	A/D Converter Bits (bit)	I/O Pins	Ambient Operating Temperature (Min-Max) (°C)	Supply Voltage (Min-Max) (V)	Additional Features
S12C (173)		Buy Direct	16-Bit Automotive Microcontroller	Active	32 128 64 96	2 4	-	SCI SPI CAN SCI SPI CAN	CAN 2.0 A/B	-	-	8	10	31 35 60	-40 to 105 -40 to 125 -40 to 85	-	Low Voltage Detect COP POR
S12A (16)		Distributor Buy Direct	Microcontroller	Active	128 512 32 64 256	8 4 12	2 1 4	SCI SPI I2C SPI SPI	-	-	-	8	10	59 91	-40 to 85 -40 to 105 -40 to 125	-	External Memory Controller Low Voltage Detect
S12HZ (34)		Sample	16-Bit Automotive Microcontroller	Active	256 64 128	12 4 6	2 1	SCI SPI I2C CAN SCI CAN	CAN 2.0 A/B	-	-	16	10	85 58	-40 to 105 -40 to 85 -40 to 125	4.5 to 5.5	LCD Controller
S12XA (13)		Distributor Sample	Microcontroller	Active	256 512	16 32	4	SCI SPI I2C SCI SPI I2C SCI	-	-	-	-	-	59 91 119	-40 to 85 -40 to 105	3.15 to 5.5	-
S12R			16-bit Automotive Microcontroller	Active	-	-	-	-	-	-	-	-	-	-	-	-	-
S12UF (4)		Distributor Buy Direct	Microcontroller	Active	32	3 5	-	SCI USB	-	USB 2.0	-	-	-	75 77	0 to 70 -40 to 85	4.25 to 5.5	Watchdog OSC/Timer Real-Time Clock
S12T (6)			16-Bit Microcontroller	Active	64	2	2	SCI SPI SCI SPI	-	-	-	8	10	-	-40 to 125	-	-
S12NE (4)		Distributor Buy Direct	Microcontroller	Active	64	8	-	I2C SCI SPI Ethernet	-	-	10/100 BaseT MAC (FEC) 10/100 Ethernet	8	10	-	-40 to 85 -40 to 105	3.13 to 3.46	-
S12XE (234)		Sample	16-Bit Automotive Microcontroller	Active	256 512 384 1000 128 768	16 32 24 64 12 48	4 2	CAN SCI SPI I2C CAN SCI CAN SCI I2C SCI CAN SPI CAN SPI SCI	CAN 2.0 A/B MSCAN12	-	-	-	-	91 119 59 152	-40 to 105 -40 to 85 -40 to 125	3.13 to 5.5	COP Low Voltage Detect POR Temperature Sensor Watchdog OSC/Timer LVI KBI

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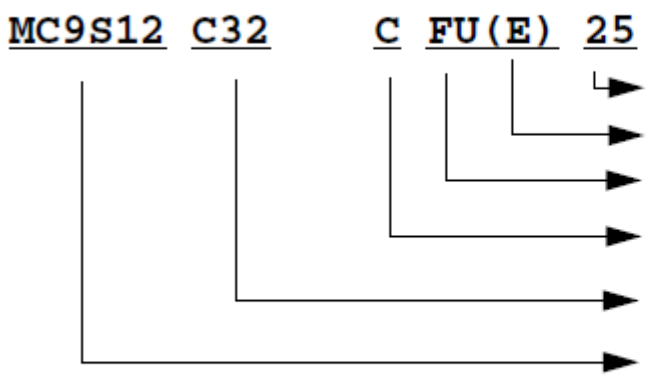
마이크로콘트롤러 [2]

Ordering Information



Temperature Options

C = -40°C to 85°C
V = -40°C to 105°C
M = -40°C to 125°C

Package Options

FU = 80QFP
PB = 52LQFP
FA = 48LQFP

Speed Options

25 = 25MHz bus
16 = 16MHz bus

Environment Option

E = Environmentally Preferred Package

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마이크로콘트롤러 [2]

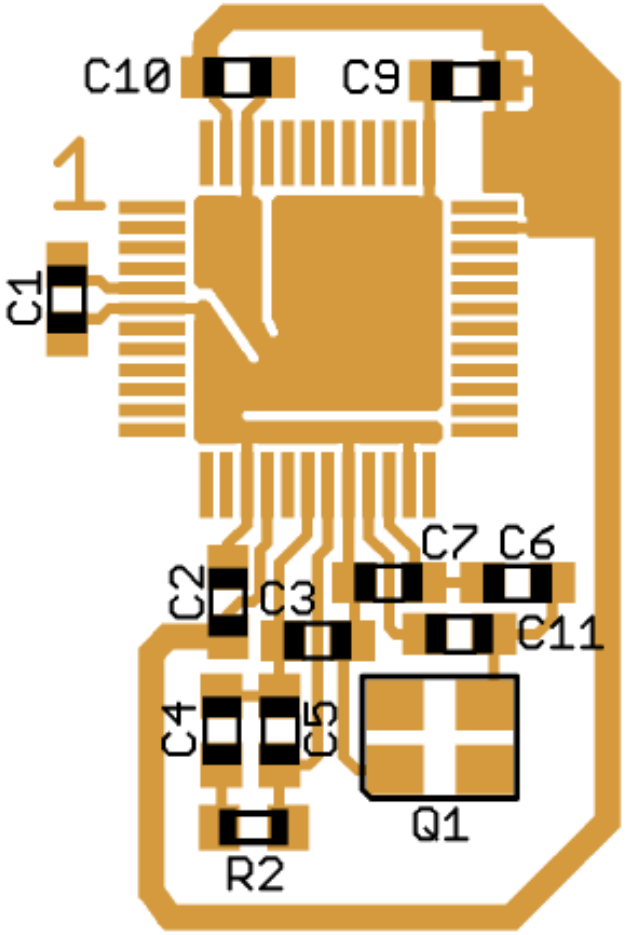

Figure 1-15. Recommended PCB Layout (48 LQFP) Colpitts Oscillator

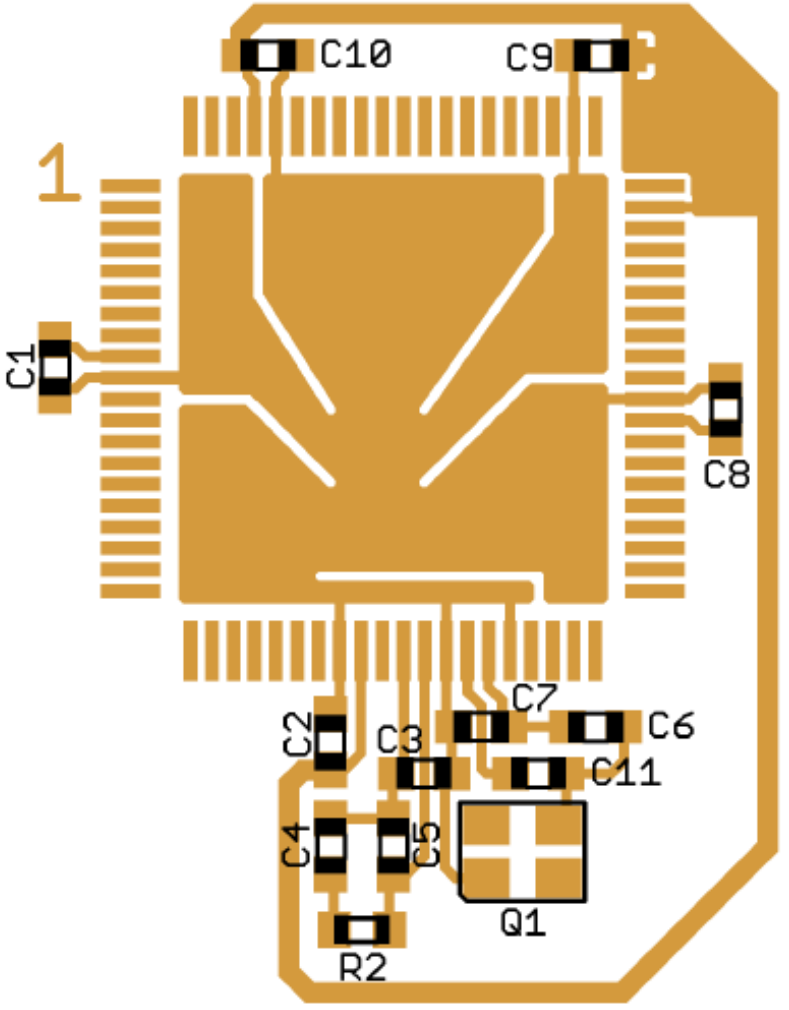

Figure 1-17. Recommended PCB Layout (80 QFP) Colpitts Oscillator

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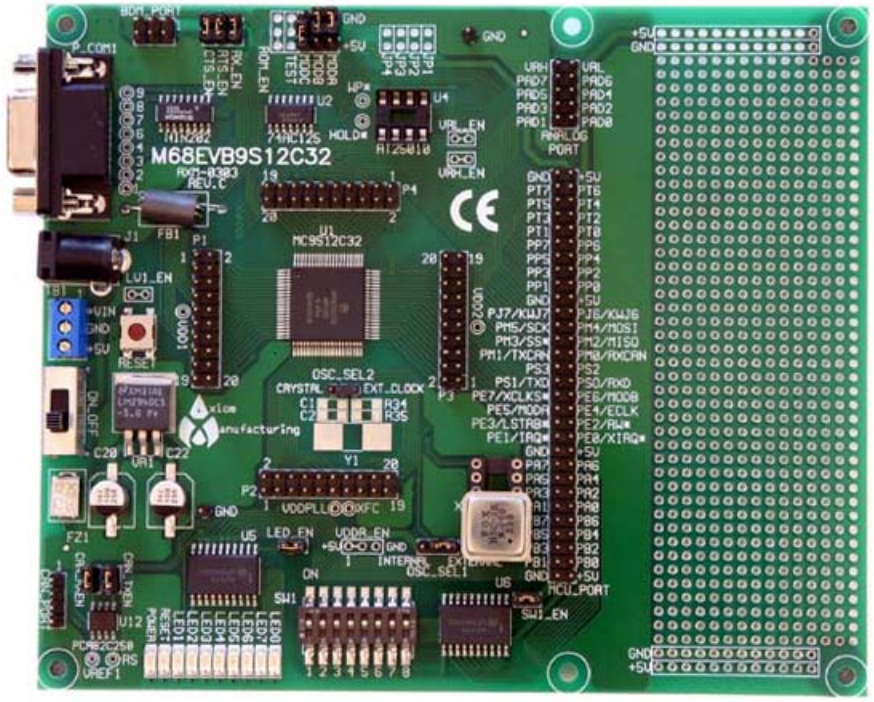
Evaluation Board



M68EVB912C32: MC9S12C32 Evaluation Board (EVB)

Orderable Parts Information

Order Availability	Part Number	Description	Tool Type	Status	Budgetary Price($US)	Compliance: Package Peak Temperature (°C)	Compliance: RoHS	Replacement Part
Buy Direct Distributor	M68EVB912C32EE	Hardware Only EVAL BOARD	Hardware	Active	1 @ $170.00 each	-	RoHS	-

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http://web.yonsei.ac.kr/hgjung

참고자료

1. 노태정 등 공역, "*메카트로닉스 4판*," 사이텍미디어, 2009.
2. Freescale, "S12C: 16-Bit Automotive Microcontroller, Data Sheets," available on http://cache.freescale.com/files/microcontrollers/doc/data_sheet/MC9S12C128V1.pdf?pspll=1

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