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## (54) Title: GENERATION OF SPATIALLY-COUPLED QUASI-CYCLIC LDPC CODES

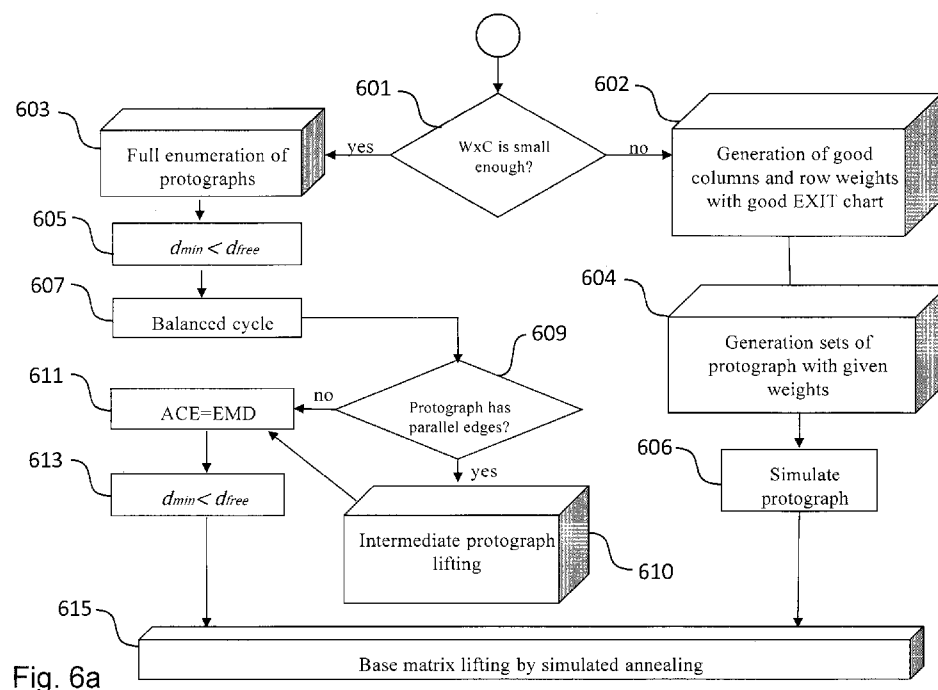


Fig. 6a

(57) **Abstract:** The invention relates to an apparatus (100) for providing at least one parity check matrix defining a spatially-coupled low density parity check, LDPC, code on the basis of a set of base matrix parameters defining a plurality of base matrices, each base matrix of the plurality of base matrices being associated with a protograph of a plurality of protographs, wherein the set of base matrix parameters defines the size  $W \times C$ , a circulant size  $N$ , a maximal column weight  $M$  and a set of allowed column weights of the plurality of base matrices, wherein the apparatus (100) comprises: a processor (101) configured to: generate on the basis of the plurality of protographs a set of candidate protographs by discarding protographs of the plurality of protographs; lift the protographs of the set of candidate protographs for generating a plurality of codes; and generate on the basis of a plurality of codes a set of candidate codes by discarding codes of the plurality of codes, wherein the processor (101) is configured to lift the protographs of the set of candidate





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DESCRIPTION

## GENERATION OF SPATIALLY-COUPLED QUASI-CYCLIC LDPC CODES

5 TECHNICAL FIELD

The present invention relates to the field of channel coding. More specifically, the invention relates to devices and methods for generating a LDPC (low density parity check) code.

10

BACKGROUND

Error-correcting coding is an efficient method of approaching the capacity of a communication system. LDPC codes, which constitute one class of error correcting codes, have been introduced in 1962. Due to the limitation in computational effort in implementing the coder and decoder for such codes and the introduction of Reed-Solomon codes, LDPC codes have been ignored for almost 30 years. During that long period, the only notable work done on the subject was a generalization of LDPC codes and the introduction of a graphical representation of these codes, which is referred to as Tanner graph. Since 1993, with the introduction of turbo codes, researchers switched their focus to finding low complexity codes which can approach the Shannon channel capacity.

It is well known that the performance of randomly constructed irregular LDPC codes closely approach the Shannon limit for the additive white Gaussian noise (AWGN) channel as the code length becomes larger. Moreover, it has been shown that it is possible for irregular LDPC codes with a block length of  $10^7$  to come very close (i.e. 0.0045 dB) to the Shannon capacity.

Although a randomly constructed LDPC code shows a good asymptotic performance, its randomness hinders the ease of analysis and implementation. In attempts towards an algebraic construction of LDPC codes, a quasi-cyclic (QC) LDPC code has been receiving increased attention, because it can be encoded in linear-time with shift registers and a small size of required memory.

With the increasing demand for applications requiring high data rates, many recent communication systems employ ultra-high throughput QC-LDPC codes to match the data-

rate requirements, such as those posed by the next generation or 5G wireless communication systems.

5 Spatially-Coupled LDPC codes show excellent performance under moderate to high lengths and rates as well as simple structures, which reduce the complexity of analysis, design, and hardware implementation for rate and length adapted codes. These properties of SC-LDPC codes offer attractive possibilities for future coding standards.

10 US 2015/0155884 A1 discloses an example of designing a base matrix of a SC-LDPC code using an algebraic approach. More specifically, US 2015/0155884 A1 discloses an algebraic approach for generating a SC-LDPC code on the basis of a multiplicative group using the approach disclosed in R. M. Tanner, D. Sridhara, A. Sridharan, T. E. Fuja and D. J. Costello, "LDPC block and convolutional codes based on circulant matrices," in IEEE Transactions on Information Theory, vol. 50, no. 12, pp. 2966-2984, Dec. 2004.

15 US 8103 931 B2 discloses a method comprising graph lifting of a base matrix using a hill-climbing technique.

In light of the above, there is a need for improved devices and methods for generating LDPC codes.

20

## SUMMARY

It is an object of the invention to provide devices and methods for generating LDPC codes.

25

The foregoing and other objects are achieved by the subject matter of the independent claims. Further implementation forms are apparent from the dependent claims, the description and the figures.

30 According to a first aspect the invention relates to an apparatus for providing at least one parity check matrix defining a spatially-coupled low density parity check, LDPC, code on the basis of a set of base matrix parameters defining a plurality of base matrices, each base matrix of the plurality of base matrices being associated with a protograph of a plurality of protographs, wherein the set of base matrix parameters defines the size  $W \times C$ ,  
35 a circulant size  $N$ , a maximal column weight  $M$  and a set of allowed column weights of the plurality of base matrices, wherein the apparatus comprises: a processor configured to:

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generate on the basis of the plurality of protographs a set of candidate protographs by discarding protographs of the plurality of protographs; lift the protographs of the set of candidate protographs for generating a plurality of codes; and generate on the basis of a plurality of codes a set of candidate codes by discarding codes of the plurality of codes,  
 5 wherein the processor is configured to lift the protographs of the set of candidate protographs on the basis of a simulated annealing technique.

In a first possible implementation form of the apparatus according to the first aspect as such, the processor is configured to discard those protographs of the plurality of  
 10 protographs that are associated with a LDPC code having a minimum Hamming distance that is larger than a minimum Hamming distance threshold value.

In a second possible implementation form of the apparatus according to the first implementation form of the first aspect, the processor is configured to estimate the  
 15 minimum hamming distance of a LDPC code C on the basis of the upper bound defined by the following equation:

$$d_{\min}(C(H)) \leq \min_{\substack{s \subseteq [W] \\ |s|=C+1}}^+ \sum_{i \in s} perm(A_{s \setminus i})$$

20 wherein  
 [W] denotes the set of numbers from [0 ... W - 1],  
 the operator  $\min^+(\dots)$  defines the minimal positive value of its argument, and  
 the permanent operator  $perm(\dots)$  is defined by the following equation:

25 
$$perm(B) = \sum_{\sigma} \prod_{j \in [m]} b_{j, \sigma(j)}$$

wherein

B is a  $m \times m$  matrix having elements  $b_{j, \sigma(j)}$  and  
 $\sigma$  takes all  $m!$  possible permutations of the set [m].

30 In a third possible implementation form of the apparatus according to the first or second implementation form of the first aspect, the minimum Hamming distance threshold value is  $(C+1)!$ .

In a fourth possible implementation form of the apparatus according to the first aspect as such or any one of the first to third implementation form thereof, the processor is further configured to discard protographs of the plurality of protographs on the basis of the balanced girth of the parity check matrix  $H$  associated with each protograph.

5

In a fifth possible implementation form of the apparatus according to the fourth implementation form of the first aspect, the processor is configured to discard those protographs from the plurality of protographs that are associated with a parity check matrix  $H$  having a balanced girth which is larger than a balanced girth threshold value.

10

In a sixth possible implementation form of the apparatus according to the first aspect as such or any one of the first to fifth implementation form thereof, the processor is further configured to lift a protograph of the plurality of protographs having at least one parallel edge to a protograph having no parallel edges.

15

In a seventh possible implementation form of the apparatus according to the first aspect as such or any one of the first to sixth implementation form thereof, the processor is further configured to discard those protographs of the plurality of protographs that are associated with an extrinsic message degree (EMD) that is smaller than an EMD threshold value.

20

According to a second aspect the invention relates to a corresponding method for providing at least one parity check matrix defining a spatially-coupled low density parity check, LDPC, code on the basis of a set of base matrix parameters defining a plurality of  
25 base matrices, each base matrix of the plurality of base matrices being associated with a protograph of a plurality of protographs, wherein the set of base matrix parameters defines the size  $W \times C$ , a circulant size  $N$ , a maximal column weight  $M$  and a set of allowed column weights of the plurality of base matrices, wherein the method comprises the steps of: generating on the basis of the plurality of protographs a set of candidate protographs  
30 by discarding protographs of the plurality of protographs; lifting the protographs of the set of candidate protographs for generating a plurality of codes; and generating on the basis of a plurality of codes a set of candidate codes by discarding codes of the plurality of codes, wherein the step of lifting the protographs of the set of candidate protographs is based on a simulated annealing technique.

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The method according to the second aspect of the invention can be performed by the apparatus according to the first aspect of the invention. Further features of the method according to the second aspect of the invention result directly from the functionality of the apparatus according to the first aspect of the invention and its different implementation forms.

According to a third aspect the invention relates to a computer program comprising program code for performing the method according to the second aspect of the invention when executed on a computer.

10

The invention can be implemented in hardware and/or software.

#### BRIEF DESCRIPTION OF THE DRAWINGS

15 Further embodiments of the invention will be described with respect to the following figures, wherein:

Fig. 1 shows a schematic diagram illustrating an apparatus for generating a LDPC code according to an embodiment;

20

Fig. 2 shows a schematic diagram illustrating an exemplary block of circulants shifted by two different values;

Fig. 3 shows a schematic diagram illustrating an exemplary spatially coupled parity-check matrix represented by blocks of circulants;

25

Fig. 4 shows a schematic diagram of exemplary blocks of circulant permutation matrices and spatially coupled blocks of circulant permutation matrices;

30 Fig. 5 shows a schematic diagram of an exemplary protograph having a trapping set;

Fig. 6a shows a schematic diagram illustrating a protograph selection or optimization stage of the code generation according to an embodiment;

35 Fig. 6b shows a schematic diagram illustrating a protograph lifting optimization stage of the code generation according to an embodiment;

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Fig. 7 shows a schematic diagram illustrating two exemplary protographs with two cycles having the same ACE value and different EMD values;

5 Fig. 8a shows a schematic diagram illustrating an exemplary cycle in a protograph having a left edge intersecting shifted zone;

Fig. 8b shows a schematic diagram illustrating an exemplary cycle in a protograph having no closed cycle in the spatially coupled graph;

10 Fig. 9 shows a schematic diagram illustrating an exemplary 4VN subgraph of a protograph;

Fig. 10a shows a diagram illustrating the performance of codes provided by embodiments of the invention in comparison with conventional codes;

15 Fig. 10b shows a diagram illustrating the performance of codes provided by embodiments of the invention in comparison with conventional codes;

Fig. 11a shows a diagram illustrating the performance of codes provided by embodiments of the invention in comparison with conventional codes; and

20 Fig. 11b shows a diagram illustrating the performance of codes provided by embodiments of the invention in comparison with conventional codes.

25 In the various figures, identical reference signs will be used for identical or at least functionally equivalent features.

#### DETAILED DESCRIPTION OF EMBODIMENTS

30 In the following description, reference is made to the accompanying drawings, which form part of the disclosure, and in which are shown, by way of illustration, specific aspects in which the present invention may be placed. It is understood that other aspects may be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following detailed description, therefore, is not to be taken in  
35 a limiting sense, as the scope of the present invention is defined by the appended claims.



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For instance, it is understood that a disclosure in connection with a described method may also hold true for a corresponding device or system configured to perform the method and vice versa. For example, if a specific method step is described, a corresponding device may include a unit to perform the described method step, even if such unit is not explicitly described or illustrated in the figures. Further, it is understood that the features of the various exemplary aspects described herein may be combined with each other, unless specifically noted otherwise.

Figure 1 shows a schematic diagram illustrating an apparatus 100 for providing a parity check matrix defining a spatially-coupled low density parity check, LDPC, code on the basis of a base matrix defining a quasi-cyclic LDPC code. The apparatus 100 comprises a processor 101 configured to: generate on the basis of a plurality of protographs associated with the base matrix a set of candidate protographs by discarding protographs of the plurality of protographs; lift the protographs of the set of candidate protographs for generating a plurality of codes; and generate on the basis of a plurality of codes a set of candidate codes by discarding codes of the plurality of codes.

The processor 101 is configured to lift the protographs of the set of candidate protographs on the basis of a simulated annealing technique, as will be described in more detail further below.

Before describing some further details of the apparatus 100 shown in figure 1 and different embodiments thereof, the following "background material" is provided for a better understanding of different embodiments of the apparatus 100.

A  $(W, C, N, L)$  tail-bitten spatially-coupled QC-LDPC code  $\mathcal{C}(H)$  of length  $W$  multiple  $L$  multiple  $N$  (i.e. if the circulant size is  $N \times N$  with  $W$  circulants coupled  $L$  times) can be defined by a parity-check base matrix  $H$  in the following way:

$$H = \begin{bmatrix} A_{0,0} & A_{1,0} & \dots & A_{WL-1,0} \\ A_{0,1} & A_{1,1} & & A_{WL-1,1} \\ \vdots & \vdots & \ddots & \vdots \\ A_{0,CL-1} & A_{1,CL-1} & \dots & A_{WL-1,CL-1} \end{bmatrix} \quad (1)$$

wherein  $0 \leq i \leq CL - 1$ ,  $1 \leq j \leq WL - 1$  and a circulant permutation matrix (CPM)  $A_{i,j}$  represents either the  $N \times N$  zero matrix  $Z$  or the  $N \times N$  circulant permutation matrix

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$I(p_{i,j})$  obtained by cyclically right-shifting the  $N \times N$  identity matrix  $I(0)$  by  $p_{i,j}$  positions. Denote by CPM-column the  $i$ -th column of  $A_{0,i}, A_{1,i}, \dots, A_{CL-1,i}$ . In a similar way define CPM-row.

- 5 For a specific tail-bitten spatially-coupled QC-LDPC code the corresponding CPM-shifts matrix can be defined as the matrix of circulant shifts that defines the QC-LDPC code, i.e.:

$$B = \begin{bmatrix} b_{0,0} & b_{1,0} & \dots & b_{W-1,0} \\ b_{0,1} & b_{1,1} & & b_{W-1,1} \\ \vdots & \vdots & \ddots & \vdots \\ b_{0,C-1} & b_{1,C-1} & \dots & b_{W-1,C-1} \end{bmatrix} \quad (2)$$

- 10 The corresponding shifts can be represented as a vector  $D$  of shifts:

$$D = \begin{bmatrix} d_0 \\ d_1 \\ \vdots \\ d_{C-1} \end{bmatrix} \quad (3)$$

with the conditions  $d_0 = 0, d_i < d_j$  iff  $i < j, \forall i d_i < W$ . If  $\frac{W}{C}$  is an integer, the vector  $D$  can be defined as  $d_i = \frac{iW}{C}$ .

15

For  $0 \leq i \leq CL-1, 0 \leq j \leq WL-1$ , if

$$i' \bmod WL \leq i < (i' + W) \bmod WL$$

then  $A_{i,j} = I(b_{i \bmod W, j \bmod C})$  else  $A_{i,j} = Z$ .

- 20 The above definitions are further illustrated by figures 2 to 4. Figure 2 shows a schematic diagram illustrating an exemplary block of circulants shifted by two different values. Figure 3 shows a schematic diagram illustrating a spatial coupled parity-check matrix represented by blocks of circulants. Figure 4 shows a schematic diagram of a blocks of circulant permutation matrices and spatially coupled blocks of circulant permutation  
25 matrices.

There is a more general case of parity check matrices, where one circulant permutation matrix can have more than one diagonal.

A weight matrix (or protograph)  $\text{wt}(H)$  of a matrix  $H$  is a matrix of number of diagonals for each circulant of  $H$ .

5 A type  $M$  of the matrix  $H$  is a maximal value of the matrix  $\text{wt}(H)$ .

Given a protograph matrix  $H$  of type  $M > 1$ , a matrix with circulant size equal to  $M$  can be generated. Choosing in each circulant the number of diagonals equal to corresponding weight, the result can be considered as a new protograph matrix  $H'$ . The type of the new  
10 protograph matrix  $H'$  is 1, and most properties of  $H'$  will remain the same as for  $H$ . Thus, without loss of generality only protograph matrices of type 1 can be considered, when it is necessary.

There is isomorphism between the ring of circulant permutation matrices over some field  $F$   
15 and the ring  $F$ -polynomials modulo  $x^N - 1$ , where  $N$  is the size of the circulant. For example  $I(0)$  can be represented as  $x^0$ ,  $I(5)$  as  $x^5$ , and  $I(0) + I(1) + I(4)$  as  $x^0 + x^1 + x^4$ .

A very important characteristic of a parity check matrix is the girth of its Tanner graph,  
20 which is defined as the minimal length of a cycle of the Tanner graph of a parity check matrix. A cycle in a Tanner graph can be defined in the following way: ...

Cycle of even length  $2K$  in  $H$  defined by  $2K$  positions of ones such that:

- 1) Two consecutive positions are obtained by changing alternatively column of row  
25 only;
- 2) All positions are distinct except first and last one;

Two consecutive elements of the path belong to different circulant permutation matrices. Thus, a chain of circulant permutation matrices can be defined as follows:

30

$$A_{i_0, j_0}, A_{i_0, j_1}, A_{i_1, j_1}, A_{i_1, j_2}, \dots, A_{i_{K-1}, j_{K-1}}, A_{i_{K-1}, j_0}, A_{i_0, j_0},$$

where  $i_a \neq i_{a+1}, j_a \neq j_{a+1}$ , for all  $0 \leq a \leq K - 1$ .

35 As each part of a cycle is one, a circulant permutation matrix  $A_{i,j}$  participating in the cycle cannot be empty. In other words,  $A_{i,j} = I(p_{i,j})$ .

Using these shifts of the identity matrix the necessary and sufficient conditions for the existence of the cycle can be expressed as follows:

$$\sum_{a=0}^{K-1} p_{i_a, j_a} - p_{i_a, j_{a+1}} \equiv 0 \pmod{N} \quad (4)$$

The Tanner graph  $T(H)$  of a parity check matrix  $H$  is a bipartite graph with two set of vertices, referred to as variable nodes  $V = \{v_0, v_1, \dots, v_{n-1}\}$  and check nodes  $C = \{c_0, c_1, \dots, c_{n-1}\}$ . The columns of the matrix  $H$  correspond to the variable nodes, and the rows thereof to the check nodes. There is an edge between a variable node  $v_i$  and a check node  $c_j$ , if and only if the cell of  $H$  at the  $i$ -th column and the  $j$ -th row is nonzero.

A trapping set  $T$  of type  $(T_1, T_2)$  is a connected subgraph of a Tanner graph, including  $T_1$  variable nodes, where  $T_2$  check nodes are connected with the trapping set  $T$  by an odd number of edges.

Simultaneously altering values of  $T_1$  variable nodes and  $T_2$  check nodes gives correct result. It means that wrong bit in  $T_2$  check nodes gives wrong decoding of  $T_1$  variable nodes. A small value of  $T_2$  gives bad trapping sets, as it is more easy to make mistakes in a small number of nodes. Trapping sets with bigger value of  $T_2$  are worse as more informational bits are wrong. Differently put, if wrong bit place to variable nodes incident to odd degree check node, then BP decoder most commonly fails due to this error (even if the code distance is greater than this number error). The graph properties are the reason for this error.

Figure 5 shows a schematic diagram of an exemplary protograph having a trapping set.

Figure 6a shows a schematic diagram illustrating a protograph selection or optimization stage of the code generation provided by the apparatus 100 according to an embodiment.

Figure 6b shows a schematic diagram illustrating a protograph lifting stage and subsequent code selection stage of the code generation provided by the apparatus 100 according to an embodiment.

In an embodiment, the input of the code generation stages shown in figures 6a and 6b are the parameters of a base matrix, namely its size  $W \times C$  (e.g.  $32 \times 16$ ), a circulant size  $N$ , a

maximal column weight  $M$  and a set of allowed column weights. As will be explained in more detail below, the final output of the code generation stages shown in figures 6a and 6b is a set of selected parity check matrices providing good LDPC codes.

- 5 The code generation stages shown in figures 6a and 6b comprises generator blocks (indicated as three-dimensional processing blocks in figures 6a and 6b) and filter or selection blocks (indicated as two-dimensional processing blocks in figures 6a and 6b). Each generator block is configured to generate either a protograph or a parity check matrix (based on the given protograph). Each filter or selection block filters its input in  
10 some way and, thereby, performs a selection operation on the basis of its input.

The first stage shown in figure 6a illustrates two branches, namely a first branch which generates protographs in processing block 603, when the input base matrix is smaller than a predefined threshold (i.e. when the search is not too complex) and a second  
15 branch which comprises processing blocks 602, 604 and 606, when the base matrix is larger than a predefined threshold (for example, for estimating an upper bound on the code distance it is necessary to enumerate  $1.1826e+17$  permanents for a base matrix  $30 \times 60$  and permanents of size  $30 \times 30$ ).

- 20 In the following several of the processing blocks shown in figures 6a and 6b and implemented in an embodiment of the apparatus 100 will be described in more detail.

In the processing step 603, the processor 101 of the apparatus 100 is configured to consider possible protograph matrices for a given length  $N$  and rate  $K/N$ . If  $K$  and  $N$  are  
25 not too large enough, the processor 101 can enumerate all protographs.

In an embodiment, the processor 101 is configured to estimate in the next processing step 605 the quality of a QC-LDPC code based on a protograph  $A$  by estimating the minimum Hamming distance of the code.

30

The permanent of the  $m \times m$  base matrix  $B$  is

$$\text{perm}(B) = \sum_{\sigma} \prod_{j \in [m]} b_{j, \sigma(j)}$$

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where  $\sigma$  takes all  $m!$  possible permutations of the set  $[m]$ . The function  $\min^+(\cdot)$  denotes minimal positive value and  $[W]$  denotes the set of numbers from  $[0 \dots W - 1]$ . Then, the upper bound  $d_{min}$  for QC code  $C(H)$  with polynomial parity-check matrix can be expressed in the following way:

5

$$d_{min}(C(H)) \leq \min_{\substack{s \subseteq [W] \\ |s|=C+1}} \sum_{i \in s} \min^+ perm(A_{s \setminus i}) \quad (5)$$

According to an embodiment, the processor 101 is configured to further process a code if the upper bound  $d_{min}$  is not less than  $(C+1)!$  in the processing block 605. In other words, in the processing block 605 the processor 101 is configured to discard photographs or corresponding codes with an upper bound  $d_{min}$  being smaller than  $(C+1)!$ .

10

The following example illustrates the use of equation (5), as applied by the processor 101 in embodiments of the invention. Consider two (2,4) regular length-4r QC codes, namely a first code  $C(H_1)$  with parity check matrix

15

$$H_1(x) = \begin{pmatrix} x & x^2 & x^4 & x^8 \\ x^5 & x^6 & x^3 & x^7 \end{pmatrix},$$

and a second code  $C(H_2)$  with parity check matrix

20

$$H_2(x) = \begin{pmatrix} x & x^2 & x^4 & x^8 \\ x^6 & x^5 & x^3 & x^9 \end{pmatrix}.$$

For both codes equation (5) provides:

25

$$d_{min} \leq \min^+\{(1 + 1) + (1 + 1) + (1 + 1)\} = 6$$

$$\sum_{a=0}^{K-1} p_{i_a, j_a} - p_{i_a, j_{a+1}} \equiv 0 \pmod{N} \quad (4)$$

30

In above equation (4) each coefficient  $p_{i,j}$  for the CPM  $A_{i,j}$  adds with plus for each even step and with minus for each odd steps. If the number of even steps for the CPM  $A_{i,j}$  equals the number of odd steps, then  $p_{i,j}$  can be eliminated from above equation (4).

A balanced cycle on the parity check matrix  $H$  is the cycle where each cell participates the same number of times in even steps and in odd steps. For a balanced cycle above equation (4) reduces to the trivial equality  $0 \equiv 0$ , which holds for any values of coefficients  $p_{i,j}$ .

5

In the processing block 607 the processor 101 is configured to estimate the minimal length of the balanced cycle for each protograph candidate.

10

The balanced girth is defined as the minimal length of the balanced cycle. The actual girth cannot be larger than the balanced girth of a parity check matrix  $H$  for any shifts of circulant permutation matrices. For this reason, the balanced girth is an important upper bound for the girth of a protograph, as implemented in embodiments of the invention.

15

In the following, a pseudo code for estimating the balanced girth of the parity check matrix  $H$  will be described, as implemented in embodiments of the invention. Here,  $K$  denotes a pre-defined constant. This pre-defined constant can be selected as a trade-off. After a certain value of balance cycle, the code distance can become too bad. Thus, the pre-defined constant can be selected as the point, where the cycle is enough to prevent performance degradation by TS and code distance.

20

Enumerate all closed cycles with length shorter than given  $K$ , going through non-empty protograph cells, with vertical lines on even steps, and horizontal lines on odd steps.

25

1. For each cycle from enumeration calculate whether this cycle is balanced or not.

- a. For each cell of the cycle calculate difference between the appearance after even and after odd steps.
- b. The cycle is balanced, if and only if all differences are zero.

30

2. Return minimal length of the balanced cycle.

35

In processing block 609, the processor 101 is configured to determine for each candidate protograph, whether the protograph has parallel edges. If this is the case, the processor 101 is configured to lift in processing block 610 a corresponding candidate protograph  $A$  having some parallel edges to a bigger protograph without parallel edges using a quasi-

cyclic technique. For a protograph of type K, the minimal possible value of the circulant size K is chosen and changed for each.

In processing block 611, the processor 101 is configured to discard protographs having a small Extrinsic Message Degree (EMD), i.e. an EMD smaller than a predefined threshold. The EMD of a cycle in the Tanner graph is defined as the number of check nodes singly connected to the variable nodes involved in the cycle. The EMD value of a code is an important characteristic, because each cycle  $C_{2n}$  of length  $2n$  is a trapping set  $(n, EMD(C_{2n}))$ .

The Approximate Cycle EMD (ACE) is defined as the number of incident edges not included in the cycle. For a cycle  $C_{2n}$  of length  $2n$  the following relation holds

$$\sum_{k=1}^{2n} ACE(C_{2n}) = (d_{v_k} - 2),$$

where  $d_{v_k}$  denotes the degree of k-th variable node.

Figure 7 shows a schematic diagram illustrating two protographs with two cycles having the same ACE value, namely ACE=5, and different EMD values, namely EMD=5 for the protograph on the left and EMD=3 for the protograph on the right.

The ACE spectrum  $\mu_{ACE} = (\mu_2, \mu_4, \dots, \mu_{d_{ACE}})$  of a Tanner graph is defined as the set of minimum ACE values of a given length range from 2 up to  $d_{ACE}$  of the graph. If there are no cycles of length k, then  $\mu_k = \infty$ .

It has been shown that the ACE and the EMD value(s) can be related in the following ways.

First, for a code with a girth g the following relation holds for a cycle  $C_k$  having a length  $k < 2g - 4$ :  $ACE(C_k) = EMD(C_k)$ .

Second, for a code with the girth g and the ACE spectrum  $\mu_{ACE} = (\mu_2, \mu_4, \dots, \mu_{d_{ACE}})$ ,  $ACE(C_k)$  of the cycle  $C_k$  of length k,  $k \geq 2g - 4$  is equal to  $EMD(C_k)$  if

$$ACE(C_k) < \min_{j \in \{g, g+2, \dots, k+4-g\}} \frac{\mu_j + \mu_{k-j+4}}{2}$$



These relations between the ACE and the EMD are illustrated by the following examples.

For a LDPC code of girth 12, all the cycles of length 12, 14, 16 and 18 have equal ACE  
5 and EMD.

For a LDPC code with ACE spectrum  $(\infty, \infty, 15, 11, 16)$  all the cycles of length 8 with the ACE value less than 13 will have equal ACE and EMD.

10 For all cycles of length 10 and ACE value less than  $13 = \frac{15+11}{2}$ .

In an embodiment, the processor 101 is configured to make use of one or more of the above relations between the ACE and the EMD in the processing block 611 for a fast evaluation of the EMD for cycles in protographs. This, in turn, allows the processor 101 to  
15 estimate the number of trapping sets and, thus, the quality of a protograph in the processing block 611.

In an embodiment, for a given protograph the following assumptions are made: non-existence of cycles and hence a Gaussian distribution for LLR on the belief propagation  
20 algorithm. On the basis of these assumptions the decoding threshold of an ensemble of protographs characterized by a given distribution of variable nodes and check nodes can be calculated, as implemented in embodiments of the present invention.

We plot chart of two EXIT functions  $I_{E,V}$  and  $I_{E,C}$ .  
25

The step function shows the growth of the information obtained by the belief propagation algorithm. If the EXIT functions are not intersecting, the belief propagation algorithm can be terminated. The decoding threshold can be defined as the value of the noise, when the two EXIT functions touch each other. The two EXIT functions  $I_{E,V}$  and  $I_{E,C}$  can be  
30 expressed in the following way:

$$I_{E,V} = J(\sigma) = J\left(\sqrt{(d_v - 1)\sigma_A^2 + \sigma_{ch}^2}\right)$$

$$J(\sigma) = 1 - \int_{-\infty}^{\infty} \frac{1}{\sqrt{2\pi}\sigma} e^{-(l - \frac{\sigma^2}{2})^2 / 2\sigma^2} \log(1 + e^{-l}) dl$$

$$I_{A,V} = J(\sigma_A)$$

$$I_{E,V} = J(\sigma) = J\left(\sqrt{(d_v - 1)[J^{-1}(I_{A,V})]^2 + \sigma_{ch}^2}\right).$$

In an embodiment, the following approximation can be used for  $I_{E,C}$ :

5

$$I_{E,C} = 1 - J\left(\sqrt{(d_c - 1)[J^{-1}(1 - I_{A,C})]^2}\right).$$

For irregular LDPC codes  $I_{E,V}$  and  $I_{E,C}$  can be calculated as weighted averages, as implemented in an embodiment of the invention.

10

In an embodiment, the weighting is given by the coefficients of the edge degree distribution polynomials  $\lambda(z) = \sum_{d=1}^{d_v} \lambda_d z^{d-1}$  and  $\rho(z) = \sum_{d=1}^{d_c} \rho_d z^{d-1}$ , where  $\lambda_d$  is the fraction of ones in the columns in the protograph with  $d$  ones in the column, and  $\rho_d$  is the fraction of ones in the rows in the protograph with  $d$  ones in the row. For irregular LDPC

15

codes this results in:

$$I_{E,V} = \sum_{d=1}^{d_v} \lambda_d I_{E,V}(d, I_{A,V})$$

$$I_{E,C} = \sum_{d=1}^{d_c} \rho_d I_{E,C}(d, I_{A,C})$$

20

In an embodiment, a pre-calculated approximation function  $J(\cdot)$  can be used having an accuracy of, for instance, better than  $10^{-5}$ .

On the basis of the weighted functions  $I_{E,V}(d, I_{A,V})$  and  $I_{E,C}(d, I_{A,C})$  the processor 101 can be configured to calculate the following iterations:

25

$$I_{A,V}^{(0)} = 0$$

$$I_{A,V}^{(n+1)} = I_{E,C}(d, I_{E,V}(d, I_{A,V}^{(n)}))$$

In an embodiment, the processor 101 is configured to stop the iteration, when  $I_{A,V}^{(n)}$  is close to 1.

30

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For each distribution of weights  $\lambda_d, \rho_d$  the minimal  $\frac{E_b}{N_0}$  (based on  $\sigma_A^2$ ) is calculated, when the iteration converges to 1 for a fixed number of steps.

Using EXIT charts, i.e. graphical representations of the exit functions, good distributions  
 5  $\lambda_d, \rho_d$  can be generated and thereafter protographs with given distributions of ones in rows and columns can be created, as implemented in embodiments of the invention and as will be described in more detail in the following.

For each value of  $\lambda_d$  the processor 101 is configured to generate a set of all possible  
 10 columns, which provides this value  $\lambda_d$ . In an embodiment, parallel edges in the protograph are allowed, i.e. a cell can not only have the values 0 and 1, but larger values as well.

In an embodiment, the processor 101 is configured to generate protographs with given weights of rows using a backtracking algorithm. In this way, the processor 101 generates  
 15 a set of protographs  $A$  possibly having a weight larger than 1. On the basis of this set of protographs  $A$  the processor 101 is configured to construct parity check matrices  $H(x)$  with  $wt(H(x)) = A$  (processing block 604 of figure 6a).

In an embodiment, a frame error rate (FER) threshold can be selected and the processor  
 20 101 is configured to perform the iterations of the belief propagation (BP) algorithm, until the smallest possible  $\frac{E_b}{N_0}$  satisfying the FER threshold has been determined. From different codes we choose that one which provides a lower  $\frac{E_b}{N_0}$ .

In processing block 615, the processor 101 is configured to perform a base matrix lifting  
 25 based on simulated annealing. To this end, a parameter  $K$  can be selected as the desired girth. In a first stage, a random initial parity check matrix can be generated by taking random values of shifts for non-empty circulant permutation matrices. This matrix usually has very low girth. Also a special parameter temperature is chosen associated with the simulated annealing approach with relatively high value.

30 In a second stage, the processor 101 is configured to iteratively improve the initial parity check matrix by repeating the procedure defined by the following pseudo code.

1. Nstep=0
- 35 2. Choose one random non-empty cell of the protograph.

3. Enumerate all possible cycles through this cell of length shorter than K.
4. Calculate number of existing cycles "ShiftCycles" for all possible shift values of this cell (using the techniques described above).
5. Take randomly one of these values with probability depending on the value of cycles and the temperature parameter of the annealing method. The probability weight function should be greater for smaller values of ShiftCycles(m), and the difference increases with a reduction of the temperature. One example of such probability weight function is  $w(m) = e^{\frac{-\text{ShiftCycles}(m)}{\text{Temperature}}}$
6. Exact probability of choice  $m$  is  $p(m) = w(m) / \sum_{i=0}^{N-1} w(i)$ .
7. Decrease value of temperature. In each step, the temperature should monotonically decrease. One example of a formula for decreasing the temperature is  $\text{Temperature} = \text{Const} \frac{\text{Total number of cycles in protograph}}{N\text{step}^2}$
8. Increment Nstep and go to step 2.
9. Then if the result is stable for many iterations, finish the procedure.

A main feature of embodiments of the invention is the enumeration of the paths going through a given cell and for each cycle the number of cycles for each value of the shift of CPM for the given cell is determined. In an embodiment, this is done on the basis of a modified backtracking algorithm, as defined by the following pseudo code:

1. Define zero vector ShiftCycles of length N.
2. Enumerate all closed cycles with length shorter than given K, starting and ending in the given cell going through non-empty protograph cells, with vertical lines on even steps, and horizontal lines on odd steps.
3. Repeat the following procedure for each cycle:
4. Consider all horizontal edges (for every  $1 \leq a < K$   $j_{a-1} = j_a$ ). Calculate the number of edges of the cycle which intersect the shifted zone of the protograph, and proceed to the left ( $i_a \leq D(j_a), i_{a-1} > D(j_{a-1})$ ) and to the right ( $i_a > D(j_a), i_{a-1} \leq D(j_{a-1})$ ). If the number of left intersections is not equal to the number of right intersections, it means that cycle is actually not-closed in the spatially-coupled matrix, and this cycle is discarded.
5. Calculate signed sum R of appearing shift  $p_{i_0, j_0}$  of initial cell in equation (4)
6. Consider the starting cell to be a CPM with a shift  $p_{i_0, j_0} = 0$  I(0) (i.e. the circulant matrix with zero shift is the identity matrix) and calculate the total shift  $S = \sum_{a=0}^{K-1} p_{i_a, j_a} - p_{i_a, j_{a+1}} \text{ mod } N$  through this cycle.

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7. The shift of the starting cell  $p_{i_0, j_0}$  in S always goes with sign +, so for an arbitrary shift the equation can be written as:  $R p_{i_0, j_0} + S = \text{mod } N$ , and the forbidden values for  $p_{i_0, j_0}$  can be found. For each solution  $p_{i_0, j_0}$  increment the value of  $\text{ShiftCycles}(p_{i_0, j_0})$  (as described further above).

5

In an embodiment, the processor 101 is configured to solve the equation  $a x = b \text{ mod } c$  occurring in step 7 of the above pseudo code in the following way:

1. Take  $d = \text{GCD}(a, c)$
- 10 2. If  $b \text{ mod } d \neq 0$ , there is no solution for  $x$ .
3. If  $b \text{ mod } d = 0$ , take  $a' = \frac{a}{d}, b' = \frac{b}{d}, c' = \frac{c}{d}$  and solve  $a' x = b' \text{ (mod } c')$ .
4. If  $a' = 0$  and  $b = 0$ , every  $x$  is a solution
5. If  $a' = 0$  and  $b \neq 0$ , there is no solution.
6. If  $a' \neq 0$  there is  $e = a'^{-1} \text{ mod } c'$ , i.e.  $a' e = 1 \text{ mod } c'$ , then  $x = b' e \text{ mod } c'$
- 15 7. All solutions of the initial equation are  $x_k = b' e \text{ mod } c' + k c'$ , for  $0 \leq k < d$ .

Figure 8a shows a schematic diagram illustrating a cycle in a protograph having a left edge intersecting shifted zone. Figure 8b shows a schematic diagram illustrating a cycle in a protograph having no closed cycle in the spatially coupled graph.

20

The following examples illustrate the performance of the base matrix lifting based on the simulated annealing (SA) algorithm described above in comparison to a conventional base matrix lifting based on a hill-climbing (HC) algorithm.

- 25 In a first example, the value of the circulant for a regular protograph with row number 3 and column number L with girth 8 (less value better) can be taken from the following table for the two different algorithms mentioned above.

	L=4	L=5	L=6	L=7	L=8	L=9	L=10	L=11	L=12
SA	9	13	18	21	25	30	35	40	45
HC	9	13	18	21	25	30	35	41	47

- 30 In a second example, the value of the circulant for a regular protograph with row number 3 and column number L with girth 10 (less value better) can be taken from the following table for the two different algorithms mentioned above.

	L=4	L=5	L=6	L=7	L=8	L=9	L=10	L=11	L=12
SA	39	63	97	144	215	297	409	542	698
HC	39	63	103	160	233	329	439	577	758

As can be taken from these tables, in both examples the SA algorithm outperforms the HC algorithm, i.e. provides smaller circulant values, for different numbers of columns.

5

The processing block 617 shown in figure 6b is based on the following considerations.

Let  $H$  be a parity check matrix based on a regular  $(j,k)$ -code  $C(H)$  with length  $n$  (with  $n = WN$ ) and let the corresponding Tanner graph have one component. Let  $L \triangleq H^T H$  and let  $\mu_1, \mu_2$  be the largest and the second-largest eigenvalue, respectively, of  $L$ . It has been shown that in this case the minimum Hamming weight and the minimum AWGNC pseudo-weight have the following lower bounds:

10

$$w_H^{\min}(C(H)) \geq w_p^{\min} \geq n \cdot \frac{2j - \mu_2}{\mu_1 - \mu_2}.$$

15

This result can be applied not only to regular codes, but to non-regular codes as well in the following way:

$$w_H^{\min}(C(H)) \geq w_p^{\min} \geq n \cdot \frac{2j_{avg} - \mu_2}{\mu_1 - \mu_2},$$

20

where  $j_{avg}$  is the average weight of the code  $C(H)$ .

On the basis of the above relations the processor 101 is configured to discard codes having a small lower bound for the pseudo code weights.

25

In a block 619 of figure 6b the processor 101 is configured to perform the same selection as described in the context of block 611 of figure 6a.

In a processing block 621 of figure 6b the processor 101 is configured to perform a further selection step on the basis of a tighter upper bound for the minimum Hamming distance of

30

the respective candidate parity check matrices on the basis of information about the CPM shifts.

Generally, the minimum Hamming distance is an important characteristic of a given parity  
5 check matrix. It provides an estimate for the level of undetectable errors as well as an upper bound on the minimum pseudo-weight of a Tanner graph representing a code.

If the size of the circulant of a spatially coupled code approaches infinity, the spatially  
coupled code becomes a convolution code. Consequently, a convolution code provides a  
10 good approximation for a spatially coupled code. As already mentioned above,  $[W]$  denotes the set of numbers from  $[0 \dots W - 1]$ . It has been shown that for a QC code  $C(H)$  with a circulant parity check matrix  $H$  an upper bound for the minimum Hamming distance of the code is the following:

$$15 \quad d_{\min}(C(H)) \leq \min_{\substack{s \subseteq [W] \\ |s|=C+1}}^+ \sum_{i \in s} wt\left(\text{perm}\left(H_{s \setminus i}(x)\right)\right) \quad (6)$$

In an embodiment, the processor 101 is configured to estimate a tighter upper bound for the minimum Hamming distance on the basis of equation (6). In an embodiment, the  
processor 101 is configured to keep a code, if the tighter upper bound of the Hamming  
20 distance provided by equation (6) is substantially equal to the upper bound provided by equation (5) (which, in turn, implies that the upper bounds are substantially equal to  $(C + 1)!$ ).

The use of equation (6), as implemented in embodiments of the invention, will be  
25 illustrated in the following on the basis of the two examples already mentioned above, i.e. for a first code  $C(H_1)$  with parity check matrix

$$H_1(x) = \begin{pmatrix} x & x^2 & x^4 & x^8 \\ x^5 & x^6 & x^3 & x^7 \end{pmatrix},$$

30 and a second code  $C(H_2)$  with parity check matrix

$$H_2(x) = \begin{pmatrix} x & x^2 & x^4 & x^8 \\ x^6 & x^5 & x^3 & x^9 \end{pmatrix}.$$

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As described above, equation (5) provides for both of these codes the same upper bound having the value 6.

Using equation (6) one obtains for the first code:

5

$$d_{\min}(C(H_1)) \leq \min^+ \left\{ \begin{array}{l} wt(x^4 + x^9) + wt(x^5 + x^{10}) + wt(x^7 + x^7) \\ wt(x^9 + x^{14}) + wt(x^8 + x^{13}) + wt(x^7 + x^7) \\ wt(x^{11} + x^{11}) + wt(x^8 + x^{13}) + wt(x^4 + x^9) \\ wt(x^{11} + x^{11}) + wt(x^9 + x^{14}) + wt(x^5 + x^{10}) \end{array} \right\}$$

$$= \min^+\{4,4,4,4\} = 4$$

Using equation (6) one obtains for the second code:

10

$$d_{\min}(C(H_2)) \leq \min^+ \left\{ \begin{array}{l} wt(x^5 + x^9) + wt(x^4 + x^{10}) + wt(x^6 + x^8) \\ wt(x^{11} + x^{13}) + wt(x^{10} + x^{14}) + wt(x^6 + x^8) \\ wt(x^{13} + x^{11}) + wt(x^{10} + x^{14}) + wt(x^4 + x^{10}) \\ wt(x^{13} + x^{11}) + wt(x^{11} + x^{13}) + wt(x^5 + x^9) \end{array} \right\}$$

$$= \min^+\{6,6,6,6\} = 6$$

Thus, the additional check performed by the processor 101 in block 621 of figure 6b would show that for the two examples above the first code is better than the second code and that, consequently, the second code would be discarded.

In a processing block 623 of figure 6b the processor 101 is configured to perform the same selection as described in the context of block 611 of figure 6a.

20

In a processing block 625 of figure 6b the processor 101 is configured to perform an exact calculation of the minimum Hamming distance for the remaining code candidates. In an embodiment, the processor 101 is configured to perform this exact calculation on the basis of an algorithm for finding the minimal distance in a lattice, as will be described in more detail in the following. In other words, in an embodiment the processor 101 is configured to determine real code distances using number theory.

25

The rows of a parity check matrix  $H$  can be considered as vectors  $b_i$ . Let

$L(b_0, b_1, \dots, b_{n-1}) = \{\sum_{i=0}^{n-1} x_i b_i : (x_0, x_1, \dots, x_{n-1}) \in \mathbb{Z}^n\}$  be a lattice over the vectors  $b_i$  ( $n=CL-$

30

1). The processor 101 is configured to determine the minimum distance between vertices of this lattice and to determine minimum Hamming distance for  $H$  on the basis thereof.



In an embodiment, the processor 101 is configured to generate a lattice based on a code  $C(H)$  such that the minimal non-zero lattice vector corresponds to the minimal Hamming distance vector in the code.

5

In a first stage, the processor 101 is configured to choose a scaling factor  $N$  with

$$N \geq \left\lceil \gamma_{\beta}^{\frac{n-1}{\beta-1}} 2\sqrt{(m+1)(n+1)} r_{\max} M^m \right\rceil,$$

10 where  $\gamma_{\beta}$  denotes the Hermite constant,  $\beta$  denotes the maximal degree of block Korkin-Zolotarev method reduction that we will be described in more detail further below,  $r_{\max}$  denotes the determined good upper bound for the minimal distance of the lattice based on previous steps of this algorithm with smaller  $\beta$ , and  $M = \max(\|A_0\|, \|A_1\|, \dots, \|A_{n-1}\|, \|d\|)$ .

15 In a second stage, the processor 101 is configured to construct the lattice  $\Lambda(B_c)$  on the basis of the matrix

$$B_c = \begin{pmatrix} N \cdot H' & N \cdot qE_{n-k} \\ E_k & 0 \end{pmatrix},$$

20 wherein  $H'$  denotes the generator matrix for the code  $C(H)$  and  $E_k$  denotes the identity matrix of size  $k$ . If one encoded vector  $H'c_1$  has more ones than another encoded vector  $H'c_2$ , i.e.  $\|H'c_1\|_1 < \|H'c_2\|_1$ , then the following relation holds for the Euclidian distance:  $\|B_c c_1\|_2 < \|B_c c_2\|_2$  (for  $N$  being large enough). For this reason, it is possible for the processor 101 to find the minimal distance vector  $v \in \{\Lambda(B_c) \setminus \emptyset\}$  with  $\|v\|_{\infty} = 1$ , which, in  
25 turn, provides the minimum Hamming distance of the code  $C(H)$ .

In an embodiment, the processor 101 is configured to use a Gram-Schmidt orthogonalization process. In an embodiment, the processor 101 is configured to generate an orthogonal basis using the following equations:

30

$$\begin{aligned} b_0^+ &= b_0, \\ b_1^+ &= b_1 - \mu_{0,1} b_0, \\ &\dots \end{aligned}$$

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$$b_{n-1}^{\perp} = b_{n-1} - \sum_{i=0}^{n-2} \mu_{i,n-1} b_i,$$

where  $\mu_{i,j} = \frac{\langle b_i, b_j \rangle}{\langle b_j, b_j \rangle}$ .

Ordered by length basis  $B = \{b_0, b_1, \dots, b_{n-1}\}$  of lattice  $L \subset \mathbb{Z}^m$  is adducted by block

5 Korkin-Zolotarev method with block size  $\beta \in [2, m]$  and precision  $\delta \in \left(\frac{1}{2}; 1\right]$ , if:

- Basis B adducted by length ( $|b_i| \leq |b_j|$  iff  $i > j$ )
- $\delta^2 \cdot \|b_i^{\perp}\|^2 \leq \lambda_1^2(L_i), i \in \{0, \dots, m-1\}$ , where  $\lambda_1(L_i)$  - length of shortest vector in the lattice  $L_i$ , in the orthogonal space with basis  $b_i, \dots, b_{\min(i+\beta-1, m-1)}$ .

10

On the basis of the definitions above, the algorithm implemented in the processor 101 for constructing a basis adducted by block Korkin-Zolotarev method can be defined by the following pseudo code:

15 Input:  $B = \{b_0, b_1, \dots, b_{n-1}\} \in [0,1]^n$ ,  $\delta \in \left(\frac{1}{2}; 1\right]$ ,  $\beta \in [2, m]$

1. Start same algorithm with lower values of  $\beta$ .
2.  $Z:=0$ ;  $j:=0$
3. WHILE  $z < m-1$  DO
  - a.  $j:=j+1$ ;  $k:=\min(j+\beta-1, m)$
  - 20 b. IF  $j=m$  THEN  $j:=0$ ;  $k:=\beta$
  - c.  $A=|b_j|$
  - d.  $b_j^{new} = \text{find\_minimal\_vector}(k, \{b_j, b_{j+1}, \dots, b_{j+k-1}\}, A)$
  - e.  $h:=\min(k+1, m)$
  - f. IF  $\delta |b_j| > |b_j^{new}|$  THEN  $b_j := b_j^{new}$ ;  $z := 0$  ELSE  $z:=z+1$

25 Output: B

In an embodiment, the processor 101 is configured determine for given  $k$ ,  $B$ ,  $A$  the shortest vector of the lattice  $L_{i,k} = \sum_{i=0}^{k-1} x_i b_{i+j} : \{x_0, x_1, \dots, x_{k-1}\} \in \mathbb{Z}^k$  spanned over the vectors  $b_j$ . In an embodiment, the corresponding algorithm implemented in the processor

30 101 can work in a parallel mode with several nodes up to  $A$  (upper bound for minimal distance). The algorithm, which according to an embodiment is implemented in the processor 101 and is defined by the following pseudo code, is basically an  $n$ -fold cycle

- 25 -

with calculated start and end for each cycle and a reduction of the upper bound A for each recorded distance.

Input:  $j, k, B = \{b_0, b_1, \dots, b_{k-1}\} \in [0,1]^k$ , id – id of the node.

- 5     1. Calculate  $B^\perp = \{b_0^\perp, b_1^\perp, \dots, b_{k-1}^\perp\}$  and matrix  $\mu_{i,j}$
2.  $X = \{\text{id}, 0, 0, \dots, 0\}$ ;  $l = \{0\}^m$ ,  $R = \{\emptyset\}$ ;
3.  $i := 0$
4. WHILE  $i \leq k$ :
  - a.  $l_i = (x_i + \sum_{j=i+1}^m x_j \mu_{j,i})^2 \|b_i^\perp\|^2$
  - 10    b. IF  $(\sum_{j=i+1}^{k-1} l_j > A)$  THEN  $i := i+1$ ;  $x_i = x_i + 1$
  - c. IF  $(\sum_{j=i+1}^{k-1} l_j \leq A)$  AND  $i=0$  THEN
    - i. IF  $\|\sum_{j=0}^{k-1} x_j b_j\| < A$  THEN  $A = \|\sum_{j=0}^{k-1} x_j b_j\|$ ,  $R = R \cup \{\sum_{j=0}^{k-1} x_j b_j\}$
    - d. IF  $(\sum_{j=i+1}^{k-1} l_j \leq A)$  AND  $i>0$  THEN
      - i.  $i := i-1$ ,
      - 15    ii.  $x_i = \left\lceil -\sum_{j=i+1}^m x_j \mu_{j,i} - \frac{\sqrt{A - \sum_{j=i+1}^m l_j}}{\|b_i^\perp\|^2} \right\rceil$
  5. Return element from R with smallest norm.

In a processing block 627 of figure 6b the processor 101 is configured to determine one or more stopping sets on the basis of the following algorithm. A stopping set of size  $s$  is a subset  $\tilde{V} = \{v_{i_0}, v_{i_1}, \dots, v_{i_{s-1}}\}$  of the variables nodes such that the induced subgraph  $T(\tilde{V})$  has no check nodes of degree one. A constraint set  $F$ , is a set  $\{(p_i, s_{p_i}) : s_{p_i} \in \{0,1\} \forall p_i \in \Gamma\}$ , where  $\Gamma \subseteq \{0, \dots, n-1\}$  ( $n = WN$ ) is a set of distinct codeword positions. Let  $\chi(F) = \{p_i : (p_i, 1) \in F\}$ , i.e. the support set of the constraint set  $F$ .  $H_A$  denotes the parity-check matrix consisting of columns from  $H$  corresponding to indices from the set  $A \subseteq \{0, \dots, n-1\}$ , and with the all-zero columns with indices from  $\Gamma \setminus A$ . The row of the parity-check matrix is active, if the row weight is exactly one. The set of indices of active rows in  $H$  is  $\phi(H)$ . The support set  $\chi(x)$  of vector  $x \in \{0,1\}^n$  is the set of indices of non-zero elements of  $x$ , where there are no active rows, i.e.  $|\phi(H)| = 0$ .  $S \subseteq \{0,1\}^n$  denotes the set of all length- $n$  binary vectors and  $S^{(F)} = (s_0, \dots, s_{n-1}) \in S : s_j = s \text{ if } (j, s) \in F$ .  $S_H$  denotes the unique maximum subset of  $\{0,1\}^n$  such that for every element  $s \in S_H$ , with support set  $\chi(s)$ . The constraint set  $F$  is valid if and only if  $S_H^F = (S_H)^F$  is non-empty. The weight function  $w(F)$  is the Hamming weight of  $(S_H)^F$  when  $F$  is valid and infinity if  $F$  is not valid (which is a way to obtain trapping sets subgraph).  $W'(F)$  is any lower bound of  $W(f)$ .

In an embodiment, the processor 101 is configured to determine one or more stopping sets on the basis of a branch-and-bound method. There are  $2^{WL}$  possible values of a coding vector of length  $WL$ . In an embodiment, this set of all possible values is split into  
 5 branches by adding constraints of the kind  $x_i = k$ . In an embodiment, the processor 101 is configured to determine all stopping sets of length  $\tau$  or less on the basis of a branch-and-bound method, as defined by the following pseudo code:

- 10 1. Generate initial list of constraints sets  $L$  from one element – empty constraint set  $F=\{\}$ .
2. Split constraint set. Take first constraint  $F$  from list  $L$ . Most general and simple constraint set  $F=\{\}$ . Every constraint set  $F$  can be split into two, by any variable  $x_i$ ,  $F_1 = F \cup \{x_i = 0\}$  and  $F_2 = F \cup \{x_i = 1\}$ . Replace constraint set  $F$  in the list  $L$  into two new constraints sets  $F_1$  and  $F_2$ .
- 15 3. Repeat the following steps 4 to 6 for each constraints set  $F_1$  and  $F_2$
4. Extend constraints set. Perform extended iterative decoding with achieve some values of  $x_i \notin F_k$ . Add these values as additional constraints to  $F_k$ . In case the extension of the constraints set leads to contradictory results, the constraint set can be eliminated.
- 20 5. Find new stopping sets. If constraint  $F_k$  has all fixed variables, i.e. corresponds to a single point, check whether it has number of 1 equal or less than  $\tau$ , add  $\chi(F_k)$  to list of the stopping sets already found.
6. Bound part, eliminate branch. Calculate lower bound  $w'(F)$  of minimal stopping set. If  $w'(F) > \tau$ , eliminate  $F_k$ .
- 25 7. If  $L$  is not empty return to step 2.

In an embodiment, the processor 101 is configured to determine a lower bound of the minimal stopping set for the constraint set  $F$  in the following way. Let  $q$  denote the number of constraints  $x_i = 1$  in the constraint set  $F$ . Let  $T(F)$  denote the set of columns, whose  
 30 indices are not empty and are not used in the constraint set  $F$ . Let  $\tilde{H}$  denote a submatrix of  $H$  consisting of columns from the set  $T(F)$ . It has been shown that the following linear lower estimation holds:

$$w'(F) = q + \min_{x_i \geq 0} \sum_{i=0}^{|T(F)|-1} x_i, \quad \text{when } \tilde{H}x \geq (1, \dots, 1)^T$$

In an embodiment, the processor 101 is configured to compute the above lower bound using linear optimisation.

In a processing block 629 of figure 6b the processor 101 is configured to estimate a pseudo code weight of a trapping set in the following way. To enumerate trapping sets an approach simulating a belief propagation algorithm with deterministic noise of specific tree-like shapes can be used by the processor 101. It is assumed that the girth of the graph is larger than 4. Consider some variable "root" node in the Tanner graph as well as three variable nodes at a distance of 2 from this root node. A minimal tree containing these 4 variable nodes is a 4VN subgraph. These 4VN subgraphs satisfy the following two important properties:

- Each trapping intersects by 3 variable vertices with at least one such 4VN subgraph. Three variable vertices are in the cycle and one variable node is connected to the cycle via a check node.
- The number of 4VN subgraphs is relatively small and possible to enumerate. The number of these variants is bounded by  $n(d_c - 1)^{d_v}$ , where  $n=WN$  denotes the number of variables,  $d_v$  denotes the weight of the column (for irregular codes maximal weight of the column), and  $d_c$  denotes the weight of the row.

Figure 9 shows a schematic diagram illustrating an exemplary 4VN subgraph of a protograph.

Using a 4VN subgraph specific noise can be constructed for belief propagation algorithm (Sum-product). As the code is linear, without loss of generality it can be assumed that the sent data is all-zeros and decoded '1' corresponds to mistakes, positive LLR corresponds to '1' and negative to '0'.

The noise measured in LLR is constructed by putting  $k(1-\varepsilon_1)$  into 4 variable nodes for a given 4VN subgraph, and for all other variable nodes  $k\gamma$  is chosen, where  $k$  is the channel factor, and  $\varepsilon_1, \gamma$  denote manually chosen parameters.

Constants are chosen to obtain the situation that an error causes only a small number of unsatisfied parity checks. The channel factor  $k$  has the same meaning as in the normal

decoding process, i.e. it is a factor used to convert received signal to the log-likelihood values. More precisely, for an AWGN channel with variance  $\sigma^2$ , the channel factor is  $\frac{2}{\sigma^2}$ .

The constant  $\gamma$  can be chosen to be less than 1 to "weaken" the graph not affected by an error impulse. Preferred values for  $\gamma$  range from 0.3 to 0.8 depending on a graph. The error magnitude  $\varepsilon$  can be chosen empirically large enough to provoke errors in the trapping sets.

For each described above error impulse the processor 101 is configured to start the decoding process. Denote by  $x_i$  the hard decision after  $i$  iterations (it is assumed that the processor 101 performs at most  $i_{max}$  iterations). Find the number of steps, when the number of unsatisfied parity checks is minimal:  $i^* = \underset{1 \leq i \leq i_{max}}{\operatorname{argmin}} w_H(Hx_i)$ . Let  $S(x)$  be a set of variable nodes whose corresponding bits in the vector  $x$  are 1.

Then a subgraph included by  $S(x_{i^*})$  is considered as a trapping set. If  $S(x_{i^*})$  is not a trapping set, the processor 101 tries growing each  $S(x_i), \frac{k_{max}}{2} \leq i \leq k_{max}$  into a trapping set. To this end, the processor 101 is configured to determine a minimal set  $S'(x_i) \supset S(x_i)$  which contains at least one cycle. Thereafter, the processor 101 is configured to find a minimal set  $S''(x_i) \subset S'(x_i)$ , which contains the same cycles as the set  $S'$  (in other words, does not contain any tree like structures). The processor 101 provides  $S''(x_i)$  as the trapping set for  $x_i$ .

In an embodiment, the apparatus 100 can maintain a list of all trapping sets found, in particular of the recently determined trapping sets. In an embodiment, this list of trapping sets is maintained by the apparatus in a lexicographic order, i.e.  $T' < T''$  iff  $T'_1 < T''_1$  or  $T'_1 = T''_1$  and  $T'_2 < T''_2$ . In an embodiment, the apparatus 100 is configured to delete the last trapping set on the list, if the list of trapping sets becomes too large.

Figure 10a shows a diagram illustrating the performance of codes provided by embodiments of the invention in comparison with conventional codes. More specifically, figure 10a shows a comparison of the performance of N=28980, R=0.879 LTE with 8 iteration max-log-map, two families of binary SC-LDPC codes which use a base matrix: regular code with column weight 3, circulant 230 and irregular RA with average column weight 3.57 and circulant 57 under 30 iterations of layered min-sum and NB GF(64) QC-LDPC based on expander graph under 30 iteration QSPA-FFT, QAM-64.

Figure 10b shows a diagram illustrating the performance of codes provided by embodiments of the invention in comparison with conventional codes. More specifically, shows a comparison of the performance of N=44160, R=0.6 LTE with 8 iteration max-log-map, two binary SC-LDPC codes which use base matrix: regular code with column weight 3, circulant 320 and irregular RA with average column weight 3.57 circulant 138 under 30 iterations of layered min-sum, QAM 256.

As can be taken from figures 10a and 10b, tail-biting SC-LDPC codes provided by embodiments of the invention show good performance in the "waterfall" region, have a hardware friendly decoder (every repetition uses the same code, moreover a window decoder can be used to get more convolutional gain with constant latency) and an encoder of reasonable complexity using CPM Gaussian elimination approach, as provided by embodiments of the invention.

Figure 11a, 11b shows a diagram illustrating the performance of Multi-edge LDPC codes provided by embodiments of the invention in comparison with known codes from recent 3gpp proposals, namely Codes A and Codes B. More specifically is shows a comparison of the SNR required for codes with rates 1/2 and 0.89 for an information length in the range from K=100 to 8000 to reach a Frame Error Rate  $10^{-2}$  under 15 iteration of layered normalized min-sum, QPSK.

Embodiments of the invention provide on the basis of a QC-LDPC protograph a block version of a convolutional code, namely a tail-biting spatially-coupled (SC) LDPC code.

Embodiments of the invention allow generating a code with SC-LDPC structures of the graph using a Belief Propagation (BP) with the following properties: large Hamming distance (code properties), better structures of cycles (graph properties – ACE Spectrum when ACE=EMD) and reasonable complexity (average column weight, size of base matrix, maximal column weight).

While a particular feature or aspect of the disclosure may have been disclosed with respect to only one of several implementations or embodiments, such feature or aspect may be combined with one or more other features or aspects of the other implementations or embodiments as may be desired and advantageous for any given or particular application. Furthermore, to the extent that the terms "include", "have", "with", or other variants thereof are used in either the detailed description or the claims, such terms are

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intended to be inclusive in a manner similar to the term "comprise". Also, the terms "exemplary", "for example" and "e.g." are merely meant as an example, rather than the best or optimal. The terms "coupled" and "connected", along with derivatives may have been used. It should be understood that these terms may have been used to indicate that  
5 two elements cooperate or interact with each other regardless whether they are in direct physical or electrical contact, or they are not in direct contact with each other.

Although specific aspects have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent  
10 implementations may be substituted for the specific aspects shown and described without departing from the scope of the present disclosure. This application is intended to cover any adaptations or variations of the specific aspects discussed herein.

Although the elements in the following claims are recited in a particular sequence with  
15 corresponding labeling, unless the claim recitations otherwise imply a particular sequence for implementing some or all of those elements, those elements are not necessarily intended to be limited to being implemented in that particular sequence.

Many alternatives, modifications, and variations will be apparent to those skilled in the art  
20 in light of the above teachings. Of course, those skilled in the art readily recognize that there are numerous applications of the invention beyond those described herein. While the present invention has been described with reference to one or more particular embodiments, those skilled in the art recognize that many changes may be made thereto without departing from the scope of the present invention. It is therefore to be understood  
25 that within the scope of the appended claims and their equivalents, the invention may be practiced otherwise than as specifically described herein.



CLAIMS

1. An apparatus (100) for providing a parity check matrix defining a spatially-coupled  
 5 low density parity check, QC-LDPC, code on the basis of a set of base matrix parameters  
 defining a plurality of base matrices, each base matrix of the plurality of base matrices  
 being associated with a protograph of a plurality of protographs, wherein the set of base  
 matrix parameters defines the size  $W \times C$ , a circulant size  $N$ , a maximal column weight  $M$   
 and a set of allowed column weights of the plurality of base matrices, wherein the  
 10 apparatus (100) comprises:

a processor (101) configured to:

generate on the basis of a plurality of protographs a set of candidate protographs by  
 15 discarding protographs of the plurality of protographs;

lift the protographs of the set of candidate protographs for generating a plurality of codes;  
 and

20 generate on the basis of a plurality of codes a set of candidate codes by discarding codes  
 of the plurality of codes,

wherein the processor (101) is configured to lift the protographs of the set of candidate  
 protographs on the basis of a simulated annealing technique.

2. The apparatus (100) of claim 1, wherein the processor (101) is configured to  
 discard those protographs of the plurality of protographs that are associated with a LDPC  
 code having a minimum Hamming distance that is larger than a minimum Hamming  
 distance threshold value.

3. The apparatus (100) of claim 2, wherein the processor (101) is configured to  
 estimate the minimum hamming distance of a LDPC code  $C$  on the basis of the upper  
 bound defined by the following equation:

$$d_{\min}(C(H)) \leq \min_{\substack{s \subseteq [W] \\ |S|=C+1}}^+ \sum_{i \in S} \text{perm}(A_{S \setminus i})$$

wherein

$[W]$  denotes the set of numbers from  $[0 \dots W - 1]$ ,

the operator  $\min^+(\dots)$  defines the minimal positive value of its argument, and

5 the permanent operator  $\text{perm}(\dots)$  is defined by the following equation:

$$\text{perm}(B) = \sum_{\sigma} \prod_{j \in [m]} b_{j, \sigma(j)}$$

wherein

10  $B$  is a  $m \times m$  matrix having elements  $b_{j, \sigma(j)}$  and

$\sigma$  takes all  $m!$  possible permutations of the set  $[m]$ .

4. The apparatus (100) of claim 2 or 3, wherein the minimum Hamming distance threshold value is  $(C+1)!$ .

15

5. The apparatus (100) of any one of the preceding claims, wherein the processor (101) is further configured to discard protographs of the plurality of protographs on the basis of the balanced girth of the parity check matrix  $H$  associated with each protograph.

20 6. The apparatus (100) of claim 5, wherein the processor (101) is configured to discard those protographs from the plurality of protographs that are associated with a parity check matrix  $H$  having a balanced girth which is larger than a balanced girth threshold value.

25 7. The apparatus (100) of any one of the preceding claims, wherein the processor (101) is further configured to lift a protograph of the plurality of protographs having at least one parallel edge to a protograph having no parallel edges, in particular using a quasi-cyclic technique.

30 8. The apparatus (100) of any one of the preceding claims, wherein the processor (101) is further configured to discard those protographs of the plurality of protographs that are associated with an extrinsic message degree (EMD) that is smaller than an EMD threshold value.

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9. A method for providing a parity check matrix defining a spatially-coupled low density parity check, LDPC, code on the basis of a set of base matrix parameters defining a plurality of base matrices, each base matrix of the plurality of base matrices being associated with a protograph of a plurality of protographs, wherein the set of base matrix parameters defines the size  $W \times C$ , a circulant size  $N$ , a maximal column weight  $M$  and a set of allowed column weights of the plurality of base matrices, wherein the method comprises:

generating on the basis of the plurality of protographs a set of candidate protographs by discarding protographs of the plurality of protographs;

lifting the protographs of the set of candidate protographs for generating a plurality of codes; and

generating on the basis of the plurality of codes a set of candidate codes by discarding codes of the plurality of codes,

wherein the step of lifting the protographs of the set of candidate protographs is based on a simulated annealing technique.

10. A computer program comprising program code for performing the method of claim 9 when executed on a computer.

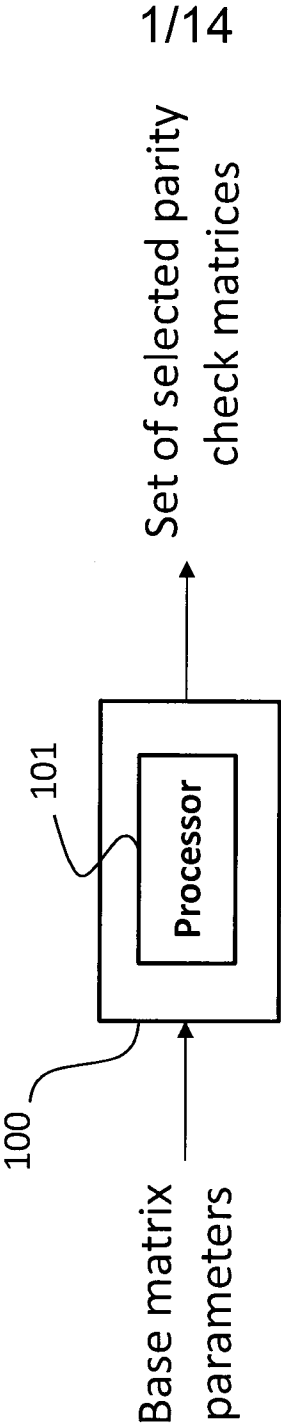


Fig. 1

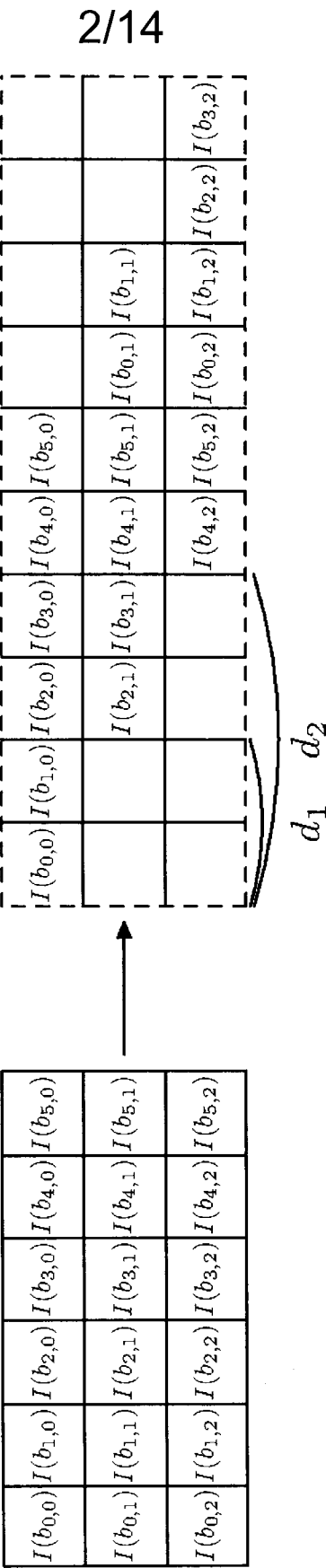


Fig. 2

[illegible]

Fig. 3

## Tail-biting

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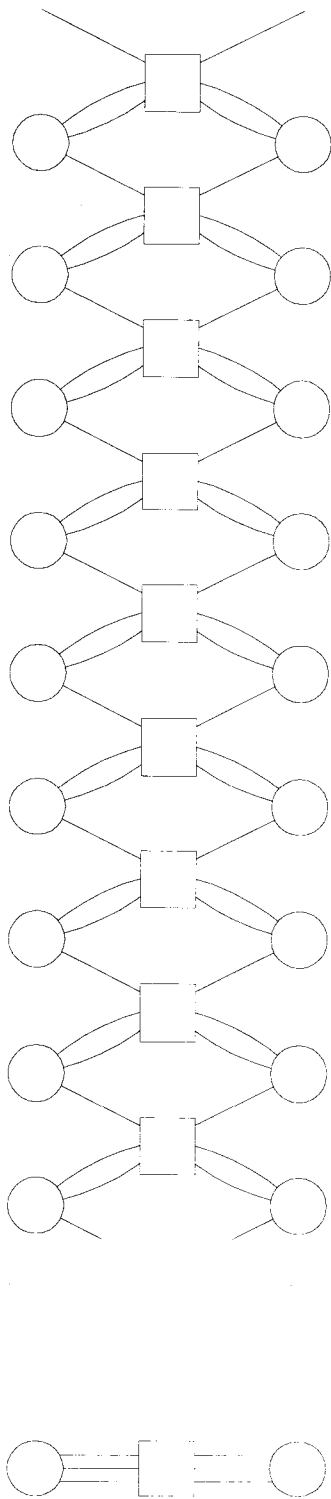


Fig. 4

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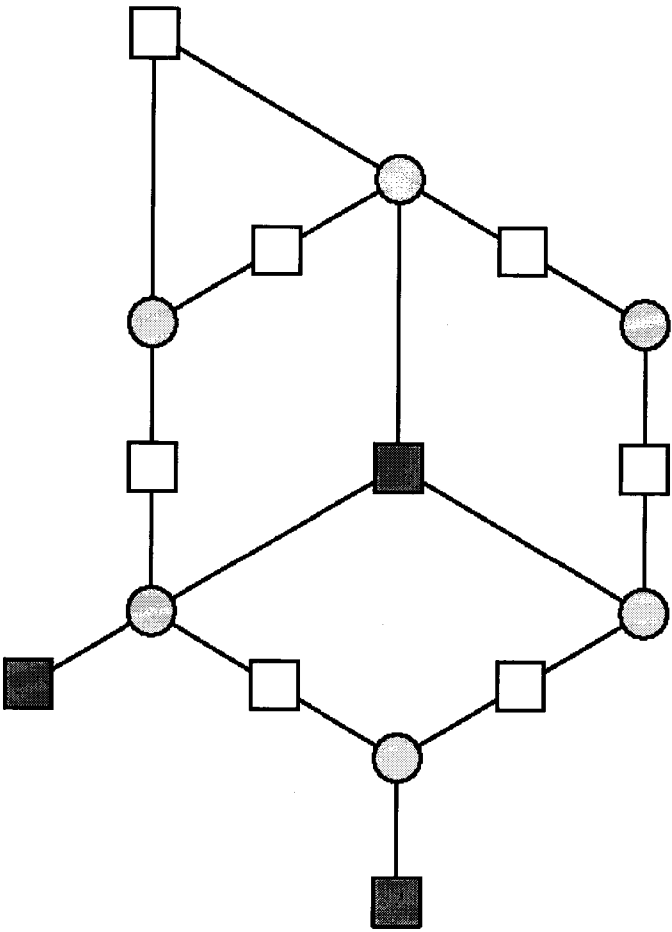


Fig. 5



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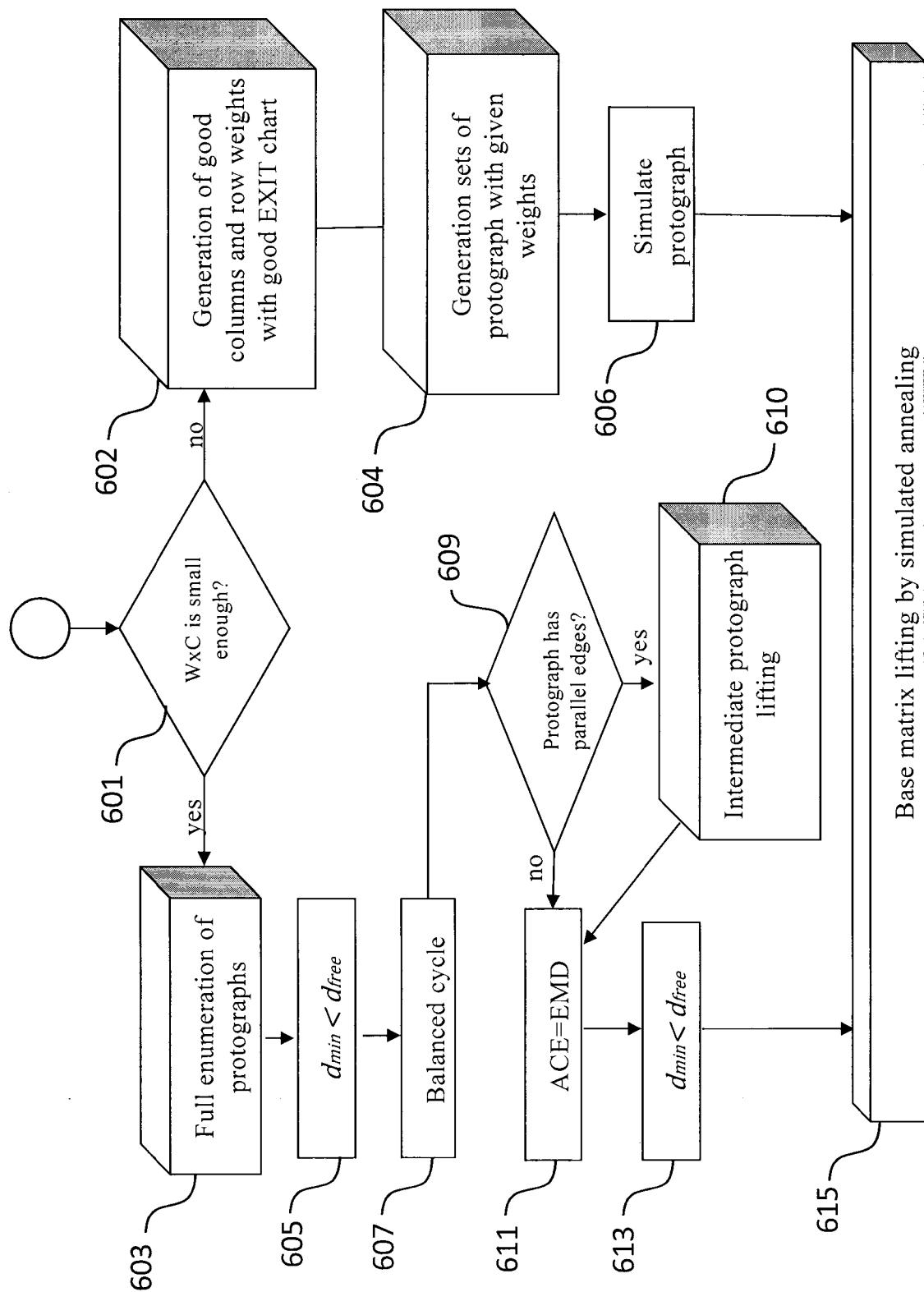


Fig. 6a

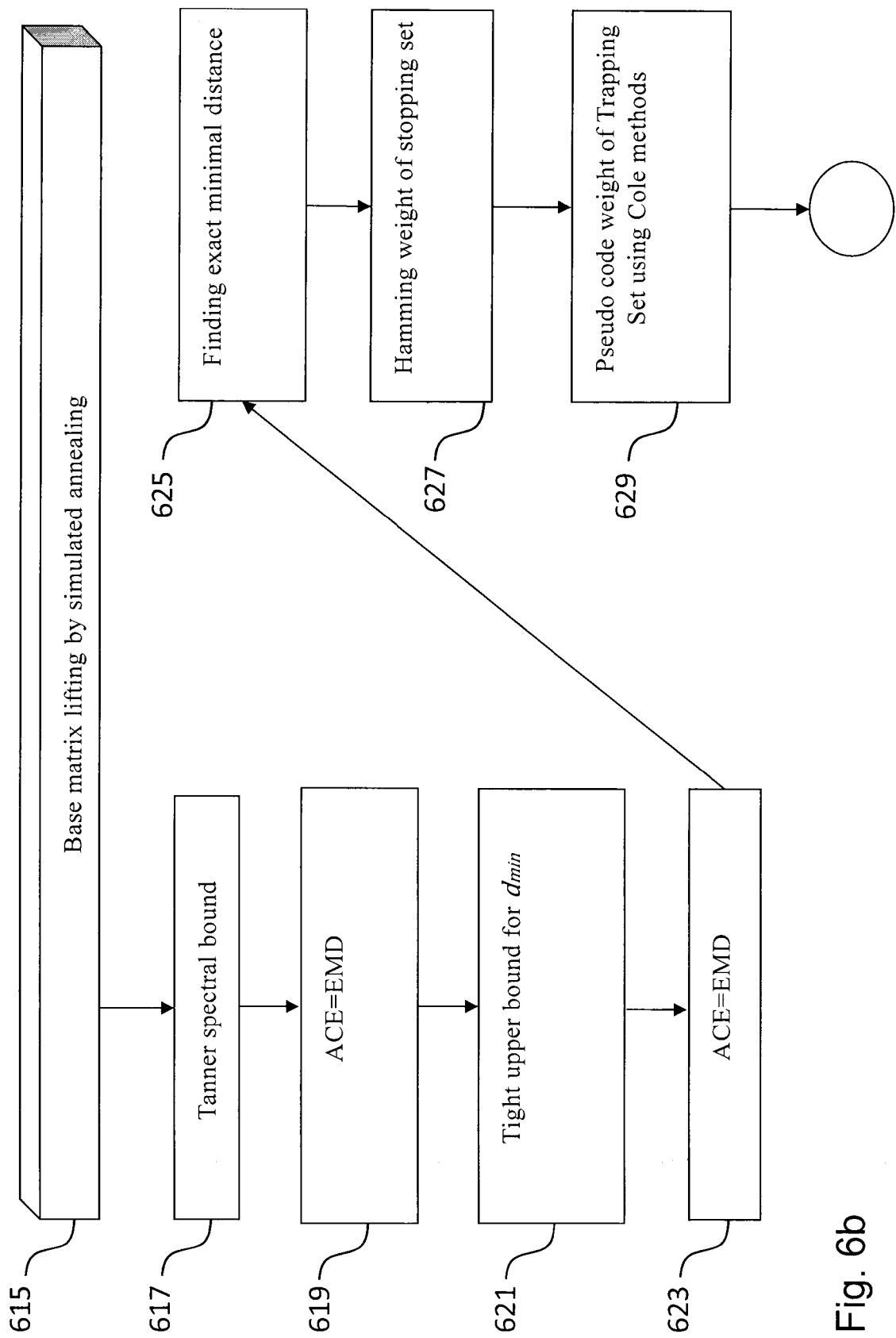


Fig. 6b

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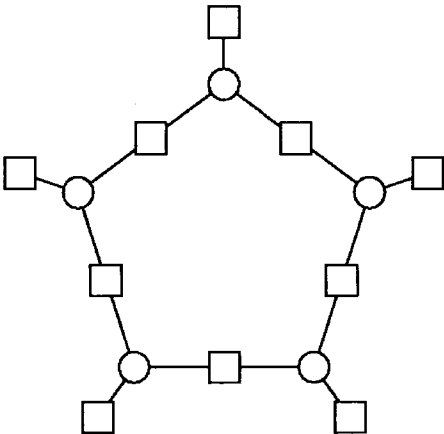
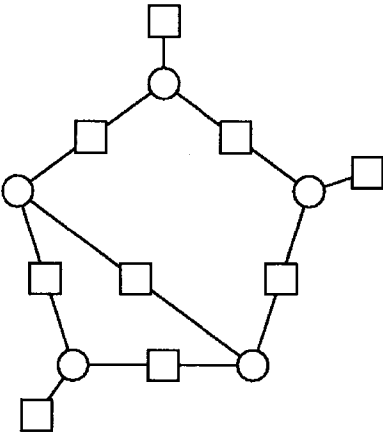


Fig. 7

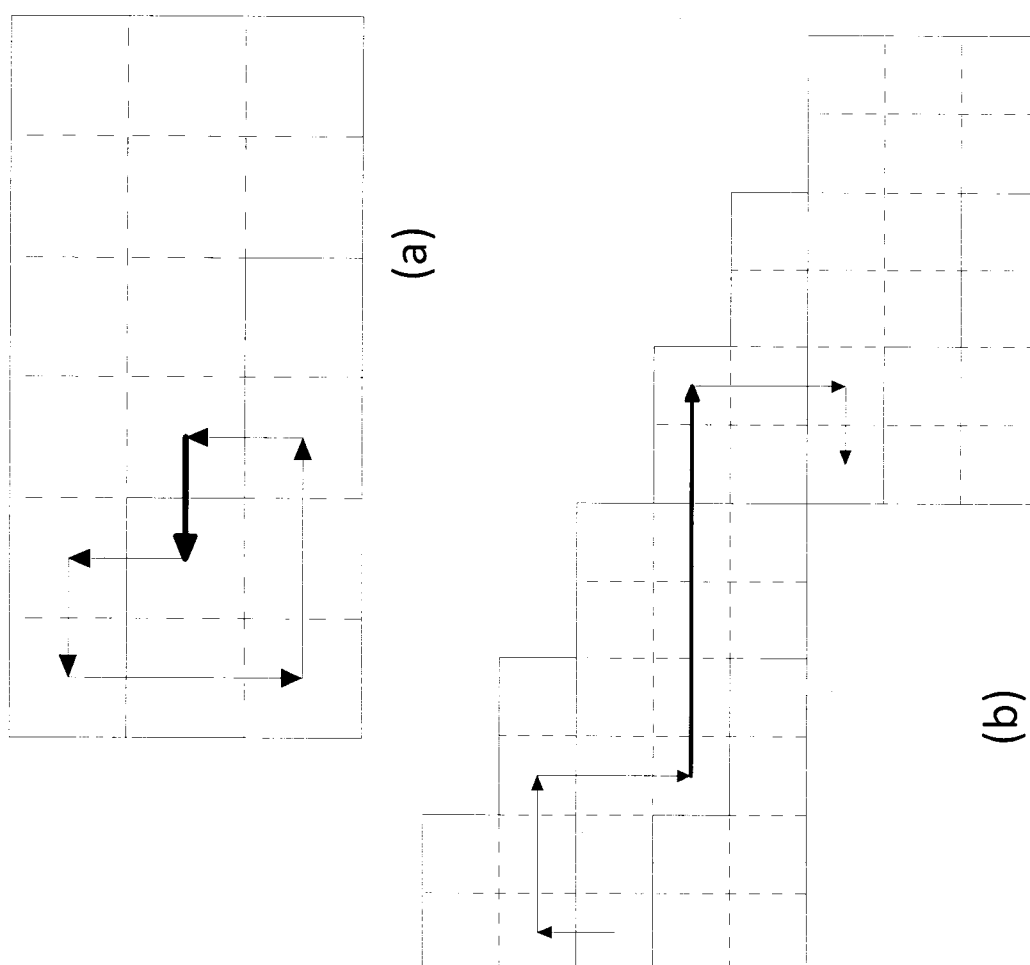


Fig. 8

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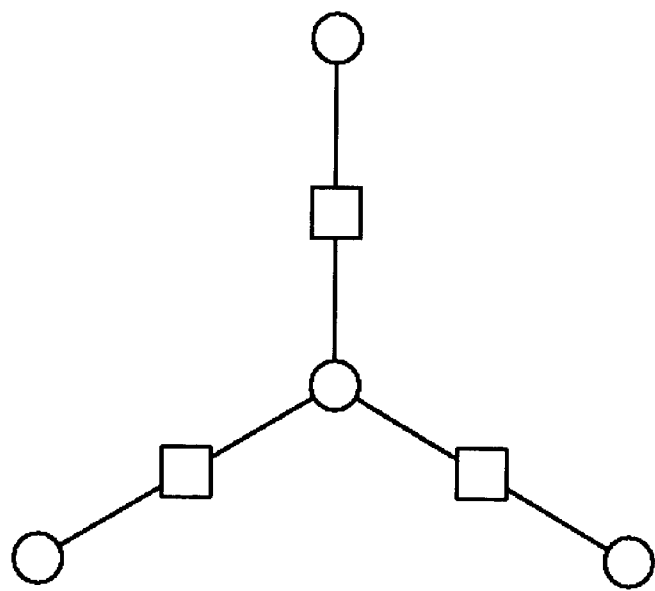


Fig. 9

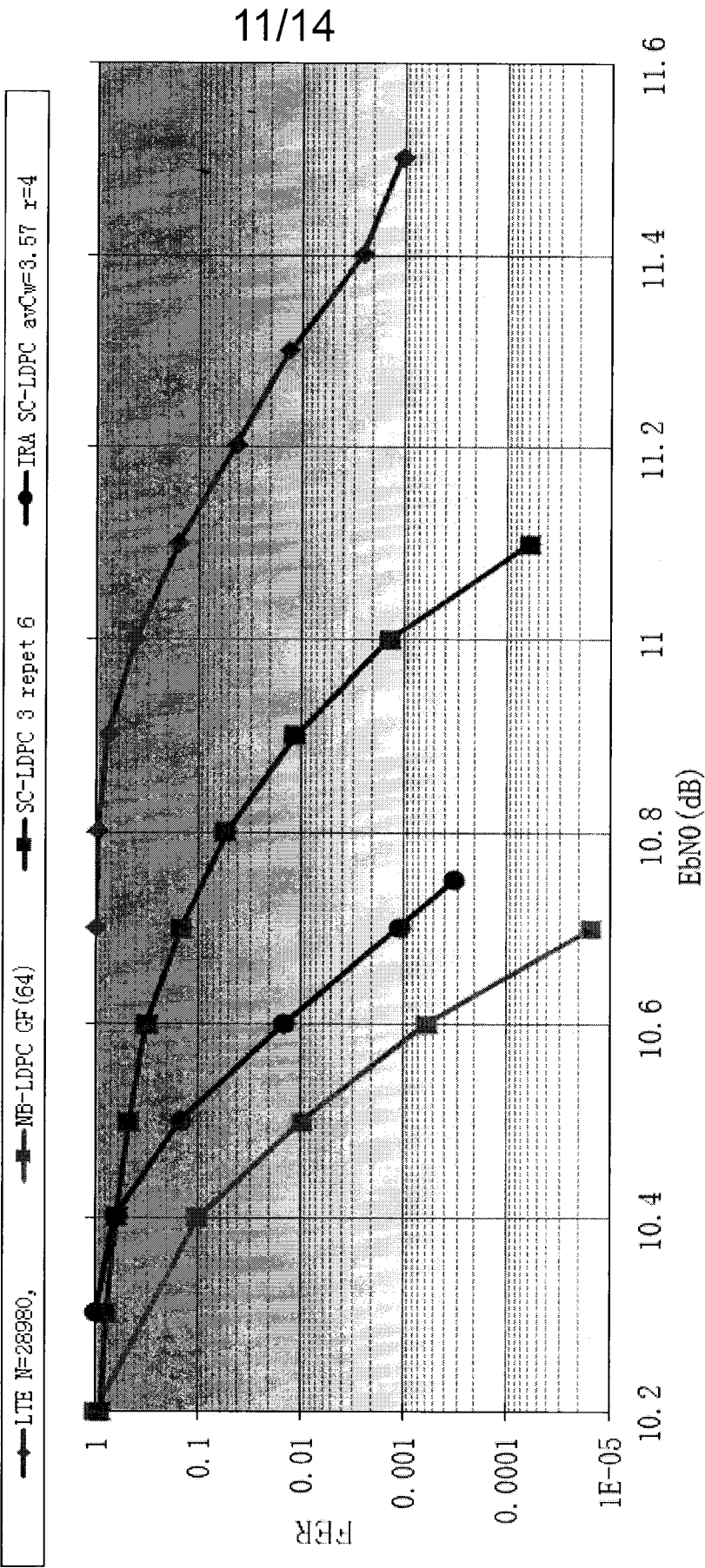


Fig. 10a

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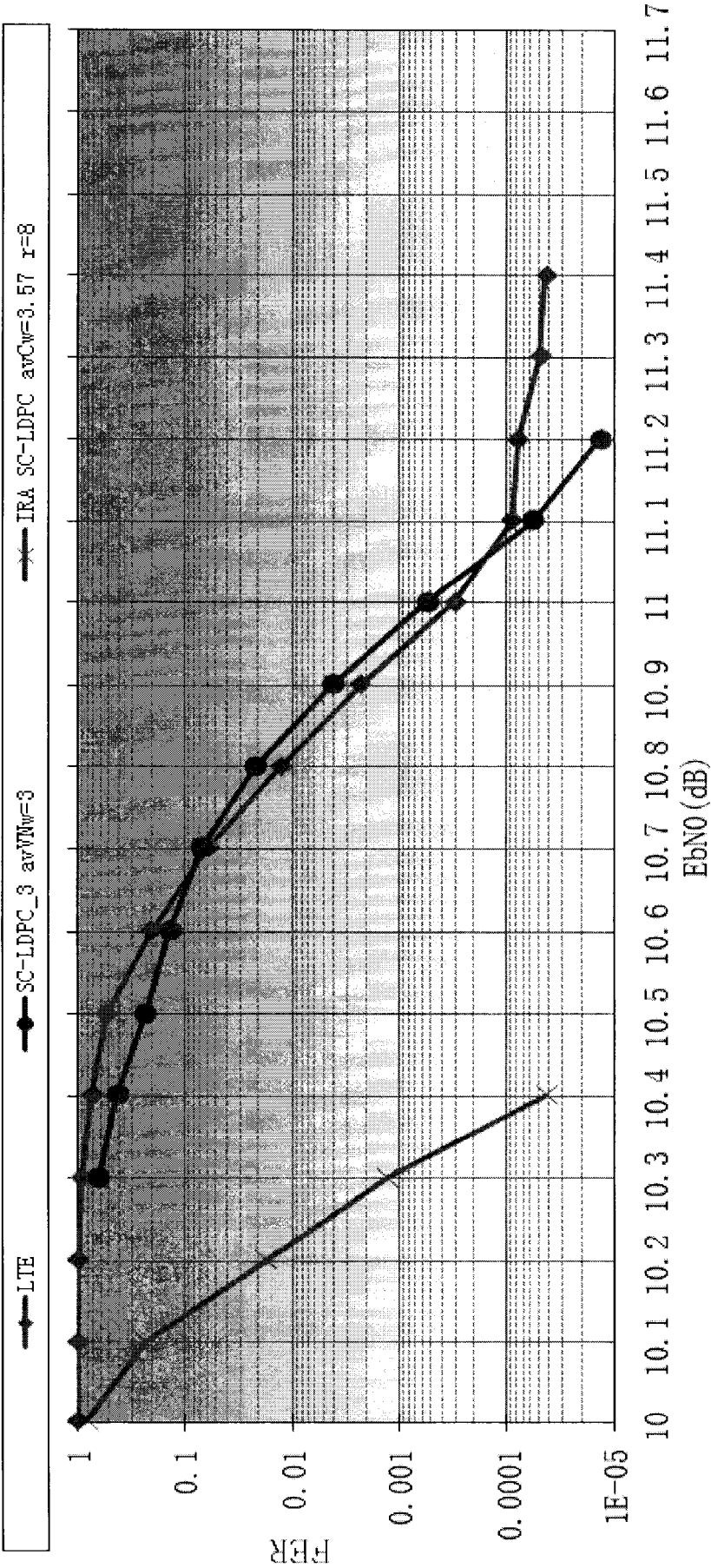


Fig. 10b

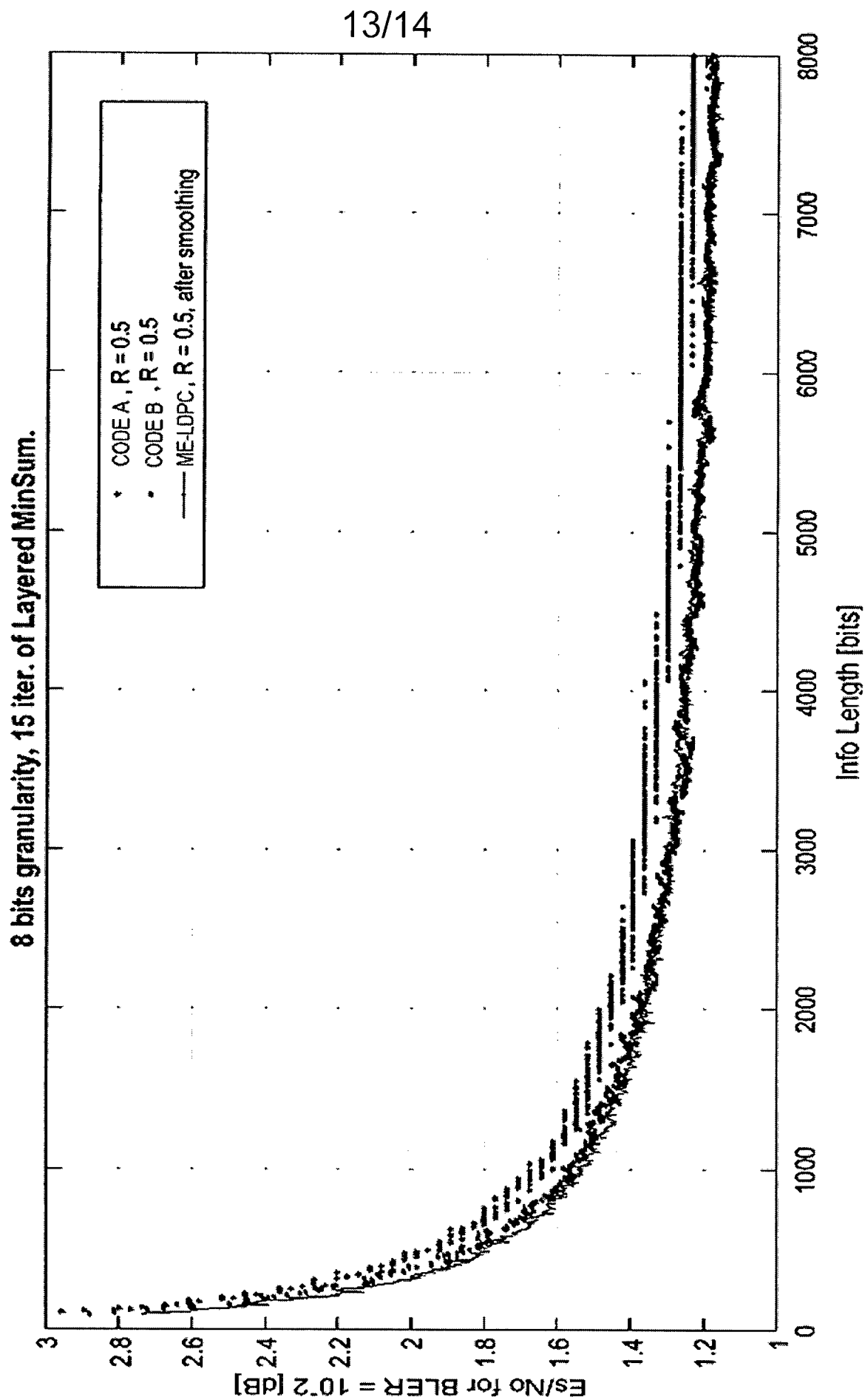


Fig. 11a



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8 bits granularity, 15 iter. of Layered MinSum.

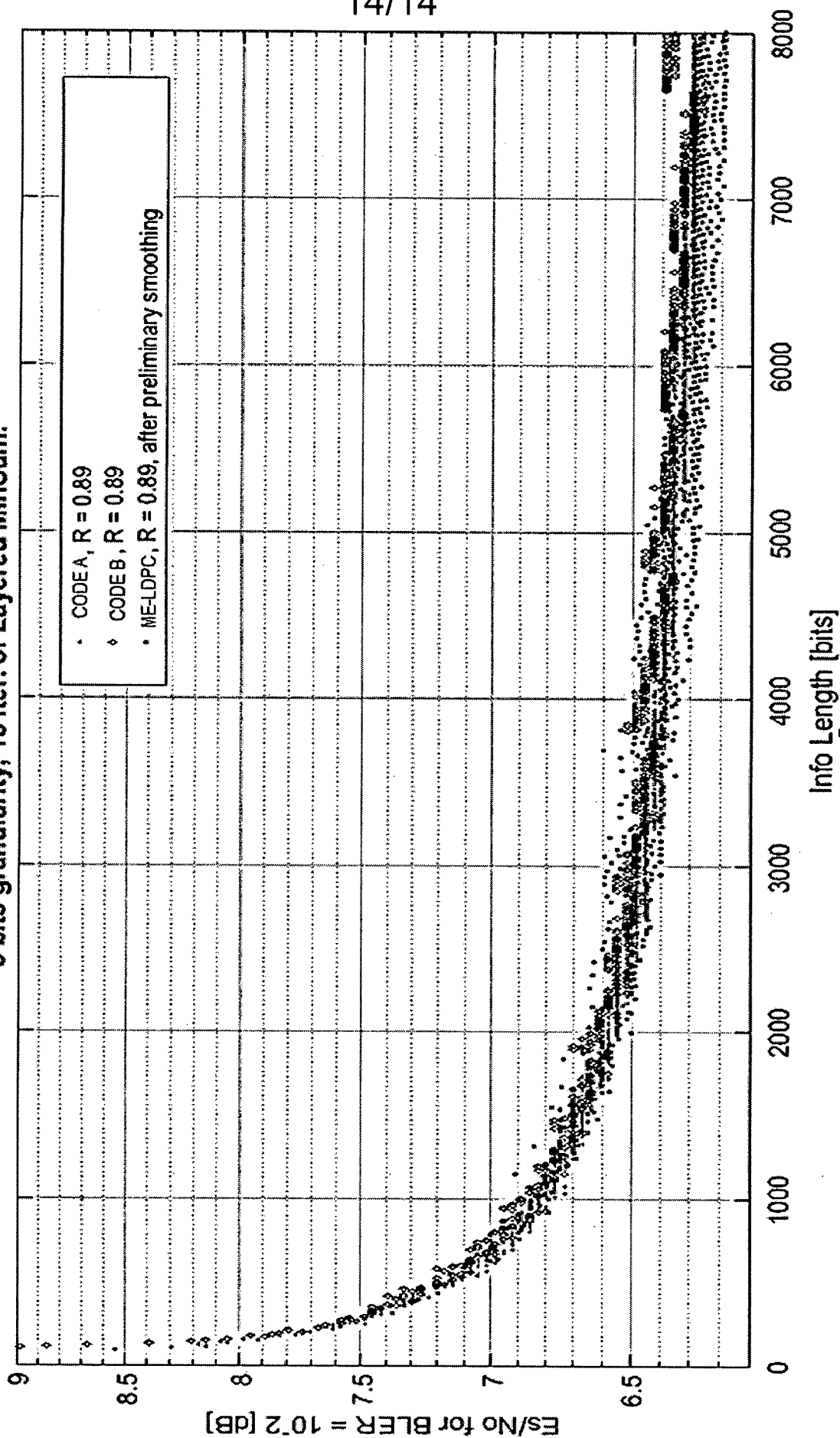


Fig. 11b

# INTERNATIONAL SEARCH REPORT

International application No  
PCT/RU2016/000799

<b>A. CLASSIFICATION OF SUBJECT MATTER</b> INV. H03M13/03 H03M13/11 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b>		
Minimum documentation searched (classification system followed by classification symbols) H03M		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EP0-Internal, WPI Data		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016/233979 A1 (KOIKE-AKINO TOSHIAKI [US]) 11 August 2016 (2016-08-11) paragraph [0048] - paragraph [0069]; figures 8,9 -----	1,5,7,8
A	US 2013/086456 A1 (YEDIDIA JONATHAN [US] ET AL) 4 April 2013 (2013-04-04) paragraph [0155] - paragraph [0162] ----- -/--	1,5,7,8
<div style="display: flex; justify-content: space-between;"> <span><input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C.</span> <span><input checked="" type="checkbox"/> See patent family annex.</span> </div>		
<div style="display: flex;"> <div style="flex: 1;"> <p>* Special categories of cited documents :</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier application or patent but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> </div> <div style="flex: 1;"> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>"&amp;" document member of the same patent family</p> </div> </div>		
Date of the actual completion of the international search  <div style="text-align: center; font-size: 1.2em;">27 July 2017</div>		Date of mailing of the international search report  <div style="text-align: center; font-size: 1.2em;">07/08/2017</div>
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer  <div style="text-align: center; font-size: 1.2em;">Offer, Elke</div>

# INTERNATIONAL SEARCH REPORT

International application No

PCT/RU2016/000799

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>YIGE WANG ET AL: "Hierarchical and High-Girth QC LDPC Codes", IEEE TRANSACTIONS ON INFORMATION THEORY, vol. 59, no. 7, 1 July 2013 (2013-07-01), pages 4553-4583, XP055394292, USA  ISSN: 0018-9448, DOI: 10.1109/TIT.2013.2253512  page 4553 - page 4554  page 4566  page 4569</p>	1,5,7,8
X	<p>-----  WO 2013/047258 A1 (MITSUBISHI ELECTRIC CORP [JP]; YEDIDIA JONATHAN [US]; WANG YIGE [US]) 4 April 2013 (2013-04-04) paragraph [0034] - paragraph [0060]; figures 3-7</p>	1,5,7,8
X	<p>-----  LAU FRANCIS C M ET AL: "Novel types of cyclically-coupled quasi-cyclic LDPC block codes", PROC., IEEE INTERNATIONAL CONFERENCE ON ADVANCED TECHNOLOGIES FOR COMMUNICATIONS, ATC, 12 October 2016 (2016-10-12), pages 27-31, XP033015949, DOI: 10.1109/ATC.2016.7764787 [retrieved on 2016-12-01] the whole document</p>	1,5,7,8
X	<p>-----  HUA ZHOU ET AL: "Cycle analysis of time-invariant LDPC convolutional codes", PROC., IEEE 17TH INTERNATIONAL CONFERENCE ON TELECOMMUNICATIONS (ICT), 2010, 4 April 2010 (2010-04-04), pages 23-28, XP031685444, ISBN: 978-1-4244-5246-0 the whole document</p>	1,5,7,8
A	<p>-----  HUA ZHOU ET AL: "Girth analysis of polynomial-based time-invariant LDPC convolutional codes", PROC., IEEE 20TH INTERNATIONAL CONFERENCE ON SYSTEMS, SIGNALS AND IMAGE PROCESSING, IWSSIP, 11 April 2012 (2012-04-11), pages 104-108, XP055393341, ISSN: 2157-8672 the whole document</p> <p style="text-align: center;">-----  -/--</p>	1,5,7,8

# INTERNATIONAL SEARCH REPORT

International application No  
PCT/RU2016/000799

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>Vasily; Usatyuk: "Some problems of Graph Based Codes for Belief Propagation decoding Quasi-cyclic Low Density Parity-check code (QC-LDPC)", 24 November 2015 (2015-11-24), XP055302971, Retrieved from the Internet: URL:https://arxiv.org/ftp/arxiv/papers/1511/1511.00133.pdf [retrieved on 2016-09-15] the whole document</p>	1,5,7,8
A	<p>----- YIGE WANG ET AL: "Construction of high-girth QC-LDPC codes", PROC., 5TH IEEE INTERNATIONAL SYMPOSIUM ON TURBO CODES AND RELATED TOPICS, 2008, 1 September 2008 (2008-09-01), pages 180-185, XP031353684, ISBN: 978-1-4244-2862-5 the whole document -----</p>	1,5,7,8

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/RU2016/000799

### Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☒ Claims Nos.: 9, 10  
because they relate to subject matter not required to be searched by this Authority, namely:  
**see FURTHER INFORMATION sheet PCT/ISA/210**
2. ☐ Claims Nos.:  
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

### Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

#### Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

**FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210**

Continuation of Box II.1

Claims Nos.: 9, 10

Rule 39.1(i) PCT - Mathematical method

The subject-matter of claims 9 and 10 does not have a technical character but constitute purely mathematical method steps or a computer program performing purely mathematical method steps. In particular, independent claim 9 specifies a method for providing a parity check matrix defining a spatially-coupled low density parity check, LDPC code. It is noted that a code and its parity check matrix are purely a mathematical construction and a tool for describing that mathematical construction, respectively. In particular, a spatially-coupled LDPC code is composed of codewords with length  $n$  and is thus a subset of all binary vectors of length  $n$ . Consequently, neither the code nor its parity check matrix defining the code have a technical character per se. It is further noted that a method for providing a parity check matrix defining a spatially-coupled LDPC code only fulfils the requirements of Rule 39 PCT if technical means for carrying out the method are claimed (see claims 1-8) or if an additional method step of using the provided parity check matrix for encoding or decoding would be claimed.

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/RU2016/000799

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