NATIONAL UNIVERSITY OF SINGAPORE
Department of Electrical and Computer Engineering

EE2027 Electronic Circuits
Supplementary Questions 3: Solution

These are supplementary questions to Tutorial 3, and they aim to provide more work examples. They will not be discussed in class, but solutions will be provided after Tutorial discussion.

S1. An n-channel MOSFET has the following parameters: threshold voltage V_{TH} = 0.75 V, gate oxide thickness t_{ox} = 40 nm and channel length L = 1 μm. The following parameters may be used: mobility of the electrons in the inversion channel, μ_n = 525 $cm^2\ V^{-1}s^{-1}$; temperature, T = 300 K; relative permittivity of the gate oxide, $\varepsilon_{r,SiO2}$ = 3.9.

(a) Calculate the gate oxide capacitance per unit area of the MOSFET.

[Ans: $C_{ox} = 8.63 \times 10^{-8}$ F / cm^2]

(b) Determine the channel width W such that when the MOSFET is biased in the saturation region, the drain current I_{Dsat} = 6 mA when the gate-source voltage, V_{GS} = 5V.

[Ans: W = 14.7 μm]

(c) The MOSFET is biased such that V_{GS} = 5 V. For each of the following cases, determine whether the MOSFET is operating in the linear region or the saturation region. Calculate also the corresponding drain current I_D.

(i) V_{GD} = 0 V; [Ans: I_D = 6 mA]

(ii) V_{GD} = 2 V. [Ans: I_D = 5.49 mA]

V_{GD} is the voltage at the gate with respect to the drain.

S1. **Solution:**

(a) Gate oxide capacitance per unit area:

$$C_{ox} = \frac{\varepsilon_{r,SiO2}}{t_{ox}} = \frac{3.9 \times 8.854 \times 10^{-14}}{40 \times 10^{-7}} = 8.63 \times 10^{-8}\,\text{F/cm}^2$$

(b) For the MOSFET to operate in saturation region with I_{Dsat} = 6 mA,

$I_{Dsat} = \frac{1}{2}\mu_n \frac{W}{L} C_{ox}(V_{GS} - V_{TH})^2$ (assuming no Channel Length Modulation effect, since λ is not given)

$$6 \times 10^{-3} = \frac{1}{2} \times 525 \times \frac{W}{1\mu m} \times 8.63 \times 10^{-8} (5 - 0.75)^2$$

$$\therefore \quad W = 14.7\mu\text{m}$$

(c) With V_{GS} = 5 V, MOSFET has a channel since $V_{GS} > V_{TH}$, and
$V_{DSsat} = V_{GS} - V_{TH}$ = 5 - 0.75 = 4.25 V.

(i) When V_{GD} = 0, $V_{DS} = V_{GS}$ = 5 V > V_{DSsat}.
The MOSFET is operating in the saturation region.
$I_D = I_{Dsat}$ = 6 mA [from part (b)]

(ii) When V_{GD} = 2 V, $V_{DS} = V_{DG} + V_{GS}$ = -2 + V_{GS} = 3 V < V_{DSsat}.
The MOSFET is operating in linear region.
Since V_{GS} = 5 V, V_{DS} = 3 V,

$$I_D = \mu_n \frac{W}{L} C_{ox}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}{}^2]$$
$$= 525 \times \frac{14.7}{1} \times 8.63 \times 10^{-8} \times [(5 - 0.75) \times 3 - \frac{1}{2} \times 3^2]$$
$$= 5.49\text{ mA}$$

S2. An n-channel MOSFET M_1 is connected as shown in Fig. S2(a) to perform I_D - V_{GS} measurements. The gate-source voltage V_{GS} is changed by varying V_{DD} and the resulting drain current I_D is measured by a current meter.

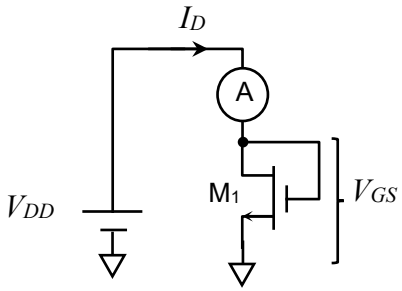


Fig. S2(a)

(a) Show that the MOSFET M_1 is operating in the saturation region, when $V_{DD} > V_{TH}$.

(b) The measured I_D - V_{GS} characteristic is shown in Fig. S2(b). Also shown is the corresponding tabulated data. Due to experimental error, the measured points do not exactly follow the square law predicted by the drain current equation in the saturation region, i.e., $I_D = K_n (V_{GS} - V_{THN})^2$. Transform the drain current equation and devise a way such that you can easily extract the device parameters K_n and V_{THN}, which are the conductance parameter and threshold voltage of the n-channel MOSFET, respectively.

(Hint: Transform the drain current equation such that it becomes a straight line equation format, such as $y = mx+C$.)

[Ans: $K_n = 2.52$ mA V^{-2}; $V_{THN} = 0.803$ V].

V_{GS} (V)	I_D (mA)
1.3	0.61
1.5	1.00
1.7	2.03
1.9	3.11
2.1	4.44
2.3	5.63
2.5	7.43
2.7	9.04
2.9	11.66
3.1	12.95
3.3	15.04
3.5	18.33
3.7	21.23
3.9	24.0

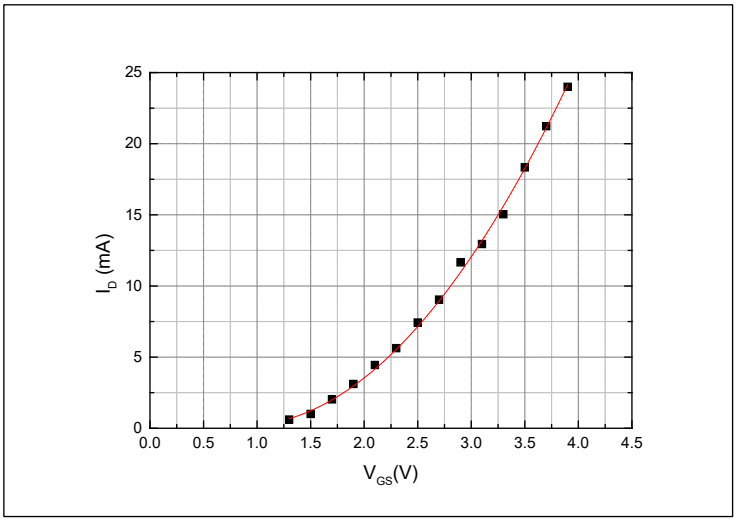


Fig. S2(b)

(c) Assuming that V_{THN} is unchanged, describe three ways of increasing K_n in the design of the MOSFET.

S2. **Solution:**

(a) As the drain and gate of M_1 are shorted together, $V_{DS} = V_{GS}$.

For an n-channel MOSFET, $V_{THN} > 0$.

Therefore, $V_{DS} = V_{GS} > V_{GS} - V_{THN}$.
Also, $V_{GS} = V_{DD} > V_{TH}$.

Hence, the MOSFET M_1 is operating in the saturation region.

N.B.: Whenever the drain and gate are shorted together, MOSFET operates in the saturation region, provided $V_{GS} > V_{TH}$.

(b) Since the MOSFET is operating in the saturation region, the equation $I_D = K_n\left(V_{GS} - V_{THN}\right)^2$ applies.

Taking the square root of equation - $I_D = K_n\left(V_{GS} - V_{THN}\right)^2 \Longrightarrow$

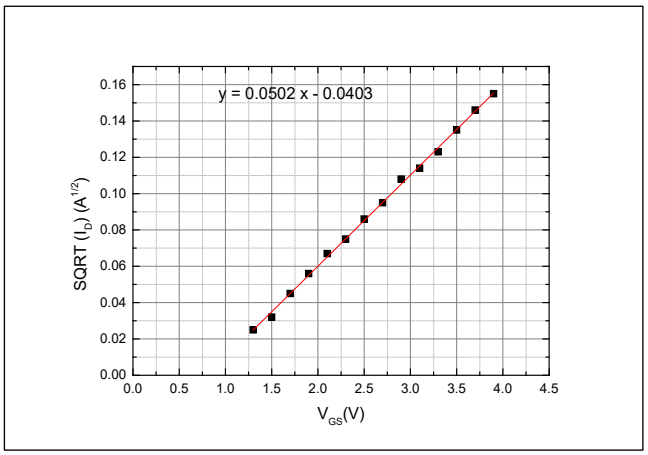
$$\sqrt{I_D} = \sqrt{K_n}\left(V_{GS} - V_{THN}\right) = \sqrt{K_n}\,V_{GS} - \sqrt{K_n}\,V_{THN}$$

This is an equation of the form $y = mx + C$, where

$$y = \sqrt{I_D}, \quad x = V_{GS}, \quad m = \sqrt{K_n}, \quad C = -\sqrt{K_n}\,V_{THN}\,.$$

Plot $\sqrt{I_D}$ versus V_{GS} and draw a best-fit straight line -

V_{GS}(V)	I_D (mA)	$\sqrt{I_D}$(A$^{-1/2}$)
1.3	0.61	0.025
1.5	1	0.032
1.7	2.03	0.045
1.9	3.11	0.056
2.1	4.44	0.067
2.3	5.63	0.075
2.5	7.43	0.086
2.7	9.04	0.095
2.9	11.66	0.108
.1	12.95	0.114
3.3	15.04	0.123
3.5	18.33	0.135
3.7	21.23	0.146
3.9	24	0.155



From the best-fit line equation, $\sqrt{K_n} = 0.0502, \Longrightarrow K_n = 0.00252$ A V^{-2} = 2.52 mA V^{-2};

$$\sqrt{K_n}\,V_{THN} = 0.0403 \Longrightarrow V_{THN} = 0.803 \text{ V}.$$

(c) Any of the following ways can be used to increase K_n:

Method 1 : Increase C_{OX} by reducing the oxide thickness,

Method 2 : Increase C_{OX} by using a dielectric material with higher permittivity.

Method 3 : Increase the width W of the MOSFET,

Method 4 : Reduce the length L of the MOSFET.

S3. The schematic cross-sectional view of an *n*-channel MOSFET is shown in Fig. S3. The MOSFET has the following parameters: $K_n = 0.5$ mA V^{-2}, $V_{TH} = 1$ V.

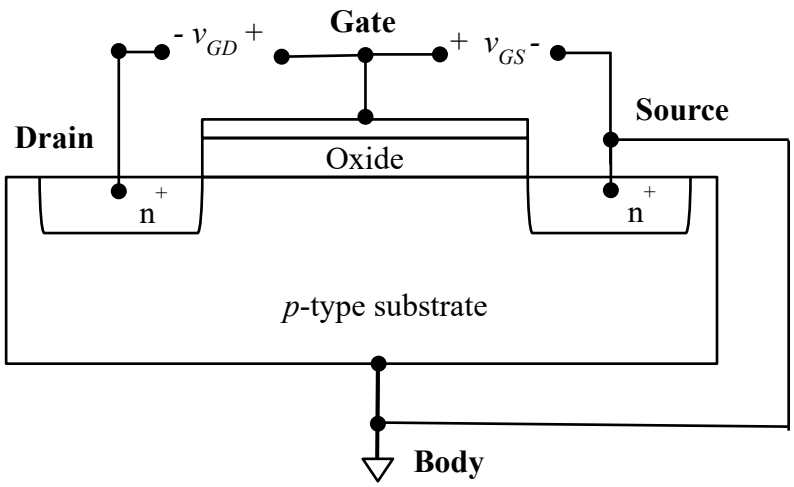


Fig. S3

For each of the following biasing conditions, determine the region in which the MOSFET operates. Calculate the drain current I_D, indicate its direction and sketch the shape of the channel in Fig. S3 -

(a) $V_{GS} = 5$ V, $V_{GD} = 0$ V; [Ans: $I_D = 8$ mA]

(b) $V_{GS} = 5$ V, $V_{GD} = 2$ V; and [Ans: $I_D = 7.5$ mA]

(c) $V_{SG} = 5$ V, $V_{GD} = 2$ V.

S3. **Solution:**

MOSFET is of the *n*-channel type.

(a) $V_{GS} = 5$ V, $V_{GD} = 0$ V

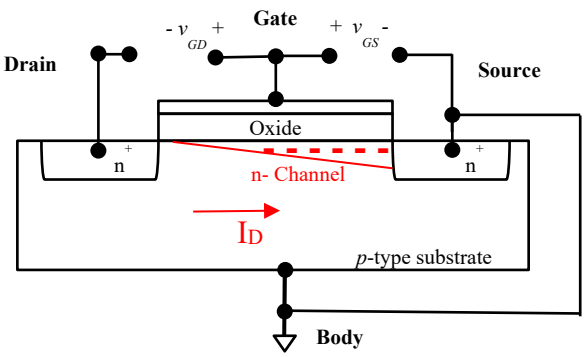
$V_{GS} = 5$ V > $V_{TH} = 1$ V, so there is a channel between Source and Drain.

$V_{GD} = 0$ V $\Rightarrow V_D = V_G \Rightarrow V_{DS} = V_{GS} = 5$ V > $V_{DSSat} = V_{GS} - V_{TH} = 5 - 1 = 4$ V. Hence, the MOSFET is working in the saturation region.

$I_D = K_n\left(V_{GS} - V_{TH}\right)^2 = 0.5$ mA V^{-2} × (5 -1) $^2 = 8$ mA.

MOSFET is of the n-channel type, so the drain current flows from the Drain (left) to Source (right).

The shape of the channel is sketched in the figure below -



Note: The channel pinch-off point should be indicated as in-between the source and drain, and NOT at the drain end as in the sketch above.

(b) $V_{GS} = 5$ V, $V_{GD} = 2$ V

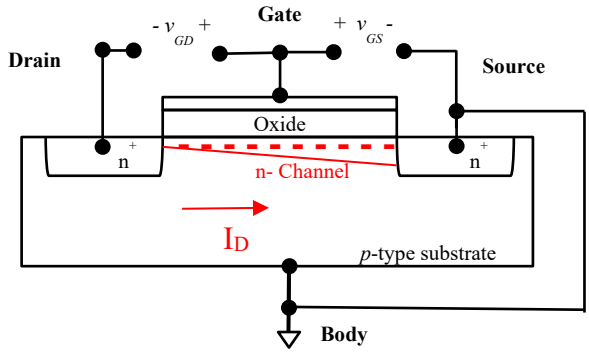
$V_{GS} = 5$ V > $V_{TH} = 1$ V, so there is a channel between Source and Drain.

$V_{GD} = 2$ V, so $V_{DS} = V_{GS} - V_{GD} = 5 - 2 = 3$ V < $V_{DSSat} = V_{GS} - V_{TH} = 5 - 1 = 4$ V. Hence, the MOSFET is working in the linear region.

$I_D = 2K_n\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right] = 2 \times 0.5$ mA V^{-2} × [(5 -1) ×3 - $\frac{1}{2}$ × 3^2]= 7.5 mA

MOSFET is of the n-channel type, so the drain current flows from the Drain (left) to Source (right).

The shape of the channel (extends from Source to Drain) is sketched in the figure below -

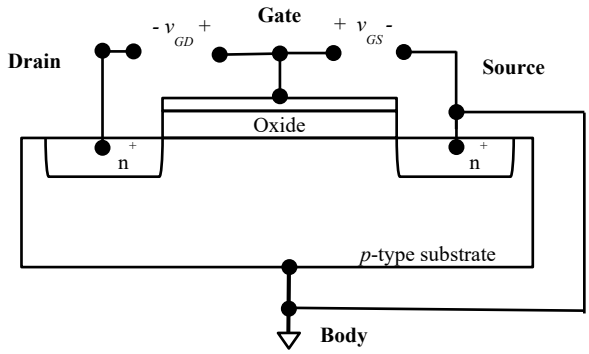


(b) $V_{SG} = 5$ V, $V_{GD} = 2$ V

$V_{SG} = 5$ V $\Rightarrow V_{GS} = -5$ V $< V_{TH} = 1$ V, so there is no channel between the Source and Drain, and the MOSFET is working in the Cut-Off region.

The drain current $I_D = 0$.

No channel is formed between Source and Drain, as indicated in the figure below -



S4. A BJT circuit is shown in Fig. S4, where the BJT is of the pnp type and has a common emitter current gain of 100.

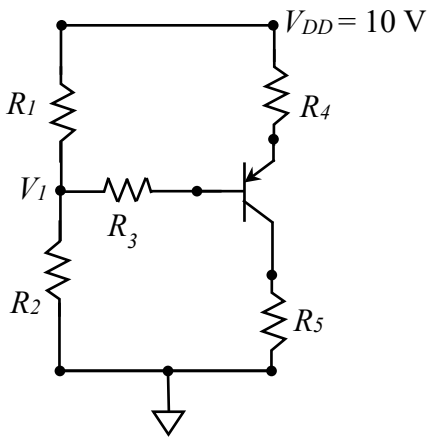


Fig. S4

The BJT is operating in the forward active mode and its collector current is 1 mA.

(a) Given that R_3 = 3.3 kΩ and R_4 = 4.9 kΩ, determine the value of V_1.

[Ans: V_1 = 4.318 V]

(b) It is also given that R_2 = 10 kΩ, estimate the value of R_1 by assuming that voltage divider is valid. Verify the assumption.

[Ans: R_1 = 13.16 kΩ]

(c) For the BJT to operate in the forward active region, determine the constraint on the value of R_5?

[Ans: R_1 < 4.351 kΩ]

S4. **Solution:**

(a) BJT is of the pnp type.

BJT is in the forward active mode and I_C = 1 mA -

- $V_{EB} \approx 0.7$ V
- $I_E = \frac{\beta+1}{\beta} I_C = 1.01 \times 1\text{m} = 1.01$ mA (or $I_E \approx I_C = 1$ mA)
- $I_B = \frac{I_C}{\beta} = 10$ µA

By means of KVL,

$$V_1 = V_{DD} - I_E \times R_4 - V_{EB} - I_B \times R_3 \approx 10 - 1.01\text{m} \times 4.9\text{k} - 0.7 - 10\mu \times 3.3\text{k}$$

$$\therefore\ V_1 = 4.318\text{ V (or } \approx 4.367\text{ V for } I_E \approx I_C = 1\text{ mA)}$$

(b) Assuming voltage divider is valid, i.e., $I_{R1} \approx I_{R2} >> I_B$

$$V_1 \approx \frac{R_2}{R_1+R_2} \times V_{DD} = \frac{10\text{k}}{R_1+10\text{k}} \times 10 = 4.318\text{ V (or } \approx 4.367\text{ V)}$$

$$\therefore\ R_1 = 13.16\text{ k}\Omega\text{ (or } \approx 12.90\text{ k}\Omega\text{)}$$

Verify voltage divider assumption –

$$I_{R1} \approx I_{R2} = \frac{V_{DD}}{R_1+R_2} = \frac{10}{13.16\text{k}+10\text{k}} = 0.432\text{ mA} \gg I_B = 10\text{ µA (valid)}$$

(c) For pnp BJT to operate in forward active region, $V_{EB} \approx 0.7\text{ V} > 0$ and $V_{CB} < 0$.

By means of KVL:

$$V_B = V_{DD} - I_E \times R_4 - V_{EB} \approx 10 - 1.01\text{m} \times 4.9\text{k} - 0.7$$

$$V_C = I_C \times R_5 = 1\text{m} \times R_5$$

$$V_{CB} = V_C - V_B = 1\text{m} \times R_5 - (10 - 1.01\text{m} \times 4.9\text{k} - 0.7) < 0$$

$$\therefore\ R_5 < 4.351\text{ k}\Omega\text{ (or 4.4 k}\Omega\text{ assuming } I_E \approx I_C)$$

S5. For each of the statements below, select TRUE (if the statement is correct) or FALSE (if the statement is wrong).

(a) A BJT can be made by connecting two pn-junction diodes back-to-back.

TRUE / FALSE

(b) For a CMOS logic circuit with multiple inputs, all the inputs must be at a low voltage for the pull-up network (PUN) to turn on and pull the output up to a high voltage.

TRUE / FALSE

(c) For a CMOS logic gate in the steady-state, when the pull-down network (PDN) does not conduct, it can be concluded that the pull-up network (PUN) is conducting and will result in a high output voltage.

TRUE / FALSE

(d) The base-emitter voltage and collector-emitter voltage of a BJT are V_{BE} = -0.72 V, and V_{CE} = -3.5 V, respectively. If the BJT is operating in the forward active region, it can be concluded that the BJT is of the pnp type.

TRUE / FALSE

(e) Given that a MOSFET has negligible channel length modulation effect, it can be concluded that its drain current, I_D, hardly depends on its drain to source voltage, V_{DS}, when operating in the linear region.

TRUE / FALSE

(f) A pn-junction can be treated as an open circuit as long as it is operating in reverse bias.

TRUE / FALSE

S6. For parts (a), (b) and (c) below, select the **correct** statement(s).

(a) Consider an n-MOSFET, which of the following statements is(are) TRUE?

(i) when $V_{GS} > V_{TH}$, the surface of the *p*-type substrate underneath the Gate becomes effectively *n*-type.

(ii) a drain current will flow as long as $V_{DS} > 0$, regardless of the V_{GS} value.

(iii) the drain current always increases with increasing V_{DS}.

(iv) $V_{DS} = (V_{GS} - V_{TH})$ is the smallest V_{DS} value for the n-MOSFET to operate in saturation mode when $V_{GS} > V_{TH}$.

(b) Which of the following statement(s) is(are) true?

(i) An n-MOSFET has its gate and source shorted together and $V_{DS} > (V_{GS} - V_{TH})$ is operating in the saturation region.

(ii) A CMOS inverter with the sizing of n-MOSFET, $(W/L)_n = 50$, and the sizing of p-MOSFET, $(W/L)_p = 100$, has $t_{pLH} > t_{pHL}$.

(iii) In ac small-signal operation, a single-port network with resistors and a MOSFET can be represented by an equivalent resistance.

(iv) An n-MOSFET operating in the linear region can be modelled as a resistor regardless of its V_{DS} value.

(c) An ideal diode has $I_S = 2\times10^{-14}$ A, a maximum power rating of 0.6 W, and a breakdown voltage of 6 V. Assume $V_T = 0.025$ V. Which of the following statement(s) is(are) true?

(i) It is safe to operate it in the reverse breakdown region with a current of 150 mA without damaging.

(ii) It is safe to operate it in the reverse breakdown region with a current of 90 mA without damaging.

(iii) It is safe to operate it in forward bias with a current of 0.9 mA without damaging.

(iv) It is not safe to operate it in forward bias with a current of 1.1 mA as it will damage the device.

S7. A npn BJT has a common-emitter current gain of 120, saturation current of 8.6×10^{-15} A, and Early voltage of 90 V. The temperature is 300 K.

(a) The BJT operates at a collector-emitter voltage, V_{CE} = 12 V, and has a collector current, I_C = 0.9 mA. Calculate the corresponding V_{BE} and V_{BC}, and verify the assumption made. Do not neglect Early effect, if present, in your calculations.

[Ans: V_{BE} = 0.631 V, V_{BC} = -11.369 V]

(b) The BJT is used in an amplifier circuit and operates at the bias point specified in part (a). Discuss if a small-signal i_b with a peak value of 10 μA will give rise to an amplified small-signal i_c without distortion.

S7. **Solution:**

BJT is of the npn type, β = 120, $I_S = 8.6\times10^{-15}$ A, V_A = 90 V.

(a) Assume BJT operates in the forward active mode,

$$I_C = I_S e^{V_{BE}/V_T}\left[1+\frac{V_{CE}}{V_A}\right] \quad \text{(with Early Effect)}$$

$$0.9\times 10^{-3} = 8.6\times 10^{-15} e^{V_{BE}/0.025}\left[1+\frac{12}{90}\right]$$

$$\boldsymbol{V_{BE} = 0.631\ \text{V}}$$

$$\boldsymbol{V_{BC}} = V_{BE} - V_{CE} = 0.631 - 12 = \boldsymbol{-11.369\ \text{V}}$$

BJT is of the **npn** type, as $\boldsymbol{V_{BE} > 0}$ and $\boldsymbol{V_{BC} < 0}$, BJT is in forward active mode operation.

(b) Small-signal i_b peak value, $i_{b,pk}$ = 10 μA (i.e., -10 μA ≤ i_b ≤ 10 μA)

The corresponding $i_{c,pk} = \beta \times i_{b,pk}$ = 1.2 mA (i.e., -1.2 mA ≤ i_c ≤ 1.2 mA) without distortion

The bias point collector current, I_C = 0.9 mA ⇒ maximum allowable negative small-signal i_c is -0.9 mA > -1.2 mA ⇒ small-signal i_b with peak value, $i_{b,pk}$ = 10 μA, will give rise to an amplified small-signal i_c with distortion in the negative half-cycle.

S8. An n-channel MOSFET has the following parameters: $\mu_n C_{ox} = 2.0 \times 10^{-5}$ A/V^2, $W/L = 5$, $V_{TH} = 1$ V, and $\lambda = 0.01$ V^{-1}. It is operating at the following 3 bias points:

(a) $V_{GS} = 5.0$ V, $V_{GD} = -8.0$ V
(b) $V_{GS} = 6.0$ V, $V_{GD} = 5.8$ V
(c) $V_{GS} = 0.5$ V, $V_{GD} = 2.0$ V

Specify the mode of operation (i.e., cut-off, linear or saturation) for each of the above cases, and determine the corresponding drain current (do not ignore channel-length modulation effect, if present). Explain your answers.

[Ans: $I_D = 0.904$ mA, 0.098 mA, 0 mA]

For the above case(s) in linear operation, estimate also the drain-to-source resistance. Justify the assumption used in your estimation.

[Ans: ≈ 2 kΩ]

[Note: If a number A is 10 times or more larger than another number B, then A can be considered much bigger than B, i.e., for $A >> B$]

S8. **Solution:**

- n-channel MOSFET with $\mu_n C_{ox} = 2.0 \times 10^{-5}$ A/V^2, $W/L = 5$, $V_{TH} = 1$ V, and $\lambda = 0.01$ V
- $K_n = \frac{1}{2} \times \mu_n C_{ox} \frac{W}{L} = 5 \times 10^{-5}$ A/V^2

(a) $V_{GS} = 5.0$ V, $V_{GD} = -8.0$ V

$V_{GS} = 5$ V > $V_{TH} = 1$ V $\Rightarrow$ Channel exists
$V_{DS} = V_{DG} + V_{GS} = -V_{GD} + V_{GS} = 8 + 5 = 13$ V > $(V_{GS} - V_{TH}) = 4$ V
So, MOSFET operates in saturation region.

$$I_D = K_n[V_{GS} - V_{TH}]^2(1 + \lambda V_{DS}) = 5 \times 10^{-5} \times [5-1]^2 \times (1 + 0.01 \times 13) = 0.904 \text{ mA}$$

(b) $V_{GS} = 6.0$ V, $V_{GD} = 5.8$ V

$V_{GS} = 6.0$ V > $V_{TH} = 1$ V $\Rightarrow$ Channel exists
$V_{DS} = V_{DG} + V_{GS} = -5.8 + 6.0 = 0.2$ V < $(V_{GS} - V_{TH}) = 5$ V
So, MOSFET operates in linear region.

$$I_D = 2K_n\left([V_{GS} - V_{TH}]V_{DS} - \frac{1}{2}{V_{DS}}^2\right) = 0.098 \text{ mA}$$

(c) $V_{GS} = 0.5$ V, $V_{GD} = 2$ V

$V_{GS} = 0.5$ V < $V_{TH} = 1$ V $\Rightarrow$ no channel $\Rightarrow$ no drain current regardless of V_{DS} value.
So, MOSFET in cut-off operation. V_{DS} value is irrelevant.

$I_D = 0$ A

Only for (b), where $V_{GS} = 6.0$ V, $V_{GD} = 5.8$, MOSFET is in linear operation.

$V_{DS} = 0.2$ V << $(V_{GS} - V_{TH}) = 5$ V [i.e., V_{DS} is more than 10 times smaller than $(V_{GS} - V_{TH})$]

$\Rightarrow$ Drain-to-source resistance, $R_{DS} = \frac{V_{DS}}{I_D}|_{small\ V_{DS}} \approx 1/[2K_n(V_{GS} - V_{TH})]$

$$R_{DS} \approx \frac{1}{\left[2 \times \frac{1}{2} \times 2.0 \times 10^{-5} \times 5 \times (6-1)\right]} = 2 \text{ k}\Omega$$