NATIONAL UNIVERSITY OF SINGAPORE
Department of Electrical and Computer Engineering

EE2027 Electronic Circuits
Tutorial 2: Solution

- Unless otherwise stated, you may assume temperature, $T = 300$ K; thermal voltage, $V_T = 0.025$ V and make use of the equations given in the lecture notes directly, without having to derive them.
- All the symbols are as defined in the lecture notes.

Homework 2:
Homework 2 has 1 question, Question 4 of Tutorial 2. You will need to submit a softcopy of your handwritten homework to the Canvas folder: Home>Homework Assignments>HW2 half an hour after class (i.e., latest by 12.30 pm) on Thursday, 19 September 2024.

The softcopy submission of your homework must be in PDF format and in a single file. Name your file following the convention "Your_Name_HW2.pdf". Failing to do that will mean zero mark for homework.

Homework questions will not be discussed in class.

Q1.

(a) To amplify input signal of $v_1(t) = 0.01\times\sin(2\pi\times 10\text{kHz}\times t)$ using an inverting amplifier with gain of -10, determine the minimum required GBW for the opamp.

(3 marks)

(b) To amplify input signal of $v_2(t) = 0.1\times\sin(2\pi\times 500\text{kHz}\times t)$ using an inverting amplifier with gain of -10, determine the minimum required GBW for the opamp.

(3 marks)

(c) You are given only **one** opamp A with GBW of 200 kHz and **two** opamp B with GBW of 8 MHz. Design an opamp circuit that will give an output voltage of $v_{out}(t) = 0.1\times\sin(2\pi\times 10\text{kHz}\times t) + 1\times\sin(2\pi\times 500\text{kHz}\times t)$ with the two input signals from (a) and (b).

(7 marks)

(d) You are given only **one** opamp A with GBW of 200 kHz and **two** opamp B with GBW of 8 MHz. Design an opamp circuit that will give an output voltage of $v_{out}(t) = 1\times\sin(2\pi\times 10\text{kHz}\times t) + 1\times\sin(2\pi\times 500\text{kHz}\times t)$ with the two input signals from (a) and (b).

(7 marks)

Q1: **Solution**

(a) To amplify input signal of $v_1(t) = 0.01\times\sin(2\pi\times10\text{kHz}\times t)$ using an inverting amplifier with gain of -10, determine the minimum required GBW for the opamp.

$$f_{3dB,CL} = GBW \times \frac{R_1}{R_1 + R_2} \Rightarrow GBW = f_{3dB,CL} \times 11 = 110 \text{ kHz}$$

The opamp needs to have GBW of at least 110 kHz.

(3 marks)

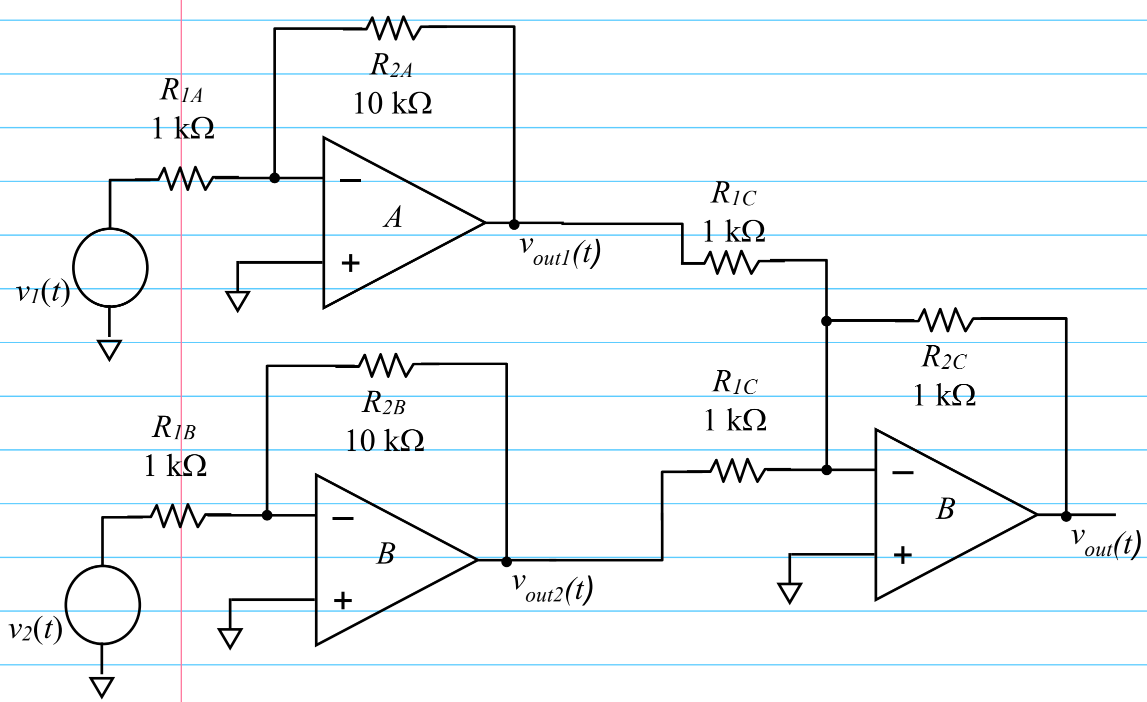
(b) To amplify input signal of $v_2(t) = 0.1\times\sin(2\pi\times500\text{kHz}\times t)$ using an inverting amplifier with gain of -10, determine the minimum required GBW for the opamp.

$$f_{3dB,CL} = GBW \times \frac{R_1}{R_1 + R_2} \Rightarrow GBW = f_{3dB,CL} \times 11 = 5.5 \text{ MHz}$$

The opamp needs to have GBW of at least 5.5 MHz.

(3 marks)

(c) You are given only **one** opamp A with GBW of 200 kHz and **two** opamp B with GBW of 8 MHz. Design an opamp circuit that will give an output voltage of $v_{out}(t) = 0.1\times\sin(2\pi\times10\text{kHz}\times t)+1\times\sin(2\pi\times500\text{kHz}\times t)$ with the two input signals from (a) and (b).



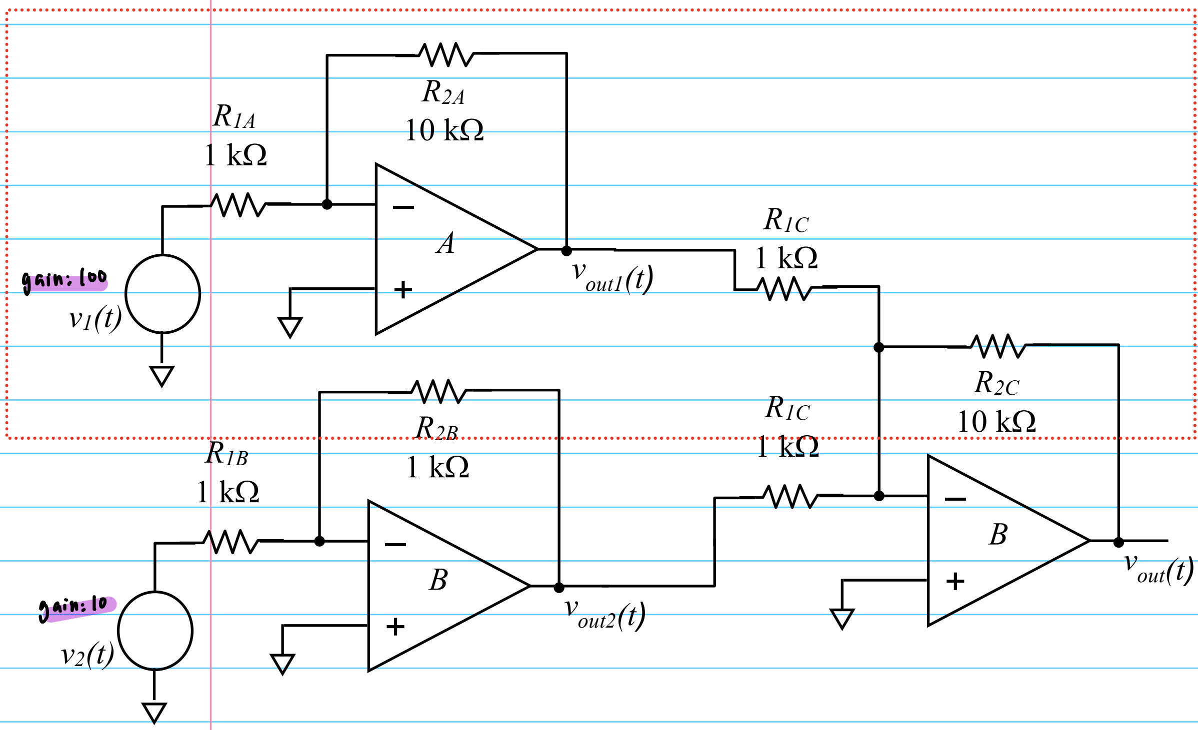
The first inverting amplifier using opamp A (lower GBW) with gain of -10 will give v_{out1}(t) = - 0.1×sin(2π×10kHz×t). Opamp B (higher GBW) should not be used here as it will be wasted. Opamp B (whose quantity is limited to only two pieces) is required for other parts of the circuit involving a higher frequency (i.e., 500 kHz) input signal to meet the GBW requirement.

The second inverting amplifier using opamp B (higher GBW) with gain of -10 will give v_{out2}(t) = - 1×sin(2π×500kHz×t). Opamp A cannot be used due to its lower GBW.

The third summing amplifier using opamp B (higher GBW) with gain of -1 will give v_{out}(t) = 0.1×sin(2π×10kHz×t) + 1×sin(2π×500kHz×t). Opamp B is required here to meet the GBW requirement as one of the input signals to the summing amplifier involves a higher frequency (i.e., 500 kHz) input signal.

(7 marks)

(d) You are given only **one** opamp A with GBW of 200 kHz and **two** opamp B with GBW of 8 MHz. Design an opamp circuit that will give an output voltage of v_{out}(t) = 1×sin(2π×10kHz×t) + 1×sin(2π×500kHz×t) with the two input signals from (a) and (b).



The first inverting amplifier using opamp A (lower GBW) with gain of -10 will give v_{out1}(t) = - 0.1×sin(2π×10kHz×t). Opamp B (higher GBW) should not be used here as it will be wasted. Opamp B (whose quantity is limited to only two pieces) is required for other parts of the circuit involving a higher frequency (i.e., 500 kHz) input signal to meet the GBW requirement.

The second inverting amplifier using opamp B (higher GBW) with gain of -1 will give $v_{out2}(t) = -0.1\times\sin(2\pi\times500\text{kHz}\times t)$. Opamp A cannot be used due to its lower GBW.

The third summing amplifier using opamp B (higher GBW) with gain of -10 will give $v_{out}(t) = 1\times\sin(2\pi\times10\text{kHz}\times t) + 1\times\sin(2\pi\times500\text{kHz}\times t)$. Opamp B is required here to meet the GBW requirement as one of the input signals to the summing amplifier involves a higher frequency (i.e., 500 kHz) input signal.

(7 marks)

Q2. (a) Derive the equivalent resistance, $R_x = v_x / i_x$, for the circuit shown in Fig. Q2(a). Note that v_1 is a dependent voltage source.

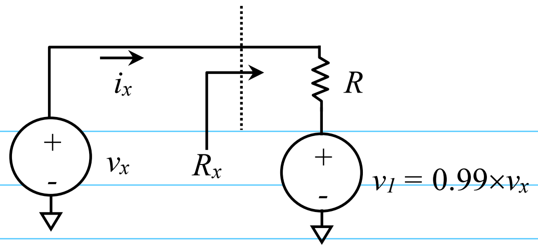


Fig. Q2(a)

(b) The dependent voltage source, v_1 of Fig. Q2(a) is implemented as shown in Fig. Q2(b) below. Derive the value of k such that $v_1 = 0.99 v_x$.

[Ans. $k = 1.97$]

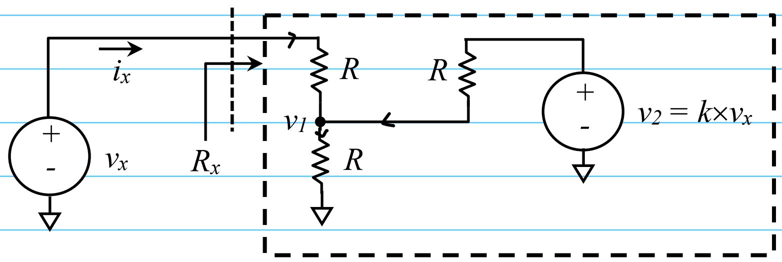


Fig. Q2(b)

(c) Design an opamp circuit that can realize the circuit within the dashed box shown in Fig. Q2(b). You may treat v_x as an independent signal source.

(d) The designed opamp circuit in part (c) is known as a **resistance multiplier**. It can realize a huge equivalent resistance with relatively small resistor values. Suggest and show a simple filtering circuit that can make use of this technique.

Q2. <u>Solution</u>:

(a) Derive the equivalent resistance, $R_x = v_x / i_x$, for the circuit shown in Figure Q2 (a). Note that v_I is a dependent voltage source.

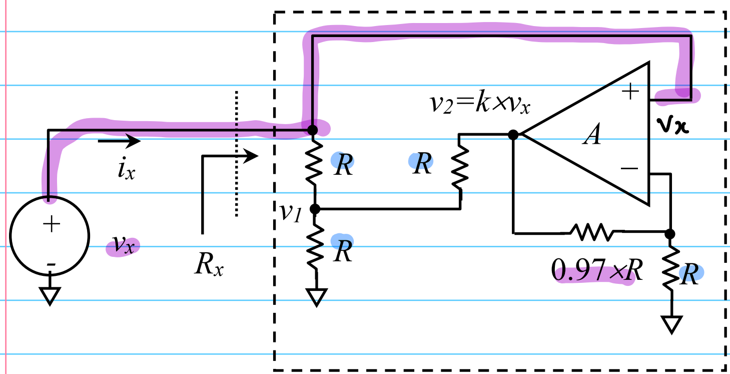
$$i_x = \frac{v_x - 0.99v_x}{R} = \frac{0.01v_x}{R} \Rightarrow R_x = \frac{v_x}{i_x} = 100R.$$

(b) The dependent voltage source, v_I of Fig. Q2(a) is implemented as shown in Fig. Q2(b) below. Derive the value of k such that $v_I = 0.99v_x$ Derive the value k for the circuit shown in Fig. Q2 (b) such that $v_I = 0.99v_x$.

Apply KCL at point v_I, and apply $v_I = 0.99v_x$ as required -

$$\frac{v_x - v_1}{R} + \frac{v_2 - v_1}{R} = \frac{v_1}{R}$$
$$\frac{v_x - 0.99v_x}{R} + \frac{kv_x - 0.99v_x}{R} = \frac{0.99v_x}{R}.$$
$$\Rightarrow k = 1.97$$

(c) Design an opamp circuit that can realize the circuit within the dashed box shown in Fig. Q2 (b). You may treat v_x as an independent signal source.



non-inverting amplifier
gain: $(1 + \frac{R_2}{R_1})$
↓
$1.97 - 1 = 0.97$

Since $v_2 = kv_x$ where k is a positive value of 1.97, if you search through the opamp library, you can see that the non-inverting amplifier fits the requirement. Hence, we replace the $v_2 = kv_x$ by a non-inverting amplifier.

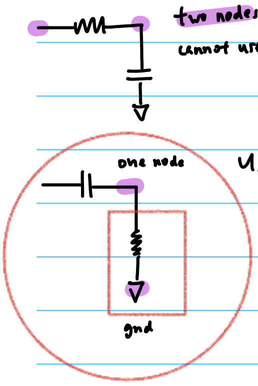
5 resistors multiplied to 100R (part a) equivalent

(d) The designed circuit in part (c) is known as a **resistance multiplier**. It can realize a huge equivalent resistance with relatively small resistor values. Suggest and show a simple filtering circuit that can make use of this technique.

↓
think of simple RC filter

As shown in part (c), the circuit in the dashed box presents an equivalent resistance of $R_x = 100R$ between one terminal and ground, hence we can use the circuit in the dashed box to replace a resistor. As shown below, the resistor in a passive high pass filter can be replaced by the opamp circuit, between one node (v_{out}) and ground.

simple RC/CR filter

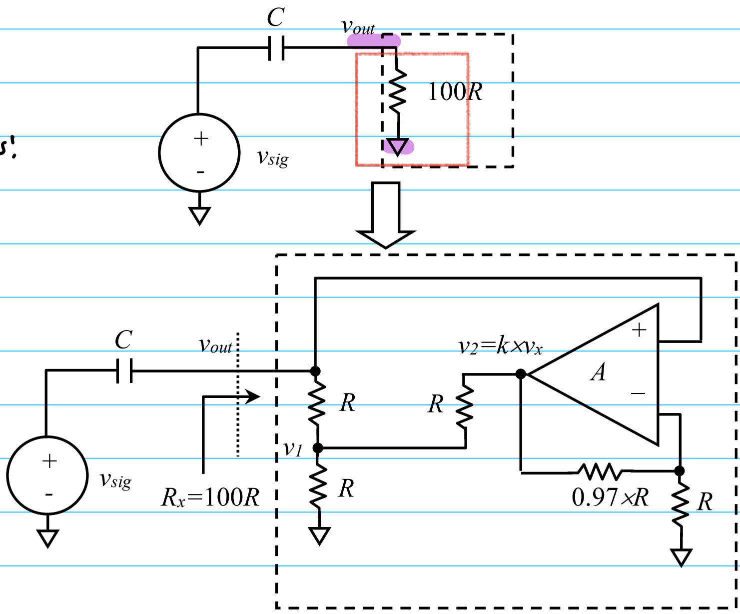


two nodes, so cannot use

one node

use this!

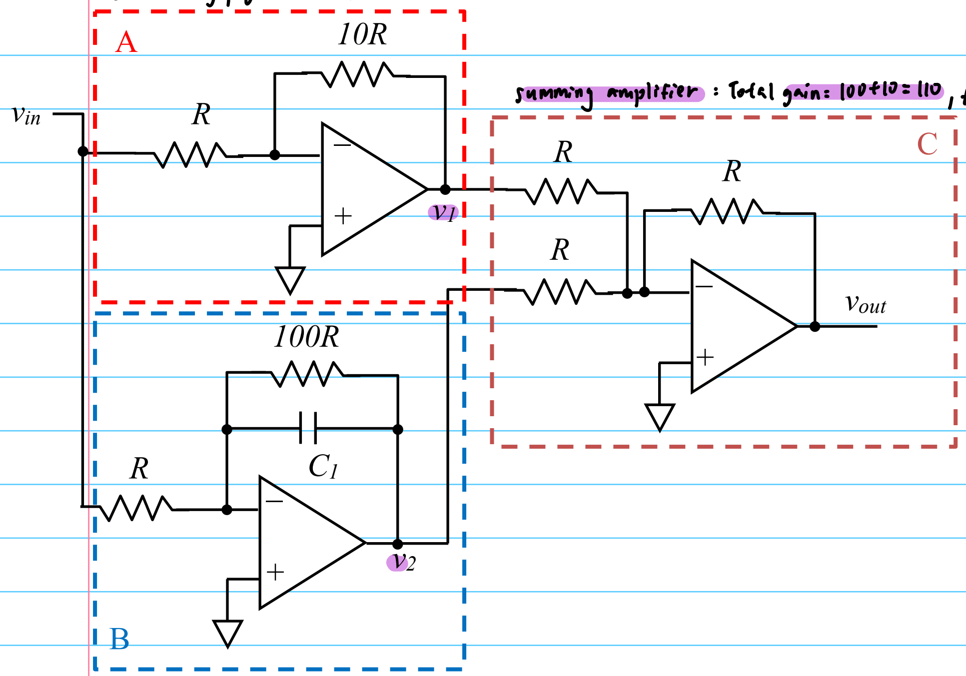
gnd



Q3. Figure Q3 shows an opamp circuit composed of 3 sub-circuits, which are shown in the three boxes, labelled as A, B and C.

Inverting, gain of 10, 20dB

summing amplifier : Total gain: 100+10=110, take 20log(110) ≈ 40 dB



First-order lowpass : Gain: 100, 40dB

Fig. Q3

The capacitance C_1 in Fig. Q3 has a value such that

$$\frac{1}{2\pi \times C_1 \times 100R} = 1\text{ kHz.}$$ → low pass cut-off, graph starts to go down

(a) Identify the function of each of the opamp sub-circuits.

(b) Sketch the Bode plots of the transfer functions v_1/v_{in}, v_2/v_{in} and v_{out}/v_{in}.

A Bode plot is a plot of the gain in decibels (dB) versus the frequency f (in $\log_{10}$ scale). Gain (dB) = $20\times\log_{10}(|v_{out}/v_{in}|)$. For example, a gain of 40 dB is equivalent to $|v_{out}/v_{in}| = 100$.

You may use the Semilog paper attached to sketch the Bode plots.

Q3. <u>**Solution**</u>**:**

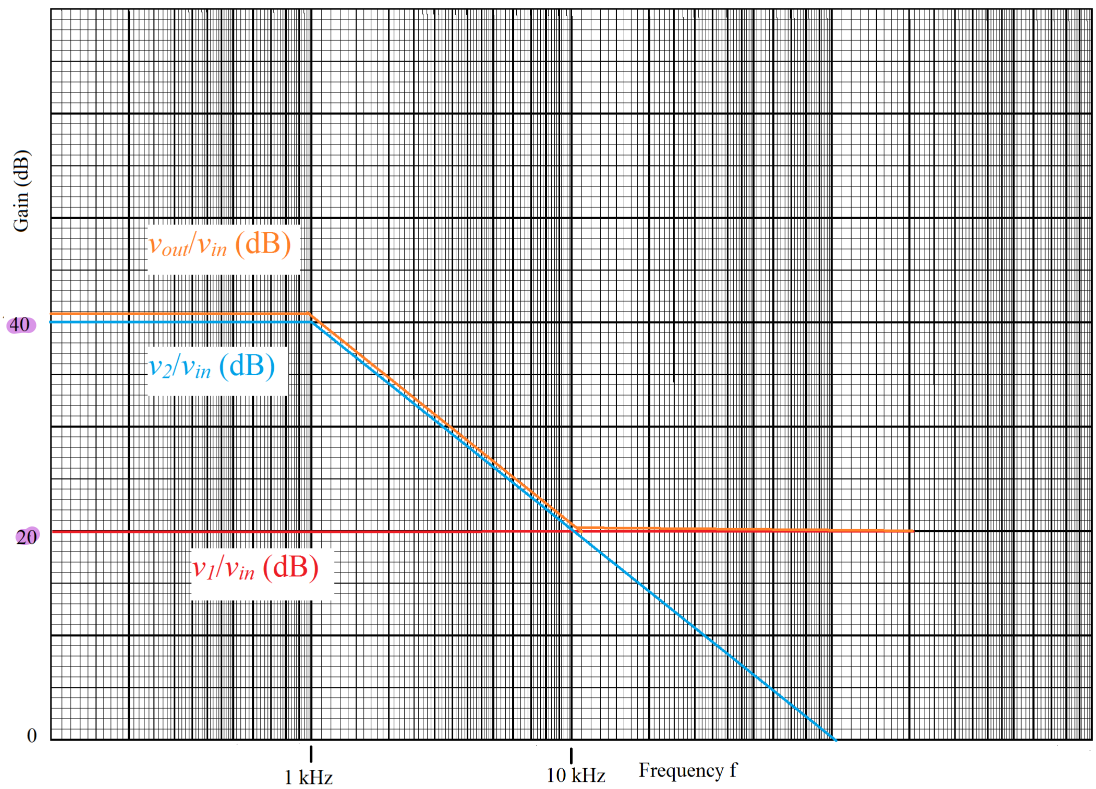
(a) Identify the function of each of the opamp sub-circuits.

<u>Sub-circuit A</u>: an inverting amplifier of |gain| = $|v_1/v_{in}|$ = 10, or 20×$\log_{10}$(10) = 20 dB. See Bode plot of v_1/v_{in} in semilog graph below.

<u>Sub-circuit B</u>: a first order low pass filter of 3 dB frequency, $f_{3dB} = \dfrac{1}{2\pi \times C_1 \times 100R}$ = 1 kHz, and a low frequency |gain| = $|v_2/v_{in}|$ = 100, or 20×$\log_{10}$(100) = 40 dB. For frequency beyond f_{3dB}, gain falls at a rate of 20 dB/decade of frequency. See Bode plot of v_2/v_{in} in semilog graph below.

<u>Sub-circuit C</u>: a summing amplifier, which sums the outputs of sub-circuits A and B: $v_{out} = v_1 + v_2$. The overall circuit has a low frequency |gain| = $|v_{out}/v_{in}| = |v_1/v_{in}| + |v_2/v_{in}|$ = 110, or 20×$\log_{10}$(110) = 40.8 dB, with the same first order frequency response as the low pass filter (sub-circuit B) from 1 to 10 kHz. See Bode plot of v_{out}/v_{in} in semilog graph below.

(b) Bode plots of v_1/v_{in}, v_2/v_{in} and v_{out}/v_{in}:



Q4. (a) Derive the equivalent impedance (Z_x) for the opamp circuit shown in Fig. Q4(a) in terms of R_1, R_2 and C_3. Hence, show that Z_x corresponds to the impedance of a negative capacitance ($- C_x$).

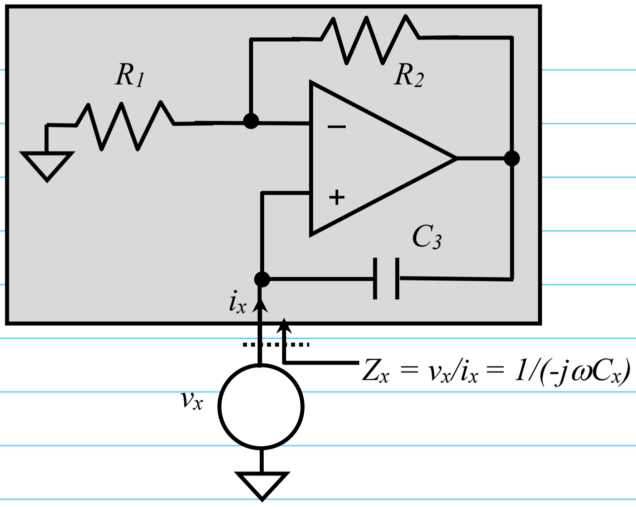


Fig. Q4(a)

(b) The LC network shown in Fig. Q4(b) exhibits a resonant frequency of $\frac{1}{2\pi\sqrt{LC}}$. Using the circuit depicted in Fig. Q4(a), show how the resonant frequency of the LC network can be changed if R_1 in Fig. Q4(a) is replaced by a variable resistor.

Derive also the resonant frequency in terms of the variable resistor.

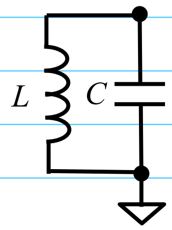


Fig. Q4(b)

Q4. <u>Solution</u>:

(a) By virtual short :

$$V_- = V_+ = v_x$$

Using $i_- = 0$, $V_o \times \frac{R_1}{R_1+R_2} = V_- = v_x$ [V_o is the output terminal voltage of opamp]

$$\Rightarrow V_o = v_x \times \left(1 + \frac{R_2}{R_1}\right)$$

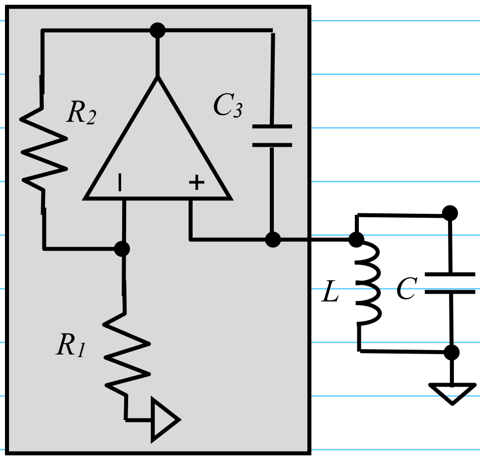
Using $i_+ = 0$, $i_x = i_c = \frac{v_x - V_o}{\frac{1}{sC_3}} = v_x \frac{\left(-\frac{R_2}{R_1}\right)}{\frac{1}{sC_3}} = -v_x \frac{sC_3R_2}{R_1}$ [i_c is the capacitor current]

$$Z_x = \frac{v_x}{i_x} = -\frac{R_1}{sC_3R_2}$$

[Note: $s \equiv j\omega \equiv j2\pi f$]

The equivalent capacitance value is $-\frac{C_3R_2}{R_1}$ (a negative value).

(b) Connect the circuit of Fig. Q4(a) in parallel to the LC network –



Capacitance of the LC network becomes $\left(C - \frac{C_3R_2}{R_1}\right)$

Resonant frequency, $f = \frac{1}{2\pi\sqrt{L\left(C - \frac{C_3R_2}{R_1}\right)}}$

By varying R_1, the total capacitance can be changed, and thus the resonant frequency f can be changed.

Q5.

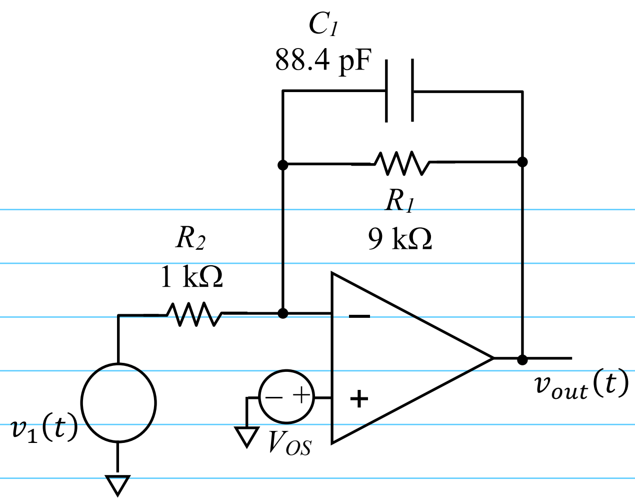


Fig. Q5 First order low-pass filter.

The opamp used in Fig. Q5 has a GBW of 2 MHz and an input offset voltage of V_{OS} = 20 mV. The opamp is powered by ± 5 V supplies.

$f_{3db} = \frac{1}{2\pi R_1 C_1}$

(a) Ignoring the GBW effect of the opamp, estimate the 3dB cut-off frequency of the first order lowpass filter and its gain shown in Fig. Q5.

[Ans. 200 kHz, $-9 \times \frac{1}{1+j\omega\times 7.96\times 10^{-7}}$]

(b) With the capacitor C_1 removed from the circuit, estimate the closed-loop 3dB cut-off frequency of the resulting circuit, taking into consideration the GBW effect.

[Ans. 200 kHz]

(c) If the GBW effect is considered, discuss the expected gain at the cut-off frequency of part (a).

[Ans. 13.1 dB]

(d) If $v_1(t)$ has a frequency well below the 3dB cut-off frequency of part (a), can we treat the capacitor C_1 as an open circuit? Explain your reasoning.

(d) If a sinusoidal voltage, $v_1(t) = v_{pk} \times sin(2\pi \times 10\text{k} \times t)$, is applied to the circuit, estimate the maximum allowable v_{pk} such that $v_{out}(t)$ is without distortion.

[Ans. 0.53 V]

(f) Suggest two methods, without changing the opamp, which can increase the maximum allowable v_{pk} in part (e).

Q5. <u>Solution</u>:

(a) Ignoring the GBW effect of the opamp, estimate the 3dB cut-off frequency of the first order lowpass filter and its gain in Fig. Q5.

$$f_{3dB,LPF} = \frac{1}{2\pi R_1 C_1} = 200 \text{ kHz}$$

$$\text{Gain} = -\frac{R_1}{R_2} \times \frac{1}{1+j\omega R_1 C_1} = -9 \times \frac{1}{1+j\omega \times 7.96\times10^{-7}}$$ (pg 77 notes)

(b) With the capacitor C_1 removed from the circuit, estimate the closed-loop 3dB cut-off frequency of the resulting circuit, taking into consideration the GBW effect.

The resulting circuit with capacitor C_1 removed is an inverting amplifier. The closed-loop 3dB cut-off frequency is

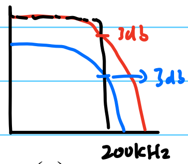
$$f_{3dB,CL} = GBW \times \frac{R_2}{R_1 + R_2} = 200 \text{ kHz}$$

(c) If the GBW effect is considered, discuss the expected gain at the cut-off frequency of part (a).

part (a) part (b)

At 200 kHz, as C_1 will contribute -3dB and GBW will contribute another -3dB, the gain will drop to - 6dB. The expected gain at 200 kHz will be:

$$20\, log_{10}\left(\frac{R_1}{R_2}\right) - 6 = 20\, log_{10}(9) - 6 = 13.1 \text{ dB}$$



(d) If $v_1(t)$ has a frequency well below the 3dB cut-off frequency of part (a), can we treat the capacitor C_1 as an open circuit? Explain your reasoning.

↓ 200kHz

Yes, the capacitor can be treated as an open circuit. This is because the gain magnitude is constant ($= R_1/R_2$) for frequencies smaller than the 3dB cut-off frequency.

→ treat capacitor open circuit at low frequencies.
treat capacitor short circuit at high frequencies

(e) If a sinusoidal voltage, $v_1(t) = v_{pk} \times sin(2\pi \times 10k \times t)$, is applied to the circuit, estimate the maximum allowable v_{pk} such that $v_{out}(t)$ is without distortion. → $\boxed{\text{either slew-rate, offset}}$

if qtn give both, check both, find the bottleneck (lower value)

Using the result of part (d), at signal frequency of 10 kHz ($\ll f_{3dB,CL} = 200$ kHz), LPF becomes effectively an inverting amplifier.

$$v_{out}(t) = V_{OS} \times \left(1 + \frac{R_1}{R_2}\right) + v_1(t) \times \left(-\frac{R_1}{R_2}\right); \text{ where } -5\text{V} < v_{out}(t) < 5\text{V}$$

$$-5\text{V} < 20\text{mV} \times 10 - 9v_{pk}\sin(2\pi \times 10\text{k} \times t) < 5\text{V}$$

$$-5.2\text{V} < -9v_{pk}\sin(2\pi \times 10\text{k} \times t) < 4.8\text{V}$$

$$-0.53\text{V} < v_{pk}\sin(2\pi \times 10\text{k} \times t) < 0.58\text{V}$$

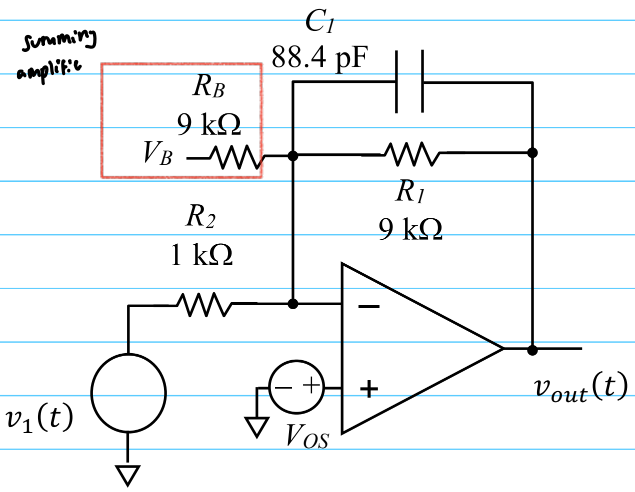
Considering a symmetrical sinusoidal voltage, v_{pk} cannot exceed 0.53 V. Maximum allowable v_{pk} would be 0.53 V.

(f) Suggest two methods without changing the opamp which can increase the maximum allowable v_{pk} in part (e).

↳ get rid of offset → use summing amplifier

Method 1:

We can employ a summing amplifier by adding an additional resistor R_B and an additional DC voltage V_B to compensate the effect of V_{OS} -



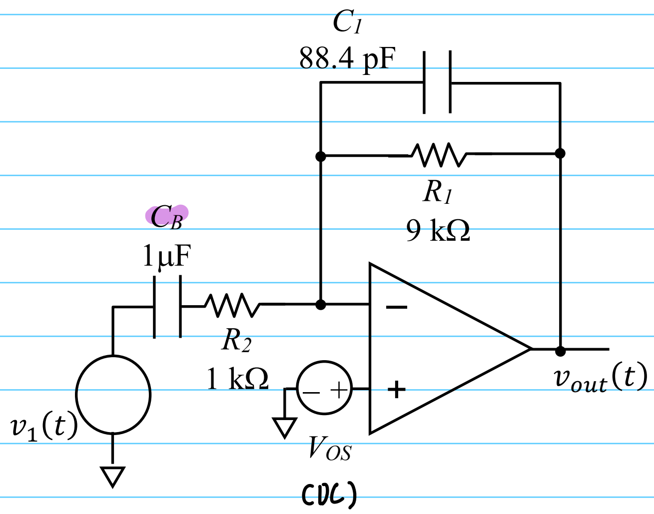
$$v_{out}(t) = V_{OS} \times \left(1 + \frac{R_1}{R_2}\right) + v_1(t) \times \left(-\frac{R_1}{R_2}\right) + V_B \times \left(-\frac{R_1}{R_B}\right)$$

As an example, for R_B = 9 kΩ, V_B of 200 mV can be added to compensate the V_{OS} effect. Maximum allowable v_{pk} would be ~0.56 V.

$V_1(t) \times \left(-\frac{R_1}{R_2}\right)$, see part (e), 20mV offset with gain: 10 compensated

Method 2: capacitor behave like open circuit in DC

We can employ a DC block capacitor C_B, as shown in the circuit below. C_B should be chosen such that its impedance is much smaller than R_2 at frequency of the desired signal (i.e., 10 kHz).



$$-5\text{V} < v_{out}(t) = V_{OS} \times \left(1 + \frac{R_1}{\infty}\right) + v_1(t) \times \left(-\frac{R_1}{R_2}\right) = v_{OS} + v_1(t) \times \left(-\frac{R_1}{R_2}\right) < 5\text{V}$$

In this case, V_{OS} is not amplified by 10 times (as C_B is an open circuit under DC), $9v_{pk}$ would now be between -4.98 and 5.02 V. Due to symmetry consideration, maximum allowable v_{pk} would be 0.55 V.

Note: when considering the effect of V_{OS}, it is DC analysis, and C_B is an open circuit.

Q6. The opamp used in Fig. Q6 has a GBW of 0.5 MHz, a slew rate of 0.5 V/µs, an offset voltage of 20 mV, and a noise voltage spectral density of 20nV/√Hz.

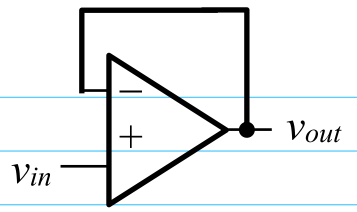


Fig. Q6

(a) Estimate the $f_{3dB,CL}$ of the circuit shown in Fig. Q6.

[Ans. 0.5 MHz]

(b) What is the minimum peak voltage of v_{in} that can be fed to the circuit?

[Ans. $v_{in,pk,min} = 25$ µV]

(c) What is the maximum peak voltage of v_{in} that can be fed to the circuit, assuming that a signal up to $f_{3dB,CL}$ is sent to the circuit?

[Ans. $V_{in,pk,max} = 0.159$ V]

(d) Sketch the v_{out} using the v_{in} of part (c).

Q6. <u>Solution</u>:

(a) Estimate the $f_{3dB,CL}$ for the circuit (a unity gain buffer) -

$$|\beta G(j\omega_{3dB,CL})| = 1$$

$$\Rightarrow |A(j\omega_{3dB,CL})| \approx \left|\frac{2\pi \times GBW}{j\omega_{3dB,CL}}\right| = 1$$

$$\Rightarrow f_{3dB,CL} = GBW = 0.5 \text{ MHz}$$

(b) What is the minimum peak voltage of v_{in} that can be fed to the circuit?

$$v_{out\_noise,rms} \approx \sqrt{V_n^2 \times 0.5\text{MHz} \times \frac{\pi}{2}} = 17.7\ \mu\text{V}$$

$$\Rightarrow v_{in,pk,min} \approx v_{out_{noise},rms} \times \sqrt{2} = 25\ \mu\text{V}$$

(c) What is the maximum peak voltage of v_{in} that can be fed to the circuit assuming signal up to $f_{3dB,CL}$ is sent to the circuit?

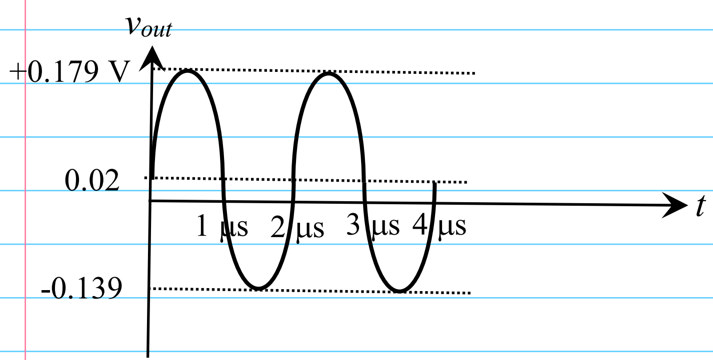
$$\frac{dV_{out}}{dt} \approx 2\pi \times 0.5\text{MHz} \times V_{out,pk} sin(2\pi \times 0.5\text{MHz} \times t) < 0.5\ \text{V}/\mu\text{s}$$

$$\Rightarrow V_{out,pk} < 0.159\ \text{V} \Rightarrow V_{in,pk,max} = 0.159\ \text{V}$$

Note: $V_{out,pk}$ is not linited by V_{OS} as supply voltage is not given.

(d) Sketch the v_{out} using the v_{in} in part (c).

v_{out} has a dc offset of V_{OS} -



Q7. As shown in Fig. Q7, a triangular wave $v(t)$, with $v_{pk\text{-}pk}$ of 2 V and period of 4T, is fed to the two opamp circuits.

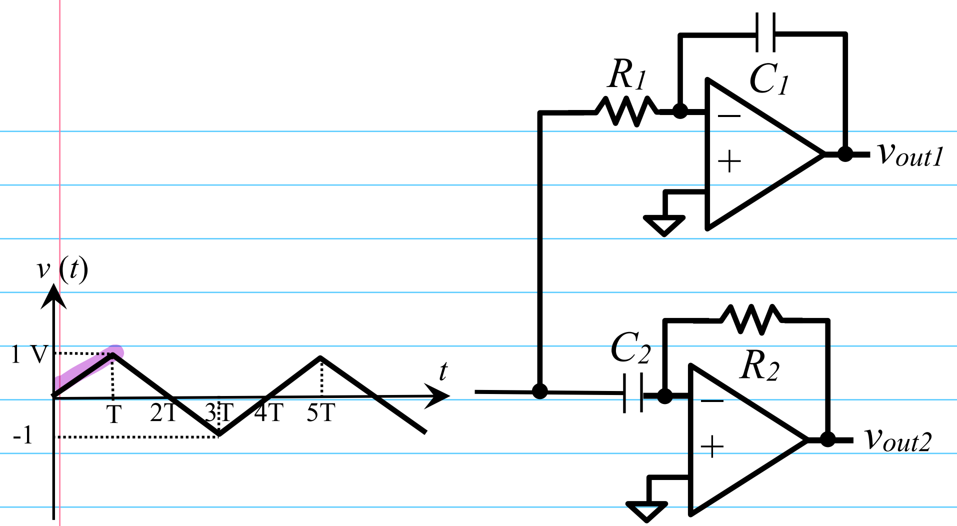


Fig. Q7

(a) Sketch and label the output waveforms, v_{out1} and v_{out2}.

$V_{\text{peak to peak}}$: $V_p = 1V$

(b) Derive the relationship between R_2 and C_2 such that v_{out2} also has $v_{pk\text{-}pk}$ of 2 V.

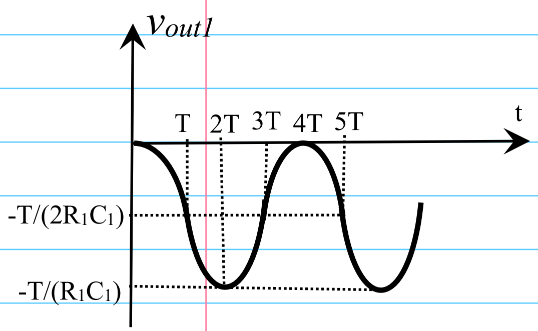
Q7. Solution:

finding area

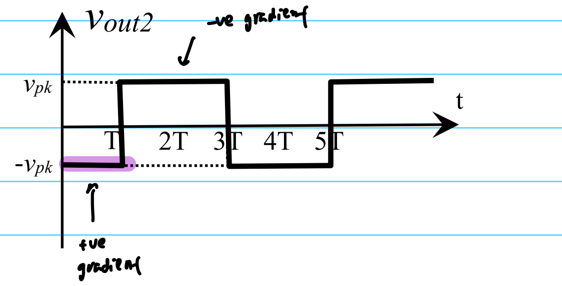
(a) v_{out1} is a function of the integration of v(t), while v_{out2} is a function of the differentiation of v(t).

finding gradient

(inverting)



(inverting)



Note: v_{out1} is not sinusoidal.

gradient : $\left(\frac{1-(-1)}{T-3T}\right) = \left(\frac{-2V}{2T}\right)$

(b) $$v_{pk} = \underbrace{-R_2C_2\frac{dv(t)}{dt}}_{\text{pg 70 notes}} = -R_2C_2\left(\frac{-2V}{2T}\right) = 1\text{V} \Rightarrow R_2C_2 = T$$

Q8. (a) If $v_1(t) = cos(2\pi \times 100000 \times t)$, determine the $dv_1(t)/dt$.

(b) If $v_2(t) = cos(2\pi \times 200000 \times t)$, determine the $dv_2(t)/dt$.

(c) Design an opamp circuit that can perform differentiation on $v_1(t)$ in (a), and give rise to a peak output value of 0.1 V. Verify that the circuit obtained can be applied to $v_2(t)$ in (b) and give rise to a peak output value of 0.2 V. [You need to specify the component values used in your opamp circuit.]

(d) A super diode circuit is used to convert the output from (c). Sketch the resulting output voltage of the super diode circuit if $v_1(t)$ is applied to (c). Repeat the same if $v_2(t)$ is applied to (c). You should indicate clearly the key characteristics of the two waveforms you plot.

(e) A RC network shown in Fig. Q8 can be connected to the super diode circuit output of (d) to form a peak detector, i.e., it can detect 0.1 V or 0.2 V, respectively from (d) if $v_1(t)$ or $v_2(t)$ is used. The capacitor in the RC network will charge up to the highest voltage detected at the output of the super diode circuit and hold on to this voltage if the RC time constant is large (i.e., RC network functions as a peak detector). A comparator can then be used to differentiate whether the signal is from $v_1(t)$ or $v_2(t)$. Draw the whole system that consists of part (c), (d), RC network and the comparator. Suggest the threshold voltage for the comparator.

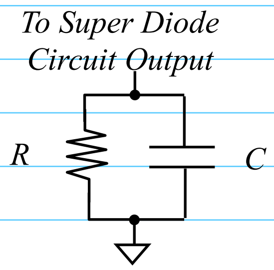


Fig. Q8

(f) Suppose all the opamps used in (e) have offset voltage of +20 mV, comment on its impact on the overall performance for (e).

Q8. <u>Solution</u>:

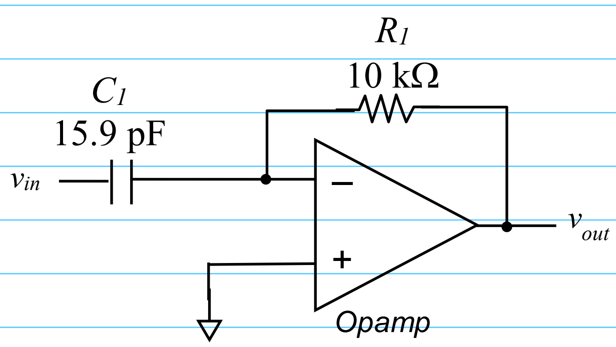
(a) If $v_1(t) = cos(2\pi\times 100000\times t)$, determine the $dv_1(t)/dt$.

$$\frac{dv_1(t)}{dt} = -2\pi \times 100000 \times sin(2\pi \times 100000 \times t)$$

(b) If $v_2(t) = cos(2\pi\times 200000\times t)$, determine the $dv_2(t)/dt$.

$$\frac{dv_2(t)}{dt} = -2\pi \times 200000 \times sin(2\pi \times 200000 \times t)$$

(c) Design an opamp circuit that can perform differentiation on $v_1(t)$ in (a), and give rise to a peak output value of 0.1 V. Verify that the circuit obtained can be applied to $v_2(t)$ in (b) and give rise to a peak output value of 0.2 V. [You need to specify the component values used in your opamp circuit.]



Using a differentiator circuit - $v_{out}(t) = -R_1C_1\frac{dv_{in}(t)}{dt}$

$$|v_{out}(t)| = |R_1C_1 \times 2\pi \times 100000 \times sin(2\pi \times 100000 \times t)| \leq 0.1$$

$$R_1C_1 \times 2\pi \times 100000 = 0.1$$

$$R_1C_1 = \frac{0.1}{2\pi \times 100000}$$

Select $R_1 = 10$ kΩ, and $C_1 = 15.9$ pF

[<u>Note</u>: Other combinations of R_1 and C_1 are also possible, provided $R_1C_1 = 1.59 \times 10^{-7}$]

<u>Verification that the circuit is applicable to (b):</u>

$$|v_{out}(t)| = |R_1C_1 \times 2\pi \times 200000 \times sin(2\pi \times 200000 \times t)| \leq 0.2$$

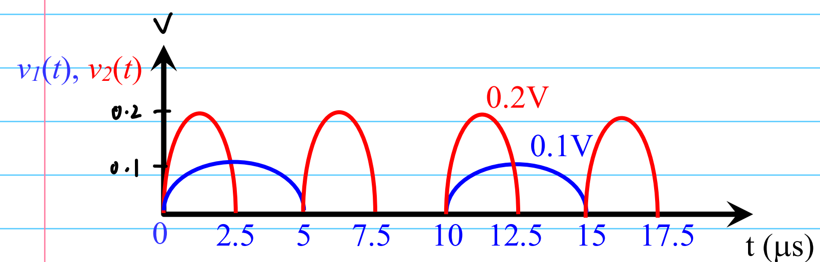
As, $R_1C_1 \times 2\pi \times 200000 = 0.2$ V

→ half-wave rectifier

(d) A super diode circuit is used to convert the output from (c). Sketch the resulting output voltage of the super diode circuit if $v_1(t)$ is applied to (c). Repeat the same if $v_2(t)$ is applied to (c). You should indicate clearly the key characteristics of the two waveforms you plot.

- Frequency of $v_1(t)$ = 100 kHz ⇒ period = 10 μS
- Frequency of $v_1(t)$ = 200 kHz ⇒ period = 5 μS

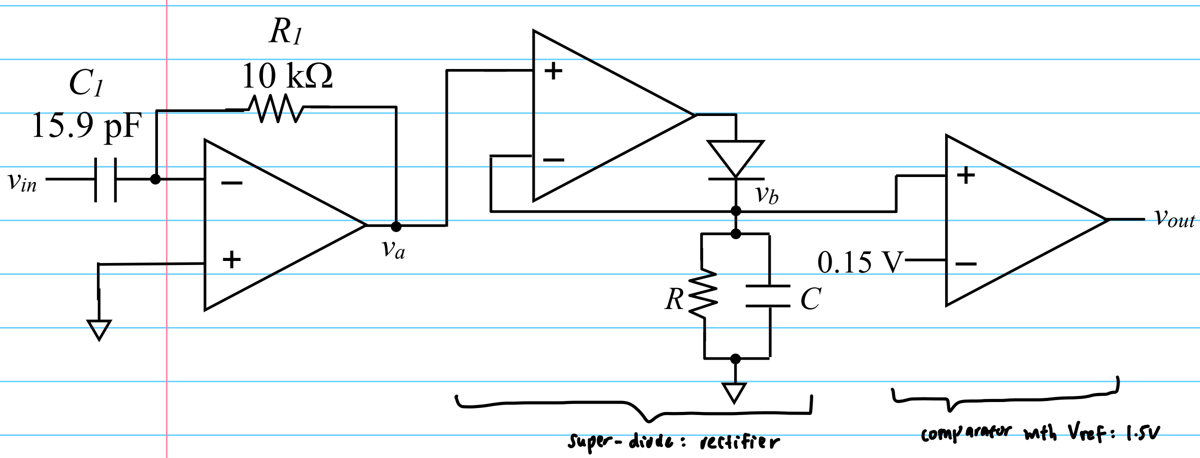
$v_2(t)$



Blue waveform: Output of super diode circuit for $v_1(t)$
Red waveform: Output of super diode circuit for $v_2(t)$

(e) A RC network shown in Fig. Q8 can be connected to the super diode circuit output of (d) to form a peak detector, i.e., it can detect 0.1 V or 0.2 V, respectively from (d) if $v_1(t)$ or $v_2(t)$ is used. The capacitor in the RC network will charge up to the highest voltage detected at the output of the super diode circuit and hold on to this voltage if the RC time constant is large (i.e., RC network functions as a peak detector). A comparator can then be used to differentiate whether the signal is from $v_1(t)$ or $v_2(t)$. Draw the whole system that consists of part (c), (d), RC network and the comparator. Suggest the threshold voltage for the comparator.

pg 92 notes → superdiode already have resistor so just need to add capacitor to form RC network

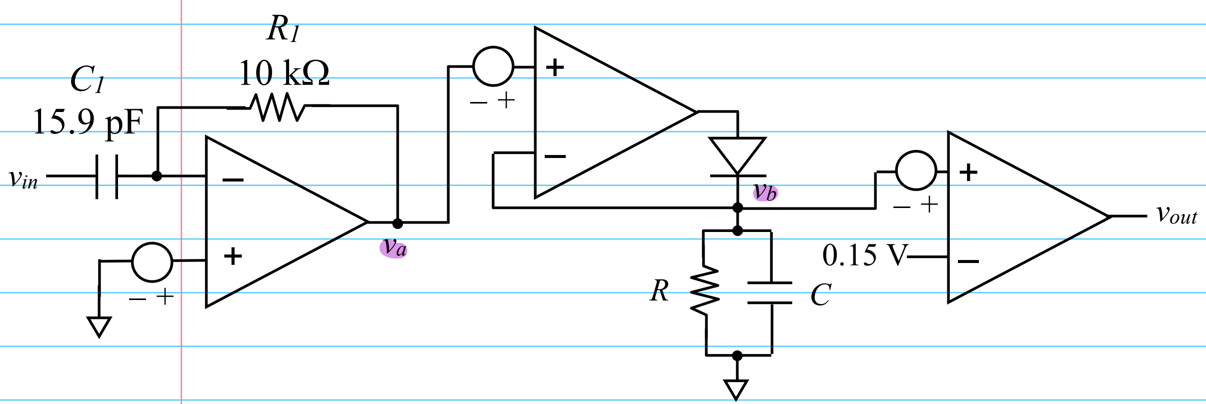


Select threshold voltage to be 0.15 V (i.e., midway between 0.1 V and 0.2 V)
(Vref)

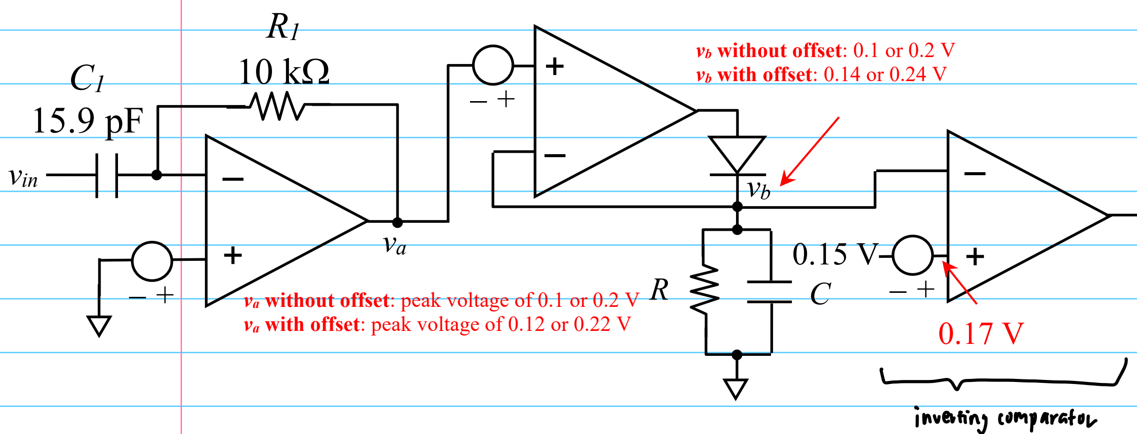
Note:
If $v_{in} = v_1(t)$, $v_b = 0.1$ V and $v_{out} = -V_{DD}$
If $v_{in} = v_2(t)$, $v_b = 0.2$ V and $v_{out} = +V_{DD}$

(f) Suppose all the opamps used in (e) have offset voltage of +20 mV, comment on its impact on the overall performance for (e).

When there is no input ($v_{in} = 0$), v_a will exhibit +20 mV. v_b will exhibit +40 mV (20 mV due to v_a). The non-inverting terminal $V+$ of the last opamp will be +60 mV. So if $v_{in} = v_1(t)$ is sent in, it will have peak voltage of 0.16 V instead of 0.1 V. For $v_{in} = v_2(t)$, it will have peak voltage of 0.26 V. However, as both 0.16 V and 0.26 V will exceed the 0.15 V threshold, the circuit would not function properly.



Clarifying notes:



Assume the input connections of the comparator are reversed as shown above (i.e., the output of the super diode circuit v_b is applied to the inverting input of the comparator and the threshold or reference voltage is applied to the non-inverting input). As v_b will exhibit +40mV when there is no input, the peak detector output v_b with input will now be either 0.14 or 0.24 V. This will be applied directly to the inverting input of the comparator. On the other hand, due to the reversed connection, the input threshold of 0.15 V that is applied to the non-inverting terminal, will now experience an offset voltage of +20 mV. The actual threshold voltage that appears at the non-inverting terminal will now become 0.17 V. As 0.17 V is between 0.14 and 0.24 V, the comparator will still be able to detect the output correctly. However, the output will now be inverted, i.e., when it is 0.24 V, it will output low and when it is 0.14 V, it will output high.

because this is an inverting comparator

1a) $V_1(t) = 0{\cdot}01 \sin(2\pi \times \underline{10kHz} \times t)$

$$10kHz = GBW \times \frac{1}{1+10}$$

$11 \times 10kHz = GBW$

$GBW = 110kHz$

$\underline{\text{inverting amp}}$ of gain: -10

$\downarrow$

$\frac{-R_2}{R_1} = -10$, take $R_2 = 10$ and $R_1 = 1$

b) $V_2(t) = 0{\cdot}1 \sin(2\pi \times 500kHz \times t)$

$$500kHz = GBW \times \frac{1}{1+10}$$

$GBW = 11 \times 500kHz$

$= 5.5MHz$

$\underline{\text{inverting amp}}$ of gain: -10

$\downarrow$

$\frac{-R_2}{R_1} = -10$, take $R_2 = 10$ and $R_1 = 1$

c) Vout: $\underbrace{0{\cdot}1}_{\text{gain:10}} \sin(2\pi \times 10kHz \times t) + \underbrace{1}_{\text{gain:10}} \times \sin(2\pi \times 500kHz \times t)$

∴ input signal (a) to op-amp A with a gain (-10) (110kHz < opamp A GBW)
input signal (b) to op-amp B with a gain (-10) (5.5MHz < opamp B GBW)

$\downarrow$ output

output from (a) and (b) into summing amplifier (gain: -1) (combined < op-amp B GBW)

d) Vout: $\overbrace{\underbrace{1}_{\text{gain:100}} \sin(2\pi \times 10kHz \times t)}^{\text{input (a)}} + \overbrace{\underbrace{1}_{\text{gain:10}} \times \sin(2\pi \times 500kHz \times t)}^{\text{input (b)}}$

∴ input signal (a) to op-amp A with a gain (-10) (110kHz < opamp A GBW)
input signal (b) to op-amp B with a gain (-1) (5.5MHz < opamp A GBW)

$\downarrow$ output

output from (a) and (b) into summing amplifier (gain: -10) (combined < op-amp B GBW)

2a) Using KVL,

$V_x - I_x R - V_1 = 0$ $R_x = \frac{V_x}{I_x}$

$R = \frac{V_x - V_1}{I_x}$

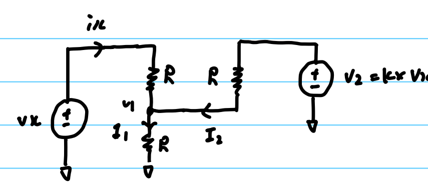
$= \frac{V_x - (0.99V_x)}{I_x}$

$= \frac{0.01V_x}{I_x}$

$R = 0.01 R_x$

$R_x = 100R$ //

b) Node V_1: KCL



$I_x + I_2 = I_1$

$\frac{V_x - V_1}{R} + \frac{V_2 - V_1}{R} = \frac{V_1}{R}$ $\times R$

$V_x - 0.99V_x + kV_x - 0.99V_x = 0.99V_x$

$kV_x = 0.99V_x + 0.99V_x - 0.01V_x$

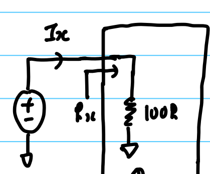
$kV_x = 1.97V_x$

$k = 1.97$ //

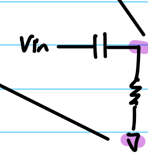
c) non-inverting op-amp with $\frac{R_2}{R_1}$ of 0.97

- positive input back to Vx

d) simple circuit, passive RC / CR
↓ ↓
low high



equivalent, hence only one node of the resistor can be used, other to ground



Hence, we use a simple high pass filter.

3a) A → Inverting amplifier

B → First-order low pass filter

C → Summing amplifier

b) <u>Inverting amplifier : $\left| \text{gain} : \left(-\frac{10}{1}\right) \right| = 10$</u>

Db scale: $20\log(10) = 20\,dB$

<u>First order low pass filter : $\left| \text{gain} : -\left(\frac{100R}{R}\right) \right| = 100$</u>

Db scale: $20\log(100) = 40\,db$

<u>Summing amplifier</u>

Gain: $10 + 100 = 110$

Db scale: $20\log(110) = 40.8\,dB$

- Cut-off frequency for low-pass filter is 1 kHz (decrease at $-20\,db$ / decade)

4a) Ideal op-amp, $i_- = i_+ = 0$, (assume no input current)

virtual short, $V_- = V_+ = V_x$

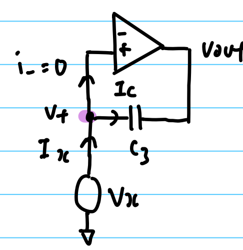
$$V_- = V_{out} \times \frac{R_1}{R_2 + R_1} = V_x$$

$$V_{out} = V_x \times \frac{R_2 + R_1}{R_1}$$

$$= V_x \times \left(\frac{R_2}{R_1} + 1\right)$$

Since we assume no input current

$i_+ = i_- = 0$,



By KVL,

$$I_x = I_c$$

$$I_x = \frac{V_+ - V_{out}}{\frac{1}{j\omega C_3}} \quad (\text{Since } V_+ = V_x)$$

$$I_x = \frac{V_x - \left(V_x \times \left(\frac{R_2}{R_1} + 1\right)\right)}{\frac{1}{j\omega C_3}}$$

$$= \frac{V_x - V_x\frac{R_2}{R_1} - V_x}{\frac{1}{j\omega C_3}}$$

$$= \frac{V_x\left(1 - \frac{R_2}{R_1} - 1\right)}{\frac{1}{j\omega C_3}}$$

$$I_x = -V_x \frac{\frac{R_2}{R_1}}{\frac{1}{j\omega C_3}} = -V_x \frac{R_2 j\omega C_3}{R_1}$$

$$Z_x = \frac{V_x}{I_x} = -\frac{R_1}{R_2 j\omega C_3} \qquad \omega = 2\pi f$$

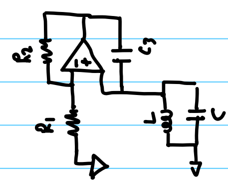
$\therefore$ Impedance of capacitor is: $\frac{1}{j\omega C}$

$$\frac{1}{j\omega C} = -\frac{R_1}{R_2 j\omega C_3}$$

$$\frac{1}{C} = \frac{-R_1}{R_2 C_3} \rightarrow C = -\frac{R_2 C_3}{R_1} \,// \quad (C \text{ has a negative impedance})$$

4b) LC resonant freq: $\frac{1}{2\pi\sqrt{LC}}$

Since in parallel, total capacitance is the sum of capacitance. Hence, we can add the LC network in parallel with the circuit in Fig 4a).



New resonant freq: $\frac{1}{2\pi\sqrt{LC(-\frac{R_2C_2}{r_1})}}$

∴ As R1 resistance varies, resonant frequency in the circuit will change.

5a) $f_{3db} = \frac{1}{2\pi R_1C_1}$

$= \frac{1}{2\pi(9k)(88.4p)}$

$\approx 200\,kHz$

gain: $-\frac{R_1}{R_2} \times \frac{1}{j\omega C_1R_1+1}$

$= \frac{-9k}{1k} \times \frac{1}{j\omega(88.4p)(9k)+1}$

$= -9 \times \frac{1}{j\omega \times 7.96\times10^{-7}+1}$

b) With capacitor 1 removed, taking into consideration of GBW effect,

$f_{3db,cL} = GBW \times \frac{1k}{1k+9k}$

$= 2M \times \frac{1}{10}$

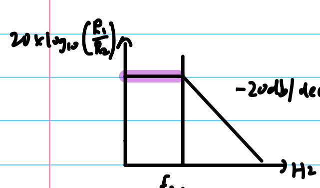
$= 200kHz$

c) Gain: $|20\log(9)| = 19.08db$

With 3db cutoff frequency, -3db, since GBW is same frequency, GBW effect, -3db

$19.08db - 3db_{cutoff} - 3db_{GBW} \approx 13.1dB$

d) Yes. Gain magnitude is constant $(\frac{R_1}{R_2})$ for frequencies smaller than the 3dB cut-off



pg 77 chap3

Low-pass filter

$\ll 200\text{kHz}$ (inverting amp)

e) If $v_1(t) = V_{pk} \sin(2\pi \times 10k \times t)$, find max V_{pk} such that V_{out} is w/o distortion

$V_{out(V_{in})} : -\frac{R_1}{R_2} \times V_{pk} \sin(2\pi \times 10kt)$ (inverting)

$V_{out(OS)} = V_{os} \times (1 + \frac{R_1}{R_2})$ (non-inverting)

Since op-amp powered by $\pm 5V$ supply

$$-5 < -\frac{R_1}{R_2} \times V_{pk} \sin(2\pi \times 10kt) + V_{os} \times (1 + \frac{R_1}{R_2}) < 5$$

$$-5 < -9V_{pk} + (20m)(1 + \tfrac{9}{1}) < 5$$

$$-5.2 < -9V_{pk} < 4.8$$

$$-0.53V < V_{pk} < 0.58V$$

Hence max allowable is $0.53V$.

f) 1) <u>Summing amplifier</u>

- Set R_3 to $9k\Omega$ so gain will be -1, input $0.2V$ to cancel out V_{os}

$$\therefore -\frac{R_1}{R_2} \times V_{pk} \sin(2\pi \times 10kt) + \underbrace{V_{os} \times (1 + \frac{R_1}{R_2}) - (\frac{R_1}{R_2}) \times 0.2V}_{\text{cancel out}}$$

2) <u>DC block capacitor</u>

- Since offset is in DC, and in DC, capacitor acts as open circuit, V_{os} will not be amplified 10 times

6 a) $f_{3db,CL} = GBW \times \frac{R_1}{R_1+R_2}$

$= GBW \times 1$ (since it is unity gain)

$= 0.5MHz$

b) Min peak voltage: $(1+\frac{R_2}{R_1}) \times \sqrt{V_n^2 \times 0.5MHz \times \frac{\pi}{2}}$

$= (1) \times \sqrt{(20n)^2 \times 0.5M \times \frac{\pi}{2}}$

$= 17.7\mu V$ → in rms

$V_p = 17.7\mu \times \sqrt{2}$

$= 25\mu V$

c) Max → slew rate / GBW

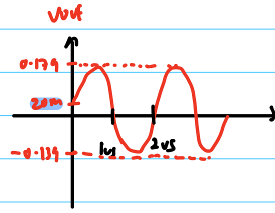
$2\pi f \times V_{out,pk} \sin(2\pi(0.5M)t) < 0.5V/\mu s$

$2\pi(0.5M) \times V_{out} < 0.5V/\mu s$

$2\pi(0.5M) \times V_{out} < 0.5\times10^6$

$V_{out} < 0.159V$

d)



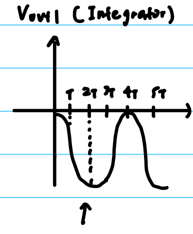
input offset = 20mV

period = $\frac{1}{f} = \frac{1}{0.5M}$

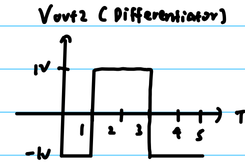
$= 2\mu s$

7) Vout1 → Integrator → area under curve
Vout2 → Differentiator → gradient of graph } both inverting

Vout1 (Integrator)



Vout2 (Differentiator)



When +ve gradient, -ve output,
when -ve gradient, +ve output

b) For V_{out2} to have $V_{pp} = 2V$, $V_p = 1V$

$V_p = -RC\frac{d(vi)}{dt} = 1V$

$= -R_2C_2\left(\frac{-2V}{2T}\right) = 1V \Rightarrow R_2C_2 = T$

6a) $v_1(t) = \cos(2\pi \times 100000 \times t)$

$$\frac{dv_1(t)}{dt} = -2\pi \times 100000 \times \sin(2\pi \times 100000 \times t)$$

b) $v_2(t) = \cos(2\pi \times 200000 \times t)$

$$\frac{dv_1(t)}{dt} = -2\pi \times 200000 \times \sin(2\pi \times 200000 \times t)$$

c) $$V_{out}(t) = -RC \frac{dV_{in}(t)}{dt}$$

$$0.1V = -RC\,(-2\pi \times 100000)$$

$$RC = \frac{0.1}{2\pi \times 100000}$$

$$= 1.59 \times 10^{-7}$$

$$R = \frac{1.59 \times 10^{-7}}{1 \times 10^{-9}}$$

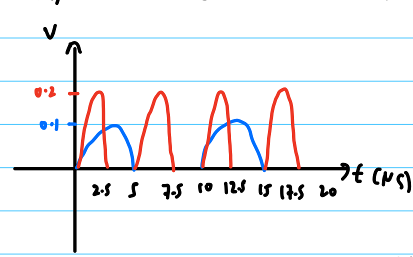
$$= 159\Omega$$

$\therefore$ Hence, we can choose a 1nF capacitor, and 159Ω resistor

check for $v_2(t)$

$$-(1nF)(159\Omega) \times -2\pi \times 200000 \approx 0.2V$$

d) Super diode acts as half-wave rectifier



$v_1(t)$

period $= \frac{1}{1M}$

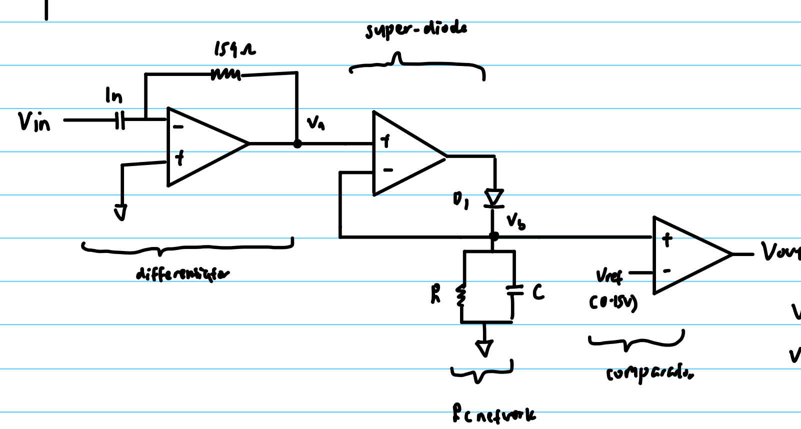
$= 10\mu s$

$v_2(t)$

period $= \frac{1}{2M}$

$= 5\mu s$

e)



Vref midpoint between V_1 and V_2

f) If all op-amps have offset voltage of 20mV, in the third op-amp, the non-inverting terminal will have a offset voltage total of 60mV. Hence, when added with the input signal, V_{in} (0·1, 0·2), the resulting input to the comparator will either be 0·16V or 0·26V. Since both these voltages are higher than the comparators threshold voltage (0·15V), the comparator will not work.