

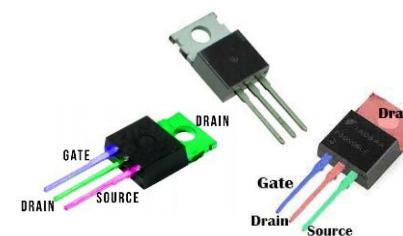
Metal Oxide Semiconductor Field Effect Transistor (**MOSFET**)

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

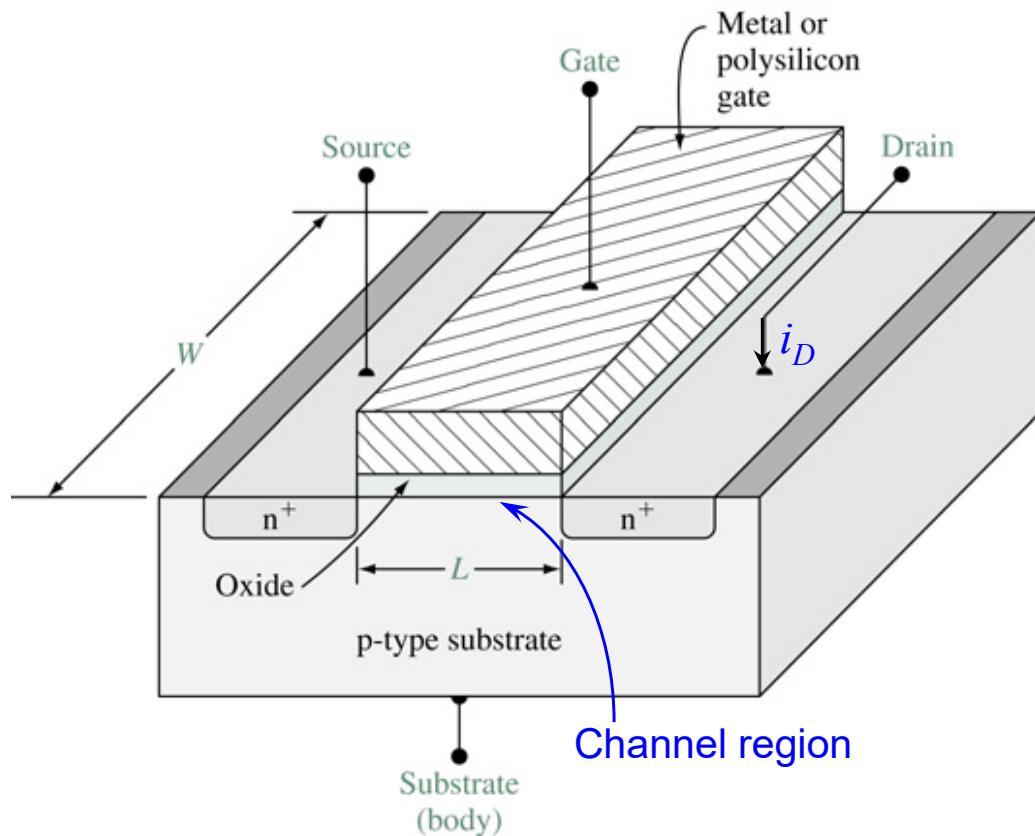
1. Introduction
2. Modes of operation: Linear, Saturation and Cut-off
3. i_D - v_{DS} Relationship of the MOSFET
4. Comparison between MOSFET and BJT
5. Large-Signal Models and dc Analysis
6. Small-Signal Model and ac Analysis
7. Channel Length Modulation
8. Body Effect and Capacitances
9. CMOS Inverter

References

- Sedra and Smith, Microelectronic Circuits, Theory and Applications, Fifth Edition (International Version), Oxford (2004), pp. 325 – 349, pp. 426-429, pp. 901-921.



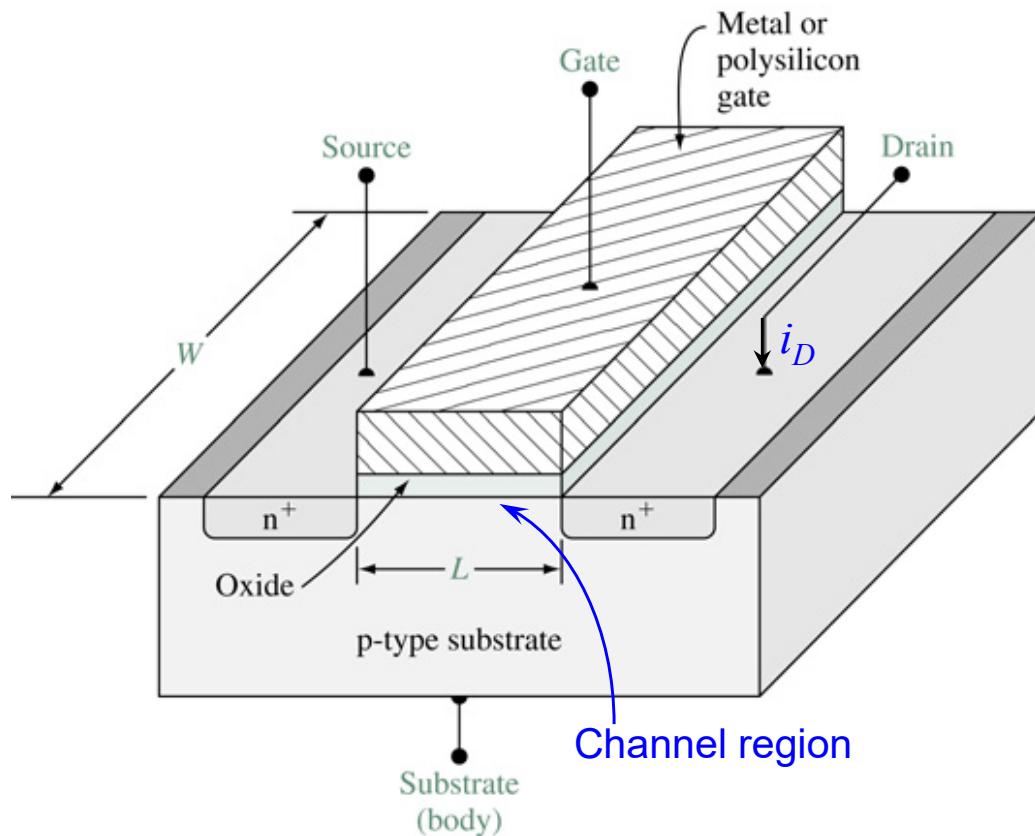
MOSFET – Introduction (Structure)



Basic structure of an n-channel MOSFET.

- Schematic on the left shows the basic structure of an *n*-channel MOSFET, also called an NMOS transistor.
- MOSFET is a transistor, performing the **same** functions as BJT: switching and amplification.
- An n-channel MOSFET is made using a *p*-type single-crystal silicon substrate.
- Heavily doped *n*⁺-type regions, created in the substrate, form the **source** and **drain** regions.
- The metal electrode on top of the thin oxide (dielectric) layer, between the **source** and **drain** regions, is called the **gate**.

MOSFET – Introduction (Carrier Flow & Current)



Basic structure of an n-channel MOSFET.
(Comparison with BJT in [Appendix A](#))

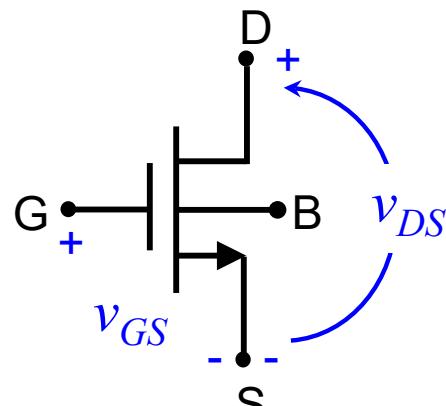
- Source, drain and gate of a MOSFET correspond to the emitter, collector and base of a BJT, respectively.
- Source terminal is the source of the carriers that will flow through the channel to the drain terminal.
- In an *n*-channel MOSFET, electrons (negatively charged carriers) flow from the source to the drain.
- Conventional current (i_D) therefore enters the drain terminal and flows to the source terminal.
- Note that MOSFET has a fourth terminal - the **substrate** or **body**. It is typically shorted to the source, making MOSFET effectively a 3-terminal device.

MOSFET – Introduction (n-MOSFET vs p-MOSFET)

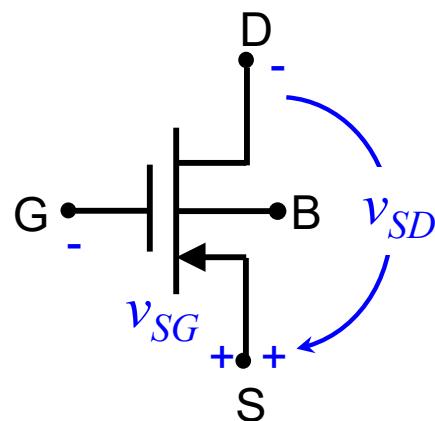
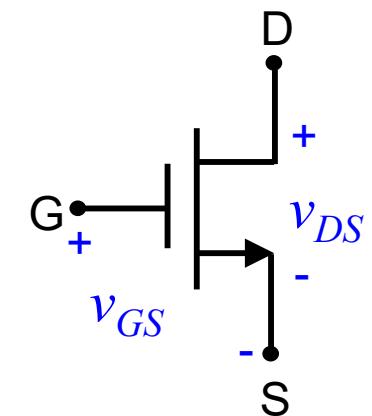
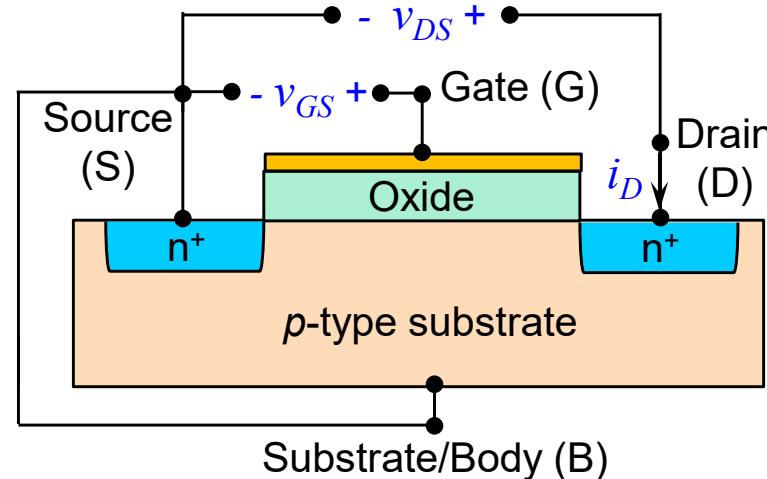
Circuit symbol of MOSFET

Schematic cross-section of MOSFET and operating biases.

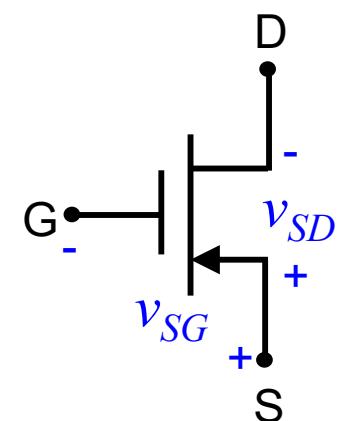
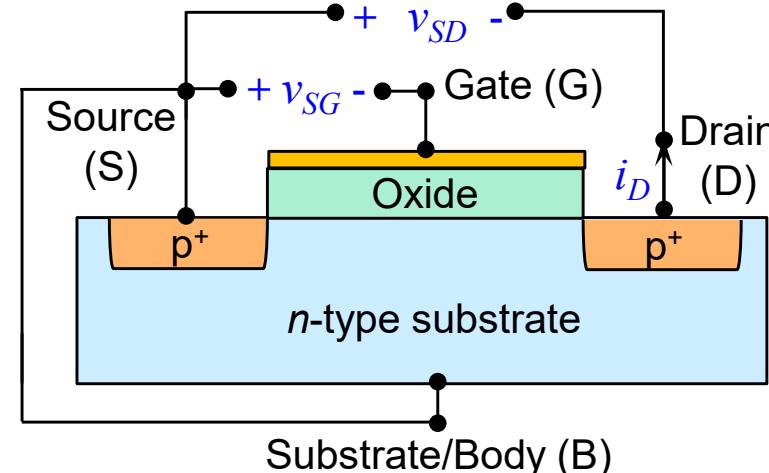
Simplified circuit symbol of MOSFET when body is shorted to source



n-channel MOSFET



p-channel MOSFET



MOSFET – Introduction (n-MOSFET Vs p-MOSFET)

- There are two types of MOSFET: n-channel and p-channel MOSFETs (see their structures and circuit models in previous slide, MOSFET-4)
- A p-channel MOSFET, also called a PMOS transistor, is made using an n-type single-crystal silicon substrate, and heavily doped p⁺-regions form the source and drain regions. Note the differences from n-channel MOSFET.
- The n-channel and p-channel MOSFETs are functionally the same. Their difference lies in the **biasing polarities** of drain-to-source voltage, v_{DS} , and gate-to-source voltage, v_{GS} ; and the **direction** of drain current, i_D . They are **opposite** between n-channel and p-channel MOSFETs for the same mode of operation.
- The arrow head in the circuit symbols, which identify the source terminal, indicate the direction of current flow in the MOSFET.
- Our discussion will focus on *n*-channel MOSFET, which applies to *p*-channel MOSFET except for the differences highlighted above: current direction and biasing voltage polarity .

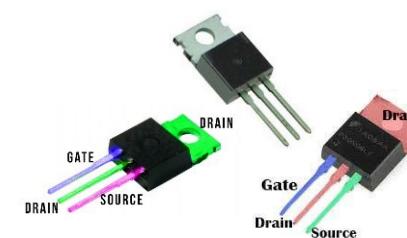
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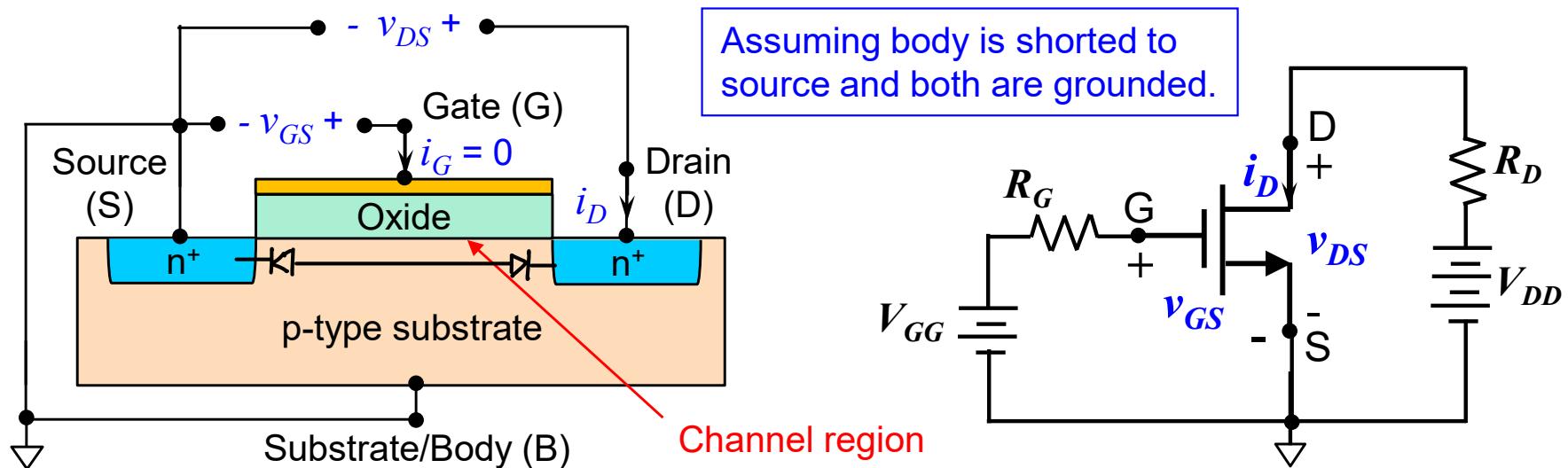
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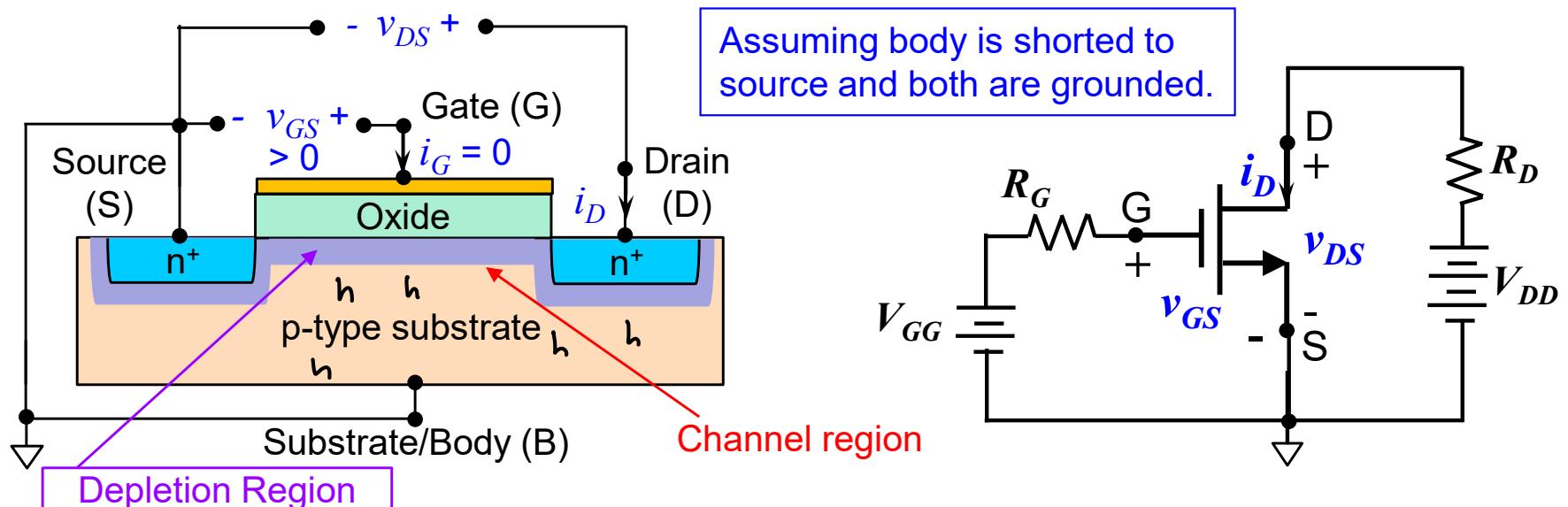


MOSFET – Modes of Operation (n-channel MOSFET)



- The main current flow in a MOSFET is between the source and drain, and it is called the drain current, i_D .
- No current flows through the gate, $i_G = 0$, as it is electrically isolated from the semiconductor substrate by the oxide.
- Two back-to-back *pn*-junctions exist in series between source and drain. One is between the n⁺-drain region and the p-type substrate, and the other is between the n⁺-source region and the p-type substrate.
- With no v_{GS} applied, the two back-to-back *pn*-junctions prevent current flow between the source and drain ($i_D = 0$) when a voltage $v_{DS} > 0$ is applied.

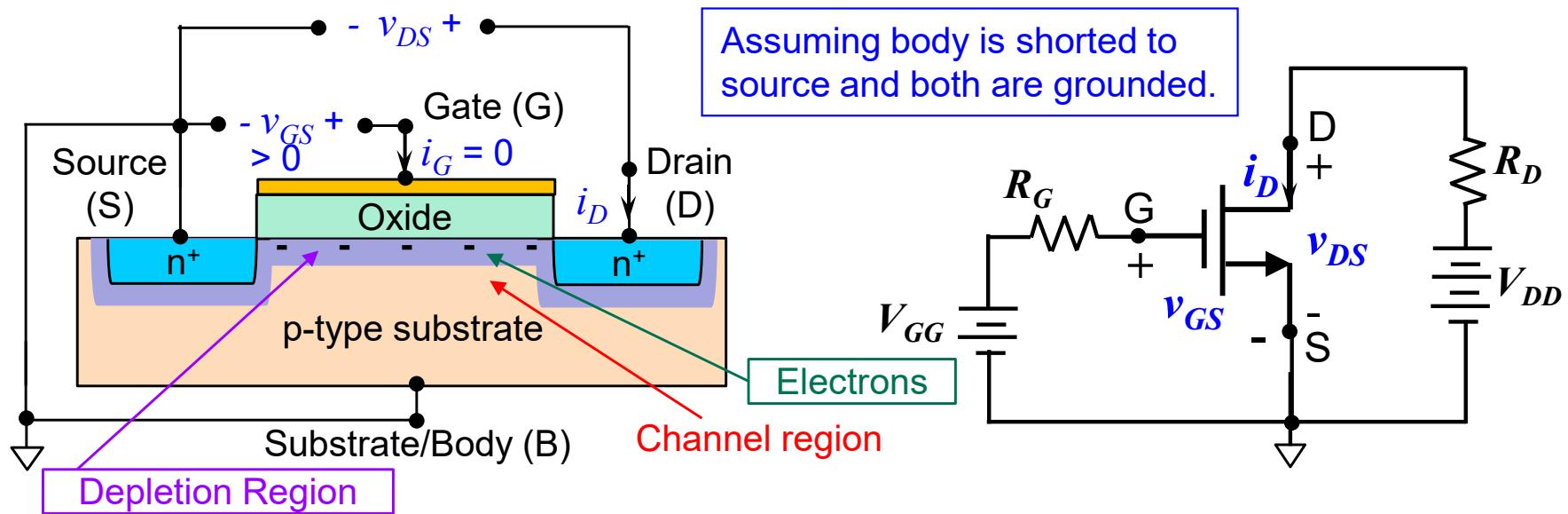
MOSFET – Modes of Operation (n-channel MOSFET)



What happens when $v_{GS} > 0$ is applied?

- Take note that in a p-type semiconductor, there are many holes (positively charged carriers) and they are mainly contributed by p-type impurities that have become ionized. The ionized p-type impurities are fixed negative charges that neutralize the positive charges of holes, thus making the p-type semiconductor overall electrically neutral (see Appendix B).
- With $v_{GS} > 0$ applied, positive voltage at the gate repels holes in the p-type substrate from the region below the gate (the channel region), leaving behind fixed ionised p-type impurities near the surface of the substrate. This produces a region depleted of holes, known as the depletion region (see Appendix C).

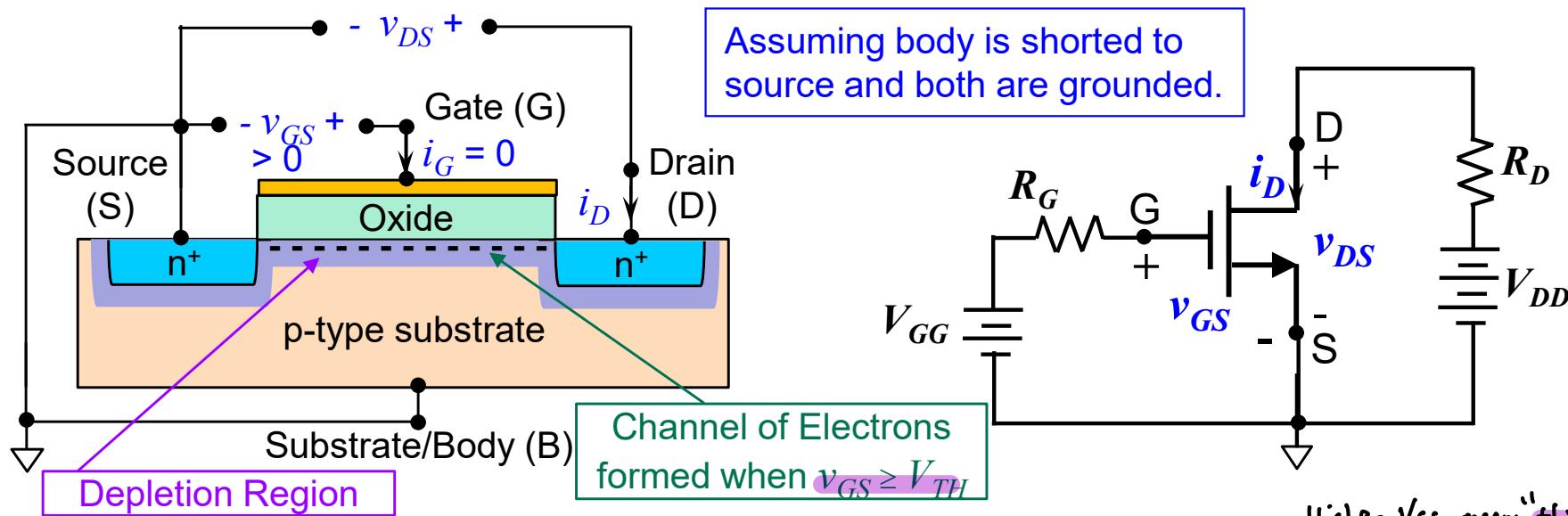
MOSFET – Modes of Operation



What happens when $v_{GS} > 0$ is applied?

- The depletion region have only fixed ionised p-type impurities, and it prevents current flow between the source and drain, $i_D = 0$., even with $v_{GS} > 0$.
- At the same time, with $v_{GS} > 0$ applied, electrons will be attracted from the n⁺-source and n⁺-drain into the p-doped channel region.
- With increasing $v_{GS} > 0$, more electrons will be attracted into the channel region, and pile up near the surface of the substrate under the gate.

MOSFET – Modes of Operation

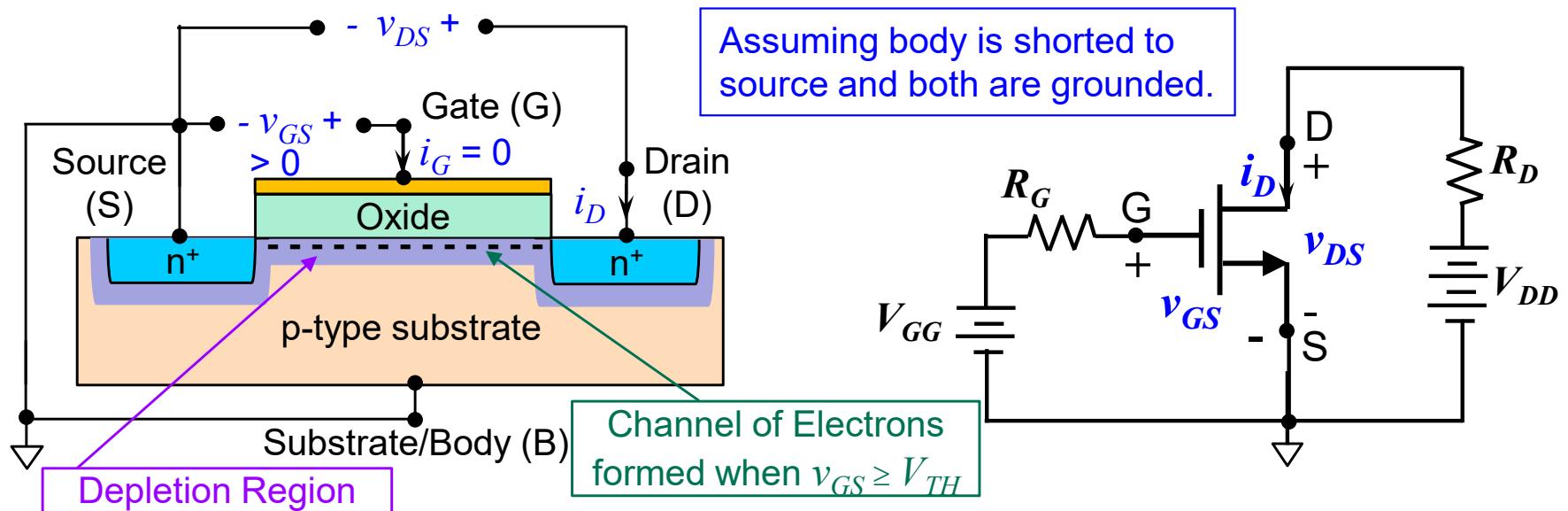


What happens when $v_{GS} > 0$ is applied?

- With high enough v_{GS} , sufficient electrons can be attracted into the channel region and pile up near the surface of p-substrate under the gate to make the surface effectively n-type, connecting the n⁺-source and n⁺-drain regions.
 - The surface of p-substrate is said to be **inverted** (or a **channel** is formed), a current i_D can flow between the source and drain when $v_{DS} > 0$ is applied.
- The v_{GS} at which the surface of the p-type substrate becomes inverted is known as the **threshold voltage**, V_{TH} (a parameter of MOSFET with the dimension of voltage). For n-channel MOSFET, $V_{TH} > 0$.

Higher v_{GS} , means "thicker" channel formed, controls current selection flow from S to D ↘

MOSFET – Modes of Operation

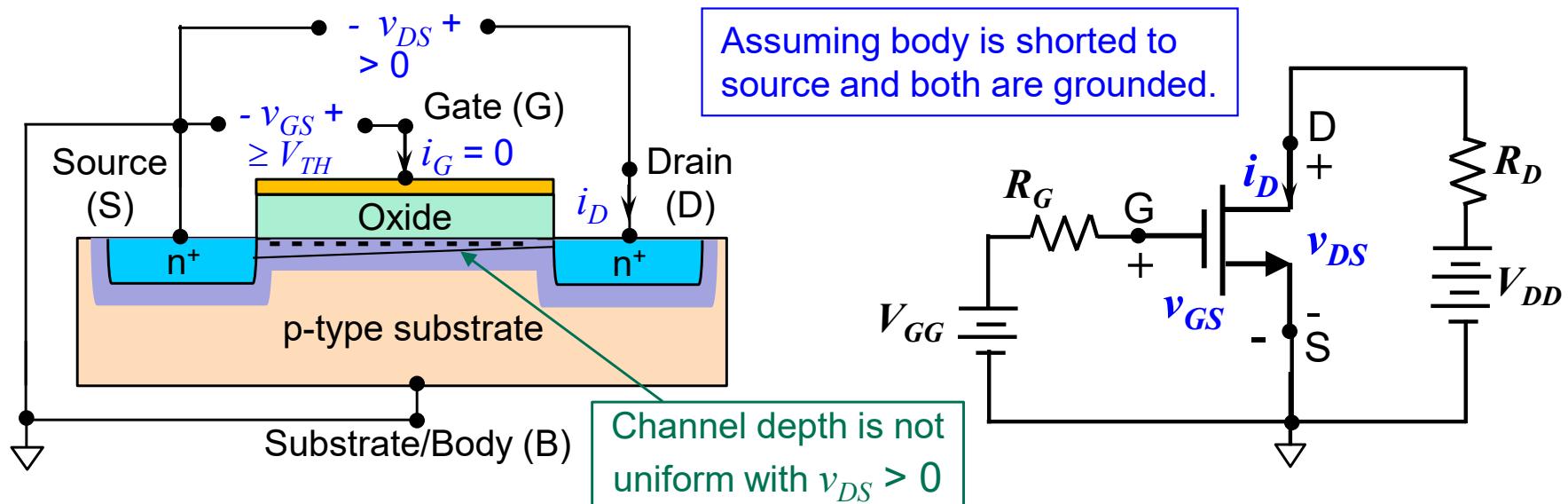


Summary - What happens when $v_{GS} > 0$ is applied ?

- With $v_{GS} < V_{TH}$, effectively no channel is formed between the source and drain, hence no current flows between them, and $i_D \approx 0$, even with $v_{DS} > 0$. MOSFET is said to operate in the **cut-off region**.
- With $v_{GS} \geq V_{TH}$, a channel is formed and i_D can flow between the source and drain when $v_{DS} > 0$ is applied. → like “incentive” for current I_D flow
Does i_D increases always with increasing v_{DS} ?

Note: n-channel MOSFET (or NMOS transistor) is so called as the channel that connects the n⁺-source and n⁺-drain regions is made up of negatively charged electrons.

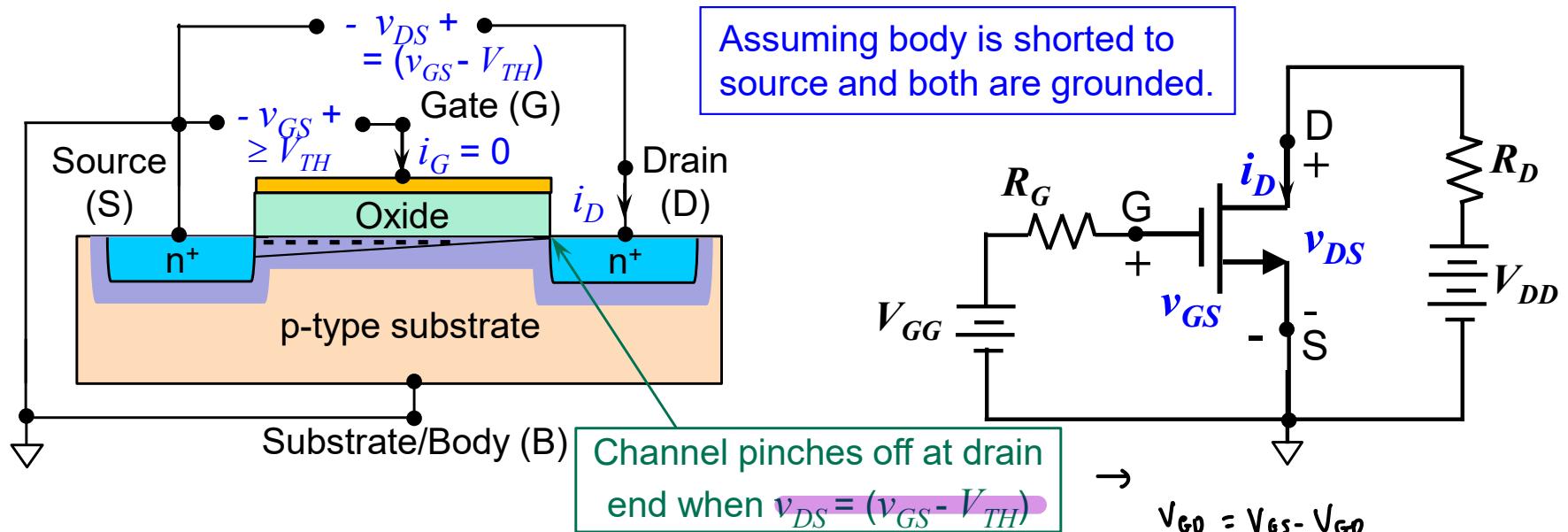
MOSFET – Modes of Operation



With $v_{GS} \geq V_{TH}$, what happens when $v_{DS} > 0$ is applied?

- With v_{GS} increasing beyond V_{TH} , more electrons will be induced in the channel. The channel conductivity increases and so does i_D for a given v_{DS} .
- With a specific $v_{GS} \geq V_{TH}$, for small $v_{DS} > 0$, i_D increases with increasing v_{DS} . The MOSFET is said to operate in the linear region.
- Take note that the channel depth at the drain end is ‘narrower’ (with fewer electrons) than the source end because the voltage between the gate and the drain ($v_{GS} - v_{DS}$) is less than that between the gate and the source (v_{GS}).

MOSFET – Modes of Operation

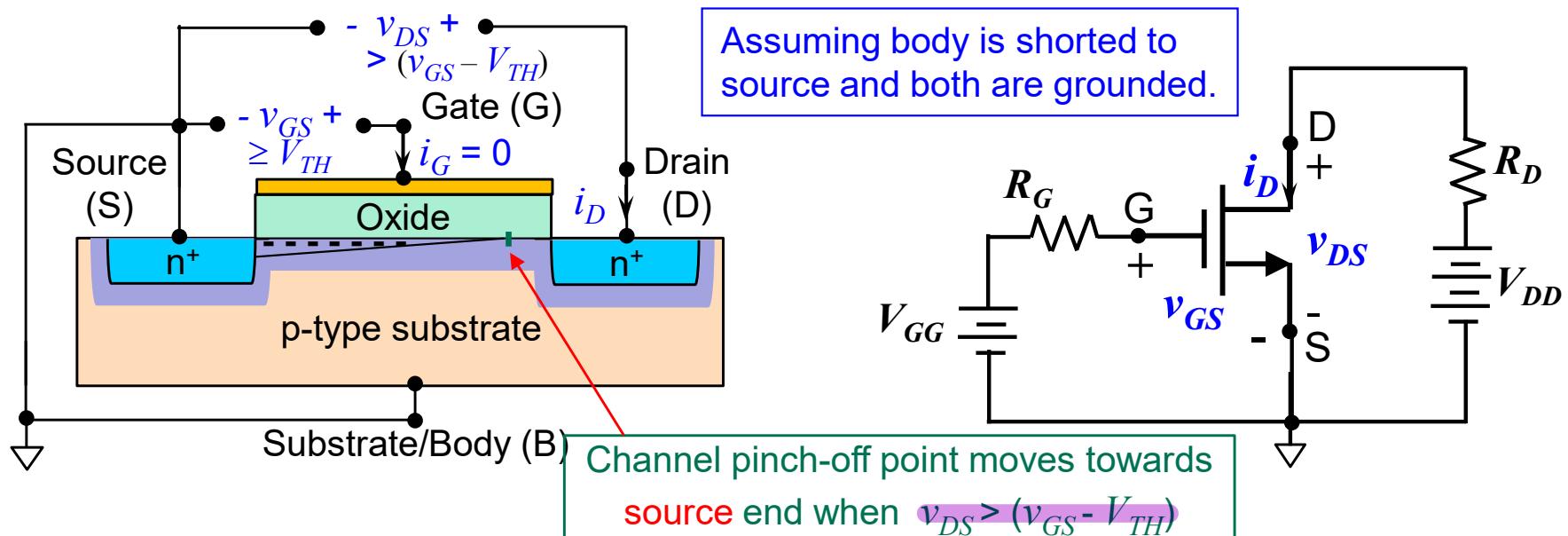


With $v_{GS} \geq V_{TH}$, what happens when $v_{DS} > 0$ is applied?

- When $v_{DS} = (v_{GS} - V_{TH})$, the voltage between the gate and the drain end of the channel = $v_{GS} - v_{DS} = v_{GS} - (v_{GS} - V_{TH}) = V_{TH}$.
- Recall that a channel forms under the gate only when $v_{GS} > V_{TH}$.
- Therefore, when $v_{DS} = (v_{GS} - V_{TH})$, the channel depth at the drain end has reduced to zero. The channel is said to be pinched off at the drain end.

$$\begin{aligned} V_{GD} &= V_{GS} - V_{GP} \\ &= V_{GS} - (V_{GS} - V_{TH}) \\ &= V_{TH} \end{aligned}$$

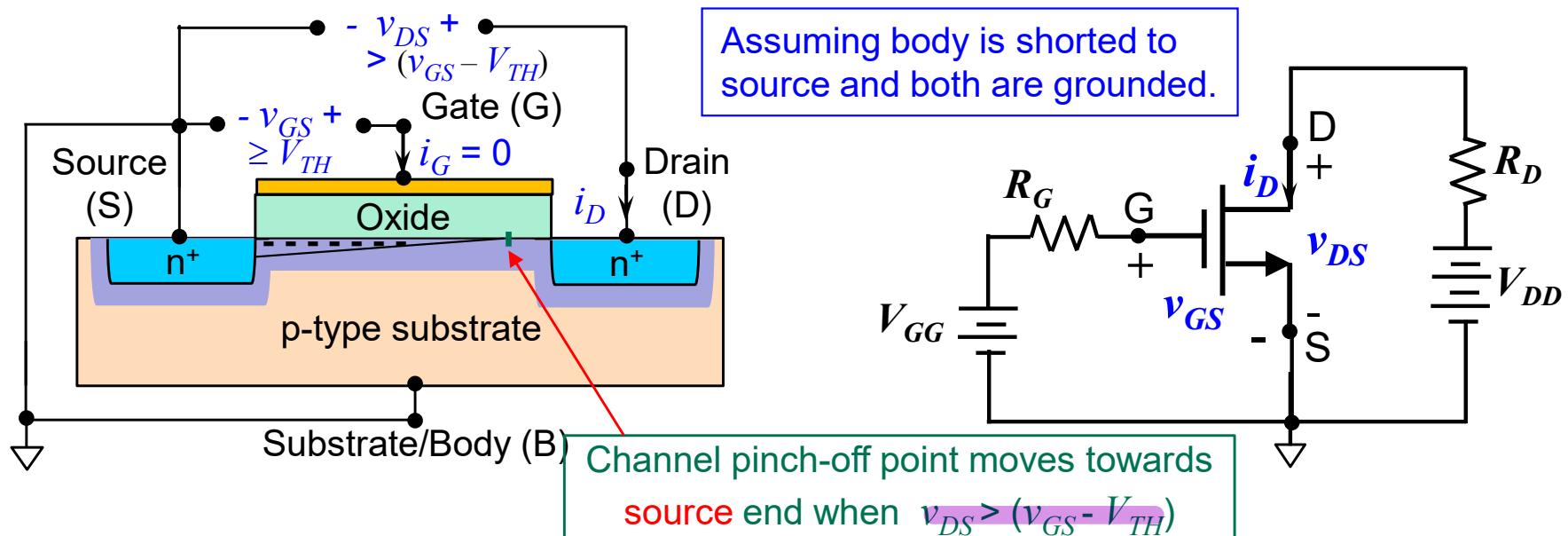
MOSFET – Modes of Operation



With $v_{GS} \geq V_{TH}$, what happens when $v_{DS} > 0$ is applied?

- When $v_{DS} > (v_{GS} - V_{TH})$, the pinch-off point of channel moves towards the source terminal. A high electric field exists in the depletion region near the drain end of the device (between pinch-off point and drain)
 - Electrons drift from the source, through the channel to the pinch-off point, where they are swept by the electric field near the drain into the drain terminal.
- Assume the MOSFET has a long channel. This means the shortening of channel as the pinch-off point moves towards source is insignificant compared to the length of channel (see Appendix D).

MOSFET – Modes of Operation



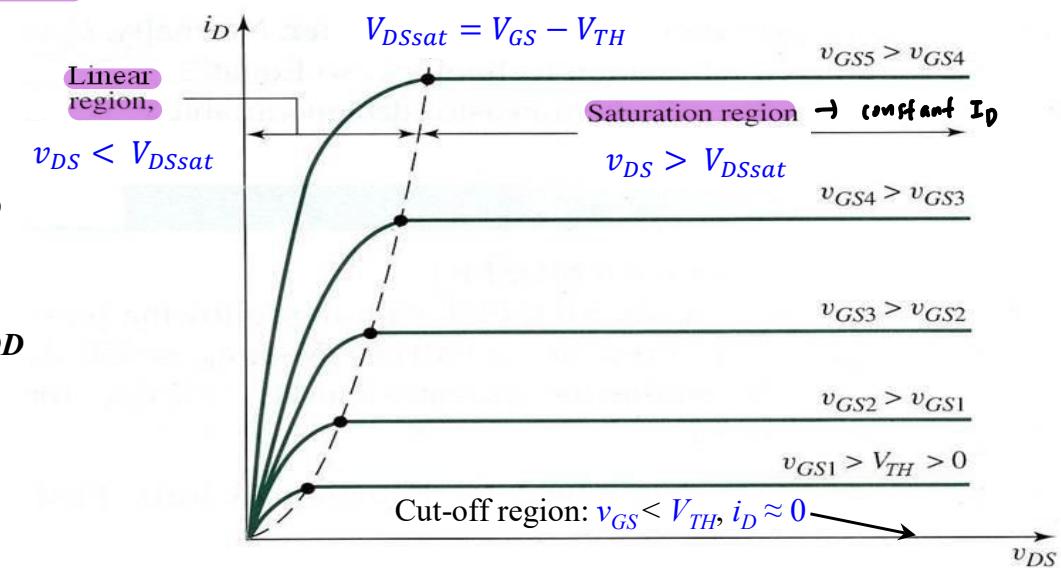
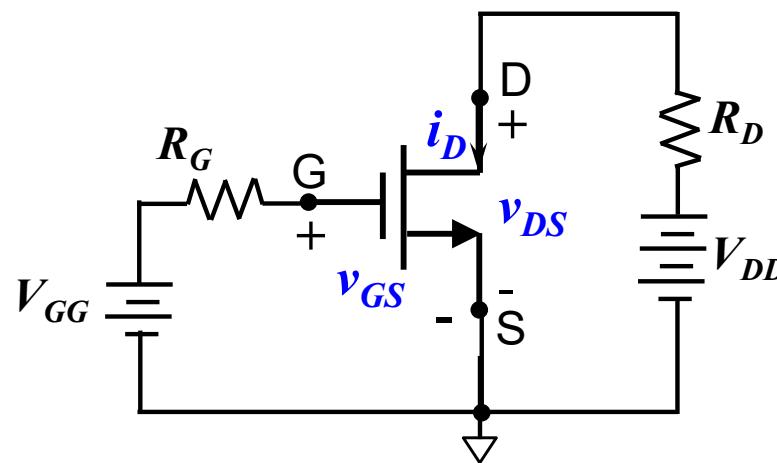
With $v_{GS} \geq V_{TH}$, what happens when $v_{DS} > 0$ is applied?

- The channel length and channel charge density, for a given v_{GS} , is therefore not changed significantly for $v_{DS} > (v_{GS} - V_{TH})$. The drain current i_D (due to the drift of electrons through the channel) is then approximately constant.
- The drain current i_D is then said to be saturated, and the MOSFET is said to operate in the saturation region.
- The drain voltage at which current saturation occurs is called the saturation drain voltage, $V_{DSsat} = (V_{GS} - V_{TH})$. Note that V_{DSsat} is a dc voltage.

MOSFET - Modes of Operation

- The relationships between the drain current, i_D , and the drain-to-source voltage, v_{DS} , for different gate-to-source voltages, v_{GS} , of an n-channel MOSFET are shown in the plot below.
- The regions corresponding to the **cut-off**, **linear** and **saturation** modes of operation are as indicated in the plot below.
 - Linear region - i_D depends on both v_{DS} and v_{GS} , i.e., $i_D = f(v_{DS}, v_{GS})$
 - Saturation region - i_D is independent on v_{DS} and is a function of only v_{GS} , i.e., $i_D = f(v_{GS})$
 - For any v_{GS} , the linear and saturation regions are separated by

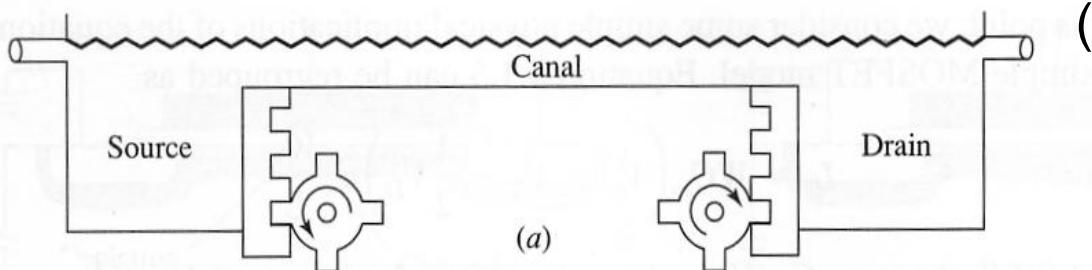
$$v_{DS} = V_{DSSat} = V_{GS} - V_{TH}.$$



Note : Do not confuse the saturation region of operation of the MOSFET with that of the BJT. See [Appendix E](#).

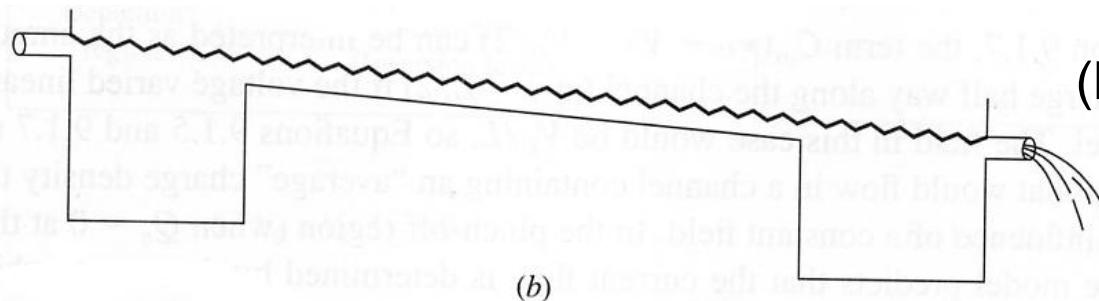
MOSFET - Modes of Operation

The operation of MOSFET and the phenomenon of saturation of the drain current can be likened, albeit imperfectly, to a water analogy, as shown below.



- (a) The water depth in the canal (channel) can be varied by the gear and track (v_{GS}). When the source and drain are level ($v_{DS} = 0$) there is **no flow**, despite the presence of a water channel ($v_{GS} > V_{TH}$).

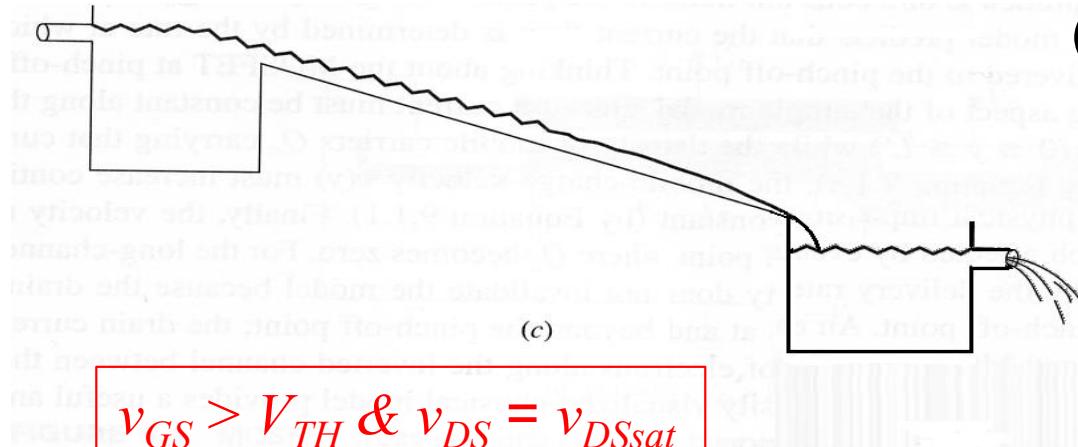
$$v_{GS} > V_{TH} \text{ & } v_{DS} = 0$$



- (b) When the drain is lower than the source ($v_{DSsat} > v_{DS} > 0$), and a water channel exists between them due to the “bias” by the gear and track ($v_{GS} > V_{TH}$), water flows along the channel. This **corresponds to the linear region** of operation of the MOSFET.

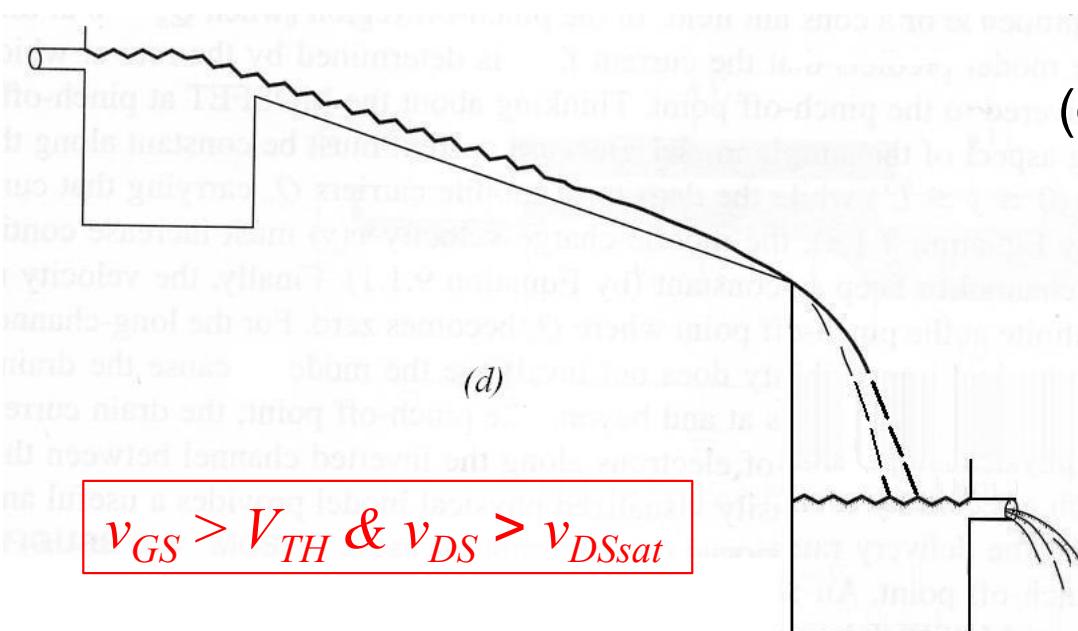
$$v_{GS} > V_{TH} \text{ & } v_{DSsat} > v_{DS} > 0$$

MOSFET - Modes of Operation



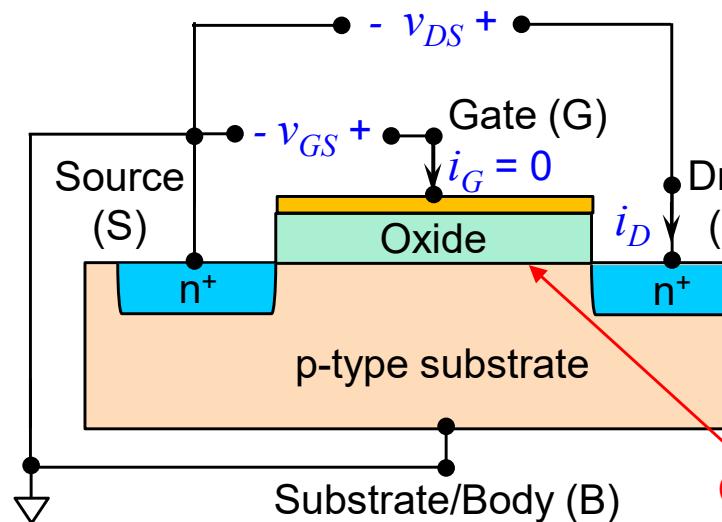
(c) The water flow is limited by the channel capacity. When the drain end of canal has been lowered to its lowest point, the limit is reached, and the rate of flow cannot be increased further. This corresponds to $v_{DS} = v_{DSSat}$.

$$\downarrow \\ v_{GS} - V_{TH}$$

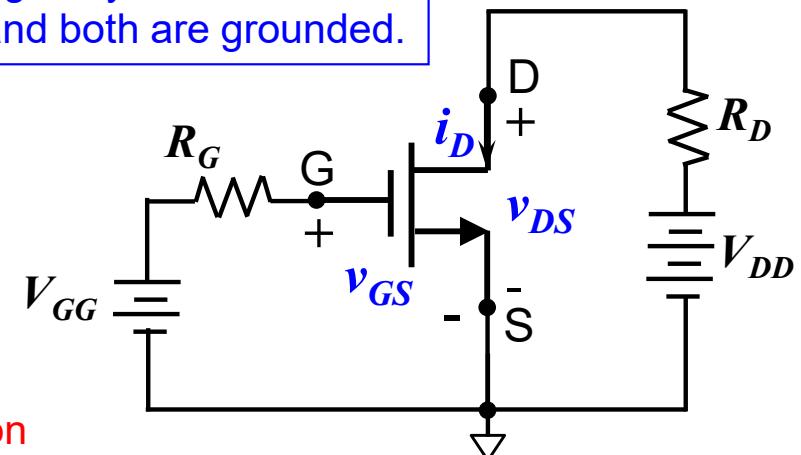


(d) Lowering the drain further (increasing v_{DS} beyond v_{DSSat}) only increases the height of the waterfall at its edge, but does not increase the rate of flow of water in the channel. This corresponds to the saturation region of operation of the MOSFET.

MOSFET - Modes of Operation



Assuming body is shorted to source and both are grounded.



Modes of operation of the n-channel MOSFET

Mode of Operation	Gate-to-Source Bias ($v_{GS} > 0$)	Drain-to-Source Bias ($v_{DS} > 0$)	Drain Current (i_D - into Drain)	Applications
Cut-off	$v_{GS} < V_{TH}$	N.A.	$i_D = 0$	CMOS Logic – OFF state
Linear	$v_{GS} \geq V_{TH}$	$v_{DS} \leq v_{GS} - V_{TH}$	$i_D = f(v_{DS}, v_{GS})$	CMOS Logic – ON state
Saturation	$v_{GS} \geq V_{TH}$	$v_{DS} \geq \underbrace{v_{GS} - V_{TH}}_{V_{DS,sat}}$	$i_D = f(v_{GS})$	Amplifier

* A similar table for p-channel MOSFET is shown in the [Appendix F](#).

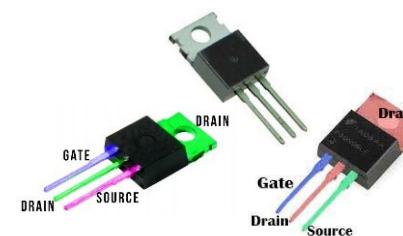
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MOSFET - i_D - v_{DS} Relationship

Consider an n-channel MOSFET and for $v_{GS} \geq V_{TH}$ -

- In linear region, $v_{DS} \leq v_{DSSat} = v_{GS} - V_{TH}$ and $i_D = f(v_{DS}, v_{GS})$ -

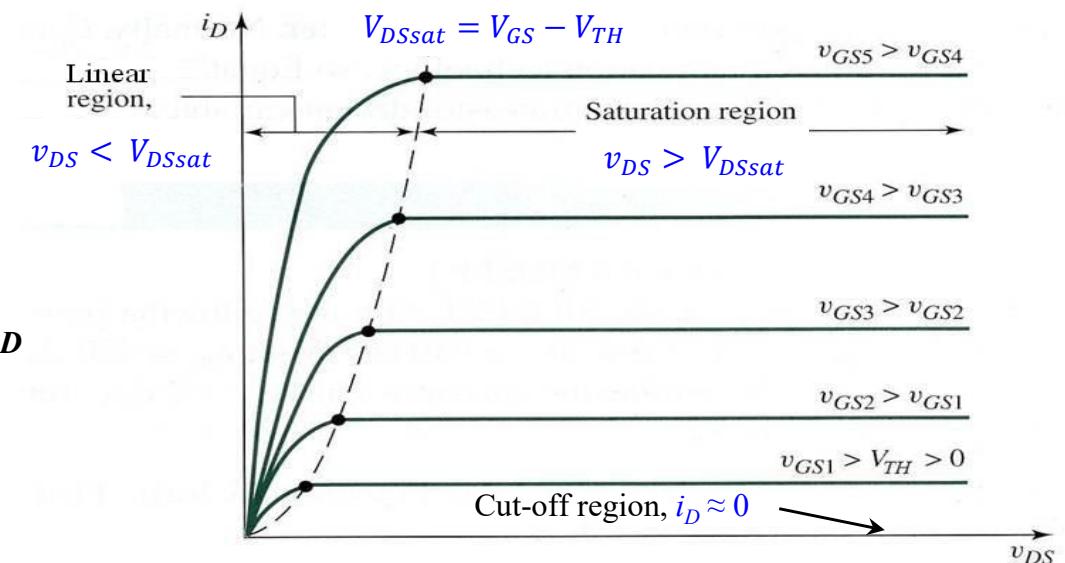
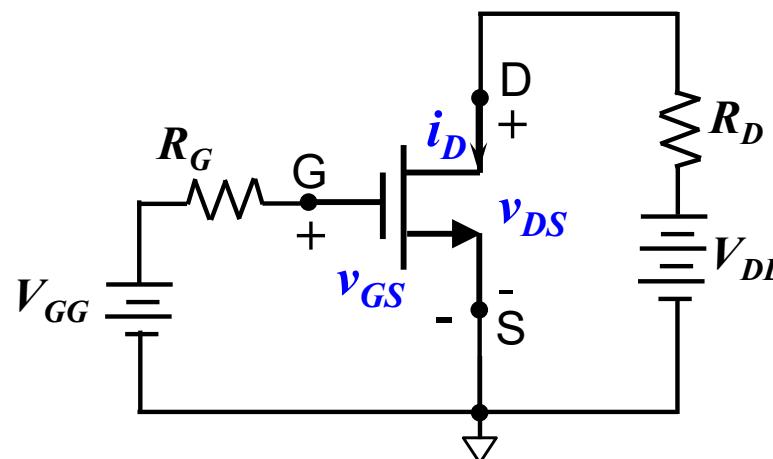
$$i_D = \mu_n \frac{W}{L} C_{ox} \left[(v_{GS} - V_{TH}) v_{DS} - \frac{1}{2} v_{DS}^2 \right] *, \quad (4.1)$$

- In saturation region, $v_{DS} \geq v_{DSSat} = v_{GS} - V_{TH}$ and $i_D = f(v_{GS})$ -

$$i_D = i_{Dsat} = \frac{1}{2} \mu_n \frac{W}{L} C_{ox} (v_{GS} - V_{TH})^2 \quad (4.2)$$

- For any v_{GS} , the linear and saturation regions are separated by -

$$v_{DSSat} = v_{GS} - V_{TH} \quad (4.3)$$



* Equation (4.1) is not valid for $v_{DS} > v_{DSSat} = v_{GS} - V_{TH}$

When solving, if unsure,
assume one of the conditions
and solve, if result no make
sense, then use other formula.
(4.1)

MOSFET - i_D - v_{DS} Relationship

- μ_n is the mobility of the electrons in the channel between the source and drain, W is the width of the channel, L is the length of the channel and C_{ox} is the gate oxide **capacitance** per unit area –

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_{r,ox}\varepsilon_0}{t_{ox}}, \quad (4.4)$$

where t_{ox} is the thickness of the oxide, ε_{ox} is the permittivity of the oxide, $\varepsilon_{r,ox}$ is the dielectric constant (or relative permittivity) of oxide and is equal to 3.9 for silicon dioxide, and $\varepsilon_0 = 8.854 \times 10^{-14} \text{ F cm}^{-1}$ is the permittivity of free space.

- Defining the conductance parameter, K_n , as

$$K_n = \frac{1}{2} \mu_n \frac{W}{L} C_{ox} \quad (4.6)$$

- Equations (4.1) and (4.2) can be re-written respectively as

$$i_D = 2K_n \left[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2} v_{DS}^2 \right], \quad \left. \right\} N_{mos} \quad (4.7)$$

and $i_D = i_{Dsat} = K_n (v_{GS} - V_{TH})^2 \quad (4.8)$

$$\left. \begin{aligned} i_D &= 2k_p [(v_{SG} + v_{TH}) v_{SD} - \frac{1}{2} v_{SD}^2] \\ i_D &= i_{Dsat} = k_p (v_{SG} + v_{TH})^2 \end{aligned} \right\} P_{mos}$$

MOSFET - i_D - v_{DS} Relationship (p-MOSFET)

- For a p-channel MOSFET, v_{DS} , v_{GS} and V_{TH} are all negative.
- For $v_{SG} = |v_{GS}| \geq |V_{TH}|$, positively charged holes form the channel, allowing holes to flow from the source to the drain, and the drain current, i_D , flows out of the drain terminal (see Appendix G).
- To maintain the same notation and sign as an n-channel MOSFET, we shall express the $i_D - v_{DS}$ equations for the p-channel MOSFET in terms of absolute values -

- In linear region, $|v_{DS}| \leq |v_{GS}| - |V_{TH}|$ -

$$|i_D| = 2K_p \left[(|v_{GS}| - |V_{TH}|) |v_{DS}| - \frac{1}{2} |v_{DS}|^2 \right], \quad (4.9)$$

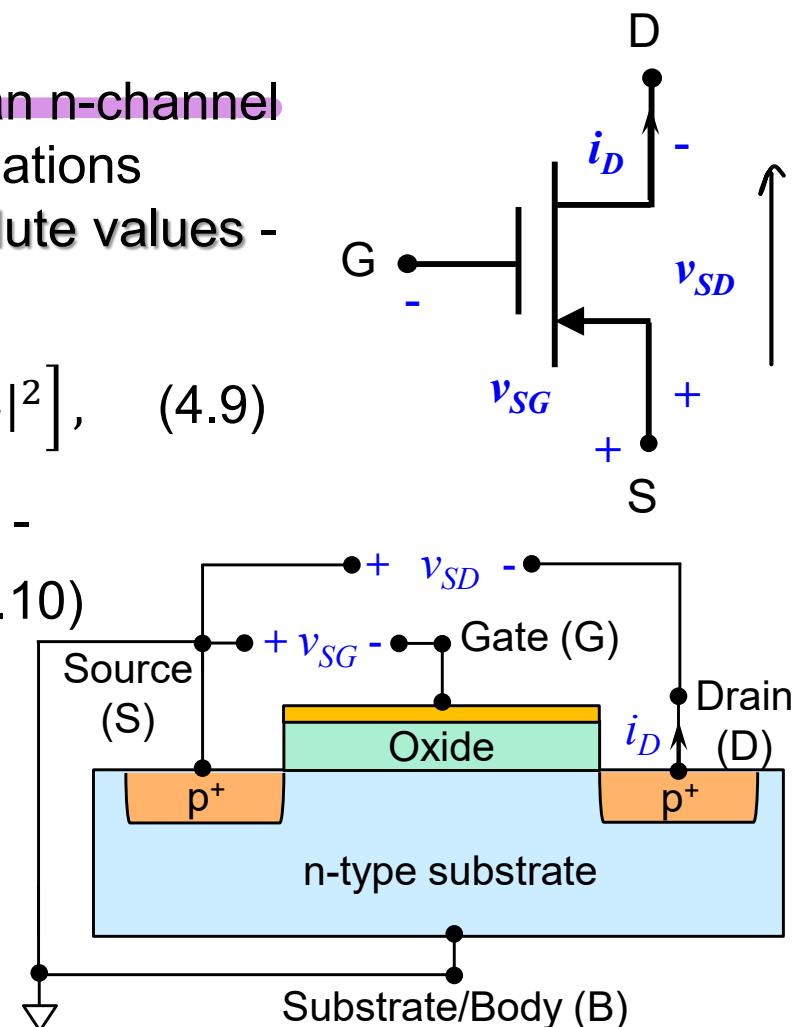
- In saturation region, $|v_{DS}| \geq |v_{GS}| - |V_{TH}|$ -

$$|i_D| = K_p (|v_{GS}| - |V_{TH}|)^2 \quad (4.10)$$

- Conductance parameter:

$$K_p = \frac{1}{2} \mu_p \frac{W}{L} C_{ox} \quad (4.11)$$

- μ_p is the mobility of the holes in the channel between the source and drain.



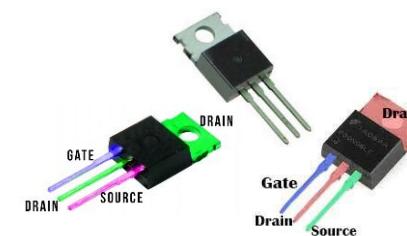
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MOSFET - Comparison between MOSFET and BJT

A MOSFET is a **four** terminal device while a BJT is a **three** terminal device. Both of them can be used as logic switches or as amplifiers. The comparison table below sets out some of the differences.

Feature	Bipolar Junction Transistor	MOSFET
Terminals	Emitter Base Collector	Source Gate Drain Substrate/ Body
Mode of operation in amplifiers	<u>Forward active</u>	<u>Saturation</u>
Modes of operation in logic switches	Cut-off for logic 'OFF' Saturation for logic 'ON'	Cut-off for logic 'OFF' Linear for logic 'ON'
Main Applications	High frequency, high speed, high power circuits	Logic, memory, mixed signal circuits, low power and VLSI circuits

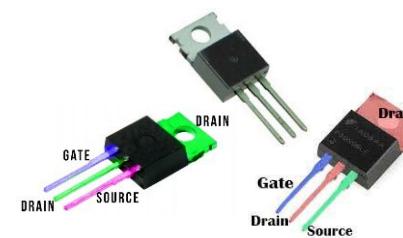
Metal Oxide Semiconductor Field Effect Transistor (**MOSFET**)

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

1. Introduction
2. Modes of operation: Linear, Saturation and Cut-off
3. i_D - v_{DS} Relationship of the MOSFET
4. Comparison between MOSFET and BJT
5. Large-Signal Models and dc Analysis
6. Small-Signal Model and ac Analysis
7. Channel-Length Modulation
8. Body Effect and Capacitances
9. CMOS Inverter

References

- Sedra and Smith, Microelectronic Circuits, Theory and Applications, Fifth Edition (International Version), Oxford (2004), pp. 325 – 349, pp. 426-429, pp. 901-921.



MOSFET – Large-Signal Model (Saturation Region)

- For an n-channel MOSFET in the saturation region –

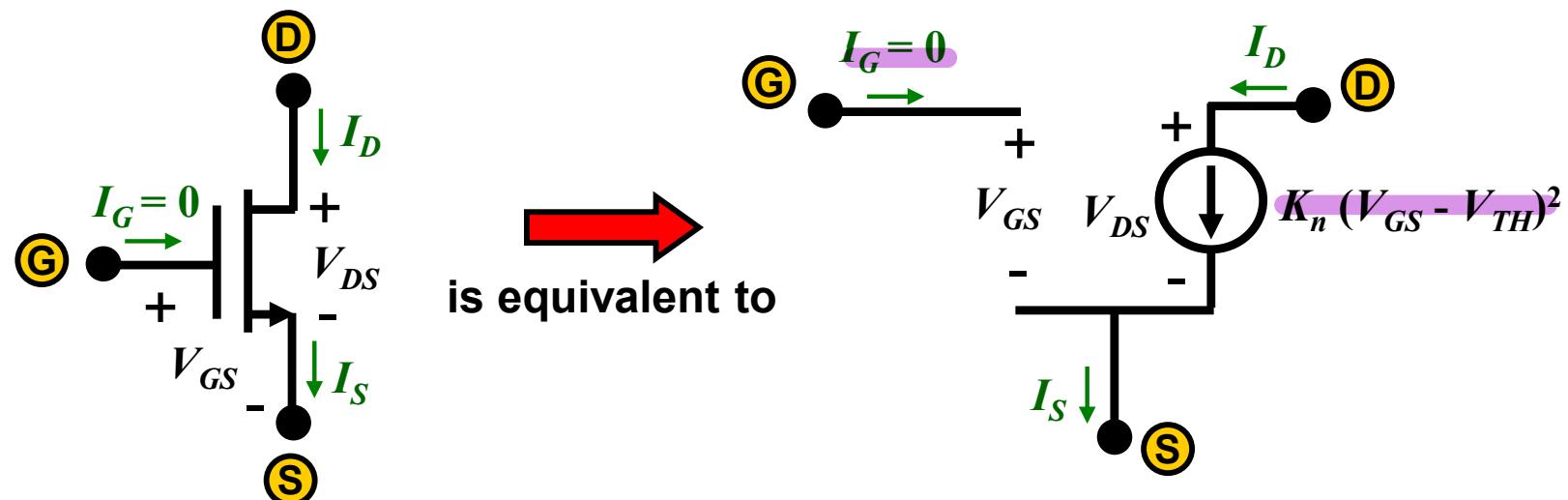
$$v_{GS} > V_{TH} \quad \text{and} \quad v_{DS} \geq v_{DSSat} = v_{GS} - V_{TH} \quad *$$

- From equation (4.8), we have, under dc condition -

$$I_D = I_{Dsat} = K_n(V_{GS} - V_{TH})^2 \quad \rightarrow \quad \text{a dependent current source}$$

- As there is no gate current –

$$I_G = 0 \quad \rightarrow \quad \text{an open circuit}$$



* $(v_{GS} - V_{TH})$ is also known as the Gate-Overdrive, and it is also the minimum v_{DS} to keep the MOSFET in the saturation region.

MOSFET – Large-Signal Model (Linear Region)

- For an n-channel MOSFET in the linear region –

$$v_{GS} > V_{TH} \quad \text{and} \quad v_{DS} < v_{DSSat} = v_{GS} - V_{TH}.$$

- From equation (4.7), we have, under dc condition -

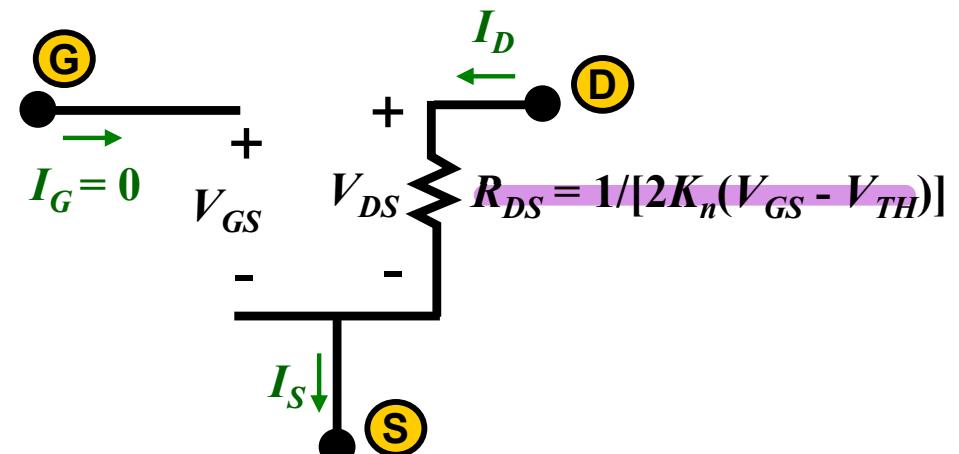
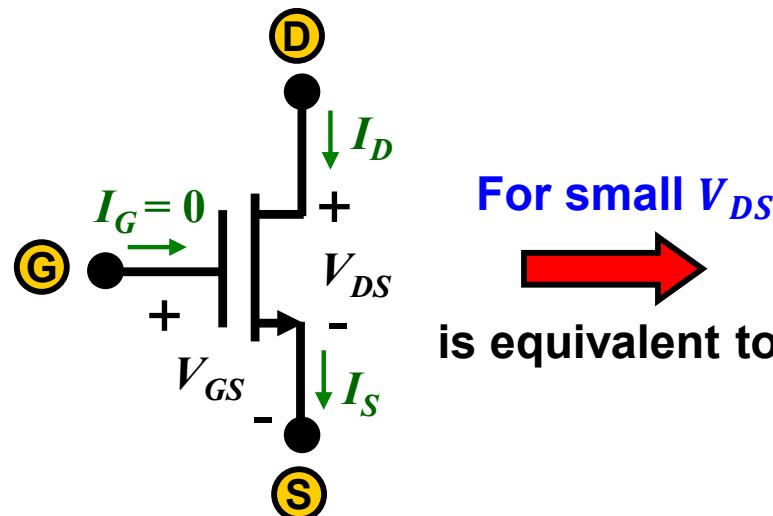
$$I_D = 2K_n \left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2 \right]$$

- For small V_{DS} , we neglect $\frac{1}{2}V_{DS}^2$,

$I_D \approx 2K_n(V_{GS} - V_{TH})V_{DS}$ → a resistance between source and drain

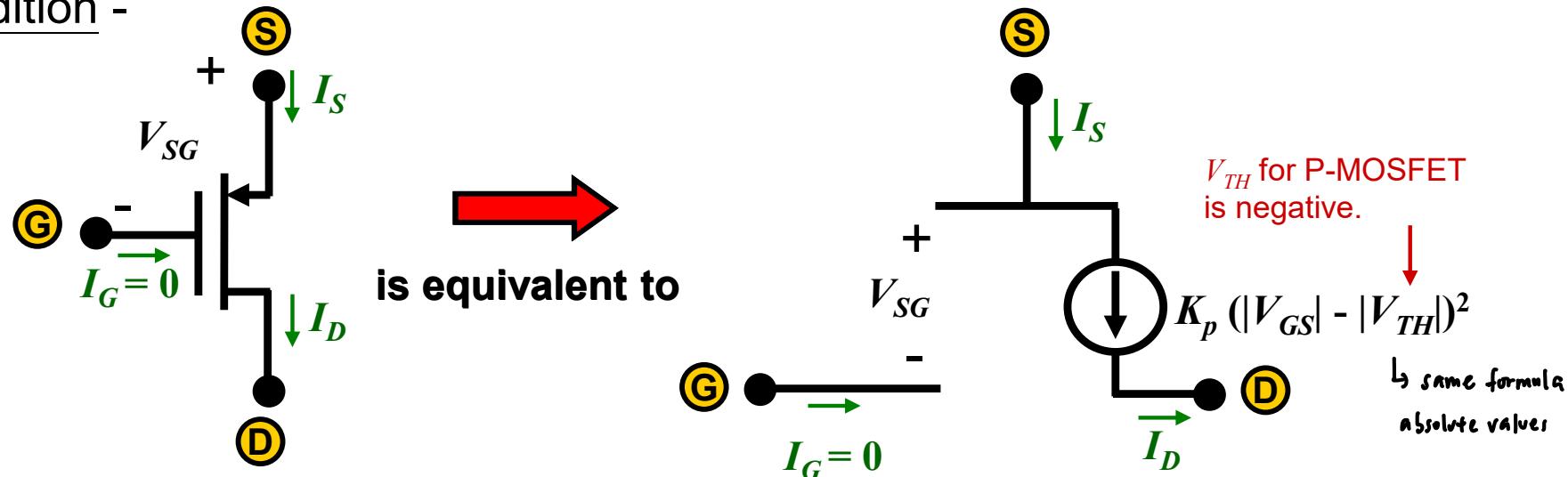
- Drain-to-source resistance for small V_{DS} is

$$R_{DS} = \frac{V_{DS}}{I_D} \mid_{small\ V_{DS}} \approx 1/[2K_n(V_{GS} - V_{TH})] \rightarrow \begin{matrix} \text{voltage controlled resistor,} \\ V_{GS} \uparrow, R_{DS} \downarrow \end{matrix}$$

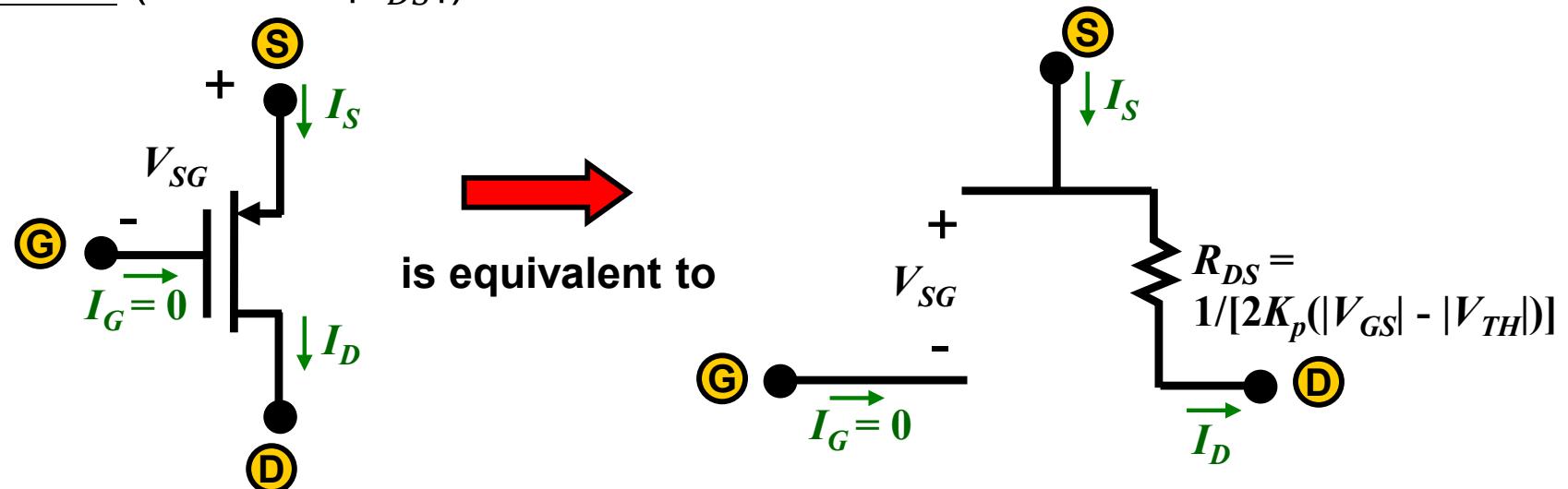


MOSFET – Large-Signal Models (p-MOSFET)

- In the **saturation region**: $|v_{GS}| > |V_{TH}|$ and $|v_{DS}| \geq |v_{GS}| - |V_{TH}|$ and under dc condition -



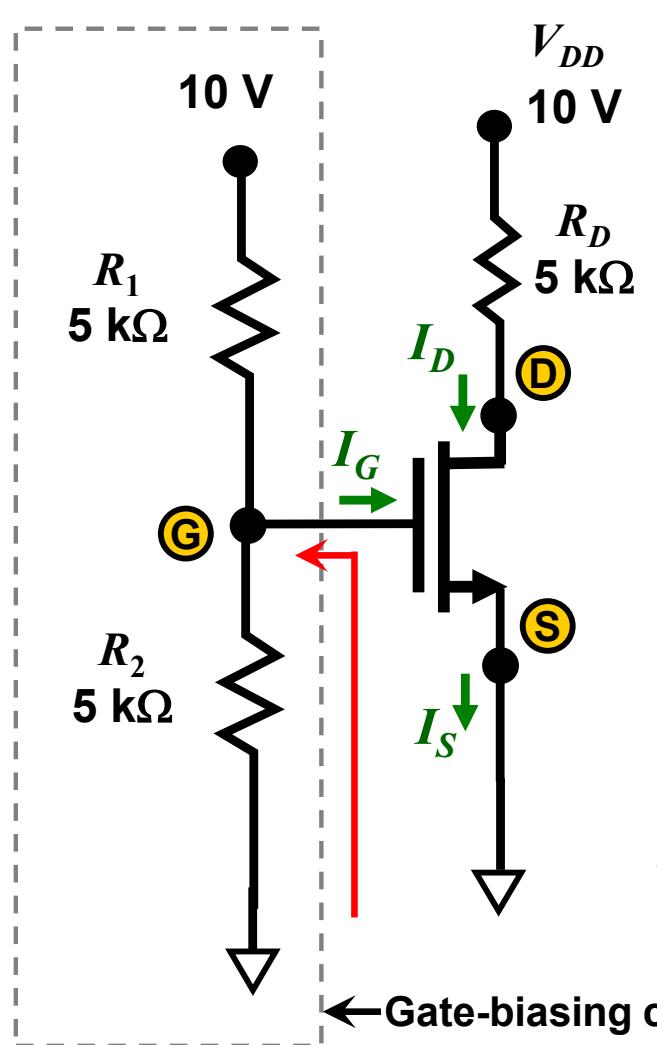
- In the **linear region**: $|v_{GS}| > |V_{TH}|$ and $|v_{DS}| \leq |v_{GS}| - |V_{TH}|$ and under dc condition (for small $|v_{DS}|$) -



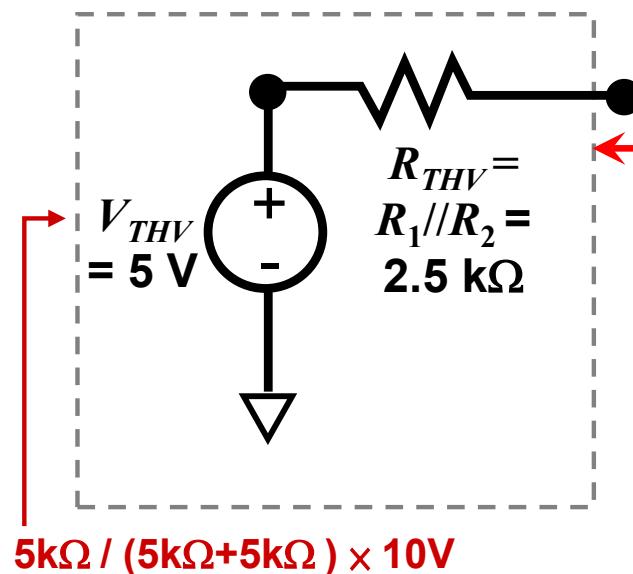
MOSFET – Calculation of Bias Point (dc Analysis)

Example 1 (Thevenin equivalent method)

Find the current I_D and the voltage V_D . Assume that $\mu_n C_{ox} = 2.0 \times 10^{-5} \text{ A/V}^2$, $W/L = 5$, and $V_{TH} = 1 \text{ V}$.



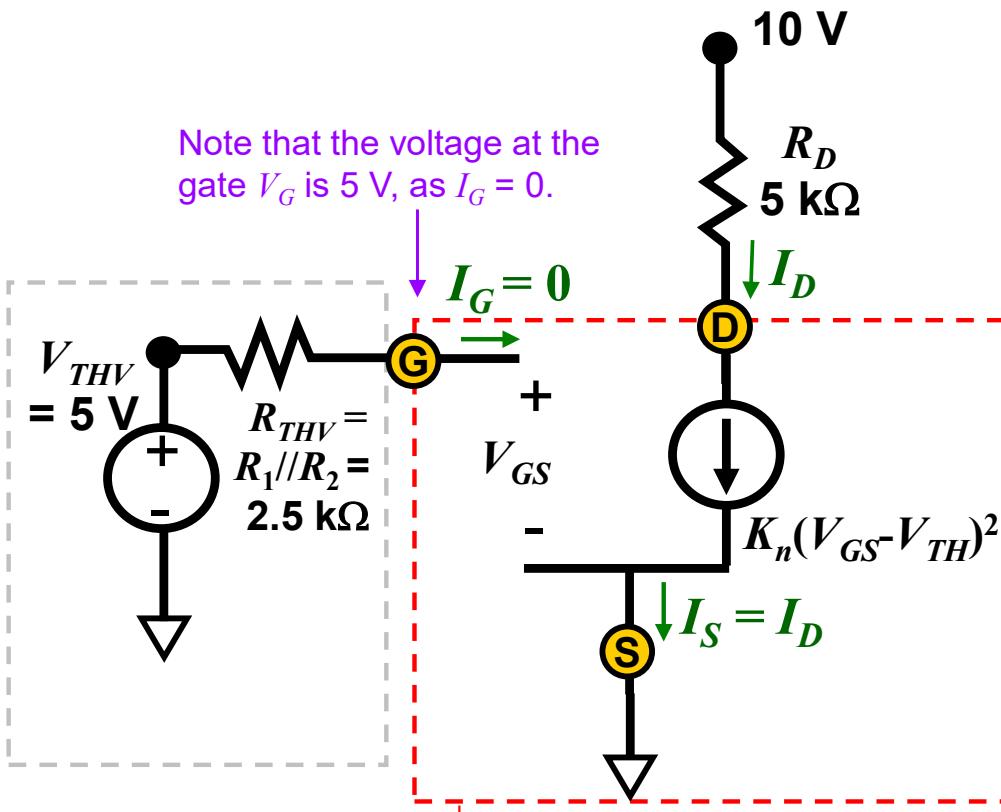
- First, we obtain the Thevenin equivalent circuit of the gate-biasing circuit shown in the dashed box (gray):



Note that the voltage divider method can also be used to find the voltage at the node G as the gate current $I_G = 0$.

MOSFET – Calculation of Bias Point

Example 1 (Thevenin equivalent method)



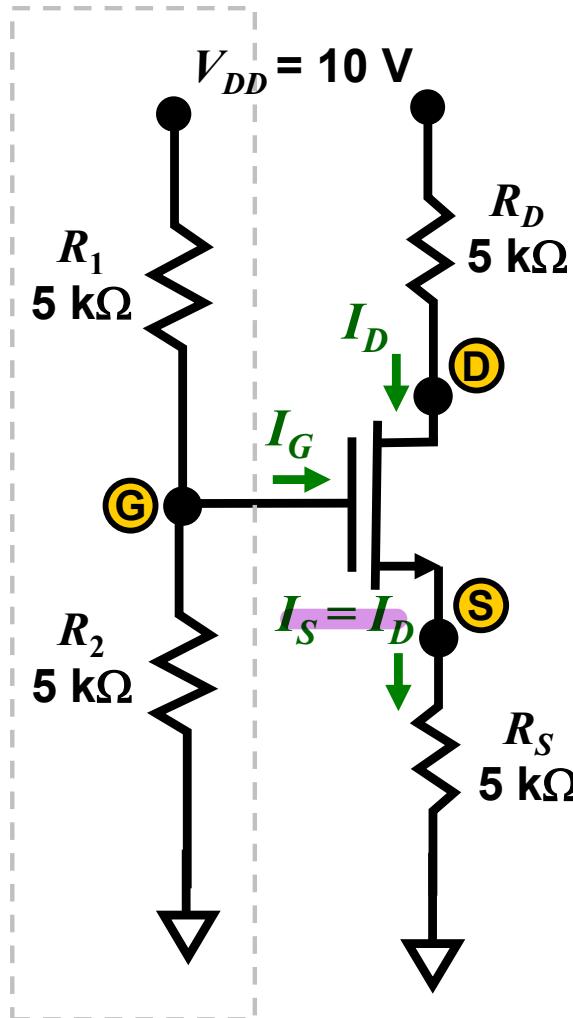
Large Signal Model for
N-MOSFET in Saturation

- Next, we **assume** the MOSFET is in **saturation** (needs to check later) and replace it with the corresponding large-signal model.
- We see that $V_{GS} = V_{THV} = 5 \text{ V} (> V_{TH})$
- Substitute V_{GS} and other given parameters into the equation for I_{Dsat} :
$$\begin{aligned} I_D &= I_{Dsat} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \\ &= 0.5 \times (2.0 \times 10^{-5}) \times 5 \times (5 - 1)^2 \\ &= 0.8 \text{ mA} \end{aligned}$$
- Hence, $V_D = 10 \text{ V} - I_D R_D = 6 \text{ V}$
- Check if MOSFET is indeed in saturation:
 - $V_{GS} = 5 \text{ V} > V_{TH} = 1 \text{ V}$
 - $V_{DS} = 6 \text{ V} > V_{GS} - V_{TH} = 4 \text{ V}$.
- Yes.

MOSFET – Calculation of Bias Point

Example 2 (Voltage Divider method)

A $5\text{ k}\Omega$ resistance is connected between the N-MOSFET source and ground of the circuit of Example 1. Determine the values of I_D and V_D .



- By means of voltage divider, $V_G = 5\text{ V}$.
- $V_{GS} = V_G - V_S$. What is V_S ?
- $V_S = I_S R_S = I_D R_S$, which depends on the solution for I_D .
↳ ohm's law
- We assume the MOSFET is in saturation (needs to check later) and replace it with the corresponding large signal model.
- Examine the equation for I_{Dsat} :

$$I_D = I_{Dsat} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$= 0.5 \times (2.0 \times 10^{-5} \text{ A/V}^2) \times 5$$

$$\times (V_G - V_S - V_{TH})^2$$

square law

if want positive, can take V_S and remove absolute because V_S higher potential than V_G ↑

P-MOS

MOSFET – Calculation of Bias Point

Example 2 (Voltage Divider method) A $5\text{ k}\Omega$ resistance is connected between the N-MOSFET source and ground of the circuit of Example 1. Determine the values of I_D and V_D .

$I_D = k_p ((V_G - V_S) - (V_S - V_{TH}))^2 \rightarrow \text{absolute}$

- $V_S = V_G - V_S$. What is V_S ? $(10V - V_S = I_D \times 5\text{ k}\Omega)$
- $V_S = I_S R_S = I_D R_S$, which depends on the solution for I_D .
- We assume the MOSFET is in saturation (needs to check later) and replace it with the corresponding large signal model.
- Examine the equation for I_{Dsat} : | -3 |

$$I_D = I_{Dsat} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$= 0.5 \times (2.0 \times 10^{-5} \text{ A/V}^2) \times 5$$

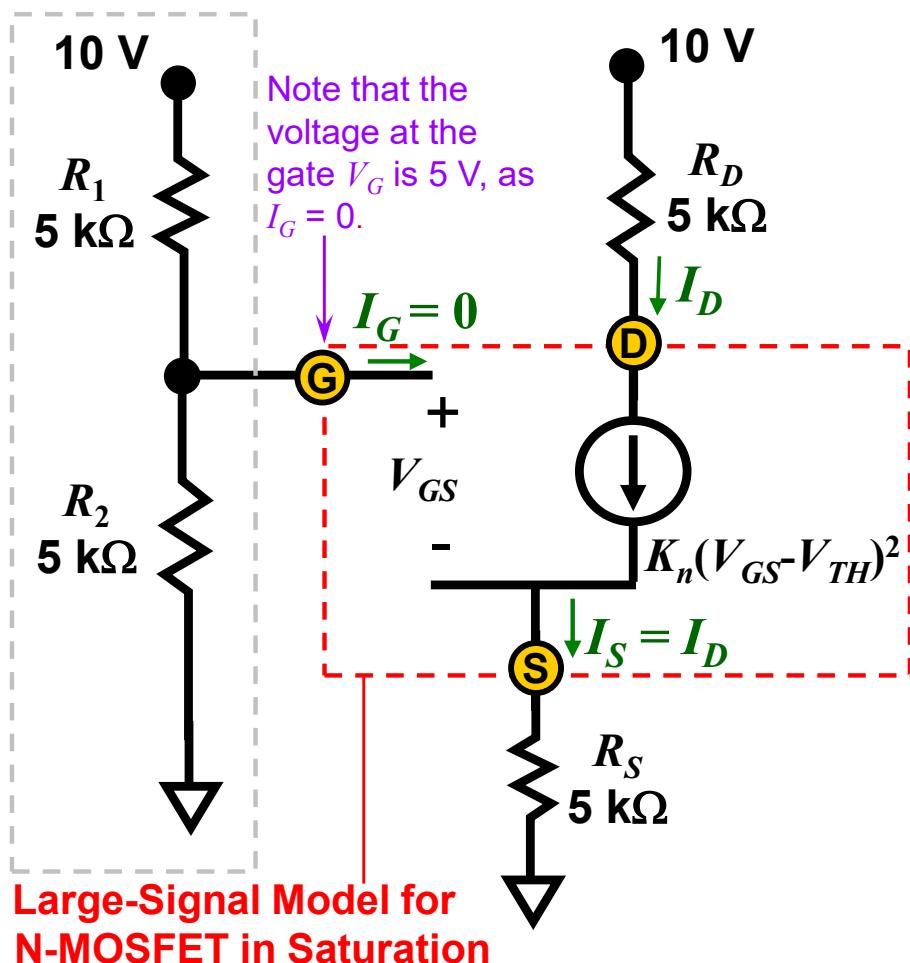
$$\times (V_G - V_S - V_{TH})^2$$

$$V_D = I_D R_D$$

$$= 0.5 \times (2.0 \times 10^{-5} \text{ A/V}^2) \times 5 \times (V_G - V_S - V_{TH})^2 = -3 |$$

MOSFET – Calculation of Bias Point

Example 2 (Voltage Divider method)



- $$I_D = I_{Dsat} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$
$$= 0.5 \times (2.0 \times 10^{-2} \text{ mA/V}^2) \times 5 \times (V_G - V_S - V_{TH})^2$$
- $$I_{Dsat} = 0.05(5 - I_{Dsat})^2$$
 I_{Dsat} in mA R_S in $\text{k}\Omega$
- Solving the above quadratic equation,
 $I_{Dsat} = 2.09 \text{ mA or } 0.31 \text{ mA.}$
- Check: $I_{Dsat} = 2.09 \text{ mA}$ cannot be a solution as this leads to $V_S > 10 \text{ V}$.
- Therefore, $I_{Dsat} = 0.31 \text{ mA.}$
In this case, $V_D = 8.45 \text{ V}$, $V_S = 1.55 \text{ V}$,
 $V_{DS} = 6.9 \text{ V}$, $V_{GS} = 3.45 \text{ V}$.

- Check that MOSFET is indeed in saturation: $V_{GS} = 3.45 \text{ V} > V_{TH} = 1 \text{ V}$ &
 $V_{DS} = 6.9 \text{ V} > V_{GS} - V_{TH} = 2.45 \text{ V}$.

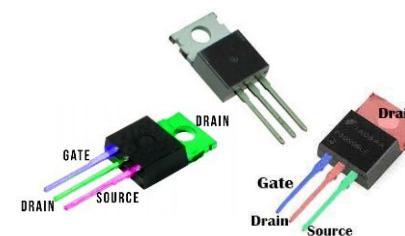
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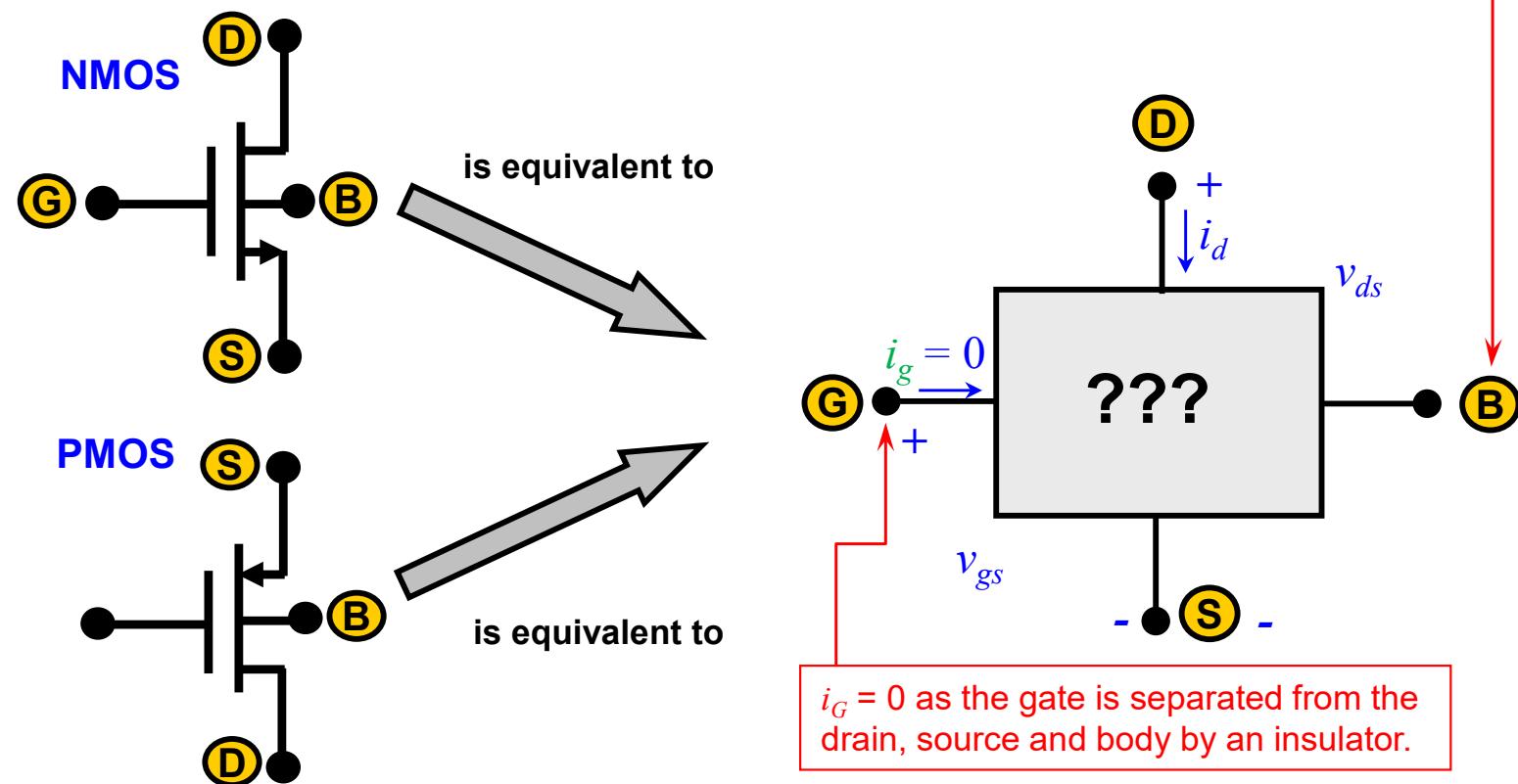
References

- Sedra and Smith, Microelectronic Circuits, Theory and Applications, Fifth Edition (International Version), Oxford (2004), pp. 325 – 349, pp. 426-429, pp. 901-921.



MOSFET – Small-Signal Model

- Interested in the small-signal model of MOSFET in **saturation** operation.
- In developing the small-signal model of MOSFET, we seek a set of **linear relationships** among the small-signal components of the drain current, gate-to-source voltage and drain-to-source voltage - i_d , v_{gs} and v_{ds} (at a bias point).
- If the body (substrate) is **not** tied to the source, then a voltage applied to the body (w.r.t. to source) will affect the current in the MOSFET. This will be dealt with in Section 8.



MOSFET – Small-Signal Model (Transconductance g_m)

- From equation (4.8), drain current in saturation –

$$i_D = i_{Dsat} = K_n(v_{GS} - V_{TH})^2$$

- At the bias point, dc drain current –

$$I_D = I_{Dsat} = K_n(V_{GS} - V_{TH})^2$$

- A linear relationships between a small change in the drain current, i_d , and a small change in gate-to-source voltage, v_{gs} , can be found by linearizing the i_D - v_{GS} characteristic.

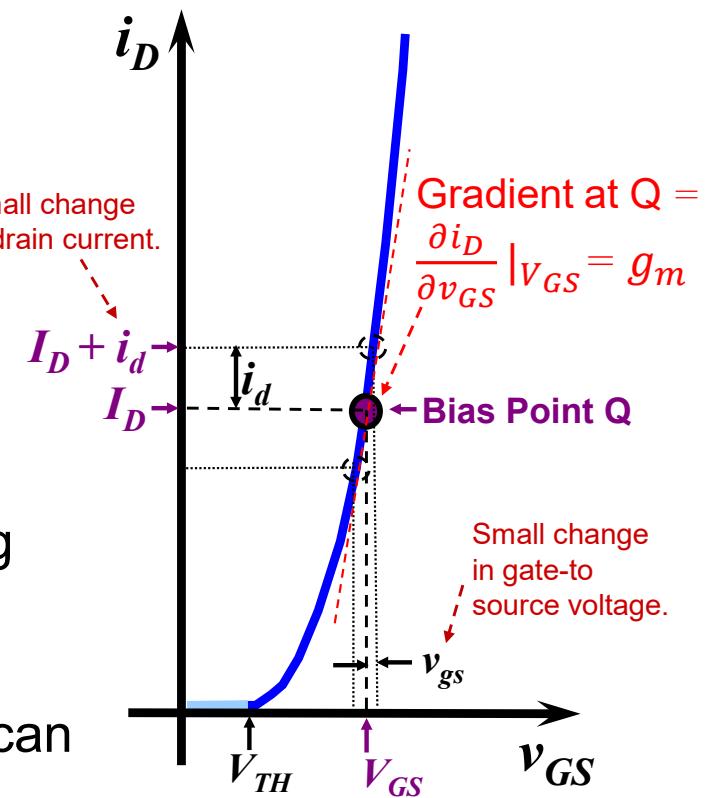
- A small change in i_D w.r.t a small change in v_{GS} , can be approximated by the derivative of i_D w.r.t v_{GS} –

$$\frac{i_d}{v_{gs}} \Big|_{V_{GS}} \approx \frac{\partial i_D}{\partial v_{GS}} \Big|_{V_{GS}} = 2K_n(V_{GS} - V_{TH}) = g_m \rightarrow 2\sqrt{K_n(V_{GS} - V_{TH})^2} \quad (4.12)$$

- Transconductance (for n-channel MOSFET):

$$g_m = \frac{i_d}{v_{gs}} = 2K_n(V_{GS} - V_{TH}) = 2\sqrt{K_n I_D} = 2I_D/(V_{GS} - V_{TH}) \quad (4.13)$$

↓
in terms of I_D (DC)



MOSFET – Small-Signal Model (Transconductance g_m)

- Transconductance (for n-channel MOSFET):

$$g_m = \frac{i_d}{v_{gs}} = 2K_n(V_{GS} - V_{TH}) = 2\sqrt{K_n I_D} = 2I_D/(V_{GS} - V_{TH}) \quad (4.13)$$

Transconductance, g_m , models a small change in the drain current, i_d , caused by a small change in gate-to-source voltage, v_{gs} -

$$i_d = g_m v_{gs} \rightarrow \text{small signal (ss)} \quad (4.14)$$

$i_d = g_m v_{gs}$

Small change in drain current.

Small change in gate-to-source voltage

- For p-channel MOSFET: $i_D = K_p(|v_{GS}| - |V_{TH}|)^2 = K_p(v_{SG} - |V_{TH}|)^2$

$$g_m = \frac{i_d}{v_{sg}} = \frac{\partial i_D}{\partial v_{SG}}|_{V_{SG}} = 2K_p(V_{SG} - |V_{TH}|) = 2K_p(|V_{GS}| - |V_{TH}|) \quad (4.15)$$

Transconductance, g_m , models a small change in the drain current, i_d , caused by a small change in source-to-gate voltage, v_{sg} -

$$i_d = g_m v_{sg} \quad (4.16)$$

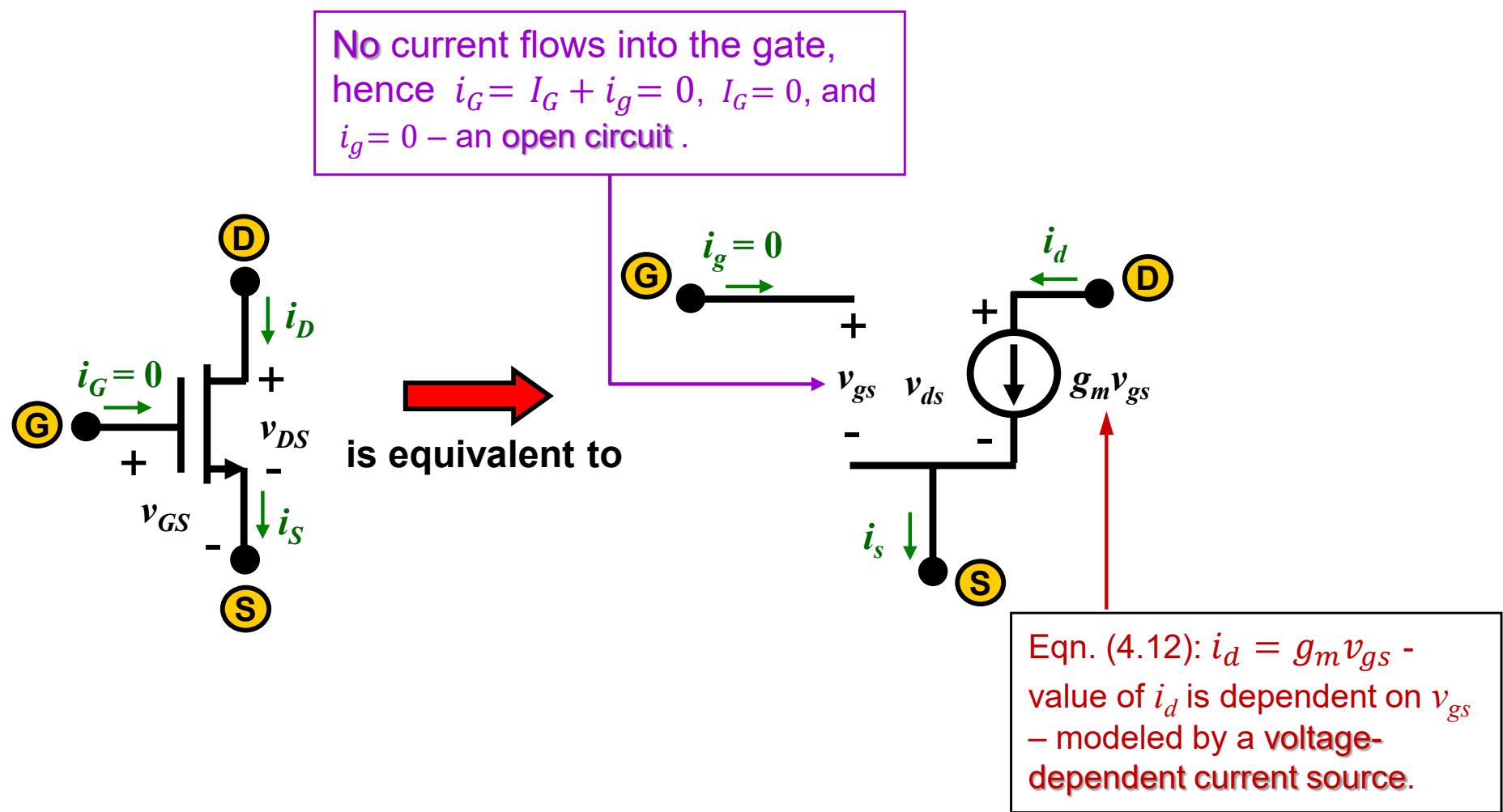
$i_d = g_m v_{sg}$

Small change in drain current.

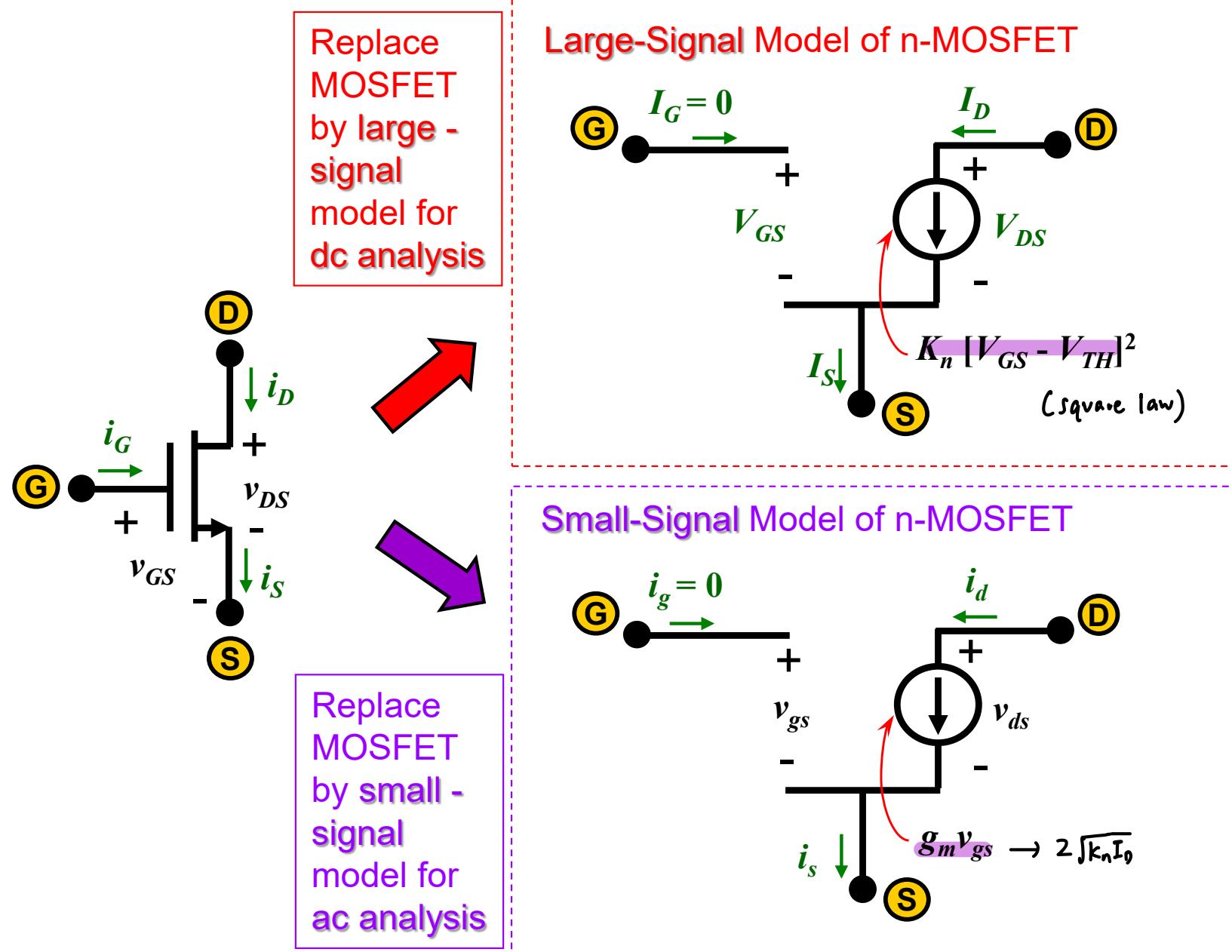
Small change in source-to-gate voltage

MOSFET – Small-Signal Model

- Small-signal model of n-channel MOSFET is developed using equation (4.13).
- Note that $i_G = I_G + i_g = 0$ since no current flows into the gate of the MOSFET, i.e. $I_G = 0$ and $i_g = 0$.

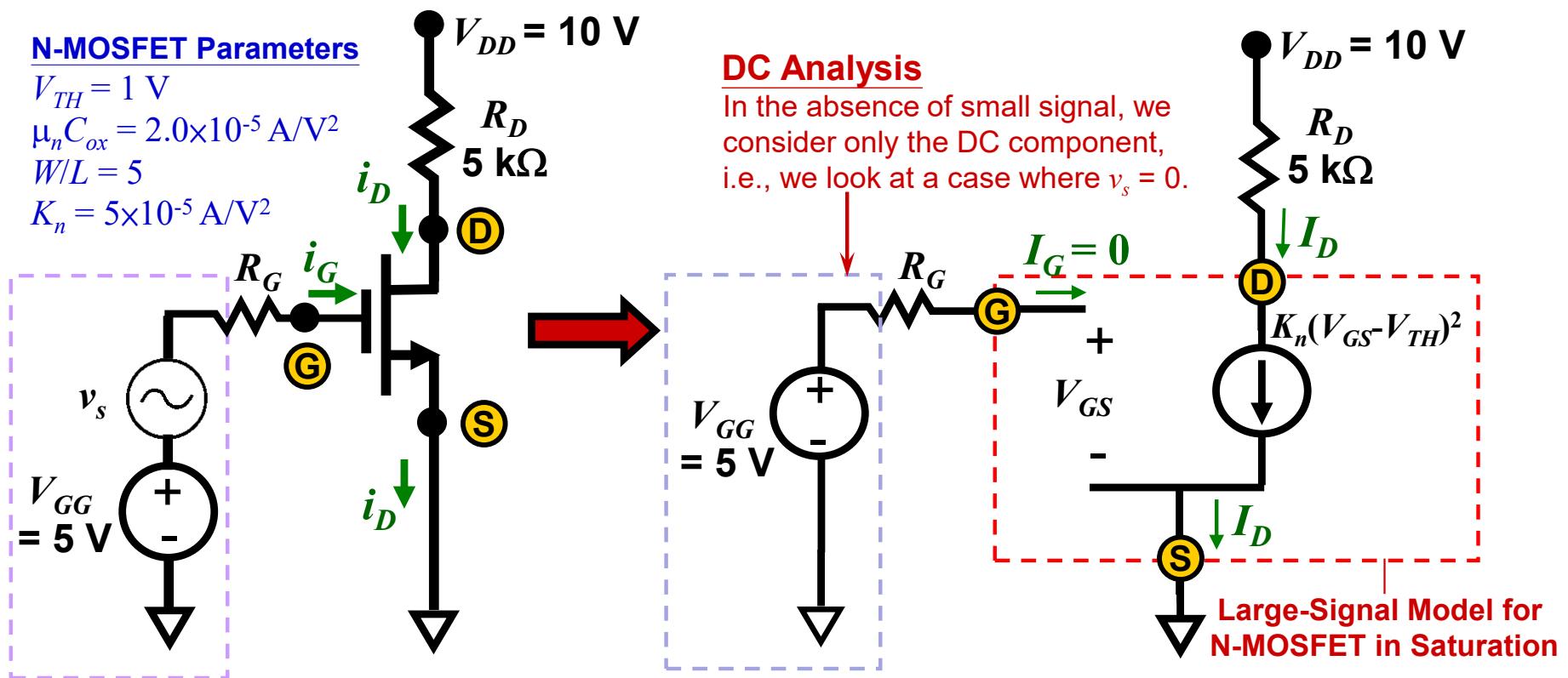


MOSFET – Large- & Small-Signal Saturation Mode Models



MOSFET – Amplifier Circuit Operation and Analysis

- A simple MOSFET amplifier circuit is shown below.
- The dc voltage sources, V_{DD} and V_{GG} are used to set the dc bias point, and an ac (small signal) source, v_s , is applied to the input circuit (involving the gate and source of MOSFET).
- Two types of operation: dc and ac operations.
- The dc bias point can be determined using the saturation mode large-signal model, and in the absence of the ac (small signal) source, v_s .

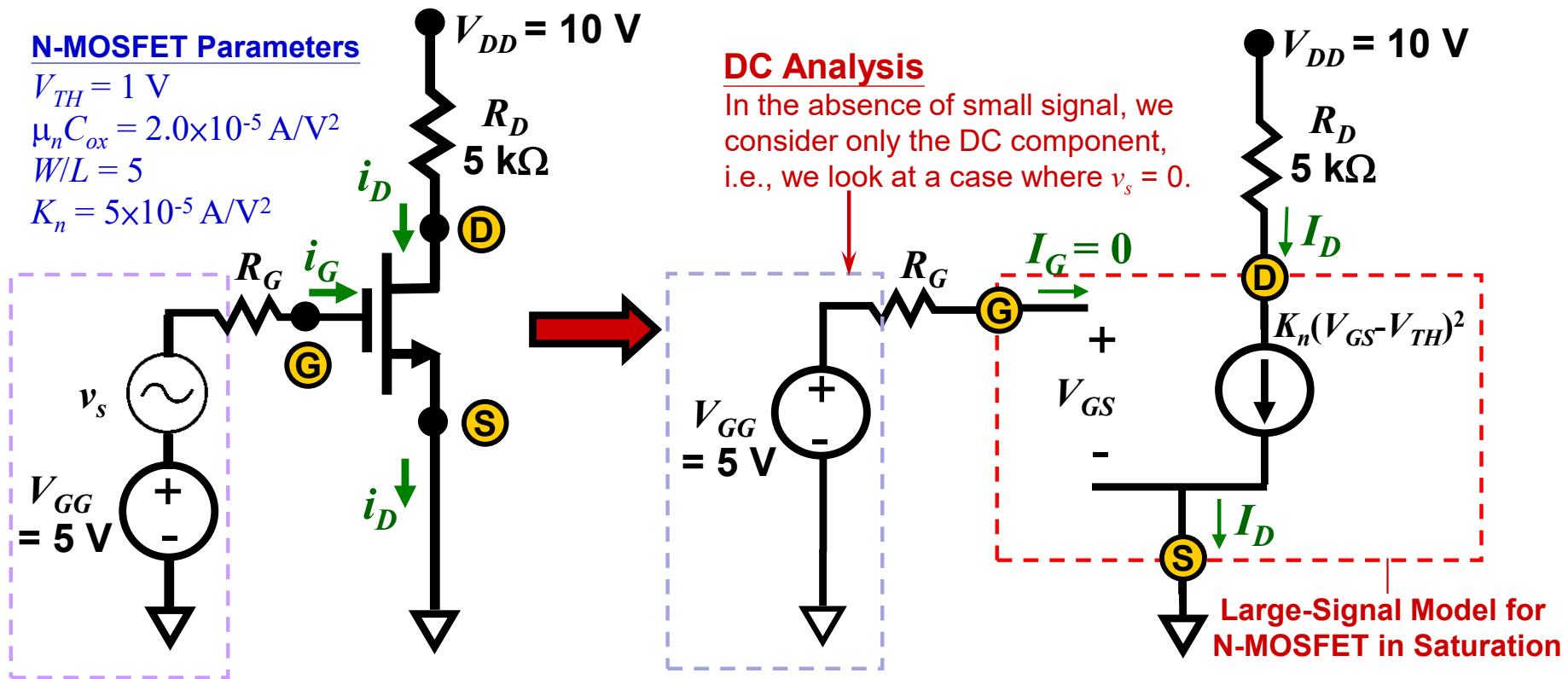


MOSFET – Amplifier Circuit (dc analysis)

- ❑ Assume MOSFET operates in saturation region (need to check later).
 - ❑ We see that $V_{GS} = V_{GG} = 5$ V (as $I_G = 0$), which can be substituted into the equation for $I_D = I_{Dsat}$ -

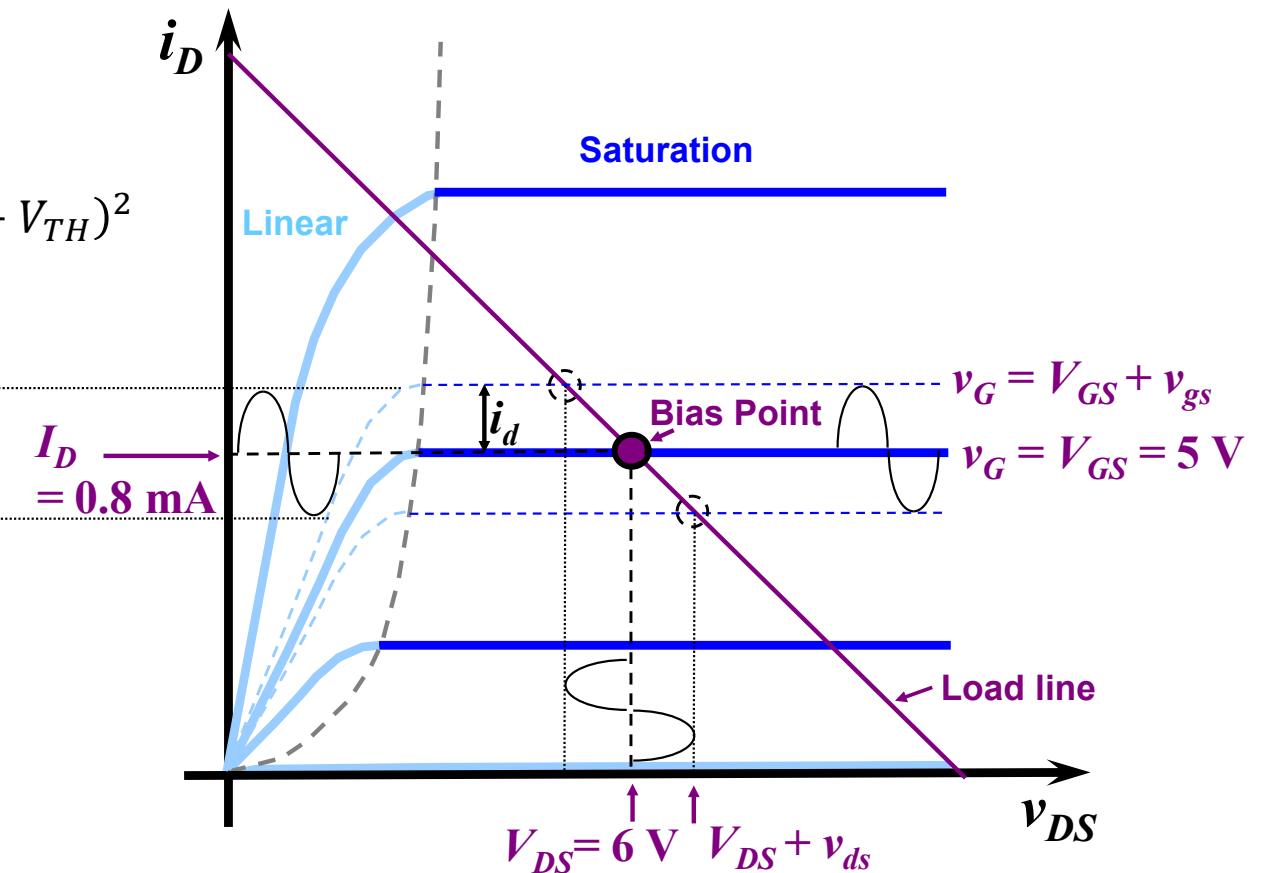
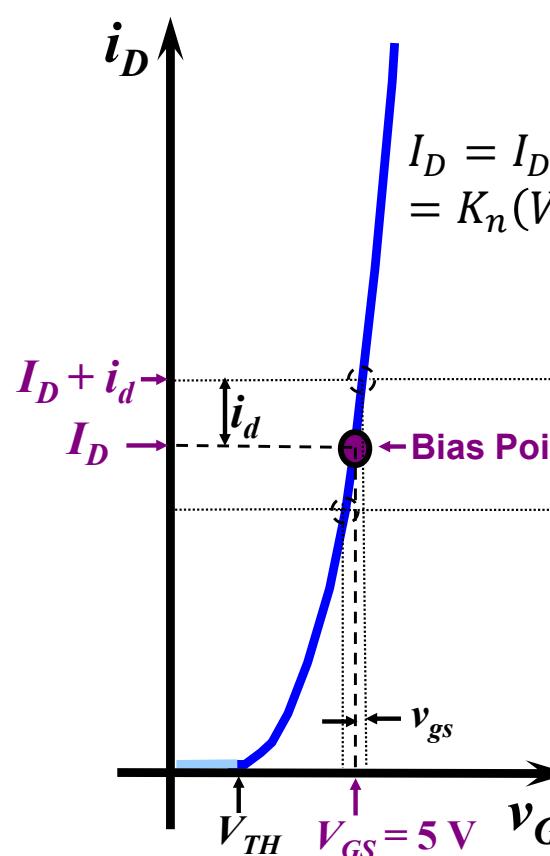
$$I_D = I_{Dsat} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 = 0.8 \text{ mA}$$

- ❑ From output circuit load line equation: $V_{DS} = V_{DD} - I_D R_D = 6$ V.
 - ❑ Check: $V_{GS} > V_{TH}$ & $V_{DS} > V_{GS} - V_{TH} = 4$ V, MOSFET operates in saturation.



MOSFET – Amplifier Circuit (dc vs ac operation)

- The dc bias point on the i_D - v_{GS} and i_D - v_{DS} curves are shown below.
- In the presence of an ac (small signal) source, v_s , -
 - $i_D = I_D + i_d$, $v_{GS} = V_{GS} + v_{gs}$, and $v_{DS} = V_{DS} + v_{ds}$
 - i_D , v_{GS} and v_{DS} all have a small signal component and they vary with time.

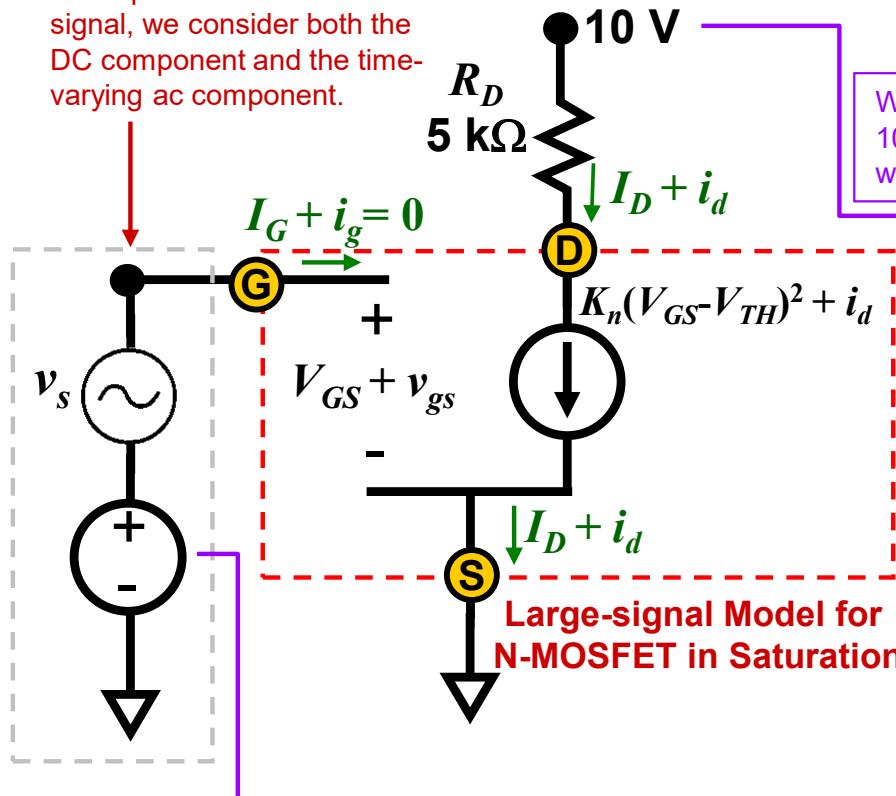


Small-signal voltage v_{gs} varies with time. It contains information to be amplified.

Load line equation: $v_{DS} = V_{DD} - i_D R_D$
 Rearranging, we have $i_D = (V_{DD} - v_{DS})/R_D$
 $= (10\text{V} - v_{DS})/5 \text{ k}\Omega = 2 \text{ mA} - (v_{DS}/5\text{k}\Omega)$

MOSFET – Amplifier Circuit (ac analysis)

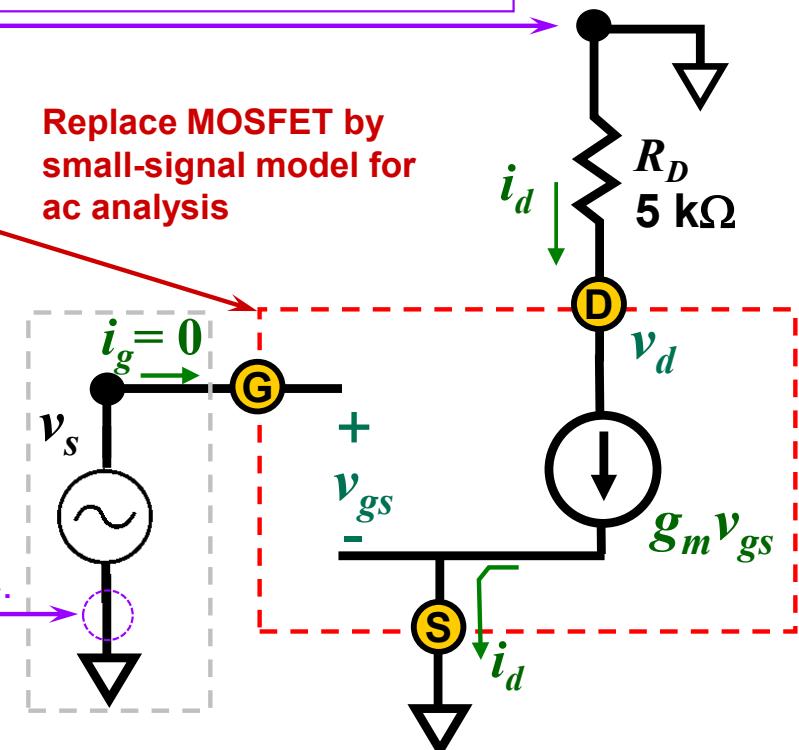
In the presence of small-signal, we consider both the DC component and the time-varying ac component.



Small-Signal Equivalent Circuit

What is the change in voltage at this point?
10 V is a constant voltage supply which does not vary with time. Answer: 0 V. This is an **ac short**.

Replace MOSFET by
small-signal model for
ac analysis



- Small-signal (ac) analysis using the small-signal equivalent circuit -

$$v_d = 0 - i_d R_D = -g_m v_{gs} R_D$$

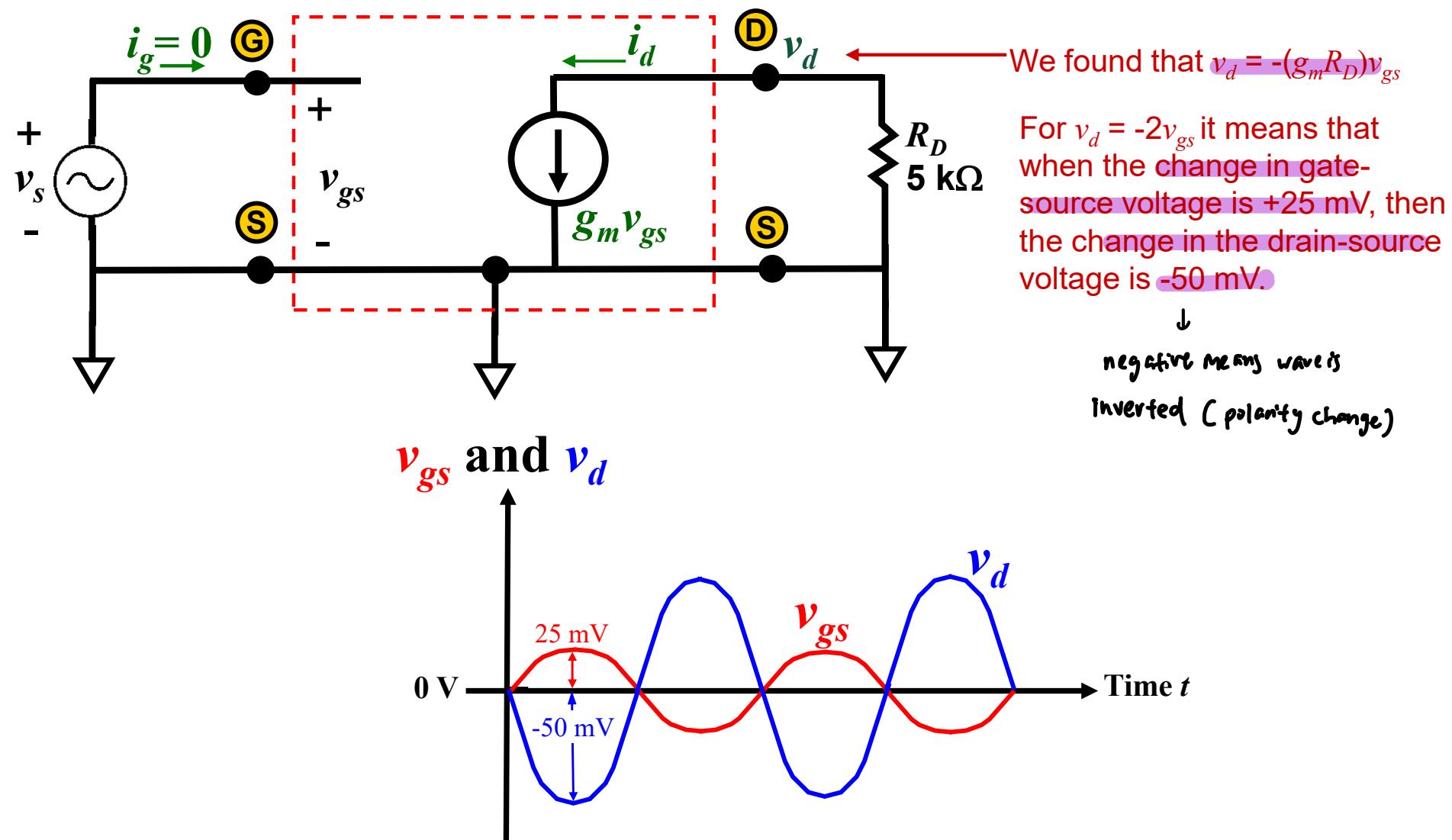
$$\text{Eqn. (4.13): } g_m = 2K_n(V_{GS} - V_{TH}) = 2(2 \times 10^{-5} \text{ A/V})(5 - 1) = 4 \times 10^{-4} \text{ A/V}$$

$$\text{Hence, } \frac{v_d}{v_{gs}} = -g_m R_D = -(4 \times 10^{-4} \text{ A/V}) \times 5\text{k}\Omega = -2$$

(Ans)

MOSFET – Interpretation of Small-Signal Analysis Results

- The small-signal equivalent circuit shown in the previous slide can be re-drawn as -

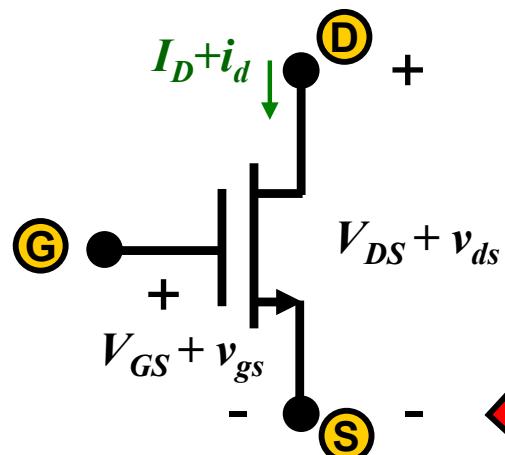




MOSFET – Small-Signal Model (p-MOSFET)

same like BJT for
small-signal

N-MOSFET

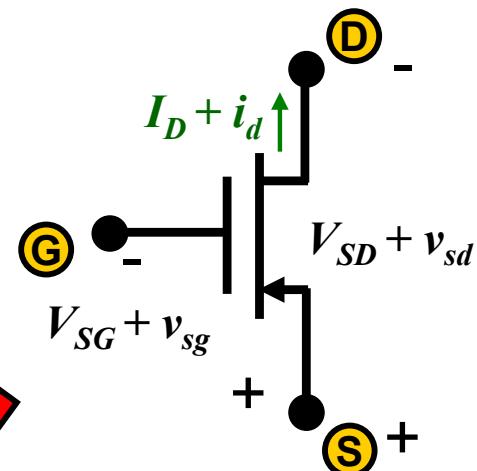


The change in drain current for the N-MOSFET is positive when there is an increase in the Drain current flowing into the drain

$$\downarrow \\ i_d = g_m v_{gs}$$

Replace the MOSFET by this Hybrid- π Model for Small-Signal Analysis

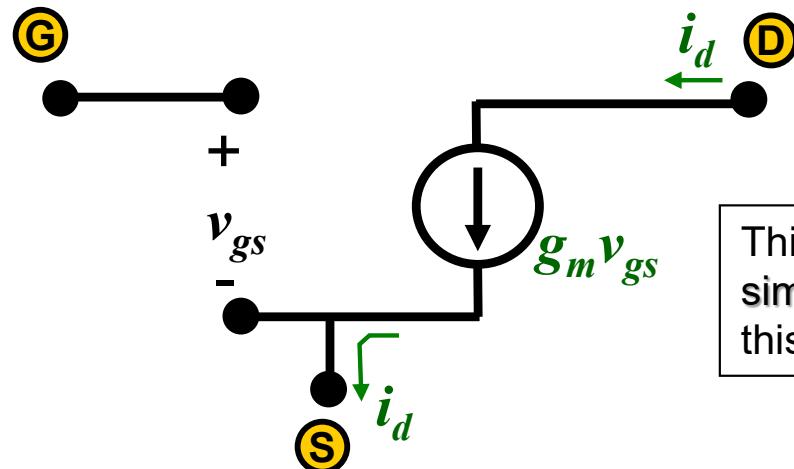
P-MOSFET



The Change in drain current for the P-MOSFET is positive when there is an increase in the Drain current flowing out of the drain

$$\downarrow \\ i_d = g_m v_{sg}$$

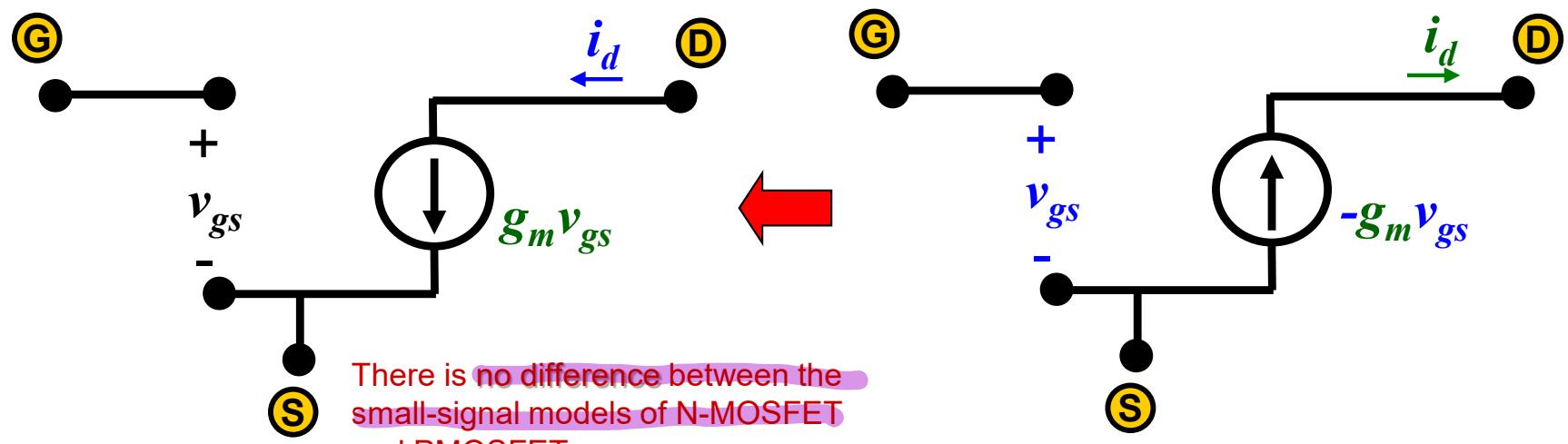
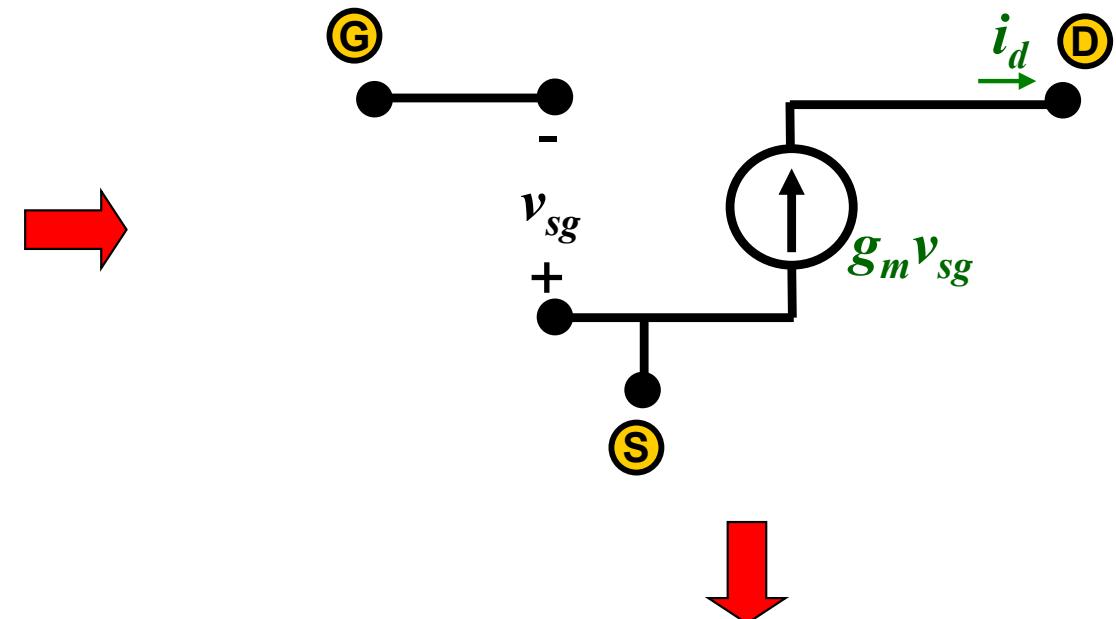
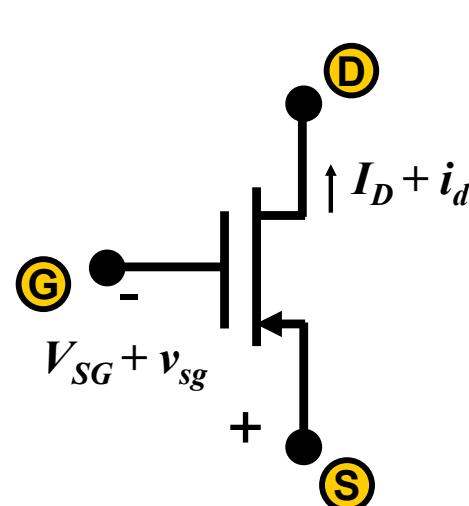
Hybrid- π Model for N-MOSFET or P-MOSFET



This Hybrid- π Model is in its simplest form here. We will use this simplest form by default.

MOSFET – Small-Signal Model (p-MOSFET)

P-MOSFET



There is no difference between the small-signal models of N-MOSFET and PMOSFET

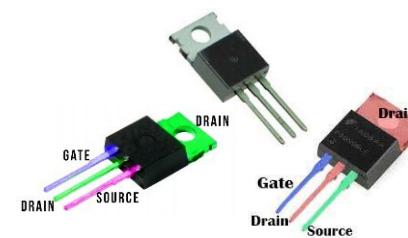
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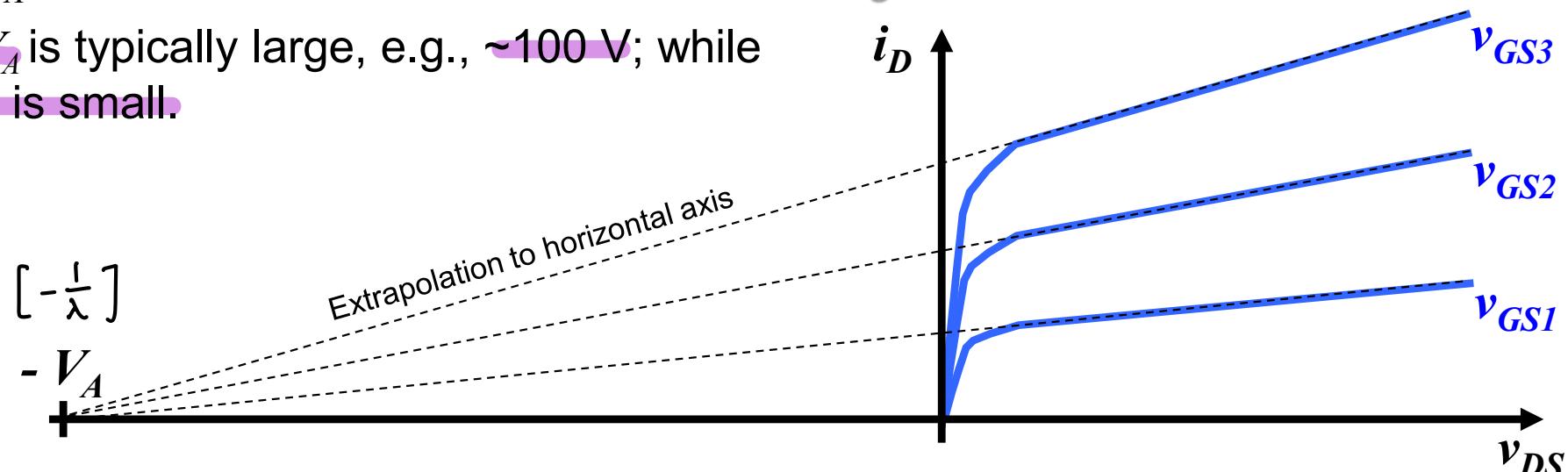
References

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MOSFET – Non-Ideal i_D - v_{DS} Relationship

- For a real (non-ideal) MOSFET, the i_D - v_{DS} characteristics in the saturation region is not independent on v_{DS} (c.f. ideal characteristics in slide MOSFET-21). In fact, there is a slight dependence owing to the Channel-Length Modulation effect*.
- The i_D - v_{DS} characteristics in the saturation region would then have a slight upward slope, as shown in the figure below.
- When the i_D - v_{DS} characteristics in the saturation region are extrapolated to the negative v_{DS} -axis, they intersect approximately at the same voltage, $-V_A$, also known as the Early voltage, as an analogy to that in the BJT.
- $V_A = 1/\lambda$, where λ is called the Channel Length Modulation factor.
- V_A is typically large, e.g., ~ 100 V; while λ is small.



*Channel-length modulation has similar effect as the Early Effect in BJT (slide BJT-14).

MOSFET – Non-Ideal i_D - v_{DS} Relationship

In exam, only if qtn explicitly states consider channel effect then use λ , if not don't bother

- With Channel-Length Modulation effect, the i_D - v_{DS} characteristics in the saturation region is modified from eqn. (4.2) on slide MOSFET-21 to –

$$\begin{aligned} i_D = i_{Dsat} &= \frac{1}{2} \mu_n \frac{W}{L} C_{ox} (v_{GS} - V_{TH})^2 (1 + \lambda v_{DS}) = f(v_{GS}, v_{DS}) \\ &= \frac{1}{2} \mu_n \frac{W}{L} C_{ox} (v_{GS} - V_{TH})^2 (1 + v_{DS}/V_A) = f(v_{GS}, v_{DS}) \end{aligned} \quad (4.17)$$

The additional factor λv_{DS} or v_{DS}/V_A above accounts for the dependence of i_D on v_{DS} , or the Channel-Length Modulation effect.

- i_D is now a function of both v_{GS} and v_{DS} : $i_D = f(v_{GS}, v_{DS})^*$.
- Small-signal drain current current, i_d , will then be contributed by not only the small-signal gate-to-source voltage, v_{gs} , but also the drain-to-source voltage, v_{ds} –

$$\Delta i_d = i_d \approx \underbrace{\frac{\partial i_D}{\partial v_{GS}}|_{V_{DS}}}_{\text{Contribution of } v_{gs}} \times v_{gs} + \underbrace{\frac{\partial i_D}{\partial v_{DS}}|_{V_{GS}}}_{\text{Contribution of } v_{ds}} \times v_{ds} \quad (4.18)$$

- Mathematical proof of equation (4.18) is given in Appendix H.

* Note the difference between equation (4.2) for an ideal n-MOSFET and equation (4.17).

MOSFET – Output Resistance r_o

- Equation (4.17) - $i_D = \frac{1}{2} \mu_n \frac{W}{L} C_{ox} (v_{GS} - V_{TH})^2 (1 + \lambda v_{DS})$
 $= \frac{1}{2} \mu_n \frac{W}{L} C_{ox} (v_{GS} - V_{TH})^2 (1 + v_{DS}/V_A) = f(v_{GS}, v_{DS})$
- For given V_{GS} and V_{DS} (point Q), when v_{DS} changes, i_D will change. Change in i_D owing to a small change in v_{DS} is given approximately by the slope (or derivative) of the corresponding i_D-v_{DS} curve –

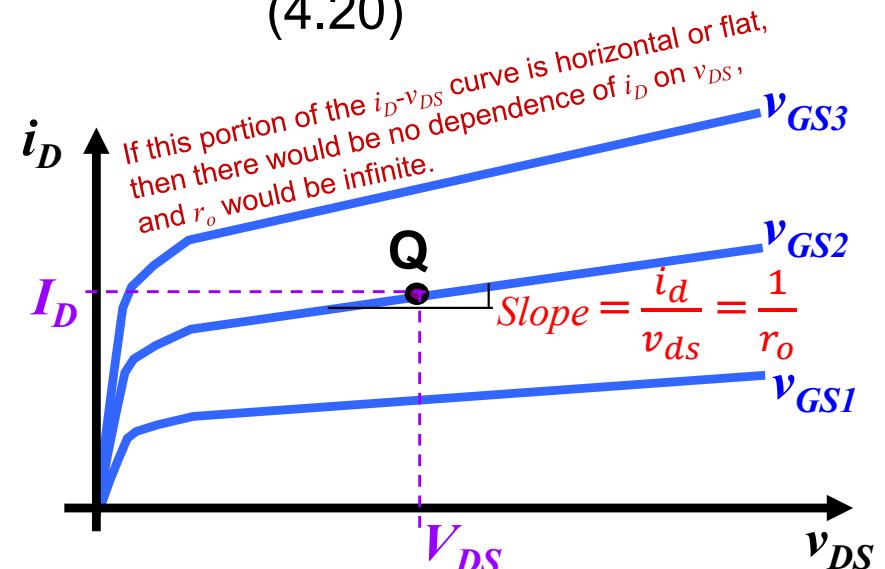
$$\begin{aligned} \frac{i_d}{v_{ds}} &= \frac{\partial i_D}{\partial v_{DS}} \Big|_{V_{DS}, V_{GS}} = \frac{1}{2} \mu_n \frac{W}{L} C_{ox} (V_{GS} - V_{TH})^2 \lambda \approx I_D \lambda = \frac{1}{r_o} \\ &= \frac{1}{2} \mu_n \frac{W}{L} C_{ox} (V_{GS} - V_{TH})^2 / V_A \approx I_D / V_A = \frac{1}{r_o} \end{aligned} \quad (4.19)$$

→ if λ fn never given, assume it to be 0

□ Output resistance: $r_o = \frac{v_{ds}}{i_d} = \frac{1}{I_D \lambda} = \frac{V_A}{I_D}$

(4.20)

- Output resistance, r_o , models a small change in the drain current, i_d , caused by a small change in drain-to-source voltage, v_{ds} .



MOSFET – Hybrid- π Model with Output Resistance

- From equation (4.18):

$$i_d \approx \frac{\partial i_D}{\partial v_{GS}}|_{V_{GS}} \times v_{gs} + \frac{\partial i_D}{\partial v_{DS}}|_{V_{DS}} \times v_{ds} = g_m v_{gs} + \underbrace{v_{ds}/r_o}_{\text{This term accounts for the dependence of } i_d \text{ on } v_{ds}.} \quad (4.20)$$

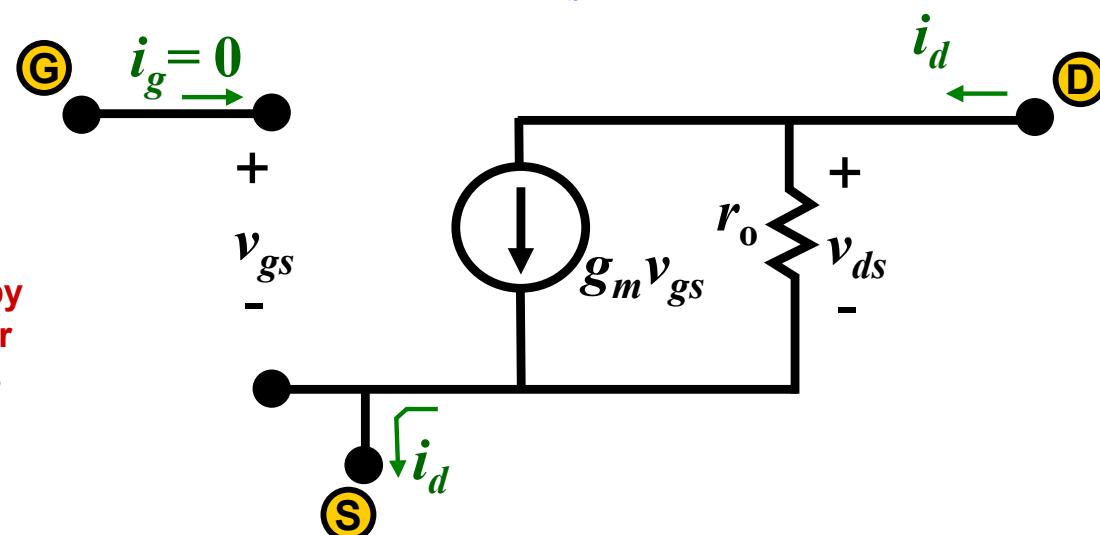
This term accounts for the dependence of i_d on v_{gs} .

This term accounts for the dependence of i_d on v_{ds} .

- To model the increase in i_D with an increase in v_{DS} , a resistance r_o is included between nodes D and S in the Hybrid- π Model for the MOSFET:

Hybrid- π Model with Output Resistance ~~※※※~~
 (The dependence of i_D on v_{DS} is accounted for)

Replace the MOSFET by this Hybrid- π Model for Small-Signal Analysis



Note: In EE2027, you can assume that r_o is infinite by default. If V_A or λ is given, then r_o should be calculated and employed in the small-signal analysis.

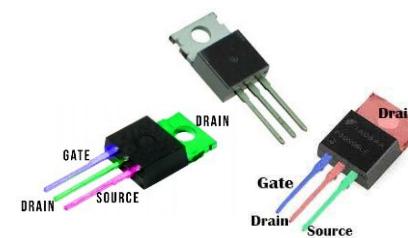
Metal Oxide Semiconductor Field Effect Transistor (**MOSFET**)

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

1. Introduction
2. Modes of operation: Linear, Saturation and Cut-off
3. i_D - v_{DS} Relationship of the MOSFET
4. Comparison between MOSFET and BJT
5. Large-Signal Models and dc Analysis
6. Small-Signal Model and ac Analysis
7. Channel-Length Modulation
8. **Body Effect and Capacitances**
9. CMOS Inverter

References

- Sedra and Smith, Microelectronic Circuits, Theory and Applications, Fifth Edition (International Version), Oxford (2004), pp. 325 – 349, pp. 426-429, pp. 901-921.



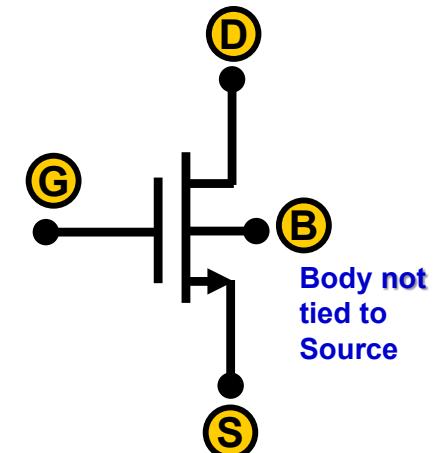
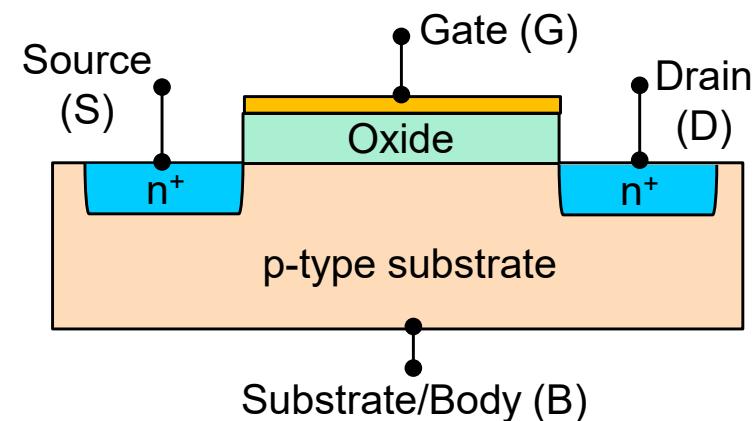
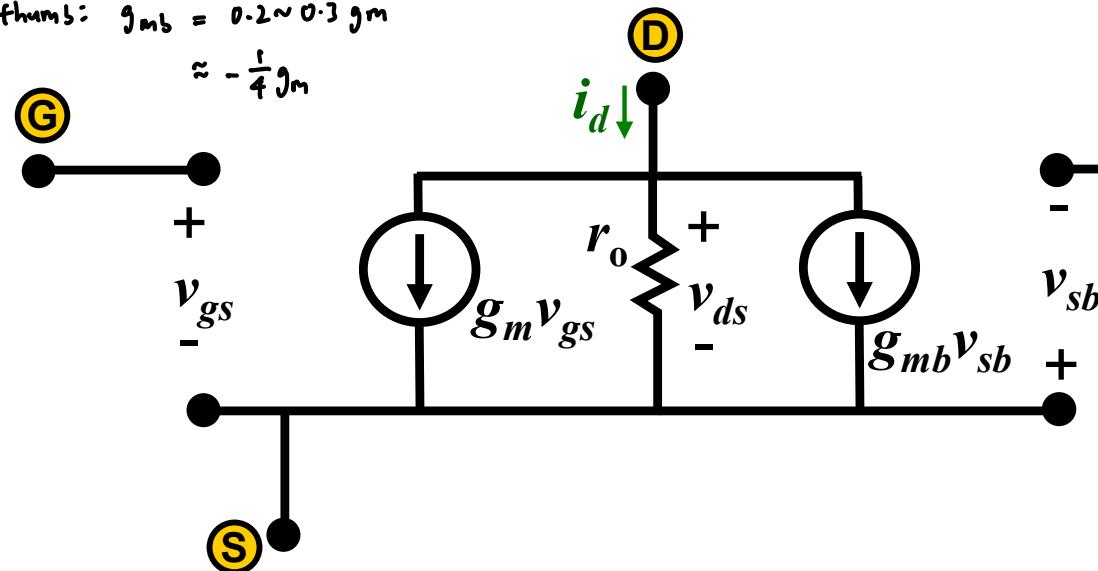
MOSFET – Body (or Bulk) Effect

- The Body Effect occurs when $v_{SB} \neq 0$ V, i.e., the source is not tied to the body.
- Consider a N-MOSFET, and suppose $v_{SB} = V_{SB} = 0$ V, but v_{SB} changes momentarily such that v_{sb} is positive. This increases the threshold voltage V_{TH} , and reduces i_D .
- The Body Effect can be modeled as

$$g_{mb} = \frac{\partial i_D}{\partial v_{SB}} \Big|_{V_{GS}, V_{DS}} = \frac{i_d}{v_{sb}} < 0$$

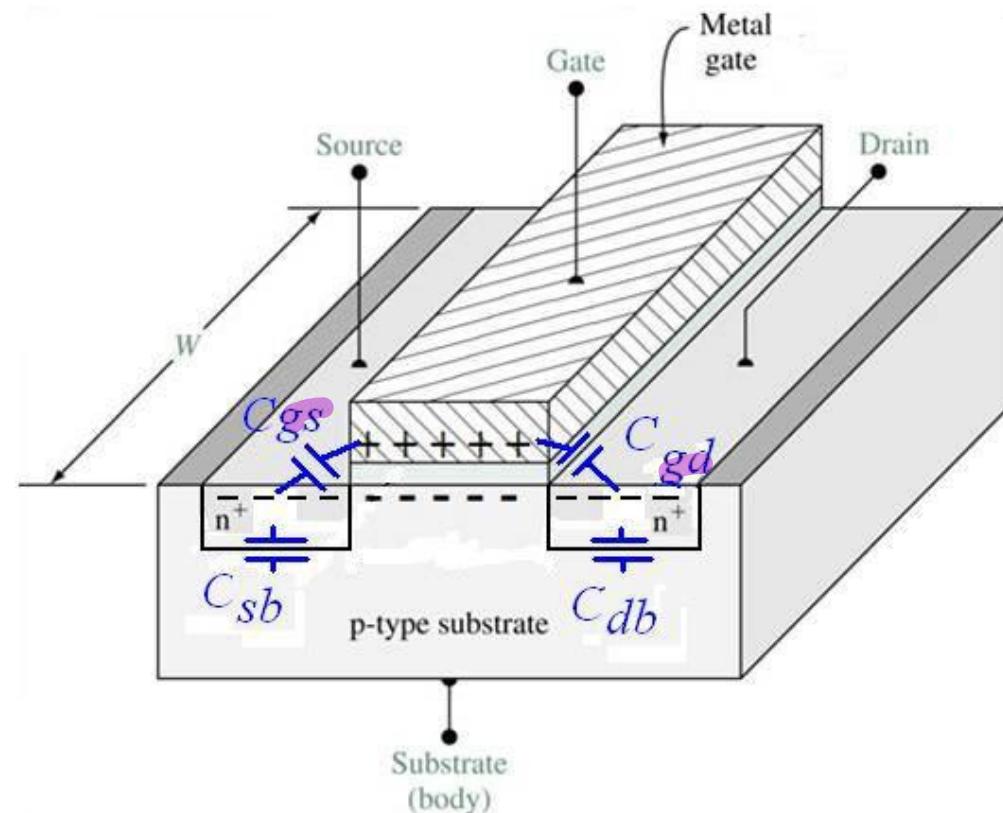
body
transconductance

L
rule of thumb: $g_{mb} = 0.2 \sim 0.3 g_m$
 $\approx -\frac{1}{4} g_m$



MOSFET - Capacitances

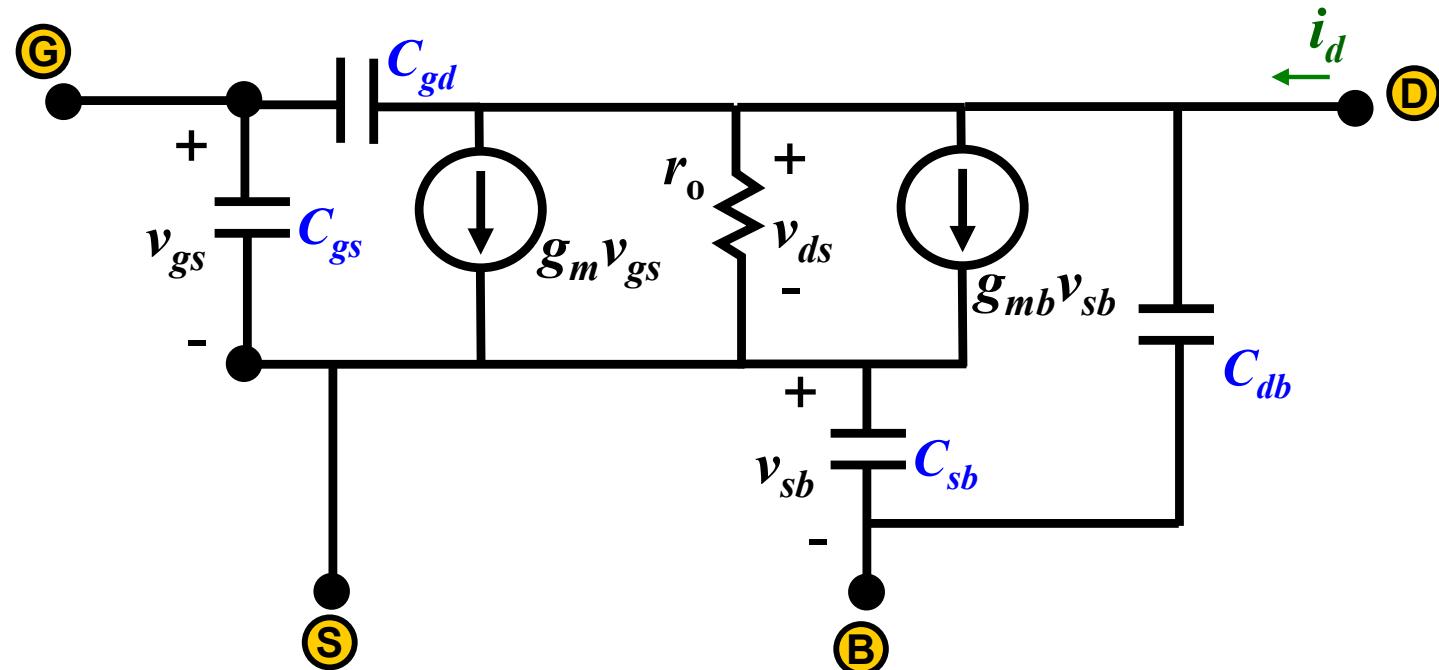
- There are charges stored in MOSFETs, and capacitances are associated with the charge storage mechanism.
- When terminal voltages change, the amount of charge stored changes.
- For studying frequency response, and for design of circuit operating at high frequencies, capacitances have to be included, e.g., C_{gs} and C_{gd} .



MOSFET - Full Hybrid- π Model at High Frequency

We introduce the existence of these capacitances here, and their inclusion in the Hybrid- π Model is necessary when frequency response is discussed. We will ignore these capacitances for low frequency signals.

High-Frequency Hybrid- π Model for MOSFET



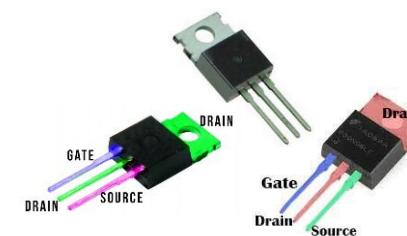
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References

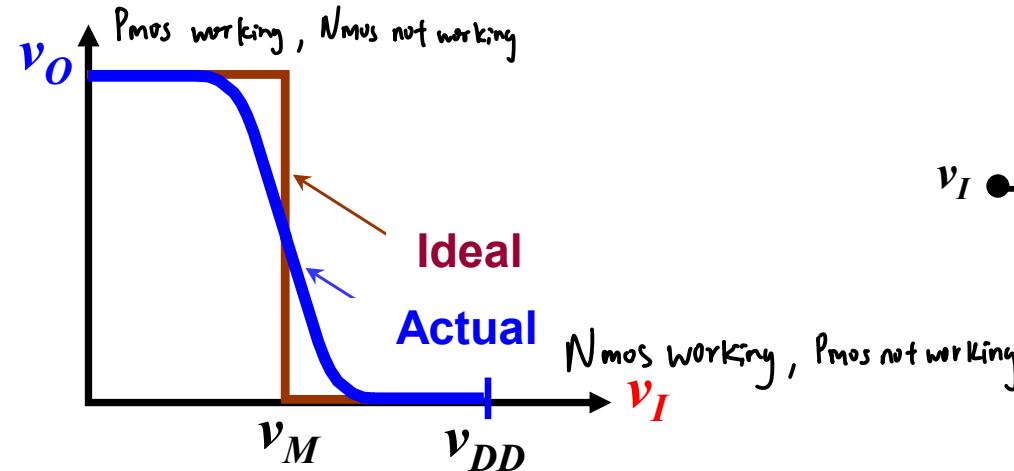
- Sedra and Smith, Microelectronic Circuits, Theory and Applications, Fifth Edition (International Version), Oxford (2004), pp. 325 – 349, pp. 426-429, pp. 901-921.



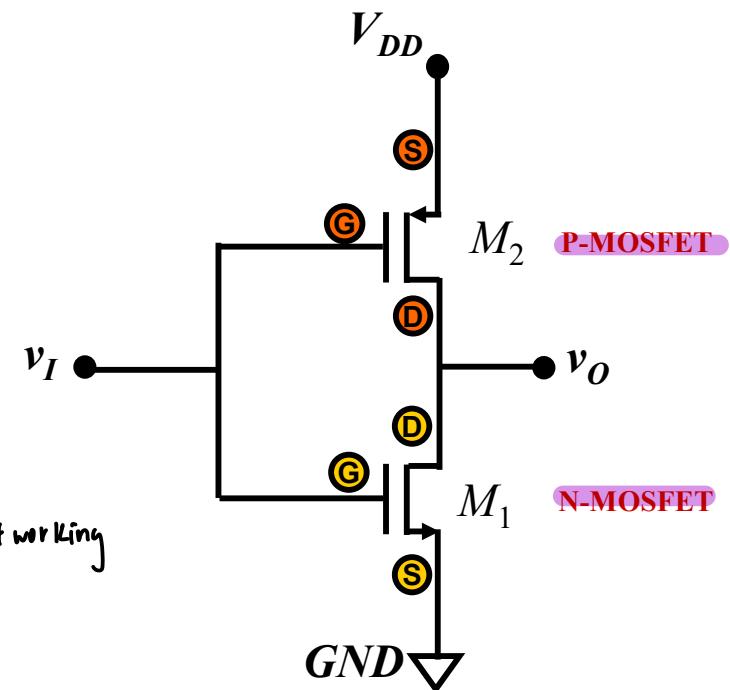
MOSFET – CMOS Inverter (Circuit Structure)

- Logic inverter is the simplest and basic circuit element in digital circuit design.
- CMOS inverter consists of a pair of N-MOSFET and P-MOSFET that operate in a complementary fashion by the input voltage, v_I . For a given v_I , either N-MOSFET or P-MOSFET is turned on, while the other is turned off.
- The source of each MOSFET is connected to its body (not shown in the following circuit). Hence, the body effect is eliminated.
- Inverter transfer characteristics:

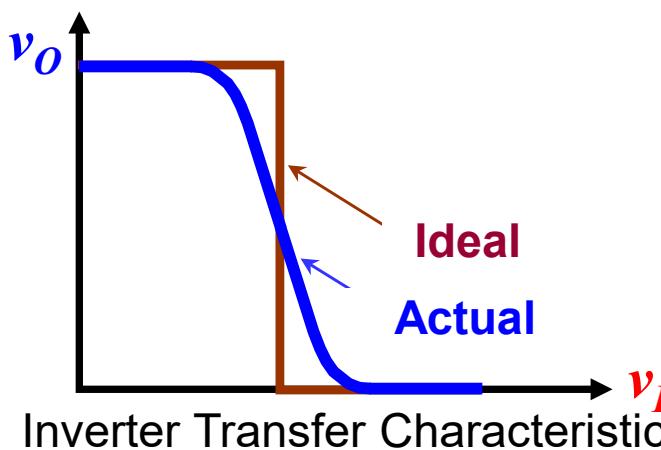
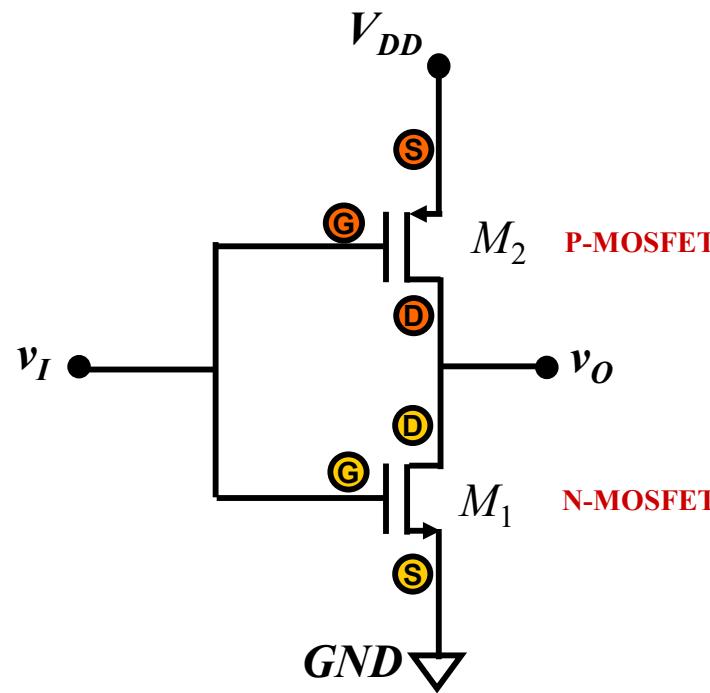
- $v_I < v_M$, v_o is a high voltage
- $v_I > v_M$, v_o is a low voltage



Inverter Transfer Characteristic



MOSFET – Symmetrical CMOS Inverter



- When the N-MOSFET and P-MOSFET are matched, a symmetrical transfer characteristic is obtained, and the following is true of the device parameters.
- The magnitudes of the threshold voltages are the same:

$$V_{THN} = |V_{THP}| = V_{TH}$$

V_{THP} (threshold voltage of the P-MOSFET) is negative
 V_{THN} (threshold voltage of N-MOSFET) is positive

- The values of conductance parameters are the same:

$$K_n = K_p = K$$

- Above conditions also means equal current driving capabilities in both N-MOSFET and P-MOSFET.
- We also assume that V_{TH} is less than $V_{DD}/2$.

MOSFET – Symmetrical CMOS Inverter

- To have a symmetrical inverter transfer characteristic, the devices are designed to have equal K_n and K_p , where

$$K_n = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_n$$

Electron mobility in the channel in N-MOSFET

$$K_p = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L} \right)_p$$

Ratio of gate width to gate length (also known as sizing) for N-MOSFET

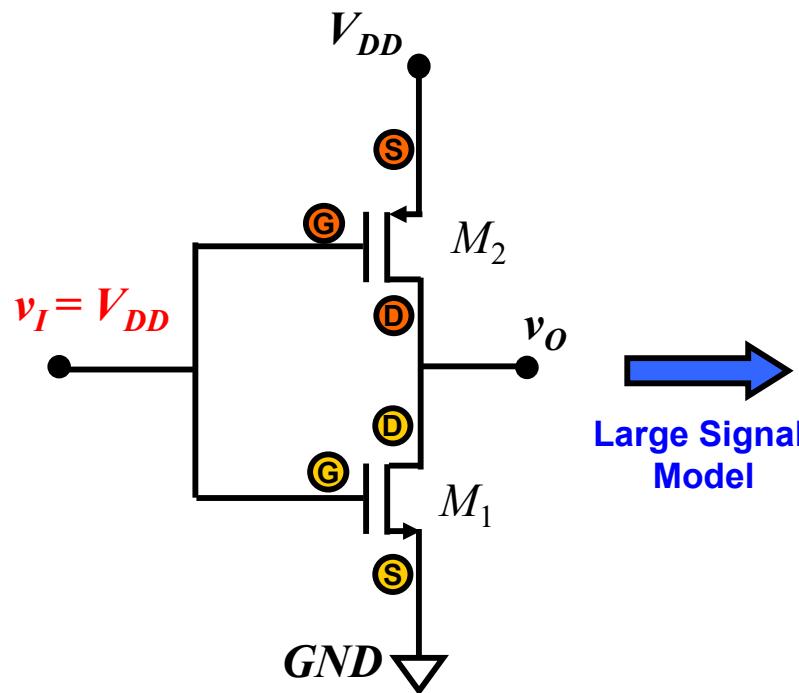
- The electron mobility in the channel, μ_n , of in the N-MOSFET is larger than the hole mobility in the channel, μ_p , in the P-MOSFET. The ratio $(\mu_n/\mu_p) \approx 2.5$.
- Therefore, to have $K_n = K_p$, the sizings of the transistors are such that:

$$\left(\frac{W}{L} \right)_p = \frac{\mu_n}{\mu_p} \left(\frac{W}{L} \right)_n$$

- Usually, the N- and P-MOSFETs have the same gate length L , and the P-MOSFET is designed to have a 2.5 times larger width than the N-MOSFET.

Why do we prefer a symmetrical inverter?

MOSFET – CMOS Inverter Operation (Input High)

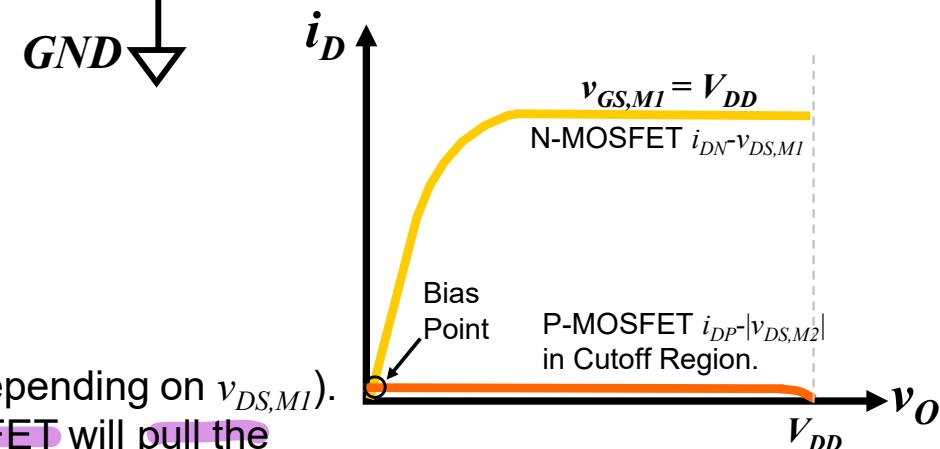
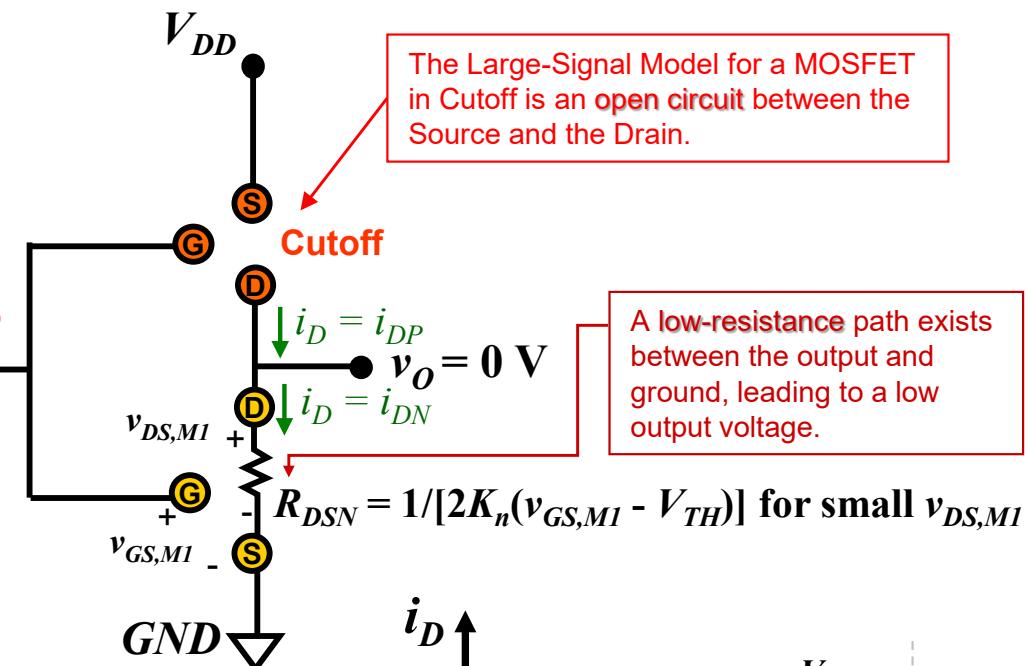


When $v_I = V_{DD}$,

- For P-MOSFET: $|v_{GS,M2}| = 0$, and $|v_{GS,M2}| < |V_{THP}| = V_{TH}$.
P-MOSFET is in the **Cutoff** region.
- For N-MOSFET: $v_{GS,M1} = V_{DD} > V_{TH}$.
N-MOSFET is either in **Linear** or **Saturation** region (depending on $v_{DS,M1}$).
If there is **no current i_D in the steady-state**, the N-MOSFET will pull the output voltage all the way down to **0 V**, and it will be in the **Linear** region.
- N-MOSFET pulls the output down to 0V (**Pull-down Network, PDN**)

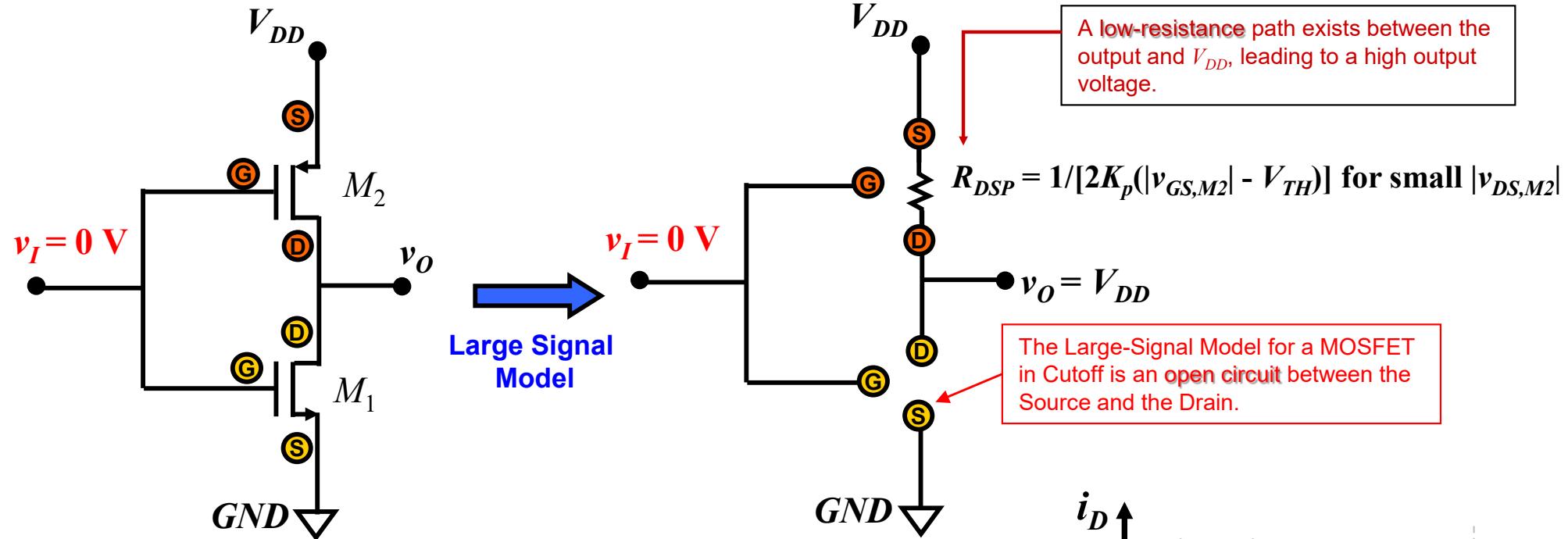
Note:

- In logic, only large-signal model is applied for transistor analysis.
- In amplifier, large-signal model is applied for DC analysis whereas small-signal model is applied for AC analysis.



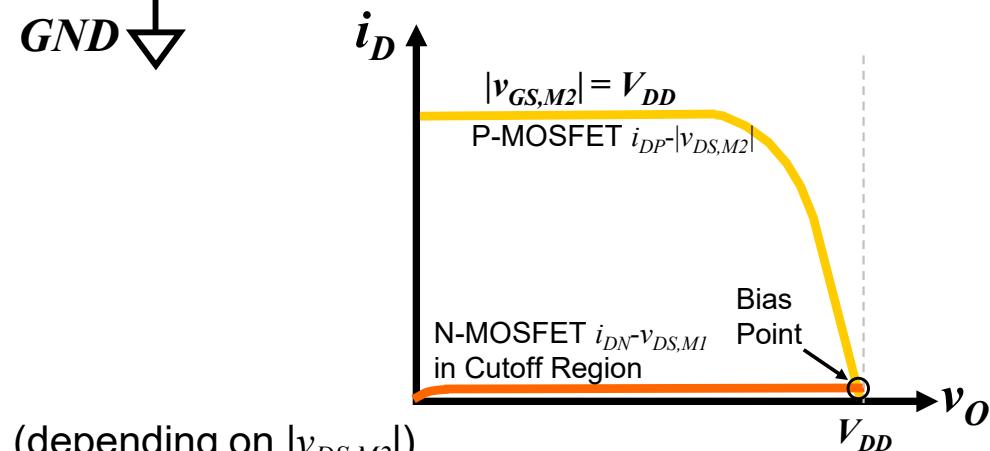
$$v_O = v_{DS,M1}$$

MOSFET – CMOS Inverter Operation (Input Low)



When $v_I = 0 \text{ V}$,

- For N-MOSFET: $|v_{GS,M1}| = 0$, and $|v_{GS,M1}| < V_{THN} = V_{TH}$.
N-MOSFET is in the **Cutoff** region.
- For P-MOSFET: $|v_{GS,M2}| = V_{DD} > V_{TH}$.
P-MOSFET is either in **Linear** or **Saturation** region (depending on $|v_{DS,M2}|$).
If there is no current i_D in the **steady-state**, the P-MOSFET will pull the output voltage all the way up to V_{DD} , and it will be in the **Linear** region.
- P-MOSFET pulls the output up to V_{DD} (**Pull-up Network, PUN**)



$$v_O = V_{DD} - v_{SD,M2}$$

MOSFET – CMOS Inverter Propagation Delay

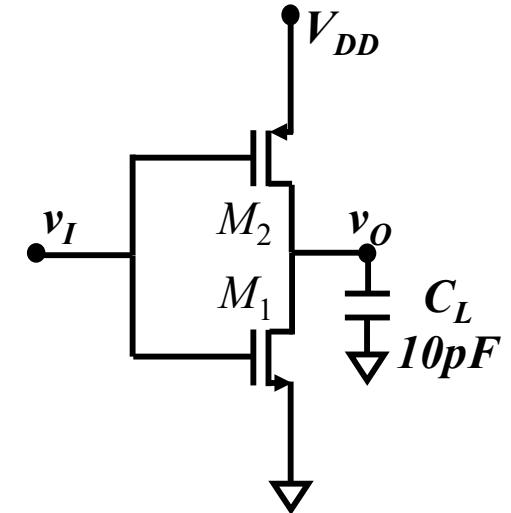
- Derived based on capacitor current. Assuming NMOS discharging current for t_{pHL} :

$$i_{DN} = C_L \frac{dv_o}{dt} = \begin{cases} K_n (V_{GS,M1} - V_{THN})^2 & \text{for saturation} \\ 2K_n \left[(V_{GS,M1} - V_{THN})V_{DS,M1} - \frac{V_{DS,M1}^2}{2} \right] & \text{for linear} \end{cases}$$

$$t_{pHL} = \sum dt = \sum \frac{C_L dv_o}{i_{DN}} \propto \frac{C_L}{K_n} \propto \frac{C_L}{\mu_n \left(\frac{W}{L} \right)_N}$$

Directly proportional to C_L , but
 inversely proportional to mobility
 μ_n and NMOS sizing (W/L)_N

propagation
 from high to low



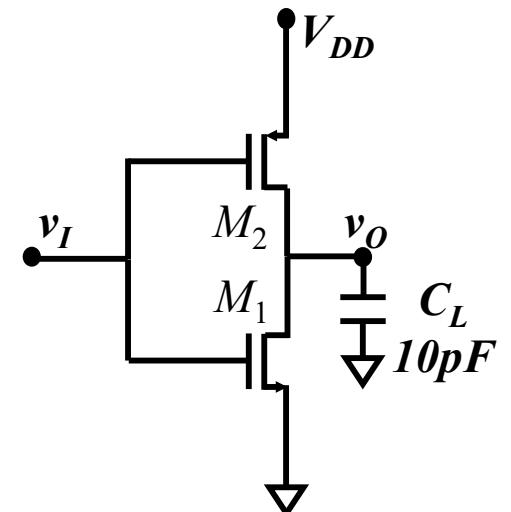
- Derived based on capacitor current. Assuming PMOS charging current for t_{pLH} :

$$i_{DP} = C_L \frac{dv_o}{dt} = \begin{cases} K_p (|V_{GS,M2}| - |V_{THP}|)^2 & \text{for saturation} \\ 2K_p \left[(|V_{GS,M2}| - |V_{THP}|)V_{DS,M2} - \frac{V_{DS,M2}^2}{2} \right] & \text{for linear} \end{cases}$$

$$t_{pLH} = \sum dt = \sum \frac{C_L dv_o}{i_{DP}} \propto \frac{C_L}{K_p} \propto \frac{C_L}{\mu_p \left(\frac{W}{L} \right)_P}$$

Directly proportional to C_L , but
 inversely proportional to mobility
 μ_p and PMOS sizing (W/L)_P

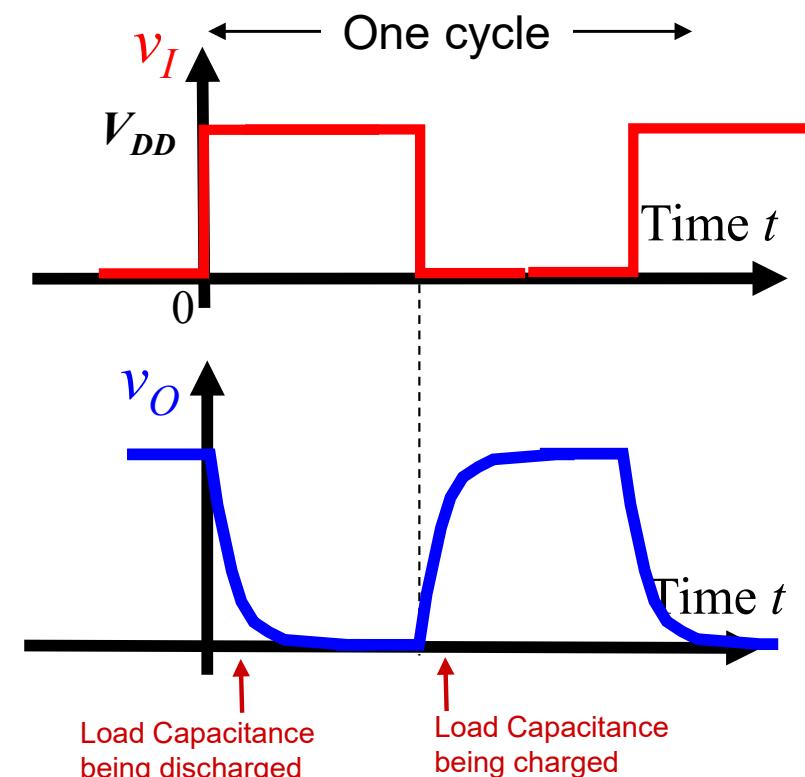
propagation
 from low to high



MOSFET – CMOS Inverter Dynamic Power Dissipation

- One advantage of CMOS logic is that power is only consumed during switching. **Very little power consumed during the static mode** (i.e., static power dissipation ~ 0), only due to leakage. (Note: Leakage power can be significant for advanced technology with trillion transistors)
- Consider v_I as being a periodic square wave with frequency f .
- At time = 0^- , $v_O = V_{DD}$, and the energy stored on the capacitor is $(C_L V_{DD})^2/2$.
- When v_I goes to high at $t = 0$, the N-MOSFET discharges the capacitor. The energy $(C_L V_{DD})^2/2$ is removed from C_L and dissipated by the N-MOSFET.
- In the other half-cycle, v_I goes to zero, and the P-MOSFET charges C_L so that v_O goes from zero to V_{DD} .
- During this charging process, $(C_L V_{DD})^2/2$ is dissipated in the P-MOSFET.
- The **total energy dissipated per cycle** is $C_L V_{DD}^2$.
- There are f cycles per second, and the **energy dissipated per second** is $f C_L V_{DD}^2$.

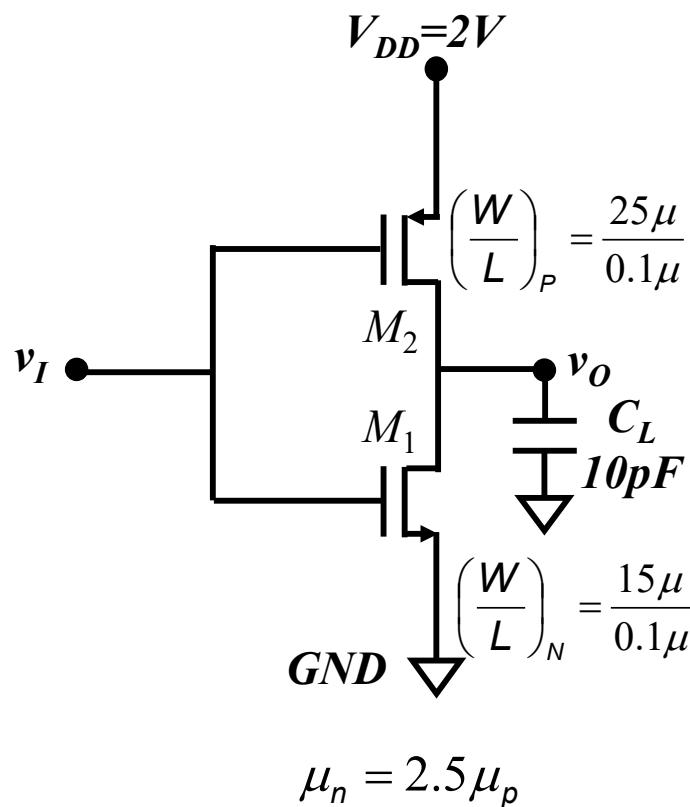
$$\text{Dynamic Power Dissipation} = f C_L V_{DD}^2$$



A larger V_{DD} would lead to a larger Dynamic Power Dissipation

***** MOSFET – CMOS Inverter (Work Example)

- Estimate the ratio of t_{pHL} and t_{pLH} , and dynamic power dissipation with input frequency of 100 MHz.



- Applying slide MOSFET-62 for propagation delay,

$$\frac{t_{pHL}}{t_{pLH}} = \frac{\frac{1}{\mu_n \left(\frac{W}{L}\right)_N}}{\frac{1}{\mu_p \left(\frac{W}{L}\right)_P}} = \frac{\mu_p \left(\frac{25}{0.1}\right)}{\mu_n \left(\frac{15}{0.1}\right)} = 0.67$$

- Applying slide MOSFET-63 for dynamic power,

$$\begin{aligned} Power &= f \times C_L \times V_{DD}^2 \\ &= 100MHz \times 10pF \times 2^2 \\ &= 4mW \end{aligned}$$

Is CMOS inverter symmetrical? → no, falltime faster than risetime in this case

MOSFET – CMOS Inverter's Power-Delay Product

- From slide MOSFET-62, propagation delay,

- $t_p \propto \frac{C_L}{W/L} \propto \frac{W_1 L}{W_2/L} \propto \frac{W_1}{W_2} L^2$

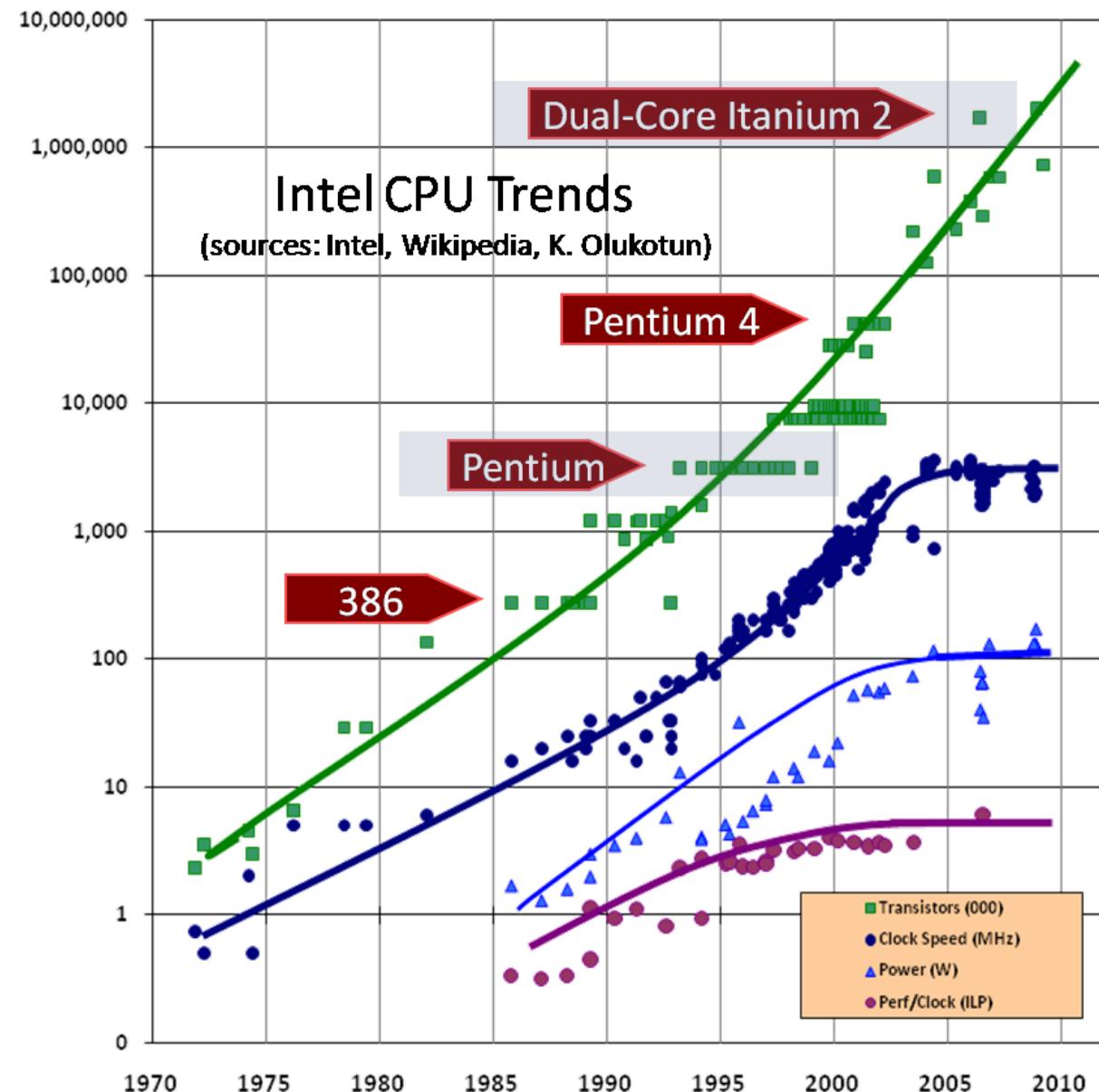
- From slide MOSFET-63, dynamic power dissipation,

- $P_d = f C_L V_{DD}^2 \propto C_L \propto W_1 L$

- Power-Delay Product (PDP), $P_d t_p \propto \frac{W_1^2}{W_2} L^3 \nearrow \text{channel length}$

- PDP is a constant for a particular technology node (as specified by the gate length, L)
- For the same technology node, there is a trade-off between P_d and t_p .
- As technology advances, L decreases, leading to a lower PDP

CPU Trend



A. P. Chandrakasan, A. Burstein, and R. W. Brodersen, "A low-power chipset for a portable multimedia applications," ISSCC Dig. Tech. Papers, pp. 82-83, Feb. 1994.

MOSFET – CMOS Logic Gates (Basic Features)

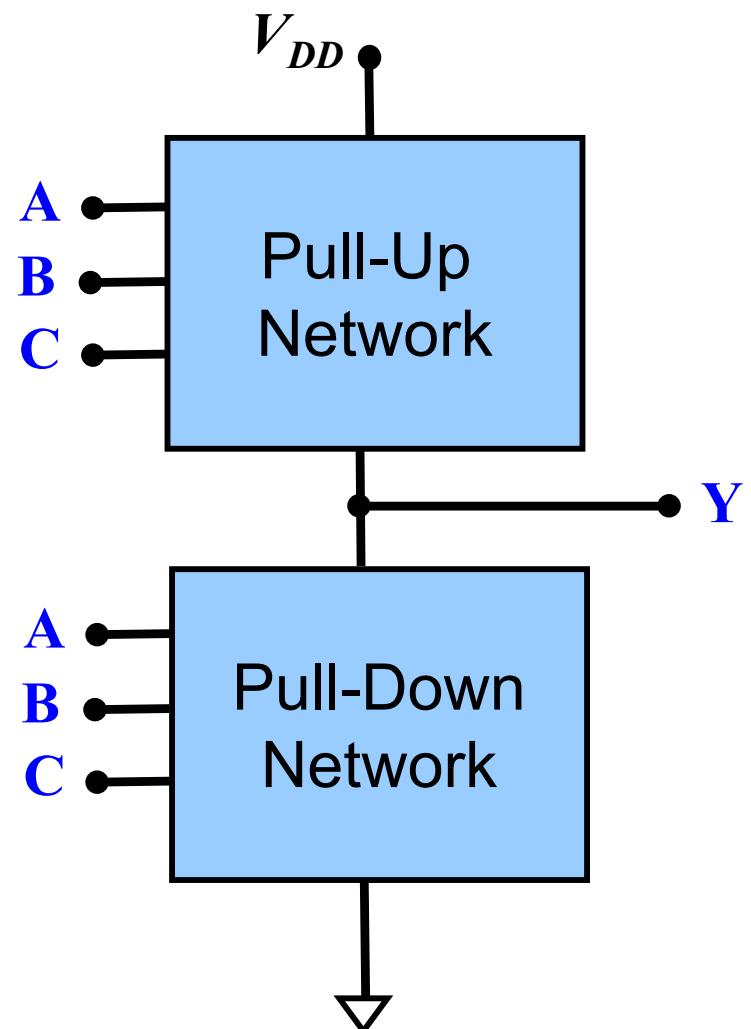
A CMOS Logic Gate Circuit is an **extension** or **generalization** of the CMOS inverter. It consists of 2 networks:

- **Pull-Up Network (PUN)** comprising multiple PMOS transistors.
- **Pull-Down Network (PDN)** comprising multiple NMOS transistors.

The Pull-Up Network (PUN) and the Pull-Down Network (PDN) are controlled by multiple input variables (e.g., A, B, C) in a complementary fashion.

PUN and PDN are **Complementary**, i.e., for a given combination of input variables, either PUN is turned on and pull the output voltage up to V_{DD} or PDN is turned on and pull the output voltage down to ground. When PUN is turned on, PDN is turned off, and vice versa.

An Example of a 3-input Logic Gate.



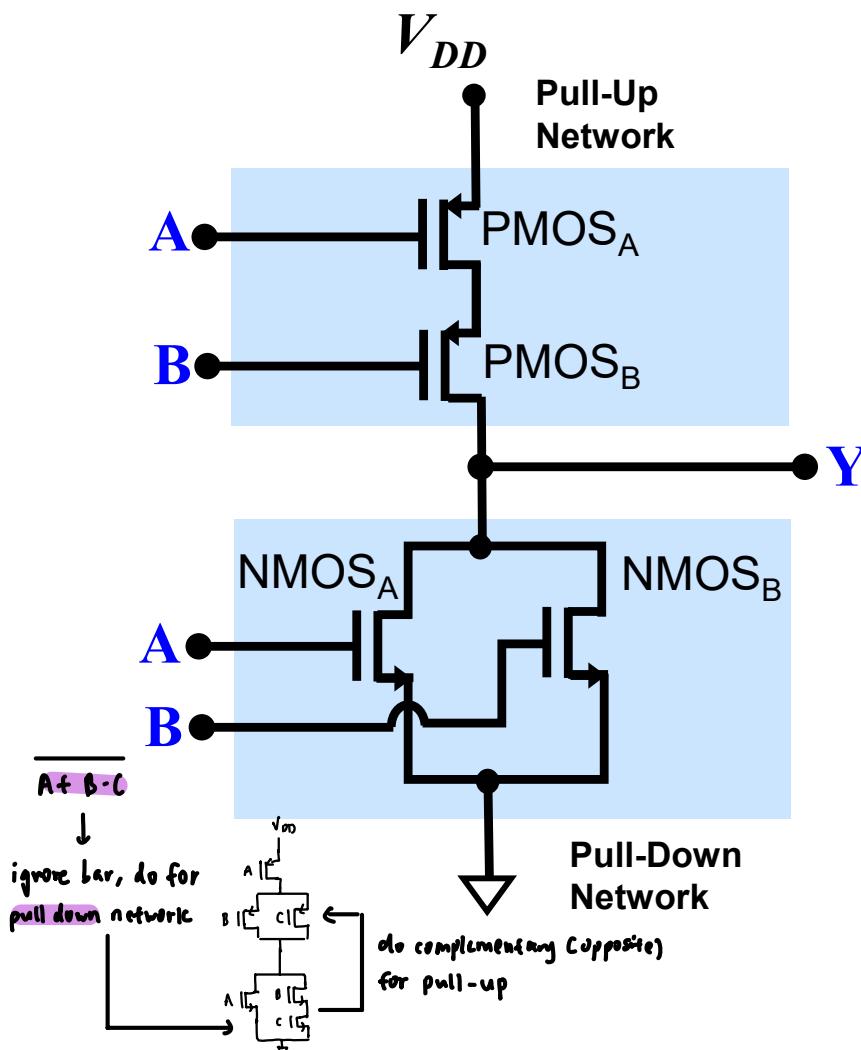
MOSFET – CMOS Logic Gates (An Example)

Consider a CMOS logic gate that realizes the two-input NOR function:

$$Y = \overline{A + B} = \overline{A} \cdot \overline{B}$$

↓ ↓
0 0

The implementation is as follows:



Note: DeMorgan's Law for Boolean algebra:

$$\overline{A + B + C} = \overline{A} \cdot \overline{B} \cdot \overline{C}$$

[+ is parallel, • in series]

- PUN has 2 PMOS transistors
- PDN has 2 NMOS transistors
- PUN and PDN are controlled by input variables A and B in complementary fashion

Y is high (PUN conducting) when A is low and B is low. At the same time, PDN does not conduct.

Since both (and) have to be low, it is connected in series

Y is low (PDN conducting) when either A is high or B is high, or both A and B are high. At the same time, PUN does not conduct.

since either, that's why it is in parallel

There are no combinations of A and B where the PUN and the PDN are both conductive or both non-conductive. The PDN and PUN are complementary, one of them is conductive, and the other is non-conductive.

MOSFET – Topics Discussed

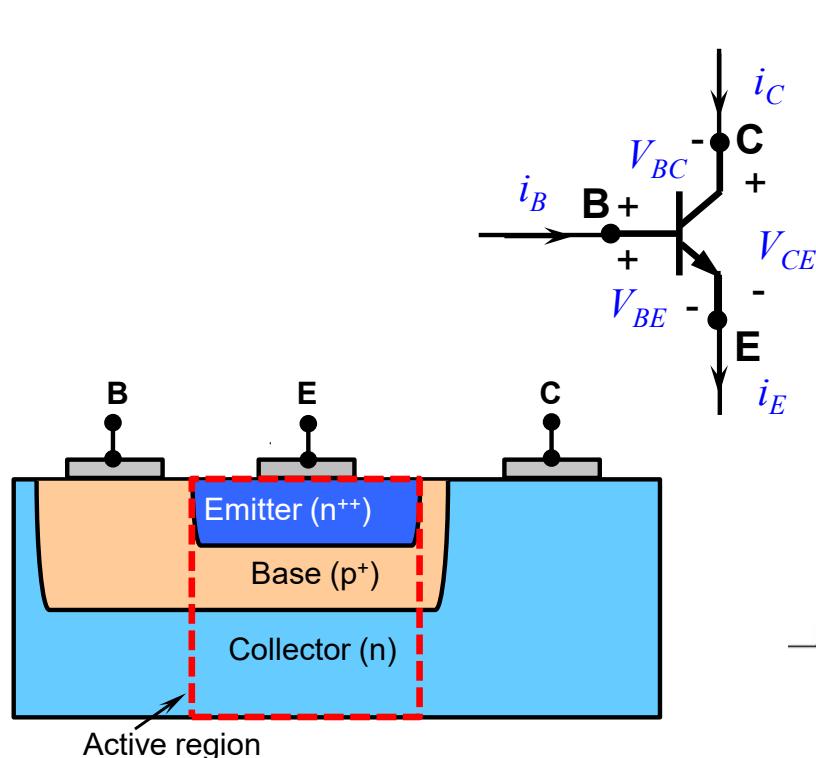
- Structure (4 terminals versus 3 terminals operation)
- Operation regions: Saturation, linear, cut-off
- i_D - v_{DS} curves
- n-channel MOSFET IV characteristic:
 - Linear region: $i_D = 2K_n \left[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2 \right]$
 - Saturation region:
 - (i) No Channel-Length Modulation - $i_D = K_n(v_{GS} - V_{TH})^2$
(Known as Square law)
 - (ii) With Channel-Length Modulation - $i_D = K_n(v_{GS} - V_{TH})^2(1 + \lambda v_{DS})$
- n-channel vs p-channel MOSFET (Structure and IV characteristics)
- Body Effect (Body not shorted to Source)

MOSFET – Topics Discussed (Cont.)

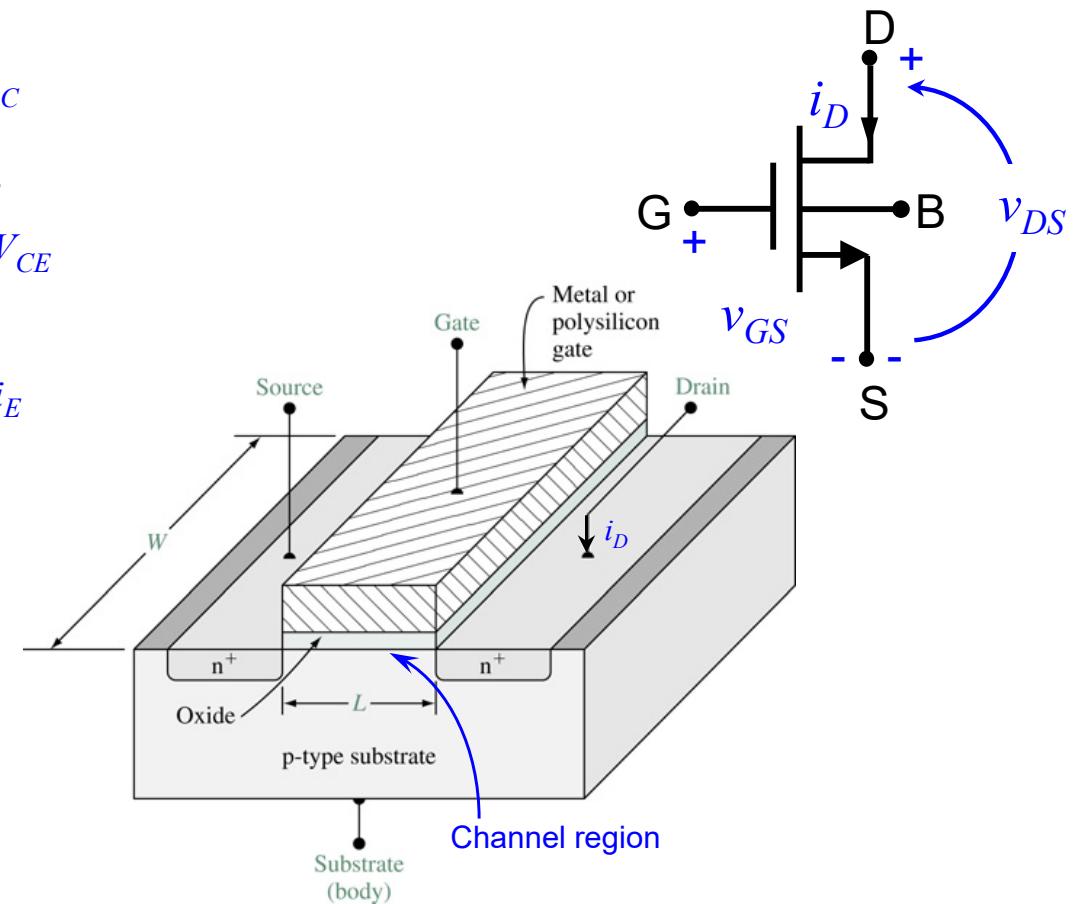
- Large-signal models (saturation & linear) & dc large-signal analysis
- Saturation region small-signal model (g_m , r_o , g_{mb}):
 - $g_m = 2\sqrt{K_n I_D} = 2K_n(V_{GS} - V_{TH}) = 2I_D/(V_{GS} - V_{TH})$
 - $r_o = \frac{1}{\lambda I_D}$ (with Channel-Length Modulation Effect)
 - $g_{mb} < 0$ (with Body Effect)
- CMOS Inverter: operation, symmetrical inverter, propagation delays (t_{pHL} versus t_{pLH}), static versus dynamic power dissipation, logic gates

APPENDICES

Appendix A: MOSFET vs BJT



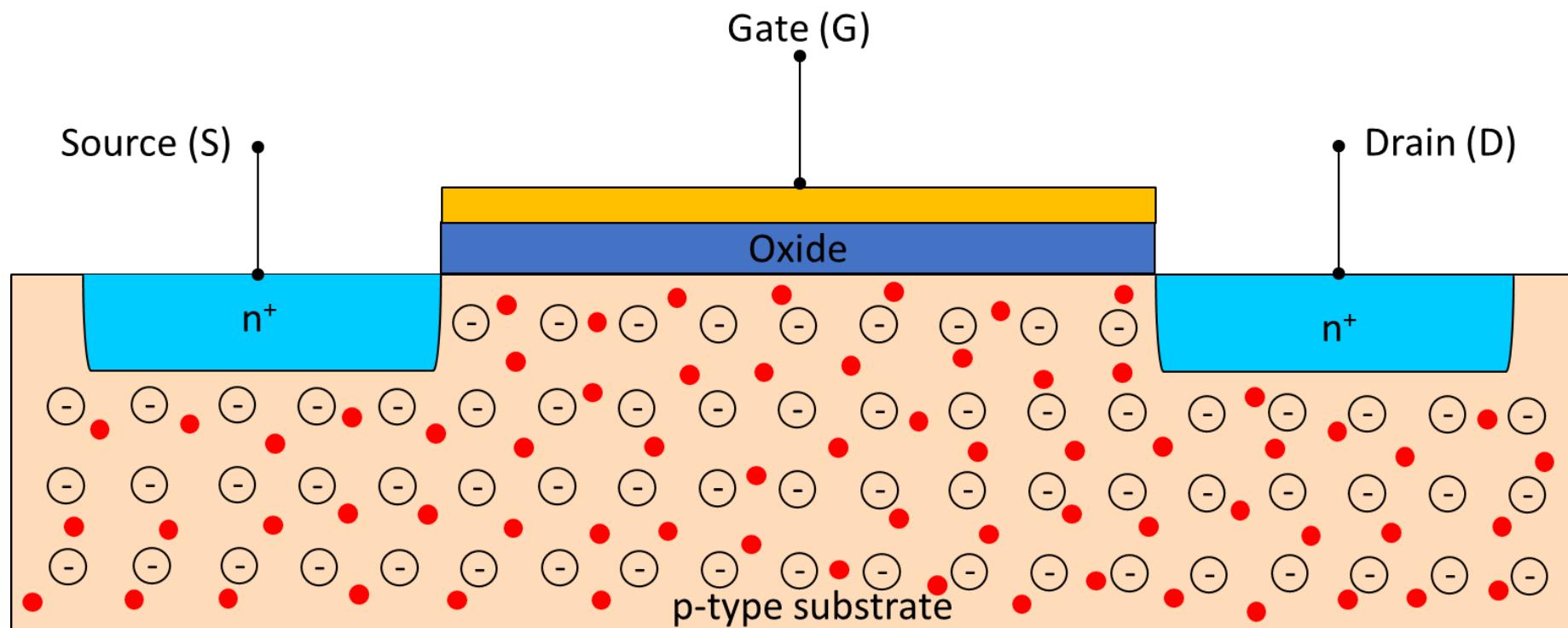
Basic structure of an npn BJT.



Basic structure of an n-channel MOSFET.

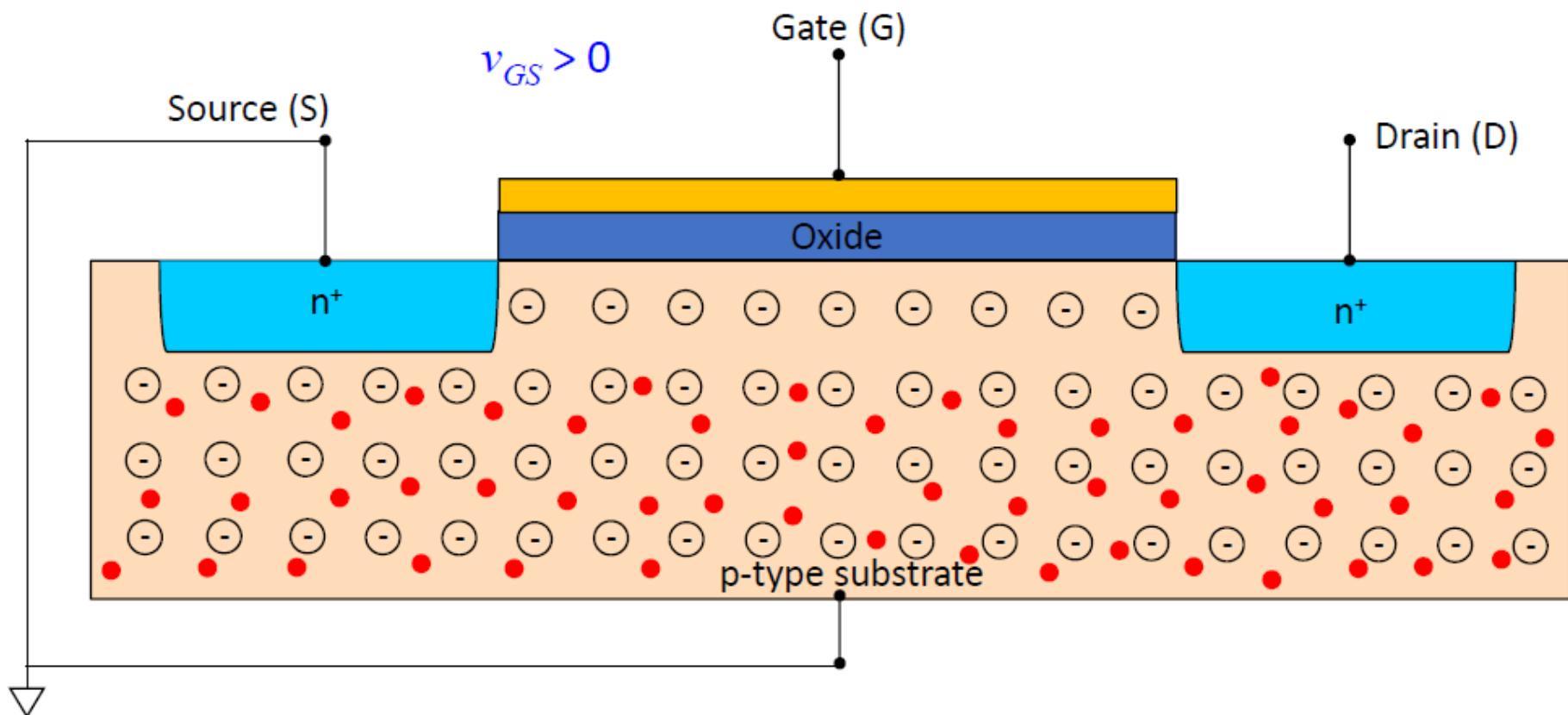
Appendix B – p-type Semiconductor

A p-type semiconductor is electrically neutral with many positively charged holes (•), and many negatively charged p-type impurity ions (⊖)



Appendix C – p-type Semiconductor with $v_{GS} > 0$

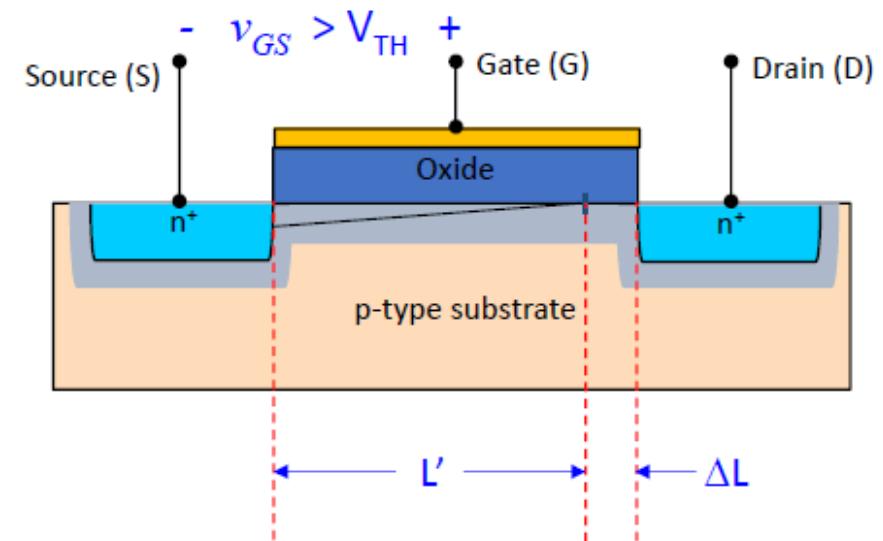
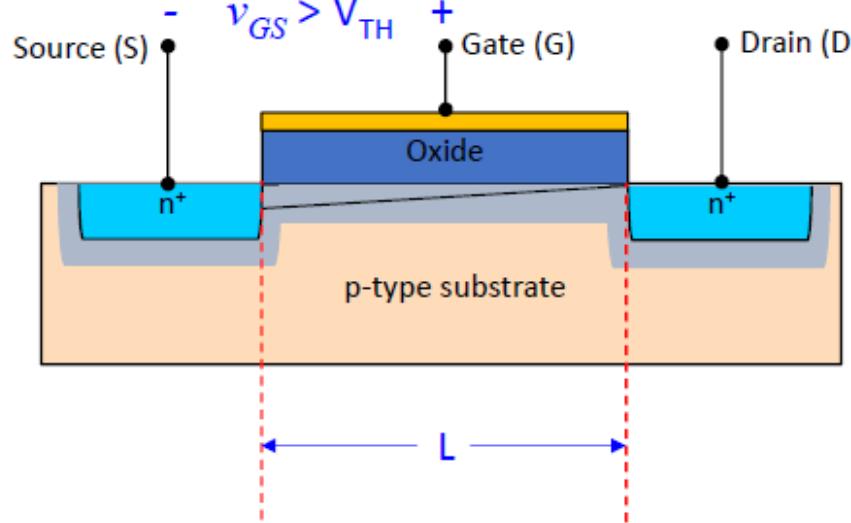
With $v_{GS} > 0$ applied, the positive voltage at the gate repels holes (•) in the *p*-type substrate from the region below the gate (the channel region), leaving behind fixed ionised *p*-type impurities (○) near the surface of the substrate, forming a depletion region.



Appendix D - Long Channel Length

$$v_{DS} = v_{GS} - V_{TH}$$

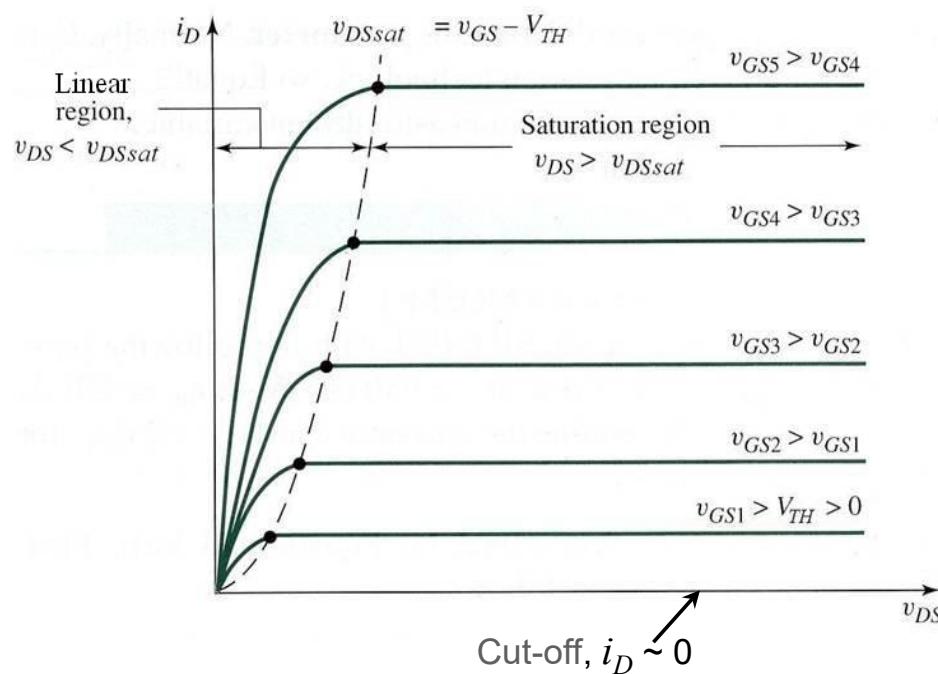
$$v_{DS} > v_{GS} - V_{TH}$$



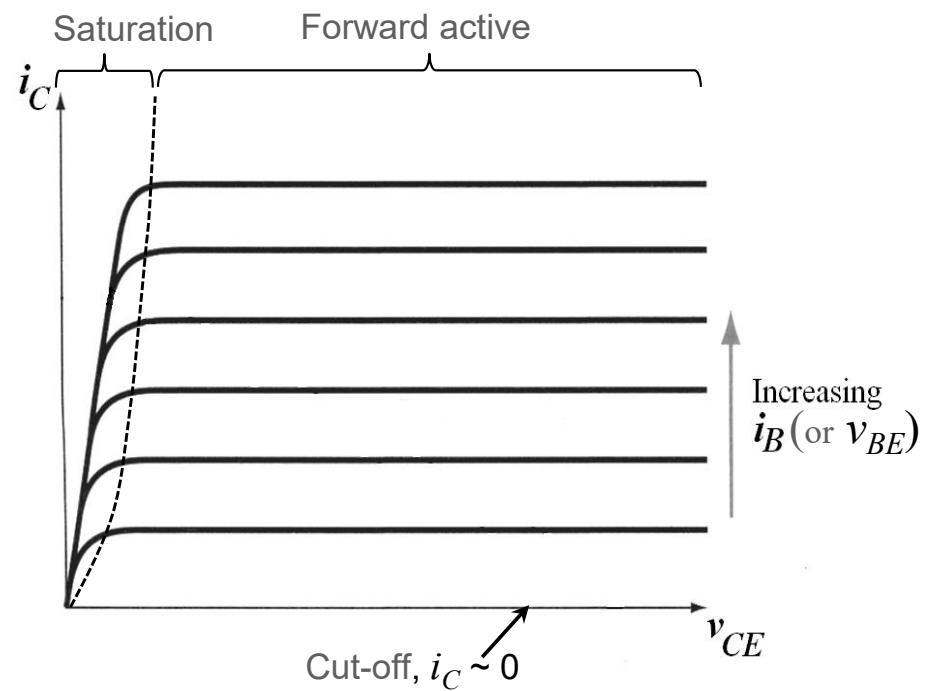
Assumption of long channel length –
 $L \gg \Delta L$, meaning $L \approx L'$.

Appendix E - MOSFET Versus BJT

Comparison of MOSFET and BJT i - v characteristics

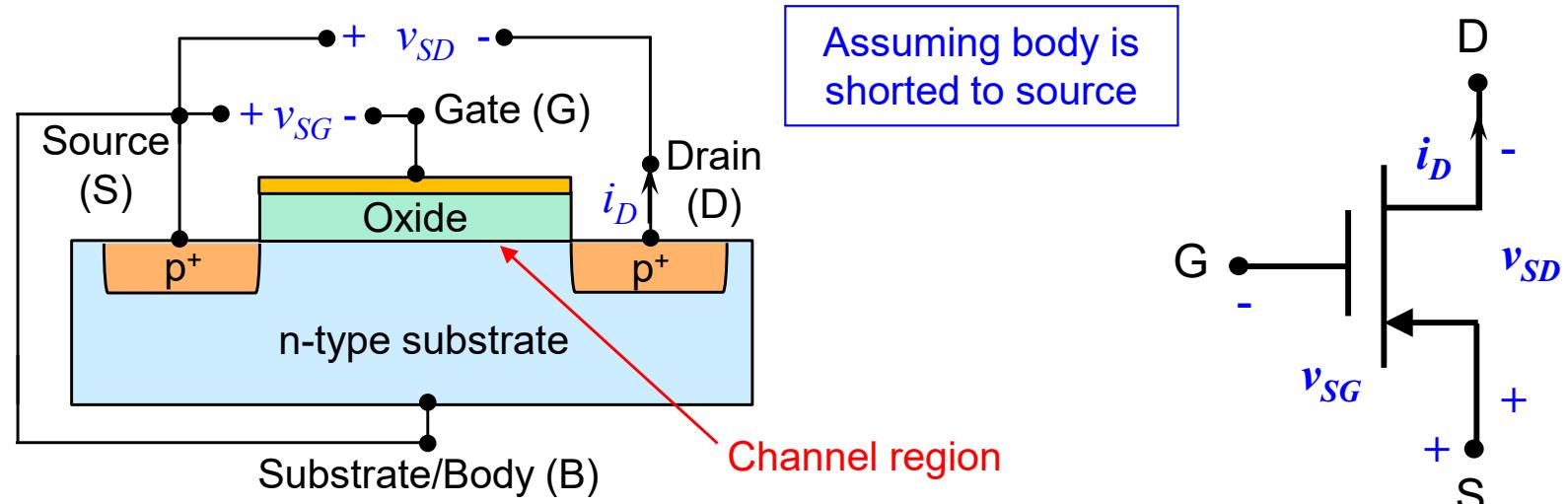


MOSFET i_D - v_{DS} characteristics for different v_{GS} .



BJT i_C - v_{CE} characteristics for different i_B (or v_{BE}).

Appendix F – Modes of Operation (p-MOSFET)

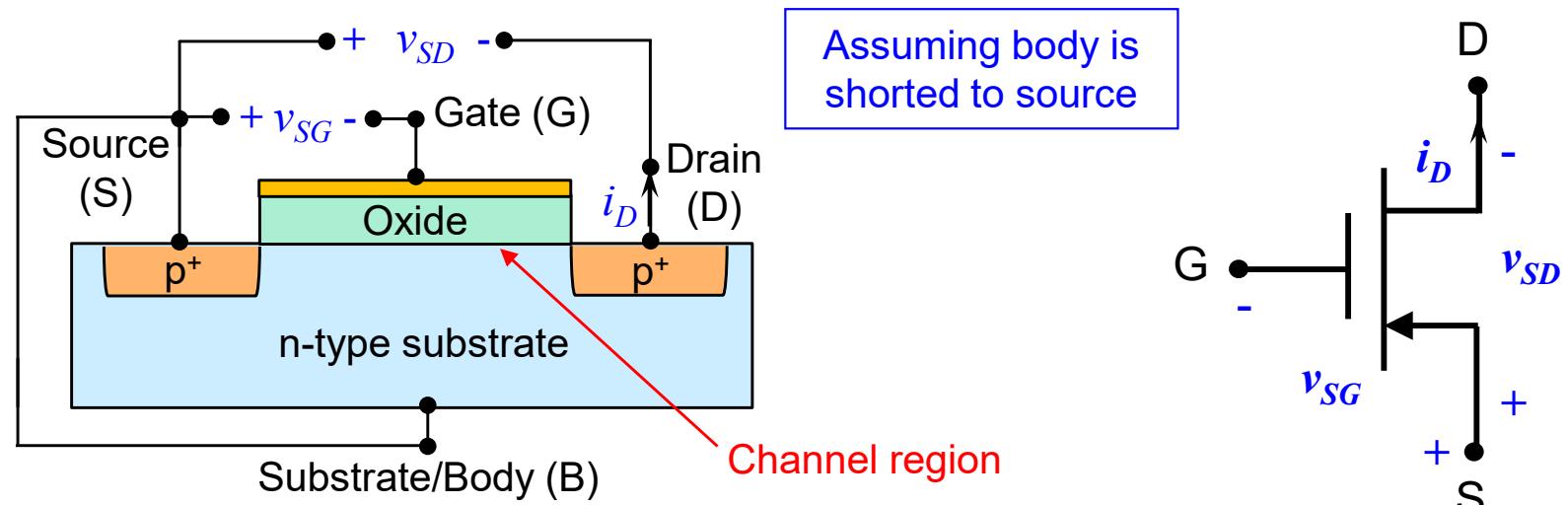


Modes of operation of the p-channel MOSFET

Mode of Operation	Gate-to-Source Bias ($v_{SG} > 0$)	Drain-to-Source Bias ($v_{SD} > 0$)	Drain Current (i_D - out of Drain)	Applications
Cut-off	$v_{SG} < V_{TH} ^*$	N.A.	$i_D = 0$	CMOS Logic – OFF state
Linear	$v_{SG} \geq V_{TH} $	$v_{SD} \leq v_{SG} - V_{TH} $	$i_D = f(v_{SD}, v_{SG})$	CMOS Logic – ON state
Saturation	$v_{SG} \geq V_{TH} $	$v_{SD} \geq v_{SG} - V_{TH} $	$i_D = f(v_{SG})$	Amplifier

* For p-channel MOSFET, $V_{TH} < 0$.

Appendix G – Modes of Operation (p-MOSFET)



- Take note that in an *n*-type semiconductor, there are many electrons (**negatively charge carriers**) and they are mainly contributed by *n*-type impurities that have become ionized. The ionized *n*-type impurities are fixed **positive** charges that neutralize the negatively charged electrons, thus making the *n*-type semiconductor overall **electrically neutral**.
- When $v_{SG} > |V_{TH}|$ is applied, a channel of holes is formed at the surface of the *n*-type substrate, connecting the *p*⁺-source and *p*⁺-drain regions and allowing holes to flow from source to drain. Drain current, i_D , flows out of the drain terminal.

Appendix H – Non-Ideal i_D -Expression

- With Channel-Length Modulation effect, the drain current i_D in saturation region is a function of both v_{GS} and v_{DS} , as seen in equation (4.17) -

$$i_D = f(v_{GS}, v_{DS}) \quad (\text{C.1})$$

- We can express the total instantaneous currents and voltages in terms of the dc (operating point) and ac (signal) currents and voltages, that is

- $i_D = I_D + i_d$
- $v_{GS} = V_{GS} + v_{gs}$
- $v_{DS} = V_{DS} + v_{ds}$

- Hence, $i_D = I_D + i_d = f(v_{GS}, v_{DS}) = f(V_{GS} + v_{gs}, V_{DS} + v_{ds}) \quad (\text{C.2})$

- Expand equation (C.2) as a Taylor series and neglecting higher order terms for small v_{gs} and v_{ds} -

$$\begin{aligned} i_D &= I_D + i_d = f(V_{GS} + v_{gs}, V_{DS} + v_{ds}) \\ &\approx f(V_{GS}, V_{DS}) + \frac{\partial i_D}{\partial v_{GS}}|_{V_{GS}} \times v_{gs} + \frac{\partial i_D}{\partial v_{DS}}|_{V_{DS}} \times v_{ds} \end{aligned}$$

- As $I_D = f(V_{GS}, V_{DS})$, small signal drain current

$$i_d \approx \frac{\partial i_D}{\partial v_{GS}}|_{V_{GS}} \times v_{gs} + \frac{\partial i_D}{\partial v_{DS}}|_{V_{DS}} \times v_{ds}. \quad (\text{C.3})$$