RS-232 TRANSCEIVER WITH SPLIT SUPPLY PIN FOR LOGIC SIDE

Check for Samples: TRS3253E-EP

FEATURES

- **V_L Pin for Compatibility With Mixed-Voltage Systems Down to 1.8 V on Logic Side**
- **Enhanced ESD Protection on RIN Inputs and DOUT Outputs**
  - **±8 kV IEC 61000-4-2 Air-Gap Discharge**
  - **±8 kV IEC 61000-4-2 Contact Discharge**
  - **±15 kV Human-Body Model**
- **Low 300-µA Supply Current**
- **Specified 1000-kbps Data Rate**
- **Auto Powerdown Plus Feature**

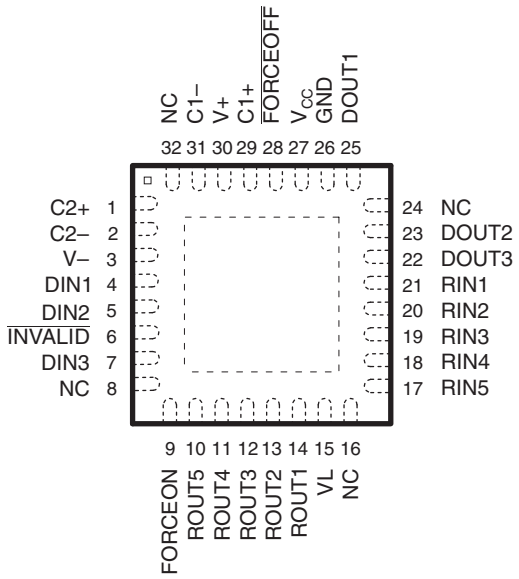
APPLICATIONS

- **Hand-Held Equipment**
- **PDAs**
- **Cell Phones**
- **Battery-Powered Equipment**
- **Data Cables**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C to 125°C) Temperature Range**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

RSM PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION

The TRS3253E is a three-driver and five-receiver RS-232 interface device, with split supply pins for mixed-signal operations. All RS-232 inputs and outputs are protected to ±8 kV using the IEC 61000-4-2 Air-Gap Discharge method, ±8 kV using the IEC 61000-4-2 Contact Discharge method, and ±15 kV using the Human-Body Model.

The charge pump requires only four small 0.1-µF capacitors for operation from a 3.3-V supply. The TRS3253E is capable of running at data rates up to 1000 kbps, while maintaining RS-232-compliant output levels.

The TRS3253E has a unique V_L pin that allows operation in mixed-logic voltage systems. Both driver in (DIN) and receiver out (ROUT) logic levels are pin programmable through the V_L pin. This eliminates the need for additional voltage level shifter while interfacing with low-voltage microcontroller or UARTs. The TRS3253E is available in a space-saving QFN package (4 mm × 4 mm RSM).

DESCRIPTION (CONTINUED)

Auto-powerdown plus can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-powerdown plus enabled, the device activates automatically when a valid signal is applied to any receiver or driver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V, or has been between –0.3 V and 0.3 V for less than 30 µs. INVALID is low (invalid data) if all receiver input voltages are between –0.3 V and 0.3 V for more than 30 µs. Refer to Figure 6 for receiver input levels.

ORDERING INFORMATION(1)

T_J	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	QFN - RSM	TRS3253EMRSMREP	RS53EP	V62/13621-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

Each Driver(1)

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown plus disabled
H	H	H	X	L	
L	L	H	<30 µs	H	Normal operation with auto-powerdown plus enabled
H	L	H	<30 µs	L	
L	L	H	>30 µs	Z	Powered off by auto-powerdown plus feature
H	L	H	>30 µs	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

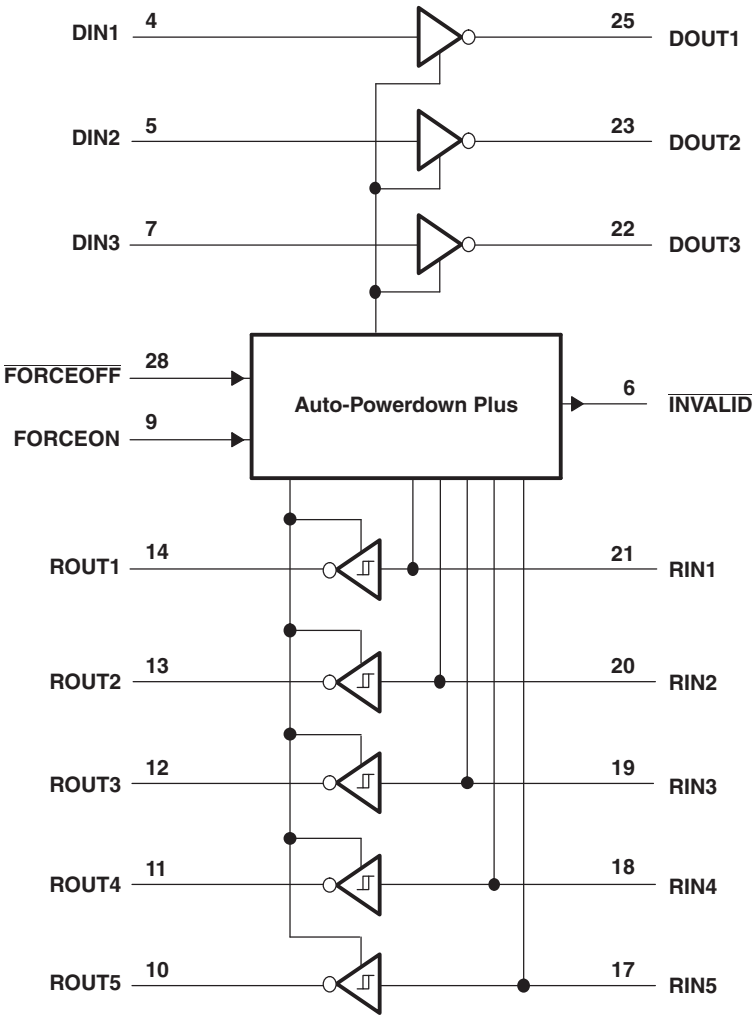
Each Receiver(1)

INPUTS			OUTPUTS	RECEIVER STATUS
RIN1–RIN5	$\overline{\text{FORCEOFF}}$	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION	ROUT1-ROUT5	
X	L	X	Z	Powered off
L	H	<30 µs	H	Normal operation with auto-powerdown plus disabled/enabled
H	H	<30 µs	L	
Open	H	<30 µs	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	RSM	
C1+, C2+	29, 1	Positive terminal of the voltage-doubler charge-pump capacitor
V+	30	5.5-V supply generated by the charge pump
C1–, C2-	31, 2	Negative terminal of the voltage-doubler charge-pump capacitor
INVALID	6	Invalid Output Pin
V–	3	–5.5-V supply generated by the charge pump
DIN1 DIN2 DIN3	4 5 7	Driver inputs
ROUT5 - ROUT1	10, 11, 12, 13, 14	Receiver outputs. Swing between 0 and V_L.
V_L	15	Logic-level supply. All CMOS inputs and outputs are referenced to this supply.
RIN5-RIN1	17, 18, 19, 20, 21	RS-232 receiver inputs
DOUT3 DOUT2 DOUT1	22 23 25	RS-232 driver outputs
GND	26	Ground
V_{CC}	27	3-V to 5.5-V supply voltage
$\overline{\text{FORCEOFF}}$	28	Powerdown Control input (Refer to Truth Table)
FORCEON	9	Powerdown Control input (Refer to Truth Table)

ABSOLUTE MAXIMUM RATINGS(1)

over junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	V_{CC} to GND		–0.3	6	V
	V_L to GND		–0.3	V_{CC} + 0.3	V
	V+ to GND		–0.3	7	V
	V– to GND		0.3	–7	V
	V+ + |V–|(2)			13	V
V_I	Input voltage	DIN, $\overline{\text{FORCEOFF}}$ to GND, FORCEON to GND	–0.3	6	V
		RIN to GND		±25	
V_O	Output voltage	DOUT to GND		±13.2	V
		ROUT	–0.3	V_L + 0.3	
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
(2) V+ and V– can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.

THERMAL INFORMATION

THERMAL METRIC(1)		TRS3253E-EP RSM 32 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	37.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	30.1	
θ_{JB}	Junction-to-board thermal resistance(4)	7.8	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.4	
ψ_{JB}	Junction-to-board characterization parameter(6)	7.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	2.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

				MIN	MAX	UNIT
V_{CC}	Supply voltage			3	5.5	V
V_L	Supply voltage			1.65	V_{CC}	V
	Input logic threshold low	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V_L = 3 V or 5.5 V		0.8	V
			V_L = 2.3 V		0.6	
			V_L = 1.65 V		0.5	
	Input logic threshold high	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V_L = 5.5 V	2.4		V
			V_L = 3 V	2.0		
			V_L = 2.7 V	1.4		
			V_L = 1.95 V	1.25		
	Junction temperature			–55	125	°C
	Receiver input voltage			–25	25	V

ELECTRICAL CHARACTERISTICS(1)

over junction temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
I_I	Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON			±0.01	±2.9	µA
I_{CC}	Supply current (T_J = 25°C)	Auto-powerdown plus disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V_{CC}		0.5	1.11	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND		1	10	µA
		Auto-powerdown plus enabled	No load, $\overline{\text{FORCEOFF}}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	

(1) Testing supply conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.15 V; C1–C4 = 0.22 µF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 µF and C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_J = 25°C.

ESD PROTECTION

PARAMETER	TEST CONDITIONS	TYP	UNIT
RIN, DOUT	Human-Body Model	±15	kV
	IEC 61000-4-2 Air-Gap Discharge	±8	
	IEC 61000-4-2 Contact Discharge	±8	

RECEIVER SECTION

Electrical Characteristics

over junction temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), T_A = T_{MIN} to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{off}	Output leakage current	ROUT, receivers disabled			±0.05	±25	µA
V_{OL}	Output voltage low	I_{OUT} = 1.6 mA				0.4	V
V_{OH}	Output voltage high	I_{OUT} = –1 mA		V_L – 0.6	V_L – 0.1		V
$V_{IT–}$	Input threshold low	T_J = 25°C	V_L = 5 V	0.8	1.2		V
			V_L = 3.3 V	0.6	1.5		
V_{IT+}	Input threshold high	T_J = 25°C	V_L = 5 V		1.8	2.4	V
			V_L = 3.3 V		1.5	2.4	
V_{hys}	Input hysteresis				0.5		V
	Input resistance	T_J = 25°C		3	5	7	kΩ

(1) Typical values are at V_{CC} = V_L = 3.3 V, T_J = 25°C

Switching Characteristics

over junction temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), T_J = T_{MIN} to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
t_{PHL}	Receiver propagation delay	Receiver input to receiver output, C_L = 150 pF	0.15	µs
t_{PLH}			0.15	
t_{PHL} – t_{PLH}	Receiver skew		50	ns
t_{en}	Receiver output enable time	From $\overline{\text{FORCEOFF}}$	200	ns
t_{dis}	Receiver output disable time	From $\overline{\text{FORCEOFF}}$	200	ns

(1) Typical values are at V_{CC} = V_L = 3.3 V, T_J = 25°C.

DRIVER SECTION

Electrical Characteristics

over junction temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), T_J = T_{MIN} to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	Output voltage swing	All driver outputs loaded with 3 kΩ to ground, V_{CC}= 3.1V to 5.5V	±5	±5.4		V
r_O	Output resistance	V_{CC} = V+ = V– = 0, Driver output = ±2 V	300	10M		Ω
I_{OS}	Output short-circuit current	V_{T_OUT} = 0			±60	mA
I_{OZ}	Output leakage current	V_{T_OUT} = ±12 V, $\overline{\text{FORCEOFF}}$ = GND, V_{CC} = 3 V to 3.6 V			±25	µA
		V_{T_OUT} = ±12 V, $\overline{\text{FORCEOFF}}$ = GND, V_{CC} = 4.5 V to 5.5 V				
	Driver input hysteresis				0.5	V
	Input leakage current	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		±0.01	±2.9	µA

(1) Typical values are at V_{CC} = V_L = 3.3 V, T_J = 25°C

Timing Requirements

over junction temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), T_j = T_{MIN} to T_{MAX} (unless otherwise noted)

PARAMETER				MIN	TYP(1)	MAX	UNIT
	Maximum data rate	R_L = 3 kΩ, C_L = 200 pF, One driver switching		1000			kbps
	Time-to-exit powerdown	$\|V_{T\_OUT}\|$ > 3.7 V			100		µs
$\|t_{PHL} – t_{PLH}\|$	Driver skew(2)				100		ns
	Transition-region slew rate	V_{CC} = 3.3 V, T_j = 25°C, R_L = 3 kΩ to 7 kΩ, Measured from 3 V to –3 V or –3 V to 3 V	C_L = 150 pF to 1000 pF	15		150	V/µs

(1) Typical values are at V_{CC} = V_L = 3.3 V, T_J = 25°C.
(2) Driver skew is measured at the driver zero crosspoint.

AUTO-POWERDOWN SECTION

Electrical Characteristics

over recommended ranges of supply voltage and junction temperature (unless otherwise noted) (see Figure 7)

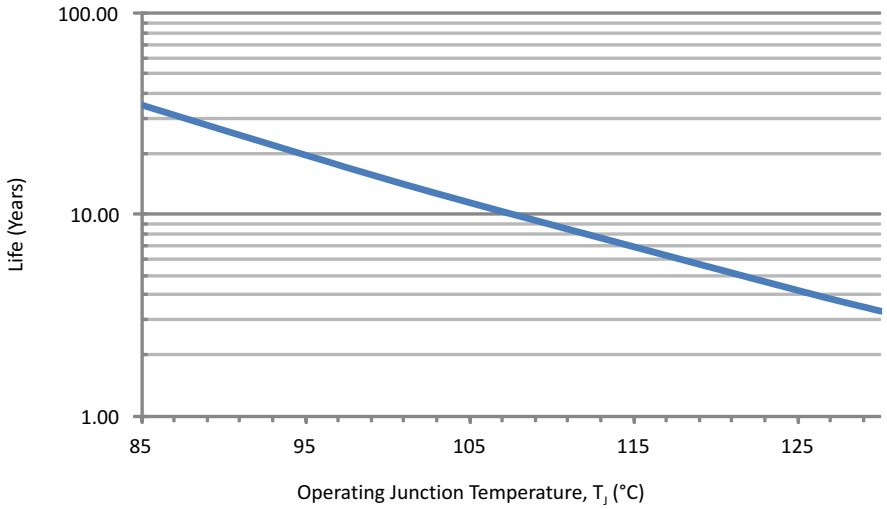
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{IT+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	$\overline{FORCEON}$ = GND, $\overline{FORCEOFF}$ = V_L		2.7	V
$V_{IT-(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	$\overline{FORCEON}$ = GND, $\overline{FORCEOFF}$ = V_L	–2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	$\overline{FORCEON}$ = GND, $\overline{FORCEOFF}$ = V_L	–0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = -1 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_L	V_L – 0.6		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_L		0.4	V

Switching Characteristics

over recommended ranges of supply voltage and junction temperature (unless otherwise noted) (see Figure 7)

PARAMETER		MIN	TYP(1)	MAX	UNIT
t_{valid}	Propagation delay time, low- to high-level output		0.1		µs
$t_{invalid}$	Propagation delay time, high- to low-level output		50		µs
t_{en}	Supply enable time		25		µs
t_{dis}	Receiver or driver edge to auto-powerdown plus		30		µs

(1) All typical values are at V_{CC} = V_L = 3.3 V and T_J = 25°C.



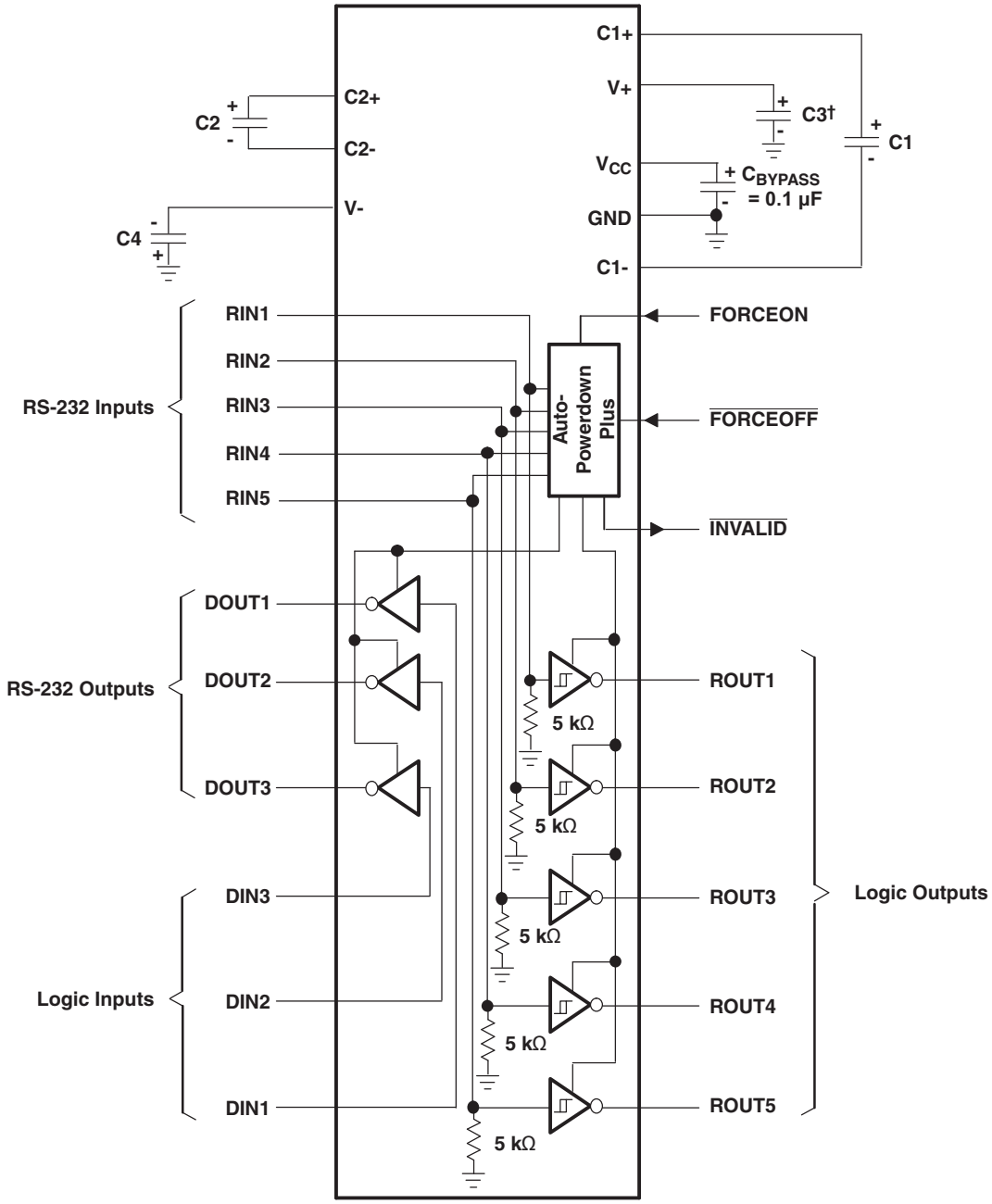
(1) See datasheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) Enhanced plastic product disclaimer applies.

Figure 1. TRS3253E-EP Operating Life Derating Chart

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

Figure 2. Typical Operating Circuit and Capacitor Values

PARAMETER MEASUREMENT INFORMATION

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

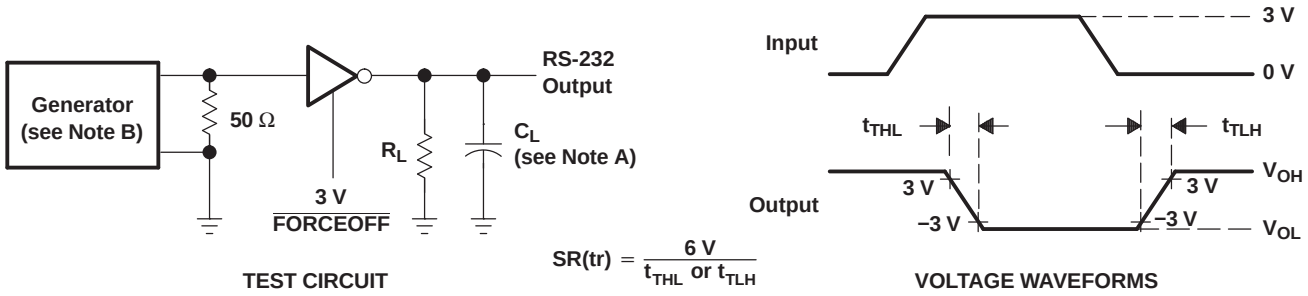


Figure 3. Driver Slew Rate

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

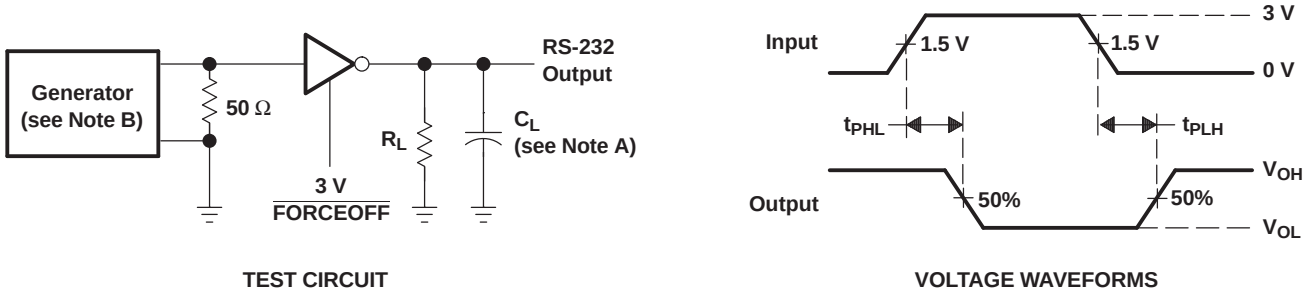


Figure 4. Driver Pulse Skew

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

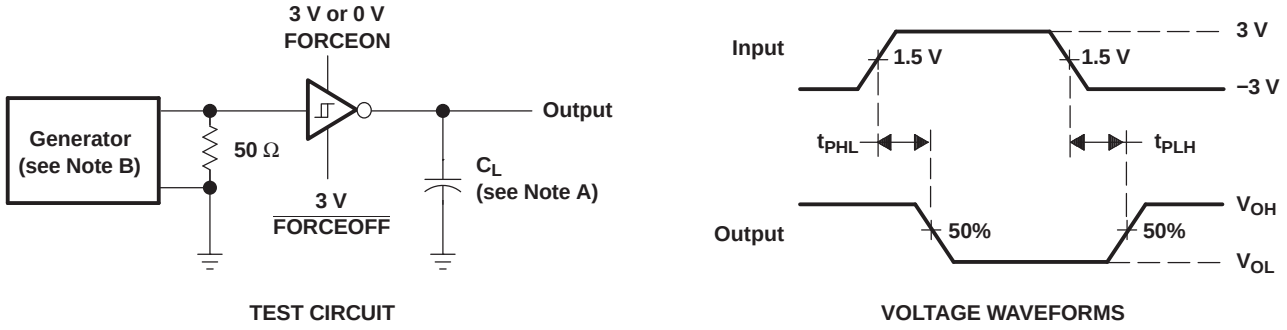


Figure 5. Receiver Propagation Delay Times

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

D. t_{PZL} and t_{PZH} are the same as t_{en}.

PARAMETER MEASUREMENT INFORMATION (continued)

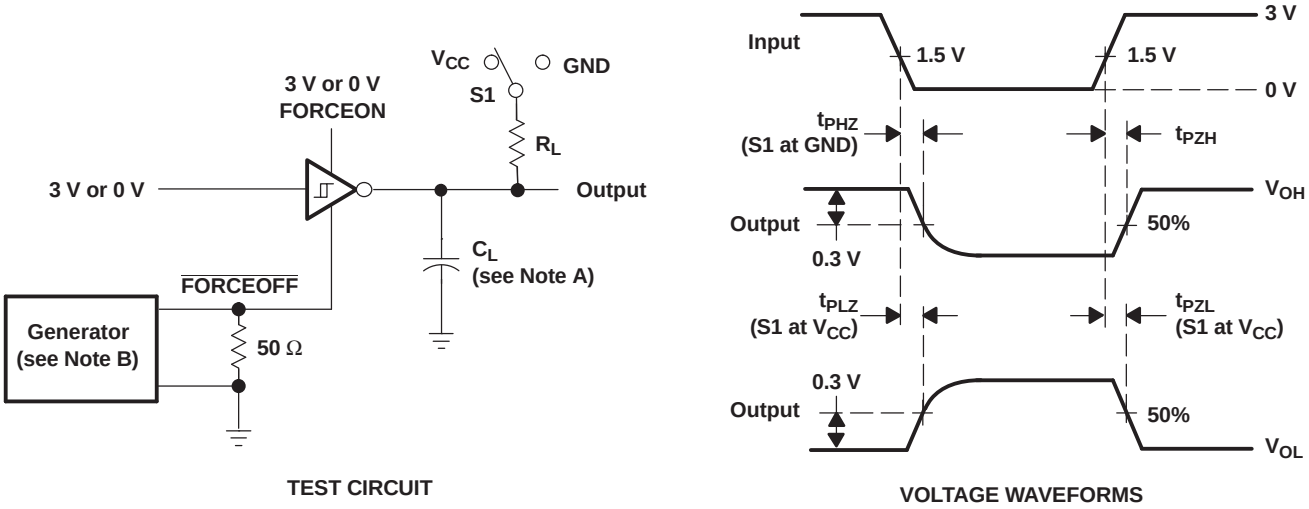
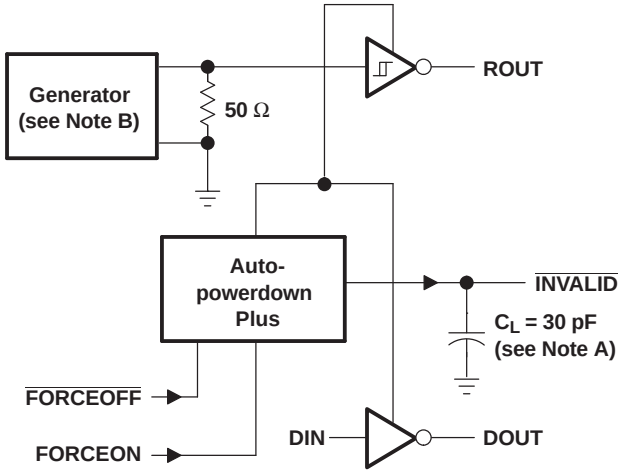
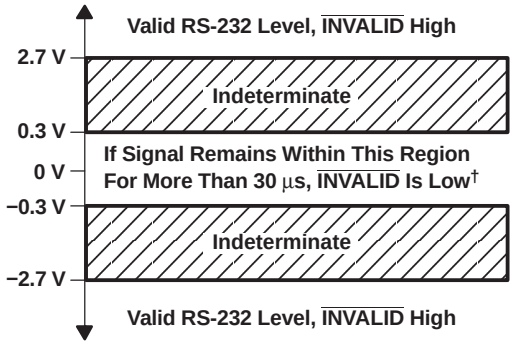


Figure 6. Receiver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION (continued)

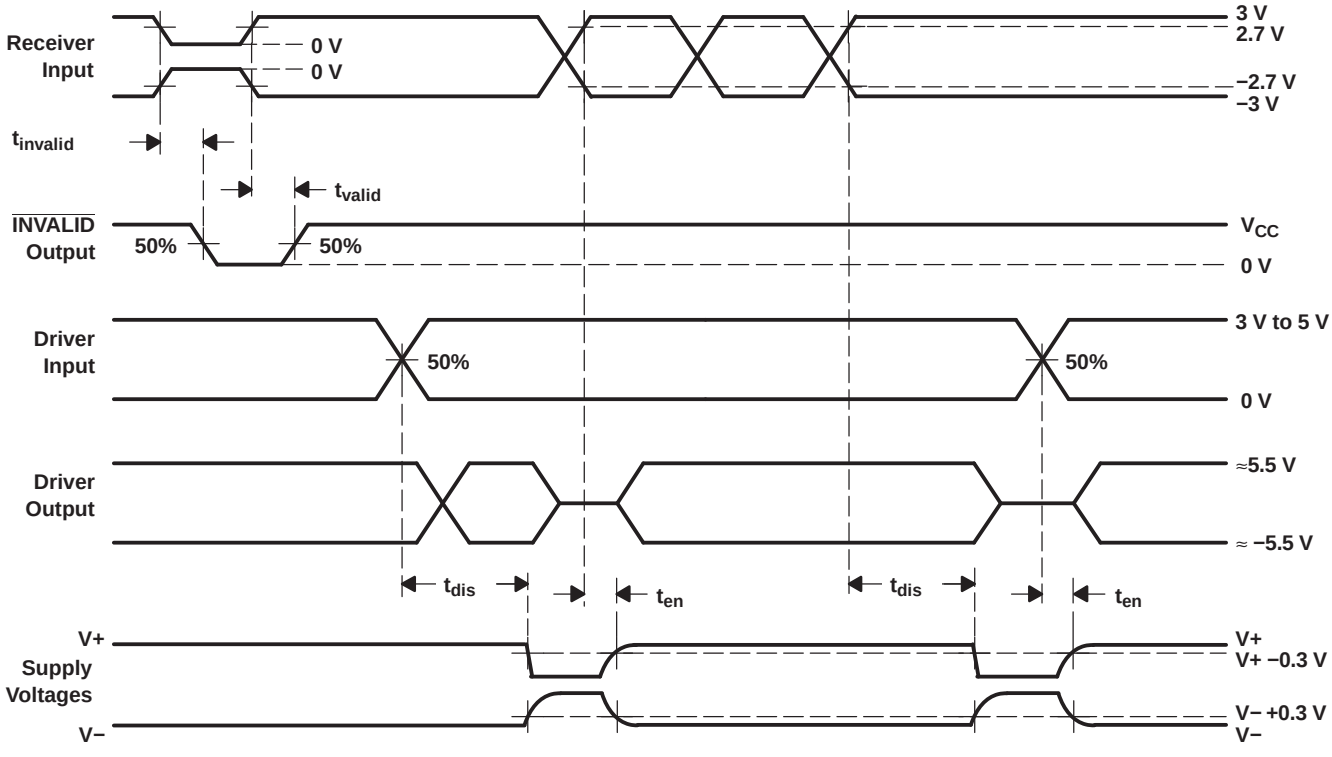


TEST CIRCUIT



† Auto-powerdown plus disables drivers and reduces supply current to 1 μA.

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.



Voltage Waveforms and Timing Diagrams

Figure 7. INVALID Propagation-Delay Times and Supply-Enabling Time

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3253EMRSMREP	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	RS53EP	Samples
V62/13621-01XE	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	RS53EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TRS3253E-EP :

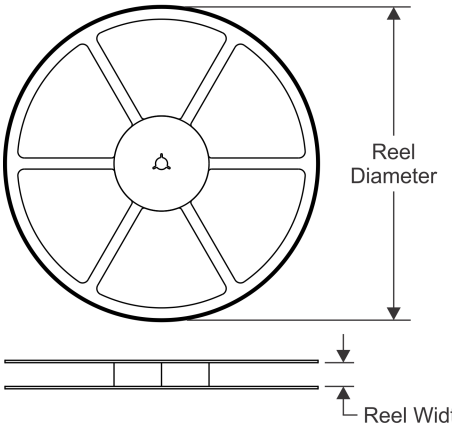
- Catalog: TRS3253E

NOTE: Qualified Version Definitions:

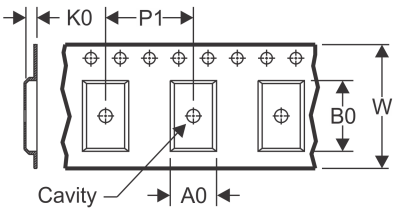
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

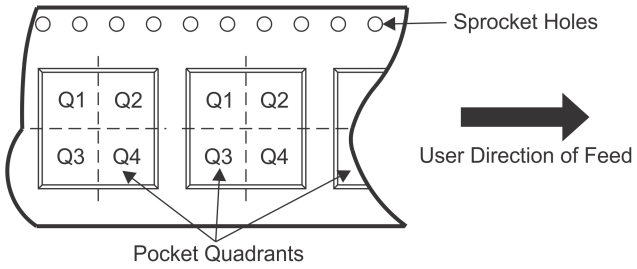


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

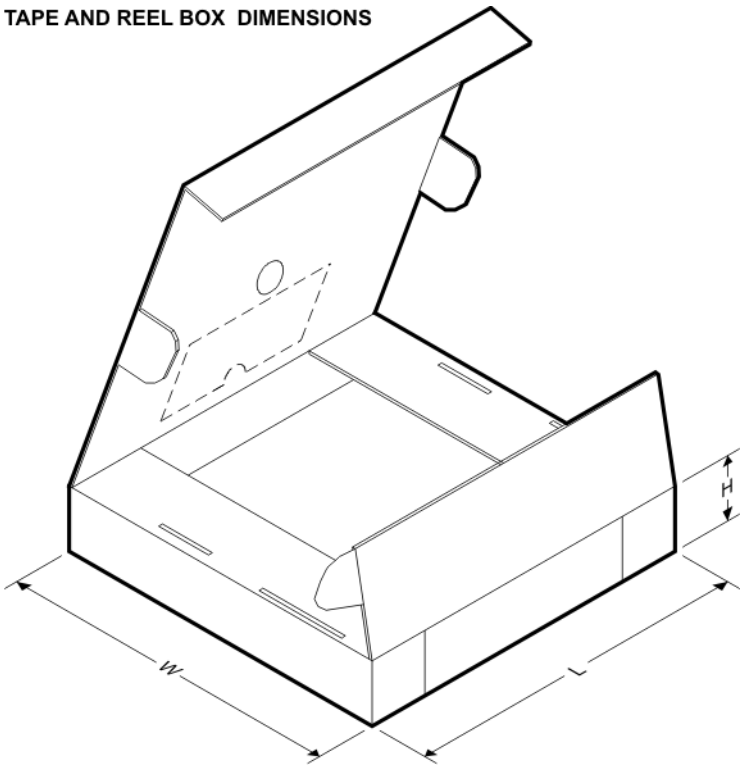
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3253EMRSMREP	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

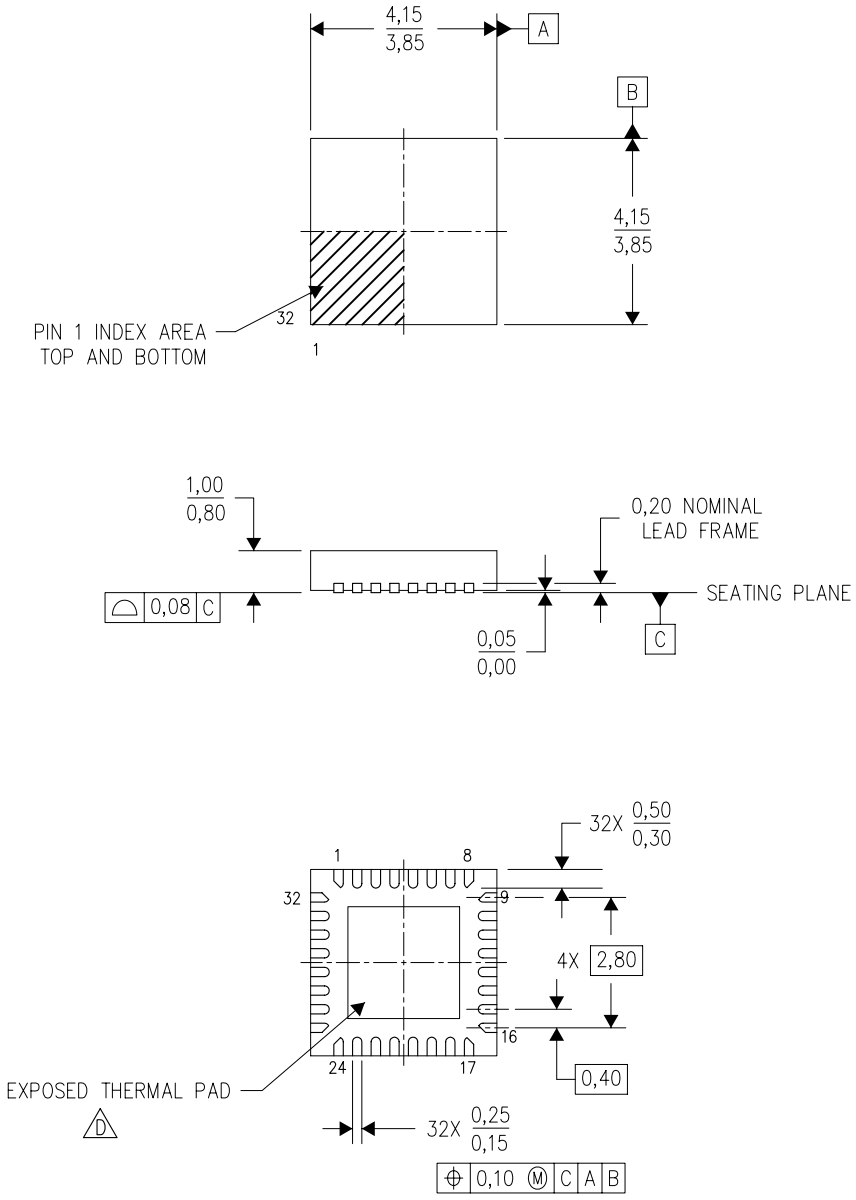
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3253EMRSMREP	VQFN	RSM	32	3000	367.0	367.0	35.0

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4207560/B 03/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

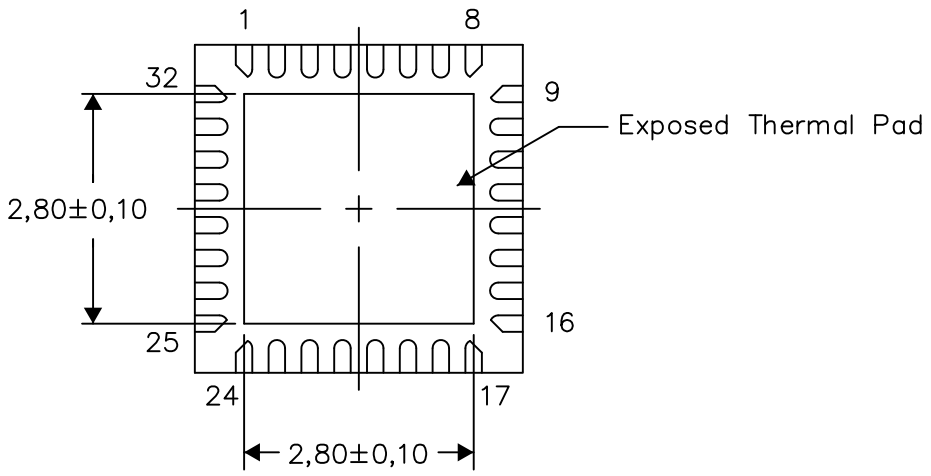
RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



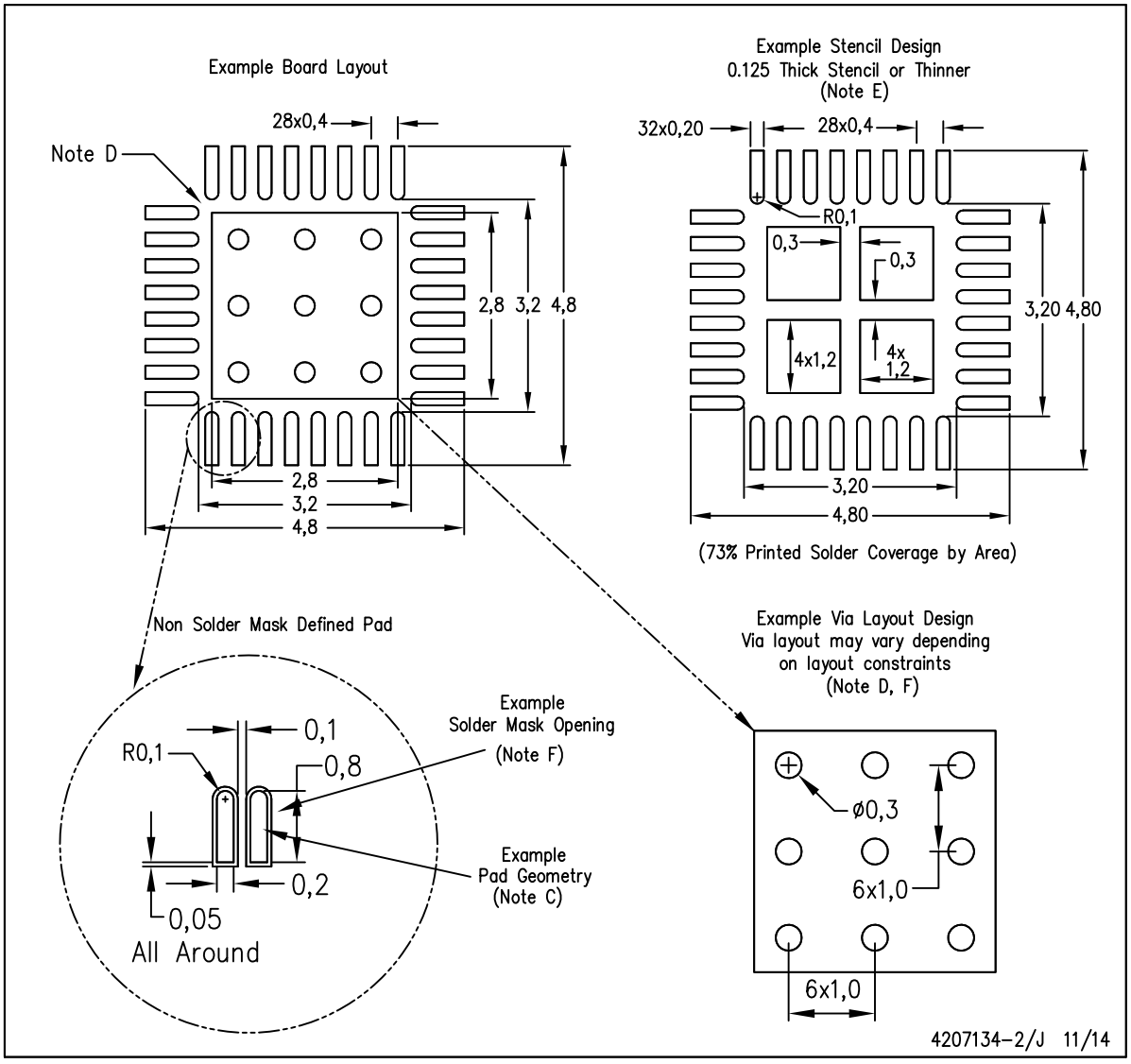
Bottom View

Exposed Thermal Pad Dimensions

4207868–2/I 07/14

NOTE: All linear dimensions are in millimeters

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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