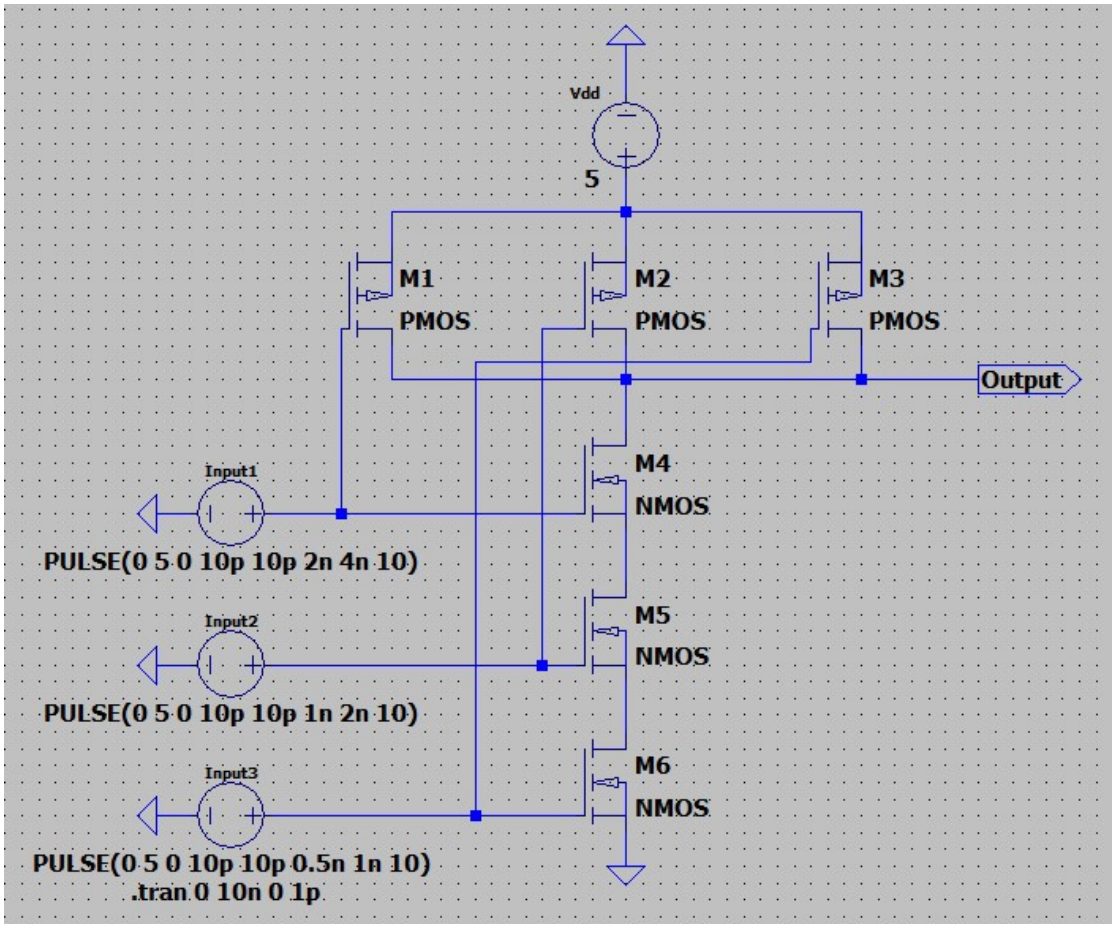
Department of
Electrical & Electronic Engineering
Independent University, Bangladesh

Summer-2020-EEE466

NAME
Faiyaz Ahmed

ID
1820545

1. **CMOS 3 Input NAND Gate:**



PMOS l=0.9u w=1.8u [M1=M2=M3]

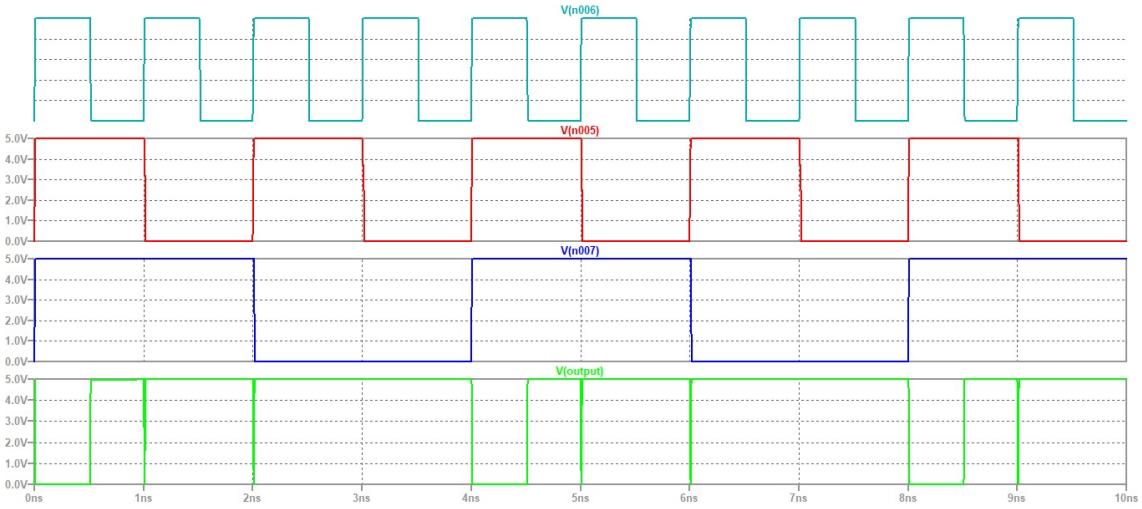
NMOS l=0.9u w=1.8u [M4=M5=M6]

$$\frac{\beta p}{\beta n} = 2$$

i. **Truth Table:**

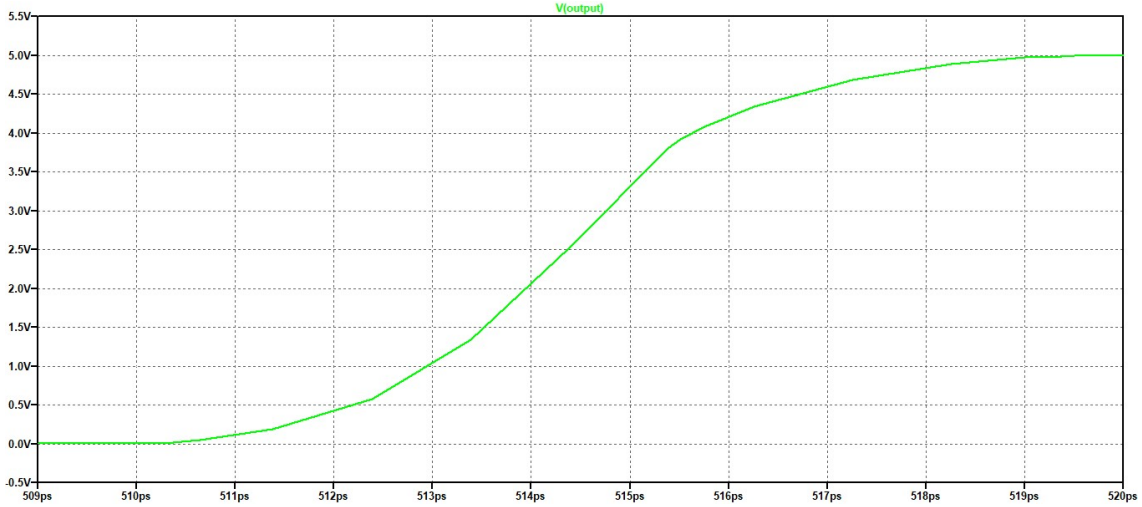
3 Input NAND Gate Truth table

inputs			Outputs
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



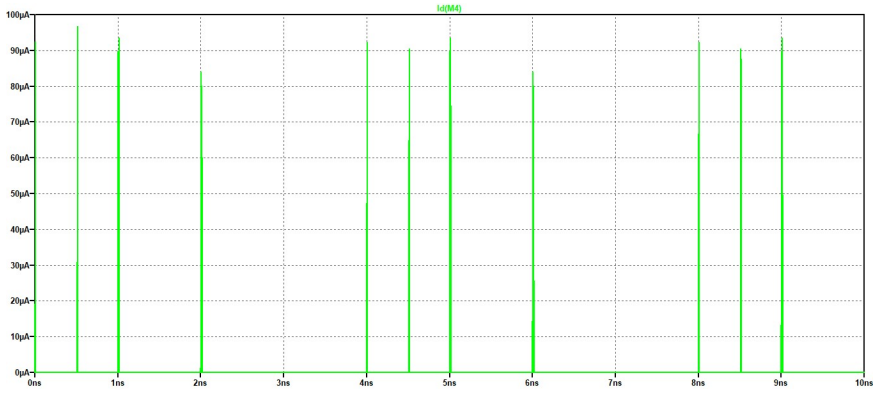
Truth Table Verified

ii. Time Delay for Output Voltage to Change:



Delay[approximately] = 10 ps

iii. Static Power Dissipation:



No Static Power Dissipation

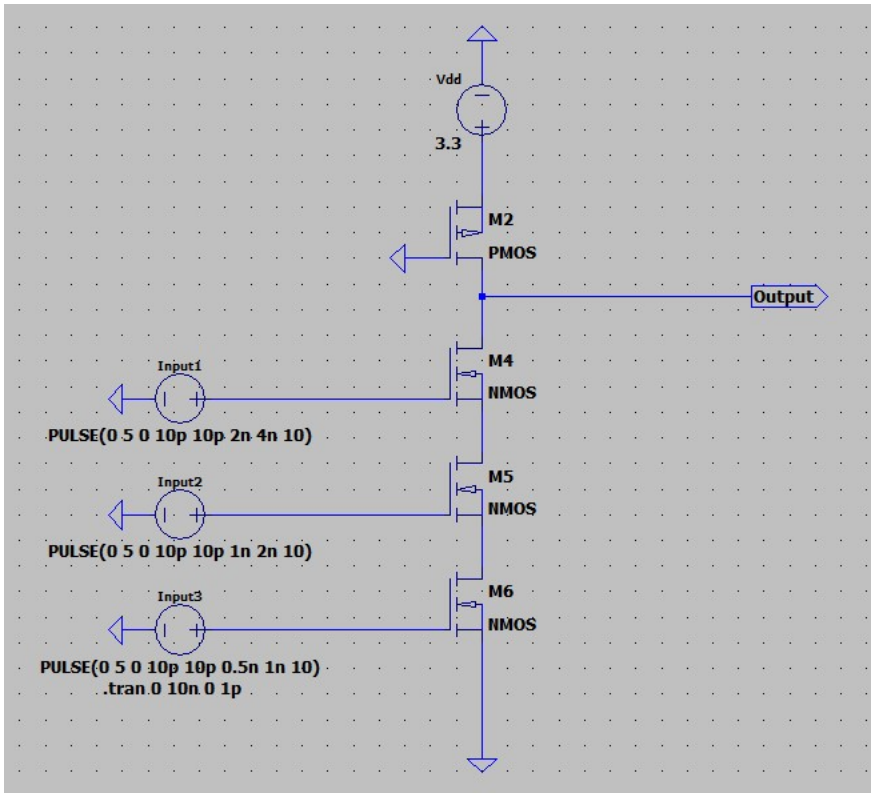
Discussion: Since there is a finite rise/fall time for both pMOS and nMOS, during transition, for example, from off to on, and vice-versa, both the transistors will be on for a small period of time in which current will find a path directly from V_{DD} to ground, hence creating a short-circuit current. Short-circuit power dissipation increases with rise and fall time of the transistors.

Average Power Dissipation [due to Short-circuit power dissipation] = $\frac{5.22x10^{-15}}{(8-4)x10^{-9}} = 1.305x10^{-6}W$

iv. Approximate Physical Area:

$$\mathbf{1.5xWxLxn_p + 1.5xWxLxn_n = 1.5x0.9x1.8x3 + 1.5x0.9x1.8x3 = 14.58\mu m^2}$$

2. Pseudo-NMOS 3 Input NAND Gate:



PMOS l=0.18u w=0.18u

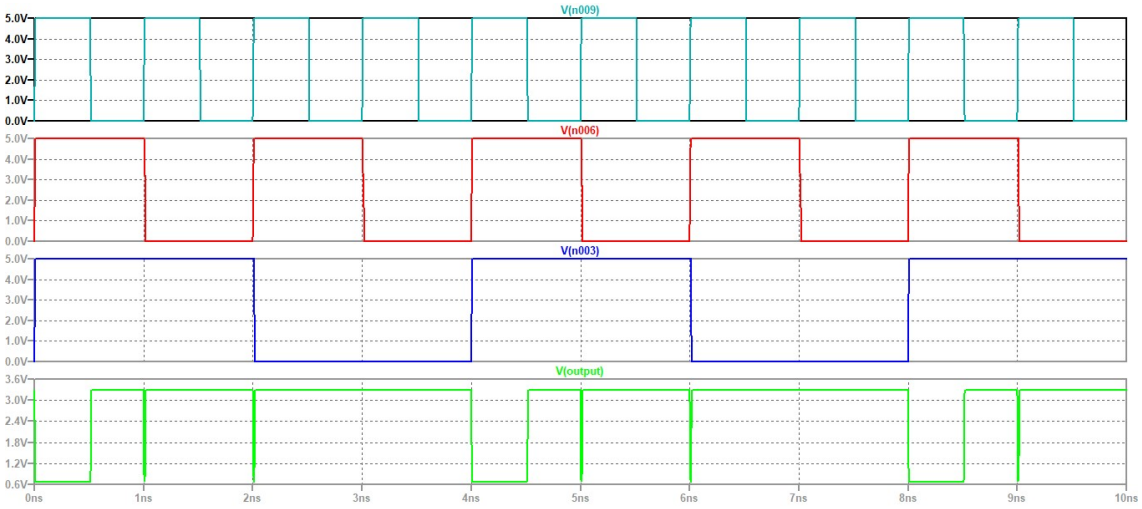
NMOS l=0.18u w=0.9u [M4=M5=M6]

$$\frac{\boldsymbol{\beta}\mathrm{p}}{\boldsymbol{\beta n}} = \mathbf{5}$$

i. Truth Table:

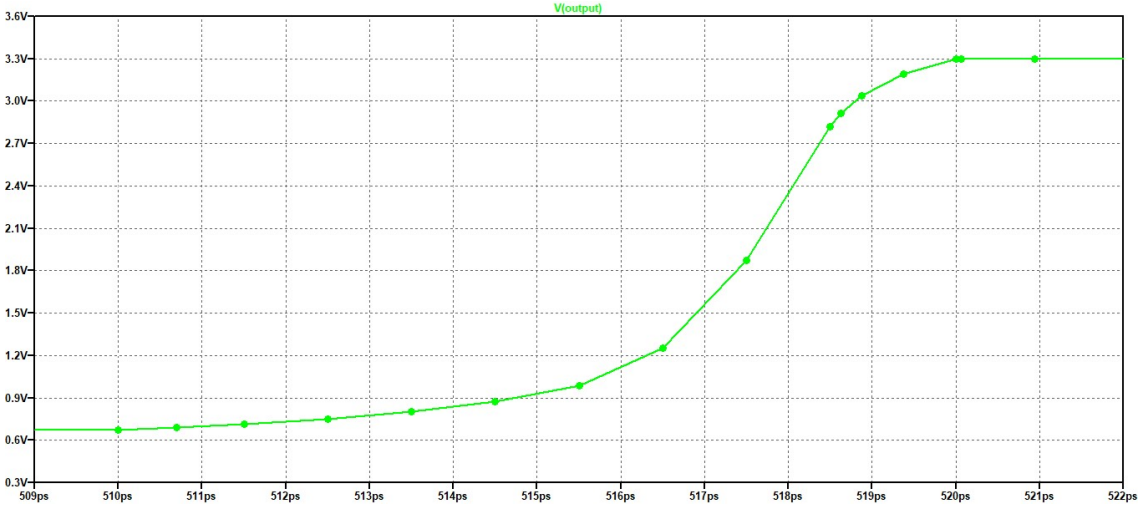
3 Input NAND Gate Truth table

inputs			Outputs
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



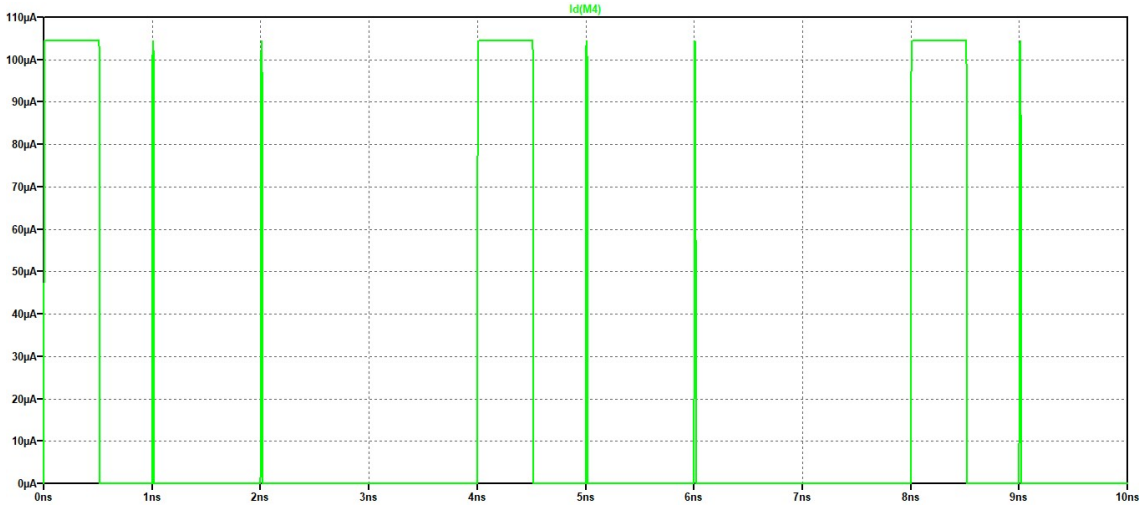
Truth Table Verified

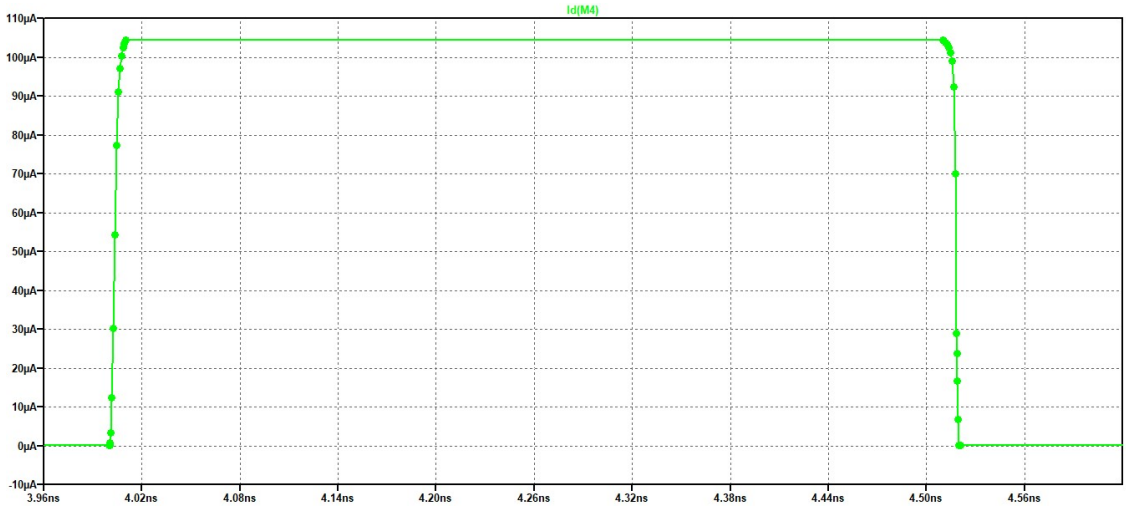
ii. Time Delay for Output Voltage to Change:



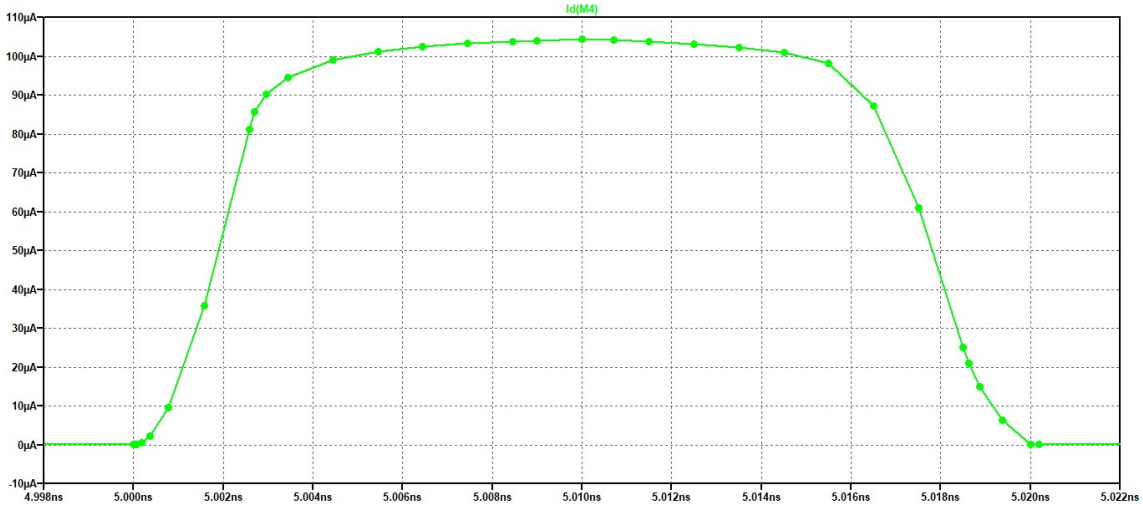
Delay[approximately] = 10 ps

iii. Static Power Dissipation:





Static Power Dissipation = $\mathrm{I_{Dmax}} x V_{DD} = 104.62 \mu A \; x \; 3.3 v = 3.45246 \; x \; 10^{-4} W$



Average Power Dissipation = $\frac{I_{Dmax}\, x\, t_{on}}{T} x V_{DD} =$

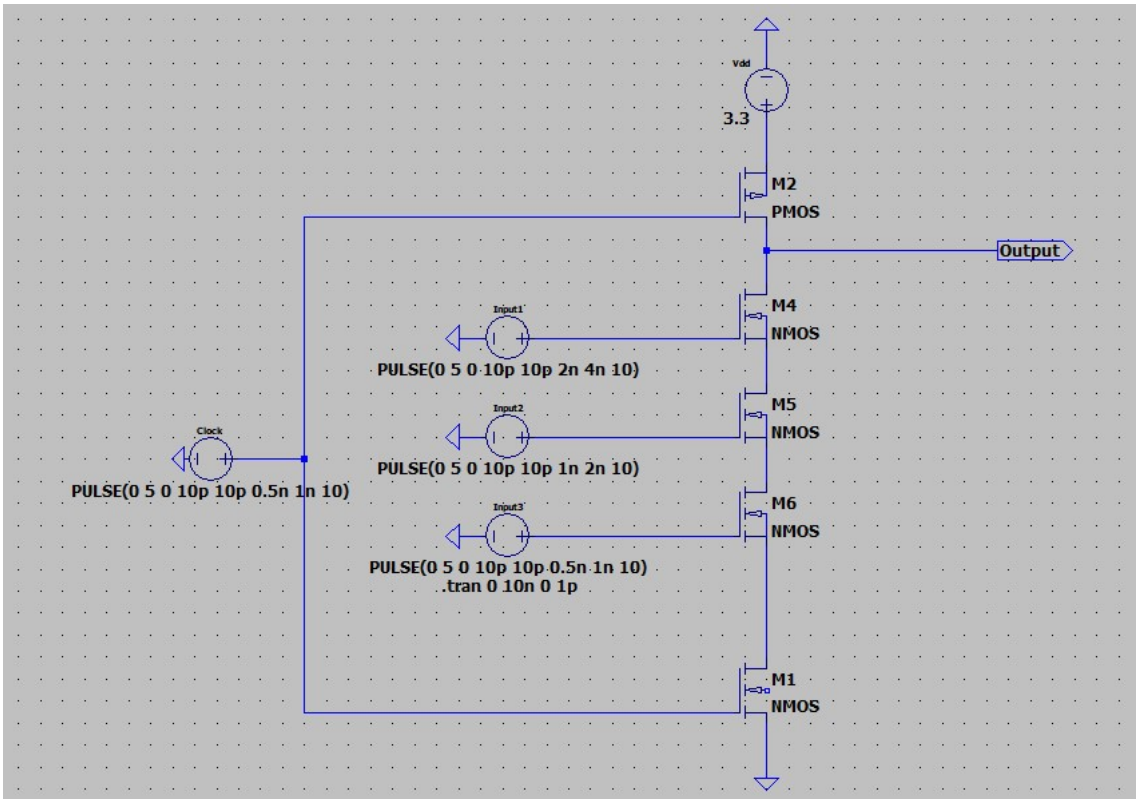
$\frac{104.62\mu A\, x\, (4.5ns - 4ns) + 2x[104.62\mu A\, x\, (5.02ns - .00ns)]}{8ns - 4ns} x3.3v = 4.66x10^{-5}$ W

iv. Approximate Physical Area:

$$1.5xWxLxn_p + 1.5xWxLxn_n = 1.5x0.18x0.18x1 + 1.5x0.9x0.18x3$$
$$= 0.7776\mu m^2$$

Discussion: Here, the larger the W/L of the load transistor, the higher the power dissipation.

3. Dynamic Logic 3 Input NAND Gate:



PMOS l=0.18u w=0.18u

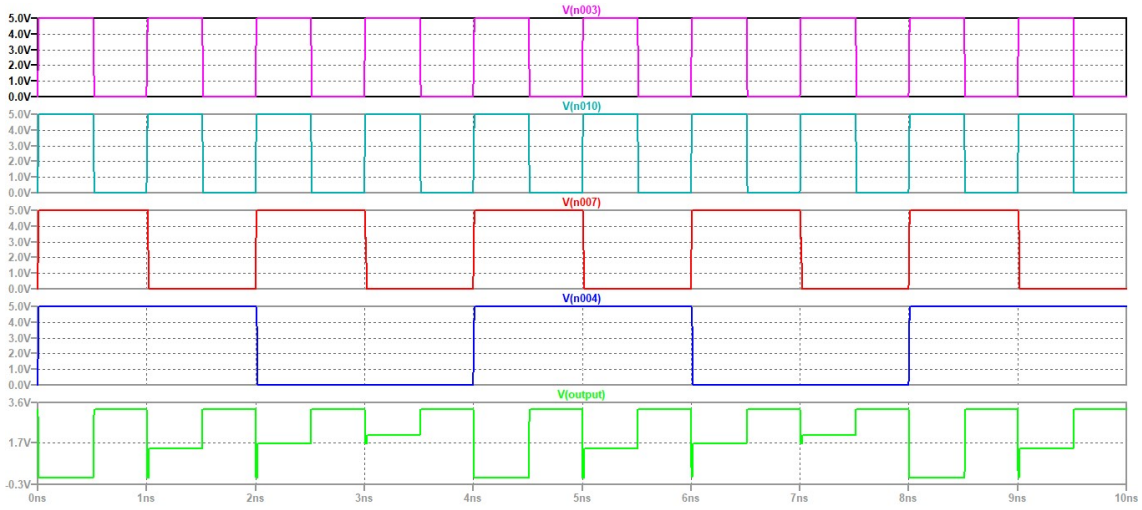
NMOS l=0.18u w=0.18u [M1=M4=M5=M6]

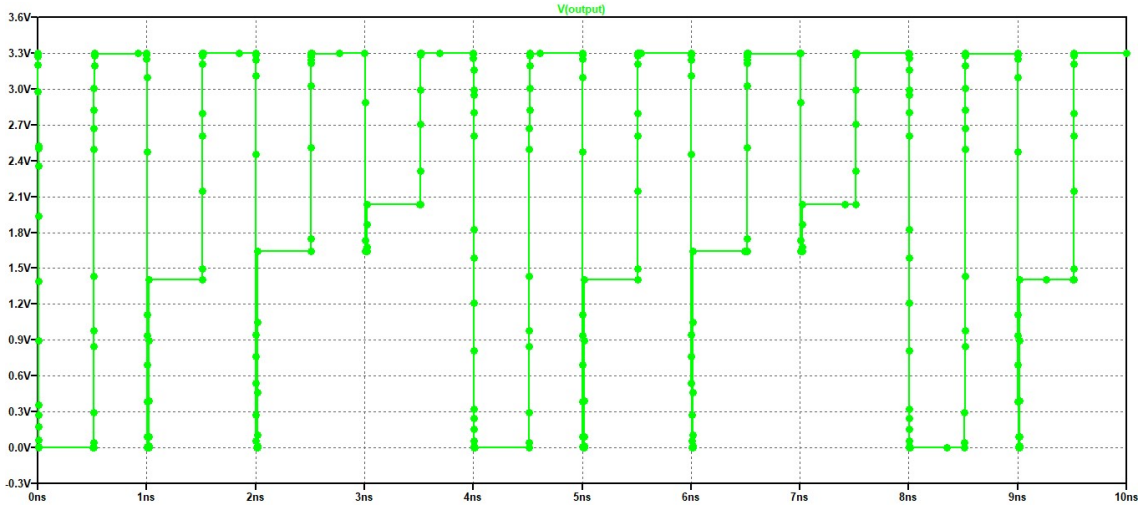
$$\frac{\beta p}{\beta n} = 1$$

i. Truth Table:

3 Input NAND Gate Truth table

inputs			Outputs
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



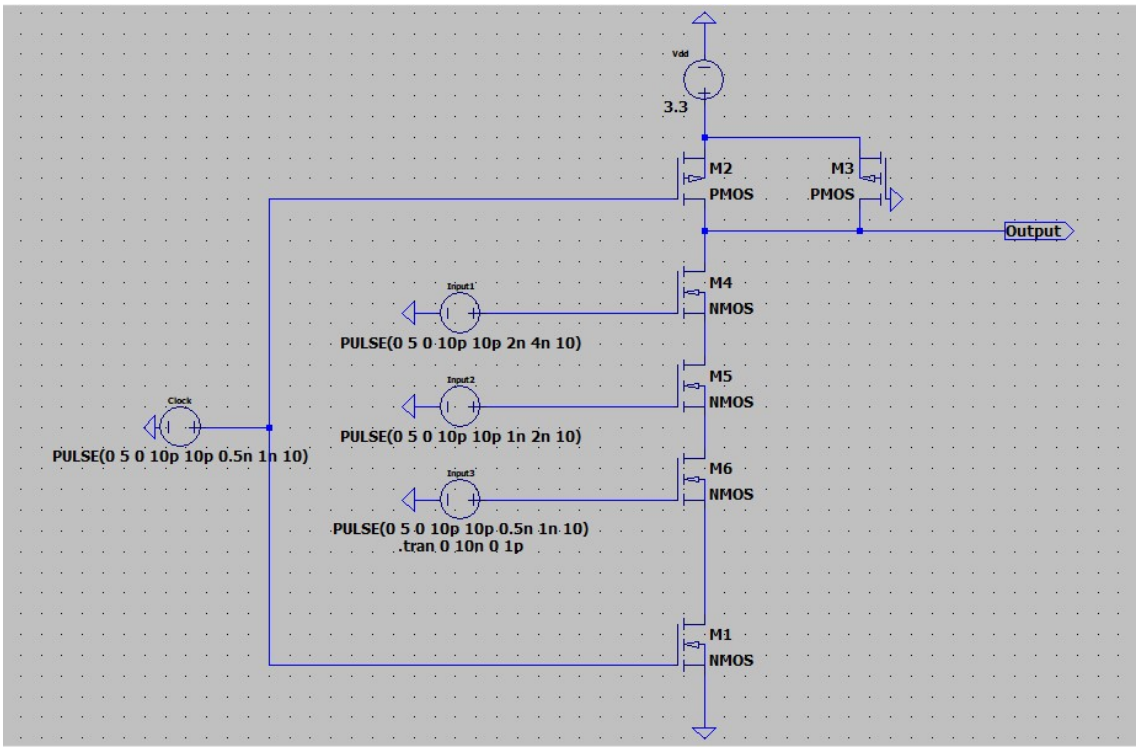


Truth table not verifiable due charge sharing effect of dynamic logic:

Discussion: Charge sharing occurs when the charge which is stored at the output node in the pre-charge phase is shared among the output or junction capacitances of transistors which are in the

evaluation phase. Charge sharing degrades the output voltage level or even cause erroneous output value.

4. Static Bleeder Dynamic Logic 3 Input NAND Gate:



PMOS l=0.18u w=0.18u [M2=M3]

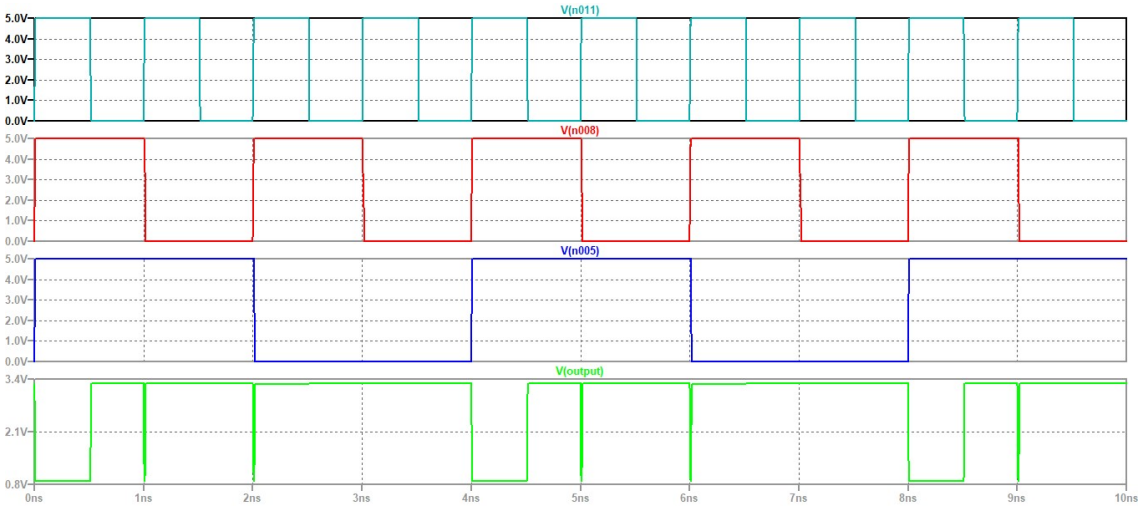
NMOS l=0.18u w=0.9u [M1=M4=M5=M6]

$$\frac{\boldsymbol{\beta}\mathrm{p}}{\boldsymbol{\beta n}} = 5$$

i. Truth Table:

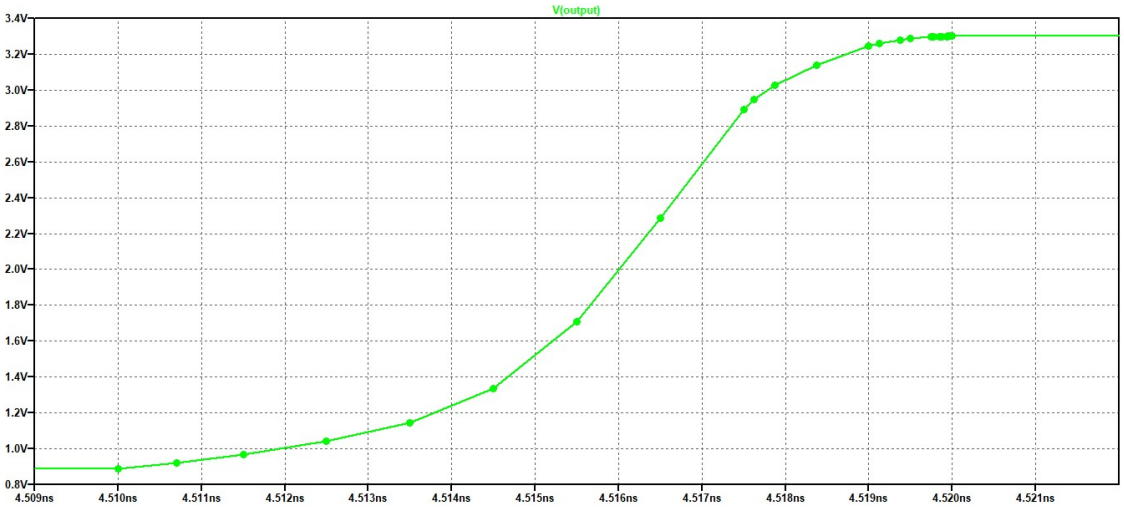
3 Input NAND Gate Truth table

inputs			Outputs
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



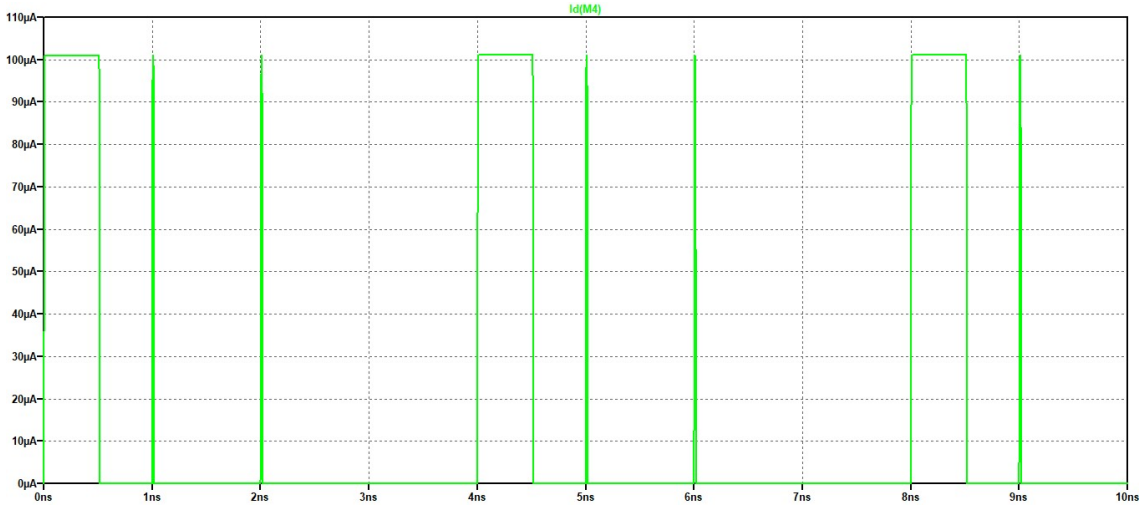
Truth Table Verified

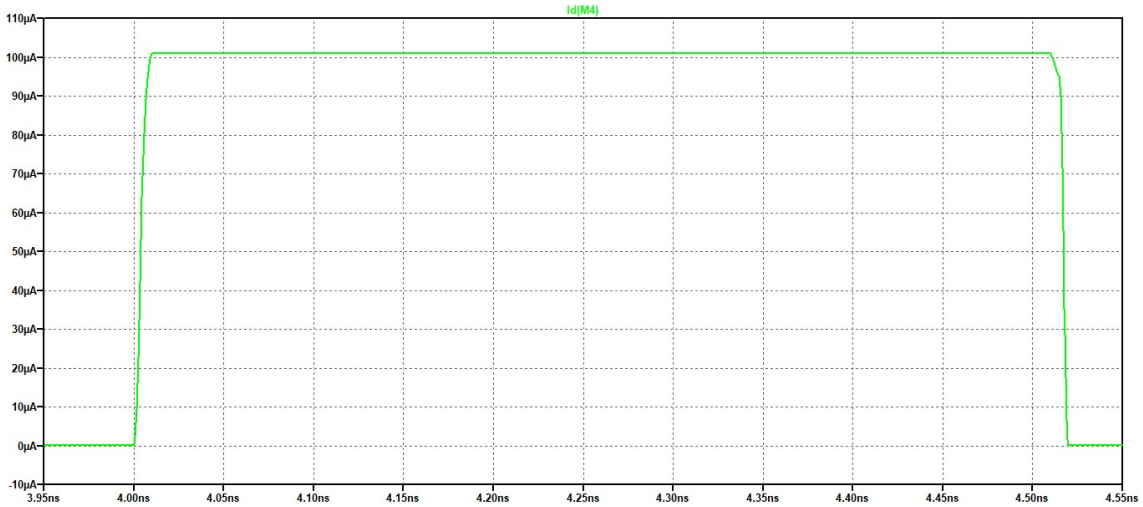
ii. Time Delay for Output Voltage to Change:



Delay[approximately]=4.520ns-4.510ns=10ps

iii. Static Power Dissipation:





Static Power Dissipation = $\mathrm{I_{Dmax}} x V_{DD} = 101.18\mu A\ x\ 3.3v = 3.33894\ x\ 10^{-4} W$

Average Power Dissipation = $\frac{\mathrm{I_{Dmax}}\ x\ \mathrm{t_{on}}}{\mathrm{T}} x V_{DD} = \frac{101.18\mu A\ x\ (4.52ns - 4ns) + 2x[101.18\mu A\ x\ (5.02ns - 5.00ns)]}{8ns - 4} x 3.3v = 4.674516x10^{-5} W$ W

i. Approximate Physical Area:

$$\mathbf{1.5xWxLxn_p + 1.5xWxLxn_n = 1.5x0.18x0.18x2 + 1.5x0.9x0.18x4}$$
$$\mathbf{= 1.0692\mu m^2}$$

Discussion: Logic 0 depends on $\frac{\beta \mathrm{p}}{\beta n}$, similar features as Pseudo NMOS

5. **Domino Logic 3 Input NAND Gate:** In dynamic logic, a problem arises when cascading one gate to the next. The precharge "1" state of the first gate may cause the second gate to discharge prematurely, before the first gate has reached its correct state. This uses up the "precharge" of the second gate, which cannot be restored until the next clock cycle, so there is no recovery from this error. In order to cascade dynamic logic

gates, one solution is domino logic, which inserts an ordinary static inverter between stages.

Hence, domino logic 3 input NAND gate would basically be the same as dynamic logic 3 input NAND gate [as at the moment no cascading is done].