Department of
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Design and Performance Analysis of a 4-bit Counter using LTSpice

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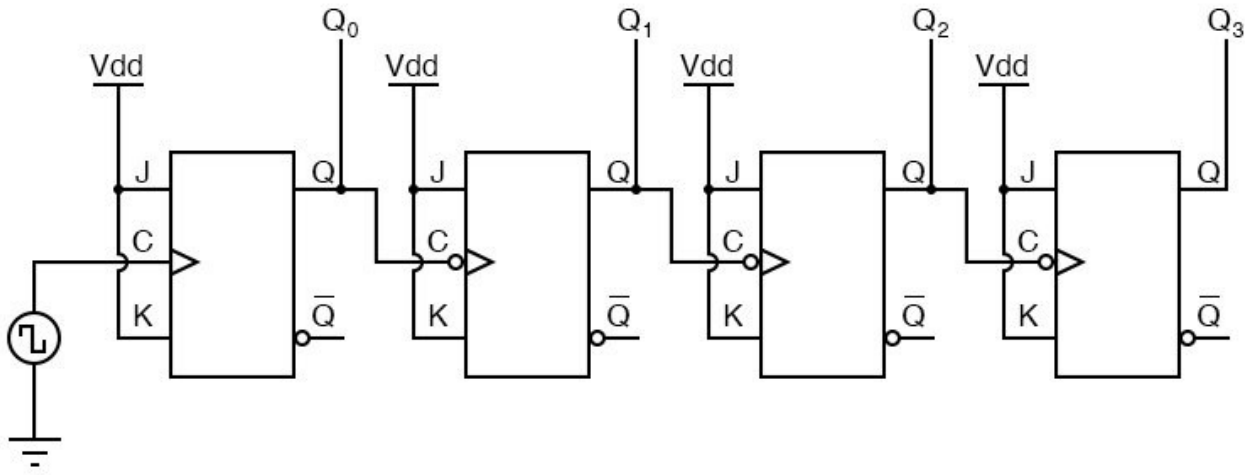
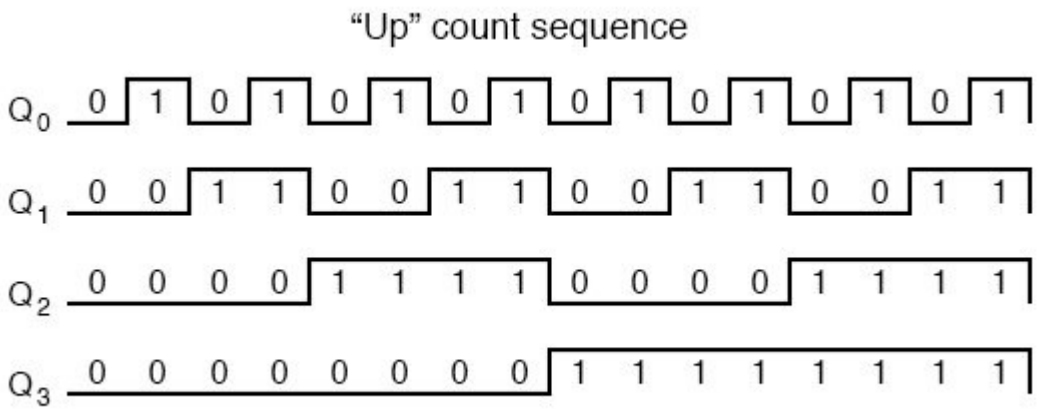
1) Asynchronous Counter

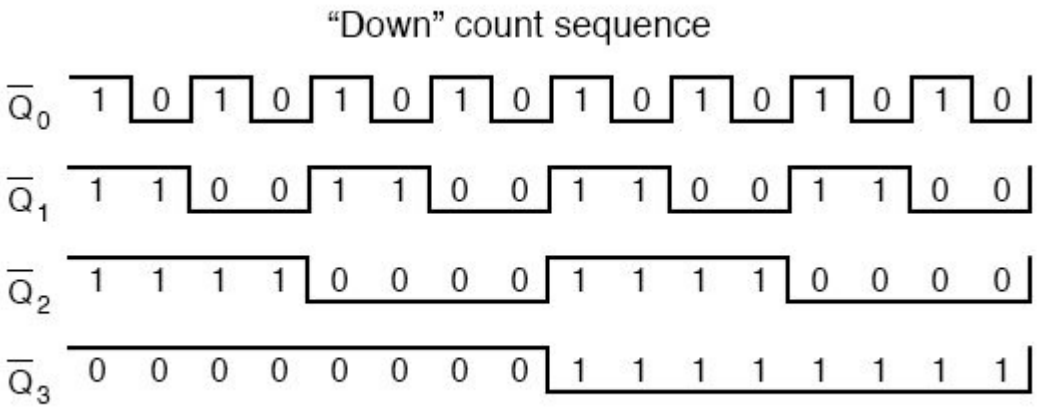
Asynchronous counters have only one Clock input in the first JK FF, the output of all other JK FF are connected to the Clock Pin of following JK FF. There may be delay in producing output as a result. The required number of logic gates to design asynchronous counters is very less. So, they are simple in design. Another name for Asynchronous counters is “Ripple counters”.

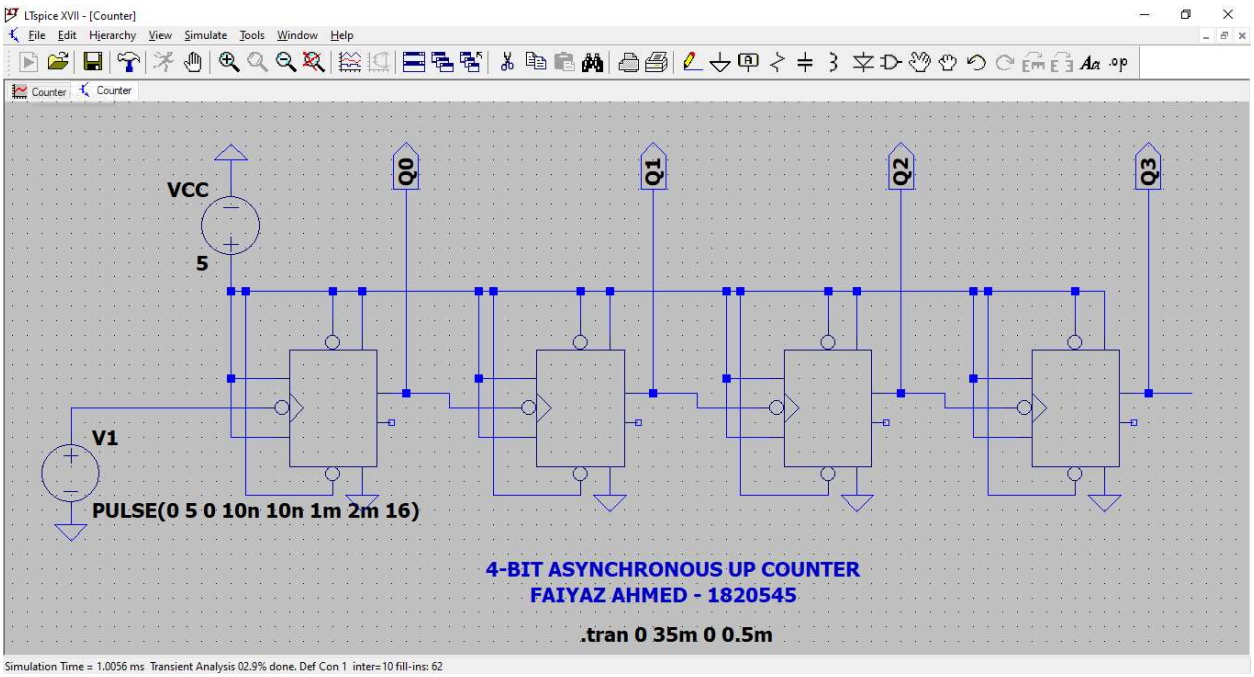
The first FF Q output, has an edge triggered clock input, so it toggles with each rising/falling edge of the clock signal. The toggling output acts as clock to the following JK FF. SR latch has a problem in that when both S and R are high, its state becomes indeterminate. JK latch shown at left eliminates this problem by using feedback from output to input, such all states in the truth table are allowable

A four-bit “up” counter



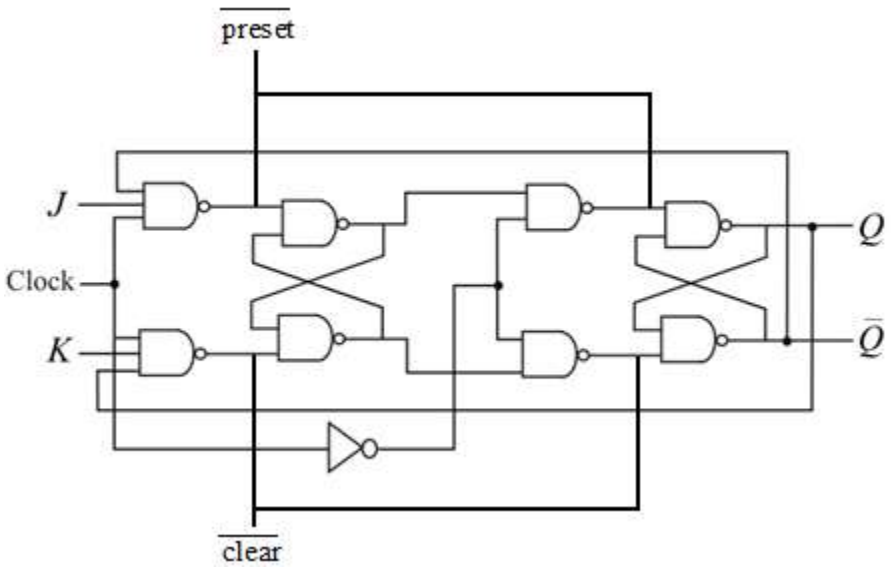

"Up" count sequence
Q_0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
Q_1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1
Q_2 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1
Q_3 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1


"Down" count sequence
$\overline{Q}_0$ 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0
$\overline{Q}_1$ 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0
$\overline{Q}_2$ 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0
$\overline{Q}_3$ 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1

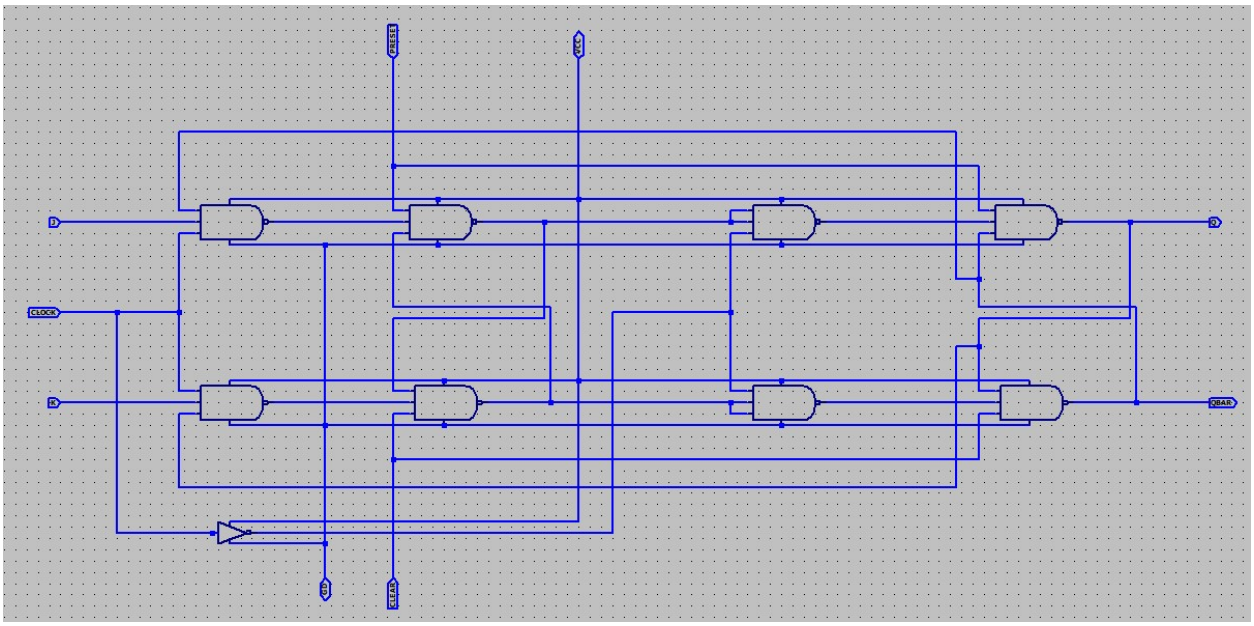

LTspice XVII - [Counter]
File Edit Hierarchy View Simulate Tools Window Help
Counter
Counter
VCC
5
Q0
Q1
Q2
Q3
V1
PULSE(0 5 0 10n 10n 1m 2m 16)
4-BIT ASYNCHRONOUS UP COUNTER
FAIYAZ AHMED - 1820545
.tran 0 35m 0 0.5m
Simulation Time = 1.0056 ms Transient Analysis 02.9% done. Def Con 1 inter=10 fill-ins: 62

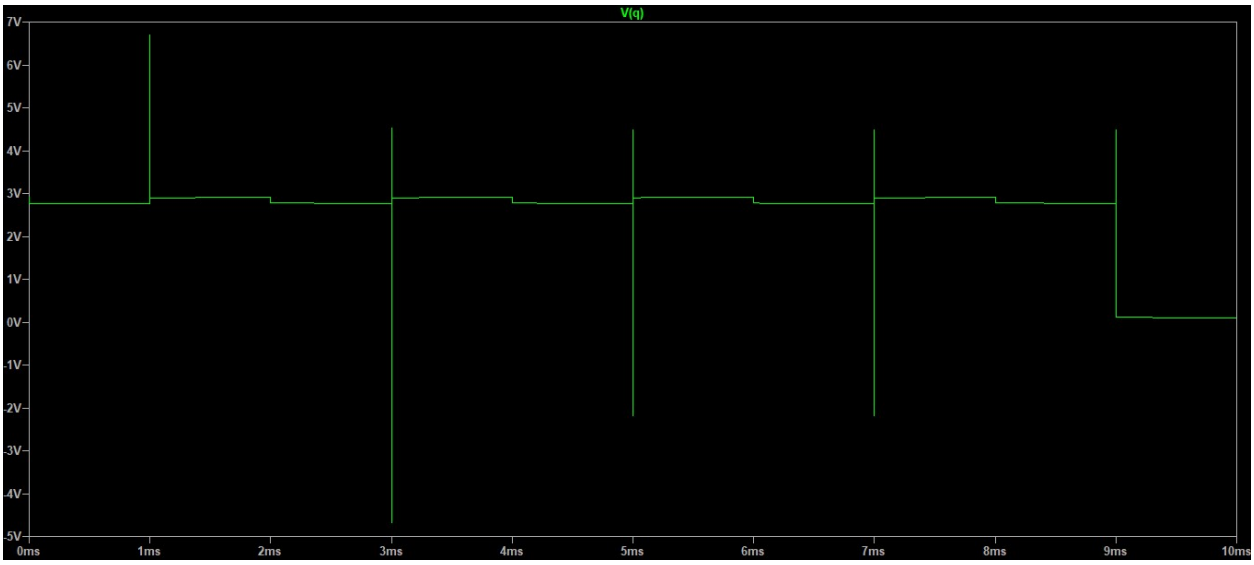
2) JK FF

	Input					Output	
	Preset	Clear	CLK	J	K	Q	$\overline{Q}$
Invalid	0	0	X	X	X	1*	1*
Preset	0	1	X	X	X	1	0
Clear	1	0	X	X	X	0	1
No change	1	1	X	X	X	Qo	$\overline{Qo}$
No change	1	1	↓	0	0	Qo	$\overline{Qo}$
Reset	1	1	↓	0	1	0	1
Set	1	1	↓	1	0	1	0
Toggle	1	1	↓	1	1	$\overline{Qo}$	Qo



CMOS implementation of JK flip flop



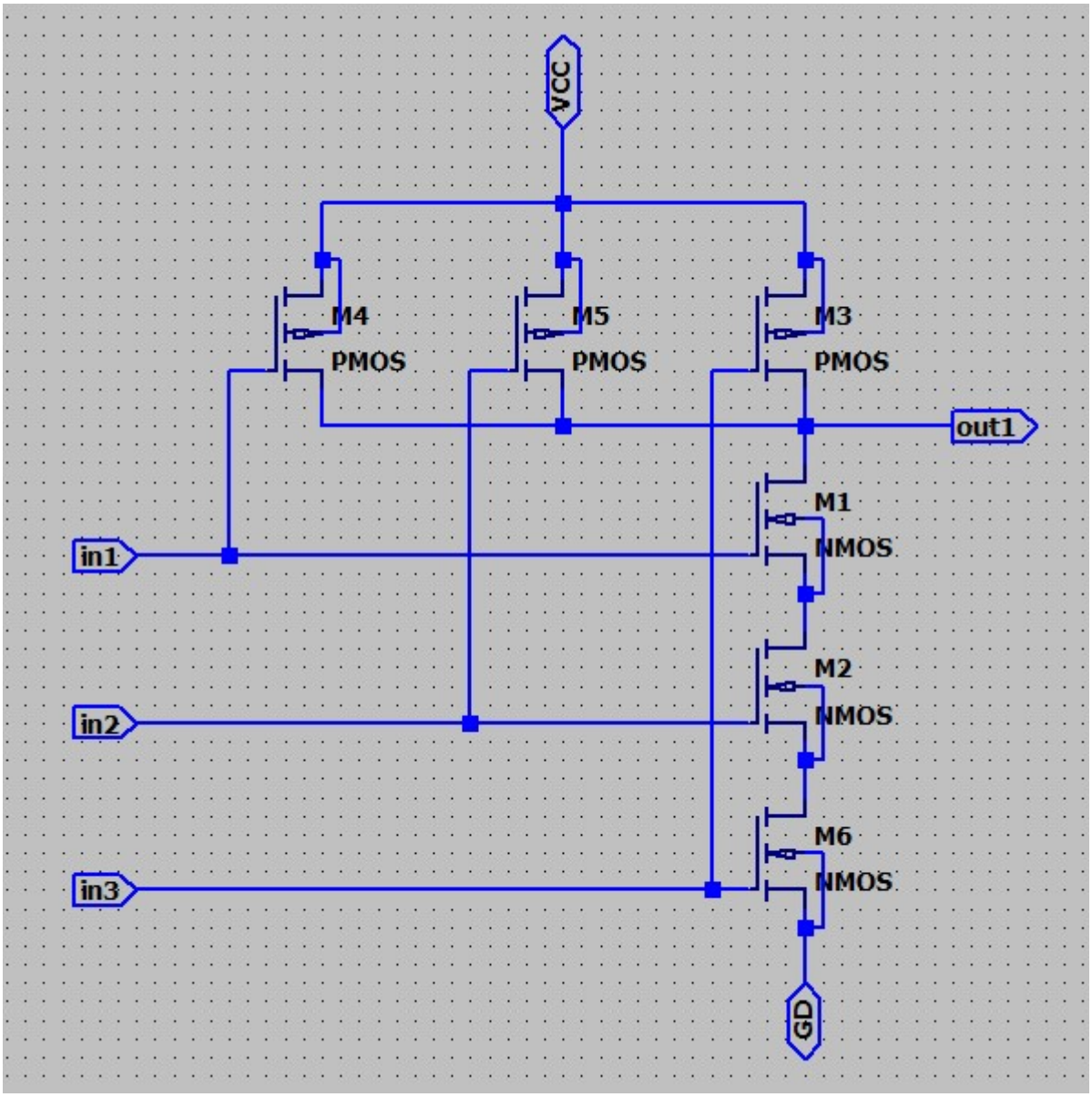


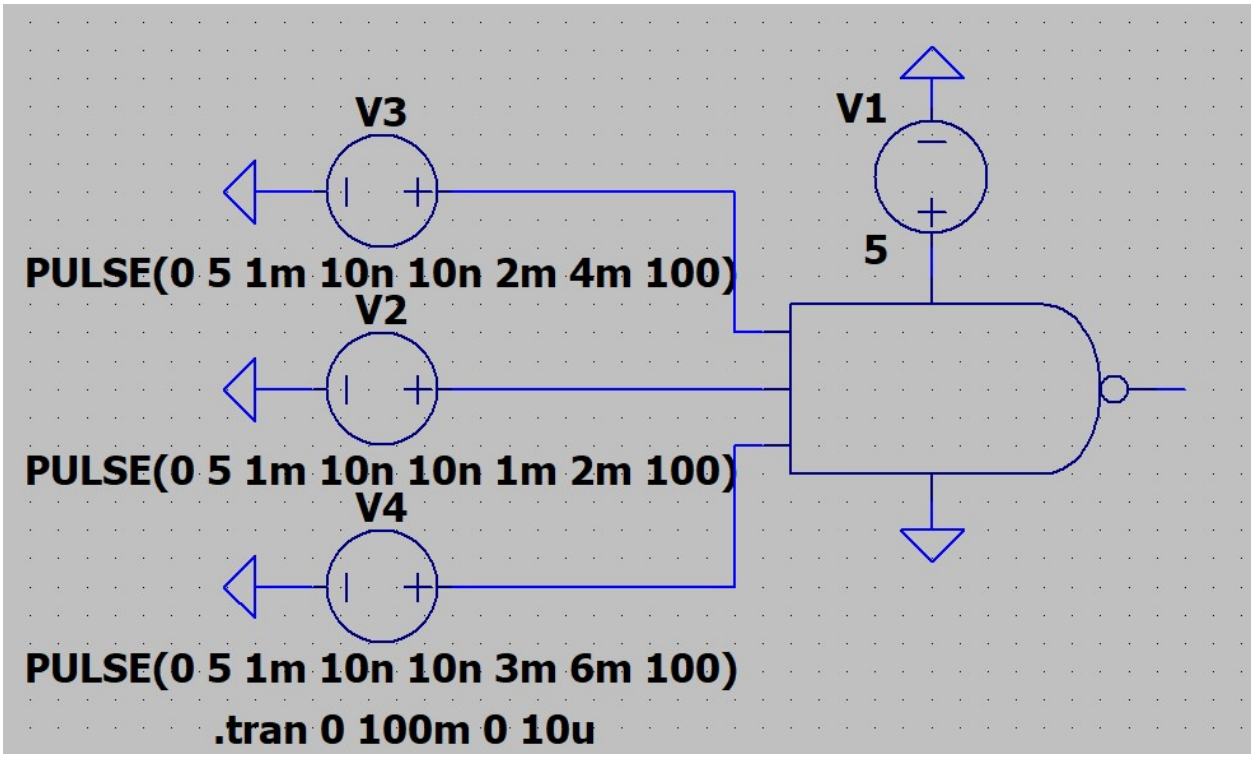
Simulation Error

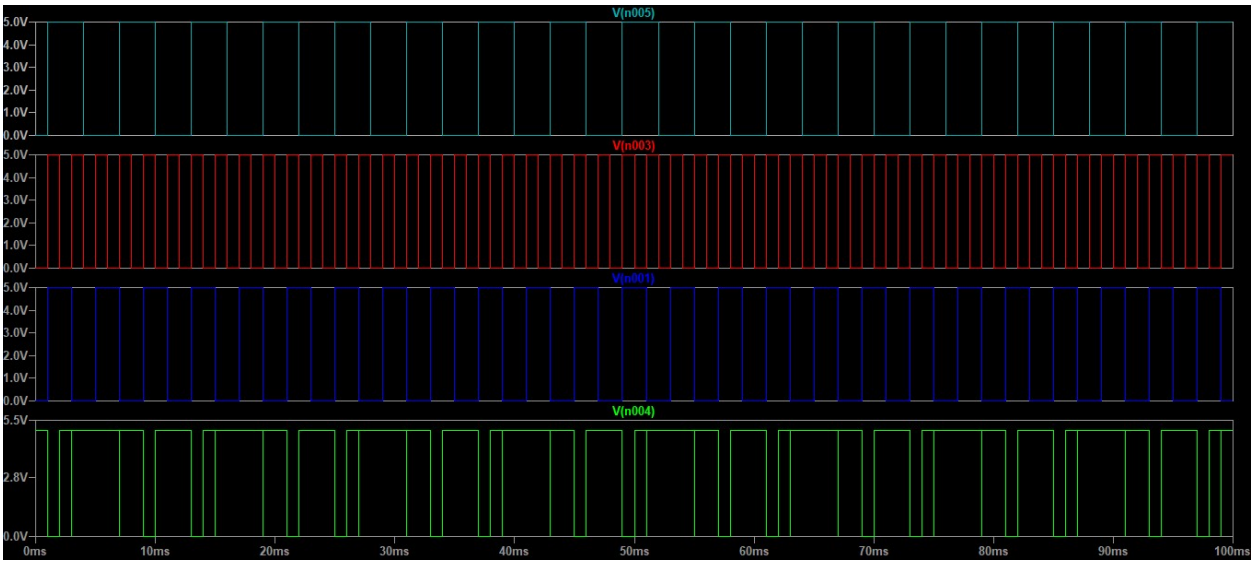
3) Nand

3 Input NAND Gate Truth table

inputs			Outputs
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

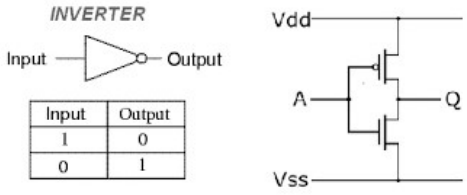

VCC
M4
PMOS
M5
PMOS
M3
PMOS
out1
M1
NMOS
in1
M2
NMOS
in2
M6
NMOS
in3
GD



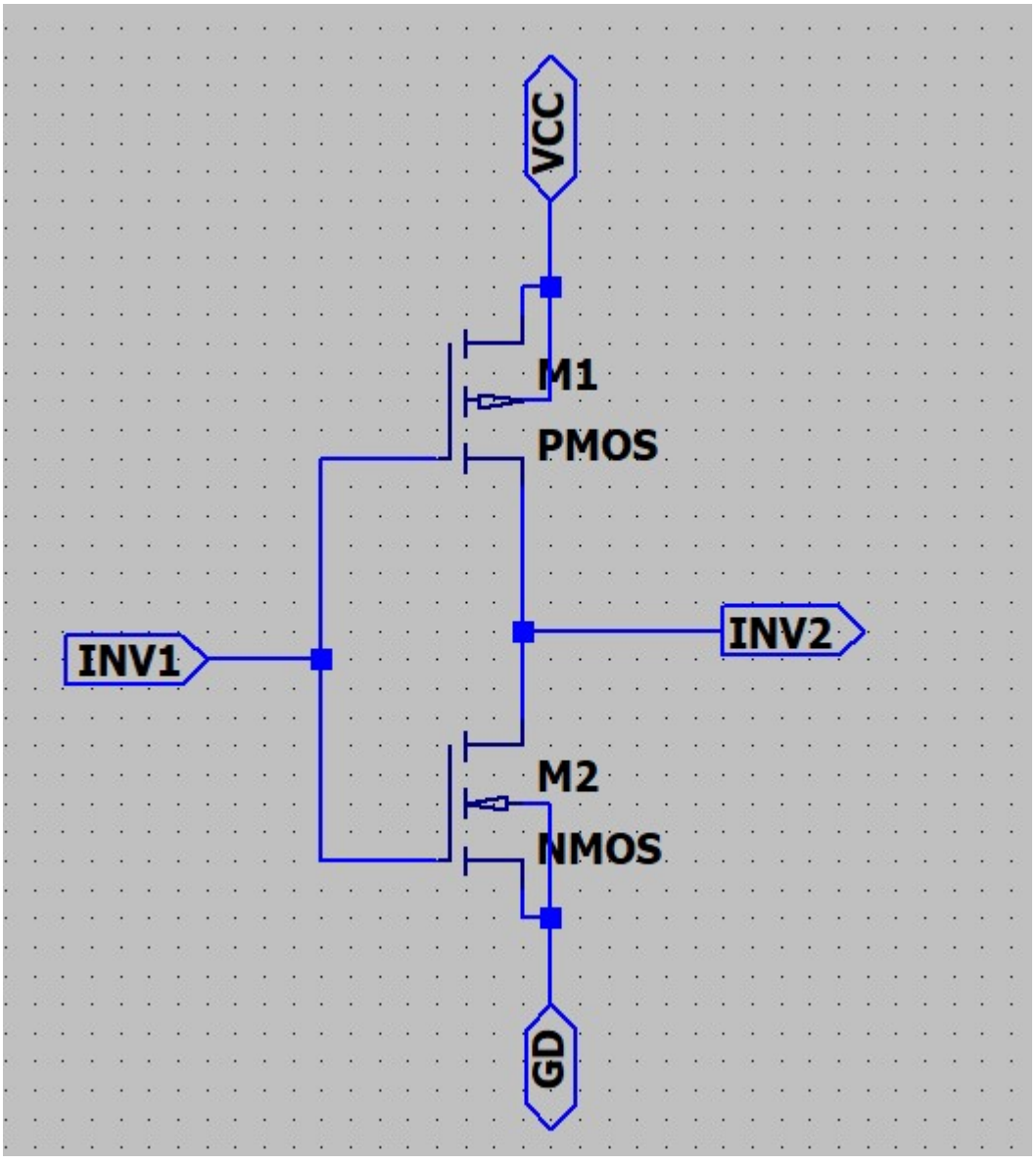


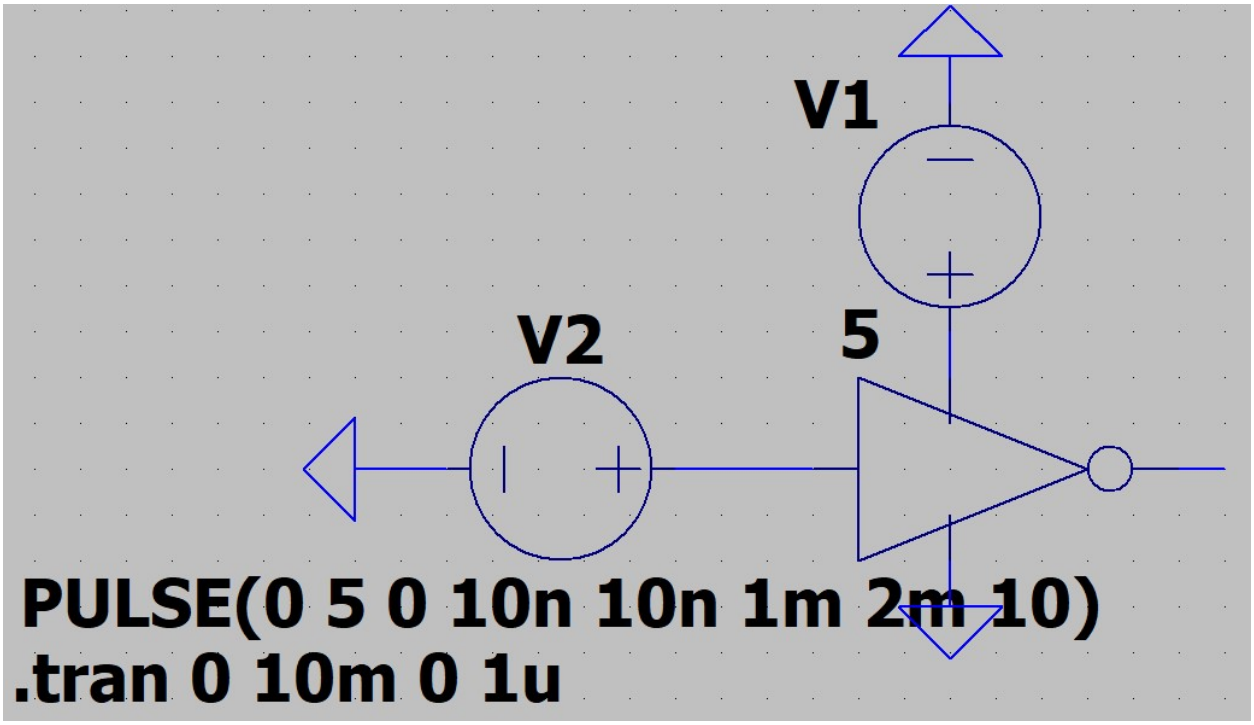
Truth Table Verified

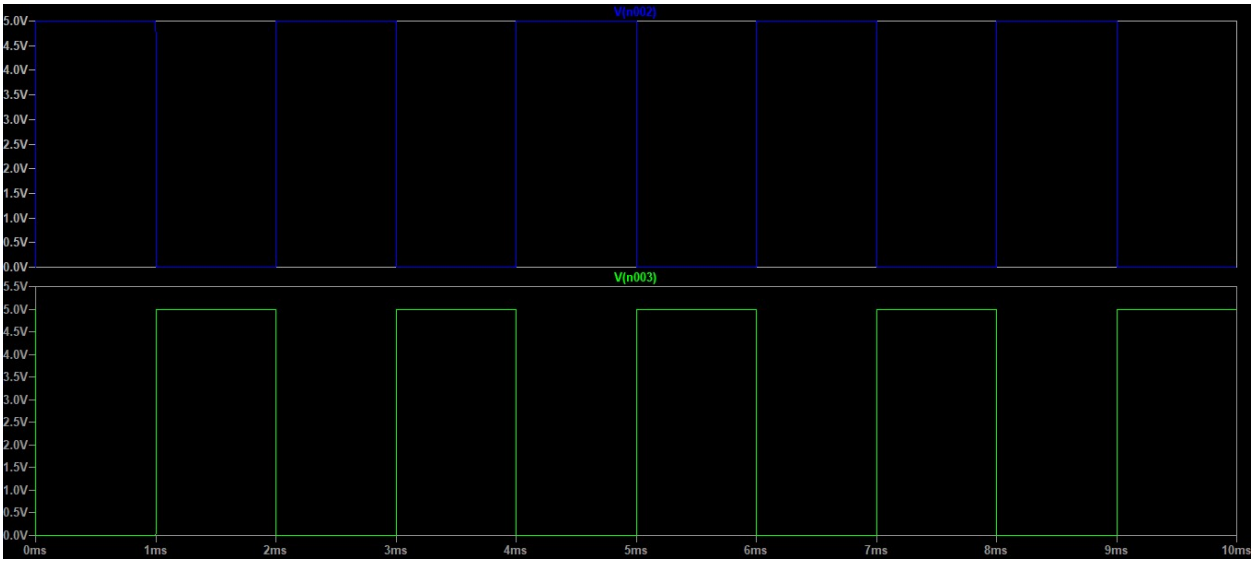
4) Inverter



Input	Output
1	0
0	1







Truth Table Verified

5) Discussion & Conclusion

Inverter schematic, nand schematic was successfully run and verifiet with their truth table.

As this LTSpice design has multiple heirchy cell cascaded with each other. LTSpice couldn't calculate JK FF output. Alternatively, predefined JK ff model in LTSpice Directory can be used to produce 4-bit Asynchronous Counters.

All W/L ratio is set to 1 as cmos design Output voltage doesn't depend on W/L ratio. True for both nmos and pmos.

6) References

- https://www.allaboutcircuits.com/textbook/digital/chpt-11/asynchronous-counters/
- https://www.elprocus.com/cmos-working-principle-and-applications/