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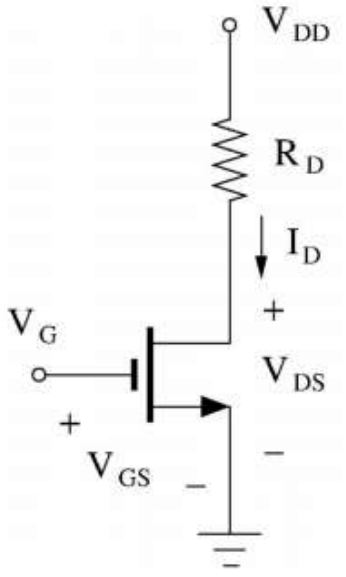
Objective: Design an Analog MOS Amplifier (common-source, single stage) with voltage gain 30dB using a 180nm process with different biasing techniques. Compare performance for each of the design in terms of power consumption, area, frequency response (gain vs frequency) and noise robustness.

Note: The major goal of "Bias" is to ensure that MOS is in saturation at all times. Bias point should be stable (i.e., resilient to variations in µnCox (W/L), Vt, … due to temperature and/or manufacturing variability.) Important parameters are ID and VDS. Bias point impacts the small-signal parameters. Bias point impacts how large a signal can be amplified. Bias point impact power consumption.

The noise sources in MOSFETs include:
(a) thermal noise
introduced by the channel;
(b) flicker noise from the channel;
(c) thermal noise introduced by the polysilicon gate resistance;
(d) thermal noise introduced by the source/drain resistance and
(e) thermal noise introduced by the distributed substrate
resistance.

1) ***Biasing by fixing VGS***

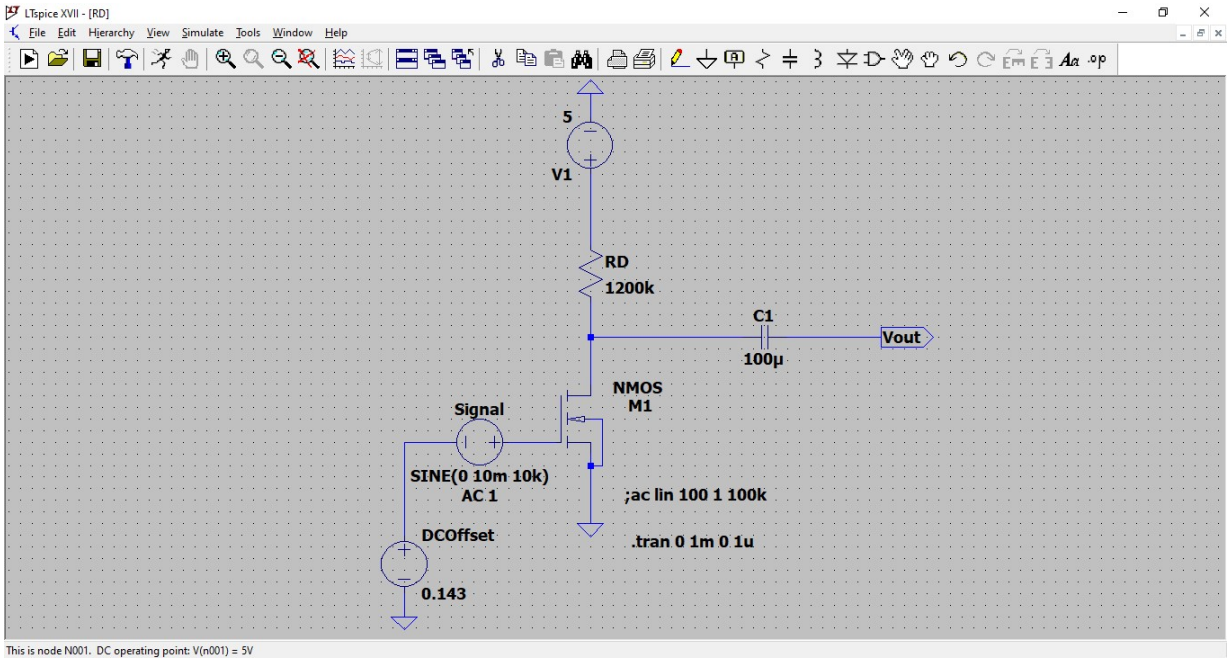
Bias with Gate Voltage



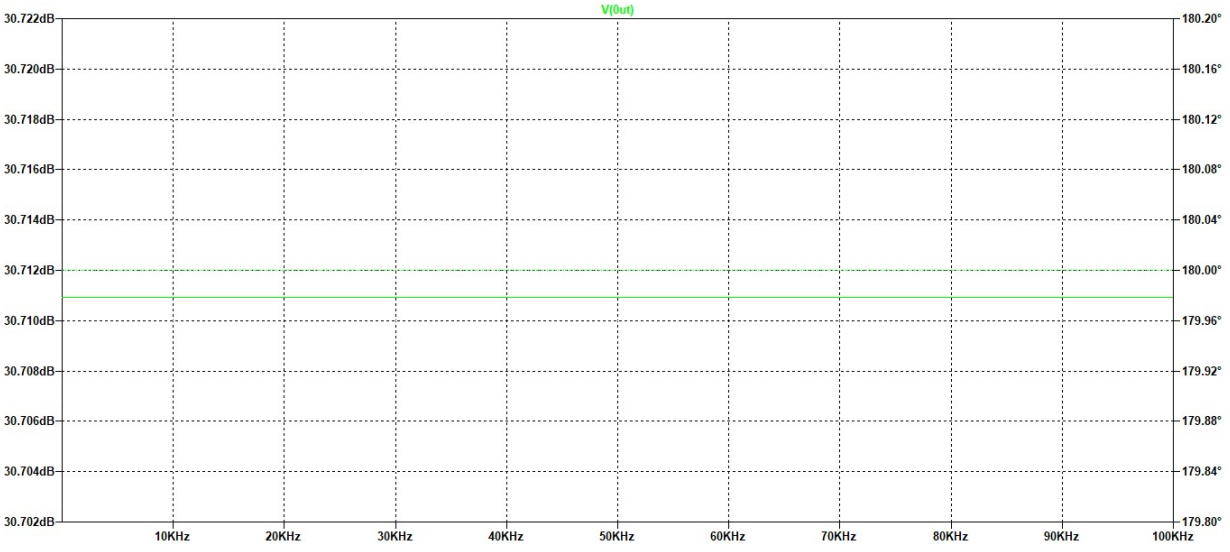
$$I_D = 0.5\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

$$V_{DS} = V_{DD} - I_D R_D$$

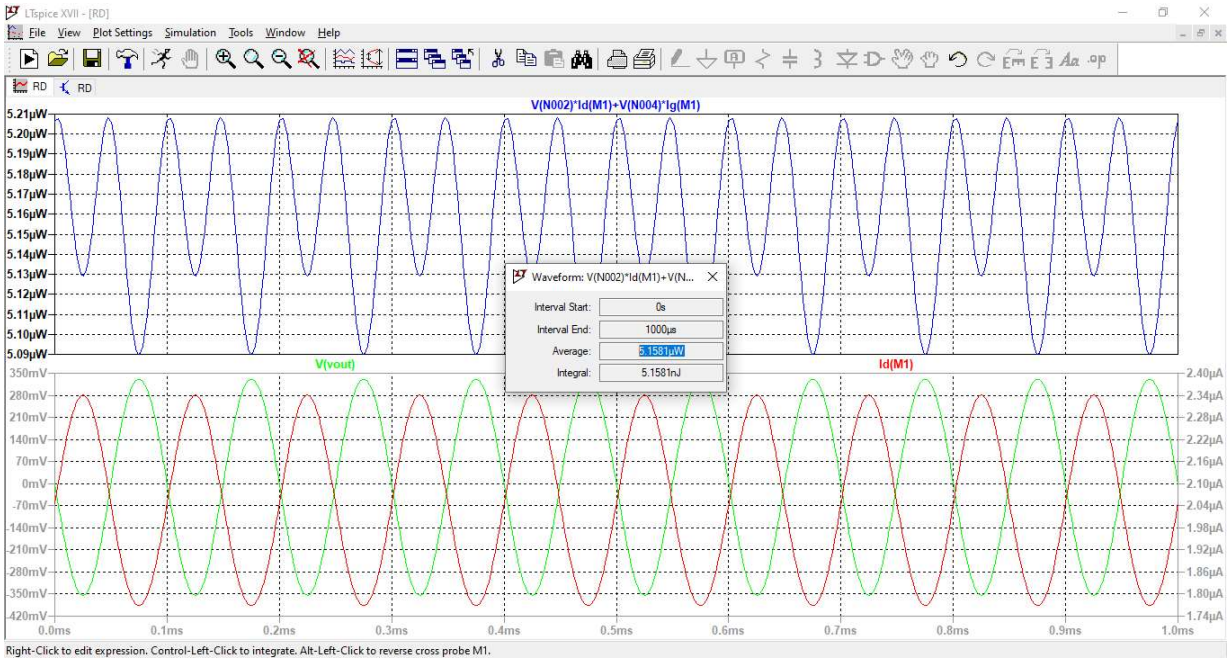
W/L=10



a) Frequency response (gain vs frequency)



b) Power consumption



Power consumption = 5.1581µW

c) Area = 1.5*W*L = 0.486 um square + resistor area + source area

d) Noise Robustness: Susceptible to dc noise

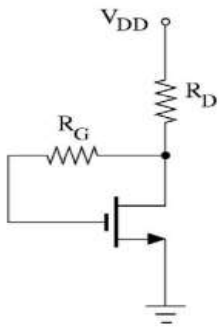
❖ ***Discussion:***

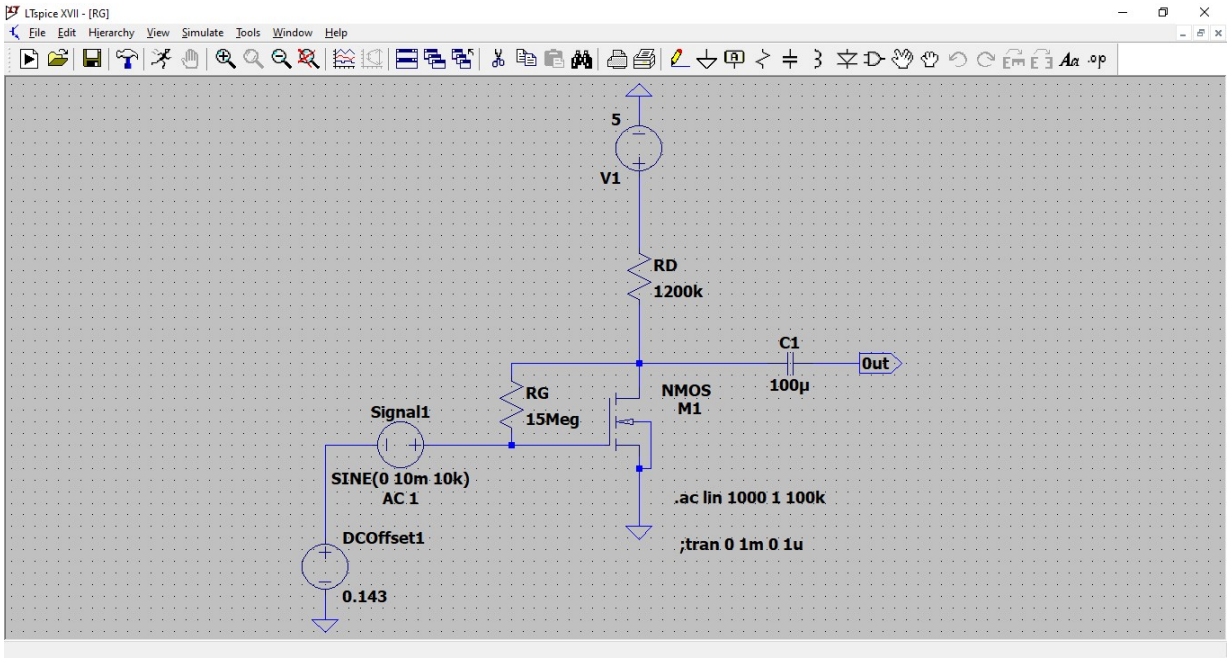
- *This method is NOT desirable as µnCox (W/L) and Vt are not "well-defined." Bias point (i.e., ID and VDS) can change drastically due to temperature and/or manufacturing variability.*

2) *Biasing using a Drain-to-Gate Feedback Resistor*

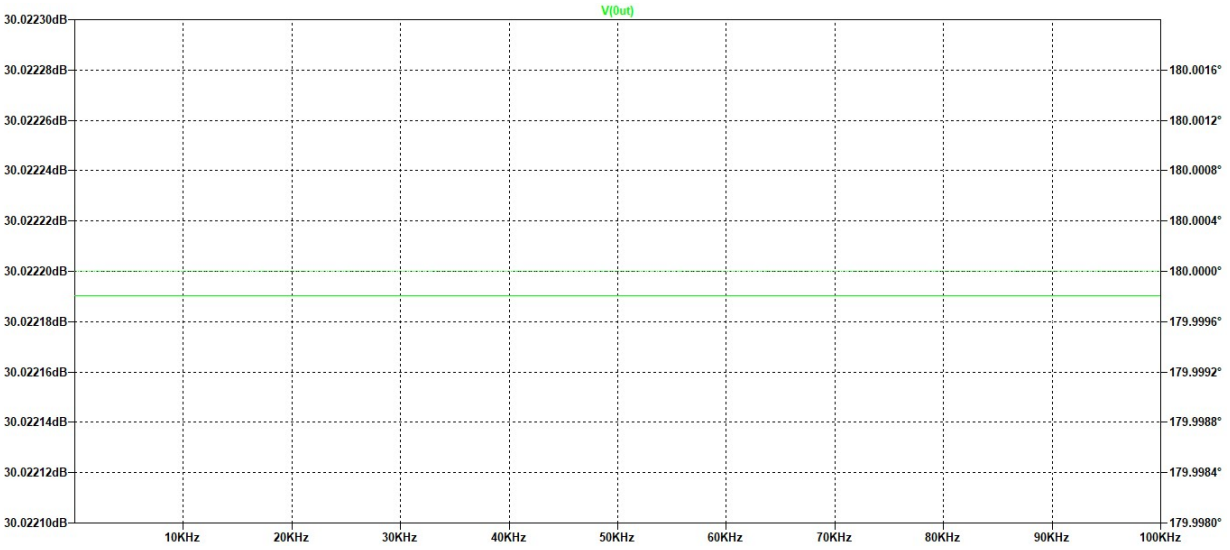
W/L=10

Drain Feedback

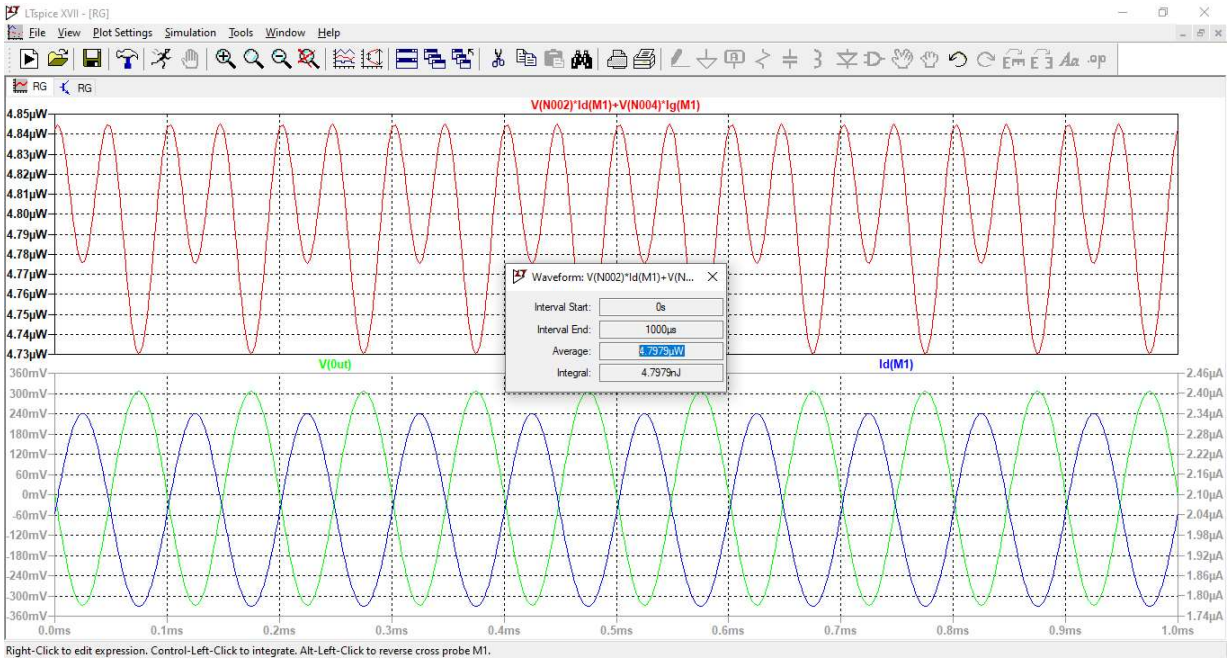




a) Frequency response (gain vs frequency)



b) Power Consumption



Power Consumption=4.7979µW

c) Area = 1.5*W*L = 0.486 um square + resistor area + sources area

d) Noise Robustness: Susceptible to DC noice

❖ ***Discussion:***

- Here the large feedback resistance R_G in, Meg range, forces DC voltage at the Gate to be equal to that at the drain because I_G=0, approximately.

Thus we can write

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D$$

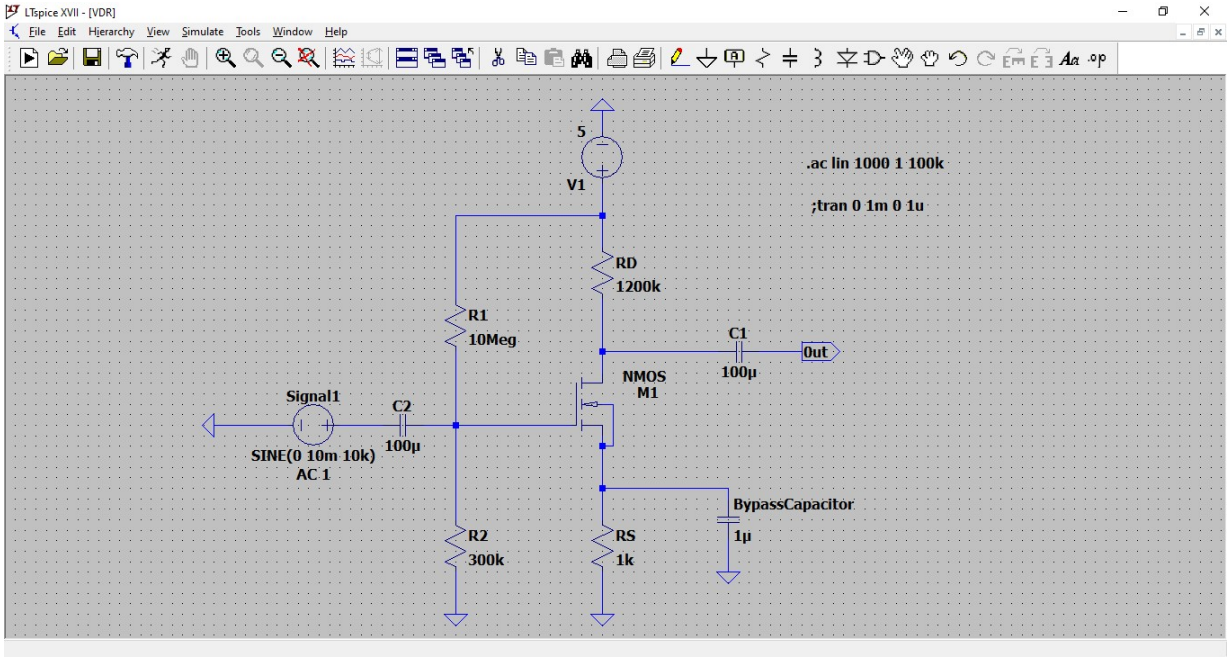
Which can be rewritten in the form

$$V_{DD} = V_{GS} + R_D I_D$$

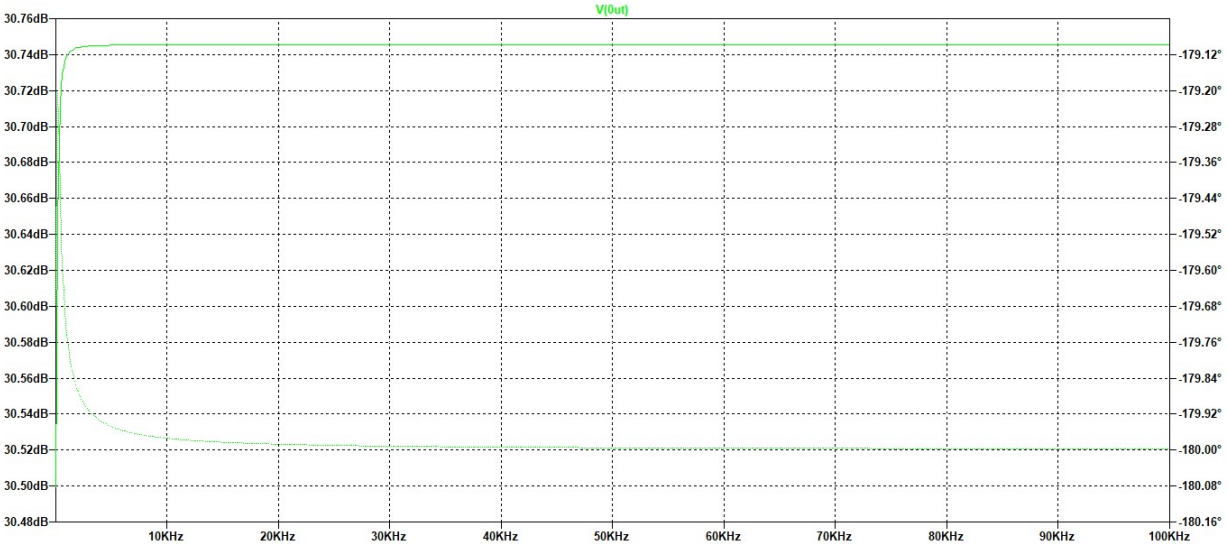
- If I_D increases due to any reason, then V_{GS} must decrease
- The decrease in V_{GS} in turn causes a decrease in I_D
- Thus, the negative feedback by R_G keeps I_D reasonably constant

3) *Biasing by fixing VG and connecting a resistance in the Source* [Degeneration Resistance]

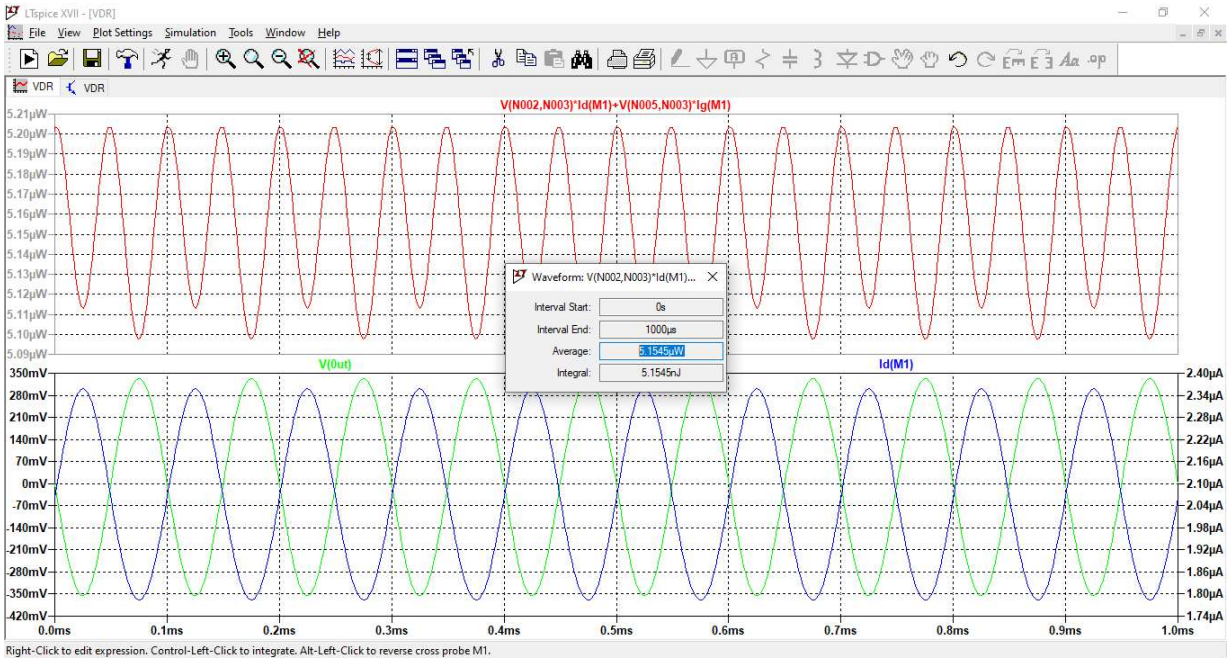
W/L=10



a) Frequency response (gain vs frequency)



b) Power Consumption



Power Consumption = 5.1545µW

c) Area = = 1.5*W*L = 0.486 um square

d) Noise: Due to capacitor coupling, not susceptible to DC noice

❖ Discussion

- Since Ig=0, R1 and R2 are selected to be very large in order to provide higher input gate resistance, and negligible current in the VDR branch such that power dissipation is negligible. Input and output coupling capacitors must be used in order to filter out DC voltage.
- Resistor Rs provides negative feedback which stabilizes the bias current ID.
- ID increases and VG remains constant, hence, VGS will decrease which will further decrease ID.
- Rs works to keep ID as constant as possible.

4) *Biasing Using a Constant-Current Source*

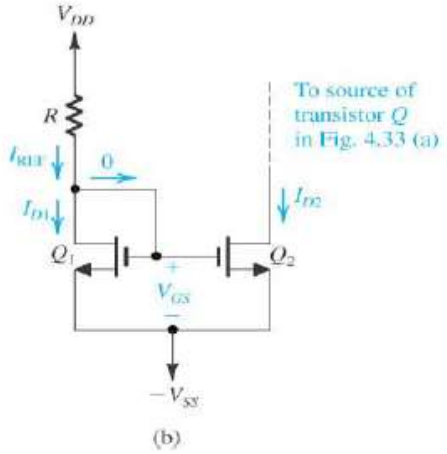
➢ It is often needed to find the value of R in order to achieve a desired IREF

➢ To ensure ID and VDS would not change (e.g., due to temperature variation). One can force ID to be constant using a current source.

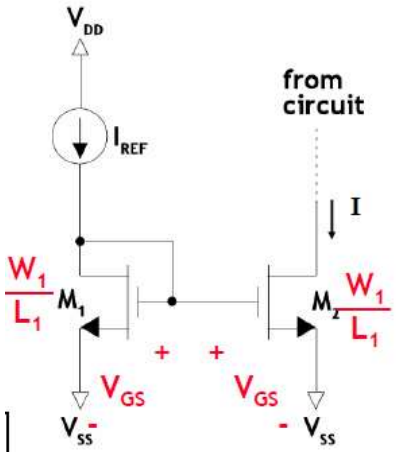
- Designing I_{REF}

$$I_{REF} = \frac{V_{DD} - V_{GS} + V_{SS}}{R}$$

$$I_{REF} = \tfrac{1}{2} k_n' \frac{W_1}{L_1} (V_{GS} - V_t)^2$$



➢ The width and length (the W/L aspect ratio) and the parameters of the two transistors *can be different.* We can choose W/L freely. In this circuit, consider W/L of both MOSFETs are the same and transistors are identical. The Gate-Source voltages are also the same, then

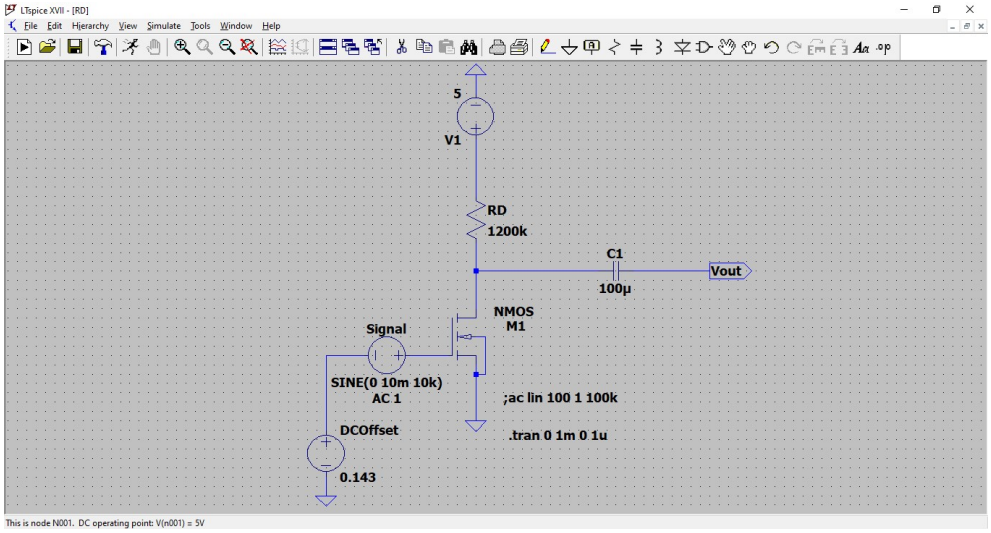


$$I_{REF} = \frac{1}{2} k_n' \frac{W_1}{L_1} (V_{GS} - V_t)^2$$

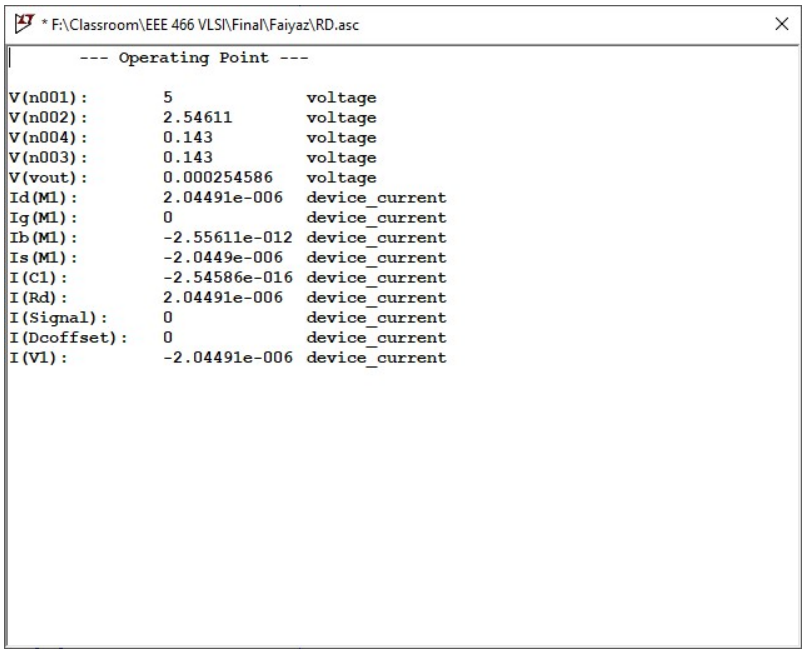
$$I = \frac{1}{2} k_n' \frac{W_1}{L_1} (V_{GS} - V_t)^2$$

- Iref=ID

Using the circuit [**Biasing by Fixing VGS**] below to calculate ID for Q-point,

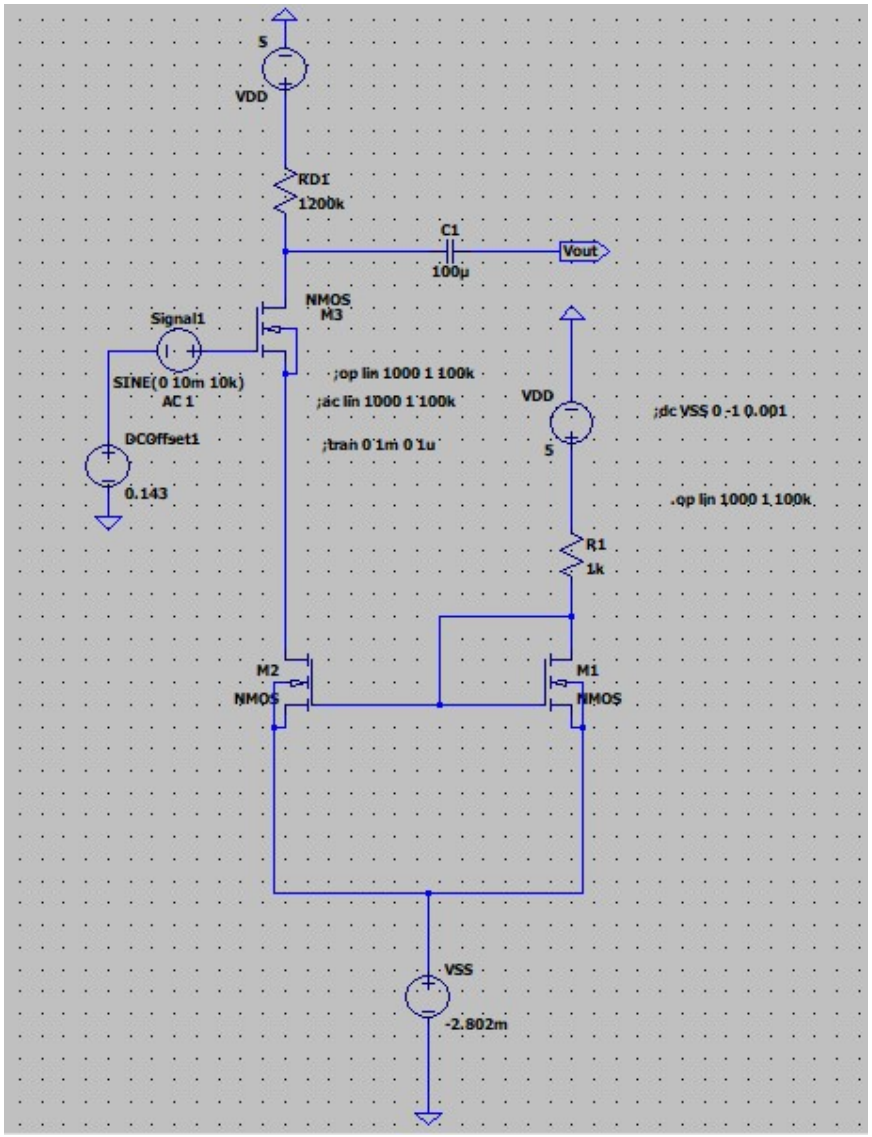


DC Operating Point analysis,



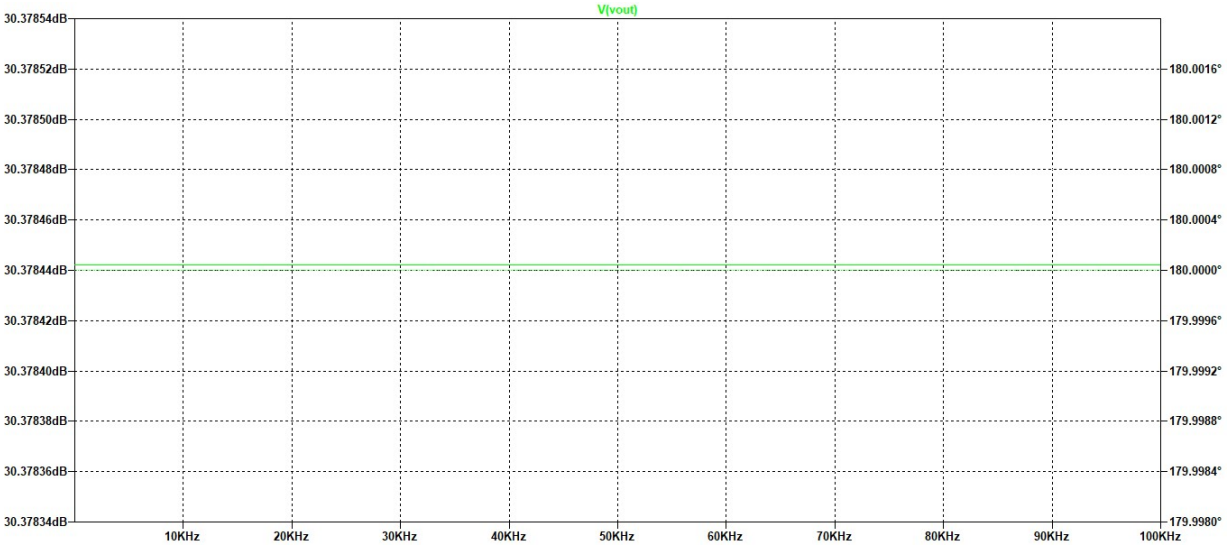
ID = 2.04491 uA

<u>Final circuit [after DC sweeping Vss to find out the right value for which the current source supplies ID at Q-point]:</u>

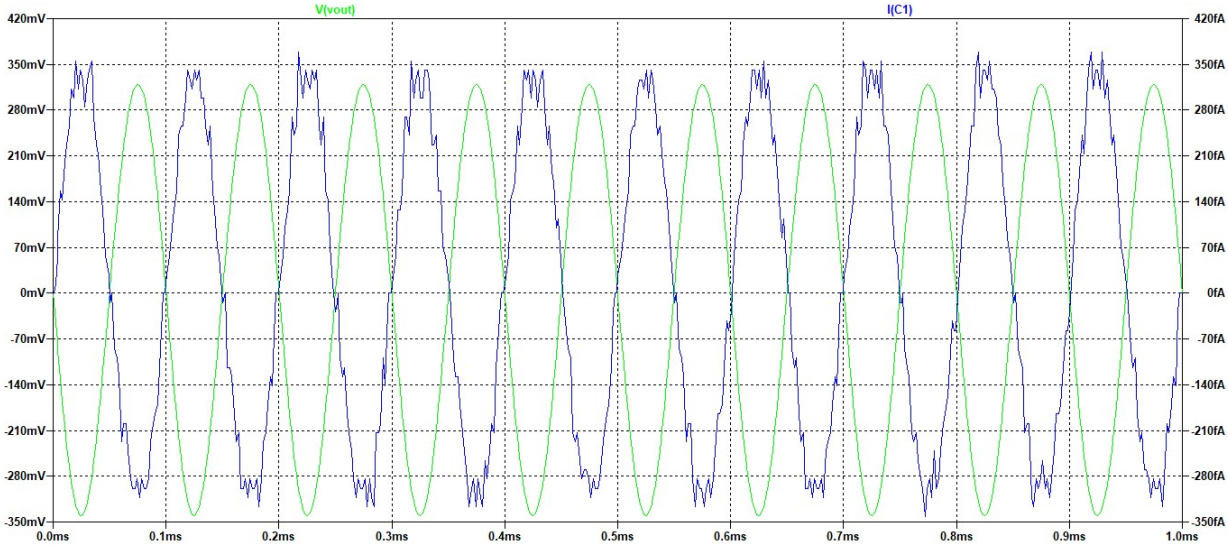


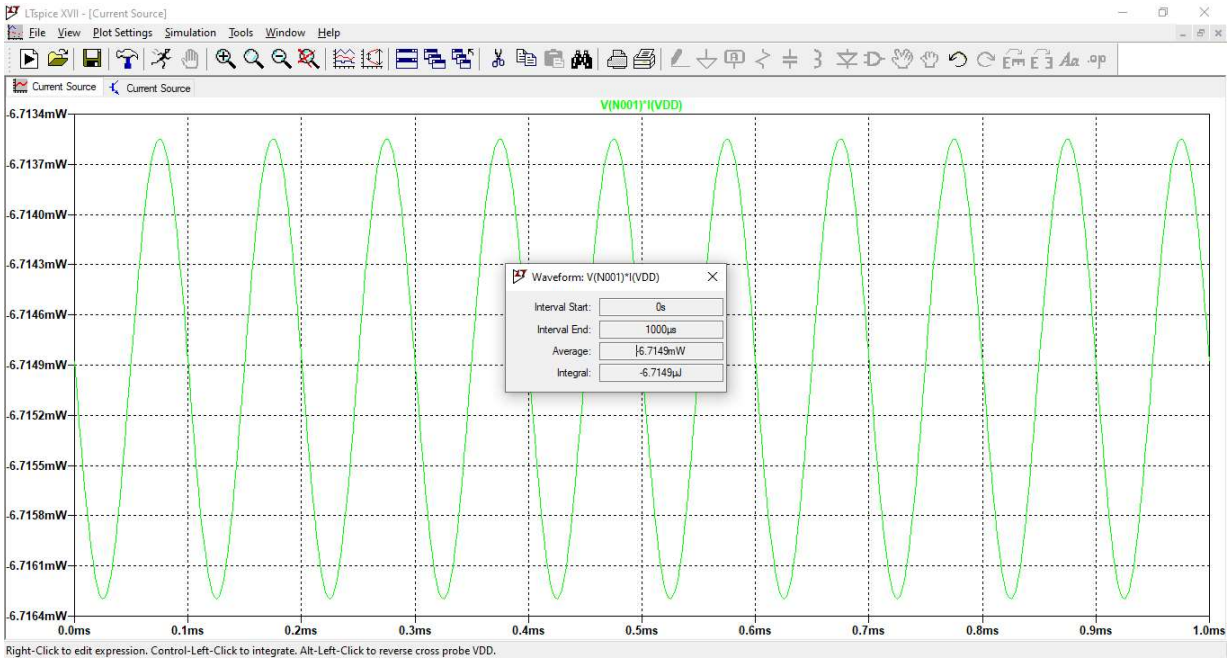
W/L=10 [Same for all Mosfet]

a) Frequency response (gain vs frequency)



b) Power Dissipation





Power Dissipation = 6.7149mW

c) Area = 3*1.5*W*L = 1.458 um square + area of resistors

d) Noise Robustness: Highly susceptible to input DC noise without coupling capacitors

❖ Discussion

- The most effective biasing technique is using a constant current source.
- Resistor RD establishes an appropriate voltage at drain to allow for the required output signal full swing while ensuring that the mosfet remains in the saturation region