Canvas Group Name: Student 1: Student 2:
Student 3:

CMPE110 HA6: DRAM & I/O Detective

Solution

Due Date: Tuesday 03/12/19

1) DRAM Capacity & Bandwidth

Assume a processor with 3 DDR DRAM channels of width 64 bit, operating at 1.4 GHz. All channels support up to 4 ranks of DIMMs. A DIMM contains multiple chips with the following properties. Banks have 8K rows and 256 columns. A DRAM chip has 8 banks and an x4 interface with a burst rate of 16.

Precalculations:

#chip = channel width/interface width = 64 bit / 4 bit = 16 chips

cache line size = channel width * burst size = 64bits * 16 = 128 bytes

Column size = interface width * burst size = 64 bits

a) How many bits does each column store? **(2 Points)**

For bits in a column (for every row buffer) = interface width*burst size = 64bits

b) What is the capacity of a single chip? **(2 Points)**

512Kb*256*8 = 1Gb = 128MB

c) What is the capacity of a DIMM? **(2 Points)**

(1) Assume it's a single-rank DIMM, so we have 4 DIMMs, then:
#chips*cap/chip * (# ranks per DIMM) = 16*1Gb = 16Gb = 2GB

(2) Assume it's a dual-rank DIMM, so we have 2 DIMMs, each of which is:
32Gb = 4GB

(3) Assume it's a quad-rank DIMM, we have 1 DIMMs with:
64Gb = 8GB

d) What is the maximum DRAM capacity supported by the processor? **(2 Points)**

#Channels * (Cap/rank * rank/Channel) = 3*64Gb = 192 Gb = 24GB

e) What is the maximum memory bandwidth that the system supports? **(2 Points)**

Given channel freq:
Data is transferred at EACH clock edge
3 * 64 bit * 1.4GHz * 2 = 537.62 Gbit/s = 67.233.2 GB/s

2) DRAM Bank Controller

Assume that a DRAM bank stores 1 Byte per column, has 4 columns per row and 16 rows per bank. Given an address, the most significant bits encode the bank, the next range of bits encode the row and the least significant bits encode the column. The controller supports one open row per bank.

a) List the bit positions within an address that specify the 3 components: **(3 Points)**

Bank: bit 6th to bit 7th (2 bits)
Row: bit 2nd to bit 5th (4 bits)
Column: bit 0 to bit 1st (2 bits)

b) Given below is a sequence generated by a DRAM controller.

Time	Byte Address (hex)	Write enable (WE)
0	0x40	0
1	0x41	0
2	0x42	1
3	0x3	0
4	0xF	1
5	0x43	0
6	0x3	1
7	0x44	0

Show the sequential sequence of commands (activate, precharge, read, write) as well as the target bank and the address (either a column or a row address) as seen by the bit-cell arrays. Assume a latency of 3 for all commands. Assume that each bank has its own command queue that contains commands that will be issued to it. Assume that all commands above have already been queued. The controller may not reorder commands within a queue. Commands from different queues can be issued and run concurrently, however, only one command can be issued per cycle. The controller can issue a command to a bank while the existing command is being processed so that 2 commands can be executed back to back (without a gap cycle). A command is sent quickly so it begins to be executed within the same cycle. **(8 Points)**

The commands were received in the above order and placed in queues ready to be issued to their respective banks.

Command	Bank	Row **or** column address	Start Cycle	End Cycle
activate	1	0	0	2
activate	0	0	1	3
read	1	0	3	5
read	0	3	4	6
read	1	1	6	8
precharge	0		7	9
write	1	2	9	11
activate	0	3	10	12
read	1	3	12	14
write	0	3	13	15
precharge	1		15	17
precharge	0		16	18
activate	1	1	18	20
activate	0	0	19	21
read	1	0	21	23
write	0	3	22	24

c)What is the overall latency of the access sequence? **(1Point)**

25 cycles