Quiz 2 Solution

In RISC-V, Ld and Sd are

- Memory transfer instructions
- Logic instructions
- Arithmetic instructions
- Control flow changing instructions

The RISC-V ISA we discussed uses 32 general purpose registers. Assume we want to increase the number of registers to 256. To enable this, the machine instruction format of three operand instructions would require:

- 9 more bits
- 3 more bits
- The same number of bits
- 256 bits

How many control flow changing instructions in the assembly code do we need as a minimum to implement the following compiled c-code:

```
if (i == j)
    a = b * c
else
    d = b / c
```

- 2
- 1
- 3
- 4

Consider the following instruction:
Ld x2, offset(x3)
Which of the following statements is correct?

- All three are correct
- The base address is stored in x3
- The destination register is x2
- The offset is an immediate

Consider the execution of the following instruction:
Beq x1, x2, label
Which one of the following statements is correct:

- The code will branch to the address represented by label
- The code will branch to the address stored in x1
- The code will branch to the address stored in x2
- All three are correct