Digital Integrated Circuits

Lab2: Study of Transistor-Transistor Logic Gates

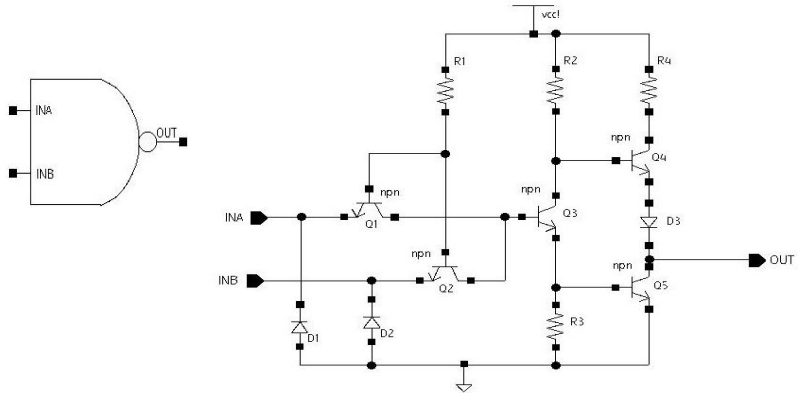
Objective

To study the properties of transistor-transistor logic (TTL) NAND logic cell as well as characteristics and parameters by application of HSpice circuit simulation tool and estimation of its values through calculations.

Laboratory tasks

2.1. TTL NAND logic cell's (NAND02 gate) circuit and input files.

- Build the circuit of TTL NAND logic cell with two inputs based on data of table 3 (Fig.2.1).



INA	INB	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 2.1. The views of TTL NAND logic cell's symbol, electrical circuit, truth table and input and output signal waveforms

- Get the circuit netlist (nmos.netl file) and put it in the following link: /student_lab/digital_ic/variant_val/...
- Input files necessary for simulation.

For input files take:

- Input slope: 50 ps and Output capacitive load value, C_{load}: 5 fF

2.1.1. The input file for defining the input characteristics of NMOS transistor in DC mode by using HSpice circuit simulation tool is listed below:

```
*NNOS Transistor
*Input Characteristics
* HSPICE Netlist
.options POST=1 parhier=local

* Models section
* Include models
.include '/student_lab/digital_ic/all_models/model_val'

* Design variables section
* Define parameters
.param vdd = VDD_val
.temp Temp_val

* Structural netlist section
.include '/student_lab/digital_ic/variant_val/nmos.netl'

vvss vss gnd dc=0
vvdd vdd vss dc='vdd'
```

```
vbulk bulk vss dc=0
vin in vss dc=0
r1 out vdd 1k

* Analysis section
* DC Analyses
.dc vin 0 vdd 0.01
.probe  v(*) i(*)

*Options
.option post probe

.end
```

2.1.2. The input file for defining the output characteristics of NMOS transistor in DC mode by using HSpice circuit simulation tool is listed below:

```
*NNOS Transistor
*Output Characteristics
* HSPICE Netlist
.options POST=1 parhier=local

* Models section
* Include models
.include '/student_lab/digital_ic/all_models/model_val'

* Design variables section
* Define parameters
.param vdd = VDD_val
.temp Temp_val

* Structural netlist section
.include '/student_lab/digital_ic/variant_val/nmos.netl'

vvss vss gnd dc=0
vvdd vdd vss dc='vdd'
vbulk bulk vss dc=0
vin in vss dc=0
r1 out vdd 1k

* Analysis section
* DC Analyses
.dc vout 0 vdd 0.01 sweep  vin 0 vdd 0.1
.probe  v(*) i(*)

*Options
.option post probe
.end
```

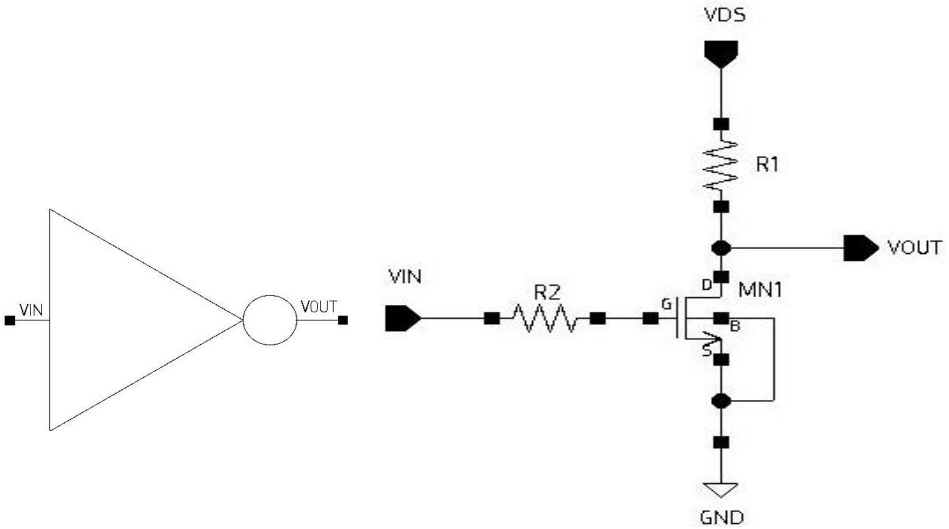
2.1.3. The input file for measuring the delays of NMOS transistor in transition mode by using HSpice circuit simulation tool is listed below:

```
*NMOS Transistor
*Propagation Delay, Transition Time
* HSPICE Netlist
.options POST=1 parhier=local

* Models section
* Include models
.include '/student_lab/digital_ic/all_models/model_val'
```

```
* Design variables section
* Define parameters
.param vdd = VDD_val
.param tr=TR_val
.param freq=FREQ_val
.param per='1/freq'
.param tst='0.5*per'
.temp Temp_val

* Structural netlist section
.include '/student_lab/digital_ic/variant_val/nmos.netl'

vss vss gnd! dc=0
vdd vdd gnd! dc=vdd
vbulk bulk 0 0
vin in gnd dc=0 pwl ( 0 0 'tst' 0 'tst+tr' vdd )
cload out 0 LOAD_val

* Analysis section
* Transient Analyses
.tran '0.01*tr' '2*per'
.probe  v(*)

*Options
.option post probe

.ic v(out)=vdd
*Measures
*Propagation Delay
.meas tran tphl trig v(in) val='0.5*vdd' rise=1 targ v(out) val='0.5*vdd' fall=1
*Transition Time
.meas tran tthl trig v(out) val='0.9*vdd' fall=1 targ v(out) val='0.1*vdd' fall=1


.end
```

2.2. Characteristics of Passive Load RTL NMOS Inverter(RTL_IVN _P)

- Build the circuit for studying passive load RTL NMOS inverter characteristics based on data of table 1 (Fig.1.2).



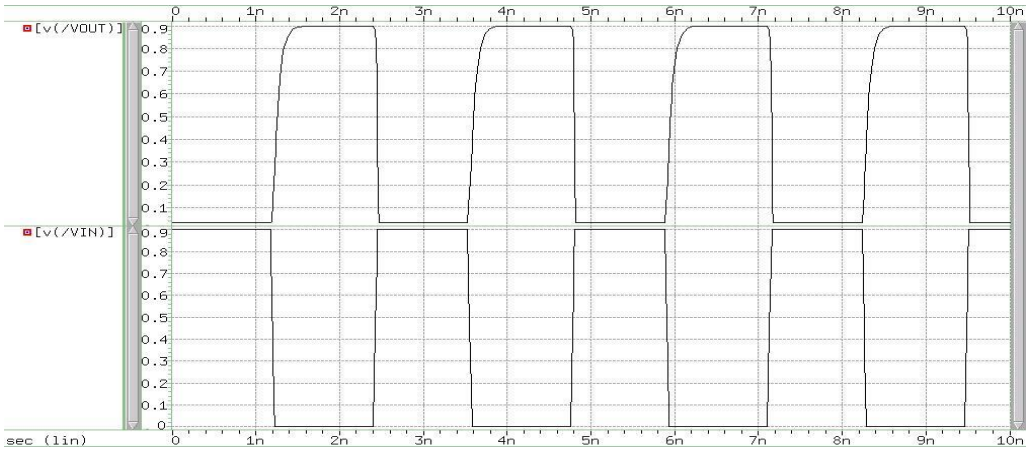


Fig. 1.2. Passive load RTL NMOS inverter symbol, electrical circuit, input and output signal waveforms

- Get the netlist of the circuit (rtl_inv_p.netl file) and put it in the following link: /student_lab/digital_ic/variant_val/...
- Input files necessary for simulation.

For input files take:

- Input slope: 50 ps and Output capacitive load value, C_{load}: 5 fF

2.2.1. The input file for measuring the switching point voltage level for passive load RTL NMOS inverter in DC mode by using HSpice circuit simulation tool is listed below:

```
* RTL_INV_P
*Threshold Voltage
* HSPICE Netlist
.options POST=1 parhier=local

* Models section
* Include models
.include '/student_lab/digital_ic/all_models/model_val'

* Design variables section
* Define parameters
.param vdd = VDD_val
.temp Temp_val

* Structural netlist section
.include '/student_lab/digital_ic/variant_val/rtl_inv_p.netl'
vvss vss gnd dc=0
vvdd vdd gnd dc='vdd'
vin in vss dc=0
cload vout gnd LOAD_val

* Analysis section
* DC Analyses
.dc vin 0 vdd 0.01
.probe  v(*) i(*)

*Measures
.meas dc vthr_in_vout find v(in) when v(in)=v(vout) td=0.1

*Options
.option post probe
```

```
.option autostop

.end
```

2.2.2. The input file for measuring the delays for passive load RTL NMOS inverter in transition mode by using HSpice circuit simulation tool is listed below:

```
* RTL_INV_P
*Propagation Delay, Transition Time
* HSPICE Netlist
.options POST=1 parhier=local

* Models section
* Include models
.include '/student_lab/digital_ic/all_models/model_val'

* Design variables section
* Define parameters
.param vdd = VDD_val
.param tr=TR_val
.param freq=FREQ_val
.param per='1/freq'
.param tst='0.5*per'
.temp Temp_val

* Structural netlist section
.include '/student_lab/digital_ic/variant_val/rtl_inv_p.netl '

vvss vss gnd dc=0
vvdd vdd gnd dc='vdd'
vin in vss pulse vdd 0 'tst+0.0*per' tr tr '0.5*per-tr' '3.0*per'
cload vout gnd LOAD_val

* Analysis section
* Transient Analyses
.tran '0.01*tr' '5*per'
.probe  v(*)

*Measures
***Propagation Delay
.meas tran tplh_in_ vout trig v(in) val='0.5*vdd' fall=1 targ v(vout) val='0.5*vdd' rise=1
.meas tran tphl_in_ vout trig v(in) val='0.5*vdd' rise=1 targ v(vout) val='0.5*vdd' fall=1
***Transition Time
.meas tran ttlh_in_ vout trig v(vout) val='0.1*vdd' rise=1 targ v(vout) val='0.9*vdd' rise=1
.meas tran tthl_in_ vout trig v(vout) val='0.9*vdd' fall=1 targ v(vout) val='0.1*vdd' fall=1

*Options
.option post probe
.option autostop

.end
```

2.3. Characteristics of Active Load RTL NMOS Inverter (RTL_IVN _A)

- Build the circuit for studying active load RTL NMOS inverter's characteristics based on data of table 1 (Fig.1.3).

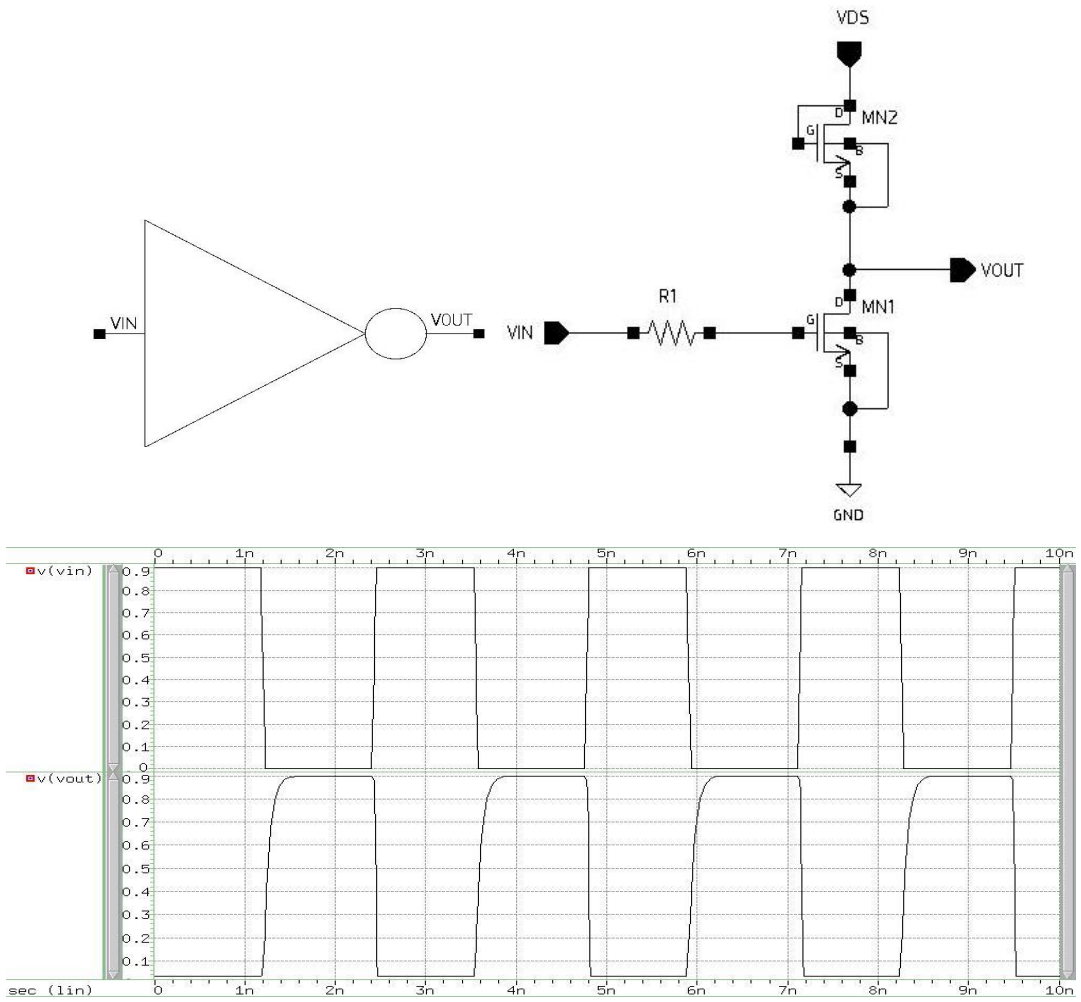


Fig. 1.3. Active load RTL NMOS inverter's symbol, electrical circuit, input and output signal waveforms

Get the netlist of the circuit (rtl_inv_a.netl file) and put it in the following link: /student_lab/digital_ic/variant_val/...

- Input files necessary for simulation.

For input files take:

- Input slope: 50 ps and Output capacitive load value C_{load}: 5 fF

2.2.3. The input file for measuring the the switching point voltage level for active load RTL NMOS inverter in DC mode by using HSpice circuit simulation tool is listed below:

```
* RTL_INV_A
*Threshold Voltage
* HSPICE Netlist
.options POST=1 parhier=local

* Models section
* Include models
.include '/student_lab/digital_ic/all_models/model_val'

* Design variables section
* Define parameters
.param vdd = VDD_val
```

```
.temp Temp_val

* Structural netlist section
.include '/student_lab/digital_ic/variant_val/ rtl_inv_a.netl'

vvss vss gnd dc=0
vvdd vdd gnd dc='vdd'
vin in vss dc=0
cload vout gnd LOAD_val

* Analysis section
* DC Analyses
.dc vin 0 vdd 0.01
.probe  v(*) i(*)

*Measures
.meas dc vthr_in_vout find v(in) when v(in)=v(vout) td=0.1

*Options
.option post probe
.option autostop

.end
```

2.2.4. The input file for measuring the delays for an active load RTL NMOS inverter in transition mode by using HSpice circuit simulation tool is listed below:

```
*RTL_INV_A
   *Propagation Delay, Transition Time
* HSPICE Netlist
.options POST=1 parhier=local

* Models section
* Include models
.include '/student_lab/digital_ic/all_models/model_val'

* Design variables section
* Define parameters
.param vdd = VDD_val
.param tr=TR_val
.param freq=FREQ_val
.param per='1/freq'
.param tst='0.5*per'
.temp Temp_val

* Structural netlist section
.include '/student_lab/digital_ic/variant_val/ rtl_inv_a.netl'

vvss vss gnd dc=0
vvdd vdd gnd dc='vdd'
vin in vss pulse vdd 0 ‘tst+0.0*per’ tr tr ‘0.5*per-tr’ ‘3.0*per’
cload vout gnd LOAD_val

* Analysis section
* Transient Analyses
.tran ‘0.01*tr’ ‘5*per’
.probe  v(*)

*Measures
***Propagation Delay
.meas tran tplh_in_ vout trig v(in) val='0.5*vdd' fall=1 targ v(vout) val='0.5*vdd' rise=1
.meas tran tphl_in_ vout trig v(in) val='0.5*vdd' rise=1 targ v(vout) val='0.5*vdd' fall=1
```

```
***Transition Time
.meas tran ttlh_in_ vout trig v(vout) val='0.1*vdd' rise=1 targ v(vout) val='0.9*vdd' rise=1
.meas tran tthl_in_ vout trig v(vout) val='0.9*vdd' fall=1 targ v(vout) val='0.1*vdd' fall=1

*Options
.option post probe
.option autostop

.end
```

Steps to Perform the Lab Exercise

3.1. Simulation of NMOS Transistor

In DC mode:

a. Get transistor input characteristics (I_D=f (VGS)) by giving 0 to VDD_val voltage values to the input. Also simultaneously change the transistor bulk voltage from 0 to VDD_val,
b. Get transistor output characteristics (I_D=f (VDS)) by giving 0 to VDD_val voltage values to the output. Also simultaneously change the transistor input voltage from 0 to VDD_val.

In transition mode:

a. Get input and output signal waveforms.
b. Measure t_{PHL} delay (Refer Table 9, point 4).
c. Measure t_{THL} delay (Refer Table 9, point 2).

3.2. Simulation of Passive Load RTL NMOS Inverter.

In DC mode:

a. Get voltage transfer characteristics by giving 0 to VDD_val voltage values to the input (Refer Table 8, point 1) when
    1) LOAD_val = 0
    2) LOAD_val = C_{load}
b. Measure switching point voltage (Refer Table 8, point 4) when
    1) LOAD_val = 0
    2) LOAD_val = C_{load}

In transition mode:

a. get input and output signal waveforms when
    1) LOAD_val = 0
    2) LOAD_val = C_{load}
b. Measure t_{PHL} and t_{PLH} delays and their average values (t_P=(t_{PHL}+ t_{PLH})/2) (Refer Table 9, points 3, 4) when
    1) LOAD_val = 0
    2) LOAD_val = C_{load}
c. Measure t_{THL} and t_{TLH} delays and their average values (t_T=(t_{THL}+ t_{TLH})/2) (Refer Table 9, points 1, 2) when
    1) LOAD_val = 0
    2) LOAD_val = C_{load}

3.3. Simulation of Active Load RTL NMOS Inverter

In DC mode:

a. Get voltage transfer characteristics by giving 0 to VDD_val voltage values to the input (Refer Table 8, points 1) when
    1) LOAD_val = 0
    2) LOAD_val = C_{load}
b. Measure switching point voltage (Refer Table 8, point 4) when
    1) LOAD_val = 0
    2) LOAD_val = C_{load}

In transition mode:

c. Get input and output signal waveforms when
    1) LOAD_val = 0

2) LOAD_val = C_{load}

d. Measure t_{PHL} and t_{PLH} delays and their average values ($t_P=(t_{PHL}+ t_{PLH})/2$) (Table 9, points 3, 4) when
   1) LOAD_val = 0
   2) LOAD_val = C_{load}
e. Measure t_{THL} and t_{TLH} delays and their average values ($t_T=(t_{THL}+ t_{TLH})/2$) (Table 9, points 1, 2) when
   1) LOAD_val = 0
   2) LOAD_val = C_{load}

Processing the Results Obtained in the Laboratory Exercise

4.1. NMOS Transistor

- Using Table 6 (T_{ox}, ε_{ox}, L, W, V_{T0}, μ_n) calculate the parameters of NMOS transistor:

$$kp_n = \mu_n \cdot \frac{\varepsilon_{ox}}{t_{ox}} \qquad \beta_n = kp_n \cdot \frac{W_n}{L_n} \qquad Coxn = \frac{\varepsilon_{ox}}{t_{ox}} \cdot W_n \cdot L_n \qquad R_n = \frac{VDD}{\frac{kp_n}{2} \cdot \frac{W_n}{L_n} \cdot (VDD - V_{THN})^2},$$

- Take the data necessary for calculations from Table 6.
- Fill in the results measured from simulation in Table 7.

Report

The lab report should include:

1. Studied circuits;
2. Texts from input files;
3. Calculated characteristics and parameters of circuits;
4. Characteristics obtained from simulation;
5. Results obtained from the exercise;
6. Brief summary.