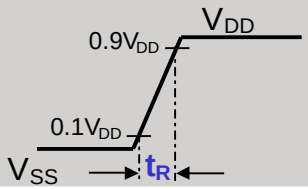
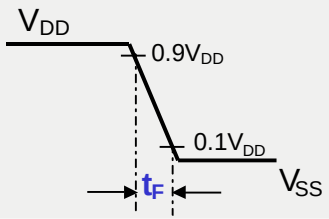
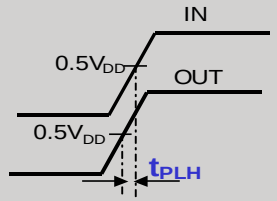
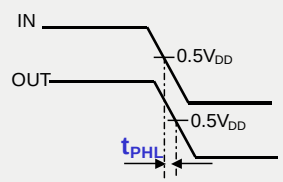
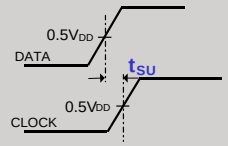
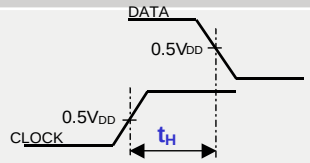
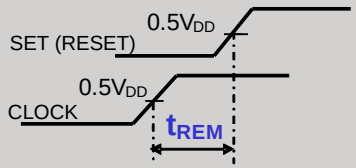
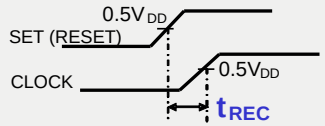
Timing Group Names

N	Parameter	Unit	Symbol	Figure	Definition
1.	Rise transition time rise_transition	ns	t_R		The time it takes a driving pin to make a transition from kV_{DD} to $(1-k)V_{DD}$ value. Usually k=0.1 (also possible k=0.2, 0.3, etc)
2.	Fall transition time fall_transition	ns	t_F		The time it takes a driving pin to make a transition from $(1-k)V_{DD}$ to kV_{DD} value. Usually k=0.1 (also possible k=0.2, 0.3, etc)
3.	Propagation delay low-to-high (rise) cell_rise	ns	t_{PLH} (t_{PR})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DD}$ when the output signal is changing from low to high
4.	Propagation delay high-to-low (Fall) cell_fall	ns	t_{PHL} (t_{PF})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DD}$ when the output signal is changing from high to low

© 2023 All rights reserved..

Timing Constraints: Timing Types

Setup/Hold, Recovery/Removal Constraints

N	Parameter	Unit	Symbol	Figure	Definition
1	Setup time (only for flip-flops or latches) setup_rising setup_falling	ns	t_{SU}		The minimum period in which the input data to a flip-flop or a latch must be stable before the active edge of the clock occurs
2	Hold time (only for flip-flops or latches) hold_rising hold_falling	ns	t_H		The minimum period in which the input data to a flip-flop or a latch must remain stable after the active edge of the clock has occurred
3	Removal time (only for asynchronous Set or Reset) removal_rising, removal_falling	ns	t_{REM}		The minimum time in which the asynchronous Set or Reset pin to a flip-flop or latch must remain enabled after the active edge of the clock has occurred
4	Recovery time (only for asynchronous Set or Reset) recovery_rising, recovery_falling	ns	t_{REC}		The minimum time in which Set or Reset must be held stable after being deasserted before next active edge of the clock occurs

© 2023 All rights reserved..