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| ĐẠI HỌC KHOA HỌC TỰ NHIÊN TP.HCM  **KHOA ĐIỆN TỬ-VIỄN THÔNG** | Môn: **KỸ THUẬT MẠCH ĐIỆN TỬ**  Năm học 2022-2023  Học kỳ II |

**BÁO CÁO ĐỒ ÁN : BITCELL 6T**

**Giáo viên hướng dẫn: Nguyễn Thị Thiên Trang**

**Group: 9**

**List member:**

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| --- | --- | --- |
| **Họ và tên** | **MSSV** |  |
| 20200145 | LÊ ĐỨC CHUNG | Leader |
| 20200374 | NGUYỄN QUỐC TRIỆU | Member |
| 20200426 | HUỲNH PHƯỚC XUYÊN | Member |
| 20200391 | TRƯƠNG CÔNG TRƯỜNG | Member |
| 20200251 | VÕ THÀNH LỘC | Member |

**Plan Form:**

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| **Task** | **Person in charge** |  |
| Features, meaning of the design( đặc điểm ý nghĩa của mạch) | Quốc Triệu |  |
| Circuit diagram & operational analysis (sơ đồ mạch và phân tích nguyên lý hoạt động) | Phước Xuyên, Công Trường |  |
| Parameter calculation in theory (tính toán các thông số của mạch lý thuyết) | Đức Chung, Thành Lộc |  |
| Set up measurement file with HSPICE tool (set up các thông số đo đạc với HSPICE) |  |  |
| Study the PDK 14 nm (nghiên cứu PDK 14nm) |  |  |
| Stick diagram |  |  |
| Schematic design |  |  |
| Pre-layout Simulation |  |  |
| Physical design |  |  |
| Check DRC & LVS |  |  |
| Parasitic Extraction |  |  |
| Post-layout simulation |  |  |

1. **Features, meaning of the design**

The Bitcell 6T circuit is a type of circuit that stores data in RAM (Random Access Memory) memory. This circuit is called "6T" because it consists of 6 transistors, arranged in a symmetrical pair to create a "cell" or "memory cell" that stores one bit of information.

The characteristics and significance of the Bitcell 6T circuit include:

* 1. Features:

• Includes 6 transistors: 4 transistors are used to create a symmetrical pair and 2 transistors to control read/write mode.

• Small size, low power consumption, fast access time.

* 1. Meaning:

• Provides faster, more efficient data storage and retrieval than other data storage circuits.

• Widely used in RAM, including cache memory in microprocessors.

• Helps optimize performance and speed up the operation of electronic systems, especially in applications that require large data processing and fast access.

• Simple and accessible structure: The Bitcell 6T circuit has a simple and accessible structure, so its design, manufacture and maintenance are also simpler and easier than other types of data storage circuits. other material.

• Space saving and production cost: With its small size and simplicity, the Bitcell 6T circuit saves on-chip space, making it the ideal choice for applications where space savings are required. . In addition, production costs are also reduced due to the lack of components and complex manufacturing processes.

• High reliability: Bitcell 6T circuit has high reliability and low error due to simple structure and few components. It is also designed to automatically recover when a fault occurs, helping to ensure the stability and reliability of the electronic system.

• Can be enhanced to store multiple bits: Although Bitcell 6T can only store one bit of information, it can be enhanced to store multiple bits of information by combining multiple bitcells.

• Low Power Consumption: The Bitcell 6T circuit consumes very low power, thus saving energy and extending the life of batteries in electronic devices.

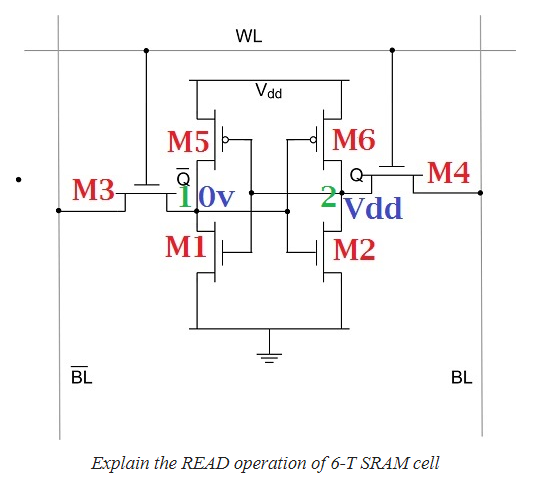
• High interpretability: Bitcell 6T is highly interpretable, meaning it allows data to be retrieved and edited easily and accurately, while minimizing the number of re-reads of data to ensure guarantee its accuracy.

• High compatibility: Bitcell 6T is compatible with many different chips and processors, so it can be used in many different applications.

• High resolution: Bitcell 6T allows storing and retrieving data with high resolution, increasing the accuracy and detail of electronic applications.

In short, Bitcell 6T is a kind of simple data storage circuit, saving space and low power consumption, with high compatibility and high reliability. It plays an important role in modern electronic systems and is widely used in applications that require fast and efficient data processing.

1. **Circuit diagram & operational analysis**

**READ operation**:

1. Assume logic 0 at node (1), V1 = 0V. Therefore, M5 and M2 are OFF and M1 & M6 are ON (linear). Therefore V1 = 0V and V2 = VDD.
2. Word line is activated and data lines CC is pre-changed to VDD.
3. Therefore, M3 and M4 are turned ON.
4. Since for M4, drain and source are at same potential therefore no current flows here.
5. But in LHS at M3 drain and source are at high differential potential therefore non-zero current flows through M3. Path M3 >> M1 >> GND
6. Voltage level at BL begins to drop which results in discharging of CC capacitor which causes V1 to increase.
7. This is sensed by sense amplifier and amplified and read by data read circuit.
8. Since V1 is increasing from 0V and it may turn on M2 if



or if V1max ≥ VT, leads to M2 being turned ON. Therefore to keep M2 in cutoff mode, V1max ≤ VT.

M3 is in saturation region and M1 is in linear region

Text, letter

Description automatically generated

Therefore, M2 will remain off provided above condition is satisfied.

**A picture containing text, diagram, plan, line

Description automatically generatedWRITE operation:**

1. Assume 1 to be stored at node 1.
2. Therefore, M1 and M6 are OFF and M2 and M5 are ON.
3. V1 = VDD and V2 = 0V before M2 and M4 are turned ON.
4. WL is activated; M3 and M4 are turned ON.
5. Since V2 < VT1, V2 cannot be used to turn ON M1. We need to turn ON M1 so that path is created from V1 to GND and voltage at V1 will decrease to zero since path is pull down to GND.
6. Therefore we turn OFF M2. V1 < VT2 to turn OFF M2. When V1 = VT,n; M3 goes in linear region and M5 in saturation region.

Text

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Due to this M2 is forced to turn OFF and M1 turns ON and hence 0 is written at V1.