?

Corrected Copy.

E2.13

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2008

BEng Honours Degree in Computing Part II
MEng Honours Degrees in Computing Part II
BEng Honours Degree in Information Systems Engineering Part II
MEng Honours Degree in Information Systems Engineering Part II
MSc in Computing Science
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER C210=E2.13

COMPUTER ARCHITECTURE

Thursday 15 May 2008, 14:30
Duration: 120 minutes

Answer THREE questions

Paper contains 4 questions
Calculators required

1 a What does RISC stand for?

b Provide three features of a RISC processor.

c Explain how the features in Part b affect:

- the speed of a RISC processor,
- the size of a RISC processor,
- the size of compiled code of a given program for a RISC processor.

d For a given program, 10% of the code is responsible for 90% of the execution time. A co-proceesor is used to speed up this 10% of the code by k times; what is the overall speedup?

e A Field Programmable Gate Array (FPGA) is an elecctronic device which contains programmable logic blocks connected together by programmable interconnections.

A new FPGA is obtained by replacing a fraction α of the area of the original FPGA by new elements which are p times faster and q times smaller. Assuming that computation is distributed uniformly across an FPGA, how much faster and smaller overall is the new FPGA campared with the original one?

The five parts carry, respectively, 10%, 15%, 15%, 30%, 30% of the marks.

2a Provide a diagram for an 8-bit programmable adder/subtractor, such that when a control input is zero, the circuit performs addition; when the control input is one, the circuit performs subtraction.

Given that T is the time that a signal takes to travel from any input to any output of the following circuits: a full adder, a multiplexor with a two-bit data input, and any other one-bit or two-bit input logic gate, what is the fastest clock speed for a 16-bit version of the above programmable adder/subtractor?

b Provide a diagram for a 16-bit programmable carry-select adder/subtractor which consists of a number of 8-bit programmable adder/subtractors given in Part a. What is the fastest clock speed, in terms of T, for this 16-bit programmable carry-select adder/subtractor?

c An 8-bit programmable registered adder/subtractor is obtained by connecting a register to every output (including the carry output) of the 8-bit programmable adder/subtractor in Part a. Two of these are then connected together to form a 16-bit programmable registered adder/subtractor. What is the fastest clock speed, in terms of T, for this 16-bit programmable registered adder/subtractor?

d The programmable registered adder/subtractor in Part c has a major defect: it does not produce the correct result. Provide a diagram showing how the 16-bit programmable registered adder/subtractor in Part c can be modified to produce correct results by including registers at the appropriate locations.

The four parts carry, respectively, 30%, 30%, 20%, 20% of the marks.

3 The four instructions for a processor P, which has a single register, are specified by the following register transfer description:

- addition: $R = R + C$
- load: $R = DM[C]$
- store: $DM[C] = R$
- jump: $PC = IM[R]$

In the above, R denotes the register, PC is the program counter, C denotes a 4-bit constant, DM is an array corresponding to the data memory, and IM is an array corresponding to the instruction memory.

a The four instuctions for P are 6-bit wide. For each instruction, explain the purpose of each of the 6 bits.

b The datapath for P includes the register R, the instruction register IR, the program counter PC, an incrementer INC for incrementing the PC, a sign-extension circuit SX, and an ALU with its output connected to the $ALUout$ register.

The instruction memory IM is connected both to PC and to IR. The data memory DM is connected both to the $ALUout$ register and to selected bits of IR. The control circuit includes two multiplexors. The ALU can add its two inputs, or select one of its inputs and pass it to the output.

Provide a block diagram showing how these components are connected together to form a multi-cycle datapath for P. The diagram does not need to include the control unit.

c Provide a state diagram showing the appropriate register transfer description in each state for a control unit controlling the multi-cycle datapath in Part b.

The three parts carry, respectively, 20%, 40%, 40% of the marks.

4a Give one advantage and one disadvantage for:

- a direct-mapped cache,
- a fully-associative cache.

b Explain how an n-way set-associative cache works. What is the effect of increasing n on the size and the speed of the cache?

c Provide a diagram of an n-way set-associative cache, dealing with p-bit addresses, which contains m blocks. How many bits are there in a tag for this cache?

d Provide a diagram of a direct-mapped cache, dealing with p-bit addresses, which contains m blocks, and each block contains n words. How many bits are there in a tag for this cache?

The four parts carry, respectively, 20%, 30%, 25%, 25% of the marks.