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Paper Number(s): **E4.16**
AM3

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2000

MSc and EEE PART IV: M.Eng. and ACGI

CURRENT-MODE ANALOGUE SIGNAL PROCESSING

Thursday, 11 May 2000, 10:00 am

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks.

Time allowed: 3:00 hours

Corrected Copy

Q. 5

Examiners: Prof C. Toumazou, Dr A.J. Payne, Dr C. Papavassiliou

Special instructions for invigilators:

None

Information for candidates:

None

1. (a) Advanced bipolar technology has led to the development of a new generation of high-speed 'current-mode' analogue building blocks: the current-feedback op-amp and the current conveyor. With the aid of a suitable current-feedback amplifier macro-model, show how constant-bandwidth amplification is obtained in EITHER of these designs.

[13 marks]

- (b) The circuit shown in *Figure 1(a)* is network symbol of a second-generation current conveyor. Describe the terminal relationships of the current conveyor, and explain why the device is so versatile.

[4 marks]

- (c) An implementation of the current-conveyor is shown in *Figure 1(b)*. Explain how the circuit works and why it can achieve a slew-rate higher than that of a classical voltage operational amplifier. Explain why transistors Q5 – Q8 help to significantly reduce offset voltage between node Y and X.

[8 marks]

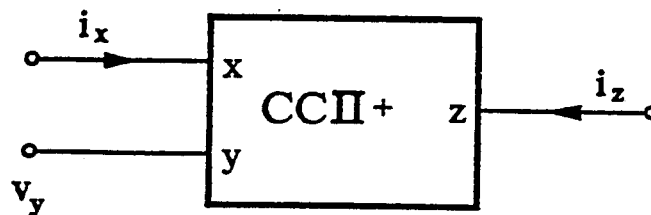
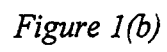


Figure 1(a)



2. (a) The circuit shown in *Figure 2* is a precision diode. Explain the operation of the circuit and sketch the corresponding waveforms at nodes V_x and V_o assuming an input sinusoidal signal. Derive an expression for the diode transfer function, and estimate the maximum input frequency, which would not result in a serious degradation in the quality of output signal. The slew-rate of the op-amp is 10 volts/ μ s.

[16 marks]

- (b) A peak detector is required, capable of acquiring an input rectangular pulse of 2.5 V maximum amplitude and 900 ns minimum width. The output feeds a 10 bit ADC, which has a total conversion time of 350 μ s. Sketch a suitable circuit to meet the above requirements and select suitable components to meet the specification. Assume the op-amp has a maximum output current limit of 10 mA.

[5 marks]

- (c) Finally, sketch a suitable circuit which achieves current-mode rectification without the use of a diode-based rectifier of the type shown in *Figure 2*.

[4 marks]

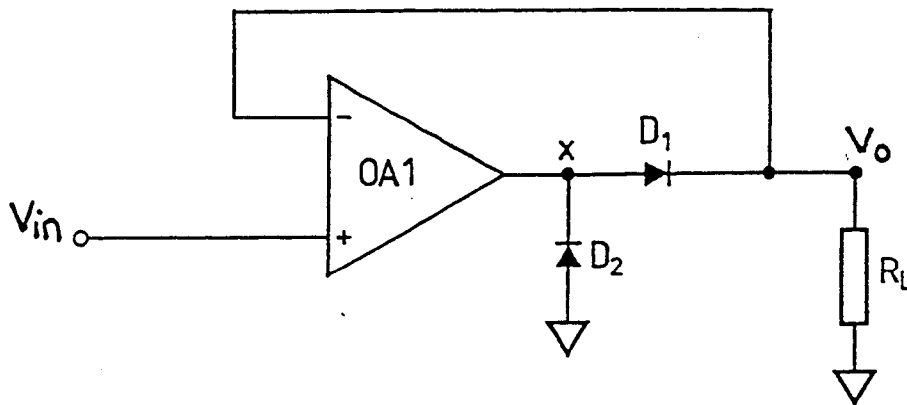


Figure 2

3. (a) The circuit in *Figure 3(a)* is a bootstrapped transconductance amplifier. Derive an expression for the output resistance of the amplifier and show that the minimum output resistance $R_{out(min)}$ is $250\text{ k}\Omega$ given that $R_3 = 10\text{ k}\Omega$ and the resistors have a tolerance of $\pm 1\%$. State any assumptions and matching conditions. [10 marks]

(b) High output resistance without the need for without resistor matching can be achieved with the circuit of *Figure 3(b)*. Explain the operation of the circuit and show how two of such circuits can realise a high CMRR differential amplifier, which also does not require precise resistor matching. [5 marks]

(c) In mixed-mode ASIC design, analogue design is constantly being optimised for digital CMOS technology and *Figure 3(c)* shows an example referred to as a switched-current integrator. Derive an expression for the time constant of the integrator. Assume non-overlapping clocks and that all the switches are ideal. [10 marks]

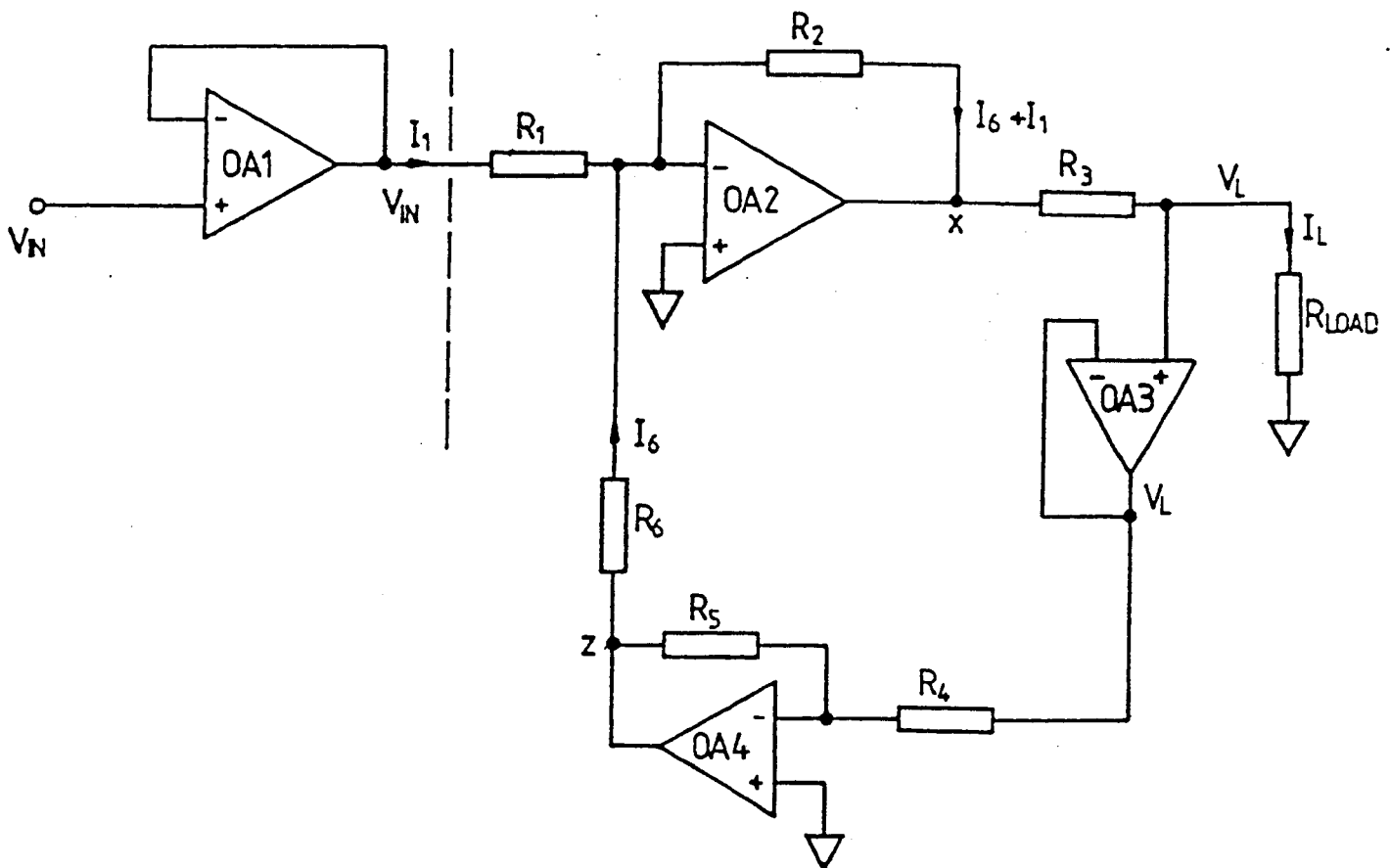


Figure 3 (a)

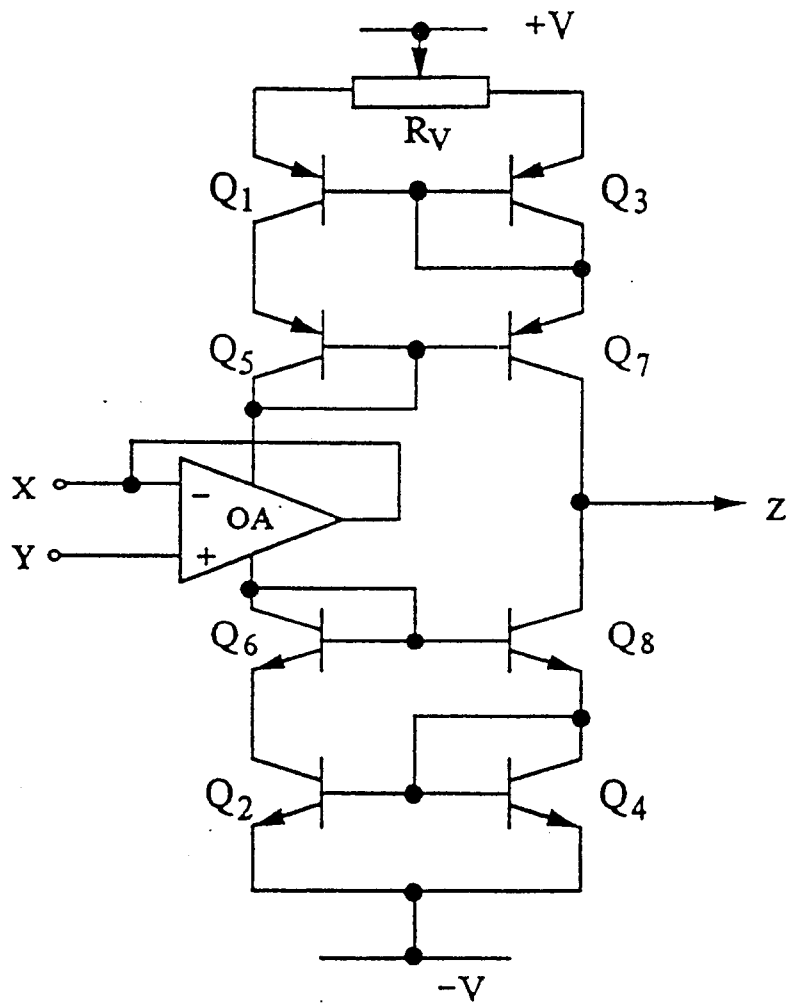


Figure 3(b)

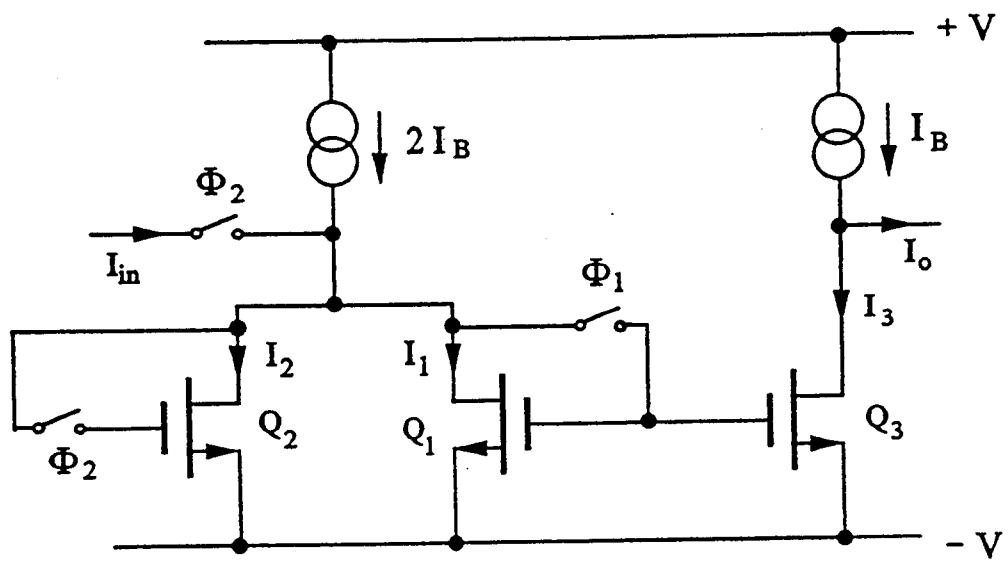


Figure 3(c)

4. (a) State the bipolar translinear principle (TLP) for a loop of p-n junctions. List five conditions which must be satisfied by the circuit in order for this principle to be valid. [5 marks]

(b) Figure 4 shows two translinear circuits. For the circuit of Figure 4a, I_1 and I_3 are input currents while I_2 and I_4 are constant bias currents. Derive an expression for the output current I_{out} stating any assumptions that you make, and hence outline the function of this circuit. What is the minimum value which should be selected for I_2 ? Write down an expression for the output current when $I_1 = \left| \frac{dI_{in}}{dt} \right|$ and $I_3 = \left| \int I_{in} dt \right|$, given that $I_{in} = A \sin \omega t$. [10 marks]

For the circuit of Figure 4b, show that the output current :

$$I_{out} = I_1 - I_2 = \frac{I_3^2 - I_4^2}{\sqrt{I_3^2 + I_4^2}}$$

where I_3 and I_4 are input currents. Hence state the function of this circuit if $I_3 = I_A |\cos \omega t|$ and $I_4 = I_A |\sin \omega t|$. [10 marks]

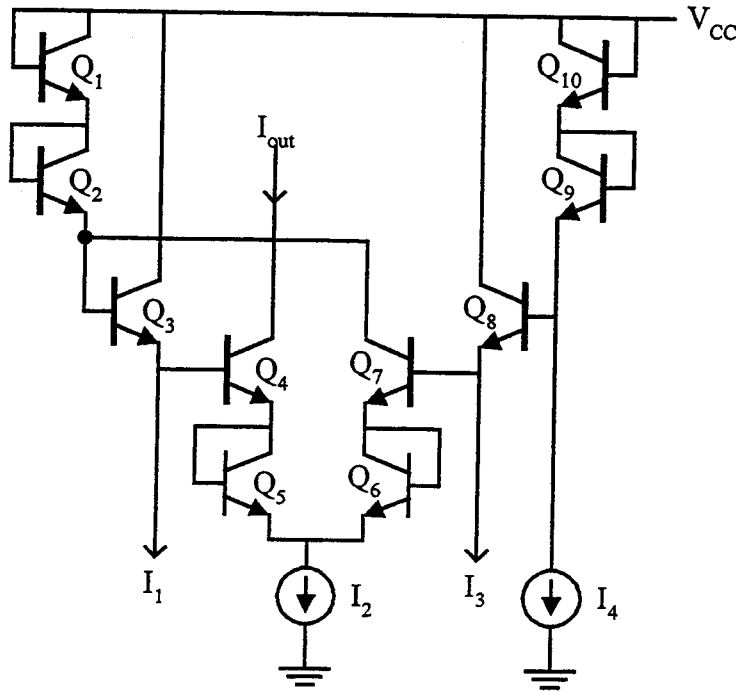


Figure 4a

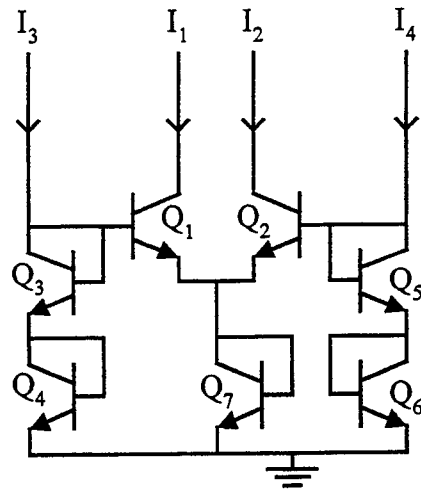


Figure 4b

5. The transfer function for a second order filter has been decomposed into the following state equations:

$$\dot{x}_1 = -\omega_0 x_2 + \omega_0 u_1$$

$$\dot{x}_2 = \omega_0 x_1 - \frac{\omega_0}{Q} x_2 + \omega_0 u_2$$

$$y = x_2$$

where y is the output, x_1 and x_2 are state variables, and u_1 and u_2 are inputs.

- (a) Show that these state equations can be used to implement either a lowpass or a bandpass transfer function, and explain the role of the two inputs u_1 and u_2 .

[7 marks]

- (b) By the use of suitable exponential variable transforms, show that the linear state equations above can be transformed into non-linear log-domain design equations.

[8 marks]

- (c) From these design equations, sketch a transistor level implementation of the final log-domain filter, and choose d.c. bias ^{current} values to give $\omega_0 = 2\pi(10 \times 10^6) \text{ rad s}^{-1}$.

You may assume that all capacitors to be used are of value 10 pF. [10 marks]

ans 10:00

6. (a) State the relationship which must be satisfied by two N-port networks, if these two networks are to be considered adjoint networks. By using this relationship, derive the adjoint network for (i) a resistor, (ii) a nullor, (iii) a unity gain voltage amplifier. Hence derive the current-mode equivalent of the Sallen-Key lowpass filter shown in *Figure 6a*. [13 marks]

- (b) *Figure 6b* shows a transistor-level implementation of a unity gain current amplifier. Derive expressions for (i) the input offset voltage when $I_{in} = 0$, (ii) the small-signal input resistance for this circuit. Describe with the aid of a diagram how this circuit may be modified to simultaneously reduce the input offset voltage and small-signal input resistance. [12 marks]

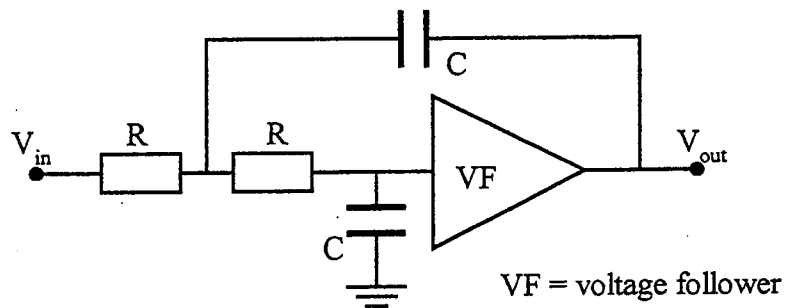


Figure 6a

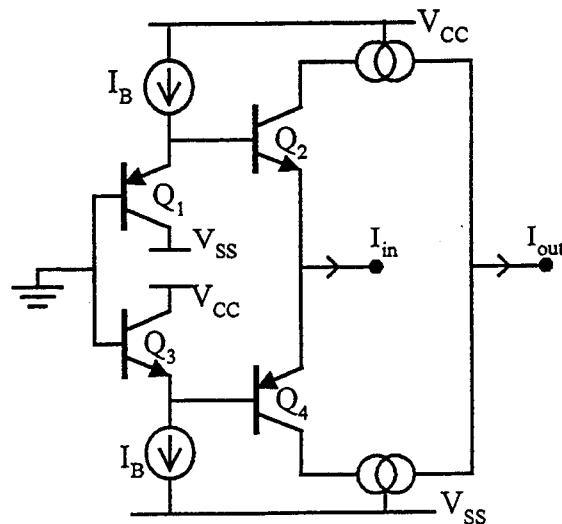


Figure 6b

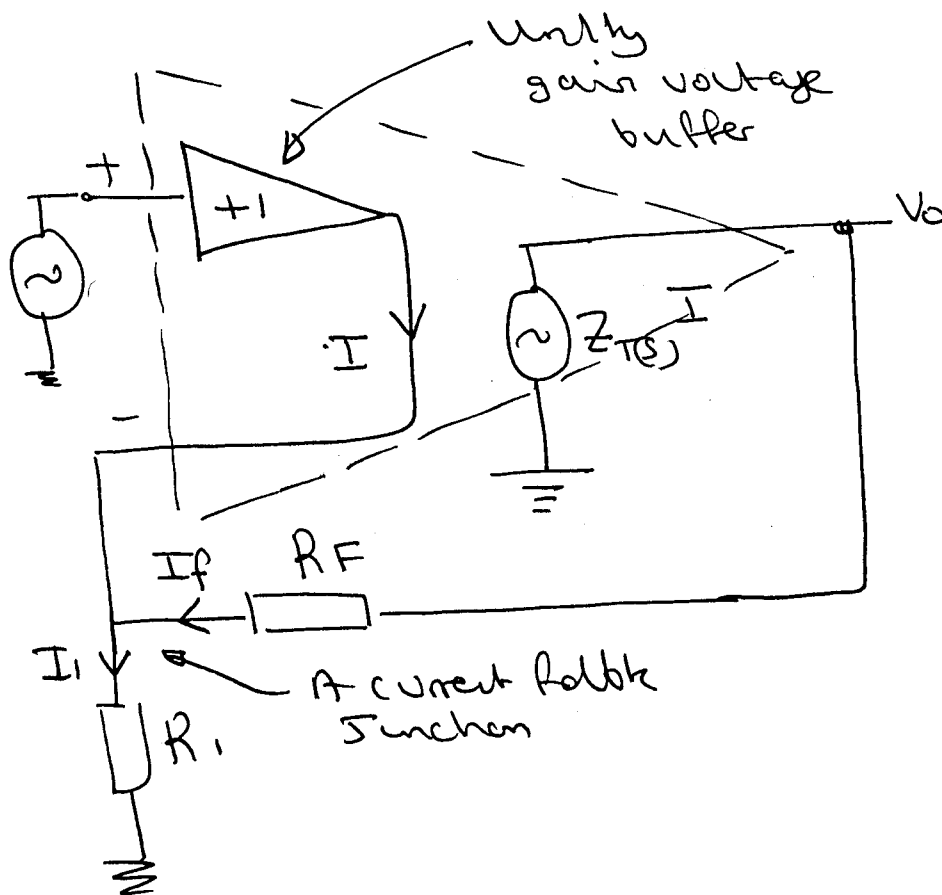


The
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Current-mode Analogue S.P.

Current-Feedback Amplifier

3/7/00
master
solution



open-loop transimpedance gain Z_{TS}

“ voltage gain $A_V(s) = I Z_{TS}$

assume $Z_{TS}(s) = Z_{TS} / (1 + j\omega/\omega_p)$

where ω_p - dominant pole frequency of
open-loop amplifier. From macromodel

3 principle equations

$$I_F = (V_o - V_s) / R_F \quad \text{--- (1)}$$

$$I_1 = V_s / R_1 \quad \text{--- (2)}$$

$$V_o = Z_{TS}(s) I = Z_{TS}(s) (I_1 - I_F) \quad \text{--- (3)}$$

substituting (1) and (2) into (3) gives

$$\boxed{5} \text{ --- } (V_o / V_s) = (1 + R_F / R_1) \left(\frac{Z_{TS}}{R_F + Z_{TS}} \right) \quad \text{--- (4)}$$

Assuming $Z_{TS} \gg R_F$

$$\text{then } V_o / V_s = (1 + R_F / R_1)$$

1 cont
Since Z_{TO} is the only frequency dependent term when gain is set almost independent of bandwidth

This is confirmed by substituting

$$Z_{TO} = Z_{TO} / (1 + j\omega / \omega_p) \text{ into (4)}$$

$$\left(\frac{V_o}{V_s}\right) = \left(1 + \frac{R_F}{R_i}\right) \left[\frac{Z_{TO}}{Z_{TO} + R_F}\right] \left[\frac{1}{\left(1 + j\omega / \omega_p \frac{(Z_{TO} + R_F)}{R_F}\right)}\right]$$

Again assuming

$Z_{TO} \gg R_F$ when

$$(8) - \left(\frac{V_o}{V_s}\right)_{j\omega} = \left(1 + \frac{R_F}{R_i}\right) \left(\frac{1}{1 + j\omega / \omega_{GB}}\right) - \boxed{8}$$

where $\omega_{GB} = \omega_p Z_{TO} = \omega_{GB}$ bandwidth product.

Closed-loop bandwidth is given

$$\omega_{CL} = \omega_{GB} / R_F$$

$R_F \rightarrow$ Bandwidth, $R_i \rightarrow$ gain

—/—

Terminal relationship.

$$V_x = V_y, I_z = \pm I_x$$

Versatile since device has both voltage mode and current-mode capability.

— $\boxed{4}$

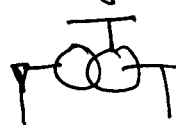
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3

Q_1, Q_2, Q_3, Q_4

So called 'diamond' voltage voltage.

Complementary Class AB Voltage follower.

 supply current-sensing current mirror

Source X node current to output Z.

High output impedance.

Limit on dv/dt determined by push-pull action of Q_2 and Q_3 . Maximum signal I_{max} determined by power ratings of transistors or $3/3$ power supply current limit.

- Since I_{max} is large then

$$(dv/dt)_{max} = [I_{max}/C] \leftarrow \text{parasitic also } 1/2$$

very large.

5

Since by connection $V_{BE4} = V_{BE7}$

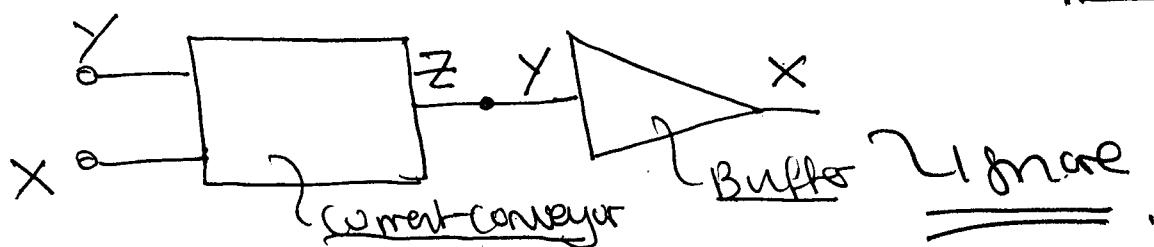
then $V_{B4} = V_{BE8}$

$$V_X = (V_{BE4} + V_{BE3}) + V_Y$$

V_{BE3} (P-device) $\Rightarrow V_{BE4} = V_{BE}$ of P-device

then $(V_X \approx V_Y)$ offset is reduced.

3



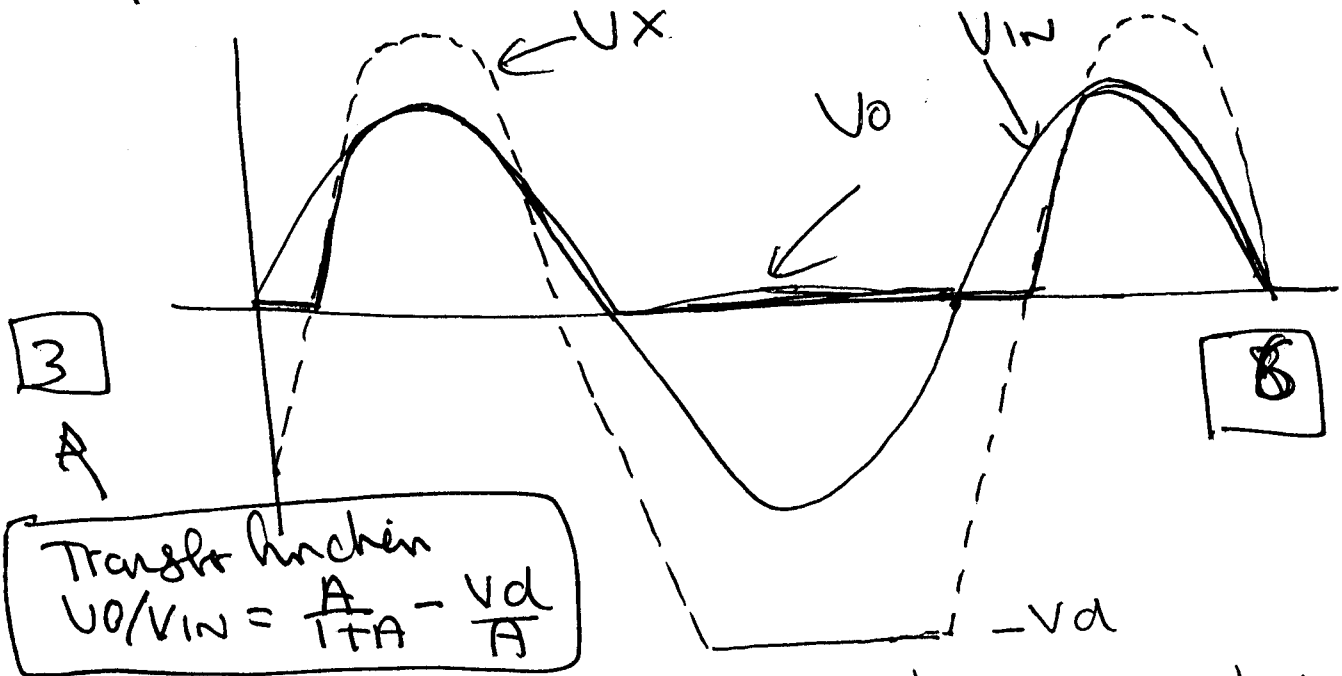
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2. Precision diode

OA1 and D1 half wave rectifier.

D1 conducts for positive input signal
For negative input OA1 output drops to

-0.6V due to recovery time. - [2]
OA1 should be short circuit current
protected.



As can be seen the output is badly distorted when the diode is not conducting because the op-amp slewing holds the diode off even when $V_{IN} > 0$. This distortion becomes more significant as the input frequency rises.

Recovery or delay time is greater than

$$(1.2 \text{ V/s} \cdot R) = \underline{dt} = 0.12 \mu\text{s}$$

Since pulse width $\approx 0.12 \mu\text{s}$

Period $\approx 0.24 \mu\text{s}$

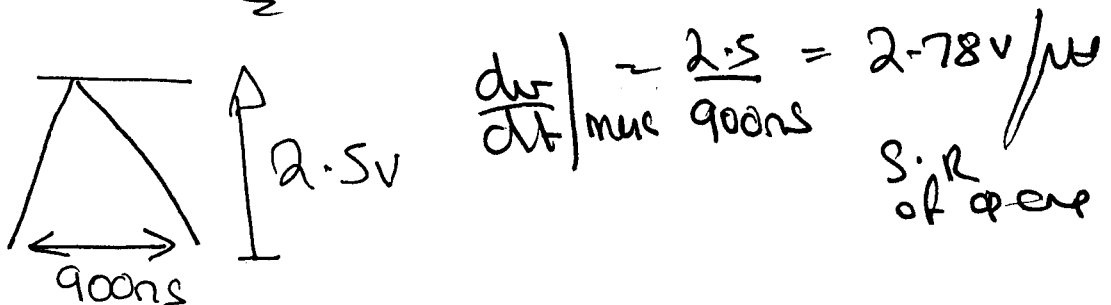
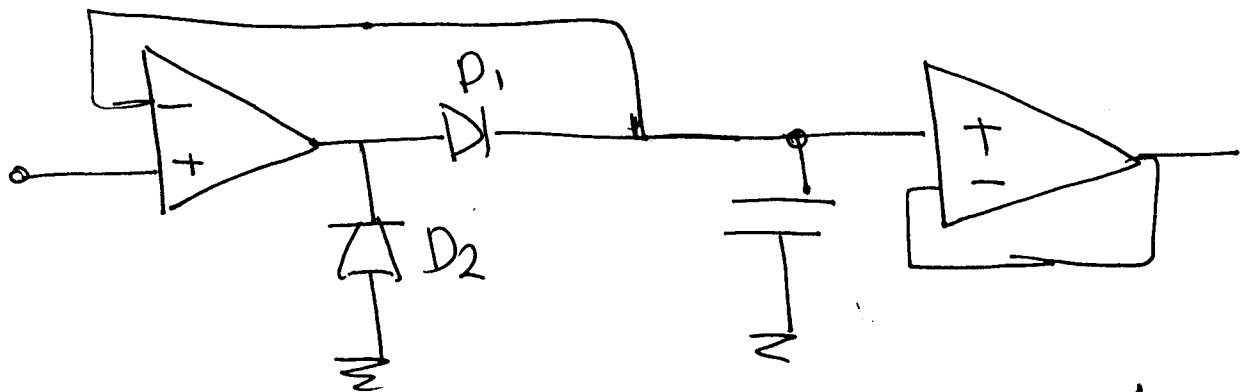
$$\underline{f = 4.16 \text{ MHz}}$$

- [5]

2 cont

5

Peak detector



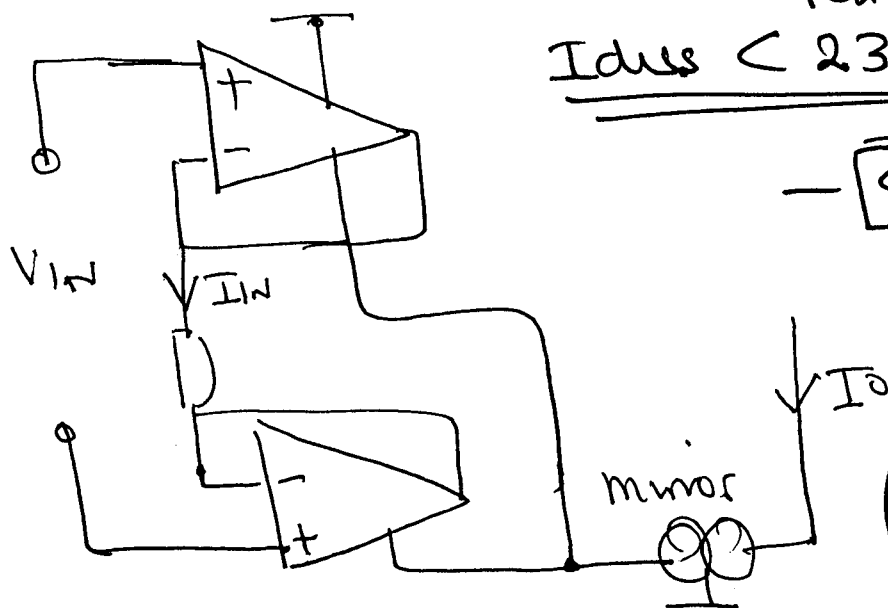
$$\frac{I_{outmax}}{C} \leq 2.78V/\mu s$$

Let op-amp give $10mA \rightarrow I_{outmax}$

$$C < \frac{10 \times 10^{-3}}{2.78 \times 10^6} = \frac{10}{2.78} nF = 3.5 nF$$

Last part

Current-mode rechner



$$\frac{I_{diss}}{C} < \frac{2.5}{1024} / 350 \times 10^{-6}$$

$$\underline{\underline{I_{diss} < 23 nA}}$$

- [4]

Turn
25
23

③. Bootsrappered Current-source

With correct choice of R_5 the voltage across R_3 is made independent of V_L because V_X of the form

$$V_X = K V_{IN} + V_L$$

$$I_3 = I_L = K V_{IN} / R_3$$

$$K = -R_2 / R_1$$

$$\text{iff } R_5 / R_4 = R_6 / R_2$$

OR

$$I_L = -(R_2 / R_1) V_{IN} / R_3 + [(R_2 R_5) / (R_3 R_4 R_6) - 1 / R_3] V_O$$

[5]

from which the output impedance is simply

$$-dV_O / dI_L = R_{out} \text{ and}$$

$$R_{out} = R_3 R_4 R_6 / (R_4 R_6 - R_2 R_5)$$

$$= R_3 / \left(1 - \frac{R_2 R_5}{R_4 R_6} \right)$$

Assume 1% resistor

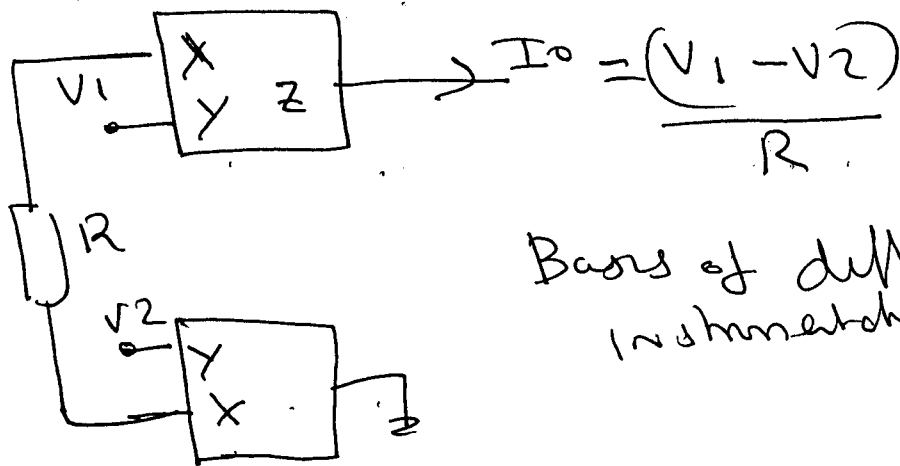
$$R_{out} = R_3 / (1 - (1 + 0.04))$$

$$R_{out} \approx 25 R_3 \approx \underline{\underline{250k\Omega}}$$

[5]

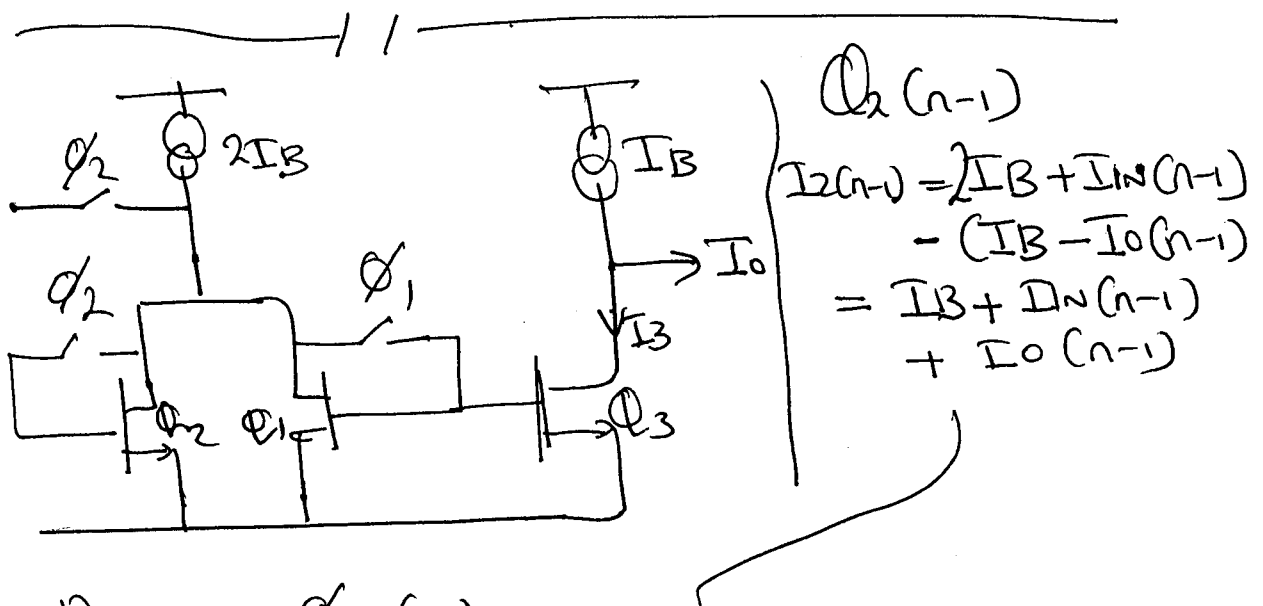
3 cont

Supply current sensing circuit.
 Current into X terminal drawn by power supplies and current minus to high output impedance node Z. Current minus are improved with n-type mos.
 RV is essentially offset bias adjustment to ensure minimum offset at output due to imbalance in P and N mos.
 Good voltage buffer between X and Y.
 Current follows between X and Z.



5

Basis of differential instrumentation amplifier.



Dummy $\phi_2(n)$

$$I_1(n) = 2IB - I_2(n-1) = IB - I_{IN}(n-1) - I_0(n-1)$$

$$\Rightarrow I_0(n) = I_{IN}(n-1) + I_0(n-1)$$

In z -domain

$$\lim(z) [1 - z^{-1}] = \lim(z) z^{-1}$$

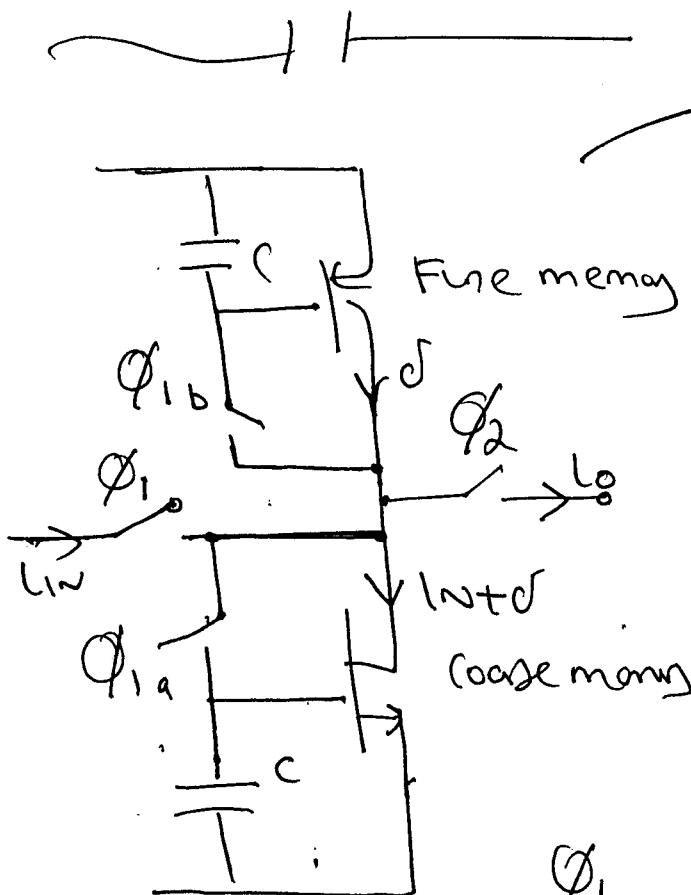
$$H(z) = \frac{\lim(z)}{\lim(z)} = \left(\frac{z^{-1}}{1 - z^{-1}} \right) = \frac{1}{z - 1}$$

Since $e^{sT} = e^{j\omega T} \approx (1 + j\omega T)$ for $\omega T \ll 1$

$\therefore H(z) = 1/j\omega T$ low-pass integrator

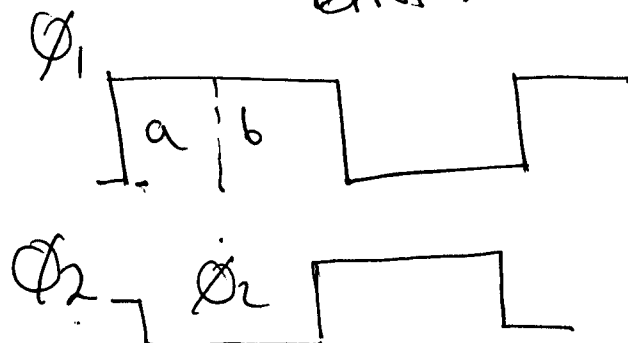
and so $\boxed{T = T}$

$\boxed{10} / \left(\frac{25}{25} \right)$



Ignore
Two step

Error in coarse memory is stored by fine memory and then subtracted from stored output cancelling error.



4. Bipolar TLP:

$$cw \prod_{j=1}^m \frac{I_{Cj}}{A_j} = ccw \prod_{j=1}^m \frac{I_{Cj}}{A_j}$$

The product of the collector currents \div by the emitter areas for devices in a clockwise direction is equal to the product of the collector currents \div by the emitter areas for devices in a counter clockwise direction.

- i) continuous loop of p-n junctions
- ii) equal number of cw & ccw npn junctions
- iii) equal number of cw & ccw pnp junctions
- iv) all devices at same temperature (same V_T)
- v) npn devices have same J_{Sn} , similarly pnp devices all have same J_{Sp} .
- vi) all transistors must be forward biased ⑤

Figure 4a:

$$(I_2 - I_{out})^2 \cdot I_1 \cdot I_{out}^2 = (I_2 - I_{out})^2 \cdot I_3 \cdot I_4^2$$

Assuming transistors all have equal areas
 β is high (i.e. base currents can be neglected)
 V_T is high (i.e. Early Voltage effects are neglected).

$$I_{out}^2 = I_4^2 I_3 / I_1$$

$$I_{out} = I_4 \cdot \sqrt{\frac{I_3}{I_1}}$$

The circuit calculates the square root of the quotient of the two inputs.

$$i_{in} = A \sin \omega t$$

$$I_1 = \left| \frac{d i_{in}}{dt} \right| = A \omega \cos \omega t$$

$$I_3 = \left| \int i_{in} dt \right| = \frac{A}{\omega} \cos \omega t$$

$$\therefore I_{out} = I_4 \sqrt{\frac{I_3}{I_1}} = I_4 / \omega$$

Output current is ^{inversely} proportional to the input frequency.

Let $I_A = (I_2 - I_{out}) =$ bias current for Q_1, Q_2, Q_7, Q_8

I_A must remain positive to keep these devices forward biased, thus $I_2 > I_{out(max)}$

(10)

Figure 4b:

$$I_3^2 = I_1 (I_1 + I_2) \quad I_4^2 = I_2 (I_1 + I_2)$$

$$I_3^2 = I_1^2 + I_1 I_2 \quad I_4^2 = I_2^2 + I_1 I_2$$

$$I_3^2 - I_4^2 = I_1^2 - I_2^2 = (I_1 - I_2)(I_1 + I_2)$$

$$I_3^2 + I_4^2 = I_1^2 + 2I_1 I_2 + I_2^2 = (I_1 + I_2)^2$$

$$(I_1 - I_2) = \frac{(I_3^2 - I_4^2)}{(I_1 + I_2)} = \frac{I_3^2 - I_4^2}{(I_3^2 + I_4^2)^{1/2}}$$

$$I_3 = I_A |\cos \omega t| \quad I_4 = I_A |\sin \omega t|$$

$$I_1 - I_2 = \frac{I_A^2 \cos^2 \omega t - I_A^2 \sin^2 \omega t}{(I_A^2 \cos^2 \omega t + I_A^2 \sin^2 \omega t)^{1/2}}$$

$$= \frac{I_A^2 (\cos^2 \omega t - \sin^2 \omega t)}{I_A}$$

$$= I_A (\cos^2 \omega t - \sin^2 \omega t)$$

$$= I_A (\cos^2 \omega t - (1 - \cos^2 \omega t))$$

$$= I_A (2 \cos^2 \omega t - 1)$$

$$= I_A (1 + \cos 2\omega t - 1)$$

$$= I_A \cos 2\omega t$$

The circuit is a frequency doubler.

(10)

$$5. \quad \begin{aligned} \dot{X}_1 &= -\omega_0 X_2 + \omega_0 U_1 \\ \dot{X}_2 &= \omega_0 X_1 - \frac{\omega_0}{Q} X_2 + \omega_0 U_2 \end{aligned}$$

$$y = X_2$$

$$\ddot{X}_2 = \omega_0 \dot{X}_1 - \frac{\omega_0}{Q} \dot{X}_2 + \omega_0 \dot{U}_2$$

$$\ddot{X}_2 = \omega_0 (-\omega_0 X_2 + \omega_0 U_1) - \frac{\omega_0}{Q} \dot{X}_2 + \omega_0 \dot{U}_2$$

$$\ddot{X}_2 + \omega_0^2 X_2 + \frac{\omega_0}{Q} \dot{X}_2 = \omega_0^2 U_1 + \omega_0 \dot{U}_2$$

Taking Laplace Transform:

$$X_2(s) [s^2 + s\omega_0/Q + \omega_0^2] = \omega_0^2 U_1(s) + \omega_0 \cdot s \cdot U_2(s)$$

$$y(s) = X_2(s)$$

$$\therefore \frac{y(s)}{U_1(s)} = \frac{\omega_0^2}{s^2 + s\omega_0/Q + \omega_0^2} \quad \text{if } U_2 = \emptyset$$

LOWPASS

$$\frac{y(s)}{U_2(s)} = \frac{s\omega_0}{s^2 + s\omega_0/Q + \omega_0^2} \quad \text{if } U_1 = \emptyset$$

BANDPASS.

U_1 = Input for lowpass + f

U_2 = Input for bandpass + f.

The input which is not being 'utilised' will generally be a dc current to maintain dc bias conditions.

$$\text{Let } x_1 = I_0 e^{u_1/V_T} \quad x_2 = I_0 e^{v_2/V_T}$$

$$\dot{x}_1 = \frac{x_1}{V_T} \dot{v}_1 \quad \dot{x}_2 = \frac{x_2}{V_T} \dot{v}_2$$

$$u_1 = I_s e^{u_{11}/V_T} \quad u_2 = I_s e^{u_{12}/V_T}$$

$$\Rightarrow \frac{x_1}{V_T} \dot{v}_1 = -\omega_0 x_2 + \omega_0 u_1$$

$$\frac{x_2}{V_T} \dot{v}_2 = \omega_0 x_1 - \frac{\omega_0}{Q} x_2 + \omega_0 u_2$$

$$\Rightarrow C \dot{v}_1 = -C \omega_0 V_T \frac{x_2}{x_1} + C V_T \omega_0 \frac{u_1}{x_1}$$

$$C \dot{v}_2 = C V_T \omega_0 \frac{x_1}{x_2} - \frac{C V_T \omega_0}{Q} + C V_T \omega_0 \frac{u_2}{x_2}$$

$$\text{Let } I_0 = C V_T \omega_0$$

$$\Rightarrow C \dot{v}_1 = -I_0 \frac{\exp(v_2 - v_1)}{V_T} + I_s \frac{\exp(v_{u1} - v_1)}{V_T}$$

$$C \dot{v}_2 = I_0 \frac{\exp(v_1 - v_2)}{V_T} - \frac{I_0}{Q} + I_s \frac{\exp(u_{12} - v_2)}{V_T}$$

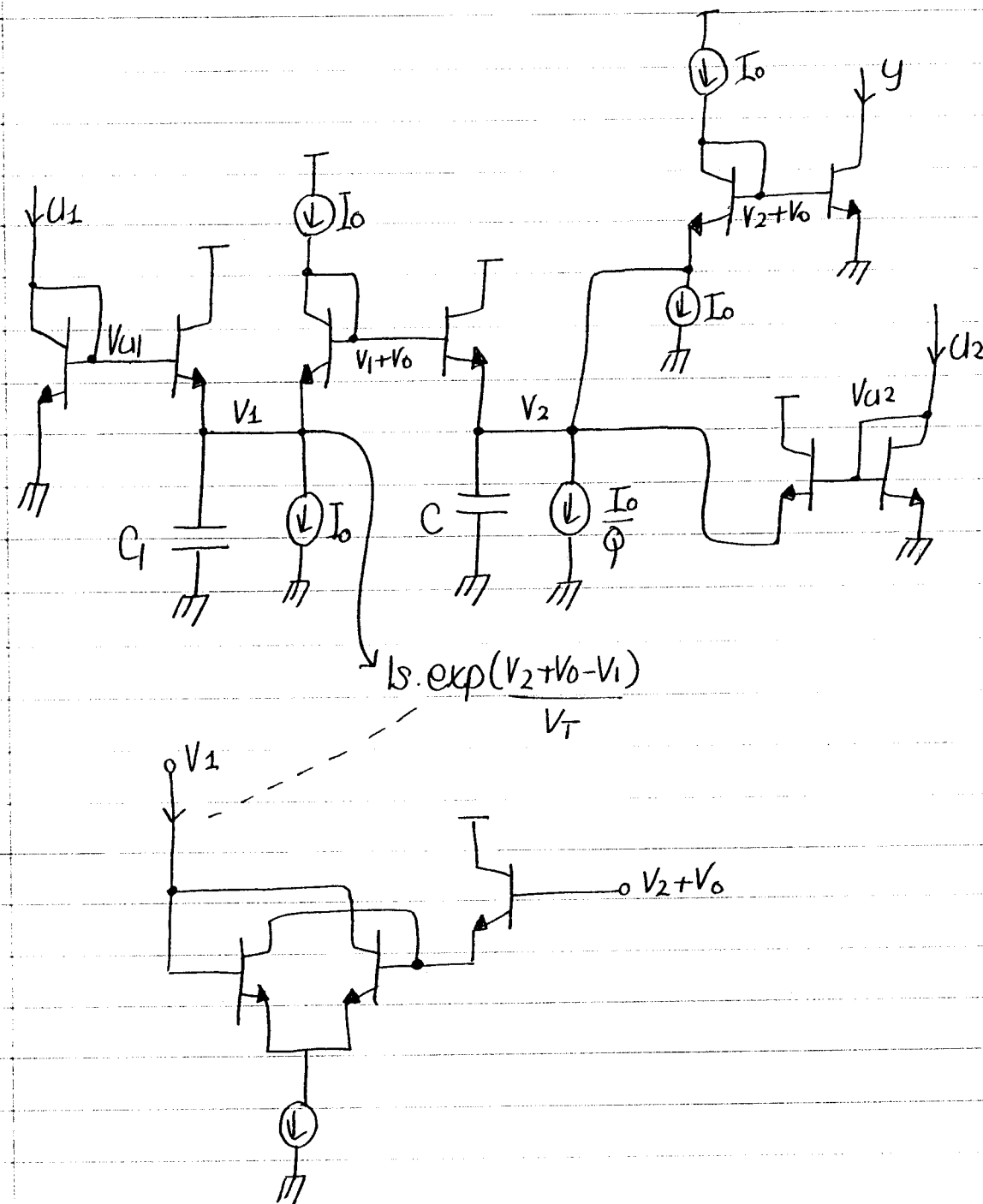
$$\text{Let } I_0 = I_s \exp(v_0/V_T)$$

$$\Rightarrow C \dot{v}_1 = -I_s \frac{\exp(v_2 + v_0 - v_1)/V_T}{V_T} + I_s \frac{\exp(v_{u1} - v_1)}{V_T}$$

$$C \dot{v}_2 = I_s \frac{\exp(v_1 + v_0 - v_2)/V_T}{V_T} - \frac{I_0}{Q} + I_s \frac{\exp(u_{12} - v_2)}{V_T}$$

$$y = x_2 = I_0 e^{V_2/V_T} = I_S \exp(V_2 + V_0)/V_T$$

CIRCUIT DIAGRAMS :



For B.P operation, we can remove u_2 stage.

For B.P. operation, u_1 stage must be present for correct dc biasing. (8)

$$I_0 = C\omega_0 V_T \quad ; \quad \omega_0 = \frac{I_0}{CV_T}$$

$$I_0 = 10p \cdot 2\pi(10 \times 10^6) 25 \times 10^{-3}$$

(2)

$$= 15.7 \mu A.$$

6 (a) Two N -port networks (A & B) must satisfy the following relationship in order to be adjoint networks:

$$\sum_{n=1}^N \{V_{A_n} I_{B_n} - I_{A_n} V_{B_n}\} = 0$$

where V_{A_n} = voltage at n^{th} port of network A, etc. (2)

(i) Resistor

$$V_A = I_A \cdot R_A, \text{ one port}$$

$$V_A \cdot I_B - I_A \cdot V_B = 0$$

$$\frac{V_A}{I_A} = \frac{V_B}{I_B} \therefore \frac{V_B}{I_B} = R_A$$

The adjoint network is a resistor of the same value. (2)

(ii) Nullor



$$V_A = \begin{bmatrix} V_{A1} & V_{A2} \end{bmatrix} = \begin{bmatrix} 0 & X \end{bmatrix}$$

$$I_A = \begin{bmatrix} I_{A1} & I_{A2} \end{bmatrix} = \begin{bmatrix} 0 & X \end{bmatrix}$$

$$V_{A1} I_{B1} - I_{A1} V_{B1} + V_{A2} I_{B2} - I_{A2} V_{B2} = 0$$

$$0 \cdot I_{B1} - 0 \cdot V_{B1} + X \cdot I_{B2} - X \cdot V_{B2} = 0$$

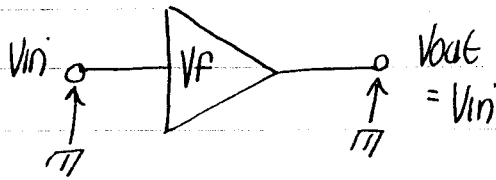
$$\underbrace{\quad}_X \quad \underbrace{\quad}_X \quad \underbrace{\quad}_0 \quad \underbrace{\quad}_0 \quad [X = \text{ANY VALUE!}]$$

$$\text{Thus } V_B = \begin{bmatrix} V_{B1} & V_{B2} \end{bmatrix} = \begin{bmatrix} X & 0 \end{bmatrix}$$

$$I_B = \begin{bmatrix} I_{B1} & I_{B2} \end{bmatrix} = \begin{bmatrix} X & 0 \end{bmatrix}$$

Nullor, but with input & output ports interchanged. (2)

(iii)



$$V_A = \begin{bmatrix} V_{A1} & V_{A2} \end{bmatrix} = \begin{bmatrix} V_{in} & V_{in} \end{bmatrix}$$

$$I_A = \begin{bmatrix} I_{A1} & I_{A2} \end{bmatrix} = \begin{bmatrix} 0 & X \end{bmatrix}$$

$$V_{A1} \cdot I_{B1} - I_{A1} \cdot V_{B1} + V_{A2} \cdot I_{B2} - I_{A2} \cdot V_{B2} = 0$$

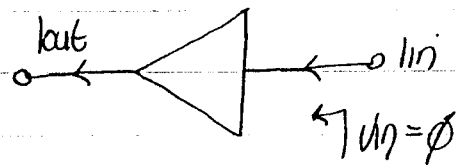
$$V_{in} \cdot I_{B1} - 0 \cdot V_{B1} + V_{in} \cdot I_{B2} - X \cdot V_{B2} = 0$$

$\underbrace{\hspace{1.5cm}}_X \qquad \qquad \qquad \underbrace{\hspace{1.5cm}}_0$

$$V_{in} \cdot I_{B1} + V_{in} \cdot I_{B2} = 0 \qquad I_{B1} = -I_{B2}$$

$$\therefore V_B = \begin{bmatrix} V_{B1} & V_{B2} \end{bmatrix} = \begin{bmatrix} X & 0 \end{bmatrix}$$

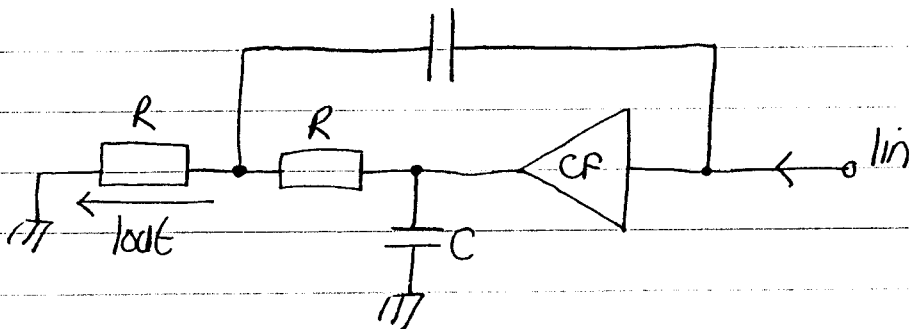
$$I_B = \begin{bmatrix} I_{B1} & I_{B2} \end{bmatrix} = \begin{bmatrix} I_{in} & I_{in} \end{bmatrix}$$



(2)

Unity gain current amp with input = port 2 & output = port 1.

Adjoint of Sallen-Key Filter:



(5)

(b). $V_{in} = V_{be1} - V_{be2}$

(i) In the absence of an input signal I_{in} , $I_{c2} \approx I_{c4}$.
Also $I_{c1} \approx I_{c3}$

Thus $V_{be1} + V_{be3} = V_{be2} + V_{be4}$

Q_1 & Q_4 are matched, Q_2 & Q_3 are matched,

$\therefore I_{c1} = I_{c2} = I_{c3} = I_{c4} = I_B$.

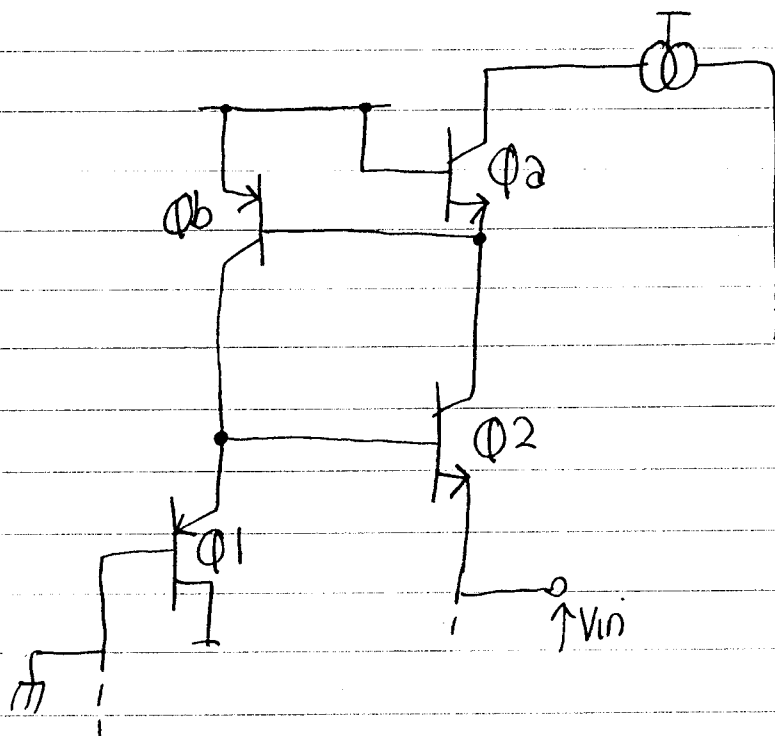
$$V_{in} = V_T \ln\left(\frac{I_B}{I_{sp}}\right) - V_T \ln\left(\frac{I_B}{I_{sn}}\right) = V_T \ln\left(\frac{I_{sn}}{I_{sp}}\right)$$

'dc' offset which will vary with temp.

(ii) Small signal input resistance, $r_{in} = r_{e2} \parallel r_{e3}$

$$= \frac{V_T}{I_{c2}} \parallel \frac{V_T}{I_{c3}}$$

To reduce V_{in} & r_{in} simultaneously:



$$V_{in} = U_{be1} - U_{be2}$$

$$U_{be2} = V_T \ln(I_{c2}/I_{sn})$$

$$U_{be}(\phi_2) = V_T \ln(I_{c2}/I_{sn}) \quad [\text{Matched to } \phi_2]$$

$$I_{c}(\phi_2) = I_{sp} \cdot \exp\left(\frac{U_{be}(\phi_2)}{V_T}\right) = I_{sp} \cdot \exp[\ln I_{c2}/I_{sn}]$$

$$= \frac{I_{sp} \cdot I_{c2}}{I_{sn}}$$

$$I_{c1} = I_{c}(\phi_2) \quad \therefore U_{be1} = V_T \ln(I_{c}(\phi_2)/I_{sp})$$

$$= V_T \ln(I_{c2}/I_{sn})$$

$$\text{i.e. } U_{be1} = U_{be2}$$

Thus V_{in} & r_{in} are reduced to zero.