

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING  
EXAMINATIONS 2004

EEE/ISE PART I: MEng, BEng and ACGI

**ANALOGUE ELECTRONICS 1**

Monday, 24 May 10:00 am

Time allowed: 2:00 hours

**There are FIVE questions on this paper.**

**Answer THREE questions.**

*All questions carry equal marks*

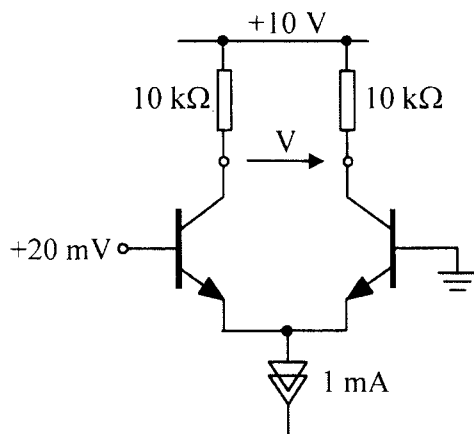
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**Any special instructions for invigilators and information for candidates are on page 1.**

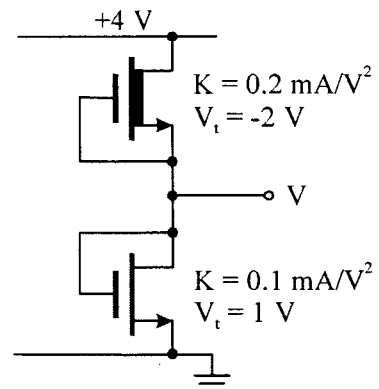
|                       |                    |             |
|-----------------------|--------------------|-------------|
| Examiners responsible | First Marker(s) :  | A.S. Holmes |
|                       | Second Marker(s) : | S. Lucyszyn |

1. For each of the circuits in Figure 1 below, determine the operating mode(s) of the transistor(s), and calculate the value of the current  $I$  or voltage  $V$ . State clearly any assumptions made in your calculations.

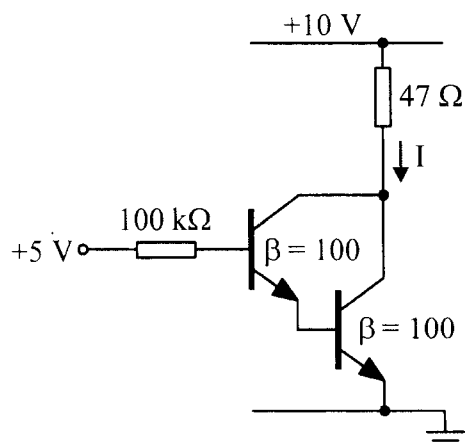
(a) [6 marks]



(b) [5 marks]



(c) [5 marks]



(d) [4 marks]

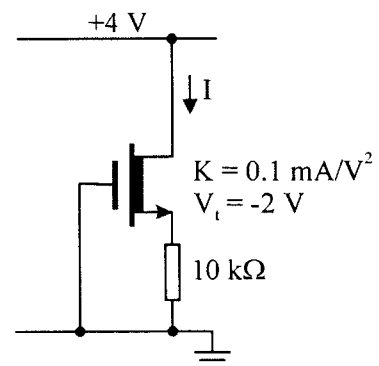


Figure 1

2. Figure 2 shows a band-pass filter comprising a common-emitter amplifier with a resonant load. You may assume in parts (a), (b) and (c) that the reactive components are ideal.

- (a) Choose the value of  $R_B$  to give a collector bias current of 1 mA, stating clearly any assumptions you make. Also determine the quiescent output voltage of the circuit. [4]
- (b) Draw a small-signal equivalent circuit of the filter, assuming the input capacitor to be a short-circuit. Hence show that the small-signal voltage gain  $A_v$  is given by:

$$A_v = -g_m(Z_{LC} \parallel r_o)$$

where  $g_m$  and  $r_o$  are the transconductance and output resistance of the transistor, and  $Z_{LC}$  is the impedance of the resonant load. What is the numerical value of  $A_v$  at resonance? [8]

- (c) Assuming the bias conditions in part (a), choose the values of  $L$  and  $C$  to give a centre frequency of 1 MHz and a  $Q$  of 100. [4]
- (d) A filter is constructed with the component values derived by you in parts (a) and (c). When tested it is found to have a  $Q$  of only 60. Estimate the equivalent series resistance of the inductor, assuming this is responsible for the lower  $Q$ . [4]

Note: the  $Q$  of a parallel RLC network is  $2\pi f_0 RC$  where  $f_0$  is the centre frequency.

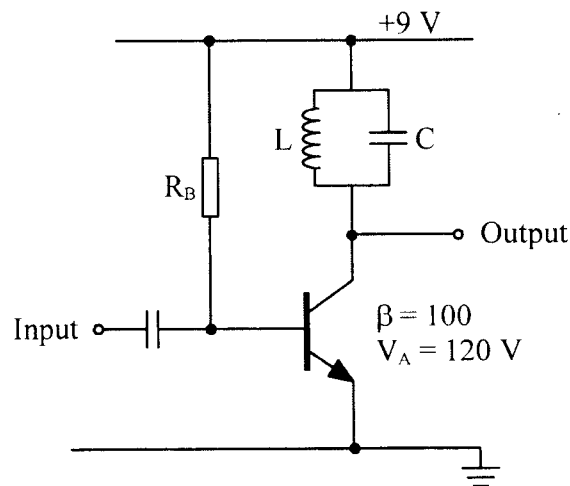


Figure 2

3. Figure 3 shows a single-stage CMOS amplifier in which both MOSFETs contribute to the small-signal gain.

- (a) Explain the role of the resistor  $R_G$ , and show that the quiescent output voltage  $V_{OUT}$  is given by:

$$V_{OUT} = \frac{V_{DD} + V_{t2} + V_{t1} \sqrt{(K_1 / K_2)}}{1 + \sqrt{(K_1 / K_2)}}$$

where the symbols  $K$  and  $V_t$  denote the usual MOSFET parameters, and the subscripts 1 and 2 refer to Q1 and Q2 respectively.

Hence determine the value of  $V_{OUT}$ , and the quiescent drain current in each MOSFET. [8]

- (b) Draw a small-signal equivalent circuit of the amplifier, including  $R_G$ , and calculate the small-signal voltage gain at frequencies for which the input capacitor is effectively short-circuit. Also determine the small-signal input resistance. [8]

- (c) If a sinusoidal input signal is applied to the amplifier, over what range of input signal amplitudes will both transistors remain active? You may assume that the input capacitor has negligible impedance at the signal frequency. [4]

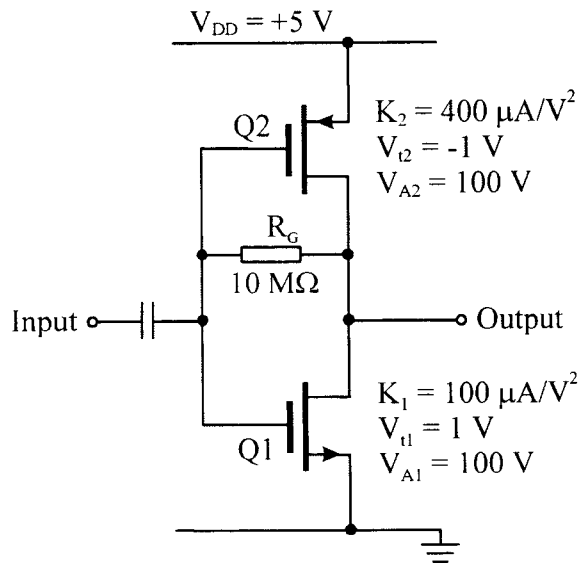


Figure 3

4. (a) Discuss briefly the relative merits of Class A, Class AB and Class B output stages. [4]

(b) Figure 4 shows an idealised Class AB output stage in which the output transistors are biased using two voltage sources, each of magnitude  $V_B$ .

Show that, if the transistors are matched and base currents are neglected, the collector currents  $I_N$  and  $I_P$  satisfy the following relations:

$$I_N - I_P = I_L \quad \text{and} \quad I_N I_P = I_Q^2$$

where  $I_L$  is the current into the load, and  $I_Q = I_S \exp(V_B / V_T)$ .

What is the significance of the quantity  $I_Q$ ? [6]

(c) On the same axes, sketch the variations of  $I_N$  and  $I_P$  with load current for load currents in the range  $-10I_Q < I_L < +10I_Q$ . Also calculate the relative magnitudes of  $I_N$  and  $I_P$  for the cases  $I_L = I_Q$  and  $I_L = 10I_Q$ . [6]

(d) Give one example of how the bias sources of Figure 4 can be implemented in a practical circuit. Your answer should include a circuit diagram of your chosen configuration. [4]

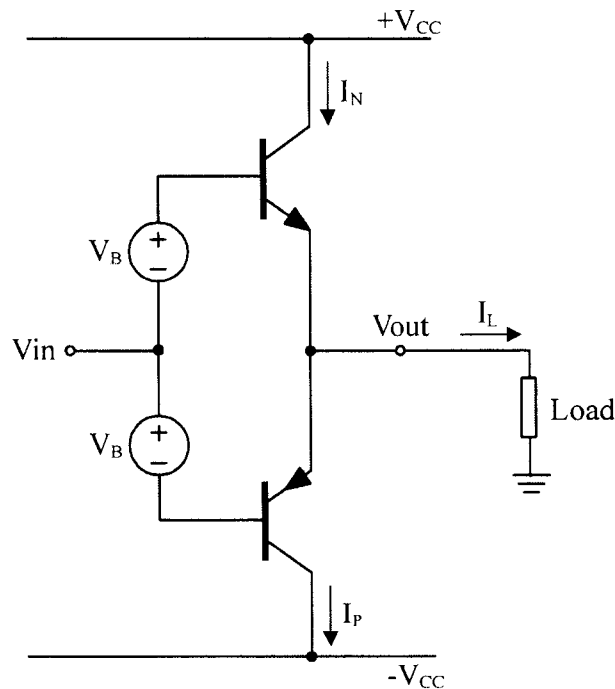


Figure 4

5. The circuit in Figure 5 is to be used to generate a positive-going, square pulse each time the push-button S1 is pressed. Both transistors have  $\beta = 200$ .

- (a) What will be the voltages at the base and collector terminals of Q1 and Q2 when the switch has been open for a long time? Explain your reasoning. [6]
- (b) Assuming starting conditions as in (a), derive an expression for the time variation of the base voltage of Q2 when the switch is pressed and held. Sketch this function, and show on the same axes the corresponding time variation of  $V_{OUT}$ . Your sketch should start just before the switch is pressed, and continue until just after the end of the output pulse.

What is the duration of the output pulse? [10]

- (c) What is the purpose of the resistor  $R_F$ ? How would the behaviour of the circuit differ if this resistor were omitted? [4]

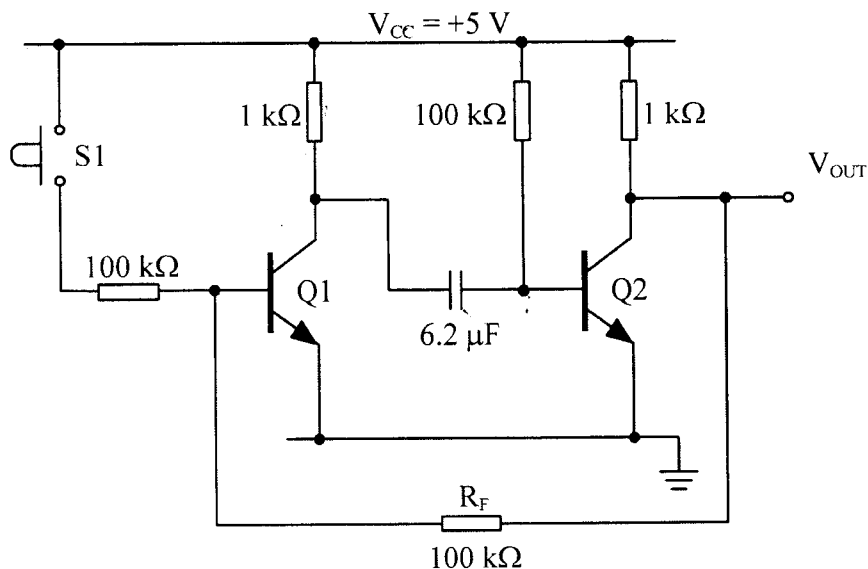


Figure 5

1 (a) Differential input voltage  $\sim V_T \Rightarrow$  use large signal equations

$$I_{C1} = \frac{I}{1 + e^{-V_D/V_T}}, \quad I_{C2} = \frac{I}{1 + e^{V_D/V_T}} \quad \text{where } I = 1 \text{ mA}$$

$V_D = 20 \text{ mV}, V_T = 25 \text{ mV}$

$$\Rightarrow I_{C1} = 0.69 \text{ mA}, \quad I_{C2} = 0.31 \text{ mA}$$

$$V_{C1} = 10 - I_{C1} \times 10 \text{ k} = 3.1 \text{ V}, \quad V_{C2} = 10 - I_{C2} \times 10 \text{ k} = 6.9 \text{ V}$$

So: Both transistors ACTIVE, with  $V = 6.9 - 3.1 = 3.8 \text{ V}$

NB: Small-signal analysis leading to  $V = 4 \text{ V}$  also acceptable.

6

(b) Lower FET Q1 is ACTIVE ( $V_{GS} = 0$ ); Upper FET Q2 needs checking

If both active, then  $I_D = K_2 V_{GS2}^2 = 0.8 \text{ mA} = K_1 (V - V_{t1})^2$

$$\Rightarrow V = 1 + 252 = 3.83 \text{ V}, \quad \text{But this value of } V \text{ is inconsistent with Q2 being active, since it implies } V_{DS2} = 0.17 < -V_{t2}.$$

So: Lower FET ACTIVE, Upper FET TRIODE

Now have to solve  $I_D = K_2 [2(-V_{t2})(4 - V) - (4 - V)^2] = K_1 (V - V_{t1})^2$

$$\Rightarrow 2V(4 - V) = (V - 1)^2 \quad \text{or} \quad 3V^2 - 10V + 1 = 0 \Rightarrow V = 3.23 \text{ or } 0.1$$

Second solution puts Q1 below threshold,  $\Rightarrow$   $V = 3.23 \text{ V}$

5

(c) Input current  $I_{B1} = \frac{5 - 1.4}{100 \text{ k}} = 36 \text{ } \mu\text{A}$

If both transistors active then  $I = [\beta + (1 + \beta)/\beta] I_{B1} = 367 \text{ } \mu\text{A}$

But this would imply  $V_{C1} = V_{C2} = 10 - 47 \times 0.367 = -7.26 \text{ V}$

$\Rightarrow$  LH transistor SATURATED, RH transistor ACTIVE

5

In this case  $V_{C1} = V_{C2} = V_{BE2} + V_{CESAT1} \approx 0.9 \text{ V}$

and  $I = (10 - 0.9)/47 = 194 \text{ } \mu\text{A}$

(d) Assuming FET is active, we have

$$I_D = K(-V_S - V_t)^2 = V_S/R \quad \text{or} \quad (2 - V_S)^2 = V_S \quad (KR = 1 \text{ V}^{-1})$$

$$\Rightarrow V_S^2 - 5V_S + 4 = 0$$

$$(V_S - 4)(V_S - 1) = 0 \Rightarrow V_S = 4 \text{ or } V_S = 1$$

First solution puts FET below threshold  $\Rightarrow V_S = 1$

and  $I = K(-1 - V_t)^2 = 0.1 \text{ mA}$

Check mode:  $V_{DS} = 3$ ;  $V_{GS} - V_t = 1 \Rightarrow$  ACTIVE

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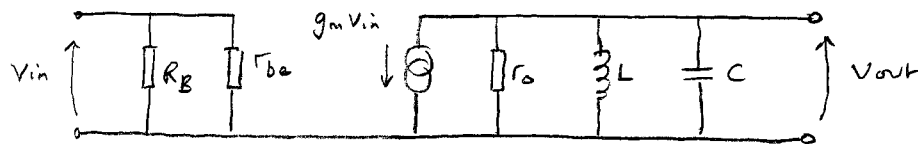
2. (a)  $I_C = 1\text{mA}$ ,  $\beta = 100 \Rightarrow$  require  $I_B = 10\mu\text{A}$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \Rightarrow \underline{R_B = 830\text{ k}\Omega} \quad \text{assuming } V_{BE} \sim 0.7\text{V}$$

Inductor is short-circuit at DC  $\Rightarrow \underline{V_{out} = +9\text{V}}$

4

(b) SSEC:



KCL @ dfr:  $g_m V_{in} + \frac{V_{out}}{r_o} + \frac{V_{out}}{Z_L} + \frac{V_{out}}{Z_C} = 0$

$Z_L = j\omega L$ ,  $Z_C = 1/j\omega C$

$$A_v = \frac{V_{out}}{V_{in}} = -g_m (r_o \parallel Z_L \parallel Z_C) = -g_m (r_o \parallel Z_{LC})$$

At resonance  $|Z_{LC}| \rightarrow \infty$  and  $A_v \rightarrow -g_m r_o = -\frac{I_C}{V_T} \frac{V_A}{I_C}$

Putting  $V_A = 120\text{V}$ ,  $V_T = 25\text{mV}$   $\underline{A_v = -4800}$

8

(c) Centre frequency is  $f_0 = \frac{1}{2\pi\sqrt{LC}}$ , and  $Q = 2\pi f_0 RC = \frac{R}{2\pi f_0 L}$

Require  $Q = 100$ ,  $f_0 = 1\text{MHz}$  with  $R = r_o = 120\text{ k}\Omega \Rightarrow \underline{C = 133\text{ pF}}$

$\underline{L = 191\text{ pH}}$

4

(d) Actual  $Q$  is 60  $\Rightarrow R = \frac{60}{100} \times 120\text{ k}\Omega = 72\text{ k}\Omega$

So equivalent parallel resistance of inductor  $R_L$  is such that  $R_L \parallel 120\text{ k}\Omega = 72\text{ k}\Omega \Rightarrow R_L = 180\text{ k}\Omega$

To transform  $R_L$  to series resistance  $r_L$  use

$$r_L = \frac{R_L}{Q_L^2} = \frac{(2\pi f_0 L)^2}{R_L} \Rightarrow \underline{r_L = 8.0\text{ }\Omega}$$

4



3 (a)  $R_G$  sets operating point by imposing the condition  $V_{GD} = 0$  on both FETs.

Both FETs active, and  $I_{D1} = I_{D2} = I_D$  (since  $I_G = 0$ )

$$\Rightarrow I_D = K_1 (V_{out} - V_{t1})^2 = K_2 (V_{out} - V_{DD} - V_{t2})^2$$

$$\sqrt{\rightarrow} \quad \sqrt{K_1/K_2} (V_{out} - V_{t1}) = \pm (V_{out} - V_{DD} - V_{t2})$$

Both FETs above threshold  $\Rightarrow$  take -ve sign

$$\Rightarrow V_{out} [1 + \sqrt{K_1/K_2}] = V_{DD} + V_{t2} + \sqrt{K_1/K_2} V_{t1}$$

$\Rightarrow$  given result

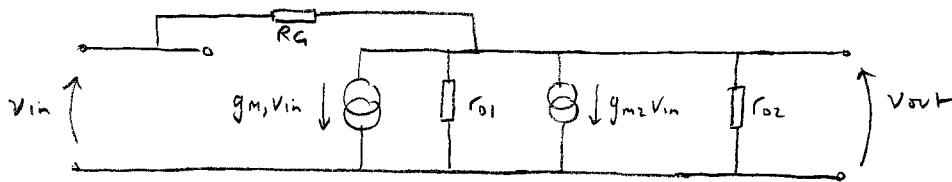
Putting  $V_{DD} = 5$ ,  $V_{t1} = 1$ ,  $V_{t2} = -1$ ,  $\sqrt{K_1/K_2} = 0.5$

$$\Rightarrow V_{out} = (5 - 1 + 0.5)/(1 + 0.5) = \underline{\underline{3V}}$$

$$I_D = K_1 (V_{out} - V_{t1})^2 \Rightarrow \underline{\underline{I_D = 0.4 \text{ mA}}}$$

8

(b) Q1, Q2 in parallel in SSEC:



KCL @ d/f:

$$g_{m1}V_{in} + g_{m2}V_{in} + \frac{V_{out}}{r_{o1}} + \frac{V_{out}}{r_{o2}} + \frac{V_{out} - V_{in}}{R_G} = 0$$

$$\Rightarrow A_v = \frac{V_{out}}{V_{in}} = - \left( g_{m1} + g_{m2} - \frac{1}{R_G} \right) \cdot (r_{o1} \parallel r_{o2} \parallel R_G)$$

$$g_{m1} = 2\sqrt{K_1 I_D} = 0.4 \text{ mS}, \quad g_{m2} = 0.8 \text{ mS}, \quad r_{o1} = r_{o2} = \frac{V_A}{I_D} = 250 \text{ k}\Omega$$

$$\Rightarrow \underline{\underline{A_v = -148}}$$

$$i_{in} = \frac{V_{in} - V_{out}}{R_G} = \frac{V_{in} [1 - A_v]}{R_G}$$

$$R_{in} = \frac{V_{in}}{i_{in}} = \frac{R_G}{[1 - A_v]} \Rightarrow \underline{\underline{R_{in} = 67 \text{ k}\Omega}}$$

8

(c) Gain is large, so can ignore deviations in  $V_{GS}$  when determining output voltage swing.

$$V_{GS1} = 3V \Rightarrow Q1 \text{ active provided } V_{out} > 3 - 1 = 2V$$

$$V_{GS2} = -2V \Rightarrow Q2 \text{ active provided } V_{out} - 5 < -2 + 1 \text{ or } V_{out} < 4V$$

$$\Rightarrow V_{out} \text{ range is } 2 < V_{out} < 4$$

ie. max o/p amplitude = 2V pk-pk

$$\text{and corresponding max i/p amplitude} = \frac{2}{148} = \underline{\underline{13.5 \text{ mV pk-pk}}}$$

4

- 4 (a) Class A : No cross-over distortion, but high power dissipation  
 Class B : Low power, but with severe distortion at cross-over  
 Class AB : Good compromise; slightly higher power than Class B, but with much lower distortion

4

- (b) If base currents are neglected,  $I_N - I_P = I_L$  follows trivially from KCL at output. Also we have;

$$I_N = I_S \exp\left(\frac{V_{in} + V_B - V_{out}}{V_T}\right), \quad I_P = I_S \exp\left(\frac{V_{out} - V_{in} + V_B}{V_T}\right)$$

Taking product of these equations gives  $I_N I_P = I_S^2 \exp\left(\frac{2V_B}{V_T}\right) = I_Q^2$   
 $I_Q$  is the quiescent current in each output transistor when  $I_L = 0$

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- (c) Eliminating  $I_P$  from the above equations gives:

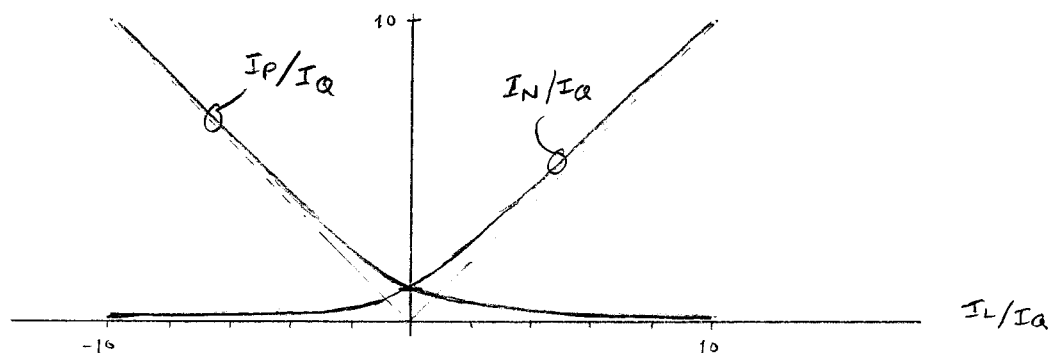
$$I_N - \frac{I_Q^2}{I_N} = I_L \quad \text{or} \quad I_N^2 - I_L I_N - I_Q^2 = 0$$

$$\Rightarrow I_N = \frac{I_L \pm \sqrt{I_L^2 + 4I_Q^2}}{2}$$

$I_N > 0 \Rightarrow$  take +ve sign

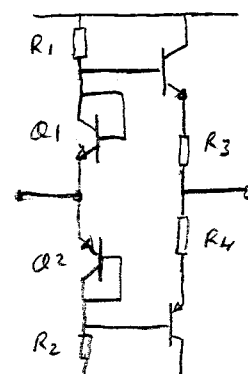
For  $I_L = I_Q$ :  $I_N = \frac{(1 + \sqrt{5})}{2} I_Q = 1.62 I_Q \Rightarrow I_P = 0.62 I_Q$

For  $I_L = 10 I_Q$ :  $I_N = \frac{(10 + \sqrt{104})}{2} I_Q = 10.1 I_Q \Rightarrow I_P = 0.099 I_Q$



6

- (d) Bias sense provides  $V_{BE}$  corresponding to desired bias current, and needs to track thermal variations in d.p. transistors to avoid thermal instability. Diode or diode-connected transistor is obvious candidate.  $R_1, R_2$  provide biasing for  $Q1, Q2$ .  $R_3, R_4$  included for improved stability.



4

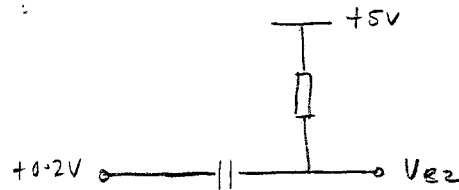
5 (a) In steady state,  $I_{CAP} = 0 \Rightarrow I_{B2} = \frac{5-0.7}{100k} = 43 \mu A$ ,  $V_{B2} = 0.7V$   
 also  $\beta I_{B2} = 8.6 mA > \frac{5V}{1k} \Rightarrow Q2$  saturated with  $V_{C2} = 0.2V$

Since  $V_{C2} \ll 0.5V$ , and  $S1$  open,  $I_{B1} \sim 0 \Rightarrow$   
 $V_{B1} = 0.2V$   
 $V_{C1} = 5V$  6

(b) When  $S1$  is closed ( $t=0$ ),  $Q1$  turns ON (saturated), and  $V_{C1}$  drops to  $\sim 0.2V$ .  $V_{CAP}$  cannot change instantaneously, so  $V_{B2}$  at  $t=0^+$  is

$$V_{B2} \Big|_{t=0^+} = V_{C1} - V_{CAP} = 0.2 - (5 - 0.7) = -4.1V$$

While  $Q2$  remains OFF,  $V_{B2}$  varies as for following circuit:



Steady state for this config is  $V_{B2} \Big|_{t \rightarrow \infty} = +5V$

$\Rightarrow$  Quoting standard result:

$$V_{B2} = 5 + (-4.1 - 5)e^{-t/\tau} \quad \text{while } Q2 \text{ is off}$$

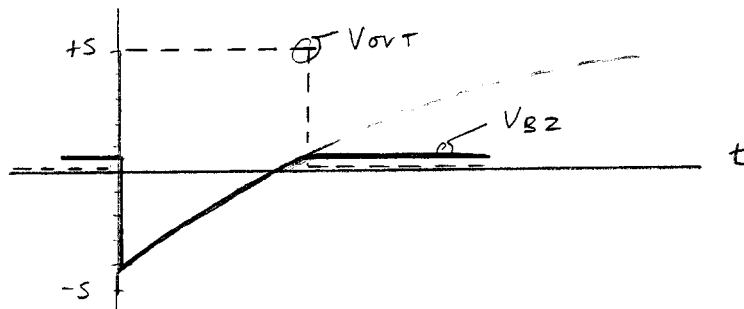
where  $\tau = RC = 6.2 \mu F \times 100k\Omega = 620 \text{ msec}$

When  $V_{B2}$  reaches  $\sim 0.7$ ,  $Q2$  turns ON again and clamps  $V_{B2}$  at this level.

$\Rightarrow$  overall time variab is

$$V_{B2} = \begin{cases} 5 - 9.1 e^{-t/\tau} & t \leq T \\ 0.7 & t \geq T \end{cases}$$

where  $T$  is given by  $0.7 = 5 - 9.1 e^{-T/\tau}$  or  $T = \tau \ln(9.1/4.3) = \underline{\underline{465 \text{ msec}}}$



(c)  $R_F$  provides +ve feedback, holding  $Q1$  ON until  $t=T$ , even if  $S1$  is released early. Without  $R_F$ , releasing  $S1$  early would terminate pulse.

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