EE3-01
EE9-AC1

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2014-15

MSc and EEE PART III/IV: MEng, BEng and ACGI

Corrected Copy

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Wednesday, 17 December 9:00 am

correction 3(c)

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : C. Toumazou
Second Marker(s) : P. Georgiou

1. (a) Figures 1(a) and 1(b) show two popular biasing schemes typically used in analogue integrated systems. Briefly outline the main feature of each of these circuits.

[4]

For the bandgap voltage reference circuit of Figure 1(a), show that $\delta V_0 / \delta T = 0$ (where T is temperature) if $(R_2/R_3) ln [I_1/I_2] = 29$ for $V_0 = 1.283$ V. Assume the temperature coefficient of V_{BE} to be -2.5mV/°C, the collector current of transistor Q_3 is 100μA and the device saturation current is $I_S = 1.2 \times 10^{-13} A$. Boltzmann's constant $k = 1.38 \times 10^{-23} J/K$ and the electron charge is $q = 1.6 \times 10^{-19} C$.

[7]

(b) Show that the circuit of Figure 1(b) can be developed into a current source with output current directly proportional to absolute temperature and virtually independent of supply voltage. It is likely that on power-up the output current will fall into a zero current state. Sketch a suitable start-up circuit that ensures that this condition will not occur and explain the operation of the circuit.

[9]

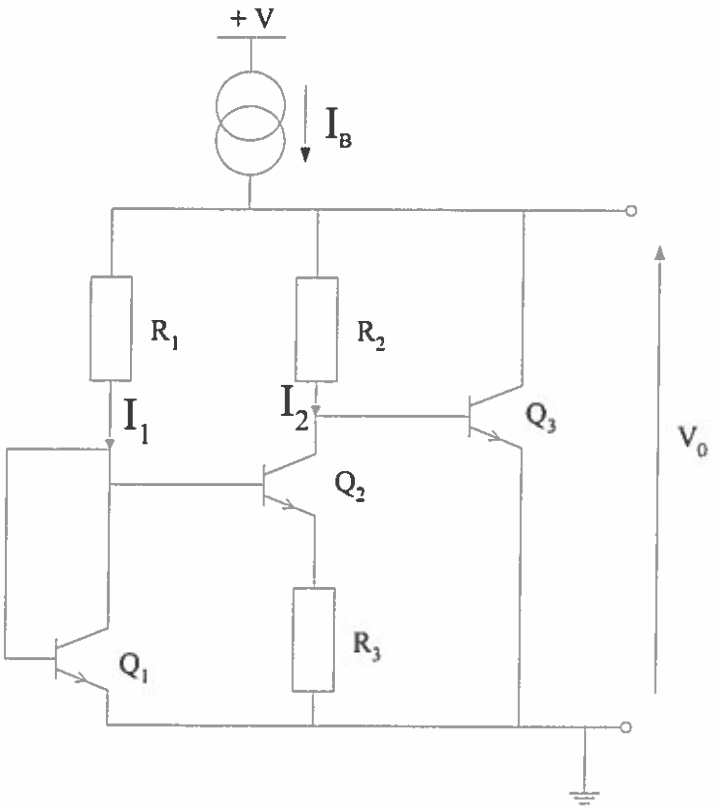

Figure 1(a)

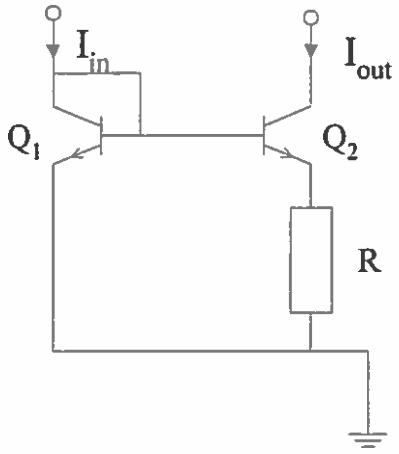

Figure 1(b)

2. (a). Figure 2 shows a two-stage CMOS op-amp. Estimate the low-frequency differential voltage gain and gain-bandwidth product of the amplifier. Aspect ratios of all devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below. What is the main advantage and disadvantage of a single-stage compared to a two-stage op-amp ?

[10]

(b). Show how the output transistors can be cascoded to increase the voltage gain. State two advantages and two disadvantages of a cascoded output stage.

[10]

CMOS TRANSISTOR PARAMETERS

MODEL PARAMETERS	$Kp\ (\mu A/V^2)$	$\lambda\ (V^{-1})$	$V_{TO}\ (V)$
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

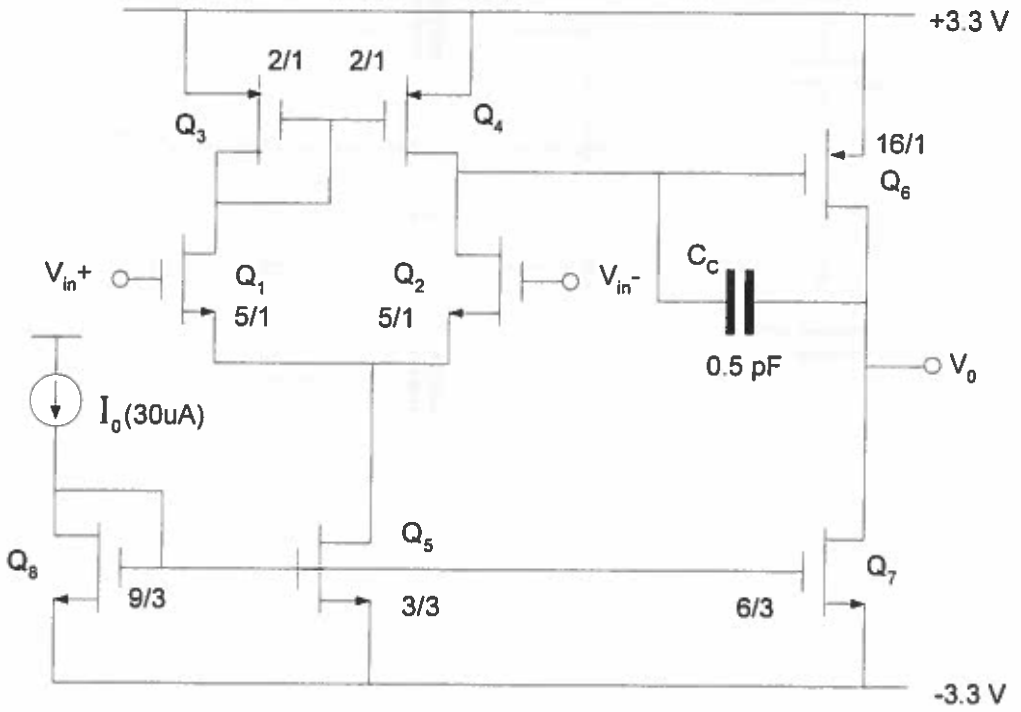

Figure 2.

3. Figure 3 shows a differential opamp which is based upon a folded cascode design

(a). Explain what is meant by folded cascode.

[4]

(b). Sketch a circuit diagram of the folded cascode opamp including a circuit which ensures the common mode voltage is maintained at the output.

[6]

(c). Derive the equation for the linear differential resistor of the circuit shown in Figure 4. Assuming the time constant of the circuit is τ=10ms, calculate the value of feedback capacitor, C, assuming input transistors Q1 and Q2 are operating in the triode region and have W/L=5, K=20uA/V2, Vg=1V, Vt=0.5V and node x is at a common mode of 0 V. You may neglect any body effects.

[10]

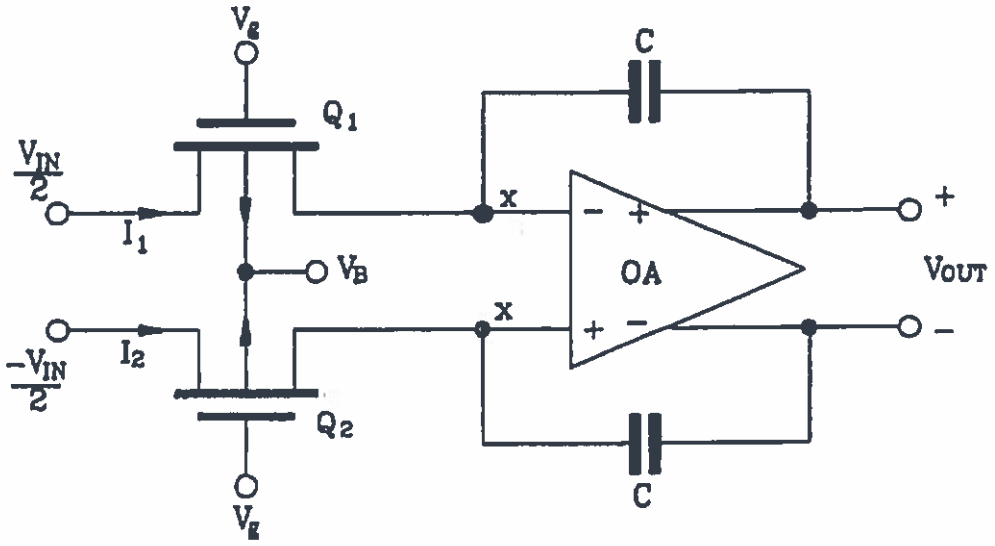

Figure 3.

4. (a) Explain the principles of sigma delta modulation and sketch a typical circuit architecture.

[10]

(b) Figure 4 shows one bit of an algorithmic data converter. Show how this can be cascaded to perform an 8-bit data conversion.

[7]

(c) What noise limits the resolution of a sampled-data converter?

[3]

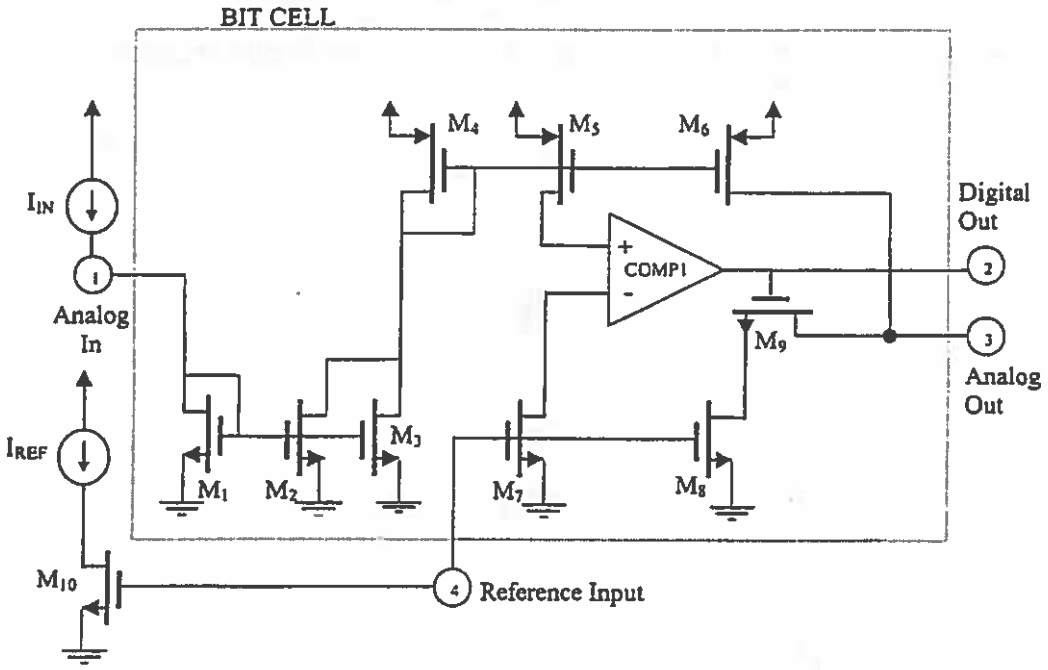

Figure 4.

5. Figure 5 shows the basic design of an analogue sampled-data precision integrator.

(a) Derive an expression for the transfer function of the integrator. Assume that the integrator is driven by non-overlapping clocks and that the switches are ideal.

[10]

(b) (i) Sketch the basic design of a 3rd-order Chebyshev low pass switched-capacitor ladder filter.

The filter is to have a cut-off frequency of 5kHz. Assume a clocking frequency of 100 kHz. The values of integration capacity for the capacitor based sections are 5.06pF and inductive section is 3.49pF. All other switched capacitors are 1pF.

(ii) From the circuit, estimate normalised passive component values for the original double-terminated LC prototype of the filter. All values should be normalised to 1 rad/s. You may assume that the clocking frequency is so high that the integrators can be assumed lossless.

[10]

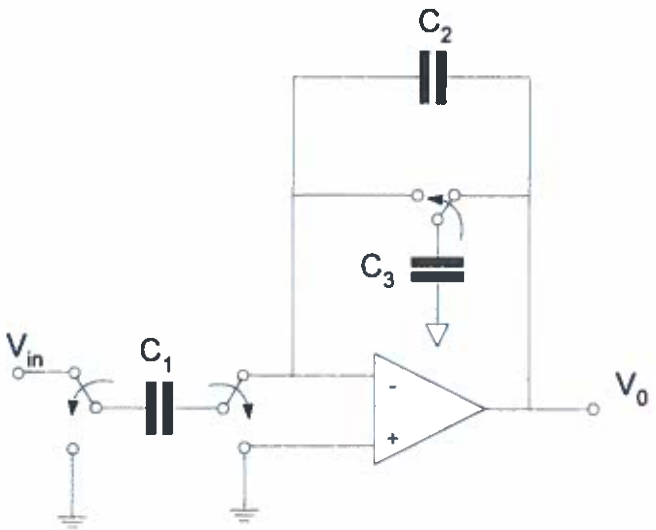

Figure 5.

6. (a) Sketch the circuit of a differential to single ended output high frequency operational amplifier that does not require miller compensation.

[7]

(b) Suggest an enhancement to the circuit in 6.a that would improve the voltage gain of the amplifier and discuss the limitation in doing this.

[3]

(c) When matching transistors special care is taken with the layout. Discuss what is meant by common centroiding when matching two transistors.

[5]

(d) For fully differential output op-amps explain what is meant by common mode feedback.

[5]