EE3-11
EE9-AO8

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2013

MSc and EEE PART III/IV: MEng, BEng.and ACGI

Corrected Copy

ADVANCED ELECTRONIC DEVICES

Tuesday, 15 January 10:00 am

Time allowed: 3:00 hours

There are FIVE questions on this paper.

Answer Question One and THREE other questions.

Question One carries 40 marks. All other questions carry 20 marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : K. Fobelets, K. Fobelets
Second Marker(s) : S. Lucyszyn, S. Lucyszyn

Special instructions for invigilators

Q1 is compulsory

Special instructions for students

Q1 is compulsory.

Constants

permittivity of free space:	$\varepsilon_o = 8.85 \times 10^{-12}$ F/m
permeability of free space:	$\mu_o = 4\pi \times 10^{-7}$ H/m
intrinsic carrier concentration in Si:	$n_{i\,Si} = 1.45 \times 10^{10}$ cm^{-3} at T = 300K
intrinsic carrier concentration in GaAs:	$n_{i\,GaAs} = 1.79 \times 10^{6}$ cm^{-3} at T = 300K
intrinsic carrier concentration in InAs:	$n_{i\,InAs} = 1 \times 10^{15}$ cm^{-3} at T = 300K
dielectric constant of SiO_2:	$\varepsilon_{ox} = 4$
dielectric constant of Si:	$\varepsilon_{Si} = 12$
dielectric constant of GaAs:	$\varepsilon_{GaAs} = 13$
dielectric constant of InAs:	$\varepsilon_{InAs} = 15$
electron affinity of Si	$\chi_{Si} = 4.05$ eV
electron affinity of GaAs	$\chi_{GaAs} = 4.1$ eV
electron affinity of InAs	$\chi_{InAs} = 4.9$ eV
electron affinity of AlAs	$\chi_{AlAs} = 3.6$ eV
effective density of states of Si:	$N_{C\,Si} = 2.8 \times 10^{19}$ cm^{-3}
	$N_{V\,Si} = 1.04 \times 10^{19}$ cm^{-3}
effective density of states of GaAs:	$N_{C\,GaAs} = 4.7 \times 10^{17}$ cm^{-3}
	$N_{V\,GaAs} = 9.0 \times 10^{18}$ cm^{-3}
effective density of states of InAs:	$N_{C\,InAs} = 8.7 \times 10^{16}$ cm^{-3}
	$N_{V\,InAs} = 6.6 \times 10^{18}$ cm^{-3}
thermal voltage:	kT/e = 0.026V at T = 300K
charge of an electron:	$e = 1.6 \times 10^{-19}$ C (1 eV)

Workfunction of metals

metal	ϕ (eV)
Al	4.08
Ni	5.01
Ti	4.33
W	4.6

Formulae

$$p = N_v e^{(E_v - E_F)/kT}$$

$$n = N_c e^{(E_F - E_c)/kT}$$

Carrier density

$$I_{DS} = \frac{\mu C_{ox} W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right)$$

MOSFET current

$$V_{th} = \phi_m - \phi_s + 2\times\phi_F + \gamma\times\sqrt{2\times\phi_F}$$

Threshold voltage

$$\phi_F = \frac{kT}{e}\ln\left(\frac{N_A}{n_i}\right)$$

Fermi potential (difference between intrinsic and Fermi level)

$$\gamma = \frac{\sqrt{2e\varepsilon_s N_A}}{C_{ox}}$$

Body effect coefficient

$$J = \frac{eD_n n_p}{L_n}\left(e^{\frac{eV}{kT}} - 1\right) + \frac{eD_p p_n}{L_p}\left(e^{\frac{eV}{kT}} - 1\right)$$

Diode diffusion current density

$$V_{bi} = \frac{kT}{e}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Built-in voltage pn diode

$$W_{depl}(V) = \left[\frac{2\varepsilon(V_{bi} - V)}{e}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]^{1/2}$$

Depletion width in pn diode

$$S = \frac{dV_{GS}}{dLog(I_{DS})}$$

Sub-threshold swing

1. Compulsory question.

a) What is the main cause for short channel effects in MOSFETs? Explain your answer briefly (max. 40 words). [2]

b) In figure 1.1 the transfer characteristic of a MOSFET is given for V_{DS} in the linear region. Three regions are indicated: I, II, III. Explain the shape of the current in each region. ([3] marks for I & III, [2] for region II) [8]

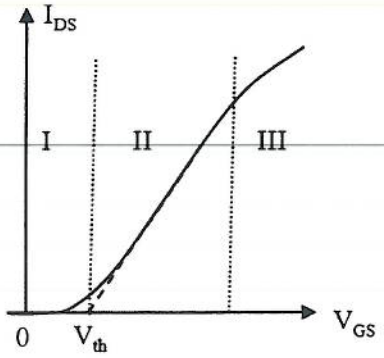


Figure 1.1: The transfer characteristic of a MOSFET in the triode region.

c) Sketch the energy band diagram (E_c, E_v, E_F) of a depletion mode n-channel MOSFET at threshold. The workfunction of the gate contact and the semiconductor are the same. [4]

d) Make different 2D or one 3D sketch of a finFET, indicating clearly the channel, gate and source/drain geometries. ([2] marks per geometry) [6]

e) Dependent on the body thickness, MOSFETs can be fabricated in fully depleted or partially depleted SOI. Why is FDSOI preferred? [4]

f) Figure 1.2 gives the cross section of a pMOSFET in which SiGe is used for elevated source and drain contacts. Give two reasons why this configuration generates a higher transconductance, g_m. ([3] marks each) [6]

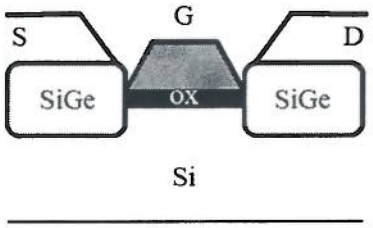


Figure 1.2: Cross section of a MOSFET with elevated SiGe source and drain.

QUESTION CONTINUES ON NEXT PAGE!

g) Figure 1.3 gives the layer structure of a HEMT. Explain the function of layers I and II. ([2] marks each). [4]

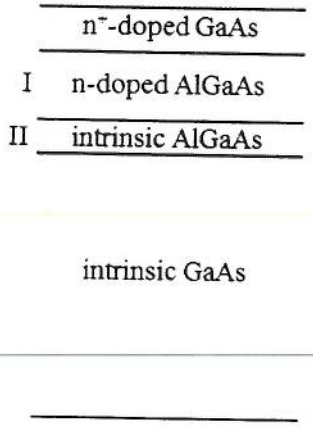


Figure 1.3: Layer structure of a HEMT.

h) Sketch the energy band diagram (E_c, E_v, E_F, E_G), along the dashed line, of the material system given in Figure 1.4. Take the semiconductor-metal interfaces into account. Al is aluminium, W is tungsten. The work function of p-GaAs is: $\phi = 4.75$ eV and of n-AlAs is $\phi = 4$ eV. [6]

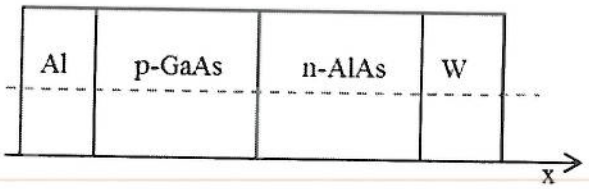


Figure 1.4: Heterojunction with metal contacts. All layers are long such that the different interfaces do not interact.

2. In figure 2.1, the material cross section of an nMOS is given. The workfunction of the gate contact is equal to that of the substrate. The source and drain implants are deep, the depth of the implants is larger than the depletion widths. The gate length is 1 μm and the width 5 μm.

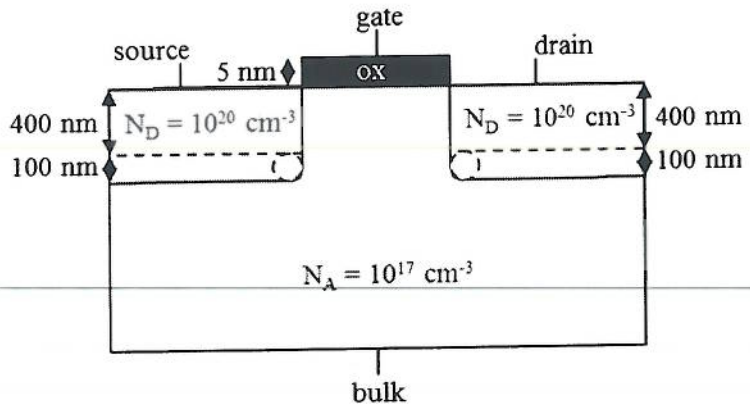


Figure 2.1: Material cross section of an nMOS.

a) Sketch the material cross section of the nMOS and add the depletion regions ([4] marks), where appropriate, for a biasing condition in the triode (linear) region at threshold. The source and bulk contact are grounded. Indicate the region(s) in which charge sharing occurs ([2] marks). [6]

b) Calculate the change in the threshold voltage, ΔV_{th} that has occurred when $V_{DS} = 0.1$ V and $V_{GS} > V_{th}$. (2 × [3] marks for the correct equations, [2] marks for the correct numerical answer) [8]

c) How does ΔV_{th} change when a bulk bias of $V = -1$ V is applied? Explain your answer briefly. [3]

d) Explain what needs to change in the approach taken in b) to calculate ΔV_{th} when the junction depth is decreased to 100 nm? [3]

3. Figure 3.1 gives the material cross section of a GaAs MESFET. The GaAs surfaces are passivated and thus do not have interface states. The gate length is 1 μm and the width is 5 μm.

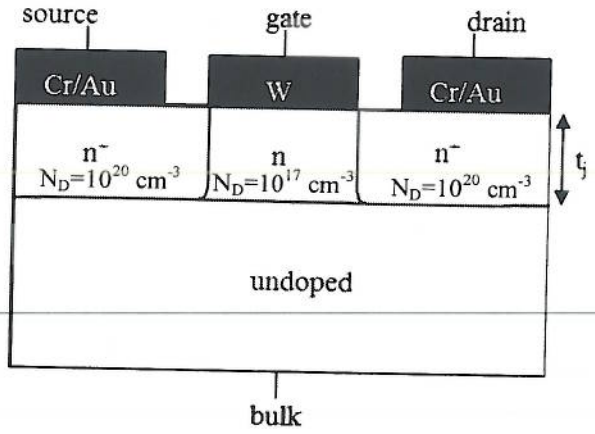


Figure 3.1: Material cross section of a GaAs MESFET.

a) Sketch the energy band diagram (E_c, E_v, E_F, E_G), from the gate through the channel into the substrate, when no bias is applied on the contacts. Indicate the build-in voltage. [6]

b) What is the type of the gate contact ([1] mark) and how will this contact control the density of carriers in the channel ([3] marks)? [4]

c) Calculate the minimum thickness of t_j for the MESFET to be depletion mode ([3] marks). You can make your calculations for $V_{DS} = V_{BS} = 0$V. Explain your approach ([3] marks). [6]

d) How would t_j change if we use InAs instead of GaAs for the MESFET and an interface state density of $Q_i = 10^{11}$ C is present? [4]

4. In figure 4.1, the material cross section of a long gate length Si pMOS is given. The gate metal is Al. The substrate doping is $N_D = 5\ 10^{16}$ cm^{-3}, the ohmic contact doping is $N_A = 10^{20}$ cm^{-3}, the oxide thickness is 2 nm and the gate length and width are, respectively, 1 μm and 10 μm.

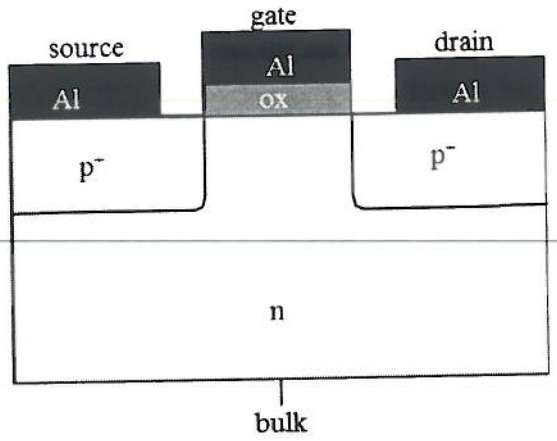


Figure 4.1: Material cross section of a pMOS.

a) Calculate the value of the work function of the Si substrate. [2]

b) Sketch the energy band diagram (E_c, E_v, E_F, E_i, E_G) from the gate through the oxide into the channel for the pMOS at $V_{GS} = V_{DS} = V_{BS} = 0$V. [4]

c) Adapt the expression for the threshold voltage, V_{th} of the nMOS, given in the formulae sheet, to describe the threshold voltage of the pMOS as a function of material parameters and geometry. [4]

d) Calculate the value of the threshold voltage. [2]

e) By what value will the threshold voltage in d) change if the oxide is replaced by a high-k dielectric of the same thickness ([4] marks) and, as a result, a positive interface charge occurs at the dielectric/Si interface ([4] marks). The dielectric constant of the high-k insulator is $\varepsilon_{h\text{-}k} = 8$. The interface trapped charges density is $n_i = 10^{12}$ cm^{-2}. [8]

5.

a) Sketch a material cross section of a Si CMOS inverter on a p-Si substrate. [6]

b) Draw the parasitic latch-up circuit consisting of coupled BJTs in the sketch of a). [4]

c) How can this latch-up be completely avoided in Si technology? [4]

d) The conduction band diagram of an n-channel III-V HEMT is given in Figure 5.1.

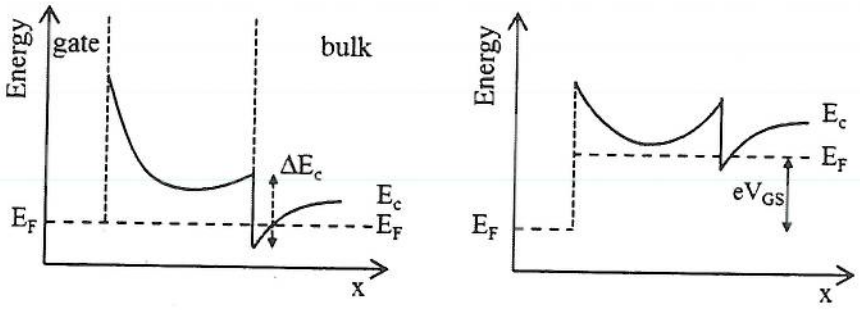


Figure 5.1 : Left: the conduction band of an AlGaAs/GaAs high electron mobility transistor without applied bias. Right: the conduction band of an AlGaAs/GaAs high electron mobility transistor with the gate forward biased.

i) Calculate the conduction band offset ΔE_c for an AlAs concentration of 30% in the AlGaAs layer for the unbiased HEMT. [3]

ii) Explain the deteriorating effects on the performance of the HEMT when the gate is forward biased. Refer to the energy band diagram in your explanation. [3]

ANSWERS 2013

1. Compulsory question.

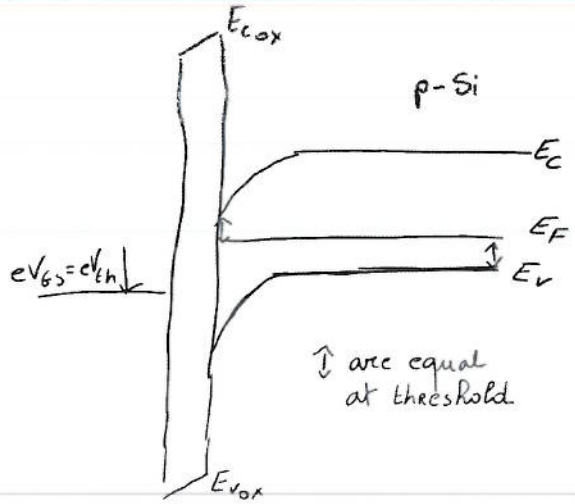
a) Short channel effects are mainly caused by the influence of the drain voltage on the depletion charges in the channel. This influence increases when the channel length decreases. [4]

b) I: weak inversion region. The channel is not yet inverted. There is a diffusion current caused by the variation in carrier concentration between source and drain. This current is exponential such as in a BJT.

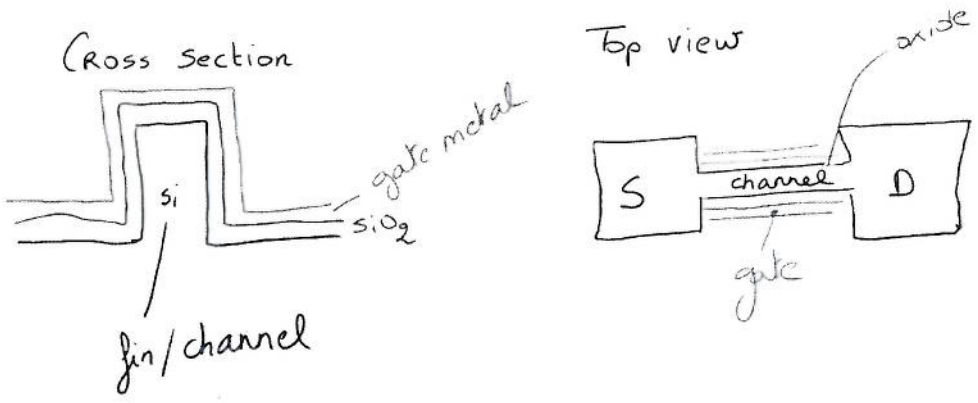
II: strong inversion. There is an inversion layer in the channel. In this case, current is mainly flowing as a result of drift of inversion layer charges. This current is approximately linear as a function of gate voltage in the triode region.

II: At high voltages, there is a high electric field pointing from the gate into the channel. This causes an increase in scattering of the charges at the Si/SiO_2 interface (interface roughness scattering). Thus the mobility decreases. [6]

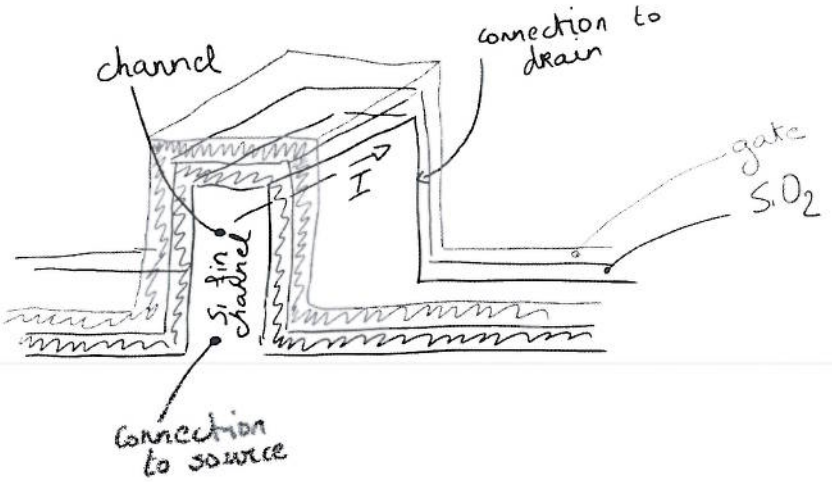
c) It does not matter that the workfunction of the gate contact and the semiconductor are the same for the sketch. [4]



d) [6]



or



f) In partially depleted SOI the body thickness is sufficiently thin for the body to be depleted at VGS=0V. It remains depleted during operation and thus avoids storage of holes when electron hole pair generation occurs in the drain side depletion region. This prevents the kink effect: sudden increase in the current due to a shift in the threshold voltage in the saturation region. [4]

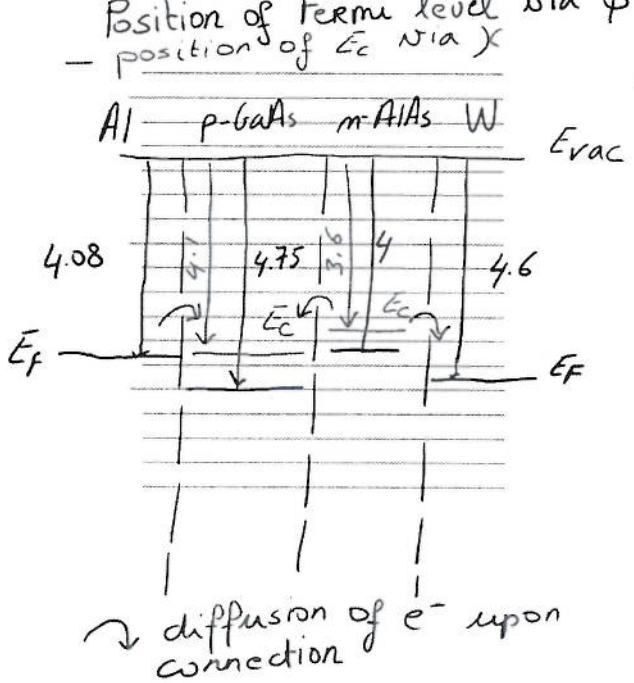
e) 1. Elevate source and drain contacts decrease the resistance of the ohmic contacts and thus maintained higher external g_m

2. the SiGe has a higher lattice constant than the Si, this is causing local strain in the Si channel. As a result the mobility increases and thus g_m increases. [6]

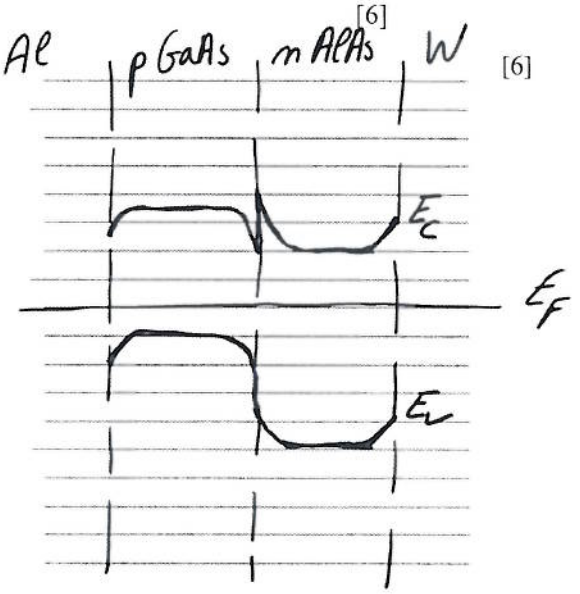
g) I is the supply layer. The purpose of the supply layer is to donate electrons to the GaAs channel that will occur under the un AlGaAs layer. This is called modulation doping and separates doping atoms from channel, maintaining high carrier mobility. [4]

II is the set-back layer. It separates the ionised charges in the supply layer (positively charged donor atoms) from the

h) [6]

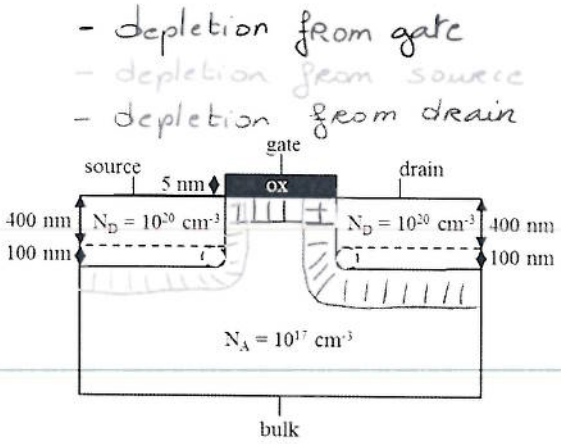


[6]



2.

a) In triode region → linear variations of the depletion width of the gate and no pinch-off. Since VDS ≠ 0 the depletion region from the drain should be slightly larger than that from the source. Depletion regions should be smaller than the implant depths. Charge sharing is where the depletion region of the source and of the drain overlap with the depletion region of the gate. [5]



b) Important in calculations are the equations that are chosen. Values should only be entered in the very last step.

Depletion width for the source and drain – use the pn junction depletion width. V = 0V for source but V = 0.1V for drain. Formulae come from the list. Since the doping density difference between the bulk doping and the ohmic contact doping is 3 orders of magnitude different, we can assume that the depletion region extends mainly into the bulk.

$$W_{depl}(V) = \left[\frac{2\varepsilon(V_{bi}-V)}{e}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)\right]^{1/2} \qquad V_{bi} = \frac{kT}{e}\ln\left(\frac{N_A N_D}{n_i^2}\right) = 0.026V \ln\left(\frac{10^{17}10^{20}}{(1.45\,10^{10})^2}\right) = 0.998V$$

The depletion width caused by the gate is at its maximum as inversion is reached. This happens when $V_s = 2\,\phi_F$.

$$W_{depl}^{S} \approx \left[\frac{2\varepsilon(V_{bi})}{e}\left(\frac{1}{N_A}\right)\right]^{1/2} = \left[\frac{2\times12\times8.85\,10^{-14}\;0.998}{1.6\,10^{-19}}\left(\frac{1}{10^{17}}\right)\right]^{1/2} = 1.15\,10^{-5}cm$$

$$W_{depl}^{D} \approx \left[\frac{2\varepsilon(V_{bi}-V)}{e}\left(\frac{1}{N_A}\right)\right]^{1/2} = \left[\frac{2\times12\times8.85\,10^{-14}\;(0.998+0.1)}{1.6\,10^{-19}}\left(\frac{1}{10^{17}}\right)\right]^{1/2} = 1.21\,10^{-5}cm$$

$$W_{depl}^{G}(V=2\phi_F) \approx \left[\frac{2\varepsilon 2\phi_F}{e}\left(\frac{1}{N_A}\right)\right]^{1/2}$$

$$\phi_F = \frac{kT}{e}\ln\left(\frac{N_A}{n_i}\right) = 0.026V \ln\left(\frac{10^{17}}{1.45\,10^{10}}\right) = 0.41V$$

$$W_{depl}^{G}(V) \approx \left[\frac{2\varepsilon 2\phi_F}{e}\left(\frac{1}{N_A}\right)\right]^{1/2} = \left[\frac{4\times12\times8.85\,10^{-14}\times0.41}{1.6\,10^{-19}}\left(\frac{1}{10^{17}}\right)\right]^{1/2} = 1.04\,10^{-5}cm$$

$$\Delta V_{th} = \frac{\Delta Q}{C_{ox}} = \frac{eN_A\left(W_{depl}^G W_{depl}^S W + W_{depl}^G W_{depl}^D W\right)}{2\varepsilon_0\varepsilon_{Si} LW} = \frac{eN_A W_{depl}^G\left(W_{depl}^S + W_{depl}^G W_{depl}^D\right)}{2\varepsilon_0\varepsilon_{Si} L}$$

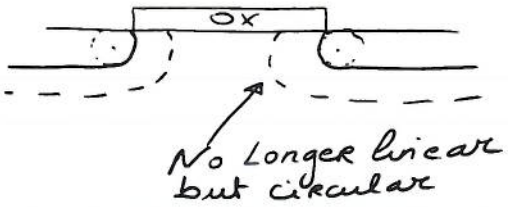
$$\Delta V_{th} = \frac{1.6\times10^{-19}\times1.04\times10^{-5}\left(1.15\times10^{-5}+1.21\times10^{-5}\right)}{2\times12\times8.85\times10^{-14}\times10^{-5}} = \frac{1.6\times10^{-19}\times1.04\times10^{-5}\left(1.15+1.21\right)}{24\times8.85\times10^{-14}} = 1.85\times10^{-12}V$$

[5]

c) Applying V = -1 V on the bulk will cause the bulk to reverse bias. This will shift the threshold voltage via the gate depletion charges. The gate voltage that needs to be applied for inversion is reduced because the reverse bias on the substrate already causes a depletion region. [5]

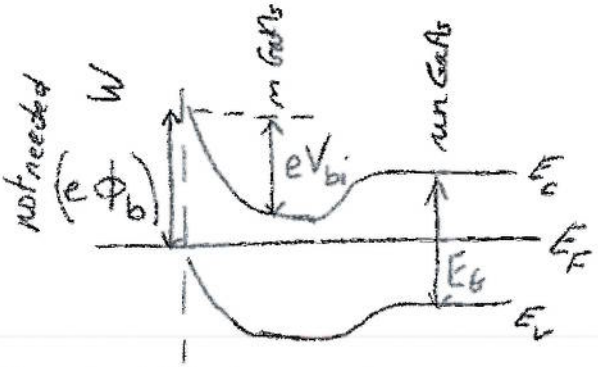
d) When the junction depth is decreased to 100 nm we can no longer use the linear approximation to estimate the charge sharing. This is because the geometry of the doping implants is circular. At 100nm this would happen at the depth of source and drain depletion.

[5]



3.

a) [6]



b) The contact is Schottky contact. A reverse bias on this contact will increase the depletion width from the gate downwards, depleting the n-GaAs channel of mobile carriers. [3] [4]

c) For the MESFET to be depletion mode, a channel must exist at $V_{GS} = 0V$. This means that the width of the n-GaAs layer has to be larger than the depletion width created by the Schottky barrier. The thickness of the n-GaAs layer is given as t_j in the figure. [3].
The expression for a depletion width from the formulae list:

$$W_{depl}(V) = \left[\frac{2\varepsilon(V_{bi} - V)}{e}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]^{1/2}$$

The depletion region of a Schottky contact behaves as a one-sided junction with $N_A >> N_D$.
The built-in voltage is calculated from the work function difference between W and n-GaAs.
However χ is given for GaAs rather than ϕ, thus $\phi = \chi + (E_c - E_F)$.
$\chi_{GaAs} = 4.1$ eV, $N_{C\,GaAs} = 4.7 \times 10^{17}$ cm^{-3}, from the formulae list:

$$n = N_c e^{(E_F - E_c)/kT}$$

$$E_c - E_F = kT \ln\left(\frac{N_c}{n}\right) = 0.026eV \ln\left(\frac{4.7\,10^{17}}{10^{17}}\right) = 0.04eV$$

$$\phi_{GaAs} = 4.1eV + 0.04eV = 4.14eV$$

$$V_{bi} = \phi_W - \phi_{GaAs} = 4.6eV - 4.14eV = 0.46eV$$

$$W_{depl} = \left[\frac{2\varepsilon V_{bi}}{eN_D}\right]^{1/2} = \left[\frac{2\times 13\times 8.85\,10^{-14}\times 0.46}{1.6\times 10^{-19}\times 10^{17}}\right]^{1/2} = 8.1\,10^{-6}cm$$

$$t_j > 81nm$$

[3]. [6]

d) When an interface states are present in InAs, the Fermi level in n-InAs will be pinned under the conduction band. As a consequence no Schottky contact can be made on InAs and thus one cannot form a MESFET. [4]

4.

a) Calculate the value of the work function of the Si substrate. [2]

χ_{Si} = 4.05 eV, N_{VSi} =1.04 × 10^{19} cm^{-3}

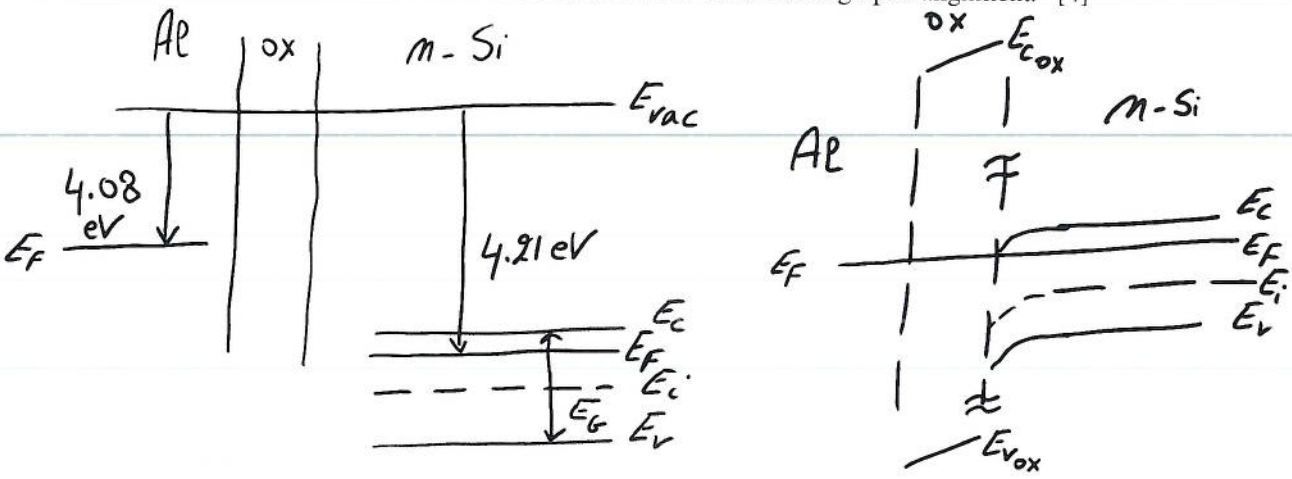
From the formulae list, we take the electron formula because the bandgap is not given:

$$n = N_c e^{(E_F - E_c)/kT}$$

$$E_c - E_F = kT \ln\left(\frac{N_c}{n}\right) = 0.026eV \ln\left(\frac{2.8\,10^{19}}{5\,10^{16}}\right) = 0.164eV$$

$$\phi_{Si} = 4.05eV + 0.164eV = 4.214eV$$

b) Since there is a workfunction difference there will be band bending upon alignment. [4]



c) V_{th} for the nMOS [4]

$$V_{th} = \phi_m - \phi_s + 2\times\phi_F + \gamma\times\sqrt{2\times\phi_F}\,;\phi_F = \frac{kT}{e}\ln\left(\frac{N_A}{n_i}\right);\gamma = \frac{\sqrt{2e\varepsilon_s N_A}}{C_{ox}}$$

V_{th} for the pMOS

$$V_{th} = \phi_m - \phi_s - 2\times\phi_F - \gamma\times\sqrt{2\times\phi_F}\,;\phi_F = \frac{kT}{e}\ln\left(\frac{N_D}{n_i}\right);\gamma = \frac{\sqrt{2e\varepsilon_s N_D}}{C_{ox}}$$

d) Calculate the value of the threshold voltage. [2]

$$\phi_F = 0.026\ln\left(\frac{5\,10^{16}}{1.45\,10^{10}}\right) = 0.39V$$

$$\gamma = \frac{\sqrt{2e\varepsilon_s N_D}}{C_{ox}} = \frac{\sqrt{2\times12\times1.6\times10^{-19}\times8.85\times10^{-14}\times5\times10^{16}}}{4\times8.85\times10^{-14}/2\times10^{-7}} = 0.074\sqrt{V}$$

$$V_{th} = 4.08 - 4.21 - 0.39 - 0.074\times\sqrt{0.39} = -0.57V$$

e) The threshold voltage shifts to more negative values + γ is changing [8]

$$V_{th} = \phi_m - \phi_s - 2\times\phi_F - \gamma\times\sqrt{2\times\phi_F} - \frac{Q_i}{C_{h-k}}; \phi_F = \frac{kT}{e}\ln\left(\frac{N_D}{n_i}\right); \gamma = \frac{\sqrt{2e\varepsilon_s N_D}}{C_{h-k}}$$

$$\gamma = \frac{\sqrt{2e\varepsilon_s N_D}}{C_{h-k}} = \frac{\sqrt{2\times12\times1.6\times10^{-19}\times8.85\times10^{-14}\times5\times10^{16}}}{8\times8.85\times10^{-14}/2\times10^{-7}} = 0.037\sqrt{V}$$

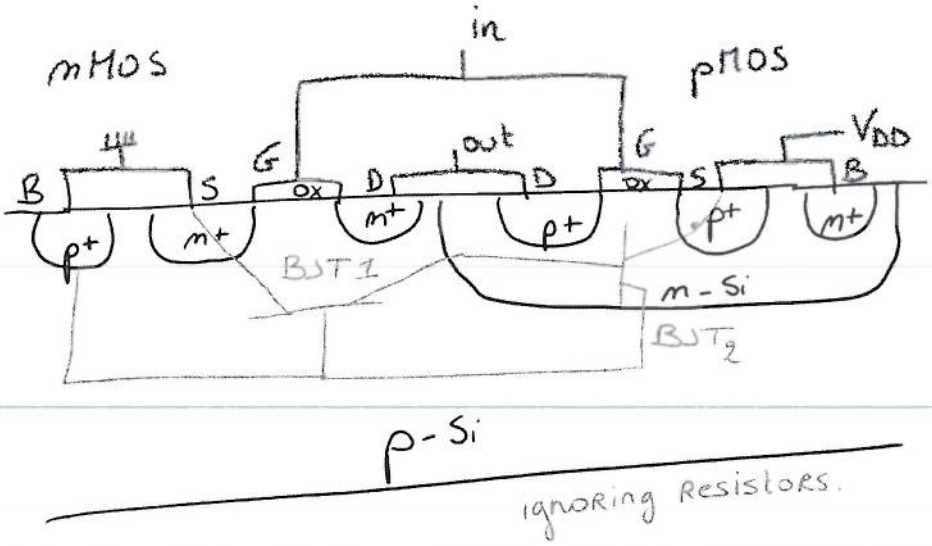
$$\frac{Q_i}{C_{h-k}} = \frac{en_i}{C_{h-k}} = \frac{en_i t_{h-k}}{\varepsilon_0\varepsilon_{h-k}} = \frac{1.6\,10^{-19}\times10^{12}\times2\,10^{-7}}{8\times8.85\,10^{-14}} = 0.045V$$

$$V_{th} = 4.08 - 4.21 - 0.39 - 0.037\times\sqrt{0.39} - 0.045 = -0.59V$$

5.

a) [4]

b) [4]



c) By using SOI (silicon on insulator) substrate. [4]
There are other methods, such as minimising jitter in the input circuit. Ensuring the nMOS bulk potential remains close to ground and the pMOS close to VDD. Increasing the well dopings to reduce the resistances. All these are less effective than using SOI. One can also use only nMOS, but this increases number of FETs.

d)

i) Electron affinity rule: $\Delta E_c = \chi_{GaAs} - \chi_{AlGaAs}$
$\chi_{GaAs} = 4.1$ eV ; $\chi_{AlAs} = 3.6$ eV: $\chi_{AlGaAs} = 0.7 \times 4.1 + 0.3 \times 3.6 = 3.95$eV
$\Delta E_c = 4.1 - 3.95 = 0.15$ eV [2]

ii) A channel is formed in the AlGaAs layer and the channel in the undoped GaAs layer is becoming un-populated. Thus carriers travel now in the doped AlGaAs layer. AlGaAs has a lower electron mobility than GaAs, moreover the channel is now in the heavily doped layer, lowering the mobility further. The reason why the channel appears in the AlGaAs layer is because E_F lies close to E_c in that layer. In addition E_F lies deeper in the QW and thus there will be less carriers populating the energy level in the QW. [2]