

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2012

EEE PART IV: MEng and ACGI

POWER ELECTRONICS

Thursday, 3 May 2:30 pm

Time allowed: 2:00 hours

There are FOUR questions on this paper.

Answer THREE questions.

All questions carry equal marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : T.C. Green, P.D. Mitcheson
 Second Marker(s) : P.D. Mitcheson, T.C. Green

Information for Candidates

There are 4 questions: Answer any 3.

Charge on the electron : 1.6×10^{-19} C
Permittivity of free space: 8.85×10^{-12} Fm $^{-1}$
Relative permittivity of Silicon: 11.7

1. This question concerns the buck SMPS shown in Figure Q1.1. Selected component information is listed below. The supply must be able to output 5 A at 3 V from a 20 V input and is designed to operate in continuous conduction mode.

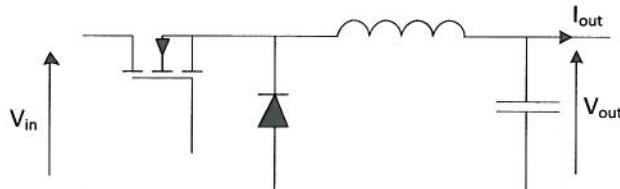


Figure Q1.1 Buck converter

MOSFET: $R_{DSon} = 30 \text{ m}\Omega$, $Q_{gs}=10 \text{ nC}$ (when $I_D=5 \text{ A}$), $Q_{gd}=17 \text{ nC}$ (when $V_{DS}=20 \text{ V}$)

Diode: $V_{on} = 0.7 \text{ V}$ (constant when conducting)

Inductor: $100 \mu\text{H}$ with a $100 \text{ m}\Omega$ series resistance

Capacitor: $1000 \mu\text{F}$, negligible ESR

- Assuming the circuit operates with no losses, what is the required duty cycle? [1]
- Recalculate the required duty cycle for the converter taking into account the diode voltage drop. Use this value of δ where required in the rest of this question. [3]
- The current ripple in the converter must be less than 150 mA. Calculate the minimum switching frequency. Use this frequency where required in other parts of the question. [2]
- Which capacitance in the MOSFET must be charged in order for the drain current to rise at turn-on, and which must be discharged for the drain source voltage to fall at turn-on? [1]
 - Calculate the switching loss in the MOSFET given that the gate drive is capable of sinking and sourcing 1 A. [3]
- Calculate the total power loss in the converter. State any assumptions you make. [3]
- It is decided to replace the diode with another MOSFET, making a synchronous buck converter. Explain why this can be beneficial and explain any additional complexities which result from this modification. [5]
- Calculate the losses in the synchronous converter and hence show that it is more efficient than the non-synchronous version. State any assumptions you make. [2]

2.

- a) Sketch a circuit diagram of a 3-phase inverter. Explain how the switches in the circuit are controlled.

[5]

- b) What is the maximum blocking voltage required by the switches in the circuit of part a)? What is the maximum phase and line voltage that can be created, assuming the phase voltages are sinusoidal?

[3]

- c) Explain how third harmonic injection can be used to increase the line voltage in an inverter. Illustrate your answer by sketching the modified phase voltages. What is the maximum voltage that the switches must block in this case?

[5]

- d) An induction motor can be controlled using slip-compensated speed control. A simplified diagram of this system is shown in Figure Q2.1. Explain the general principle of operation of the scheme and describe the function of the box marked "X".

[4]

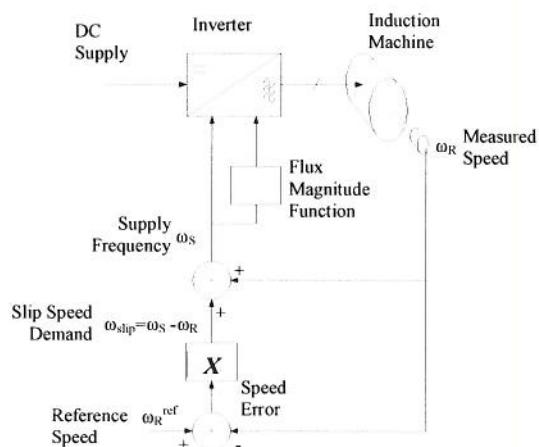


Figure Q2.1 Slip compensated speed control

- e) Figure Q2.2 shows a simplified equivalent circuit of an induction machine. Show that when operating the machine at the rated air gap flux, the magnitude of the stator voltage should be set in proportion to stator frequency at high speed and derive a modified expression for low speed operation.

[3]

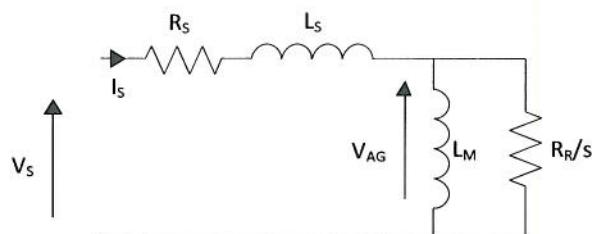


Figure Q2.2 Simplified equivalent circuit of an induction machine

3. International Rectifier (IRF) are designing a new family of power MOSFETs rated to block 250 V. A cross-section through the device is shown in Figure Q3.1. Two doping profiles are being considered for the drift region.

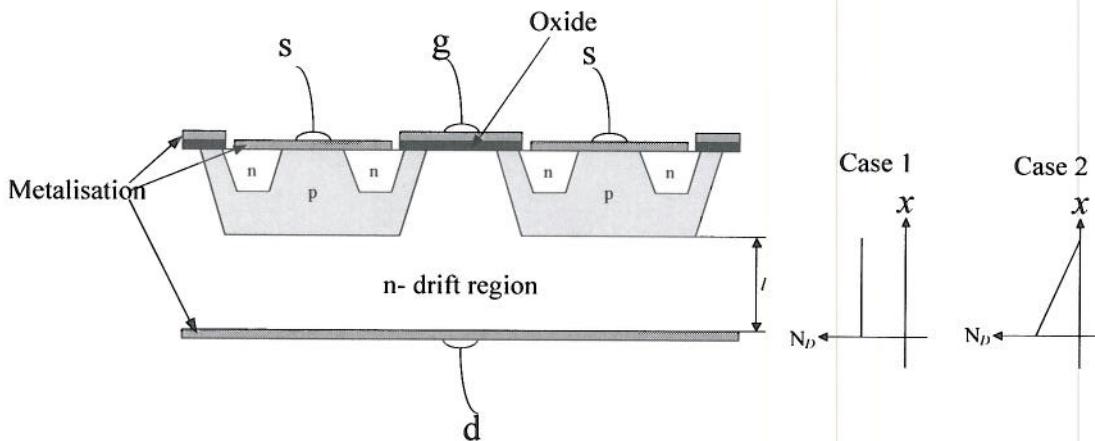


Figure Q3.1 Structure of new proposed IRF MOSFET family with two proposed drift region doping profiles

- Explain why the structure of Fig Q3.1 is used in power MOSFETs and why drain-source resistance eventually becomes too high for efficient device operation as the device is designed for increasing blocking voltage.
[3]
- In the first design iteration, IRF decide to use a constant doping density of the n- drift region of $1 \times 10^{15}/\text{cm}^3$ of donors (case 1 in Figure Q3.1). What length of drift region is required to meet the 250 V blocking capability? Assume that the voltage across the depletion layer which grows in the p diffusion is negligible, so that all of the voltage is blocked across the n- drift region. [Hint: the space charge density is given by the doping density times the charge on the electron]
[3]
- In the second iteration, IRF decide to use a doping profile in the n- region which is non-constant. The doping density is effectively 0 at the p to n-interface and increases linearly as a function of distance towards the drain (case 2 in Figure Q3.1). Calculate the required drift-region length l to meet the 250 V blocking capability, given that the doping density at the drain is fixed at $1.5 \times 10^{15}/\text{cm}^3$.
[3]
- Using your knowledge of the operation of a $p-i-n$ diode, explain why the second doping profile may be beneficial when designing MOSFETs.
[3]

- e) IRF then test the newly designed MOSFET when switching a diode-clamped inductive load with a turn-on snubber.
- Sketch the snubber circuit with waveforms of relevant voltages and currents showing snubber operation. Only consider the case when the rate of change of current is **not** limited by the MOSFET. [5]
 - Explain the operation of the turn-on snubber specifically describing how it can reduce power loss in the MOSFET. [3]

4. A power supply is being designed for the avionics bay of an aircraft to power a radar unit from a 100 V DC bus in the aircraft. The radar equipment requires a negative DC voltage rail at -20 V DC.
- The designer considers both a Ćuk converter topology and a buck-boost topology. What are the advantages and disadvantages of each topology in this application? [3]
 - The designer finally chooses a Ćuk converter, shown in Figure Q4.1. Derive its voltage transfer ratio, stating your assumptions.

[4]

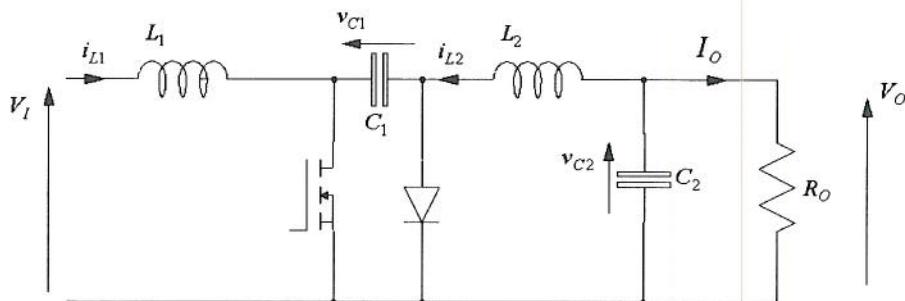


Figure Q4.1 Ćuk converter

- The radar equipment will draw between 40 W and 50 W from its -20 V rail. Calculate the minimum inductor sizes for the converter to stay in continuous conduction mode if the converter switching frequency is 100 kHz. Explain why in practice these inductors would be significantly larger than this minimum.

[5]

- A second supply is required for the aircraft, which must give an output of 10 V from a 400 V DC bus. The specification states the converter must be isolated and so the designer considers using both a double-switched flyback converter and an isolated full-bridge buck converter. Explain the fundamental difference in the way that the mutually coupled inductors are used in each case.

[4]

- The designer eventually picks a double-switched isolated flyback topology and chooses to operate it in discontinuous mode.

- Give a reason as to why discontinuous mode may have been chosen in this application.

[1]

- Choose a suitable duty cycle for discontinuous operation and calculate the required primary and secondary side inductances if the converter operates at a switching frequency of 200 kHz at a power output of 130 W.

[3]

Information for Candidates

There are 4 questions: Answer any 3.

Charge on the electron : 1.6×10^{-19} C
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Relative permittivity of Silicon: 11.7

1. This question concerns the design of a buck SMPS as shown in Figure Q1.1. Selected data sheet information of the components used is listed below. The supply must be able to output 5 A at 3 V from a 20 V input and is designed to operate in continuous conduction mode.

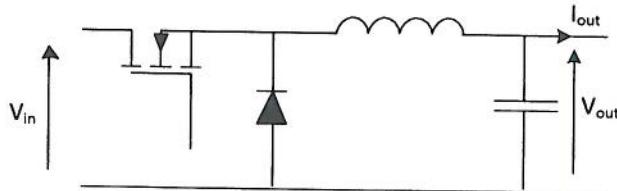


Figure Q1.1 Buck converter

MOSFET: $R_{DSon} = 30 \text{ m}\Omega$, $Q_{gs}=10 \text{ nC}$ (when $I_D=5 \text{ A}$), $Q_{gd}=17 \text{ nC}$ (when $V_{DS}=20 \text{ V}$)

Diode: $V_{on}=0.7 \text{ V}$ (constant when conducting)

Inductor: $100 \mu\text{H}$ with a $100 \text{ m}\Omega$ series resistance

Capacitor: $1000 \mu\text{F}$, negligible ESR

- a) Assuming the circuit operates with no losses, what is the required duty cycle?

[1]

[Easy start...]

$$V_{out}/V_{in} = \delta, \text{ giving } \delta = 0.15$$

- b) Recalculate the required duty cycle for the converter taking into account the diode voltage drop. Use this value of δ where required in the rest of this question.

[3]

[Simple application of known theory...]

The students should use a modified version of the well known equation for a buck converter to account for the diode losses. This equation can be easily derived

$$\frac{(V_{in} - V_{out})}{L} \frac{\delta}{f} + \frac{(-V_{diode} - V_{out})}{L} \frac{(1-\delta)}{f} = 0$$

$$\delta = \frac{V_{out} + V_{diode}}{V_{in} + V_{diode}}$$

Thus $\delta = 0.179$ (3sf)

- c) The current ripple in the converter must be less than 150 mA. Calculate the minimum switching frequency.

[2]

{Application of known formula}

$$\Delta I_{on} = \left(\frac{V_m - V_{out}}{L} \right) \frac{\delta}{f}$$

$$\therefore f = \left(\frac{V_m - V_{out}}{L} \right) \frac{\delta}{\Delta I_{on}} = \left(\frac{20 - 3}{100 \times 10^{-6}} \right) \frac{0.179}{160 \times 10^{-3}} = 190.2 \text{ kHz}$$

d)

- i) Which capacitance in the MOSFET must be charged in order for the drain current to rise at turn-on, and which must be discharged for the drain source voltage to fall at turn-on?

At turn on, the current rises as the gate-source capacitance is charged. When the drain current is equal to the inductor current, the diode can fall out of conduction, allowing the drain voltage to fall, which requires discharging of the gate-drain capacitance.

- ii) Calculate the switching loss in the MOSFET given that the gate drive is capable of sinking and sourcing 1 A.

[3]

{calculation}

The switching time for the MOSFET is thus the time taken for the gate drive to supply a total charge of $10 + 17 = 27 \text{ nC}$. This is a switching time of 27 ns , giving a switching loss per commutation of:

$$E_{loss} = V_{DS} \times I_D \times T \times 0.5 = 20 \times 5 \times 27 \times 10^{-9} = 1.35 \times 10^{-6} \text{ W}$$

This gives a total switching power loss of $1.35 \times 10^{-6} \times 2 \times f = 0.51 \text{ W}$

- e) Calculate the total power loss in the converter. State any assumptions you make.

[3]

{Simple calculation but the students need to remember all the contributions...}

Assume the effect of the ripple current is negligible

$$\text{Conduction loss in MOSFET} = I_{on}^2 \times R_{DSon} \times \delta = 5^2 \times 0.03 \times 0.179 = 0.134 \text{ W}$$

$$\text{Switching loss in MOSFET} = 0.51 \text{ W}$$

$$\text{Conduction loss in diode} = V_{diode} \times I \times (1 - \delta) = 0.7 \times 5 \times 0.821 = 2.87 \text{ W}$$

$$\text{Conduction loss in inductor} = I_L^2 \times R_L = 5^2 \times 0.1 = 2.5 \text{ W}$$

$$\text{Total loss} = 6.02 \text{ W}$$

- f) It is decided to replace the diode with another MOSFET, making a synchronous buck converter. Explain why this can be beneficial and explain any additional complexities which result from this modification.

[5]

The diode drop in a non-synchronous converter often accounts for the majority of conduction loss when the output voltage is low, as is the case here. The on-state drop for a conducting MOSFET can be much less than a diode drop, and losses can be reduced.

There are three additional complexities that are encountered when turning a non-synchronous converter into asynchronous converter. These are:

- A second (low-side) gate drive is required
 - Dead times must be used in order that both devices are not on at the same time, thus preventing a shoot-through current
 - If the converter ever enters discontinuous mode, the low-side MOSFET must be turned off to prevent the energy in the output capacitor being transferred from output to the input.
- g) Calculate the losses in the synchronous converter and hence show that it is more efficient than the non-synchronous version. State any assumptions you make.

[2]

We must make an assumption of the duty cycle for the synchronous rectifier case. Either one can be accepted (0.15 or 0.179) as long as the student realises that both are actually an approximation in this case. The figures below assume 0.179. It is not expected that the actual duty cycle is calculated here (only 2 marks available!)

$$\text{Conduction loss in MOSFETS} = I_{on}^2 \times R_{DSon} = 5^2 \times 0.03 = 0.75 \text{ W}$$

$$\text{Switching loss in MOSFET} = 1.03 \text{ W (twice the previous value)}$$

$$\text{Conduction loss in diode} = 0 \text{ (diodes now removed)}$$

$$\text{Conduction loss in inductor} = I_L^2 \times R_L = 5^2 \times 0.1 = 2.5 \text{ W (unchanged)}$$

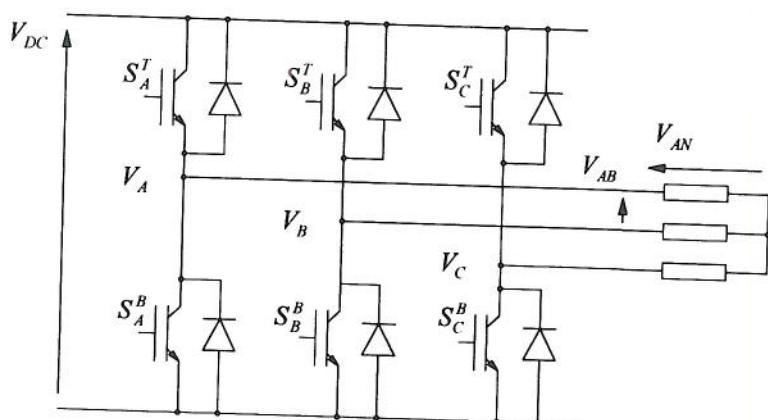
$$\text{Total loss} = 4.28 \text{ W}$$

Which is less than before.

2

- a) Sketch a circuit diagram of a 3-phase inverter. Explain how the switches in the circuit are controlled.

[5]

*/bookwork/**The circuit is a 3 phase inverter as shown:*

The DC to three-phase inverter consists of 6 semiconductor switches arranged in series pairs. The mid-point of each pair can be connected to the +ve or -ve rail of the DC supply. Anti-parallel diodes are necessary to provide a current path for inductive loads when the current direction is opposite to the normal conduction of the switch. The switches of each pair are turned on and off in anti-phase with a short dead-time in between. The duty cycle can be sinusoidally modulated by taking the switching instances from comparison of a high frequency triangle wave carrier and a sinusoidal modulating wave. The three-phases would share the same carrier wave but would use modulating waves phase displaced by 120 degrees.

- b) What is the maximum blocking voltage required by the switches in the circuit of part a)? What is the maximum phase and line voltage that can be created, assuming the phase voltages are sinusoidal?

[3]

/simple calculation/

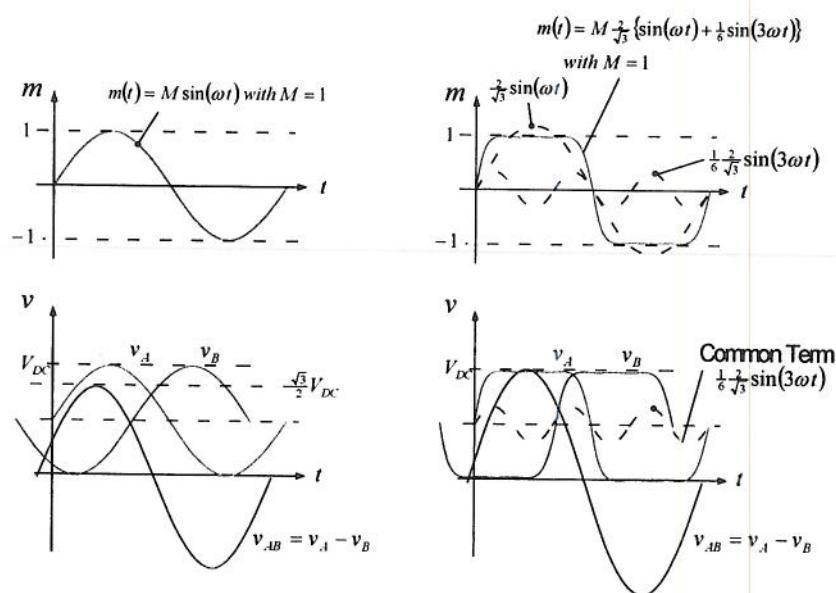
Each phase voltage is limited to an amplitude of $V_{DC}/2$ and the switches must be able to block the full DC voltage. In practice the switches would be rated to more than V_{DC} to allow for voltage overshoots due to inductance in the circuit when switching occurs. The maximum line voltage is just $\sqrt{3}/2 \cdot V_{DC}$.

- c) Explain how third harmonic injection can be used to increase the line voltage in an inverter. Illustrate your answer by sketching the modified phase voltages. What is the maximum voltage that the switches must block in this case?

[5]

A common mode term can be added into the phase voltages at a frequency of three times the fundamental (i.e. third harmonic). The common mode signal is added in a way that makes the phase voltages flat-topped (adding in the same way as a Fourier series of a square wave) sinewaves – i.e. the peak of the fundamental is in phase with the trough of the 3rd harmonic. As this reduces the amplitude of the phase voltage, the phase voltage can be scaled back up again, increasing the line-to-line voltage presented to the connected load.

This can be seen by sketching the waveforms.



The phase voltages are unchanged – as is the circuit topology – so the maximum voltage that the devices must block is unchanged.

- d) An induction motor can be controlled using slip-compensated speed control. A simplified diagram of this system is shown in Figure Q2.1. Explain the general principle of operation of the scheme and describe the function of the box marked “X”.

[4]

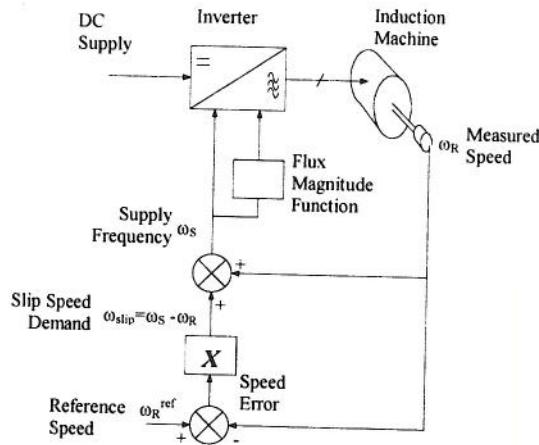


Figure Q2.1 Slip compensated speed control

[largely bookwork but room for additional info to be given]

An induction machine should be run in a region with a limited slip. Thus, the slip can be calculated from the difference between the reference speed and the measured speed. This slip can then be added to the measured speed to calculate the required electrical frequency to be applied to the motor. An inverter supplies a 3-phase set to the motor at the slip compensated speed. The flux magnitude function block ensures that the correct voltage magnitude is applied to the machine in order to keep the air gap flux at the correct value for the machine.

The box marked "X" contains a controller (to shape the slip demand signal) and a limit block to limit the maximum slip demand. This is necessary because If the slip is too large, the rotor currents become excessive and exceed the maximum rated current of the machine. This causes excessive heating and will saturate the machine.

- e) Figure Q2.2 shows a simplified equivalent circuit of an induction machine. Show that when operating the machine at the rated air gap flux, the magnitude of the stator voltage should be set in proportion to stator frequency at high speed and derive a modified expression for low speed operation.

[3]

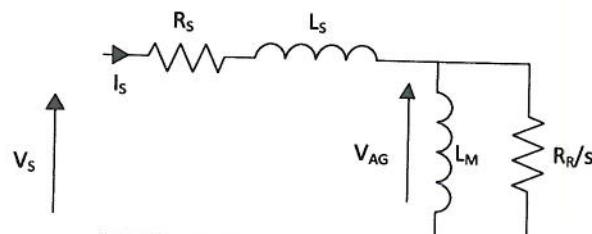


Figure Q2.2 Simplified equivalent circuit of an induction machine

The voltage across the stator is:

$$V_s = R_s I_s + j\omega_e L_s I_s + V_{AG}$$

$$V_{AG} = j\omega_e \psi_{AG}$$

So when operating the machine at the rated air gap flux, the stator voltage is proportional to the electrical frequency at high frequency. At low frequency the resistance term dominates and the stator voltage tends to $R_s * I_c$.

3. International Rectifier (IRF) are designing a new family of power MOSFETs rated to block 250 V. A cross-section through the device is shown in Figure Q3.1. Two doping profiles are being considered for the drift region.

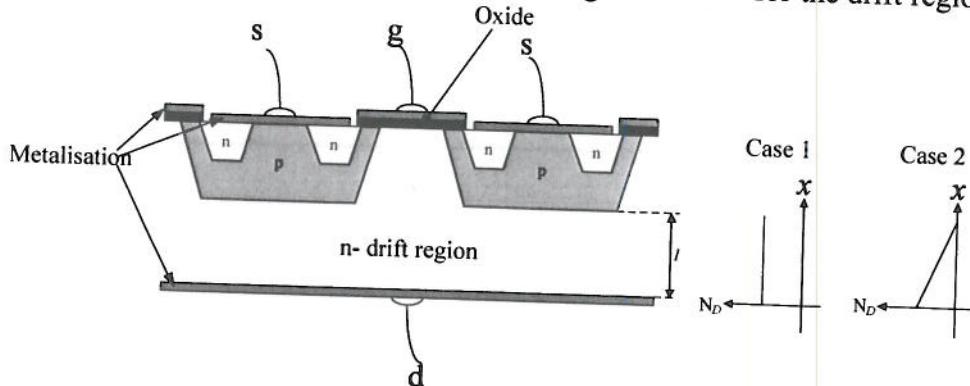


Figure Q3.1 Structure of new proposed IRF MOSFET family with two proposed drift region doping profiles

- a) Explain why the structure of Fig Q3.1 is used in power MOSFETs and why drain-source resistance eventually becomes too high for efficient device operation as the device is designed for increasing blocking voltage.

[3]

/bookwork/

A Power MOSFET is constructed vertically through the wafer, blocking voltage between the top and bottom side of the wafer and conducting current through the area of the wafer to make efficient use of the Silicon. In a lateral signal device, conduction occurs on the wafer surface and increasing the voltage blocking capability increases the area of silicon used. Therefore the DD MOSFET uses the electrical properties of the whole volume of the wafer rather than just the surface as is the case with signal devices.

The device is double diffused in order to make a set of PNP layers through the wafer. In a signal MOSFET only a single diffusion is required for the source and drain.

Multiple cells are used in order to maximise the available channel area. Higher cell density reduces the specific on resistance and adding cells in parallel reduces the absolute drain-source resistance for a given cell size.

Past a given voltage blocking limit, the resistance of the low doped n- region becomes too great (it gets longer for higher blocking capability), at which point the IGBT is the preferred device.

- b) In the first design iteration, IRF decide to use a constant doping density of the n- drift region of $1 \times 10^{15}/\text{cm}^3$ of donors (case 1 in Figure Q3.1). What length of drift region is required to meet the 250 V blocking capability?

Assume that the voltage across the depletion layer which grows in the p diffusion is negligible, so that all of the voltage is blocked across the n-drift region. [Hint: the space charge density is given by the doping density times the charge on the electron]

[3]

[Calculation]

The electric field in the n-region is given by:

$$\begin{aligned} E(X) &= \frac{1}{\epsilon_0 \epsilon_r} \int_0^X \rho dx \\ &= \frac{\rho}{\epsilon_0 \epsilon_r} X \end{aligned}$$

Thus, the voltage blocked over a length L is given by:

$$\begin{aligned} V &= \int_0^L \frac{\rho}{\epsilon_0 \epsilon_r} x dx \\ &= \frac{\rho l^2}{2 \epsilon_0 \epsilon_r} \end{aligned}$$

Doping density in SI units is $1e21/m^3$

Rearranging, and substituting the values gives:

$$L = \sqrt{2V\epsilon_0\epsilon_r/\rho} = \sqrt{2*250*8.85e-12*11.7/1.6e-19/1e21} = 18.0\mu m \text{ (3sf)}$$

- c) In the second iteration, IRF decide to use a doping profile in the n-region which is non-constant. The doping density is effectively 0 at the p to n-interface and increases linearly as a function of distance towards the drain (case 2 in Figure Q3.1). Calculate the required drift-region length l to meet the 250 V blocking capability, given that the doping density at the drain is fixed at $1.5 \times 10^{15}/cm^3$.

[3]

[Calculation]

The doping density at the drain is equal to $1.5 \times 10^{21}/m^3$

An equation for the doping is thus $N_D(x) = k - (k/l)x$ where $k = 1.5 \times 10^{21}$

Integrating from the drain end a distance X, we calculate that

$$\begin{aligned} E(X) &= \frac{1}{\epsilon_0 \epsilon_r} \int_0^X k - \frac{kx}{l} dx \\ &= \frac{1}{\epsilon_0 \epsilon_r} \left(kX - \frac{kX^2}{2l} \right) \end{aligned}$$

Giving a voltage blocking capability of:

$$V = \frac{1}{\epsilon_0 \epsilon_r} \int_0^l kx - \frac{kx^2}{2l} dx$$

$$\therefore V = \frac{kl^2}{3\epsilon_0 \epsilon_r}$$

Substituting the numbers, gives:

$$l = (3 * 250 * 8.85e-12 * 11.7 / 1.6e-19 / 1e22)^{1/2} = 18.0 \mu m$$

- d) Using your knowledge of the operation of a *p-i-n* diode, explain why the second doping profile may be beneficial when designing MOSFETs.

[3]

[interpretation of existing knowledge to new scenario]

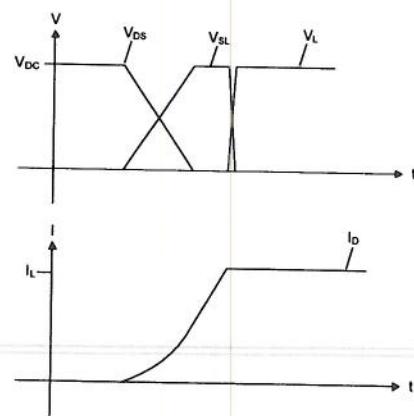
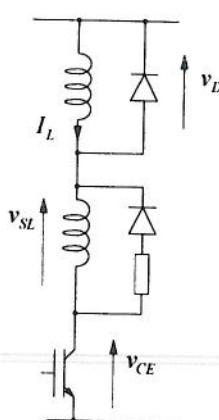
A pin diode has an almost intrinsic region between the *p* and *n* doping, which allows the electric field profile to achieve a flat top shape (rather than being triangular as is the case in a *pn* diode). The graded doping which is seen in this question uses the same concept – by making the doping close to the junction very low and increasing the *n*-doping as you move away from the centre of the junction. Hence, this concept of graded doping means that the peak field strength in the MOSFET is reduced so even though the drift region lengths are found to be identical, the peak field strength in the second design is lower. This means that such a doping profile can realise higher voltage MOSFETs (for a given length) than the first, which is beneficial for cost and in terms of minimising on-state resistance.

- e) IRF then test the newly designed MOSFET when switching a diode-clamped inductive load with a turn-on snubber.

- i) Sketch the snubber circuit with waveforms of relevant voltages and currents showing snubber operation. Only consider the case when the rate of change of current is *not* limited by the MOSFET.

[5]

[bookwork]



- ii) Explain the operation of the turn-on snubber specifically describing how it can reduce power loss in the MOSFET.

[3]

/bookwork/

When switching a diode-clamped inductive load without a snubber, at device turn off the current through the device must rise before the voltage across it can fall. This causes power dissipation. The snubber allows the current rise to be slowed down, allowing a smaller overlap between drain current and drain-source voltage, reducing power loss.

Waveforms are shown below.

At the instant of turn on the device voltage starts to fall. Assuming this happens linearly the voltage across the snubber inductor rises linearly (as the voltage across the main inductor is clamped by the diode). This causes a square law increase in device current. When the device drain voltage has fallen to zero, the voltage across the snubber inductor is fixed and so rises linearly until the diode drops out of conduction, allowing a constant current through the snubber inductor with no voltage across it.

A discharge path of a resistor and additional diode must be provided to discharge the snubber during the off time, ready for the next turn-on event.

4. A power supply is being designed for the avionics bay of an aircraft to power a radar unit from a 100 V DC bus in the aircraft. The radar equipment requires a negative DC voltage rail at -20 V DC.
- a) The designer considers both a Ćuk converter topology and a buck-boost topology. What are the advantages and disadvantages of each topology in this application?

[3]

/Application of knowledge to an application area/

Both converters have the same voltage transfer ratio, both of which are able to provide a step down 100 to 20v (with delta=0.17)

The input and output currents in the Ćuk converter are smoothed by an inductor. On the input side, this means the current drawn from the aircraft DC bus is smooth and thus radiates little energy. As the output current is smooth, the voltage ripple due to the ESR of the capacitor is small, also improving EMC compatibility. In the buck-boost converter, both the input and output currents are chopped, which is bad in terms of EMC.

However, the Ćuk converter may have lower efficiency for a given volume as it contains more components in the main current path. Its complexity may also mean reliability is worse. The Ćuk converter will also be heavier than the buck-boost which may be important in an aeronautical application.

- b) The designer finally chooses a Ćuk converter, shown in Figure Q4.1. Derive its voltage transfer ratio, stating your assumptions.

[4]

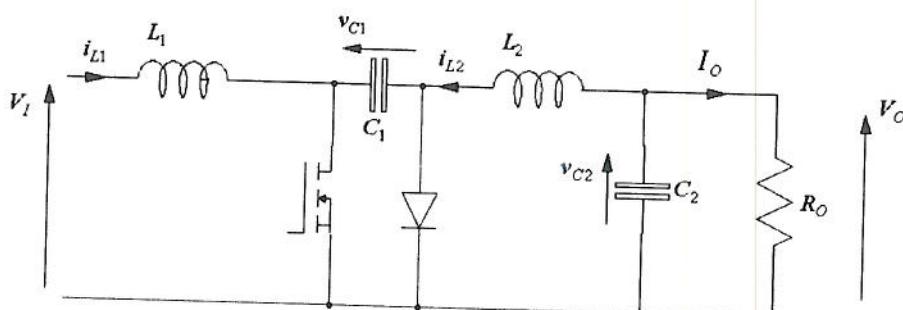


Figure Q4.1 Ćuk converter

/bookwork/

Assuming continuous conduction mode, and that the voltage ripple across the capacitors is negligible, we can do a volt-second balance across both inductors, to give:

For L1:

$$\begin{aligned} 0 &= \Delta i_{L_1}^{On} + \Delta i_{L_1}^{Off} \\ 0 &= \frac{V_1}{L_1} \cdot \delta T + \frac{V_I - V_{C1}}{L_1} (1-\delta)T \\ \frac{V_{C1}}{V_I} &= \frac{1}{1-\delta} \end{aligned}$$

For L2:

$$\begin{aligned} 0 &= \Delta i_{L_2}^{On} + \Delta i_{L_2}^{Off} \\ 0 &= \frac{V_{C1} + V_O}{L_2} \cdot \delta T + \frac{V_O}{L_2} (1-\delta)T \\ \frac{V_O}{V_{C1}} &= -\delta \end{aligned}$$

So we can write:

$$\begin{aligned} \frac{V_O}{V_I} &= \frac{V_O}{V_{C1}} \cdot \frac{V_{C1}}{V_I} \\ &= -\frac{\delta}{1-\delta} \end{aligned}$$

- c) The radar equipment will draw between 40 W and 50 W from its -20 V rail. Calculate the minimum inductor sizes for the converter to stay in continuous conduction mode if the converter switching frequency is 100 kHz. Explain why in practice these inductors would be significantly larger than this minimum.

[5]

[Calculations and interpretation]

The worst case scenario for ripple current is when the average currents are smallest and this is when the power through the converter is at the minimum, i.e. 40 W in this case. At the input side this gives an input current of $40W/100 = 0.4A$. On the output

side the current is $40W/20V=2A$. Thus, the maximum ripple current on this input is $0.8A$ and on the output is $4A$.

For a step down from $100V$ to $20V$, the duty cycle must be 0.17 .

As the ripple current on the input side is given by:
 $V_{in} L_1 * df$

$$I_{ripple} = \frac{V_{in}}{L_1} \frac{\delta}{f}$$

This gives:

Minimum value of $L_1 = 212.5\mu H$

For L_2 we have:

$$I_{ripple} = \frac{V_o}{L_2} \frac{(\delta)}{f}$$

Giving a minimum value of L_2 of $8.5\mu H$

In this application, the point of using a Cuk converter is the feature of smooth input and output currents. Letting the converter approach discontinuous conduction defeats this object, and so in reality we expect the converter to operate with a ripple currents that are small fractions of the average output current.

- d) A second supply is required for the aircraft, which must give an output of $10V$ from a $400V$ DC bus. The specification states the converter must be isolated and so the designer considers using both a double-switched flyback converter and an isolated full-bridge buck converter. Explain the fundamental difference in the way that the mutually coupled inductors are used in each case.

[4]

[largely book work]

In an isolated flyback converter, the transformer core is used as an intermediate energy store, being charged from the input side when the primary side switches are on, and discharged into the output side via the secondary winding when the switch is off. In the buck arrangement, the core is utilised purely to provide isolation and energy is not stored in the core (other than that arising from core magnetisation).

- e) The designer eventually picks a double-switched isolated flyback topology and chooses to operate it in discontinuous mode.
- i) Give a reason as to why discontinuous mode may have been chosen in this application.

[1]

[Interpretation]

A reason for choosing discontinuous mode is to reduce the core size to the minimum required for a particular power flow through the converter as weight is an issue in aerospace applications.

- ii) Choose a suitable duty cycle for discontinuous operation and calculate the required primary and secondary side inductances if the converter operates at a switching frequency of 200 kHz at a power output of 130 W.

[3]

[Calculation]

A reason for choosing discontinuous mode is to reduce the core size to the minimum required for a particular power flow through the converter as weight is an issue in aerospace applications.

When designing in discontinuous mode, it is advisable to use a duty cycle of around 0.4, an output side conduction time of 0.4, which leaves 20% of the cycle with no current in the mutual inductors.

In discontinuous mode, we need to ensure that current at the end of the on-time is sufficient to store enough energy in the core to maintain the required power flow through the converter:

$$\hat{I}_{L1} = \frac{di_{L1}}{dt} t_{on} = \frac{V_I}{L_1} \frac{\delta}{f}$$

$$\begin{aligned}\hat{E} &= \frac{1}{2} L_1 \hat{I}_{L1}^2 \\ &= \frac{1}{2} \frac{1}{L_1} \left(\frac{V_I \delta}{f} \right)^2 \\ L_1 &= \frac{(V_I \delta)^2}{P f}\end{aligned}$$

For the values chosen, this gives: $0.5 * (400 * 0.4)^2 / 130 / 200000 = 492 \mu H$

And we need to make sure that on the output side, the current falls to zero within the required conduction time (again, 0.4 of a cycle)

$$\hat{I}_{L2} = \frac{di_{L2}}{dt} t_{diode} = \frac{V_O}{L_2} \frac{\delta_{diode}}{f}$$

$$\begin{aligned}\hat{E} &= \frac{1}{2} L_2 \hat{I}_{L2}^2 \\ &= \frac{1}{2} \frac{1}{L_2} \left(\frac{V_O \delta_{diode}}{f} \right)^2 \\ L_2 &= \frac{(V_O \delta_{diode})^2}{P f}\end{aligned}$$

For the values chosen, this gives: $0.5 * (10 * 0.4)^2 / 130 / 200000 = 0.3 \mu H$