E4.20
AC3
ISE4.19

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2005

MSc and EEE/ISE PART IV: MEng and ACGI

INTRODUCTION TO DIGITAL INTEGRATED CIRCUIT DESIGN

Monday, 9 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung
Second Marker(s) : T.J.W. Clarke

Information for Invigilators:

Students may bring any written or printed aids into the examination.

Information for Candidates:

Students may need red, green, blue, yellow and black coloured pens.

1. a) *Figure 1.1* (see the colour supplementary sheet) shows the layout of an n-well CMOS circuit with four terminals: `Req_R`, `Req_L`, `Ack_R` and `Ack_L`. Extract and draw the transistor-level schematic diagram.

[12 marks]

c) Draw the vertical cross sections of the chip along the lines `AA'` and `BB'`. Label your diagram indicating the n-well region and the different types and levels of doping (e.g. p^-, n^+ etc).

[8 marks]

2. *Figure 2.1* (see the colour supplementary sheet) shows the layout of a 4 x 4 ROM array without the address decoder and output inverting buffer circuits.

a) Given that the value stored at address 0 is 0000_2 and that Out0 is the least significant bit, what are the values stored at the other three locations?

[6 marks]

b) Draw the circuit schematic for this layout.

[8 marks]

c) Draw the transistor-level schematic diagram of the rest of the circuit (i.e. address decoder and output buffer) to form a working 4 x 4 ROM. Explain briefly how your circuit works.

[6 marks]

3. a) *Figure 3.1* shows the circuit diagram of a flip-flop. Assuming that the signals CLK and D are as shown in *Figure 3.2*, draw a timing diagram showing the waveforms for CLK, D, X, Y and Q. Hence or otherwise, explain how this circuit works.

[10 marks]

b) State two shortcomings of this circuit.

[4 marks]

c) Modify the flip-flop circuit shown in *Figure 3.1* so that the Q output also implements embedded logic described by the following Boolean equation:

$$Q\_next = (A + B)(C + D) + (E + F)(G + H)$$

[6 marks]

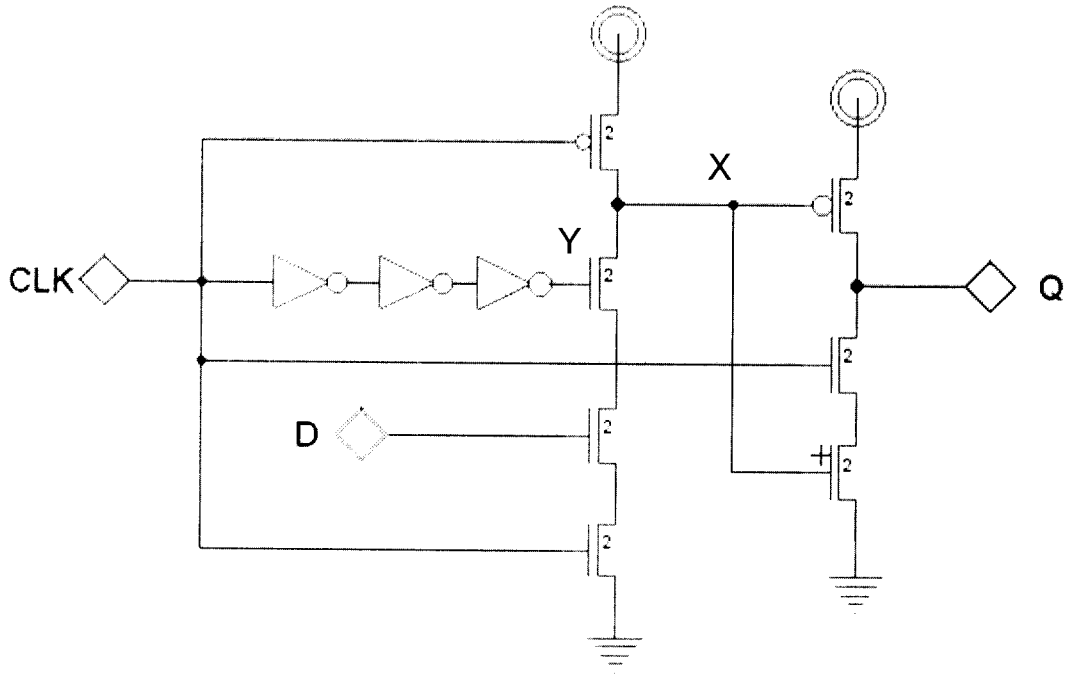


Figure 3.1

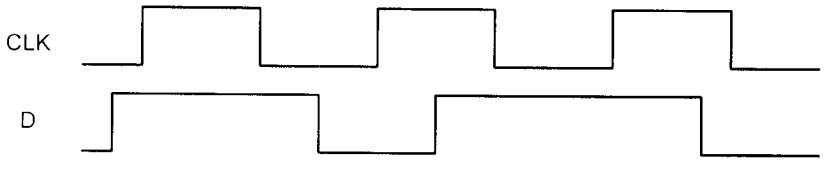


Figure 3.2

4. a) For the circuit in *Figure 4.1*, assume a unit delay through the register and logic blocks (i.e., $t_L = t_R = 1$). Assume that the registers, which are positive edge-triggered, have a set-up time t_S of 1. The delay through the multiplexer t_M equals 2 t_R.

(i) Assuming that the clock skew is zero, determine the minimum clock period of the circuit.

[4 marks]

(ii) What is the minimum clock period of θ if the clock skew is $\delta = t'_\theta - t_\theta = 4$?

[4 marks]

b) In a 0.25μm CMOS process, the widths of a minimum size inverter p and n transistors are 0.5μm and 0.25μm respectively. The unit delay is given to be 30ps. The circuit contains two separate clock paths P1 and P2 as shown in *Figure 4.2*. The total gate widths seen by the two paths are 900μm and 100μm respectively.

(i) Using the method of logical effort, or otherwise, estimate the clock skews between the paths if the inverters shown in *Figure 4.2* are minimum size.

[5 marks]

(ii) Determine the best number of stages of inverters (N_{p1} and N_{p2}) to use on the two paths in order to minimize the clock skew. For this number of stages, size the inverter buffer circuits for each clock path so that the clock signal delay on each path is minimized.

[7 marks]

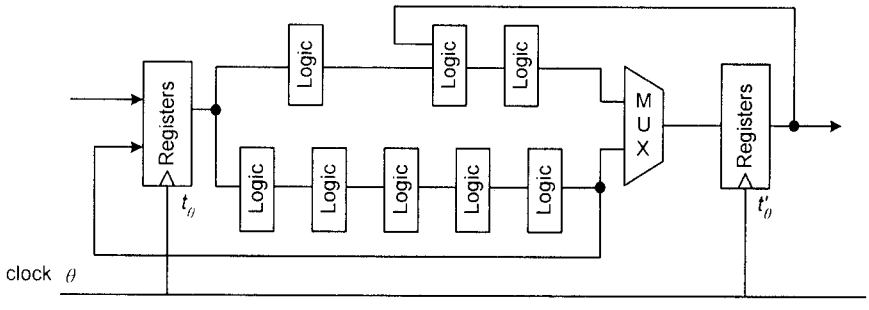


Figure 4.1

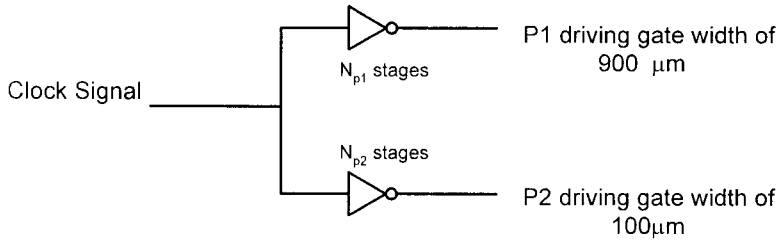


Figure 4.2

5 *Figure 5.1* shows a 1-bit comparator circuit that compares a_j with b_j. c_j and d_j are inputs and c_{j+1} and d_{j+1} are outputs.

a) Derive the truth table that describes the function of this circuit.

[5 marks]

b) Design the layout of this comparator cell using a stick diagram or other form of symbolic layout.

[7 marks]

c) Four such cells can be cascaded to form a 4-bit binary comparator as shown in *Figure 5.2*. To what values should input signals C0 and D0 be set in order for the comparator to operate correctly? How should the outputs C4 and D4 be interpreted. Note that A0 corresponds to the most significant bit and A3, the least significant bit, of the number A.

[4 marks]

d) By considering the following three cases and the values for c_j and d_j at all four stages of the circuit, explain the operation of this 4-bit comparator.

(i) $A = 1011_2$ $B = 0011_2$
(ii) $A = 0111_2$ $B = 1011_2$
(iii) $A = 1001_2$ $B = 1001_2$

[4 marks]

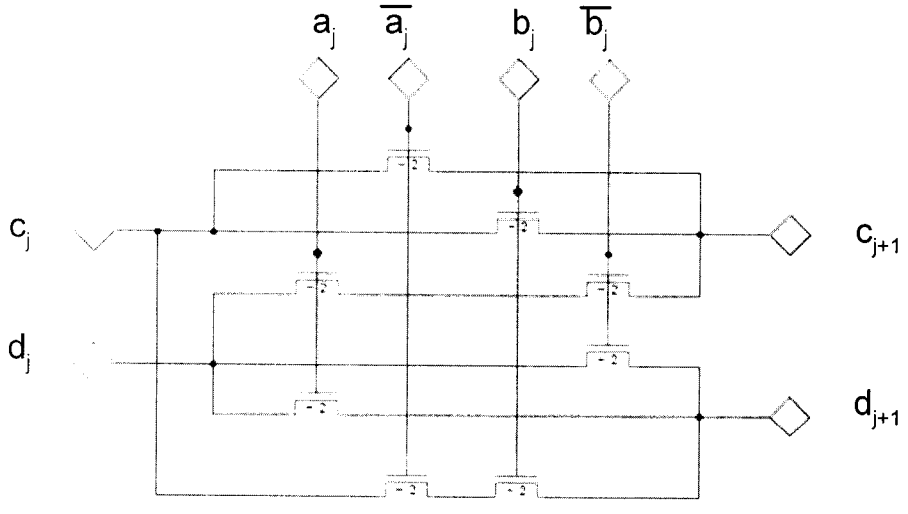


Figure 5.1

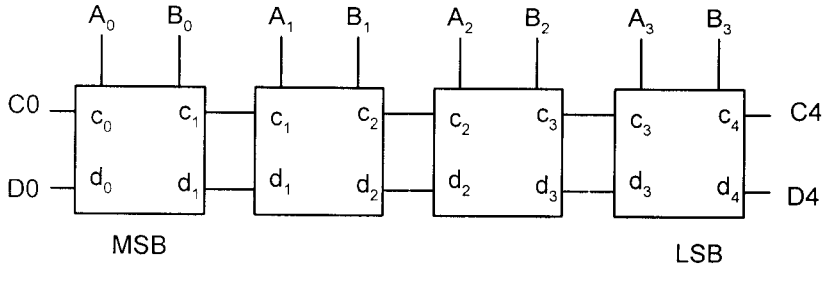


Figure 5.2

6. a) Deduce the Boolean equation for the circuit shown in *Figure 6.1*.

[2 marks]

b) Determine the optimal sizes of all transistors in this circuit assuming that 0.25μm technology is used and the mobility of n-transistors is twice that of p-transistors. Justify your answer.

[4 marks]

c) By applying either the path sensitisation or the Boolean differences method, find all the test vectors that will detect stuck-at faults at the node B.

[7 marks]

d) By adding a suitable flip-flop circuit and by implementing suitable drivers for A, B C and D inputs to the circuit shown in *Figure 6.1*, design a transistor-level circuit of a single-bit scan-path register.

[7 marks]

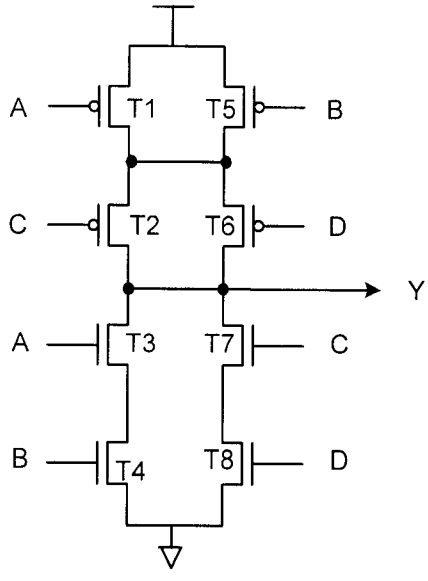


Figure 6.1

Colour Supplementary Sheet

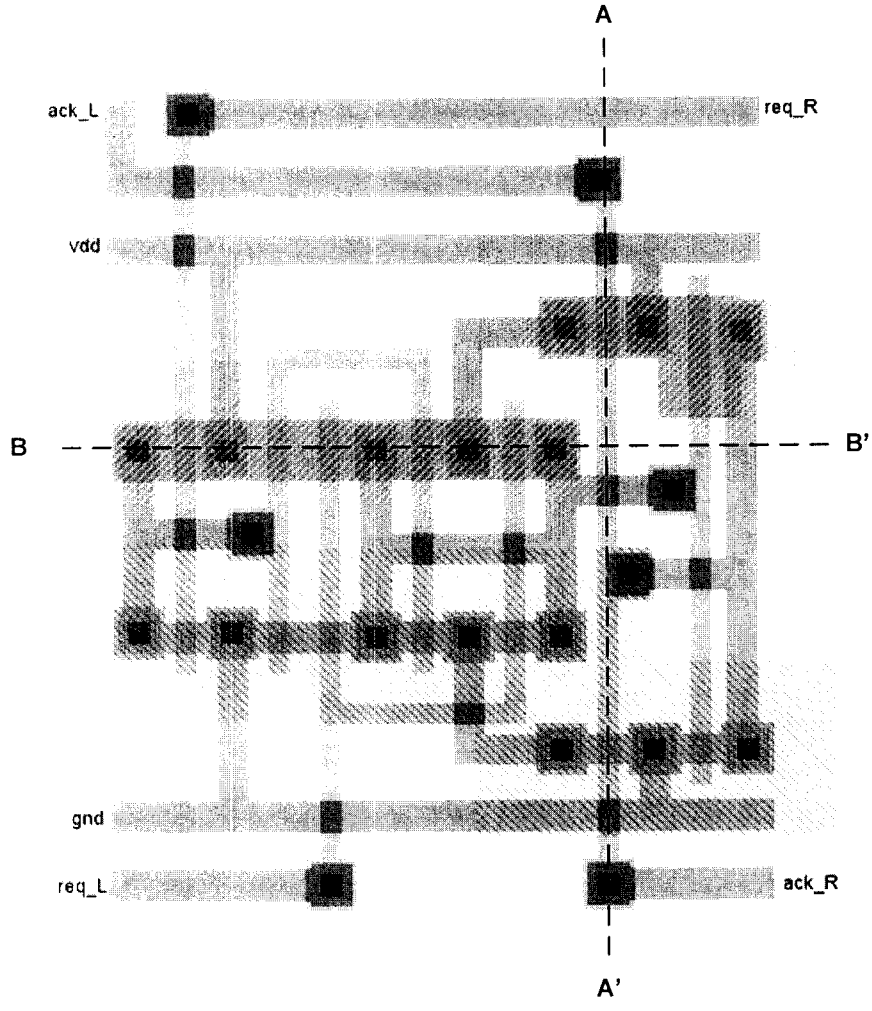


Figure 1.1 Layout of a full-custom cell for Question 1

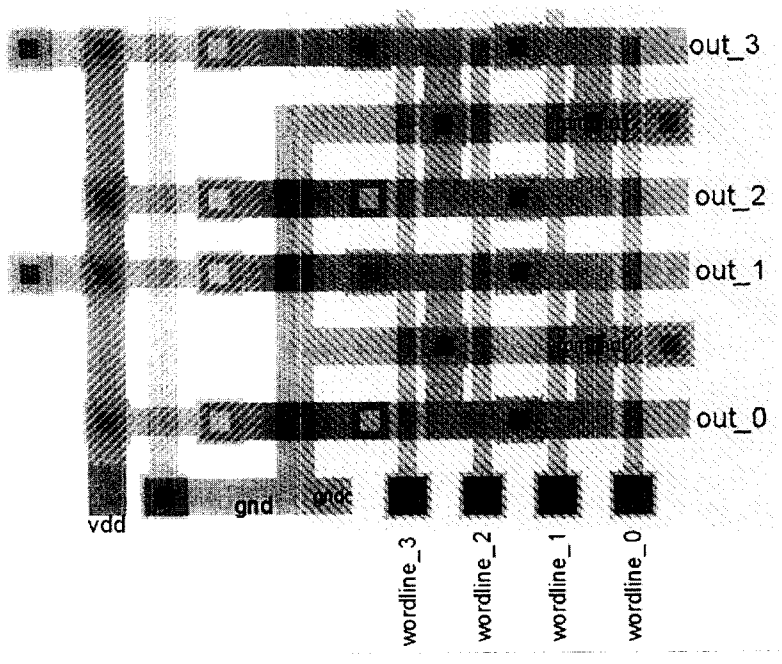


Figure 2.1 Layout of a 4 x 4 ROM array for Question 2

IMPERIAL COLLEGE OF SCIENCE TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
M.Eng. and A.C.G.I. EXAMINATIONS 2004

PART IV

INTRODUCTION TO DIGITAL IC DESIGN

SOLUTIONS

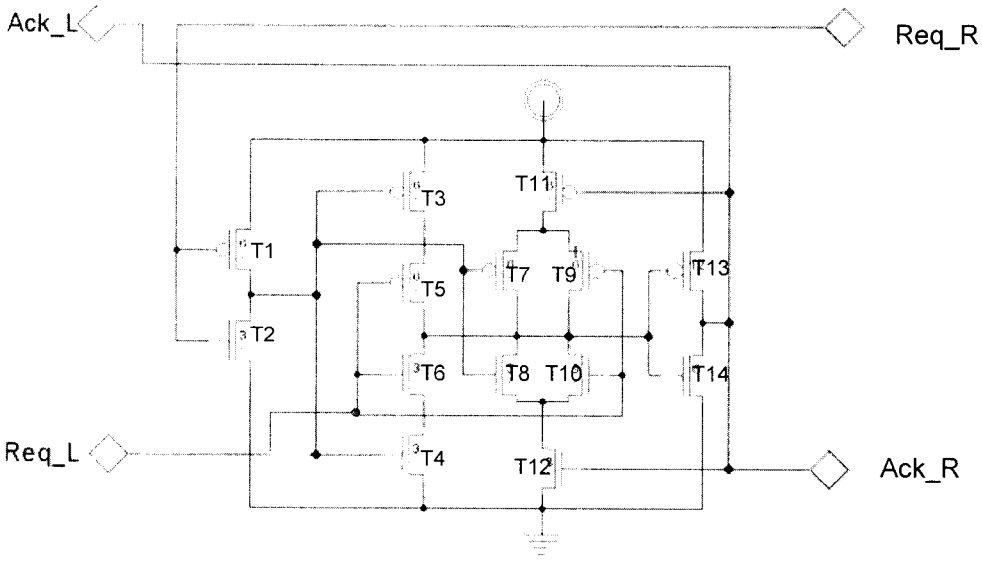
This is an open-book examination.

You may need red, green, blue, yellow and black coloured pens.

First Marker: *Peter Cheung*
Second Marker: *Thomas Clarke*

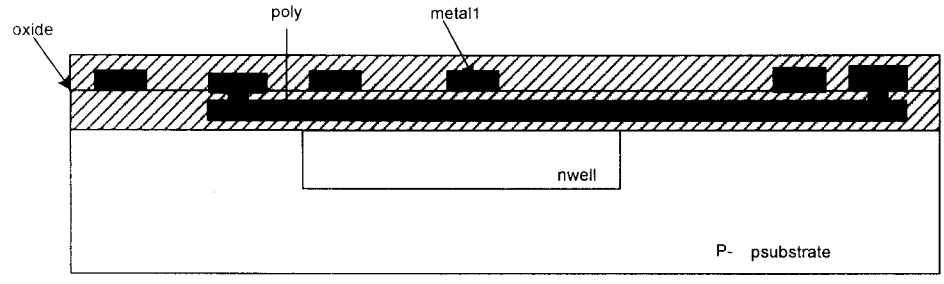
Solution to Question 1

a) This question tests student's ability to understand a full custom layout. This is a special cell for asynchronous systems, known as the Muller-C element with an extra inverter. Students do not need to know the circuit in order to answer this question.



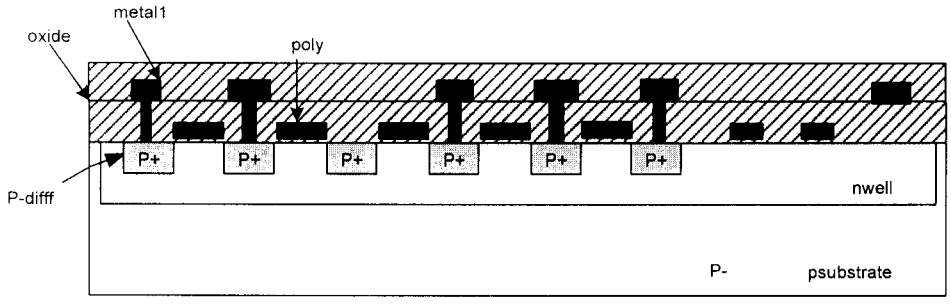
[12 marks]

b) This part of the question tests student's ability to relate the layout to the physical process and different layers on the chip.



A - A'

[4]



B - B'

[4]

[8 marks]

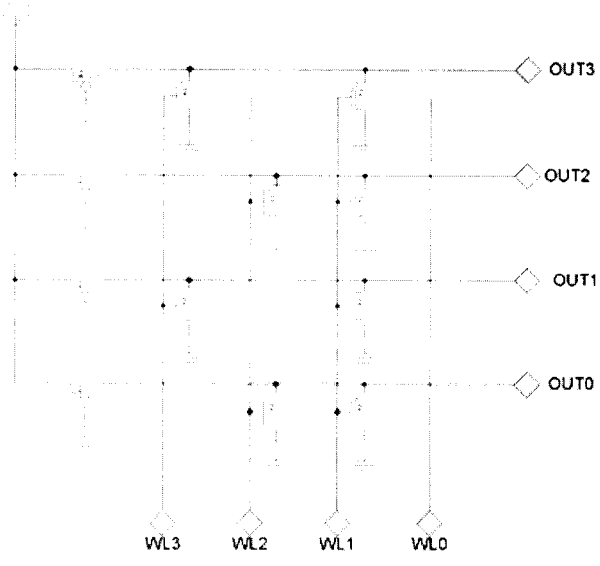
Solution to Question 2

a)

Address	ROM Content
0	0000
1	1111
2	1010
3	0101

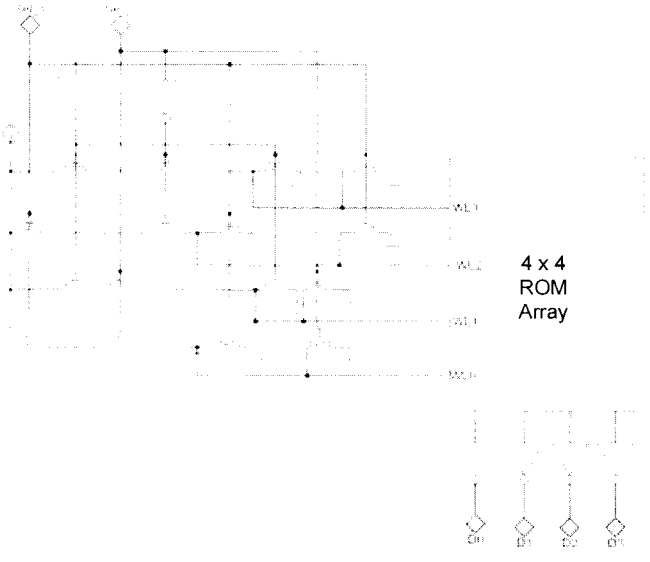
[6 marks]

b)



[8 marks]

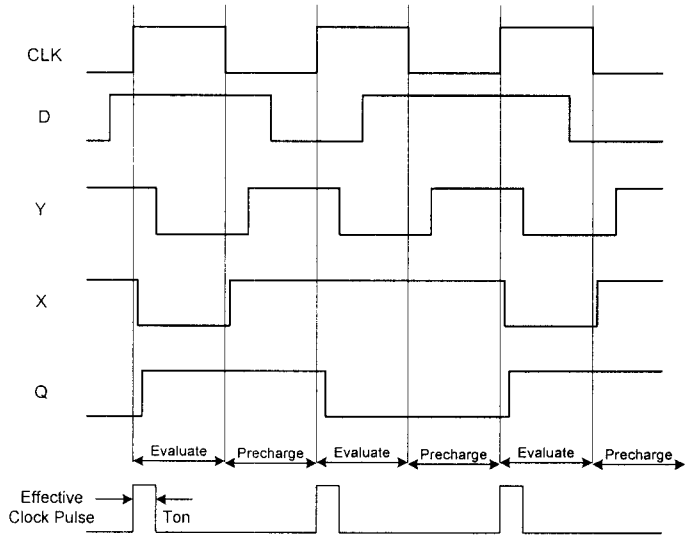
c)



[6 marks]

Solution to Question 3

(a) When clock CLK is low, the flip-flop is in the precharge phase. Node X is precharged to the level of the power supply, and node Q holds its previous value. On the rising edge of the clock, the flip-flop enters the *evaluation phase*. Here two periods are distinguished. In the first period when CLK is high, but Y is also high, it corresponds to an active clock pulse to the circuit and the circuit is in the *sampling* (or transparent) mode. The value of output Q is determined by the value of input D. Once the internal node X is discharged, due to its precharge nature, it will stay low until the next clock cycle. In the second period, the pulse is inactive. The sampling of D is disabled, so X and Q will retain the values they acquired during the sampling period. Notice that any subsequent change at D after the sampling period will have no effect on Q.



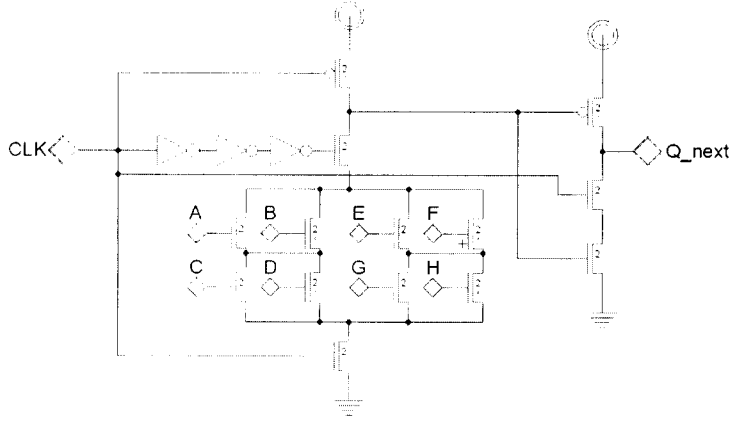
[10 marks]

(b) The shortcoming of this circuit are (any two of the three here will do):

1. Internal node X is a dynamic node and therefore this circuit will not work at low frequency.
2. Output Q is in high impedance when the clock signal CLK is low.
3. The timing of the sampling window Ton is critical: too short a Ton could lead to metastablility or functional failure because the sampling window is too short to correctly evaluate the input. Too long a Ton may cause poor performance by imposing a long hold time.

[4 marks]

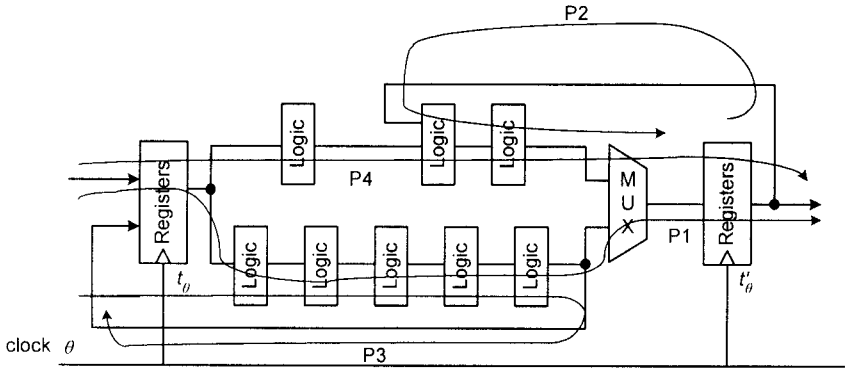
(c)



[6 marks]

Solution to Question 4

a)



(i) Out of the 4 paths shown in the figure, p1 is the critical one and determines the lower bound on the clock period. Using $T \geq t_{reg} + t_{logic} + t_{setup} - \delta$, we get ***Tmin* = 1+7+1 = 9.**

[4 marks]

(ii) As the clock skew increases, the most significant path changes. Repeating the calculations in part (i) we get : Tmin(p1) = 9 - 4 = 5, Tmin(p2) = 6, Tmin(p3) = 7, Tmin(p4) = 7 - 4 = 3. (Note that the clock skew is 0 for paths p2 and p3). Therefore the minimum clock period is Tmin = 7.

[4 marks]

b) (i) Gate width of minimum size inverter is 0.75 μm. t_d = 30ns. Therefore, the Electrical Effort (and total effort F) for the two paths are:

F_{P1} = 900 /0.75 = 1200; F_{P2} = 100 / 0.75 = 133;

Delay estimates of the two paths are: D_{P1} = 1200 * t_d = 36 ns; D_{P2} = 133 * t_d = 4 ns
P1-P2 skew = 1067 * t_d = 32 ns.

[5 marks]

(ii)

Total effort F for P1 = 1200, P2 = 133. Best number of stages (from notes) is given by:
Nbest = log (F)/ log (3.59). $N_{P1} \approx 5.5$, $N_{P2} \approx 3.8$. P1 should be buffered by 6 inverter stages, P2 also by 4 stages. Therefore

For P1, each stage should increase in size by $\sqrt[6]{1200} = 3.26$,
for P2, each stage should increase in size by $\sqrt[4]{133} = 3.4$.

Solution – increase sizes of p-trans and n-trans by these factors for each of the stages:

Stage	1	2	3	4	5	6
P1:	x 1	x 3	x 10	x 35	x 113	x 368
P2:	x 1	x 3	x 12	x 39		

P1 delay ≈ (3/1 + 10/3 + 35/10 + 113/35 + 368/113 + 1200/368) * t_d = 22.5 t_d
P2 delay ≈ (3/1 + 12/3 + 39/12 + 133/39) * t_d = 13.7 t_d
Clock skew ≈ 8.8* t_d

[7 marks]

Solution to Question 5

a)

a_j	b_j	c_{j+1}	d_{j+1}
0	0	c_j	d_j
0	1	c_j	c_j
1	0	d_j	d_j
1	1	c_j	d_j

[5 marks]

b) Design of the layout depends on student. Marks will be deducted if the layout is inefficient or contains excessive unnecessary crossovers.

[7 marks]

c)

$c_j = (\mathbf{a_j > b_j})$, and $d_j = (\mathbf{a_j = b_j})$

C0 = '0', D0 = '1' indicating that we assume A=B to start.
C4 = (A>B), D4 = (A=B).

[4 marks]

d) (i)

j	0	1	2	3	4
A	1	0	1	1	-
B	0	0	1	1	
C	0	1	1	1	1
D	1	0	0	0	0

(ii)

j	0	1	2	3	4
A	0	1	1	1	-
B	1	0	1	1	
C	0	0	0	0	0
D	1	0	0	0	0

(iii)

j	0	1	2	3	4
A	1	0	0	1	-
B	1	0	0	1	
C	0	0	0	0	0
D	1	1	1	1	1

[4 marks]

Solution to Question 6

a)

Y = NOT (A*B + C*D)

[4 marks]

b) $\lambda = 0.25\mu$ Then all lengths are 1 λ. In order to ensure worst case rise and fall time to be roughly the same, all n-trans use 4 λ width, and all p-trans 8 λ width.

[4 marks]

c) Use Boolean difference method:

Y (B=0) = Y (A,0,C,D) = NOT (C*D)
Y (B=1) = Y (A,1,C,D) = NOT (A + C*D)

Therefore Boolean difference is:

dY/dB = Y(B=0) XOR Y(B=1)
= NOT (C*D) XOR NOT(A + C*D)
= A* NOT(C) + A*NOT(D)

To test for stuck-at-0 fault at B,
test input = B*(dY/dB),
= A*B*NOT(C) + A*B*NOT(D) = 1

Therefore the test vector for B stuck-at-0 = 110x and 11x0, i.e. (1100, 1101, 1110)

To test for stuck-at-1 fault at B,
test input = NOT(B)*(dY/dB),
= A*NOT(B)*NOT(C) + A* NOT(B)*NOT(D) = 1

Therefore the test vector for B stuck-at-1 = 100x and 10x0, i.e. (1000, 1001, 1010)

[5 marks]

d) If B = NOT(C), then we can use the cell as a MUX between A and D inputs.

[7 marks]