EE4-16
EE9-AC6

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2017

MSc and EEE PART IV: MEng and ACGI

ANALOGUE SIGNAL PROCESSING

Corrected copy

Thursday, 18 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P. Georgiou
Second Marker(s) : K. Fobelets

Special instructions for students

Unless otherwise stated the following parameters have the following definitions:

V_{DS}*: Drain Source Voltage.*

V_{GS}*: Gate Source Voltage.*

V_{TH}*: Threshold Voltage.*

U_t*: Thermal Voltage.*

n *: Weak Inversion Slope factor.*

g_m*: Transconductance.*

1.

a. Compare Voltage and Current mode domains with regards to dynamic range, processing, signal distribution and speed.

[4]

b. The equation for the drain current of a new type of cubic transistor is given below, whereby K and I_0 are constants and all other terms have their usual meaning.

$$I_D = KI_O(V_{GS} - V_{th})^3$$

i) Derive the transconducance of the device and sketch its relationship with the transistors gate voltage.

[4]

ii) Derive the transconductance efficiency of the device, stating your answer only in terms of I_D, I_0 and K.

[2]

iii) The cubic transistor is used in a switched current memory cell shown in Figure 1.1. Give and explain one reason why such a transistor would have worse performance when compared with a standard MOSFET operating with a square law characteristic.

[2]

c. For the cascade of amplifiers shown in Figure 1.2, derive the output referred noise, explaining the meaning of all terms and identifying what factors can be optimized to improve the signal to noise ratio.

[8]

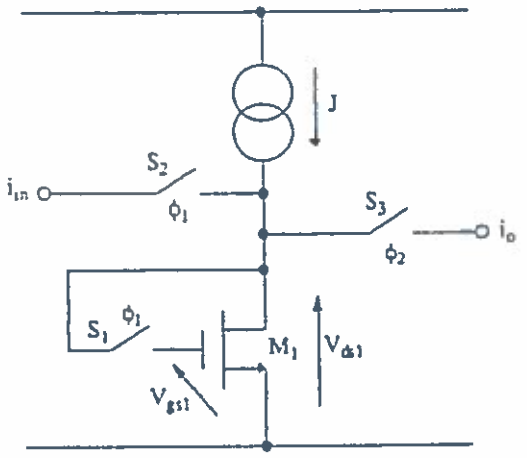

Figure 1.1: Switched current memory cell

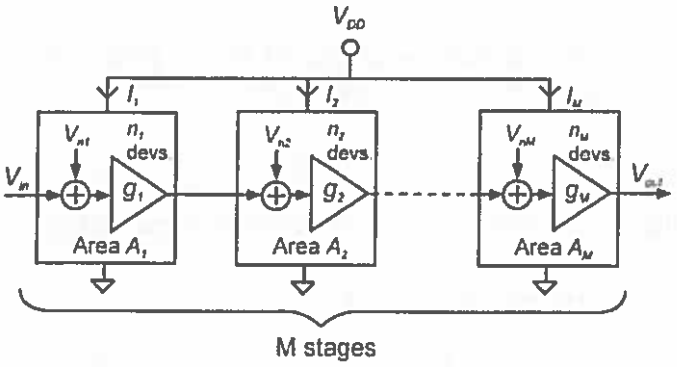

Figure 1.2: Cascade of amplifiers

2.

a. State and derive the translinear principle (TLP) for a loop of MOS transistors working in weak inversion. Give all assumptions you make.

[5]

b. Show how short channel effects in MOS transistors operating in weak inversion, lead to multiplicative errors in output currents of translinear circuits.

[4]

c. Figure 2.1 shows a translinear circuit.

i. Derive the transfer function I_{out} of this circuit using the translinear principle. You may assume that currents I_1 and I_3 are input currents and I_2 and I_4 are a static bias.

[5]

ii. Write down an expression for the output current I_{out} when $I_{in} = A \times \sin(\omega t)$ and I_1 and I_3 are given as:

$$I_3 = \left|\frac{dI_{in}}{dt}\right|, \qquad I_1 = \left|\int I_{in}\, dt\right|$$

[4]

iii. What is the function of this circuit when the inputs are applied as in 2.b.ii?

[2]

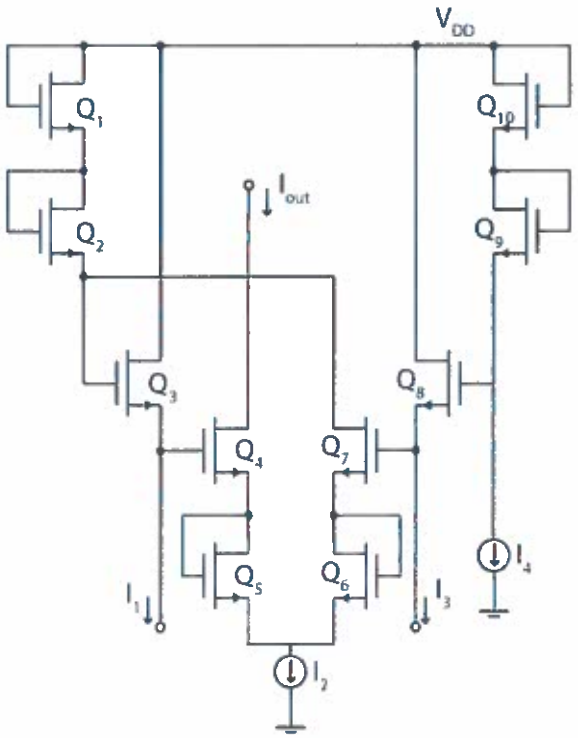

Figure 2.1: Translinear Circuit

3. The transfer function of a second order topology has been decomposed into the following state-space equations:

$$\dot{X_1} = -\left(\frac{\omega_0}{2Q}\right) X_1 - \omega_0 \left(1 - \frac{1}{4Q^2}\right) X_2 + \omega_0 U$$
$$\dot{X_2} = -\left(\frac{\omega_0}{2Q}\right) X_2 + \omega_0 X_1$$
$$Y_1 = X_1$$
$$Y_2 = X_2$$

whereby Y_1 and Y_2 are the outputs, X_1 and X_2 are the state-variables and U is the input.

a. Show that the output Y_1 can be used to implement a second order lowpass transfer function and the output Y_2 can be used to implement a "two-pole one-zero" second order transfer function.

[4]

b. By using the mappings below, show how these state space equations can be mapped to non-linear log-domain design equations. State any assumptions you make.

$$X_1 = I_1 \exp\left(\frac{V_1}{nU_t}\right) \qquad X_2 = I_2 \exp\left(\frac{V_2}{nU_t}\right) \qquad U = I_U \exp\left(\frac{V_U}{nU_t}\right)$$

[6]

c. With these log-domain design equations, sketch a schematic of the final log domain topology which realises the two outputs Y_1 and Y_2 using weak inversion MOS transistors.

[10]

4. Figure 4.1 shows a NMOS sampling switch that is used in the switched capacitor circuit. The width and length of transistor M1 are (W/L)=50/2. This switch causes an error in V_{out} when it closes.

   a. State 4 phenomena which could cause an error in V_{out} with equations descibing each case.

   [8]

   b. Show, with the aid of a graph, how the error induced by the most significant of these phenomena causes non-ideal gain and offset.

   [4]

   c. Design a method which cancels out two of these phenomena stating assumptions and showing calculations, where necessary, to prove it cancels these.

   [4]

   d. What is the advantage of bottom plate sampling of the capacitors in the circuit in Figure 4.2 and state how this should be connected so as not to degrade the circuit's speed and precision.

   [4]

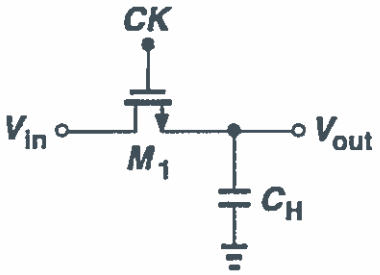

Figure 4.1:NMOS sampling switch and capacitor

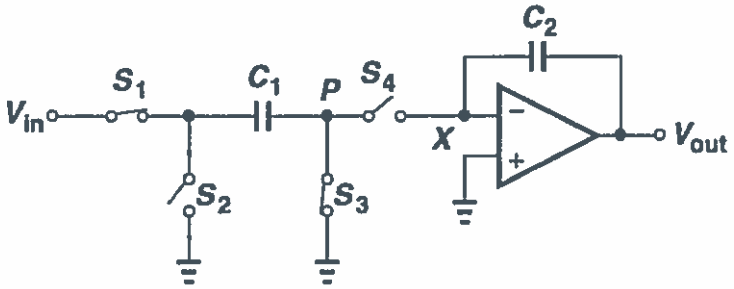

Figure 4.2: Switched Capacitor Integrator

5.

a. Figure 5.1 shows a conventional second-generation positive current conveyor, CCII+.

   i. Explain its operation principle and describe how impedances at each of its three ports, X, Y, Z, differ from a standard operational amplifier.

   [4]

   ii. Draw the circuit of a CMOS implementation of a bi-directional CCII+.

   [4]

   iii. Propose a method to increase its output impedance and use this to draw the new circuit.

   [2]

b. Figure 5.2 shows the circuit for a current normalizer. Derive the transfer function for the generalized current I_{out} where i indicates the selected output branch from the circuit.

   [4]

c. Figure 5.3 shows a circuit that is used as a variable OTA. Using your results from part b. or otherwise, derive an equation for the output current I_j as a function of the differential input voltage (E_j-V). You may assume all transistors are operating in weak inversion.

   [6]

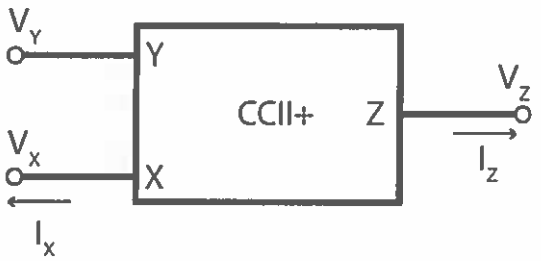

Figure 5.1: Conventional second-generation positive current conveyor.

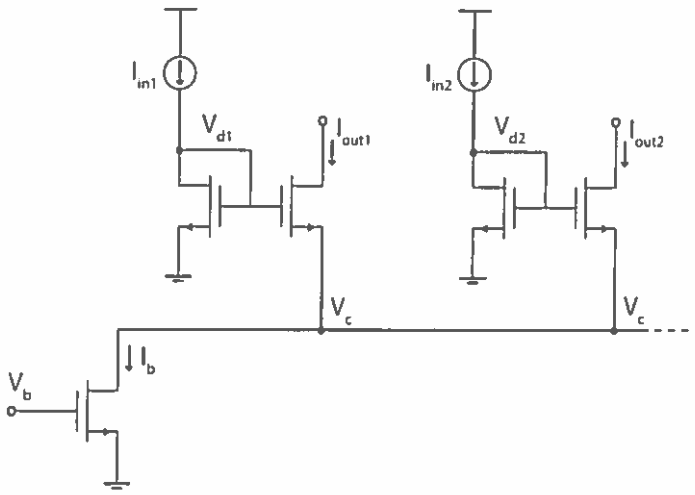

Figure 5.2: Current mode normalizer circuit

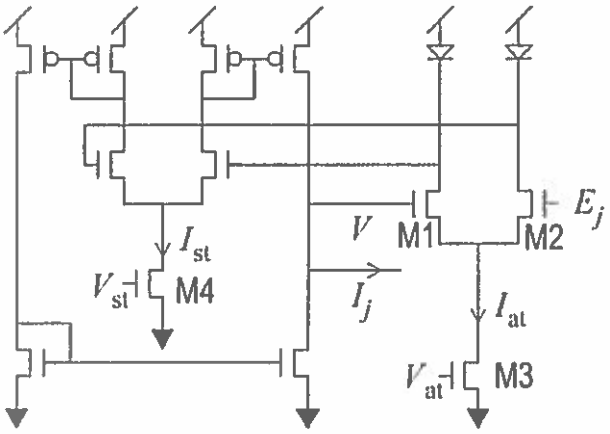

Figure 5.3: Variable OTA circuit

6. Figure 6.1 shows the block diagram of a cochlear prosthesis.

a. Explain the concept of dynamic range mapping used in this system and why it is beneficial.

[5]

b. Sketch the schematic of a suitable low-power Analogue Front End (AFE) which is suitable for audio frequencies and explain its operation.

[5]

c.

i) Sketch the schematic of a suitable logarithmic analogue to digital converter which also uses autozeroing to remove any offset in the amplifiers.

[5]

ii) Explain its operation showing timing diagrams and equations where necessary.

[5]

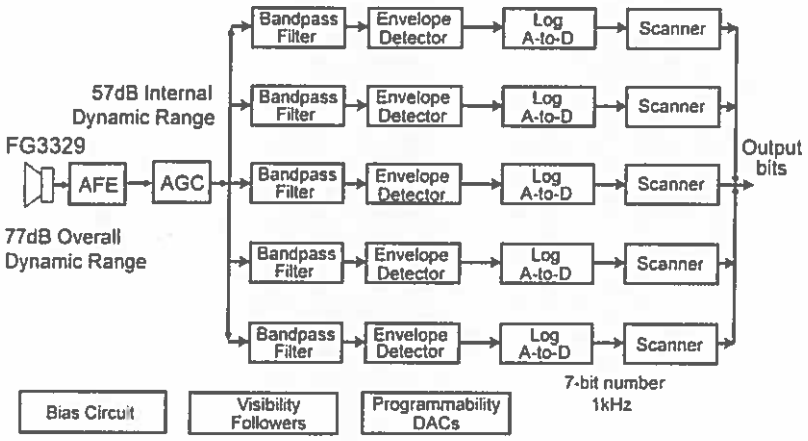

Figure 6.1: Block diagram of a cochlear prosthesis.