IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2004

EEE/ISE PART I: MEng, BEng and ACGI

DIGITAL ELECTRONICS 1

Friday, 4 June 10:00 am

Time allowed: 2:00 hours

There are FIVE questions on this paper.

Question 1 is compulsory.

Answer THREE questions, including Question 1.

All questions carry equal marks

Corrected Copy

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung
Second Marker(s) : P.A. Naylor

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X[7:0] is an eight bit bus with X7 being the MSB and X0 the LSB.

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

[Question 1 is compulsory]

1. a) Figure 1.1 shows the truth table of a three-input, two-output logic function. Using Karnaugh maps, derive the minimal sum-of product expression for F and G.

inputs			output	
A	B	C	F	G
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 1.1

[4]

b) The waveforms for signals P and Q shown in Figure 1.2 are applied to the circuit shown in Figure 1.3. Copy the timing diagram and add waveforms for R, S, T and U. Assume that initially T=0 and U=1.

[4]

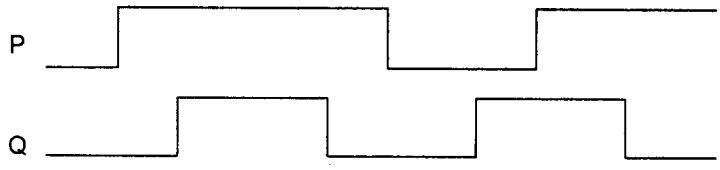


Figure 1.2

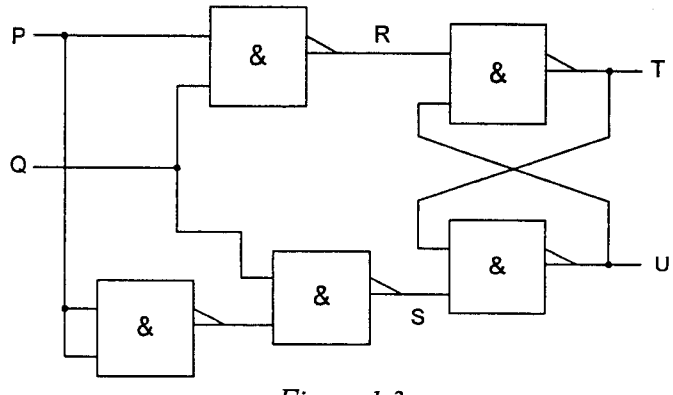


Figure 1.3

c) Assuming that all numbers are represented using 16 bits, complete the missing entries which are not shaded in the following table. (No marks will be awarded for this question unless you show how the solutions are derived.)

Decimal	Hexadecimal	Binary
2765	?	
?	5A2F	?
-1024	?	

[4]

d) For the circuit shown in Figure 1.4, draw a truth table showing the output Q for all combinations of inputs A, B and C.

[4]

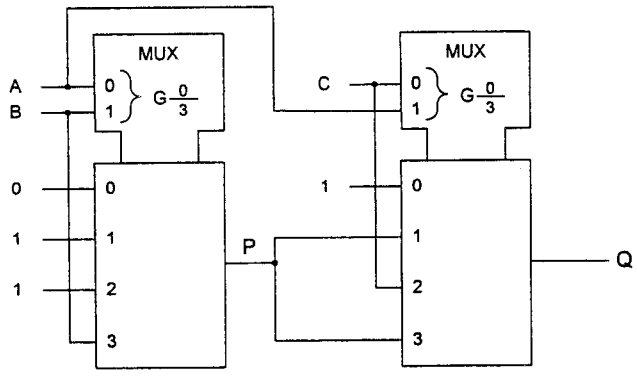


Figure 1.4

e) Prove the following Boolean equation.

$$f = (A + C)(\overline{A} + B) = AB + \overline{A}C$$

[4]

2. Figure 2.1 shows a shaft encoder system that measures the angle of rotation in a rotating machine. The encoder consists of a disc with the fixed pattern shown in Figure 2.1 rotating in the anti-clockwise direction. Three light sources are used to shine light through each of the three concentric rings on the encoder and are detected by the three photo detectors on the other side of the encoder disc. The inner most ring encodes the most significant bit (MSB) of the angle. In this way, one revolution is divided into 8 separate segments where segment 0 is from 0° to 45°, segment 1 is from 45° to 90°, and so on up to and including segment 7. Light cannot penetrate through the shaded region of the disc. Each photo detector produces a logic '1' if light is detected and a logic '0' otherwise.

a) Draw a table showing the segment number and the corresponding signals G0, G1 and G2.

[5]

b) Design the minimized Boolean equations for the decoder circuit that translates G0, G1 and G2 to the segment number A[2:0].

[10]

c) Find a solution that is equivalent to your answer to part (b) but uses only NOR functions.

[5]

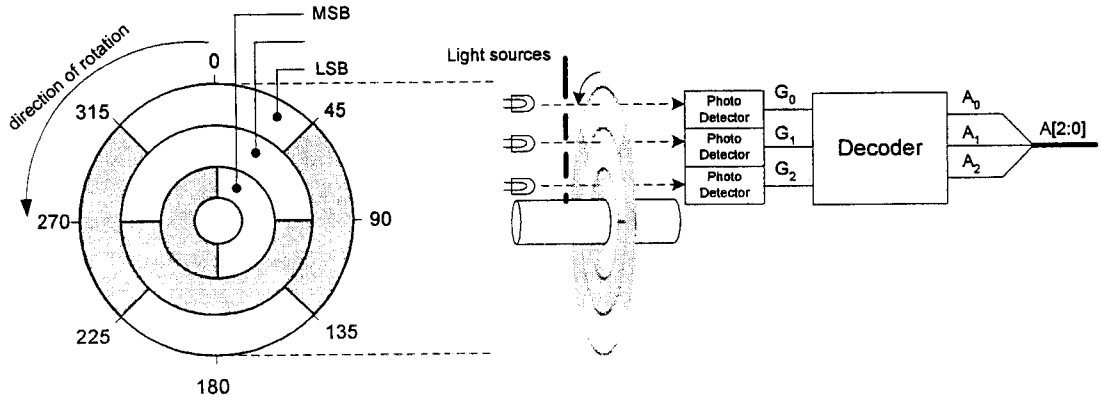


Figure 2.1

3. a) Figure 3.1 shows a finite state machine (FSM) implemented using three D-type flip-flops with outputs A, B, and C, and a number of gates.

Assuming that the states in the FSM are encoded as A:B:C with A and C being the most and least significant bits respectively, draw the state transition diagram and give the state transition table for the FSM.

[12]

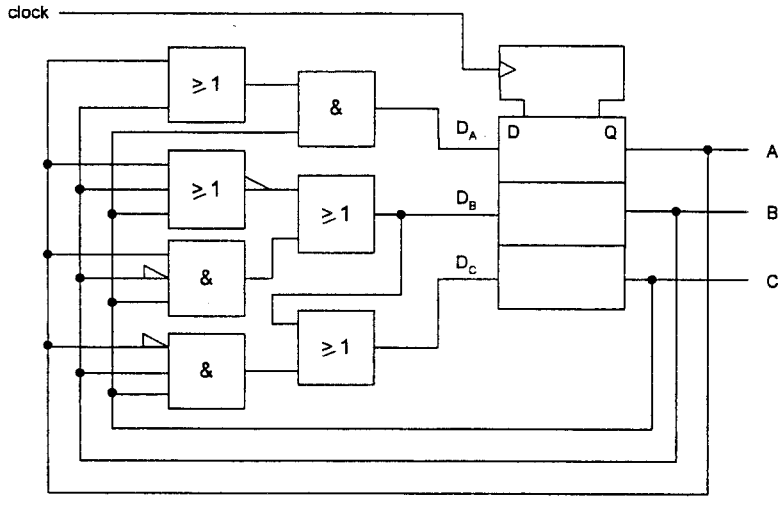


Figure 3.1

b) With the aid of a diagram, show how the following logic function can be implemented on a PAL device.

$$f = A \oplus B \oplus C$$

[8]

4. Figure 4.1 shows an arithmetic module COMP that performs comparison between two 2-bit unsigned numbers A[1:0] and B[1:0]. It produces a logic '1' on outputs GT, EQ and LT if A>B, A=B and A<B respectively.

a) Derive the Boolean expressions for GT, EQ and LT. There is no need to simplify your Boolean equations.

[12]

b) Show how you can combine three COMP modules and other appropriate logic gates to perform the same comparison operation if A and B are 6-bit numbers.

[8]

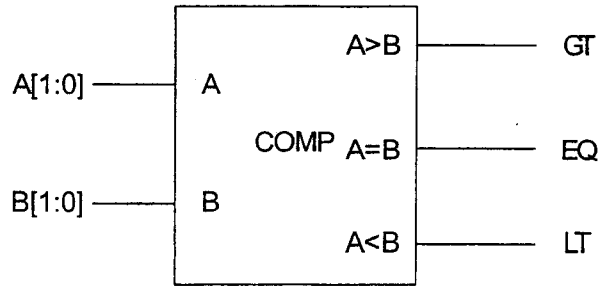


Figure 4.1

5. Figure 5.1 shows a chocolate vending machine controller that accepts either 10p or 20p coins and vends chocolate bars, each costing 30p. When a 10p or a 20p coin is inserted, P10 or P20 will respectively go high for one clock cycle shortly after the rising edge of the clock signal CLK. Only one coin can be inserted at any one time. Whenever the signal VEND is high, a chocolate bar is dispensed from the vending machine on the next clock cycle. Whenever the signal CHANGE is high, a 10p coin is returned on the next clock cycle.

   a) Design a finite state machine (FSM) in the form of a state diagram to implement the vending machine controller. State clearly any assumptions made.

   [8]

   b) Draw the state transition table for your state machine.

   [4]

   c) Derive minimized Boolean equations for your FSM.

   [8]

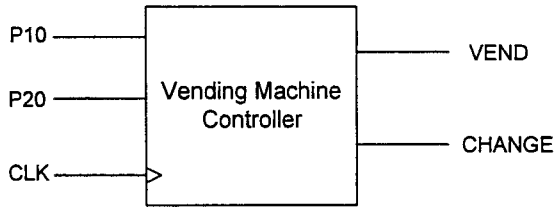


Figure 5.1

[THE END]

E1.2 Digital Electronics 1
Solutions 2004

Question 1 is compulsory.

1. a)

F

	AB	$A\overline{B}$	$\overline{A}\overline{B}$	$\overline{A}B$
C	1	0	1	0
$\overline{C}$	0	1	0	1

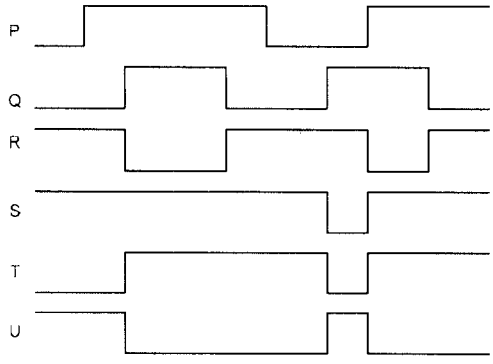
G

	AB	$A\overline{B}$	$\overline{A}\overline{B}$	$\overline{A}B$
C	1	1	0	1
$\overline{C}$	1	0	0	0

$$F = ABC + A\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C}$$
$$G = AB + AC + BC$$

[4]

b)



[4]

c)

Decimal	Hexadecimal	Binary
2765	0ACD	
23087	5A2F	0101101000101111
-1024	FC00	

[4]

d)

C	B	A	P	Q
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	0
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

[4]

e)

$$(A + C)(\overline{A} + B)$$
$$= A\overline{A} + AB + \overline{A}C + BC$$
$$= AB + \overline{A}C + BC$$
$$= AB + \overline{A}C + BC(A + \overline{A})$$
$$= AB\,(1 + C) + \overline{A}C\,(1 + B)$$
$$= AB + \overline{A}C$$

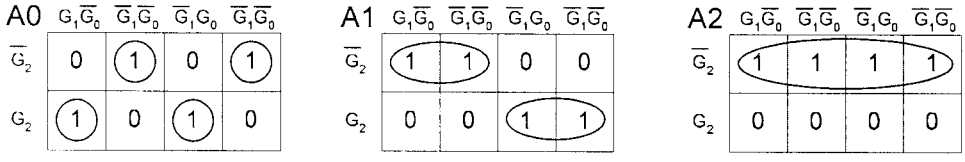
[4]

2. a)

Segment	Angle °	G2	G1	G0	A2	A1	A0
0	0 – 45	1	1	1	0	0	0
1	45 – 90	1	1	0	0	0	1
2	90 – 135	1	0	0	0	1	0
3	135 – 180	1	0	1	0	1	1
4	180 – 225	0	0	1	1	0	0
5	225 – 270	0	0	0	1	0	1
6	270 – 315	0	1	0	1	1	0
7	315 – 360	0	1	1	1	1	1

[5]

b)



$$A2 = \overline{G2}$$

$$A1 = \overline{G2}\,G1 + G2\,\overline{G1}$$

$$A0 = G2G1\,\overline{G0} + \overline{G2}\,G1G0 + G2\,\overline{G1}\,G0 + \overline{G2}\,\overline{G1}\,\overline{G0}$$

[10]

c)

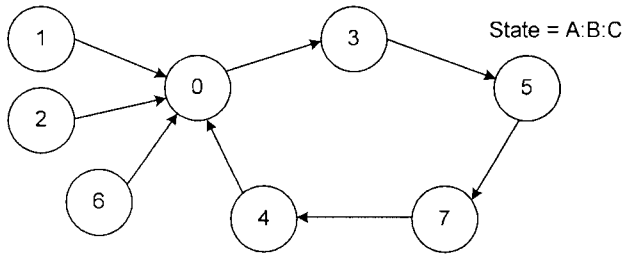
$$A2 = \overline{G2} = \overline{(G2 + G2)}$$

$$\begin{aligned}\overline{A1} &= \overline{\overline{G2}\,G1 + G2\,\overline{G1}} \\ &= \overline{\overline{G2}\,G1} + \overline{G2\,\overline{G1}} \\ &= \overline{(\overline{G2} + G1)} + \overline{(G2 + \overline{G1})}\end{aligned}$$

$$\begin{aligned}\overline{A0} &= \overline{G2G1\,\overline{G0} + \overline{G2}\,G1G0 + G2\,\overline{G1}\,G0 + \overline{G2}\,\overline{G1}\,\overline{G0}} \\ &= \overline{G2G1\,\overline{G0}} + \overline{\overline{G2}\,G1G0} + \overline{G2\,\overline{G1}\,G0} + \overline{\overline{G2}\,\overline{G1}\,\overline{G0}} \\ &= \overline{(\overline{G2} + \overline{G1} + G0)} + \overline{(G2 + \overline{G1} + \overline{G0})} + \overline{(\overline{G2} + G1 + \overline{G0})} + \overline{(G2 + G1 + G0)}\end{aligned}$$

[5]

3. a) (i)



[8]

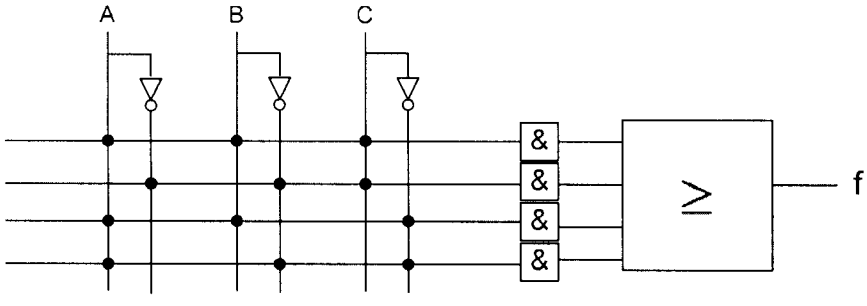
(ii)

State	A	B	C	D_A	D_B	D_C
0	0	0	0	0	1	1
1	0	0	1	0	0	0
2	0	1	0	0	0	0
3	0	1	1	1	0	1
4	1	0	0	0	0	0
5	1	0	1	1	1	1
6	1	1	0	0	0	0
7	1	1	1	1	0	0

[4]

b)

$$f = A \oplus B \oplus C$$
$$= ABC + \overline{A}\,\overline{B}\,C + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C}$$



[8]

4. a)

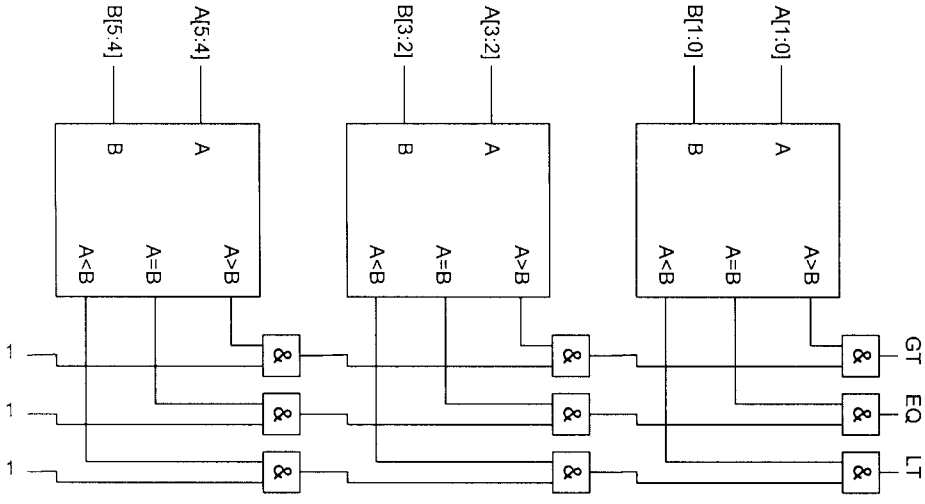
$$EQ = \overline{A1}\ \overline{B1}\ \overline{A0}\ \overline{B0} + \overline{A1}\ \overline{B1}A0B0 + \overline{A1B1A0}\ \overline{B0} + A1B1A0B0$$

$$GT = A1\overline{B1} + A1\ B1A0\ \overline{B0} + \overline{B1}\ A0\ \overline{B0}$$

$$LT = B1\overline{A1} + B1\ A1B0\ \overline{A0} + \overline{A1}\ B0\ \overline{A0}$$

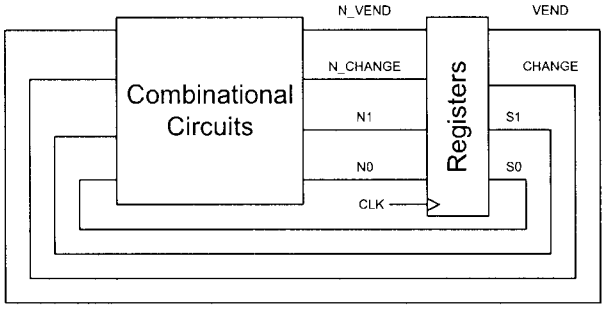
[12]

b)

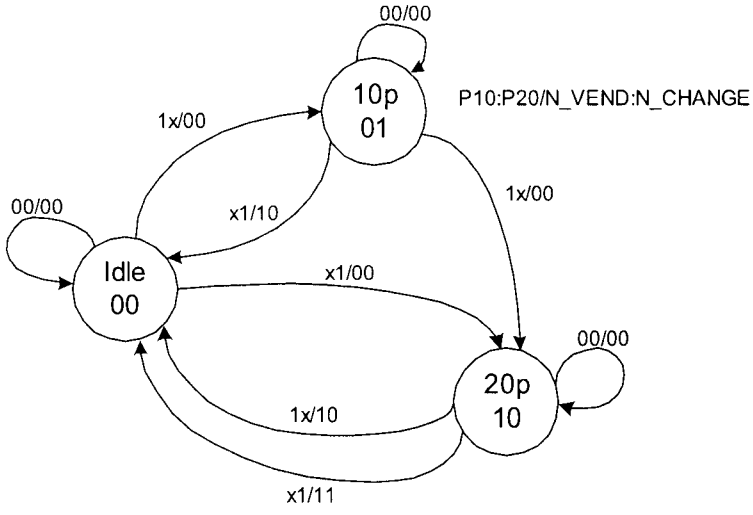


[8]

5. a) Since P10 and P20 cannot be high at the same time, we can simplify the state diagram considerably by assuming the following: if P10 is '1', P20 is a don't care and vice versa.



State diagram:



[8]

(b)

S1	S0	P20	P10	N1	N0	N_VEND	N_CHANGE
0	0	0	0	0	0	0	0
0	0	X	1	0	1	0	0
0	0	1	X	1	0	0	0
0	1	0	0	0	1	0	0
0	1	X	1	1	0	0	0
0	1	1	X	0	0	1	0
1	0	0	0	1	0	0	0
1	0	X	1	0	0	1	0
1	0	1	X	0	0	1	1

[4]

(c) Must register VEND and CHANGE so that they take effect on the next cycle.

$$N0 = P10\,\overline{S0}\,\overline{S1} + \overline{P10}\,\overline{P20}\,S0\,\overline{S1}$$

$$N1 = P20\,\overline{S0}\,\overline{S1} + P10\,S0\,\overline{S1} + \overline{P20}\,\overline{P10}\,\overline{S0}\,S1$$

$$N\_VEND = P20\,S0\,\overline{S1} + P10\,\overline{S0}\,S1 + P20\,\overline{S0}\,S1$$

$$N\_CHANGE = P20\,\overline{S0}\,S1$$

[8]