UNIVERSITY OF LONDON

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

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BEng Honours Degree in Computing Part II
MEng Honours Degrees in Computing Part II
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER 2.4

ARCHITECTURE II

Friday, May 1st 1998, 2.00 - 3.30

Answer THREE questions

For admin. only: paper contains 4 questions

1 The MIPS processor has 32 general-purpose registers. Each MIPS instruction is 4 bytes in length. The opcode occupies 6 bits for all instructions. The R-type instructions have two source register fields, one destination register field, one shift-amount field, and one 6-bit function code field; the I-type instructions have one source register field, one destination register field and one data field; the J-type instructions have one jump address field.

a Label each field and the corresponding bit length for an R-type instruction. Repeat this step for an I-type instruction and a J-type instruction.

b The MIPS Plus processor has 50 general-purpose registers instead of 32. Its instructions are still 4 bytes long, and it uses the same opcode and function code as those in the MIPS processor, although the number of bits for other fields can be different from those of the MIPS processor. Explain how this change will affect the R-type, I-type and J-type instructions. For each type of instruction, label each field and the corresponding bit length as in part a.

c The MIPS Plus Plus processor has 100 general-purpose registers. Its instructions are still 4 bytes long. For R-type instructions, the shift-amount field is shared with the second source register field. Discuss the advantages and disadvantages of the following options for the format of R-type instructions used in the MIPS Plus Plus processor:

i) for the opcode field, adopt a different number of bits from that in the MIPS processor,

ii) for the function code field, adopt a different number of bits from that in the MIPS processor,

iii) adopt a different number of bits for the two source register fields.

The three parts carry, respectively, 15%, 40%, and 45% of the marks.

2 Consider a 4-bit Arithmetic Logic Unit (ALU) which can perform addition and bit-wise logical AND for numbers in two's complement representation.

a Draw:

i) a circuit diagram showing the internal structure of a component ALUB which can be replicated 4 times to form the ALU. Do not show the internal structure of multiplexors and fulladders;

ii) a circuit diagram showing how the ALU can be built from 4 copies of ALUB. Label the signal values on all the wires in the diagram when the ALU adds the two numbers 0011 (3 in base ten) and 1111 (-1 in base ten).

b Explain what is overflow when adding two numbers. Design an overflow detector for the 4-bit ALU, using a single 2-input logic gate. Label the signal values on all the wires in the ALU with the above overflow detector when adding the two numbers 0111 and 0100. Hint: consider the truth table for the fulladder at the most-significant bit.

c A 4-bit circuit ABS is required for computing the absolute value of a number in two's complement representation.

i) Design a circuit A, containing only an exclusive-or gate and a halfadder, which can be replicated to form ABS.

ii) Show how ABS can be built from 4 copies of A. Label the signal values on all the wires in your circuit for the input 1111.

d The ALU in part a is to be extended to produce the absolute value of its first input. The extended ALU contains 4 copies of the component ALUBA.

i) Show how the circuit ALUB in part a and the circuit A in part c can be combined to form ALUBA.

ii) Show how the extended ALU can be built from 4 copies of ALUBA.

The four parts carry, respectively, 20%, 30%, 30%, and 20% of the marks.

Turn over...

3a Explain how the WHILE-loop can be implemented in hardware using the token-passing method. Your circuit diagram should clearly indicate the *start* input for the token to enter, and the *finish* output for the exit of the token.

b Provide a circuit for generating a single token to initialise a circuit produced by the token-passing method.

c The following program generates the sequence 1,3,6,10,15,... in the 8-bit variable `X`:

```
int_8 X, Y
SEQ
  X, Y := 1, 2
  WHILE TRUE
    X, Y := X+Y, Y+1
```

Provide a diagram for the circuit produced by compiling the above program using the token-passing method. Label the number of bits for each multi-bit wire.

d It is suggested that, instead of compiling the program in part c directly into hardware, the program can be translated into machine code for execution by a processor with the following fetch-decode-execute loop (comments are preceded by two dashes):

```
int_4 PC: int_6 IR: int_8 A: [16] int_8 M:
WHILE TRUE
  SEQ
    IR, PC := M[PC], PC+1
    CASE ((Opcode(IR))
      0: A   := Operand(IR)              -- LDC instruction
      1: M[Operand(IR)] := A             -- STA instruction
      2: A   := A + M[Operand(IR)]       -- ADD instruction
      3: PC := Operand(IR)               -- JMP instruction
```

`Opcode(IR)` and `Operand(IR)` correspond respectively to the opcode field and the operand field extracted from `IR`. Develop a machine code program for this processor which will implement the program in part c.

e Compare the implementations in part c and part d, given that the processor in part d is also compiled into hardware using the token-passing method.

The five parts carry, respectively, 20%, 15%, 25%, 25% and 15% of the marks.

4a Suggest advantages and disadvantages of increasing the cache size for a given processor.

b A machine M1 with a cycle time $t1$ takes on average c cycles per instruction without considering memory stalls. M1 has a miss penalty of p cycles for all misses. When executing a program P with n instructions and f data references per instruction, M1 has an instruction miss rate $i1$ and a data miss rate $d1$. Calculate the time $T1$ for M1 to execute P, ignoring effects of write buffer stalls.

c A machine M2 is the same as M1, except that it has a larger cache. As a result, M2 has a different cycle time $t2$, instruction miss rate $i2$ and a data miss rate $d2$ when compared with M1. Which is likely to be larger, $t1$ or $t2$? Also compare the values of $i1$ and $i2$, and $d1$ and $d2$. Justify your answer briefly.

d Derive a formula for the average cycles per instruction without considering memory stalls (variable c described in part b) such that the time $T2$ for M2 to execute P is larger than $T1$.

e A machine M3 is the same as M1, except that it has a second-level cache which has a miss penalty α times that for the main memory ($\alpha < 1$). As a result, both the instruction miss rate and the data miss rate to main memory are reduced by a factor of β when compared with M1. Calculate the following for M3:

i) the number of stall cycles per instruction for the secondary cache,

ii) the number of stall cycles per instruction for the main memory,

iii) the execution time for P.

The five parts carry, respectively, 15%, 20%, 15%, 15% and 35% of the marks.

End of paper