IMPERIAL COLLEGE OF SCIENCE TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
M.Eng. and A.C.G.I. EXAMINATIONS 2001

PART IV

INTRODUCTION TO DIGITAL IC DESIGN

This is a THREE HOUR paper.
There are SIX questions in this paper. Answer FOUR questions.

This is an open-book examination.

You may need red, green, blue, yellow and black coloured pens.

First Marker: *PYKC/TJWC*
Second Marker: *TJWC/PYKC*

1. a) Using your own group design project as a reference, describe the proper procedure for designing a full-custom integrated circuit.

[4 marks]

b) Draw a diagram showing the hierarchy of cells used in the chip that your group designed. Comment on the partitioning of your design in light of the cell hierarchy.

[4 marks]

c) Outline your own personal contributions and justify any design decisions made. If you and your group were to design the same chip again, what if anything would you have done differently?

[8 marks]

d) Explain and assess the strategy you adopted for verifying and testing your chip.

[4 marks]

2. a) *Figure 1* (See the colour supplementary sheet) shows the layout of a CMOS cell with three inputs `IN1`, `IN2` and `IN3`, and one output `OUT`. Extract and draw the transistor-level schematic diagram.

[10 marks]

b) Draw the vertical cross sections through the chip along the lines `AA'`, `BB'` and `CC'`. Label your diagram and indicate the different types and levels of doping (e.g. p^-, n^+ etc).

[8 marks]

c) What function does this circuit perform?

[2 marks]

3. a) *Figure 2a* shows the transistor-level schematic diagram of a sequential circuit. Given that the timing diagram for the input signals `CLK`, `IN1` and `IN2` is as shown in *Figure 2b*, draw the timing diagram for the signals at `P`, `Q`, `R`, `S` and `OUT`. Label your timing diagram indicating the various states of the signal nodes as:

driven low (DL) - a path to ground exists,
driven high (DH) - a path to Vdd exists,
weak low (WL) - a path to ground through a p-channel transistor exists,
weak high (WH) - a path to Vdd through a n-channel transistor exists,
charged low (CL) - high impedance with no stored charge, and
charged high (CH) - high impedance with stored charge at Vdd.

[14 marks]

b) Hence or otherwise, explain the function of this circuit.

[6 marks]

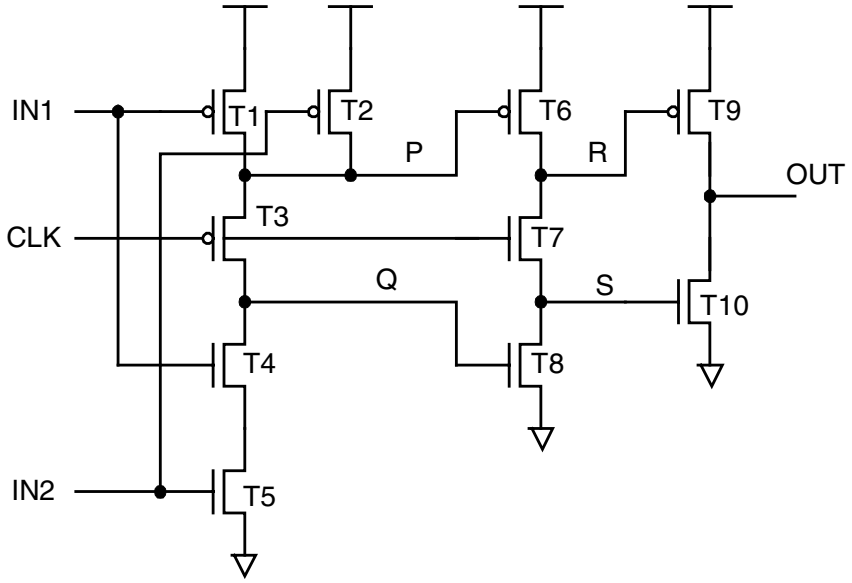


Figure 2a

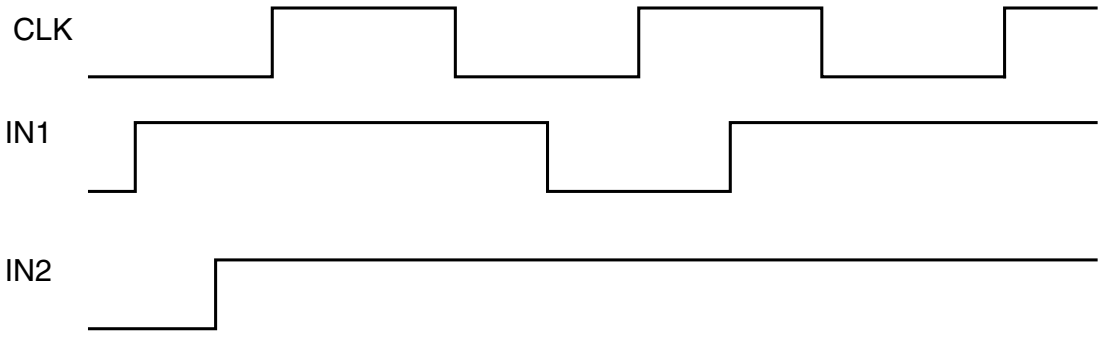


Figure 2b

4. a) *Figure 3a* shows a circuit used for calibrating the speed of a CMOS process. It contains one NAND gate and 18 inverters connected as a ring oscillator. The output is measured via another inverter acting as a buffer. All transistors in the NAND gate are of minimum size with width of 0.25µm, and all inverters are also of minimum size with p and n transistors having widths of 0.5µm and 0.25µm respectively. The measured oscillation frequency at the output `X` is 983.6 MHz.

Estimate the delay t_d of a minimum-sized inverter driving an identical inverter.

[5 marks]

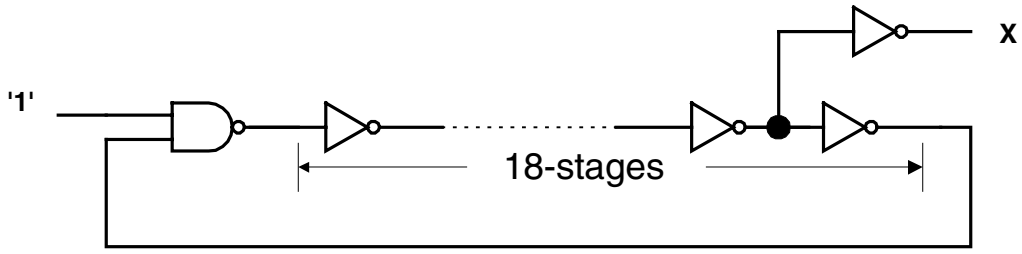
b) A circuit using the same CMOS process contains three separate clock paths `P1`, `P2` and `P3` as shown in *Figure 3b*. The total gate width seen by the three paths are 600µm. 400µm and 200µm respectively.

(i) Using the method of logical effort, or otherwise, estimate the clock skews between the paths.

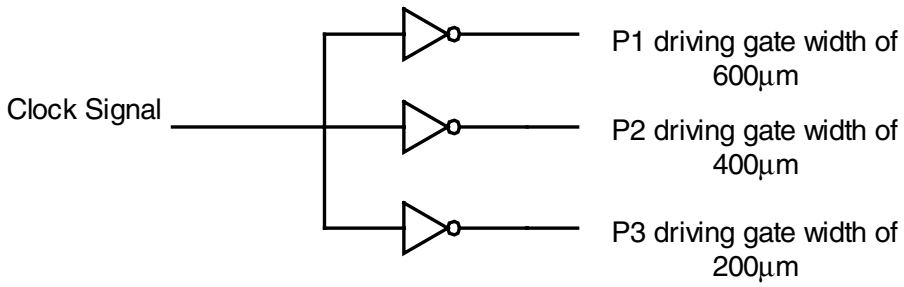
[7 marks]

(ii) Design suitable buffer circuits for each clock path so that the clock signal delay on each path is minimized. Give the sizes of the transistors in the buffer circuits and estimate the new clock skews between the paths.

[8 marks]



(a) Ring Oscillator



(b) Three Clock Paths

Figure 3

5. *Figure 4a* shows part of an address decoder circuit for a CMOS memory chip. `T1` and `T6` are strong and weak transistors respectively when compared with the pull-down transistors `T2-T5`. The signals `addr5:0` forms the 6-bit row address of a memory array.

a) Design the predecoder circuit so that the output signal `Y` drives the WORD line high for the row address $3A_{16}$.

[4 marks]

b) Given that the timing diagram for the input signals `addr_clock` and `addr5:0` are as shown in *Figure 4b*, draw the timing diagram for the signals at `X` and `Y`. Label your timing diagram with the following four possible signal states: *driven low* (**DL**), *driven high* (**DH**), *charged low* (**CL**) and *charged high* (**CH**).

[6 marks]

c) Design the layout of the decoder circuit shown in *Figure 4a* (excluding the predecoder) in the form of symbolic layout or stick diagram.

[10 marks]

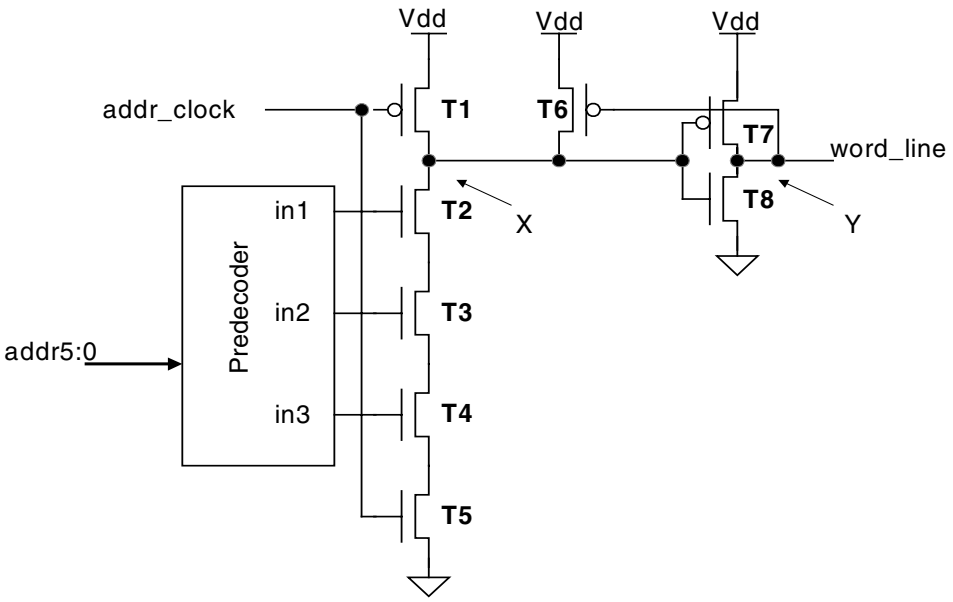


Figure 4a

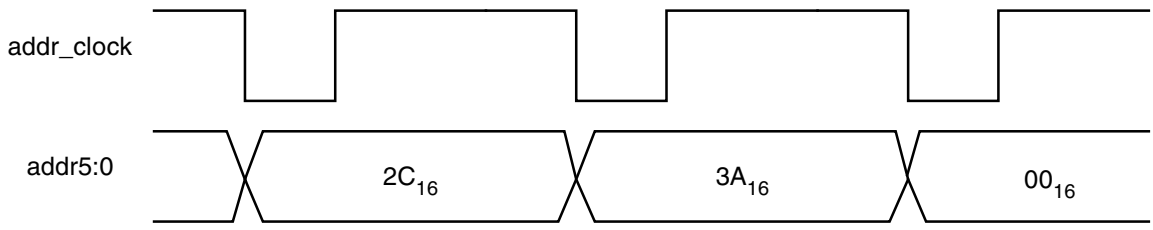


Figure 4b

6. a) Deduce the Boolean equation for the circuit shown in *Figure 5*.

[4 marks]

b) By applying either the path sensitisation or the Boolean differences method, find all the test vectors that will detect stuck-at faults at the node B.

[8 marks]

c) By using the circuit shown in *Figure 5*, or otherwise, design a transistor-level circuit of a single-bit scan-path register.

[8 marks]

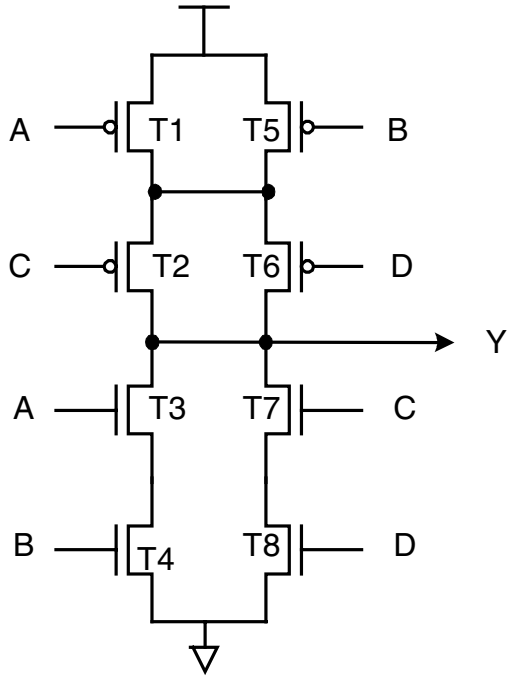


Figure 5

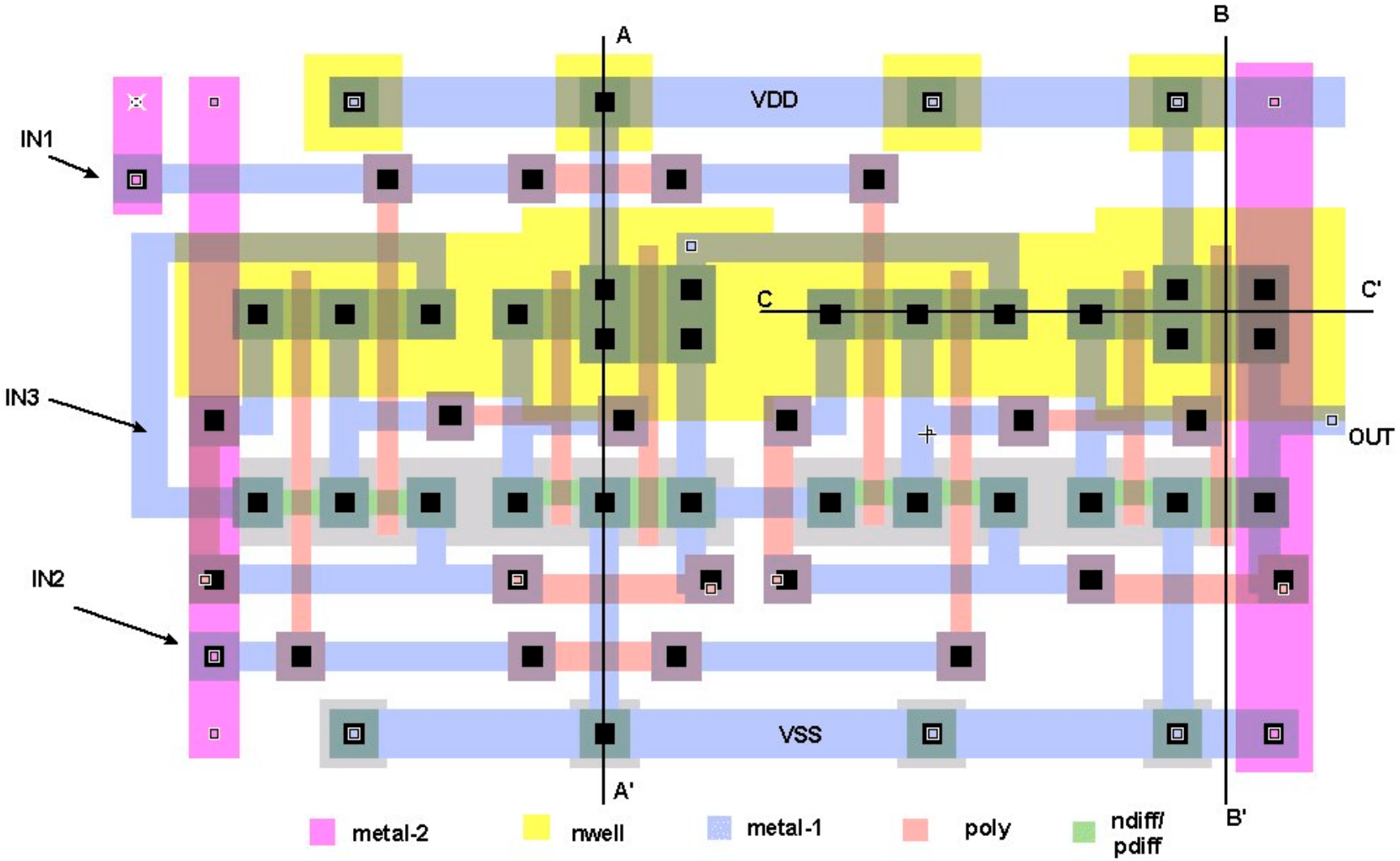


Figure 1 Layout of a full-custom cell for Question 2

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SOLUTIONS

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Solution to Question 1

Each student was involved in a group design project to design a full-custom integrated circuit during the course. Since they were learning while doing the project, a number of mistakes were made. The four parts of this question are intended to test how much each student learned through this experience.

a) The following are some of the points expected to be discussed:
- Clarify specification of project right from the start, avoid chaning spec during design
- Adhere to top down design approach as much as possible. Model chip behaviourally to verify chip function
- Careful floorplanning early on for the entire chip
- For cell based designs, define cell boundary size and terminal location
- Use autoplace & route tools if possible
- Consider test right at the beginning of the design cycle. Design a good test vectore file, and use it for regressive verification and testing
- Maximize regularity and minimize different types of cell designs
- Pitch-match cells where possible
- Hierarchical design, both simulation and layout. Avoid excess use of hierarchy

I also expect more individual answers depending on student's chip design.

[4 marks]

b) This part depends on student's chip.

[4 marks]

c) This part of the question allows for recognition of individual understanding of, and contribution to, the project. In particular students are expected to learn from what they have done and suggest improvements to both the tools they used and the nature of project undertaken.

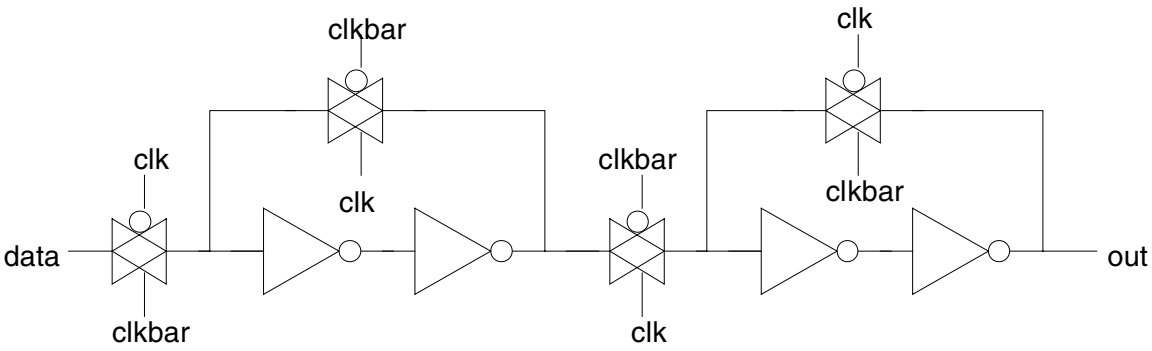
[8 marks]

d) I expect students to have at least a high level model of the chip to generate test vectors. I also expect them to consider test coverage and possibly some of design for test such as scan registers or even built-in self tests.

[4 marks]

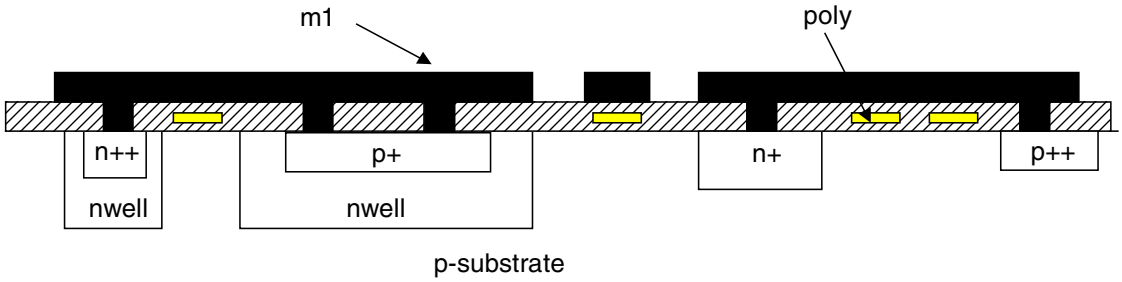
Solution to Question 2

a) IN1 = clk; IN2 = clkbar; IN3 = data; OUT = out.

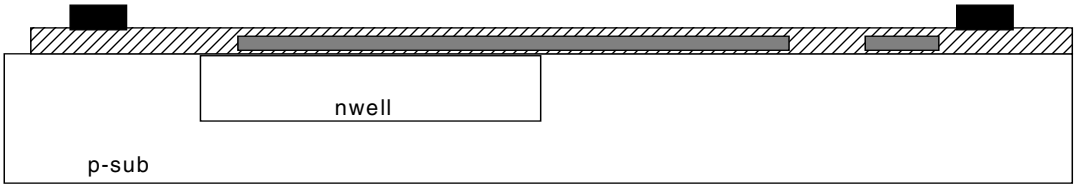


[10 marks]

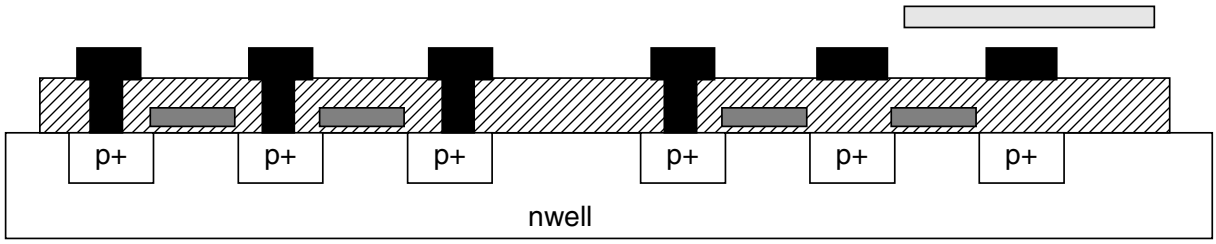
b) Cross-section of AA':



Cross-section of BB'. Note that no diffusion underneath the polysilicon gate



Cross-section of CC'.



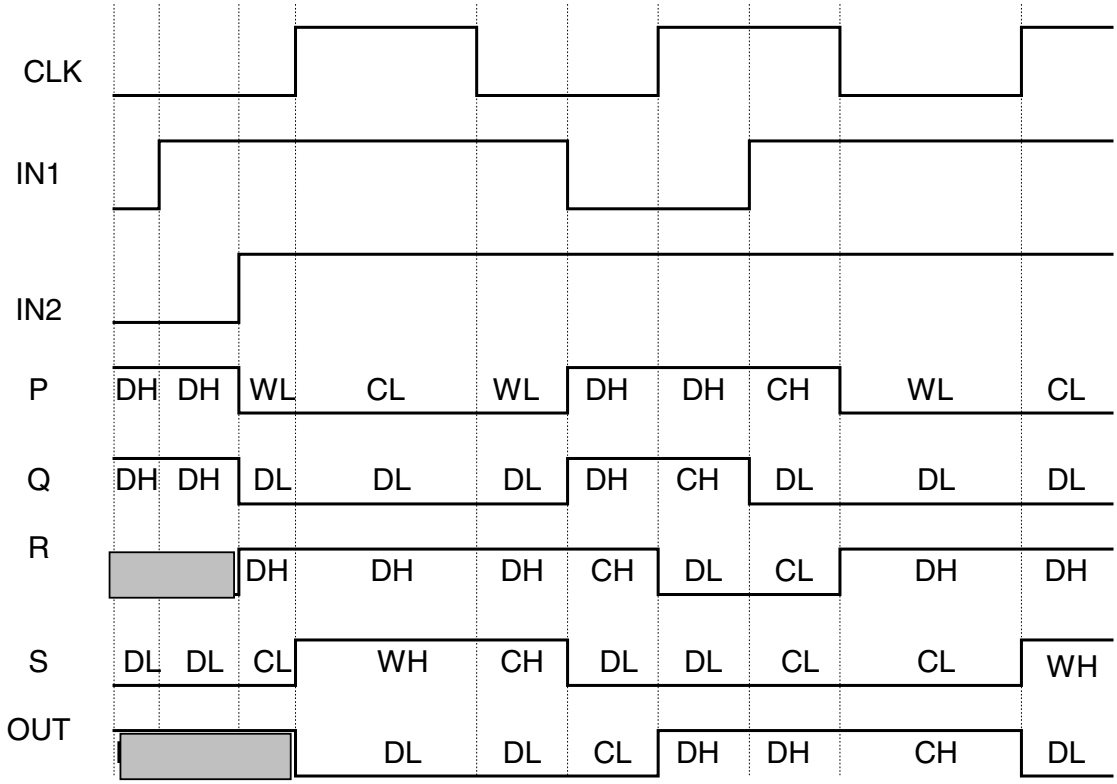
[8 marks]

c) This is a D flip-flop using two phase complementary clock signals.

[2 marks]

Solution to Question 3

a)



[14 marks]

b) This is a true single phase positive edge triggered flip-flop with a 2-input NAND gate function integrated at the front.

[6 marks]

Solution to Question 4

a)

This question tests the student's ability to apply Ivan Sutherland's "Method of Logical Effort" to delay estimation and transistor sizing.

Delay of the ring oscillator chain:

Nand ----------17 inv (unit load) ------- inv (double load)

4/3 td + 17 td + 2 td = 20.333 td

Therefore 0.5x(1/983.6MHz) = 20.333 td, td ≈ 25 ps.

[5 marks]

b) Gate width of minimum size inverter (as seen by previous stage) is 0.75 μm. Therefore, the Electrical Effort for the two paths are:

H_{P1} = 600 /0.75 = 800; H_{P2} = 400 / 0.75 = 533; H_{P3} = 200/0.75 = 267.

Delay estimates of the three paths are: D_{P1} = 800 * td = 20 ns; D_{P2} = 533 * td = 13.3 ns; D_{P3} = 267 * td = 6.7ns.

P1-P2 skew = 6.7 ns; P2-P3 skew = 6.6 ns; P1-P3 skew = 13.3 ns.

[7 marks]

c)

Total effort for P1 = 800 P2 = 533 and P3 = 267. From table in notes, P1 should be buffered by 6 inverter stages, P2 also by 6 stages and P3 by 4 stages, in order to minimize delay.
Therefore for P1, each stage should increase in size by $\sqrt[6]{800} = 3.05$,
for P2, each stage should increase in size by $\sqrt[6]{533} = 2.85$,
for P2, each stage should increase in size by $\sqrt[4]{267} = 4.03$.

Solution – increase sizes of p-trans and n-trans by these factors for each of the stages:

Stage	1	2	3	4	5	6
P1:	x 1	: x 3	: x 9	: x 28	: x 86	: x 263
P2:	x 1	: x 3	: x 8	: x 24	: x 71	: x 207
P3:	x 1	: x 4	: x 14	: x 53		

P1 delay ≈ (3/1 + 9/3 + 28/9 + 86/28 + 263/86 + 800/263) * td = 18.3 td
P2 delay ≈ (3/1 + 8/3 + 24/8 + 71/24 + 207/71 + 600/207) * td = 17.5 td
P3 delay ≈ (4/1 + 14/4 + 53/14 + 200/53) * td = 15.1 td

Therefore new clock skews are:

P1-P2 skew = 20 ps; P2-P3 skew = 60 ps; P1-P3 skew = 80 ps.

[8 marks]

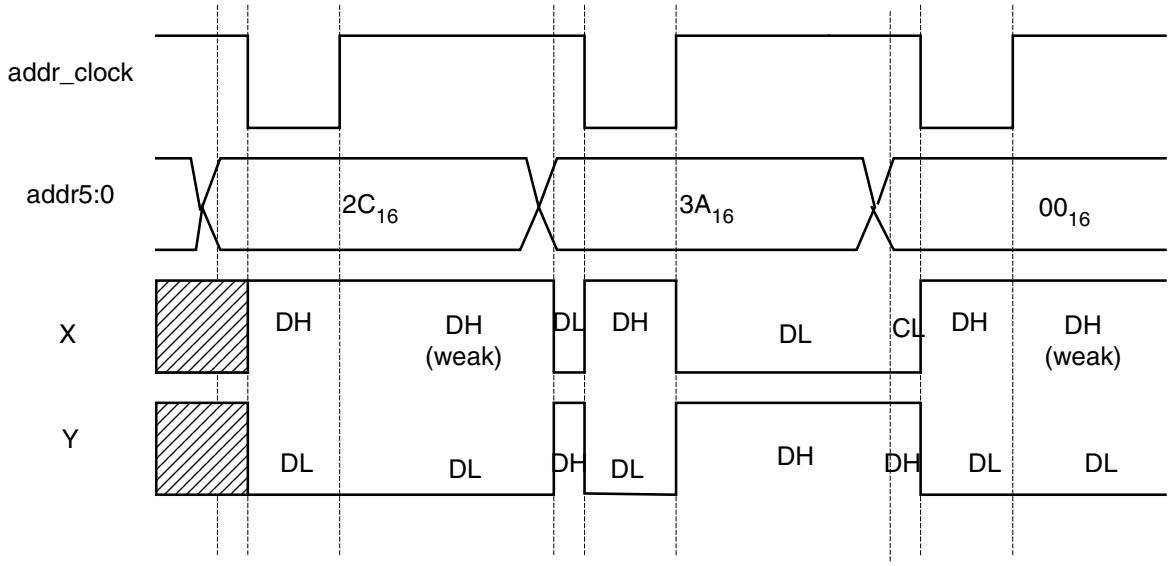
Solution to Question 5

a)

```
IN1 = !addr0 • addr1
IN2 = !addr2 • addr3
IN3 = addr4 • addr5
```

[4 marks]

b)



[6 marks]

c) Layout depends on student's design.

[10 marks]

Solution to Question 6

a)

Y = NOT (A*B + C*D)

[4 marks]

b) Use boolean difference method:

Y (B=0) = Y (A,0,C,D) = NOT (C*D)
Y (B=1) = Y (A,1,C,D) = NOT (A + C*D)

Therefore boolean difference is:

dY/dB = Y(B=0) XOR Y(B=1)
= NOT (C*D) XOR NOT(A + C*D)
= A* NOT(C) + A*NOT(D)

To test for stuck-at-0 fault at B,
test input = B*(dY/dB),
= A*B*NOT(C) + A*B*NOT(D) = 1

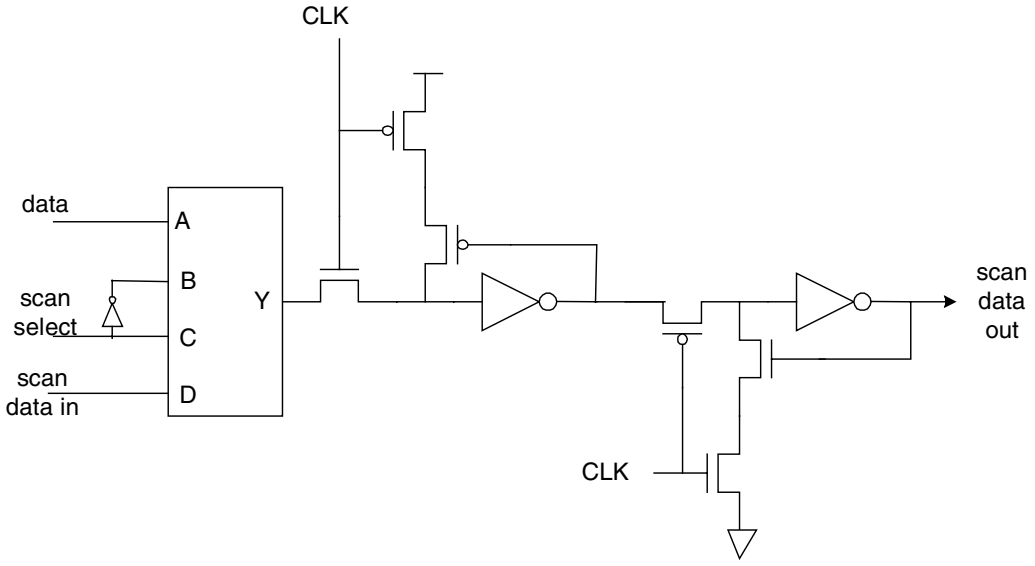
Therefore the test vector for B stuck-at-0 = 110x and 11x0, i.e. (1100, 1101, 1110)

To test for stuck-at-1 fault at B,
test input = NOT(B)*(dY/dB),
= A*NOT(B)*NOT(C) + A* NOT(B)*NOT(D) = 1

Therefore the test vector for B stuck-at-1 = 100x and 10x0, i.e. (1000, 1001, 1010)

[8 marks]

c) If B = NOT(C), then we can use the cell as a MUX between A and D inputs.



[8 marks]