Paper Number(s): **E3.05**
AC2
ISE3.19

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2002

MSc and EEE/ISE PART III/IV: M.Eng., B.Eng. and ACGI

DIGITAL SYSTEM DESIGN

Thursday, 25 April 10:00 am

There are SEVEN questions on this paper.

Answer FOUR questions.

Time allowed: 3:00 hours

Corrected Copy

Examiners responsible:

First Marker(s): Cheung,P.Y.K.

Second Marker(s): Brookes,D.M.

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X7:0 is an eight bit bus with X7 being the MSB and X0 the LSB.

Hexadecimal numbers are prefixed with '$'. For example the decimal number 10 is written as $A.

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

1. The operation of a 9-tap convolver is given by the equation

$$y = \sum_{n=0}^{8} a_n x_n \qquad (1)$$

where $\{a_0, a_1, ..., a_8\} = \{1.5, 0.375, -0.625, 0.375, 0.125, -0.125, 1.25, -0.125, 0.25\}$, and x_n for n = 0 to 8 are 8-bit integer data in 2's complement form.

a) Show that Equation 1 can be rewritten as:-

$$y = \{\left[\left[(x_0 + x_6)\times 2 + (x_0 - x_2)\right]\times 2 + (x_1 + x_3 + x_6 + x_8)\right]\times 2 + (x_1 - x_2 + x_3 + x_4 - x_5 - x_7)\}\times 0.125$$

[6 marks]

b) Hence, or otherwise, design a circuit to implement this convolver using a tree of two-input adders or subtractors. Explain clearly how the adders and subtractors are interconnected in order to ensure that no overflow can occur. Show clearly the width of all the datapaths in your circuit and the position of the binary point at the output.

[14 marks]

2. a) Given that $1 + x^4 + x^9$ is a primitive polynomial, design a pseudo random binary sequence generator circuit with a sequence length of 511. Your circuit should work regardless of the initial state of any registers.

[6 Marks]

b) In a data processing system, all data are stored in memory as 4-bit digits. To ensure any single bit error can be corrected, each digit is stored with its Hamming error correction codes.

(i) How many check bits are required for each digit? Show the Boolean relation between the data bits and each check bit.

[4 Marks]

(ii) If a stored value of 1010 is retrieved as 1000, demonstrate how this error can be corrected.

[5 Marks]

(iii) Design a digital circuit that corrects any single bit errors when a digit is read from memory. Your solution can be in the form of Boolean equations.

[5 Marks]

3. a) Explain what is meant by metastability in a digital system and the circumstances under which it can arise.

[3 marks]

b) *Figure 3.1* shows a circuit to synchronise an asynchronous input A to a synchronous system G. The synchronous system G can operate with a maximum clock frequency of 100 MHz and the input setup time is 2 ns. The flip-flops FF1 to FF4 have a setup time of 3 ns and clock-to-output delay of 5 ns. Ignoring the possibility of metastability, what is the maximum clock frequency of this circuit?

[5 marks]

c) The mean time between failures (MTBF) of a synchronising flip-flop is given by:

$$MTBF = \frac{e^{\left(\frac{t}{\tau}\right)}}{T_o \times f \times a} \qquad (2)$$

where t is the maximum duration over which metastability may persist from the time of the clock edge without causing errors, f is the frequency of the clock signal to the synchroning flip-flop, a is the transition rate of the asynchronous input, and $T_0 = 1.0 \times 10^{-10} s$ and $\tau = 0.23 ns$ for these flip-flops.

Using the maximum clock frequency determined in b), and assuming that the asychronous transition rate is 10MHz, determine the synchronizer's MTBF.

[8 marks]

d) If the MTBF is not sufficiently high, outline how this circuit could be modified to improve it.

[4 marks]

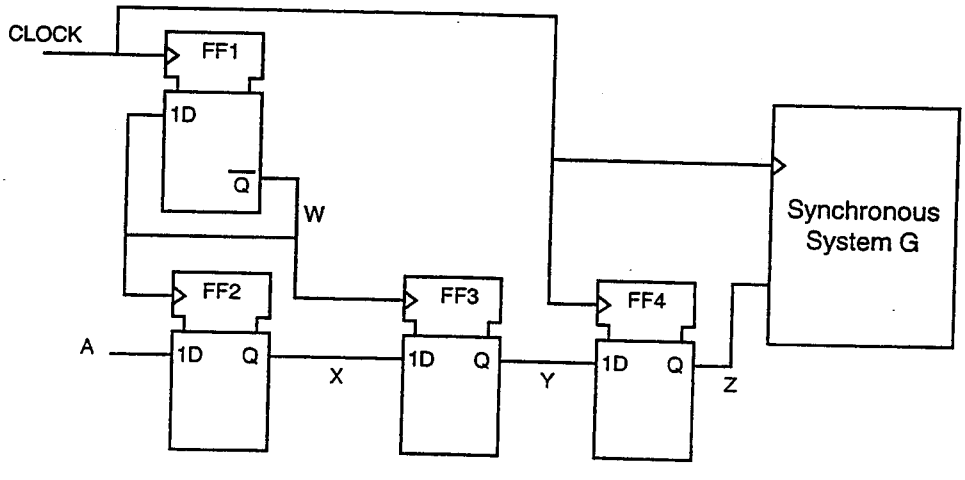

Figure 3.1

4. Given that x and y are N-bit signed two's complement numbers and that N is even, a modified Booth encoded multiplier implements the function shown in Equation 3.

$$x \times y = y \times \sum_{j=0}^{N/2-1} 2^{2j}(-2x_{2j+1} + x_{2j} + x_{2j-1}) \qquad (3)$$

where $x_{-1} = 0$, and for $i \geq 0$, x_i is bit i of the multiplier x, and y is the multiplicand.

Figure 4.1 shows a block diagram of a modified Booth encoded parallel multiplier for N=8 with 4 identical stages. Each stage consists of two modules: the Booth encoder module (BE) and the partial product module (PP). The BE module takes three bits from the multiplier x and performs modified Booth encoding. The PP module calculates $y \times 2^{2j}(-2x_{2j+1} + x_{2j} + x_{2j-1})$ for a particular value of j and adds it to the cumulative total.

a) Design the BE module at gate level showing the three outputs D (double), N (not-zero) and S (subtract).

[4 marks]

b) Design the PP module using AND gates, multiplexers and parallel adders/subtractors, showing the sizes of all datapaths including p, q and r, and how the final product is formed.

[12 marks]

c) Assume that the delay of any gate, a multiplexer and the clock-to-output delay of a register is 1 ns, and the delay of an m-bit adder is $2m$ ns, the setup and hold times of a register are respectively 1ns and 0ns. Determine the worst case delay from any input to any output of the multiplier.

[2 marks]

d) Pipelining can be used between each stage to increase the clock frequency of a system using this multiplier. Estimate the maximum clock frequency that can be used with this pipelined multiplier. State any assumptions used.

[2 marks]

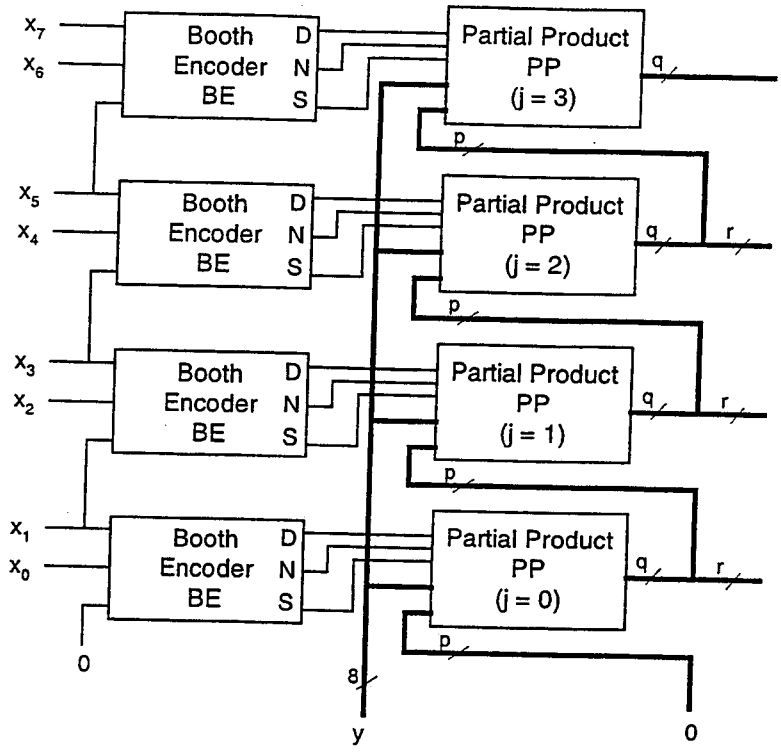
x_7
x_6
Booth Encoder BE
D N S
Partial Product PP (j = 3)
q
p
x_5
x_4
Booth Encoder BE
D N S
Partial Product PP (j = 2)
q
r
p
x_3
x_2
Booth Encoder BE
D N S
Partial Product PP (j = 1)
q
r
p
x_1
x_0
Booth Encoder BE
D N S
Partial Product PP (j = 0)
q
r
p
0
8
y
0

Figure 4.1

5. *Figure 5.1* shows the schematic of a 4-input, 4-output finite state machine (FSM) implemented using an Embedded Array Block (EAB) in Altera's FLEX10K PLD device. The input `IN3:0` to the FSM is one-hot encoded. The EAB is configured as a 256 x 8 ROM with registered address inputs. The contents of some of the ROM locations are shown in *Figure 5.2*. All the other locations contain the value 0.

   a) Draw a state transition diagram for this FSM.

   [8 marks]

   b) A Logic Element (LE) in Altera's FLEX10K PLD device consists of a 4-input lookup table and a flip-flop. Re-implement the FSM using LEs instead of EAB in the FLEX10K device using one-hot state encoding. How many LEs are required to implement the FSM?

   [12 marks]

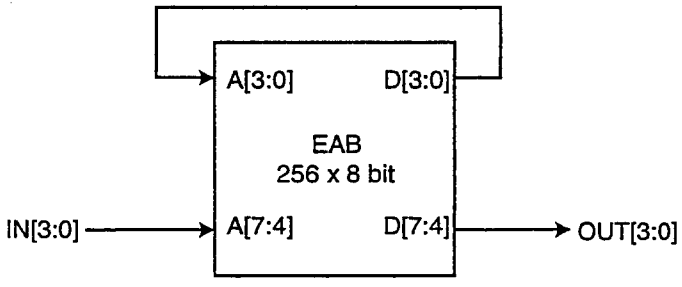

Figure 5.1

FSM inputs A[7:4]	A[3:0]	FSM outputs D[7:4]	D[3:0]
1	0	3	1
2	0	3	2
4	0	3	3
8	1	5	0
4	1	5	5
1	2	A	1
4	2	A	5
1	3	C	1
8	3	C	4
1	4	F	5
4	4	F	3
1	5	4	5
2	5	4	0

Figure 5.2

6. In a 32-bit microprocessor system shown in *Figure 6.1*, a 1K X 32 bit cache memory is used to increase the effective speed of the main memory. The operation of the microprocessor and the memory interface circuit is controlled by the clock signal *CLK*. *Figure 6.2* shows the timing diagram during three different types of memory accesses.

The address bus *A31 : 2* becomes valid and the address strobe signal $\overline{AS}$ is asserted in T_0 shortly after the rising edge of *CLK*. The microprocessor samples the data acknowledge signal $\overline{DTACK}$ on the rising edge of *CLK* at the end of T_1. If $\overline{DTACK} = 0$, the microprocessor completes the current memory access and proceeds to the next memory operation. However if $\overline{DTACK} = 1$, the microprocessor inserts a wait cycle and continues to sample $\overline{DTACK}$ until it becomes 0. During T_0 $\overline{WR}$ is set to low for a write operation and set to high for a read operation.

During a memory read operation, if the data being accessed is stored in cache memory, the cache circuitry asserts *HIT* before the end of T_0 indicating that the data will be available from the cache at the end of T_1. Such a cache read operation takes only 2 clock cycles to complete. However if the data being accessed is not in cache, *HIT* is deasserted and data must be read from main memory at the end of T_4. At the same time it is also written to cache by asserting the $\overline{WCACHE}$ signal. Such a main memory read operation takes 5 cycles to complete.

All memory write operations also take 5 cycles to complete at the end of T_4 by asserting $\overline{WMEM}$ and $\overline{WCACHE}$ signals in T_4. Writing to main memory is always accompanied by writing to the cache.

Design a finite state machine that takes as input signals $\overline{AS}$, $\overline{WR}$ and *HIT*, and produces the signals $\overline{DTACK}$, $\overline{WCACHE}$ and $\overline{WMEM}$.

[20 marks]

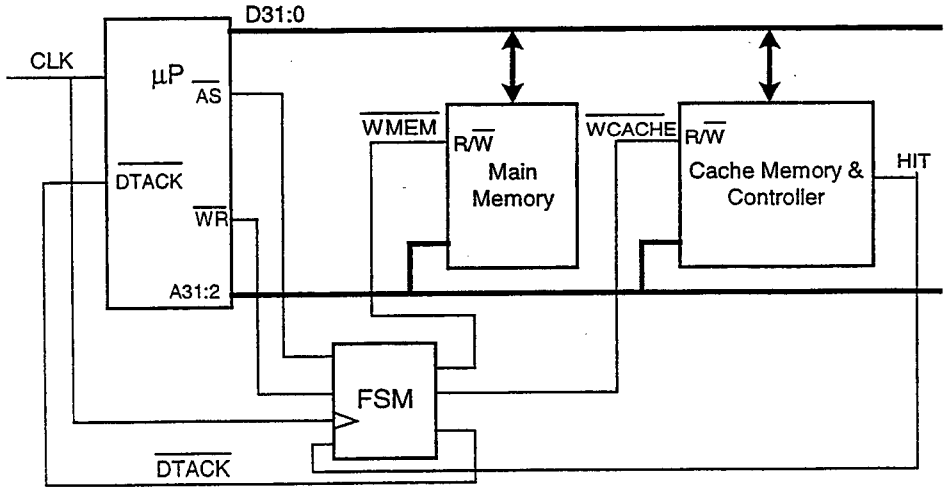

Figure 6.1

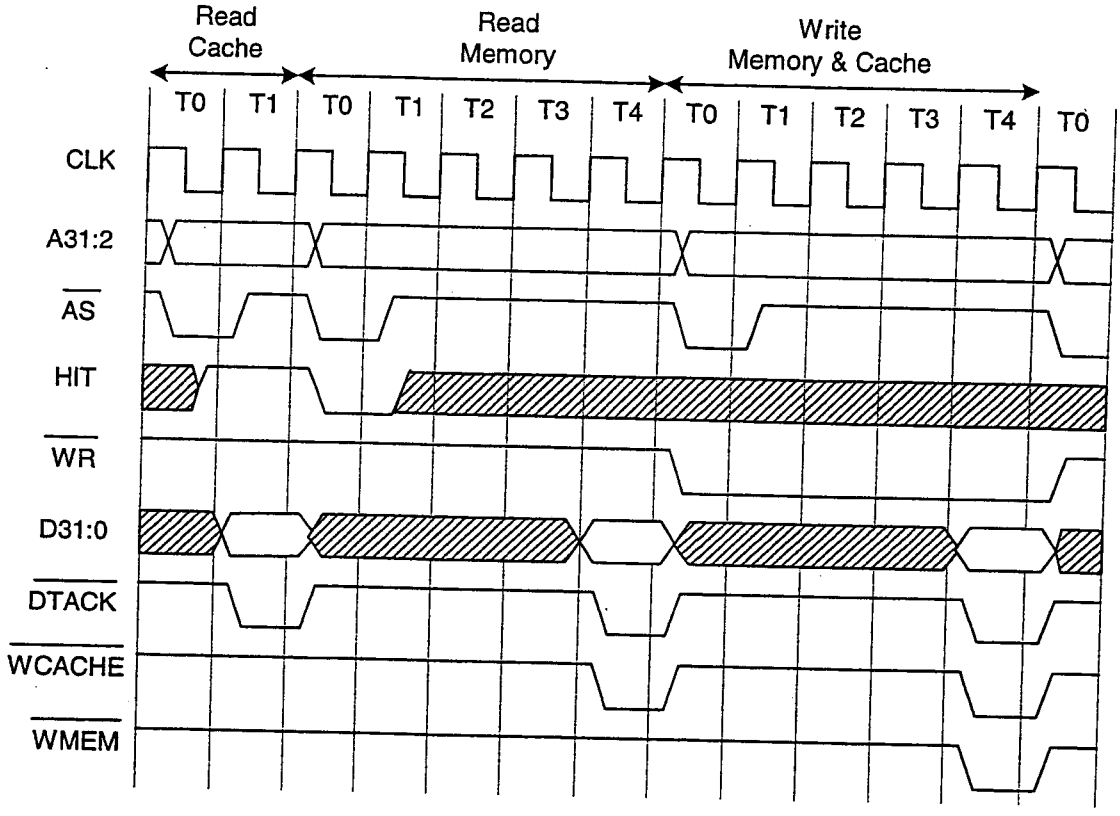
Read
Cache
Read
Memory
Write
Memory & Cache
T0
T1
T0
T1
T2
T3
T4
T0
T1
T2
T3
T4
T0
CLK
A31:2
AS
HIT
WR
D31:0
DTACK
WCACHE
WMEM

Figure 6.2

7. *Figure 7.1* shows a clock controller circuit consisting of a 4-bit up-counter with synchronous load inputs M1. The preload input of the counter is connected to an unsigned 4-bit number N3 : 0. The counter output is CNT3 : 0. The signal X goes low whenever CNT3 : 0 equals to 15.

   a) *Figure 7.2* shows the timing diagram for the signals CLK and S. Complete the timing diagram showing the signals CLK, S, X, SCLK and CNT3 : 0 given that N3 : 0 = 13. The initial state of CNT3 : 0 is 15 as shown.

   [12 marks]

   b) Given that the frequency of the clock signal CLK is f_c, derive an expression for the average frequency of SCLK when S is high in terms of f_c and N, where N is the value of N3 : 0.

   [8 marks]

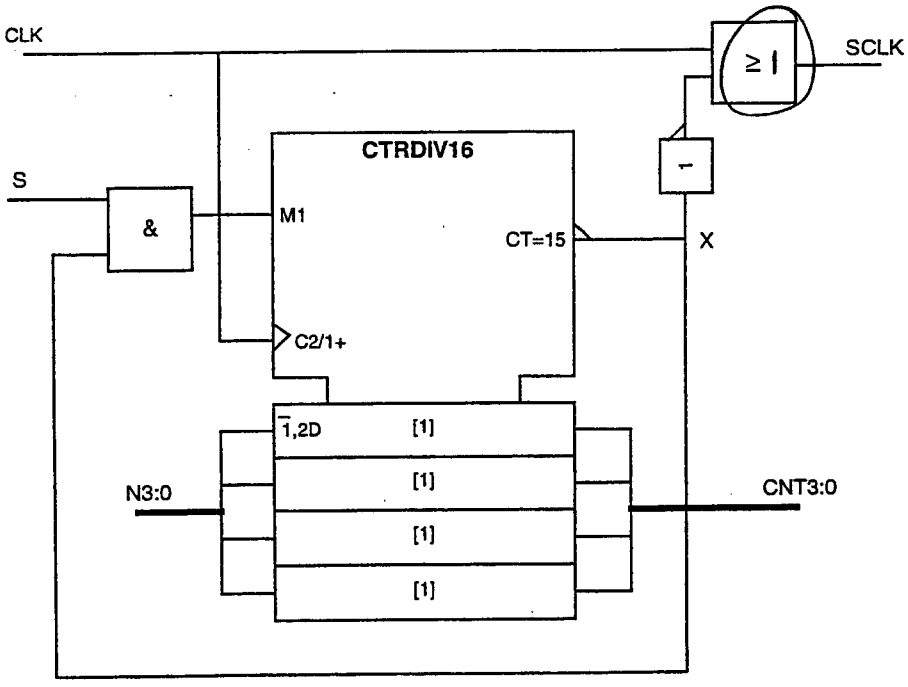

Figure 7.1

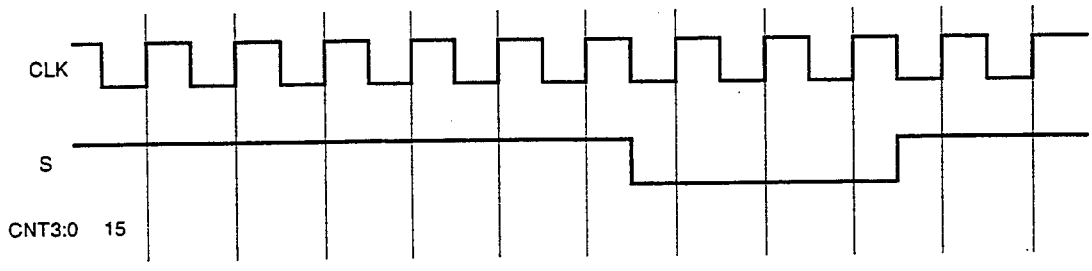

Figure 7.2

[END]

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M.Eng., B.Eng., B.Sc(Eng.) and A.C.G.I. EXAMINATIONS 2002

PART III and PART IV

DIGITAL SYSTEM DESIGN

SOLUTIONS

First Marker: *PYKC*

Second Marker: *DMB*

Answer to Question 1

(a) Step 1: scale all coefficient with a factor 0.125 to make them integers.

Coeff	Sign	Bit 3	Bit 2	Bit 0	Bit 1
a0	+	1	1	0	0
a1	+	0	0	1	1
a2	-	0	1	0	1
a3	+	0	0	1	1
a4	+	0	0	0	1
a5	-	0	0	0	1
a6	+	1	0	1	0
a7	-	0	0	0	1
a8	+	0	0	1	0

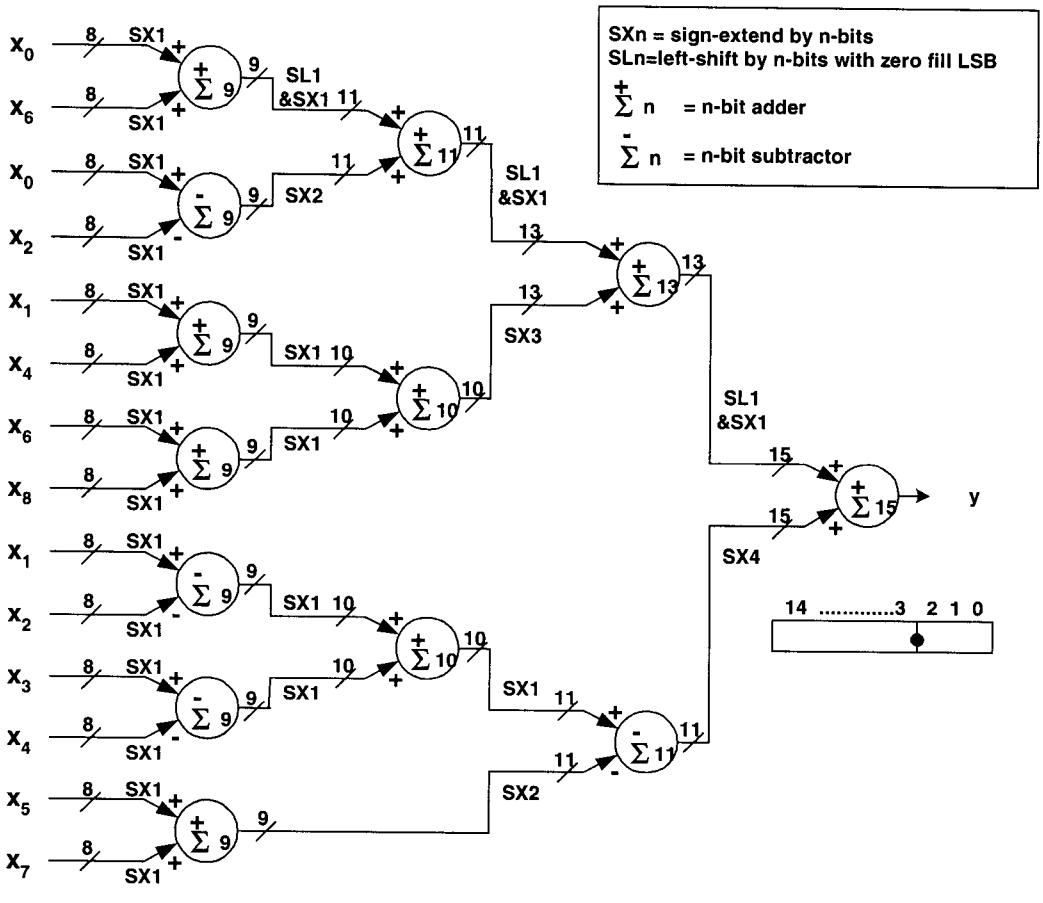
Step 2: From table, use distributed arithmetic, with MSB first, we can write

$$y = \{(x_0 + x_6)2^3 + (x_0 - x_2)2^2 + (x_1 + x_3 + x_6 + x_8)2 + (x_1 - x_2 + x_3 + x_4 - x_5 - x_7)\}0.125$$

Hence
$$y = \{\left[\left[(x_0 + x_6)\times 2 + (x_0 - x_2)\right]\times 2 + (x_1 + x_3 + x_6 + x_8)\right]\times 2 + (x_1 - x_2 + x_3 + x_4 - x_5 - x_7)\}\times 0.125$$

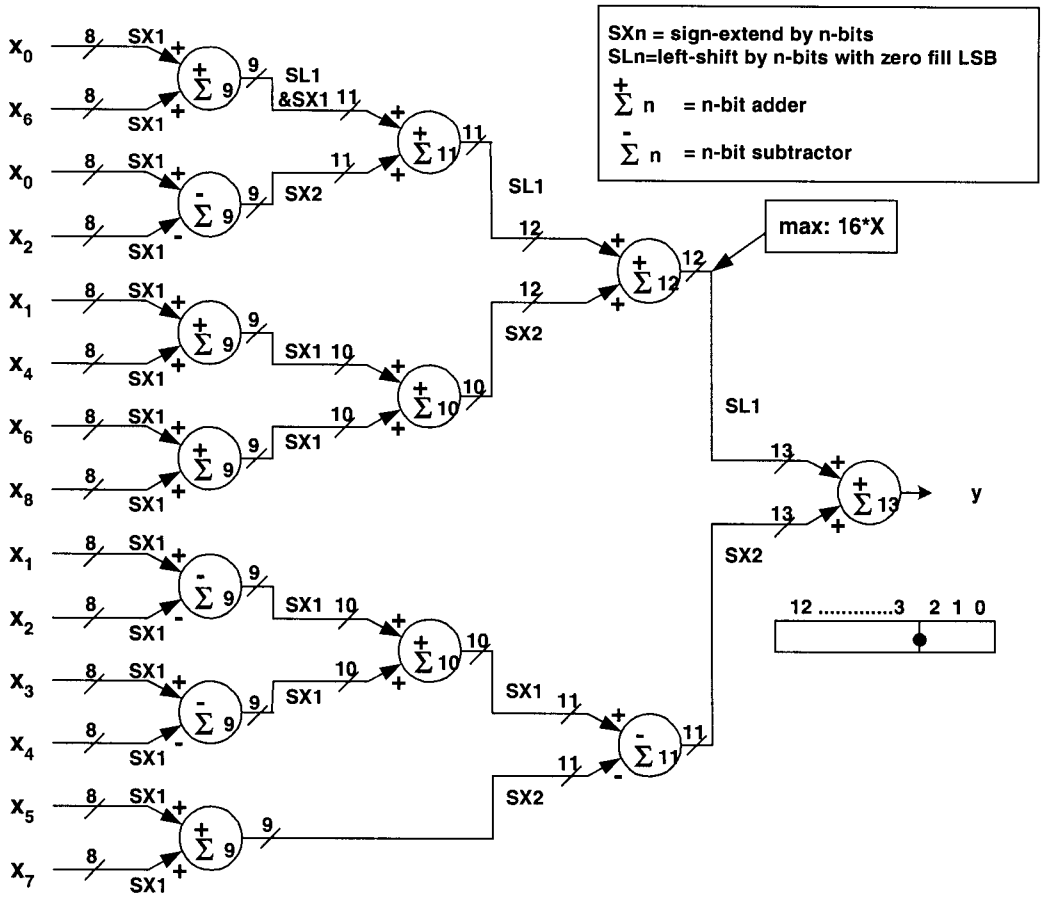
[6 marks]

(b) Considering only bit-width growth locally, the solution is:



[14 marks]

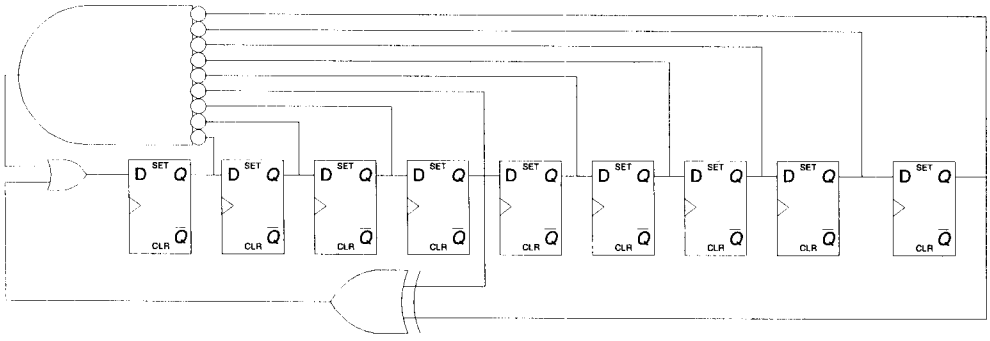
If we consider the size of data propogated from left to right and optimize the bit-width at each stage, the solution is slightly smaller:



Bonus marks for this optimal solution!

Answer to Question 2

(a)



PRBS sequence is taken from the D flip-flop Q output.

[6 marks]

(b) (i) N check bits can check $2^N - N - 1$ data bits. Therefore we need 3 check bits.

	0	1	2	3
p0	x	x		x
p1	x		x	x
p2		x	x	x

Therefore

p0 = d0 ⊕ d1 ⊕ d3
p1 = d0 ⊕ d2 ⊕ d3
p2 = d1 ⊕ d2 ⊕ d3

[4 marks]

(ii)

If a nibble digital of 1010 is read as 1000, d1 is wrong. Parity bit derived would be p0 p1 p2 = 111 instead of 010. We can conclude that p0 and p2 are wrong. With single bit error assumption, the only possible conclusion is that d1 is wrong. Therefore d1 can be corrected.

If the nibble digital of 1010 is read as 0000, then both d1 and d3 are wrong. Parity bit derived will be 000 instead of 010.

[5 marks]

(iii)

Assuming p0', p1' and p2' are the stored parity bits, d0' to d3' are stored data bits, and p0, p1 and p2 are the derived parity bits. Then:

The correct data bits are:
d0 = d0' ⊕ ((p0 ⊕ p0') • (p1 ⊕ p1') • !(p2 ⊕ p2'))
d1 = d1' ⊕ ((p0 ⊕ p0') • !(p1 ⊕ p1') • (p2 ⊕ p2'))
d2 = d2' ⊕ (!(p0 ⊕ p0') • (p1 ⊕ p1') • (p2 ⊕ p2'))
d3 = d3' ⊕ ((p0 ⊕ p0') • (p1 ⊕ p1') • (p2 ⊕ p2'))

[5 marks]

Answer to Question 3

a) Metastability can occur in any synchronous system interfacing to one or more asynchronous input. Since the input signal is not synchronised to the system clock, it may violate the setup or hold time of the synchronous system.

[3 marks]

b) Worst case delay contraint for this circuit is:

Clock -> Qbar(FF1) -> Q(FF3) -> setup of FF4.

Therefore:

Tmin = (5 + 5 + 3) ns = 13 ns, fmax = 76.92 MHz.

[5 marks]

c) Since the synchronizer is operating at half the clock frequency, or 38.46MHz, the available time for metastability to settle is (13 x 2 – 3) ns = 23 ns.

Therefore

MTBF (23ns) = $\exp(26/0.26) / (10^{-10} \times 38.46 \times 10^{6} \times 10^{7})$

$= 7 \times 10^{38}$ sec.

[8 marks]

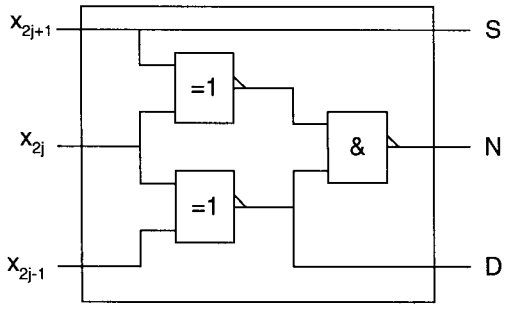
d) Replace the divide by two circuit with a divide by N circuit where N>2.

[4 marks]

Answer to Question 4

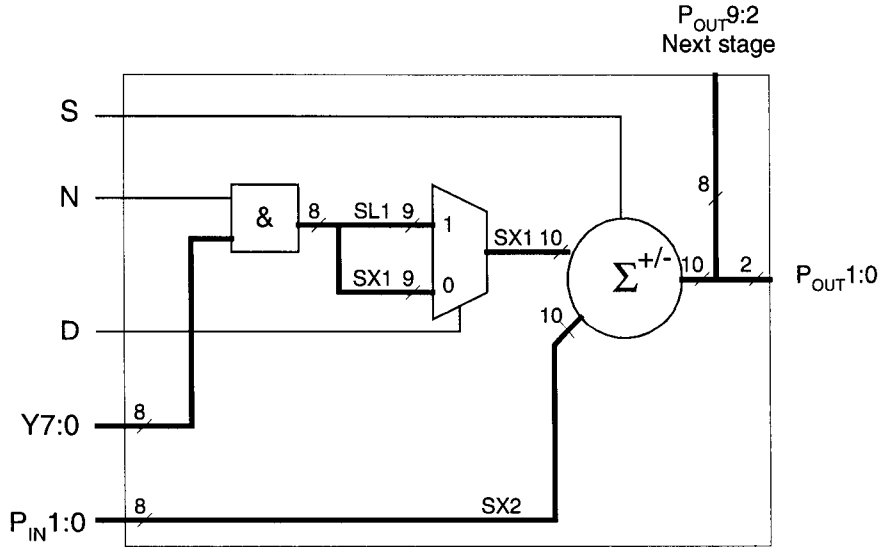
a)

$x_{2\,i+1}$	$x_{2\,i}$	$x_{2\,i-1}$	D	N	S	Action
0	0	0	0	0	0	0
0	0	1	0	1	0	y
0	1	0	0	1	0	y
0	1	1	1	1	0	2y
1	0	0	1	1	1	-2y
1	0	1	0	1	1	-y
1	1	0	0	1	1	-y
1	1	1	0	0	0	0



[4 marks]

b)



p=8, q=10, r=2.

[12 marks]

c)

X -> N delay in BE = 2 ns.

Delay in PP, N to Pout = 22 ns; Therefore, X -> Pout delay = 24 ns.

Delay in PP, Pin to Pout = 20 ns.

Worst case delay from x0 to Pout = 24 + 20 + 20 + 20 = 84 ns.

[2 marks]

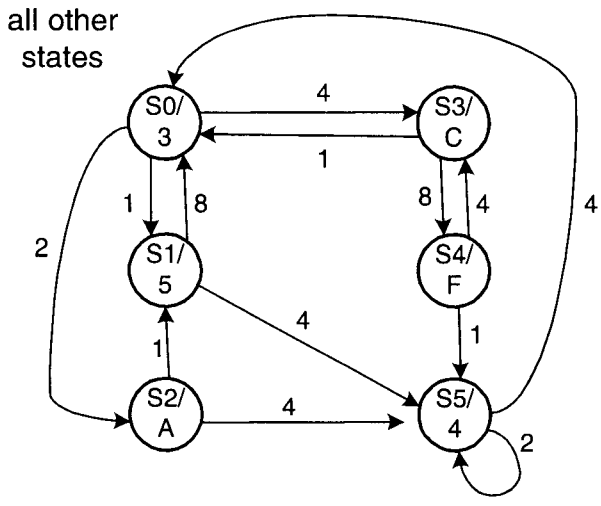
d) Assumption: register at input and output of multiplier.

Pipeline register inserted between stages, must include setup and clk-> output delay time, then tmin (pipelined) = 24 + 1 + 1= 26 ns, fmax(pipelined) = 38.46MHz.

[2 marks]

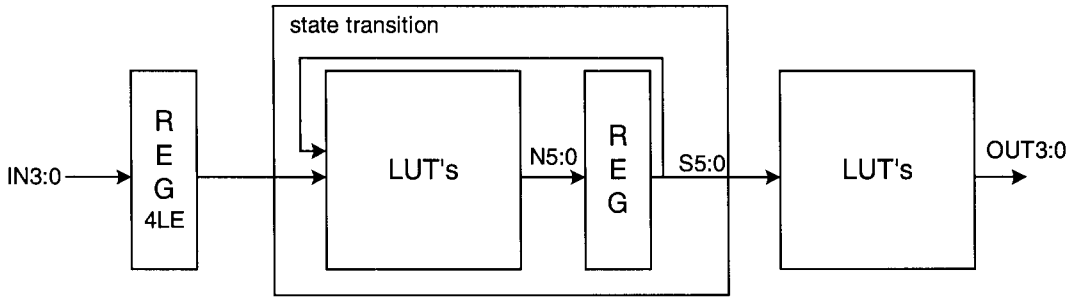
Answer to Question 5

(a)



[8 marks]

(b)



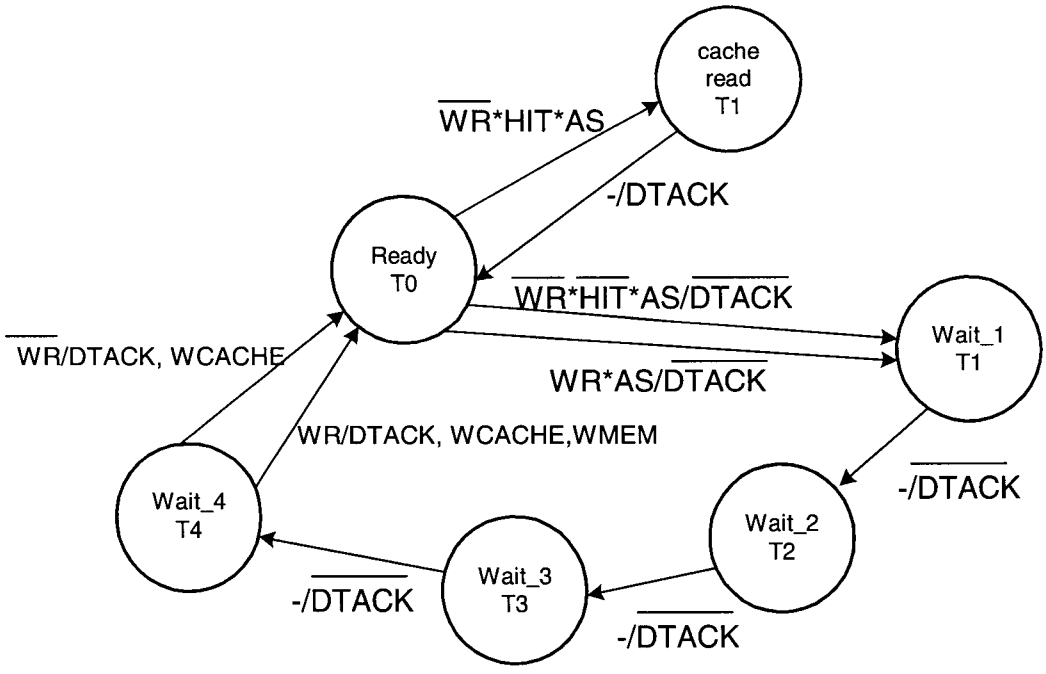
6 states, therefore 6 FF for one-hot encoding, each representing one state. Note that the inputs are also one-hot!

N0 = S1*IN3 + S5*IN1
N1 = S0*IN0 + S2*IN0 + S3*IN0
N2 = S0*IN1
N3 = S0*IN2 + S4*IN2
N4 = S3*IN3
N5 = S1*IN2 + S2*IN2 + S4*IN0 + S5*IN0
OUT0 = S0 + S1 + S4
OUT1 = S0 + S2 + S4
OUT2 = S1 + S3 + S4 + S5
OUT3 = S2 + S3 + S4

All except N5 requires only 1 LE. Therefore no of LE used = 11 + 4 (i/p reg) = 15 LEs.

[12 marks]

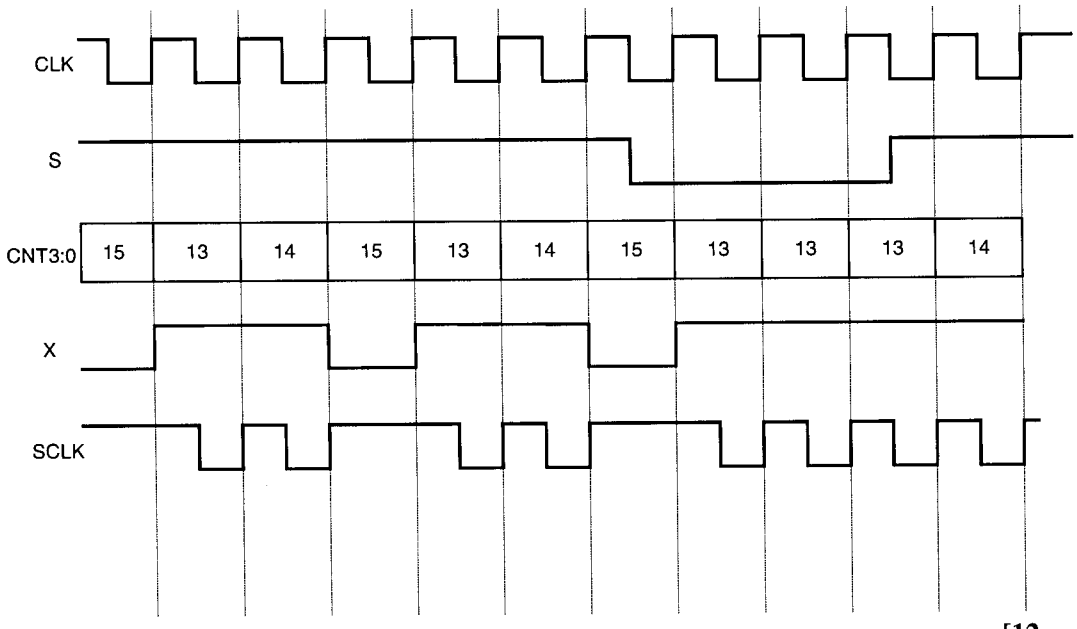
Answer to Question 6



Answer to Question 7

This is a swallow counter that "swallows" some clock pulses if S is high.

(a)



[12 marks]

(b) f(sclk) = fc *(15-N)/(16-N).

[8 marks]