ANALOG

EJ.01 / AC1

EXAM 2008 - SOLUTIONS

Q1/ Bandgap voltage reference circuit has almost zero temperature coefficient. Used many as stable voltage reference in ICs. 2

PTAT (Proportional to absolute temperature) current generator. Output current virtually insensitive to power supply voltage. Used as a biasing circuit in most precision ICs. 2

For BG reference :- $V_{BE1} = V_{BE2} + I_2 R_3$ $(\beta \gg 1)$

Since $V_{BE1} - V_{BE2} = V_T \ln (I_1/I_2)$

then $V_o = V_{BE3} + (R_2/R_3) V_T \ln (I_1/I_2)$

$V_T \ln [I_3/I_s]$ → assume room temp.

for $dv_o/dt = 0$, then $dV_{BE3}/dT = \frac{V_T}{T}\frac{R_2}{R_3}\ln\frac{I_1}{I_2}$

Since $\frac{dV_{BE}}{dt} = -2.5\,mV/°C$, $\frac{V_T}{T} = \frac{1.38\times10^{-23}}{1.6\times10^{-19}}$

then $\left(\frac{R_2}{R_3}\right)\ln\left(\frac{I_1}{I_2}\right) = 29$ and so

$$V_o = 1.283\,V$$

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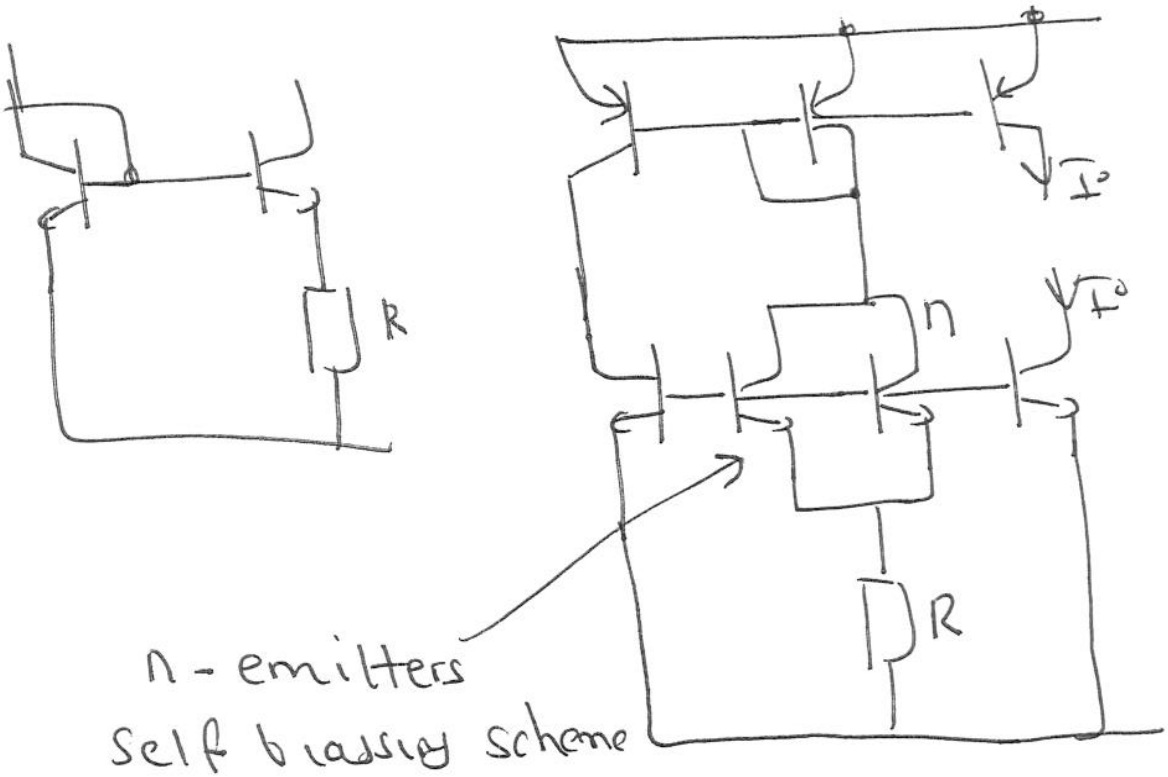
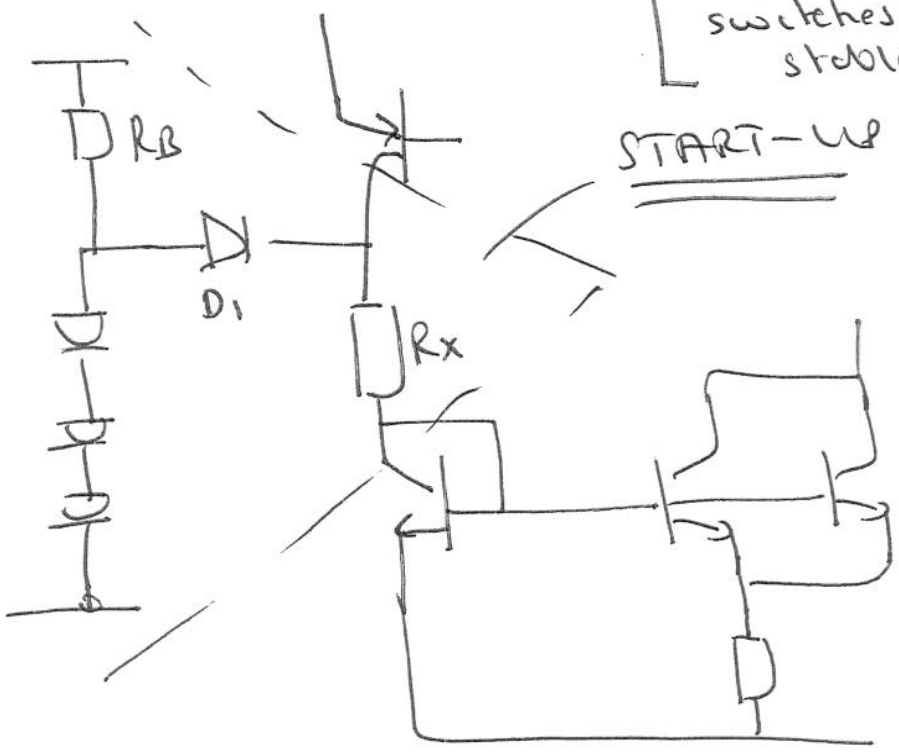
Question 1 continued.



n - emitters
Self biassing scheme
requires start up.

$$I_O = \frac{V_T}{R} \ln [n]$$

[D_1 - conducts on start-up switches off in stable-state]



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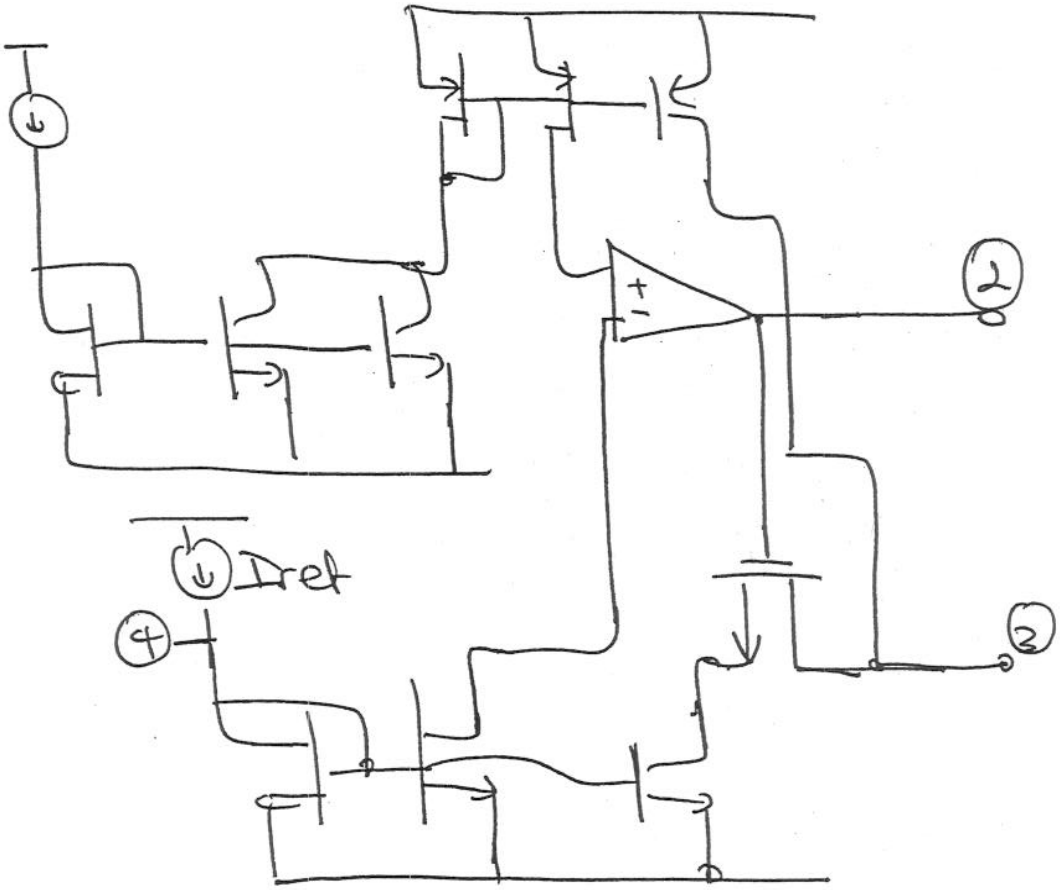
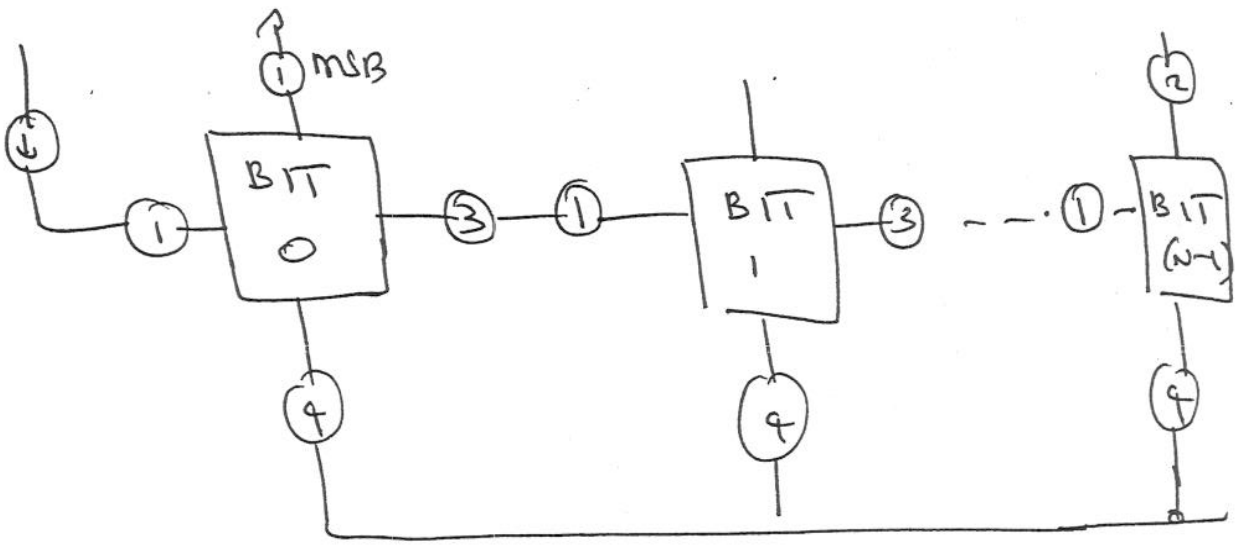
Question 2

Algorithmic Converter 1 Bit



(2)



BASIC ARCHITECTURE

(2)

(3)

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Question 2 – Continued

If $2I_{IN} < I_{ref}$

Comp goes low, digital output = 0 and analogue output $2I_{IN}$.

If $2I_{IN} > I_{ref}$, comp output goes high, digital = 1

Analogue output $(2I_{IN} - I_{ref})$

Analogue output feeds into following bit which performs exactly the same function. The process is repeated on many times as necessary to achieve the desired resolution. (6)

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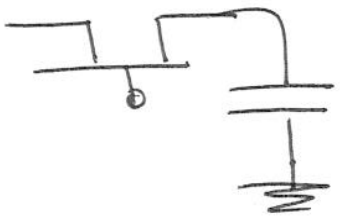
Last part

$DR \triangleq V_{refl}/Noise = 2^N$



RMS noise of switch capacitor

$\sqrt{\frac{kT}{C}}$

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Assume $f_c = \frac{1}{10 \cdot R \cdot C}$, then

Solving for C gives

$$DR = 2^N = V_{rell} / \sqrt{kT\ 10 \cdot R \cdot F_c}$$

$$R_{on} = \frac{1}{2\beta(V_{gs} - V_T)} \approx \frac{1}{(2\beta \times 4)}$$

$$\beta = \left(\frac{kW}{2L}\right)$$

Can now find DR @ 40kHz.

(10)

Question 3

(a) Floating integrated RC integrator.

Double mos differential

$$R = \frac{V_{IN} - (-V_{IN})}{(I_1 - I_2)} = \frac{1}{2\beta(V_{C1} - V_{C2})} \Rightarrow \text{Expected answer.}$$

$$\tau \approx RC = \frac{C}{2\beta(V_{C1} - V_{C2})} \quad -(8) \quad (6)$$

(b) Differential, parasitic insensitive SC integrator. During one switch phase C_1 charges to $(V_1 - V_2)$ such that $I_{C1} = 1/T(V_1 - V_2)C$ or $f_c C_1 (V_1 - V_2)$ where f_c = clock frequency.

During the 2nd clock phase

$$I_{C1} = I_{C2} = j\omega C_2 V_o$$

$$\therefore V_o = \frac{C_1}{C_2}\left[\frac{f_c}{j\omega}\right](V_1 - V_2)$$

Assumes $f_c \gg 2\pi/\omega$

$$\tau = \left[\frac{C_2}{C_1 f_c}\right] \longrightarrow (2) \quad (6)$$

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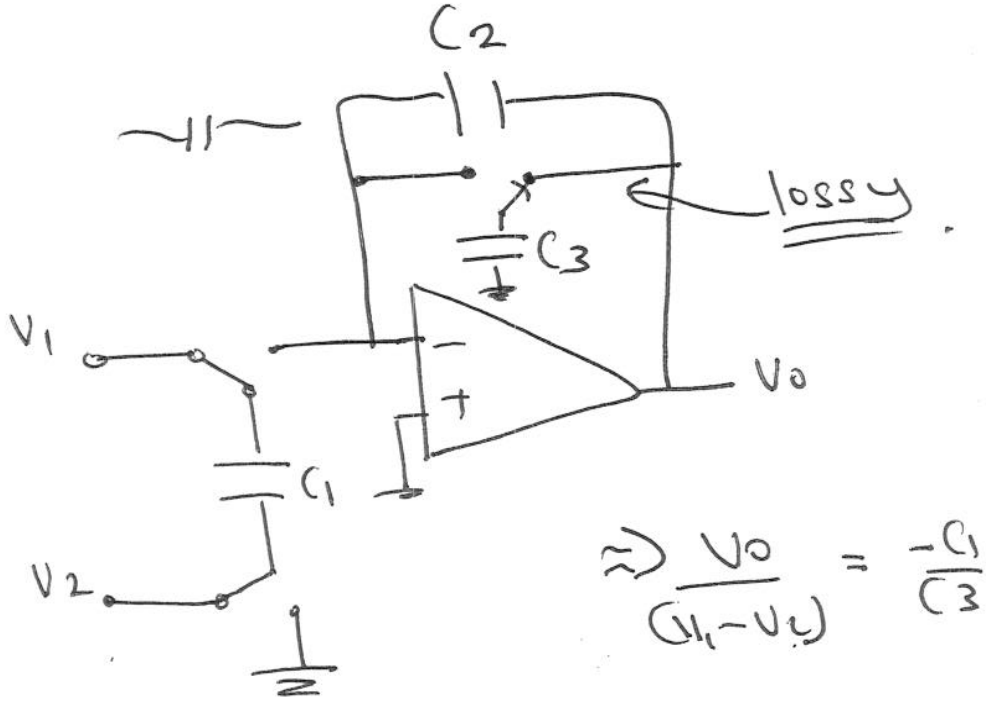
Question 3 – continued.

Continuous-time → Fast
→ potential low power.
→ inaccurate / need tuning

Switched-cap → Accurate
→ low frequency
→ higher power
→ precision (cap ratios)

(4)



$$\Rightarrow \frac{V_0}{(V_1 - V_2)} = \frac{-C_1}{C_3}\left[\frac{1}{(1 + j\omega\frac{C_2}{C_3}T}\right]$$

(4)

Q4. 8

a) Bandgap reference. Output voltage reference independent of temperature.
Assumes $V_{BE} \simeq -2.5mV/°C$
And thus $\beta >> 1$

$$V_{BE3} - V_{BE2} = V_{TH}(I_1/I_2) = I_2 R_1$$

Thus $V_o = V_{BE3} + (R_2/R_3)(V_T) \ln I_1/I_2$

For $dv_o/dt = 0$, then $(R_2/R_3) \ln I_1/I_2$ (2)
$\simeq 24.5$, $V_o = 1.283V$

b) V_{gs} multiplier. Can replace stacked diodes with a single resistor for biasing purposes.

$$V_o \simeq V_{GS}[1 + R_2/R_1]$$

$$\simeq (1 + R_2/R_1)[V_T + \sqrt{I_D/\beta}]$$ (2)

c) PTAT (proportional to absolute temperature) constant current source/sink. The output current is virtually independent of the power supply voltages. Diode chain R_3 and R_1 form automatic start-up circuitry ensures circuit behaves in correct output state. (2)

Analysis – Assuming matched devices $\beta >> 1$,
then $I_O = \Delta V_{BE}/R = [V_T \ln(I_N/I_O)(I_{S3}/I_{S1})/R$
$(I_{S3} = 2I_{S1})$ then $I_O = (V_T \ln 2) R$. (2)

Question 4 – continued.

Fig 4d →

Regulated Cascode current sink, since drain–source voltage of Q_1 is regulated by the feedback amplifier Q_2 the circuit has a very high output impedance equivalent to that of a double cascode.

Analysis, $I_O = \beta (V_a - V_T)^2$

assume FET Q_1 is saturated (2)

b) $I_O = (V_T \ln 2)/R$

assuming $V_T = 25\,mV$ at $300°k$

then $R = 3.465\,k\Omega$.

$$T_{CF} = \frac{1}{V_T}\frac{\partial V_T}{\partial T} - \frac{1}{R}\frac{\partial R}{\partial T}$$

$$= \frac{1}{T} - \left(\frac{1}{R}\frac{\partial R}{\partial T}\right)$$

$$= (1/300) - 1500 \times 10^{-6}$$

$$= \underline{1833\ ppm/°C} \quad (4)$$

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Question 4 - continued.

Rout of $(Q_3 \rightarrow Q_1)$ cascode

$R_{out} = (g_{m3} r_{o3} r_{o1})$

with regulated gate of Q_3

$R_{out} = (g_{m3} r_{o3} r_{o1}) g_{m2} r_{o2}$

$\Rightarrow$ assuming $I_{B(ro)} \approx 0$

if $g_{m3} = g_{m2} = g_m$, $r_o = r_{o3} = r_{o1} = r_{o2}$ $\rightarrow R_{out} = g_m^2 r_o^3$ (5)

If gate Q_3 set to a d.c level then local feedback to regulate gate. Node x will swing with output current and so I_o will change. Regulating gate of Q_3 ensures that $V_{node}(x)$ is reduced by local loop gain $A_2 \approx g_{m2} r_{o2}$ (3)

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6/

Advantages of Current-mode

- Higher frequency performance, wider dynamic range
- lower power supply voltage

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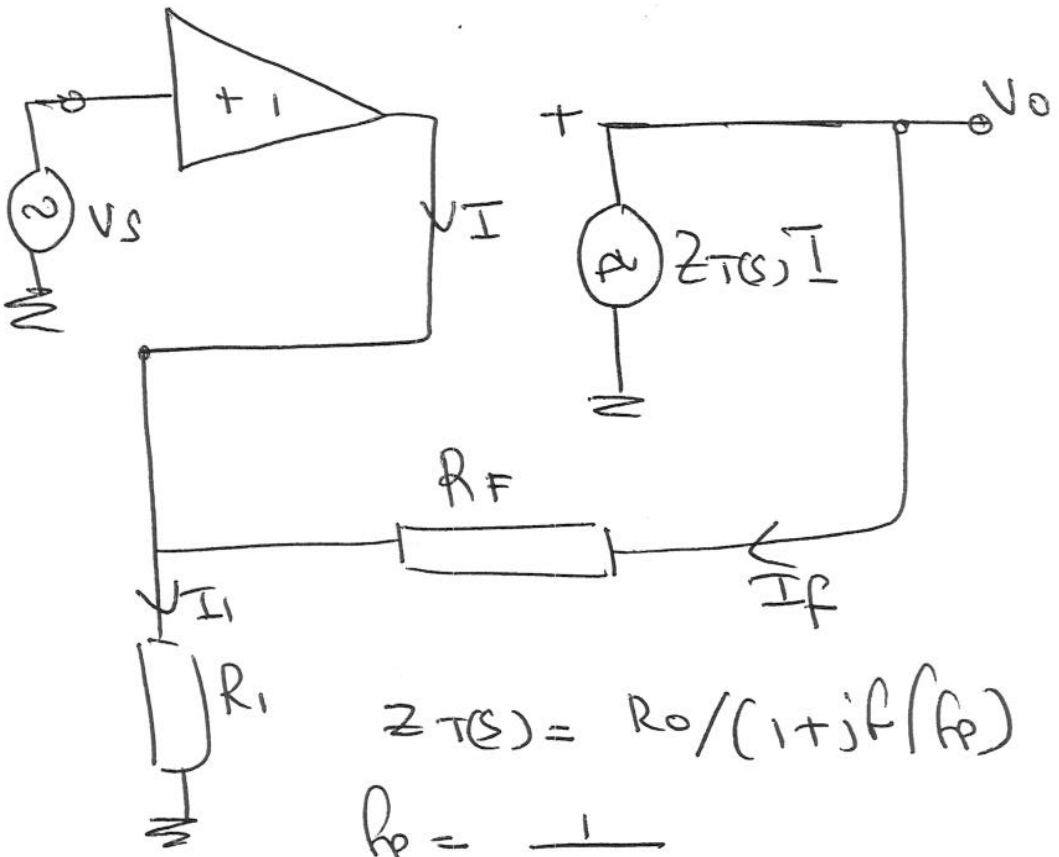

$$Z_{T(s)} = R_o/(1+jf/f_p)$$

$$f_p = \frac{1}{2\pi R_o C}$$

C = compensation capacitor

3 equations

$$I_f = (V_o - V_s)R_F \quad - (1)$$

$$I_1 = V_s/R_1 \quad - (2)$$

$$V_o = Z_{T(s)}\,I = Z_{T(s)}\left[I_1 - I_f\right] - (3)$$

8

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CT

Subs ① and ② into ③ gives,

$$(V_o/V_s) = (1+R_F/R_1)\, Z_{T(s)}/(R_F + Z_{T(s)})$$

Subs for $Z_{T(s)}$

$$(V_o/V_s)_{cw} = \underbrace{(1+R_F/R_1)\left[\frac{R_o}{R_o+R_F}\right]}_{\text{gain}} \times \frac{1}{\left(1+jf/\underbrace{f_p\left[\frac{R_o+R_F}{R_F}\right]}_{BW}\right)}$$

Assuming $R_o \gg R_F$

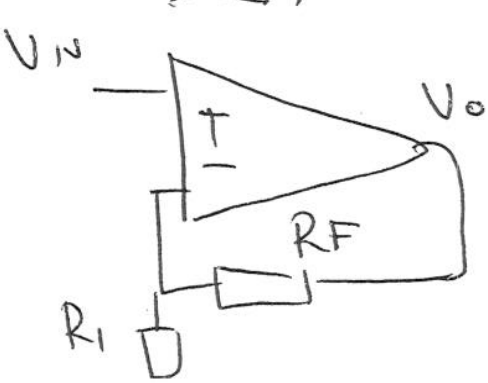
then

Closed loop gain $\simeq (1+R_F/R_1)$ — *

Closed loop Bandwidth $\simeq \frac{f_p R_o}{R_F} = \frac{1}{2\pi R_F C}$

L*.

Hence R_F sets the amplifiers constant BW and R_1 chosen to set the gain



$BW = \frac{1}{2\pi R_F C} = 10\text{MHz}$

$\therefore$ Given $C = 4pF$

$R_F = 3.98\,k\Omega$

Since $A = (1+R_F/R_1) = 100$

$R_1 = 40.2\,\Omega$

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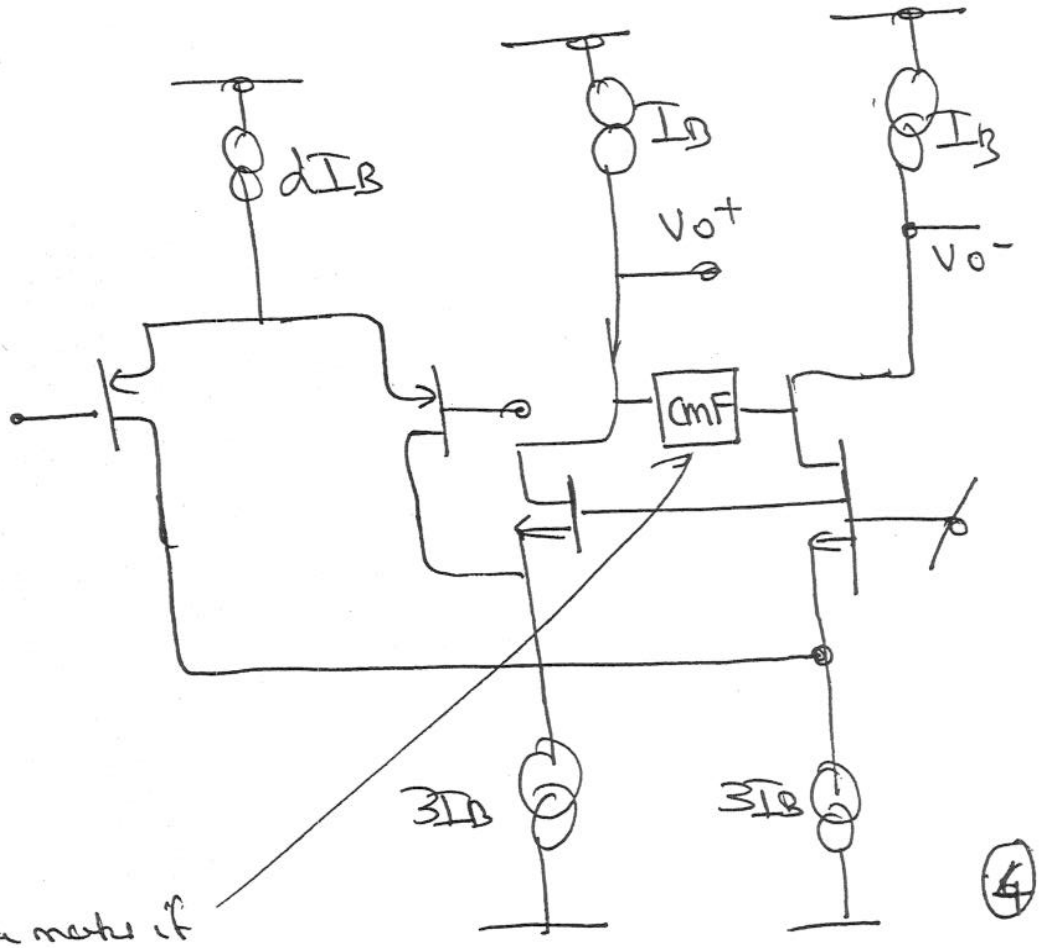
Question 6

a)

Main advantage is that signal path is folded giving a balance between input and output allowing supply voltage to be reduced. (2)



(4)

Extra marks if CmF circuit connected.

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Question 6 – cont

6) Sole stage

Advantage :- High speed
Good phase margin

Disadvantage :- lower gain
lower CMRR/output swing.

(3)

OP-AMP 3(b)

Volt gain = $-g_{m2} / (g_{02} + g_{04})$

$(g_{02} + g_{04}) = I_{D2} (\lambda_N + \lambda_P) =$

$5 \times 10^{-6} \times 0.05 = 2.5 \times 10^{-7} s$

$g_{m2} = \sqrt{2 \beta_2 I_{D2}} \Rightarrow \beta_2 = \frac{K_N}{2} \left(\frac{W}{L}\right)_2 = 7.5 \times 10^{-5}$

$g_{m2} = 3.87 \times 10^{-5} s$

$A_1 = -154.9$

$(g_{07} + g_{06}) = I_{D6} (\lambda_N + \lambda_P)$

$= 20 \times 10^{-6} \times 0.05$

$= 10 \times 10^{-7} \mu^{-1}$

$g_{m6} = \sqrt{2 \beta_1 I_{D6}} \Rightarrow \beta_6 = \frac{K_P}{2} \left(\frac{W}{L}\right)_6$

$= 1.6 \times 10^{-4} A/V$

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Question 6(b) continued.

$$\Rightarrow g_{m6} = 1.13 \times 10^{-4}$$

$$A_2 = -113 \quad (7)$$

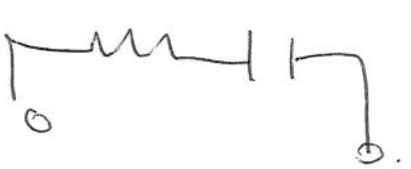
$$A_{TOTAL} = A_1 A_2 = 17503$$

$$G.B_P = \frac{g_{m2}}{2\pi C_C} = 4.1\,MHz \quad (2)$$

Yi—

last Part.

Introduce R



Improved phase Margin

Feedforward compensation eliminates RHP zero.

Zero given by $Z = -g_{m6}/C_C$

with R $\Rightarrow Z = -1/(1/g_{m6} - R)$ (3)

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