

UNIVERSITY OF LONDON  
IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2001

BEng Honours Degree in Computing Part II  
MEng Honours Degrees in Computing Part II  
for Internal Students of the Imperial College of Science, Technology and Medicine

*This paper is also taken for the relevant examinations for the  
Associateship of the City and Guilds of London Institute*

PAPER C210

ARCHITECTURE II

Monday 30 April 2001, 14:00

Duration: 90 minutes  
(Reading time 5 minutes)

*Answer THREE questions*

Paper contains 4 questions  
Calculators required

- 1a What does CPI stand for? Explain whether the CPI for a processor can be affected by the compiler, the instruction set architecture, and the implementation technology for that processor.
- b A subset of the instructions for a machine  $M$  can be accelerated by  $n_1$  times using a coprocessor  $C_1$ . Given that a program  $P$  is compiled into instructions of  $M$  such that the overall speedup is  $K_1$ , calculate  $\alpha_1$ , the fraction of instructions that belongs to the subset which can be accelerated by  $C_1$ .
- c For the system containing  $M$  and  $C_1$  described in part b, express  $\beta_1$ , the ratio of the time for  $C_1$  to process instructions amenable to its acceleration and the overall execution time of the system, in terms of  $\alpha_1$  and  $n_1$ .
- d Another subset of the instructions for the machine  $M$  in part b, which does not overlap with the instruction subset for  $C_1$ , can be accelerated by  $n_2$  times using a coprocessor  $C_2$ . Given that  $P$  is compiled into instructions of  $M$ , such that a fraction  $\alpha_1$  of the instructions is accelerated by  $C_1$  and a fraction  $\alpha_2$  of the instructions is accelerated by  $C_2$ . What is the overall speedup that can be achieved using  $C_1$  and  $C_2$ ?

*The four parts carry, respectively, 30%, 25%, 25% and 20% of the marks.*

- 2 This question concerns regular combinational circuits formed by replicating a simple unit. For each of the four parts below, provide a circuit diagram and label one of the replicating units using a dotted box.
- a Design a circuit for multiplying an N-bit number by 3, using only N fulladders. Label the signal value on all the wires in your circuit when  $N=4$  and the input is 0100.
  - b Design a circuit, using and-gates, or-gates and inverters, that will produce a one at the output when all the input bits are the same. Provide a diagram for the case when the input is 0000.
  - c Leading zeroes of a multi-bit number are zeroes in a more significant position than the most significant one; for instance there are two leading zeroes in 001XXX, and three leading zeroes in 0001XX, where X is either a zero or a one.

Design a circuit, using inverters, and-gates and halfadders, that counts the number of leading zeroes in an N-bit number. Provide a diagram for the case when  $N=5$ , the input is 00101 and the output is 010.

*The three parts carry, respectively, 25%, 25% and 50% of the marks.*

- 3a Provide an advantage and a disadvantage for datapaths supporting
- i) horizontal microinstructions, and
  - ii) vertical microinstructions.
- b A datapath containing  $m$  control signals has been developed for a set of instructions with an  $n$ -bit opcode. A microsequencer, which supports  $k$ -bit horizontal microinstructions, has been developed for this datapath. The microsequencer contains an incrementer, a ROM (Read-Only Memory), a register, and address select logic. Provide a diagram for the microsequencer, and label the size of components and wires in the diagram whenever possible.
- c Describe how the address select logic in part b can be implemented using ROMs and multiplexors. Explain how the number of ROMs in the address select logic relates to the state diagram for the control unit.
- d The microprogram for a microsequencer has  $n$   $\ell$ -bit microinstructions, some of which are identical. Given that there are  $k$  distinct microinstructions in this microprogram, explain how the total microprogram storage can be reduced by reducing the width of the microinstructions, while including an additional store of the  $k$  distinct microinstructions. Calculate the value of  $\ell$  to achieve a reduction of  $\alpha$  bits in microprogram storage using this approach, and comment on possible disadvantages.

*The four parts carry, respectively, 20%, 25%, 20% and 35% of the marks.*

- 4a Give one advantage and one disadvantage of
- i) a direct-mapped cache, and
  - ii) a fully-associative cache.
- b Explain what an  $n$ -way set-associative cache is, and indicate the effect of increasing  $n$  on the size and speed of the cache.
- c Calculate the total number of tag bits when implementing a cache, containing  $2^n$  blocks and dealing with  $m$ -bit addresses, as:
- i) a direct-mapped cache,
  - ii) a  $2^k$ -way set-associative cache, and
  - iii) a fully-associative cache.
- d Explain what TLB stands for, and how associative caches improve the performance of TLBs.

*The four parts carry, respectively, 20%, 30%, 30% and 20% of the marks.*