Section A

1.

(a) For the two sets of three-phase voltages shown below, v_k and v_l, describe how the voltages would appear once transformed into $DQ\gamma$ form. [4]

$$v_k = \begin{bmatrix} 300\cos(\omega t + 15°) \\ 300\cos(\omega t + 135°) \\ 300\cos(\omega t - 105°) \end{bmatrix} \qquad v_l = \begin{bmatrix} 25 + 25\cos(\omega t - 90°) \\ 25 + 25\cos(\omega t + 150°) \\ 25 + 25\cos(\omega t + 30°) \end{bmatrix}$$

[Calculation examples – 2 marks each]
v_k has three terms of the same amplitude and phase differences of 120° and an overall phase angle for the set of 15°. There is no zero-sequence term and therefore no γ-axis term. The sequence set is negative, thus, there when transformed to DQ it will appear as a double frequency term.

v_l contains a 25V DC signal that is common to all phases. It is common mode and appear in the γ-axis. It also contains a balanced positive sequence set of 25V magnitude and phase offset of 90°. This will appear as a constant term on the D and Q axes and because of the 90° offset appears a 25V on the Q-axis and 0 on the D-axis.

(b) Figure 1.1 shows a three-phase low-pass filter. Figure 1.2 shows the same filter transformed to the equivalent $DQ\gamma$ form. Justify the format of the transformed filter. [8]

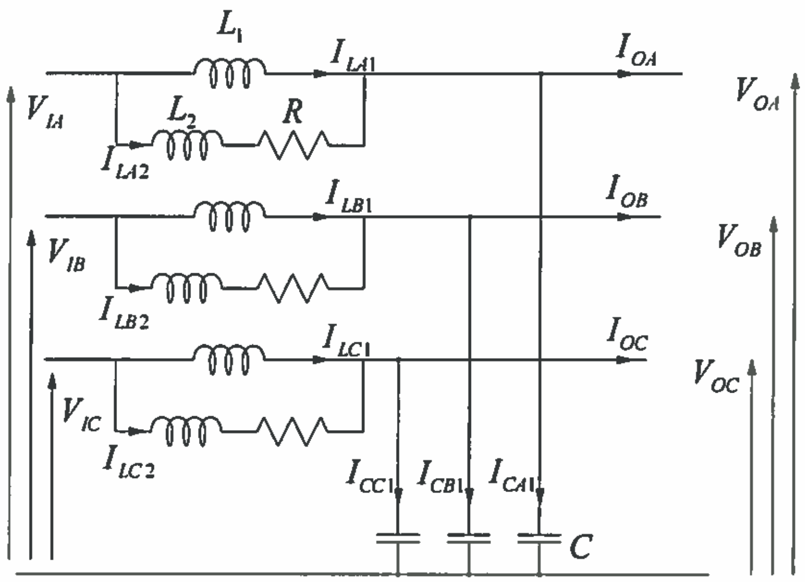


Figure 1.1 A three-phase low-pass filter,

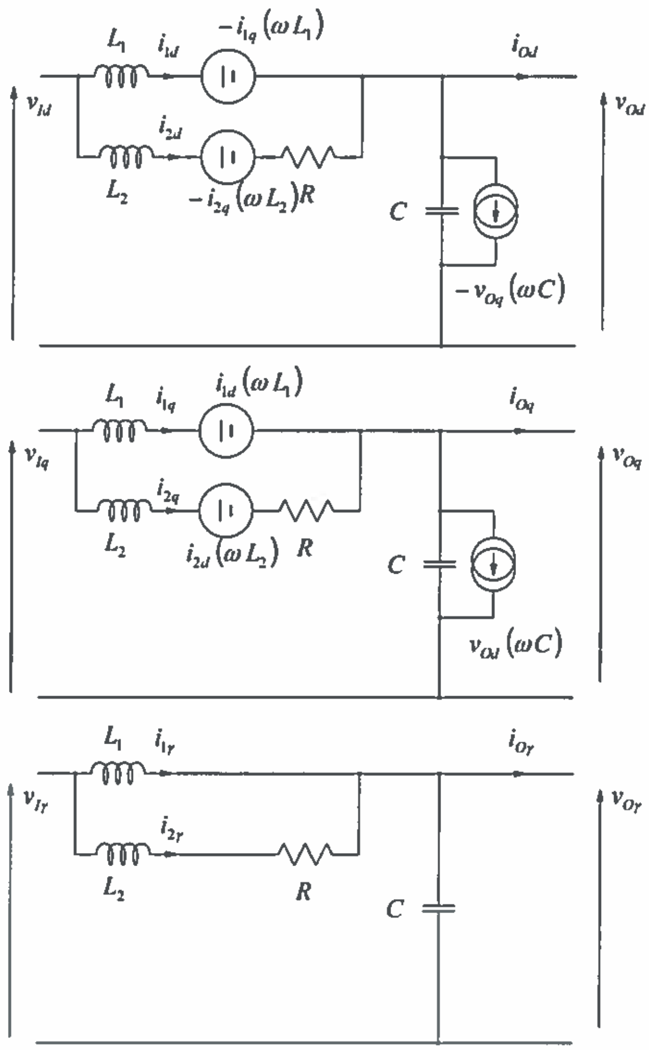


Figure 1.2 *DQγ* representation of filter in Figure 1.1

[Interpretation of example using bookwork]

The DQγ transformation creates equivalent circuits with the following features

- Each axis of the transformed circuit is a separate circuit (they are orthogonal and the power flow associated with the variables in each axis can be calculated independently for each axis. Fig .12 shows three separate circuits. [2 marks]
- The γ-axis gathers the common-mode (zero-sequence) components. The original filter is a 4-wire design with a path between the phase and neutral thus paths for current flow appear in the γ-axis circuit also – this filter will act on the zero-sequence terms. [2 marks]
- Each reactive component is governed by a differential equation. The DQγ transform converters the steady sinusoidal terms to DC terms. The differential of the sinusoidal variation is now shown as a controlled source. For instance, the inductor is now represented by an inductor that has a voltage drop proportional to the change in amplitude of the current and a steady voltage drop represented by the series connected voltage source that arises from the original sinusoidal variation of the instantaneous signal. Because the inductive voltage drop is 90° leading on the current, the steady voltage in the D-axis is made proportional to the Q-axis current. Similarly, the capacitors have controlled current sources (controlled by voltage in the other axis) representing

the steady-current flow through the capacitor under sinusoidal voltage excitation. [4 marks]

(c) Consider the system shown in Figure 1.3. It is composed of a power source (in this case a PV panel followed by a DC/DC converter), a DC-link capacitor, a DC/AC converter, interface inductors, a 3-phase grid, a current controller and a high-level controller.

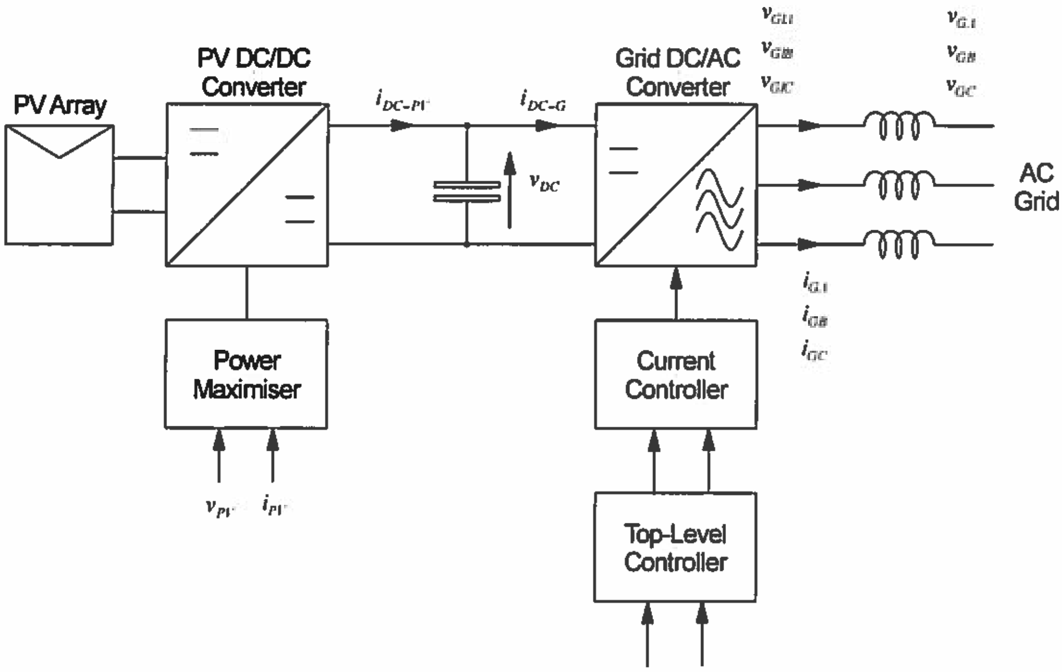


Figure 1.3 Schematic diagram of the current controller for a three-phase inverter.

(i) Figure 1.4 shows the control system to be used for current controller of figure 1.3 which acts on the PWM signals of the DC/AC converter. Explain the purpose of each block in figure 1.4. [5]

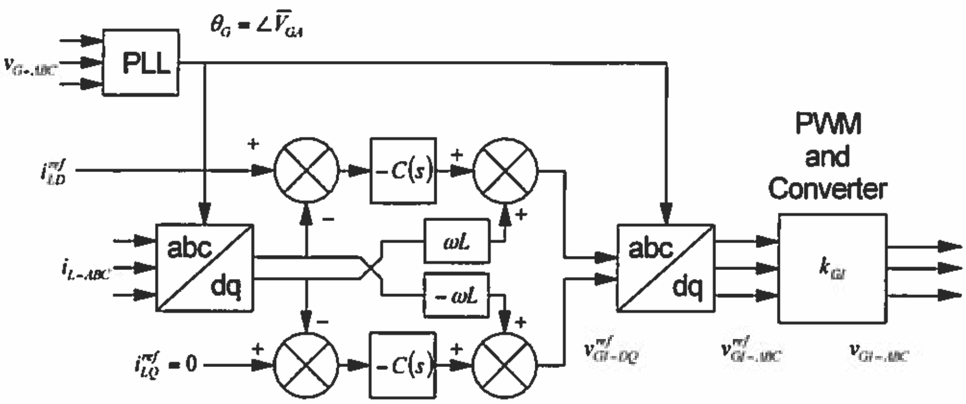


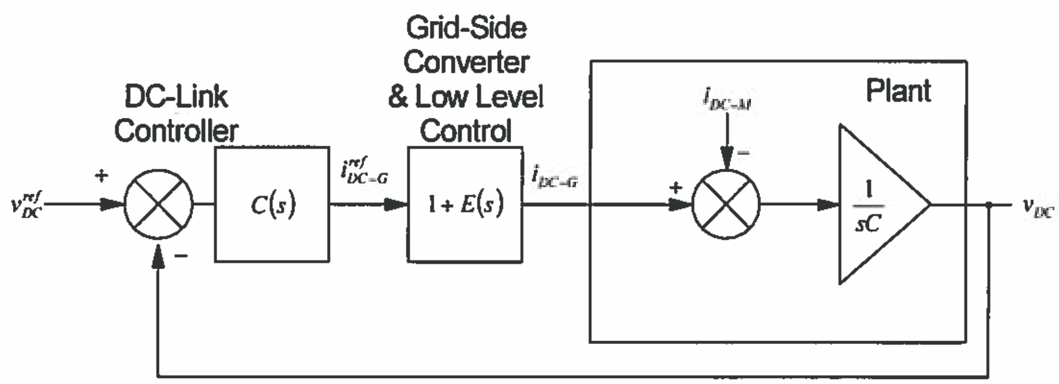
Figure 1.4 Schematic diagram of the current controller for a three-phase inverter.

[Interpretation of example using bookwork]
The blocks are:

- PLL – phase-locked-loop –this identifies the instantaneous phase angle of the grid voltage and is used as the rotation angle for the converting between the ABC and DQ0 frames of reference. [1 mark]
- Input variables to the control (feedback from the circuit) and output variable (control inputs to the inverter) are converted too and from the DQ0 reference frame in order to design and implement controller in that frame. [1 mark]
- Difference blocks and control gain– the first stage of the controller is the subtraction of the feedback currents from the references for D and Q axes to form error terms that are multiplied by gain functions. [1 mark]
- The control signals (processed errors) have feed-forward terms added before being applied to the plant. These terms add the (estimated) voltage that will be dropped in one axis due to the current flow in the other. By feeding forward these cross-coupling terms, (most) of the disturbance in one axis from perturbations in the other is cancelled with out the need for the feedback controllers to respond. [2 mark]

(ii) **Sketch and describe the format of the top-level controller that sets current references for the controller of figure 1.3 in order to export the power from the source.** **[3]**

[Bookwork]
The task is to export all of the power created by the source minus any losses. Any error in this task will lead to a rise of fall in the voltage across the DC-link and this can be exploited as the basis for the control design. The DC-link voltage is measured and compared to a reference value and the error used to drive the exported power to the correct value. The exported power can be expressed in terms of a current magnitude since the AC-grid voltage is essentially constant. This forms the D-axis reference current for the current controller. The Q-axis current can be set to zero or possibly used for reactive power support of the grid.



2.

(a) Figure 2 illustrates an Voltage Source Converter (VSC) connected to a 350 kV (line-to-line) AC grid at 50 Hz and a DC network at ±330 kV.

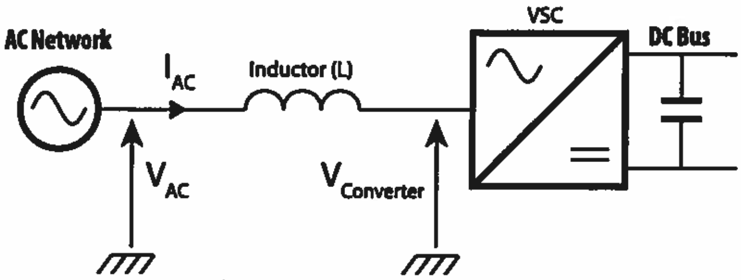


Figure 1 - VSC schematic

Consider the converter inverting 600 MW (power going from DC to AC) and generating 200 MVAr of capacitive reactive power (at the AC connection point).

(i) Compute the magnitude and angle of the AC current. [1]

$$I = \frac{S^*}{\sqrt{3}\,V_{line}} = \frac{(-600 - j200)\times 10^3}{\sqrt{3}\ 350\times 10^3} = 1.04\ kA_{RMS}\ and\ 161.6°$$

(ii) Assuming that the phase reactors are 190 mH, calculate the magnitude and angle of the converter voltage. [1]

$$V_{converter} = V_{AC} - j\omega L\, I = 229.5\ kV_{RMS}\ and\ 14.9°$$

(iii) What is the modulation index at which the VSC running? [1]

$$k = \frac{\hat{V}_{converter}}{V_{DC_{terminal}}} = \frac{\sqrt{2}\times 229.5\ kV}{330\ kV} = 98.35\ \%$$

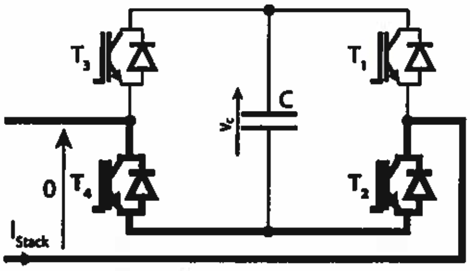
(b) The cells of a Modular Multi-Level Converter (MMC) can be implemented in several ways.

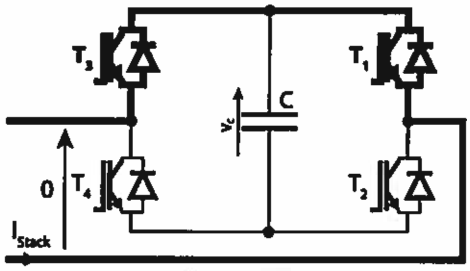
(i) Explain briefly the differences between full H-bridge cells (FB) and half-bridge cells (HB) for use in an MMC. [3]

[Bookwork: 1 mark for each off: number of devices, power losses and fault blocking] Both types consist of a charged DC capacitor and a set of IGBT/diode switches. However the full H-bridge cells contain 4 IGBT/diode modules as compared to 2 in the half-bridge cell. This implies that the full H-bridge cells are more complex, expensive and generate more power losses than the half-bridge cells (since more devices are present in the current path). The half-bridge cell has a draw back in that if the DC bus voltage of the MMC is reduced by a fault, the current path into the fault is via diodes only and can not be interrupted. The H-bridge cell has an IGBT in the fault path.

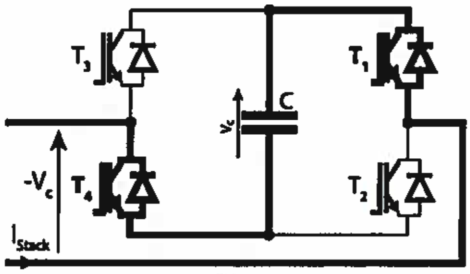
(ii) **Draw the four switching states of a full H-bridge cell and indicate through which devices the current is flowing depending on its direction.** **[3]**

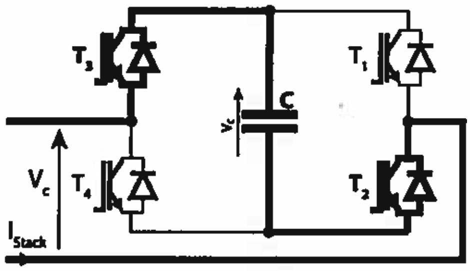
[Bookwork: 1 marks for diagrams; 2 marks for correct identification of voltage loops and devices in each state]





	Zero-voltage mode 1	Zero-voltage mode 2
I>0	IGBT T2 + Diode T4	Diode T1 + IGBT T3
I<0	Diode T2 + IGBT T4	IGBT T1 + Diode T3





	Negative-voltage mode	Positive-voltage mode
I>0	Diode T1 + Diode T4	IGBT T2 + IGBT T3
I<0	IGBT T1 + IGBT T4	Diode T2 + Diode T3

(c) **Discuss the main advantages and disadvantages of the half-bridge MMC, especially compared to other converter topologies such as the 3-level neutral point clamped (NPC) converter.** **[4]**

[Bookwork: full 4 marks for mention of 4 significant points such as reduction of switching loss and filter size; bulk; complexity]

The MMC essentially retain the advantages of the classic VSC (e.g. constant DC voltage, full 4-quadrant P-Q operation, black start capability…) but gains from its high number of cells (or submodules). This fact enables the MMC to generate a converter voltage waveform with numerous voltage steps, reducing significantly the need for high frequency PWM switching of its IGBT modules, thus increasing the converter's power efficiency. Other positive consequences of this operating mechanism consists in the saving on both the AC and DC filter banks and the modular design.

On the negative side, the MMC requires a larger valve hall because of its numerous bulky cells. The control of the converter has been significantly made more complex because of the large number of modules needing to be switch independently. Finally, the half-bridge MMC is still weak against DC-side fault as the fault current can still run through the anti-parallel diodes.

(d) An half-bridge MMC has the following parameters:

- Power rating: 800 MW
- DC bus voltage: ±330 kV
- Nominal cell voltage: 1,650 V

(i) Determine the maximum AC line voltage that this MMC converter can generate. [2]

$$\hat{V}_{converter} = \pm V_{DC_{terminal}} = \pm 320\ kV$$
$$V_{converter} = 226.3\ kV_{RMS} = 391.9\ kV_{line-to-line}$$

(ii) Calculate the number of IGBT/diode modules and DC capacitors. [2]

$$N_{cell} = \frac{V_{DC}}{V_{cell}} = \frac{2\times 330\ 10^3}{1650} = 400\ per\ arm = 2{,}400\ in\ total\ (6\ arms)$$
$$N_{IGBT} = 6\times 2\times N_{cell} = 12\times 400 = 4800\ modules$$
$$N_{capacitors} = 6\times N_{cell} = 6\times 400 = 2400\ Capacitors$$

(iii) Assuming that the stack of cells can sustain a maximum energy deviation of 850 kJ, calculate the minimum value of the cell capacitors in order to limit their voltage excursion to 5%. [3]

$$C_{cell} = \frac{2\ \Delta E}{N_{cell}\ V_{cell}^2\ (1.05^2 - 1)} = \frac{2\times 850\ 10^3}{400\times 1650^2\ (1.05^2 - 1)} = 15.2\ mF$$

3.

a)

i) An ideal power semiconductor switch has zero on-state resistance (to an arbitrary current rating), zero off-state conductance (to an arbitrary voltage rating), and transitions between the on and off-state in zero time. Discuss the fundamental trade offs in achieving these characteristics for both majority and minority carrier devices.

[5]

[bookwork]
High voltage devices need to be long, i.e. they need distance between source and drain/anode and cathode/collector and emitter. This inherently means that the on-state resistance per unit area of device increases.

[1]

This is particularly a problem in majority carrier switches (mosfets) because the long n- drift region then present a significant contribution to the on-state resistance.

[1]

A solution is to use minority carrier devices, such as an IGBT. This allows reduces on-state resistance at a given voltage due to conductivity modulation of the drift region. However, this then slows down the device switching speed because carriers have to be removed from the device at switch off.

[2]

There is also an inherent trade off that increased current handling capability causes increased leakage currents, as the cross sectional area will be greater, increasing leakage.

[1]

ii) Wide band gap semiconductors (such as SiC) are of great interest to the power electronics community. Explain why this is.

[3]

[bookwork]
Wide band gap devices have several advantages over silicon devices. These include:

- Higher electric field strength before breakdown
- Higher thermal conductivity (aids getting heat out of the device)
- Higher operating temperature

b) IGBTs are commonly available in ratings to a few kV. When circuits require ratings greater than this, devices are often put in series. Explain why sharing networks are required and sketch a sharing network that would ensure sharing in both the transient and DC states.

[5]

[bookwork]

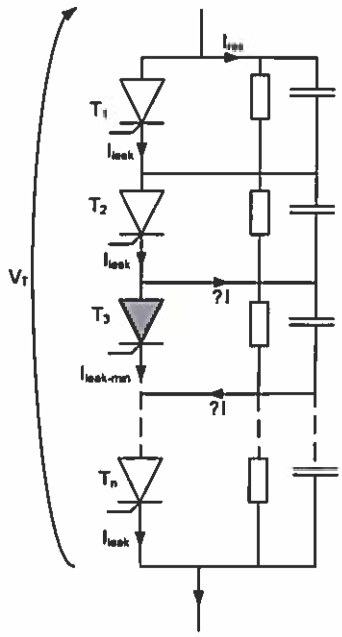
Devices are not perfectly matched, either in terms of manufacturing (doping density, exact replication of geometry etc) or in terms of operating temperature due to imperfect packaging and finite heatsink thermal resistance

[1]

This means that leakage currents differ between devices, as does the required reverse recovery charge when the device goes into blocking mode.

[1]

This means that a series string of resistors (to equalise DC voltage blocking due to unequal leakage currents) and a series string of capacitors (to equalise voltage during switching due to differences in recovery charge should be used as shown:



[3]

c) It is suggested that, rather than using a sharing network, the drain voltage waveform could be fed back to aid the switching of a chain of devices. Fig Q3.1 shows the proposed setup.

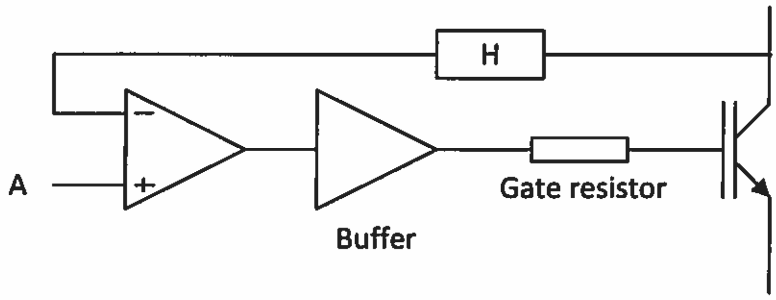


Figure Q3.1 Drain voltage feedback system for one device to be used in a series string

i) What are the purposes of the buffer and gate resistor?

[2]

[application of knowledge]
The buffer provides sufficient current to quickly charge and discharge the gate of the device to allow it to switch on and off quickly. The resistor provides damping for resonant tank formed between the transistor parasitic capacitances and the inherent inductance in the gate drive loop.

ii) The component "H" has a flat frequency response and a gain of 1/1000. What is its purpose?

[1]

[previously unseen material]
The gain H connects the drain voltage back to a comparator – hence H is a simple potential divider which converts the potentially high drain voltages to levels which are comparable with the signal electronics.

iii) Explain how the system is expected to work. In your answer, make reference to what the signal fed in as "A" represents.

[4]

[previously unseen material]
The system contains negative feedback whereby a signal fed into A is compared to a faction (by H) of the drain voltage. Hence, the signal fed into A is a scaled version of the required drain voltage.

[1]

The negative feedback in the system ensures that the drain voltage follows a waveform which is 1000 times (due to the gain H) that which is fed into the A input. The buffer ensures that there is sufficient gate drive current available to make this happen quickly. Therefore, multiple devices can be stacked in series and fed with the same A drive signal, and due to feedback they will all switch in a uniform way allowing equal voltage sharing.

Part B

4.

a)

i) How is the loadability of a transmission circuit defined?

[3]

The loadability of a transmission circuit is the ability to continuously carrying current without violating prevalent operating and technical constraints such as thermal, voltage and stability limit violations. The loadability is generally expressed as ampere – for design engineer it is expressed as loading (MW) normalised to surge impedance loading or natural loading.

ii) How does circuit length influence the loadability of a transmission circuit?

[3]

Lines which are relatively shorter such as less than 80 Km, the temperature rise and sag (minimum ground clearance) limits the loading limit. This varies from season to season. With longer lines the reactive consumptions of the line at higher loading and hence the voltage drop decides the upper limit. Angle stability becomes an important consideration for longer lines (400 KM and above) while loading them.

b) Unlike a telecommunication line, a power line should not be terminated by its characteristic impedance – justify this statement through technical arguments.

[4]

The termination of a line at surge impedance results in voltage and current at the same phase throughout the length of the lines. The communication line transmits signal at much larger frequency than power frequency. Fidelity and strength of the signal at the receiving end are the primary consideration. Termination of communication line through characteristic impedance is a practical way of operation to avoid distortion on the line. The energy associated with communication line is small, so the efficiency is of minor interest. In contrast, efficiency, economy and reliability of supply are factors of prime importance in the case of power transmission. There is only one frequency so the distortion is not a problem in the same sense as it is in communication lines. The length of most power lines are fraction of the normal wavelength, hence the line can be terminated at load impedance much lower than the characteristic impedance.

c) A 500 kV transmission circuit is 500 Km long. Despite the fact that the line has two current carrying capacities (summer and winter) both of them are hardly utilised. Justify with reason.

[3]

When a transmission circuit is 500 km long, the loadability is mainly influenced by small signal angle stability limit. Small signal stability limit is much lower than thermal capacity limits (be it summer or winter). Naturally there is only one consideration.

d) Many HV/EHV circuits, particularly in developed countries are re-insulated to upgrade to a higher voltage. What are the other implications on the terminal equipment that must be assessed and addressed before upgrading them to higher voltage?

[3]

With larger insulation and upgrading lines to higher voltage will affect ground capacitance and also overall fault level. They will require reassessment of the suitability of the circuit breaker switching capability in the presence high switching overvoltage. The fault level being different, it will require coordination of the over current protection through recalculated plug and time multiplier setting. Overall the protection against faults and transients need to be redesigned and set.

e) **Describe two important benefits of FACTS technologies.**

[4]

The commissioning of FACTS device in a long line will lift the stability limit. Typically a series capacitor will make a long transmission lines electrically shorter, so more can be transferred with keeping the stability margin uncompromised.

Reduce reactive power flows thus allowing lines to carry more active power. With voltage based compensation at the midpoint of transmission system, the reactive component of the current will drop and active component of the current in the line will increase. This also improves voltage stability margin. So the line at the receiving end can receive more active power.

5

a)

i) **Describe the principle of series compensation in a power transmission system.**

[4]

The series capacitor works by increasing the voltage across the transmission line that is function of line current. This happens as part of the inductive voltage drop in the line is compensated by the capacitive drop. The conventional view is that the series capacitor cancels a portion of the series reactance and thereby reducing the effective transfer reactance. An interesting physical view is in to order increase the current through the line increased voltage has to be impressed across the physical line, this can be accomplished by adding series connected circuit element (passive or active) that would provide a voltage in phase opposition to the voltage prevalent across the series line reactance. A simple capacitor can be used to do this but a synchronous voltage source can also do the job in much controlled way.

The technology has matured from fixed capacitor (FC) to controllable one. In FC, fixed value of capacitance is connected in series with the line. The module is achieved through large number of units. The amount of series compensation is expressed as percentage of total line reactance. Typically it varies from 10-70 %.

ii) **With the help of power angle characteristics of a transmission line, show how a series capacitor boosts the steady state power transfer margin.**

[5]

The percentage of compensation is defined as k*100%, where k is degree of compensation. The effective transmission reactance is given by

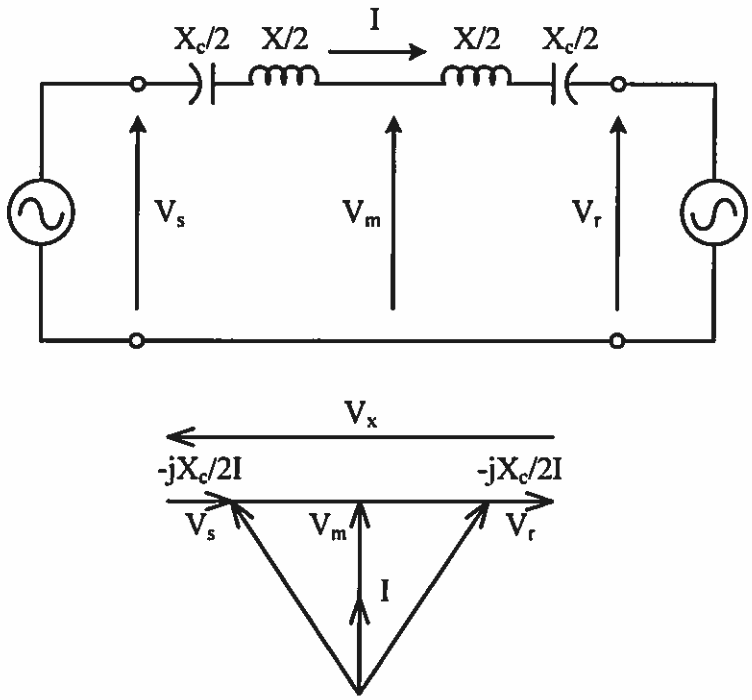
$X_{eff} = X_L - X_c\ ;\ k = \frac{X_c}{X_L}$

'k' is known as the degree of series compensation. The expressions for power are given as:

$$P = \frac{V^2}{(1-k)X}\sin\delta, Q_c = \frac{2V^2}{X}\frac{k}{(1-k)^2}(1-\cos\delta)$$

Consider a two machine power system as shown in Fig A5.1. The power angle equation is as follows:

$$P = \frac{V^2}{X_L(1-k)}Sin\delta;\ Q = \frac{2V^2}{X_L(1-k)^2}(1-cos\delta)$$



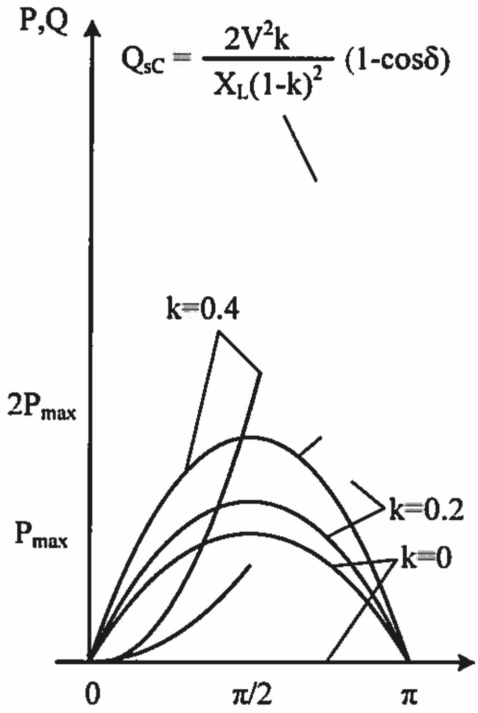


Fig A5.1 Power flow control through fixed capacitor

It is seen that the power transfer capacity is enhanced because of reduction effective line impedance. The power transfer capability increases with degree of compensation. The reactive power supplied by the capacitor to the system also rapidly increases with degree of compensation. The series capacitor is being used for over last 50 years.

iii) A simple 500 kV transmission circuit shown in Fig 5.1 transfers 400 MW of power. Additional generation from a wind farm at the sending end is planned. The wind farm has 100 turbines each of 3.6 MW capacity. Obtain the range of the degree of compensation required to extract the power from the wind farm producing at full capacity keeping the power transfer stability margin at the same level of uncompensated case. Assume 1.0 p.u. voltage at the sending and receiving ends. The line impedance is 0.16 p.u. and is purely reactive. Assume base MVA to be 100.

[6]

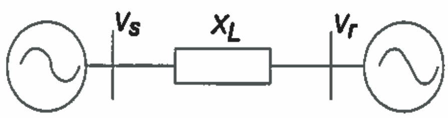


Fig 5.1: A simple interconnected power system model

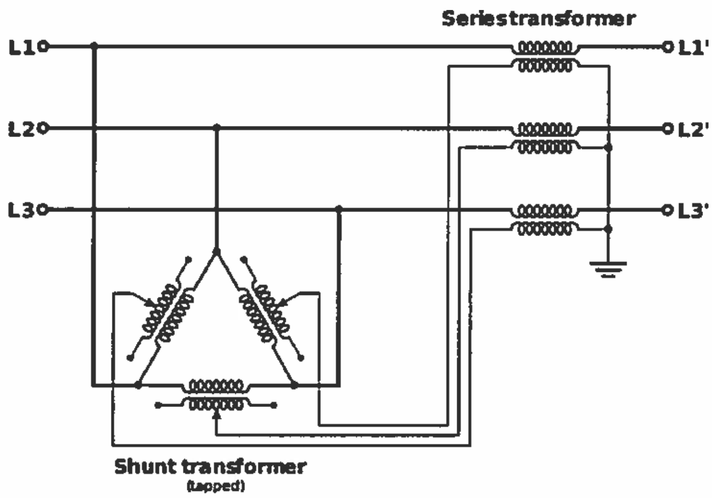
Let us consider degree of compensation is ‘k’ . The power transfer angle is δ

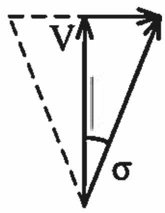
The power angle equation for uncompensated case $P_1 = P_{max1}Sin\delta_1$ and for compensated case is $P_2 = P_{max2}Sin\delta_2$. Since steady state power transfer stability margin has to be maintained, power angle should remain same i.e $\delta_1 = \delta_2$. $P_1 = 4.0\,p.u, P_2 = 7.6\,p.u, P_{max1} = \frac{1}{0.16}, P_{max2} = \frac{1.0}{(1-k)*0.16}$
Solving the above for the compensation, it was found $k = 0.48$ or 48%

b) Many power transmission grids around the world have installed quadrature boosters for power flow control. With the help of schematic and vector diagram show how they control the power flow.

[5]

The quadrature booster is a technology that injects a small fraction of line voltage in series with other phase voltage. The device utilises a shunt and series transformer combination. The three phase shunt transformer secondary produced a stepped down voltage. Part of this voltage is then injected in series with the line. As can be seen in the figure, a fraction of the voltage between line 2 and line 3 is injected in series with line 1. The concept utilises a 90 degree phase shift between voltage (L23) and phase voltage in L1. Thus the phase angle of the voltage in L1 after the series transformer is changed appreciably while keeping the magnitude virtually unchanged. Since real power flow is very sensitive to angle – power flow can be easily influenced. This helps in power transfer between the two ends of a line. This is similar to the technology of thyristor control phase shifter (TCPS) except it is not switchable. Once a particular tap position from the secondary of the shunt transformer is connected with the primary of the series transformer it cannot be altered while it is in operation. The phase angle introduced will be fixed. It has to be taken out of service for readjusting the tap position. The vector diagram shows the phase shift introduced by the quadrature boosting technology. The technology is very simple, reliable but in the situation when variable power flows through lines are desired, it has its limitation.





6

a)

i) Describe through a suitable circuit schematic how a Unified Power Flow Controller (UPFC) works.

[5]

The UPFC is the most versatile members of the FACTS family as virtually the operating characteristics of all the other FACTS controllers discussed so far can be realised with it. Fig A6.1

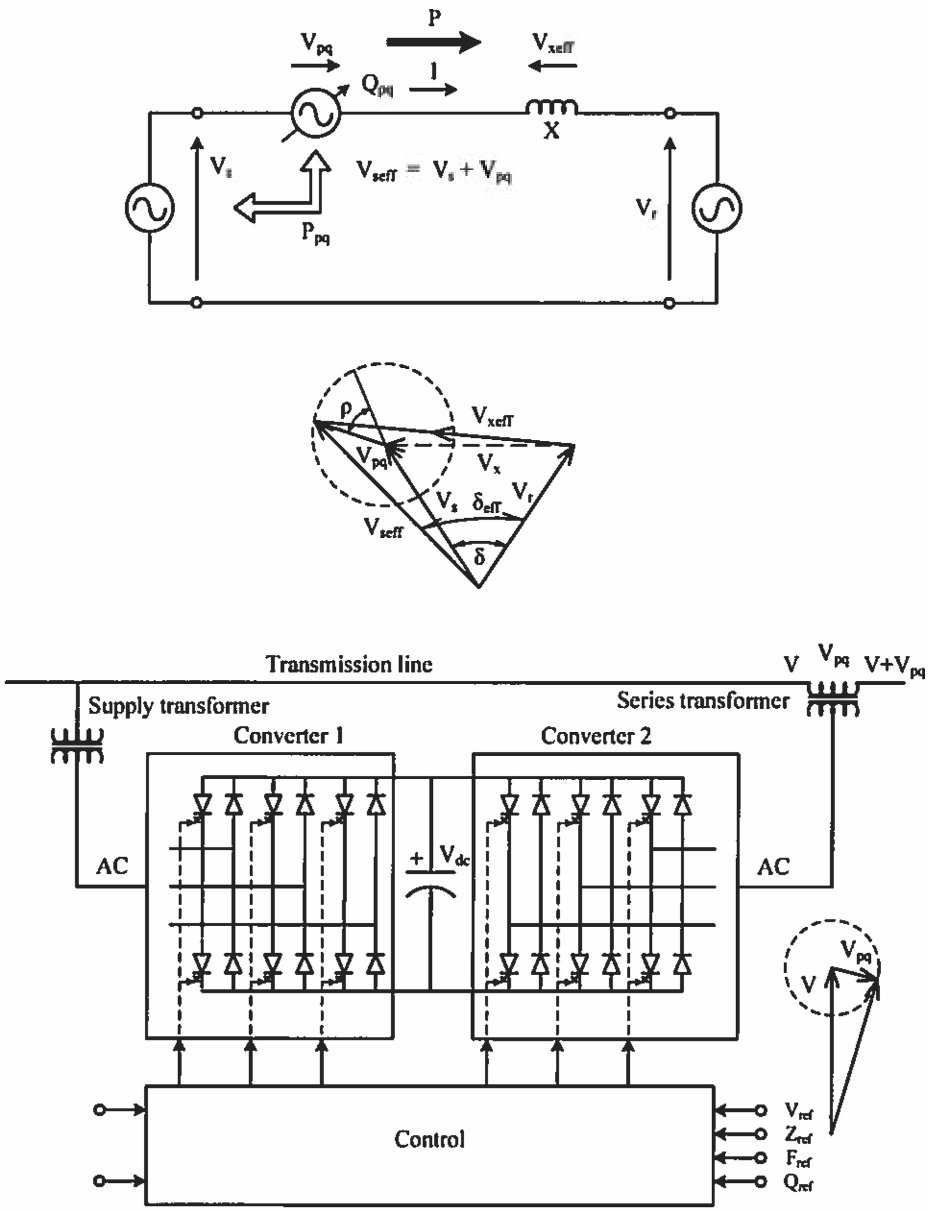
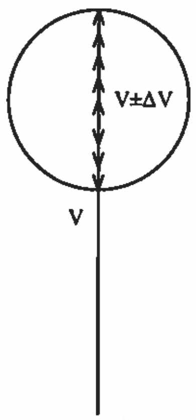


Fig A6.1: Unified Power Controller topology and circuit model

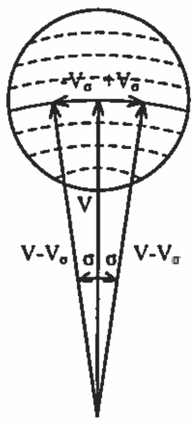
ii) With the help of a vector diagram, show the phase angle and voltage regulation capability of the UPFC.

[8]

The following diagram shows how voltage and phase angles are controlled in UPFC. [4] for the phase angle diagram and [4] for the voltage regulation diagram.



Voltage regulation



Phase shifting

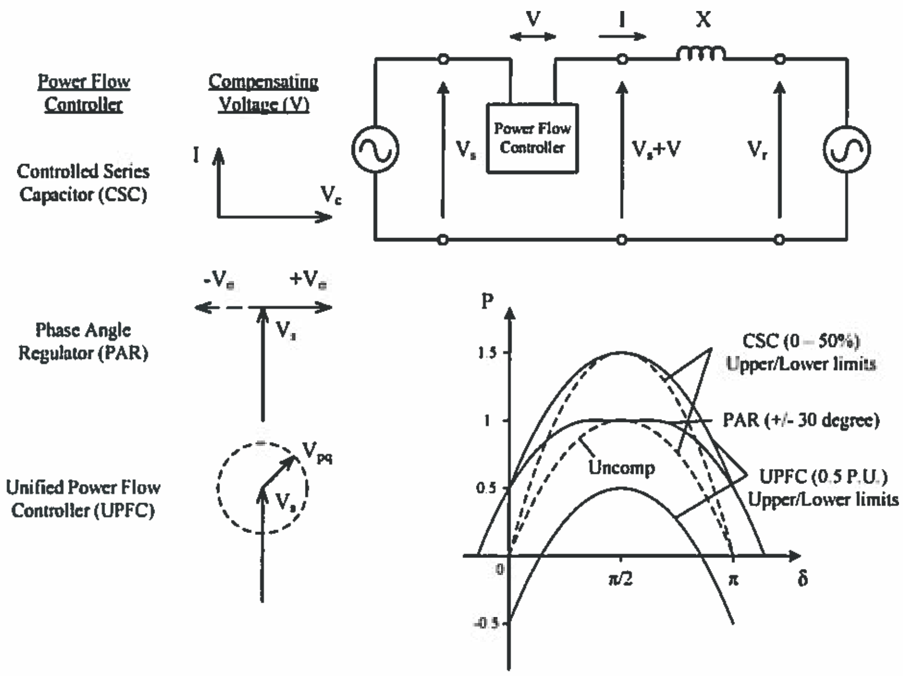


Fig A6.2: VI and power flow characteristics of UPFC b)

i) Describe the loss characteristics of static var compensator (SVC) employing a Fixed Capacitor and Thyristor Controlled Reactor (FC+TCR) and a Thyristor Switched Capacitor and Thyristor Controlled Reactor (TSC+TCR).

[5]

In FC+TCR topology there are three distinct components of losses: capacitor and associated filter banks which reasonably constant because of fairly constant system voltage, in the inductor, it varies proportional to the square of the current through it, and in thyristor switches where the losses are proportional to the current (linear). Fig A6.3 shows its loss characteristics. Overall when the device absorbs plenty of var through TCR, the loss is high and when it operates as a capacitor, the loss is fairly small.

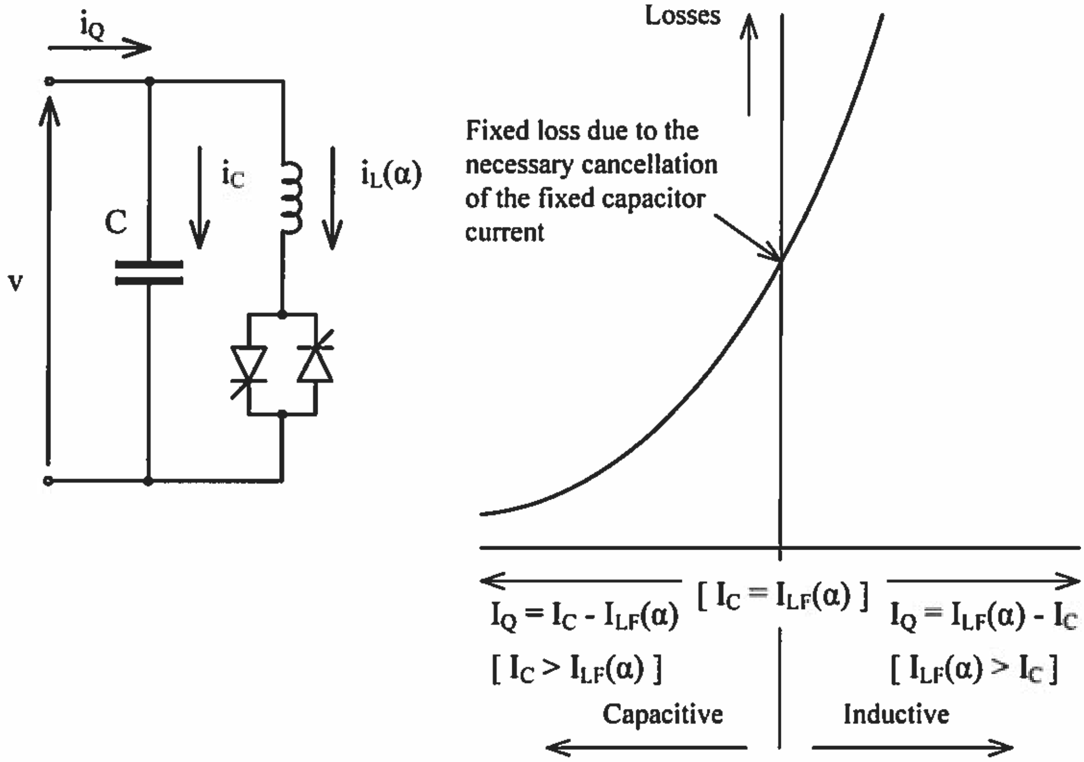


Fig. A6.3: Loss characteristics of FC+TCR type of var generator

[2.5 marks]

In TSC+TCR topology, the loss versus var output characteristics is shown in Fig A6.4 and it can be understood easily from the principle of operation of the device. At or slightly below zero var output, all capacitor banks are switched out, the TCR current is zero or negligibly small and consequently, the losses are zero or almost zero. As the capacitive output is increased, an increasing number of TSC banks are switched in with the TCR absorbing the surplus capacitive vars. Thus with each TSC bank, the losses increase by a fixed amount. To this fixed loss, there are the added losses of the TCR which may be maximum to zero between successive switching of the TSC banks as illustrated in the figure. Overall the loss of TSC+TCR topology is proportional to the var output.

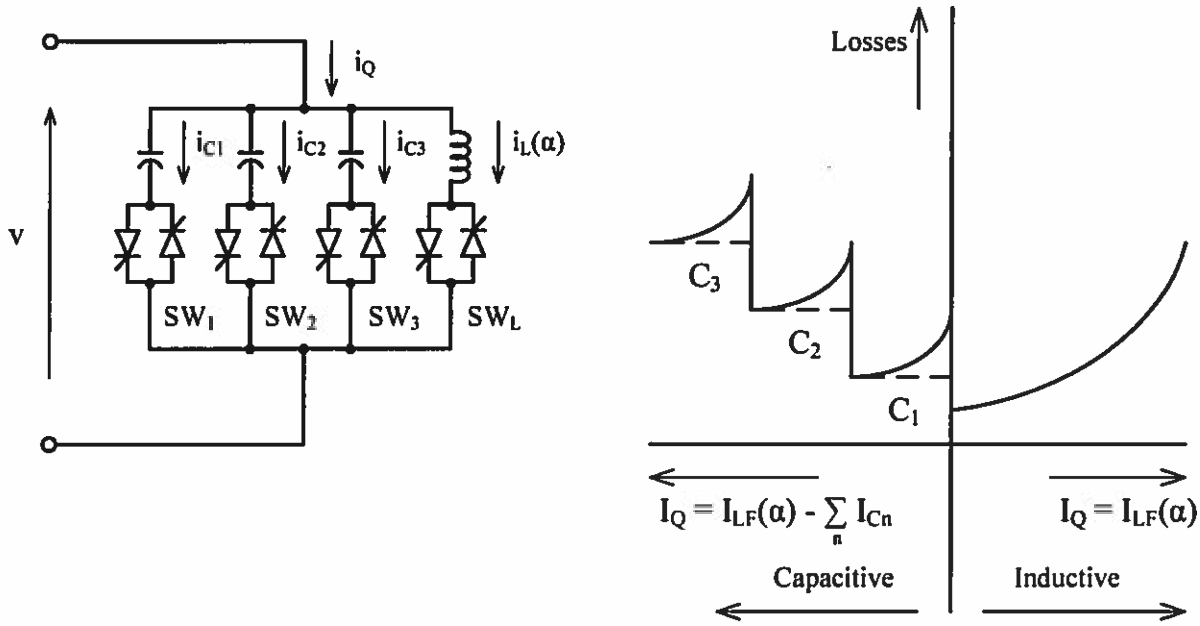


Fig A6.4: Loss characteristics of FC+TCR type of var generator

[2.5 marks]

ii) Justify with reason which of these technologies is more suitable for dynamic voltage support at the substation feeding a large steel production plant.

[2]

The steel production process through induction heating draws plenty of reactive power. This increases current in the substation feeder. The impact of high current is drop in voltage across nearby loads. It is important provide the reactive power requirement locally. SVC can act most of the time to produce leading capacitive current thus the TCR part will not see much current. As one can see from the loss characteristics in Fig A6.3, it is very beneficial to use FC+TCR types of technology. For such industrial application where power factor correction is primary objective, FC+TCR should be preferred because of its low losses.