

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING  
EXAMINATIONS 2011

EEE PART II: MEng, BEng and ACGI

## **ANALOGUE ELECTRONICS 2**

Thursday, 2 June 2:00 pm

Time allowed: 2.00 hours

**There are THREE questions on this paper.**

**ALL questions are compulsory.**

**Question 1 carries 40% of the marks and Questions 2 and 3 carry 30% each.**

**Any special instructions for invigilators and information for candidates are on page 1.**

**Basic expressions for voltage gain, input and output resistance for single stage amplifiers are given on the last page.**

Examiners responsible

First Marker(s):

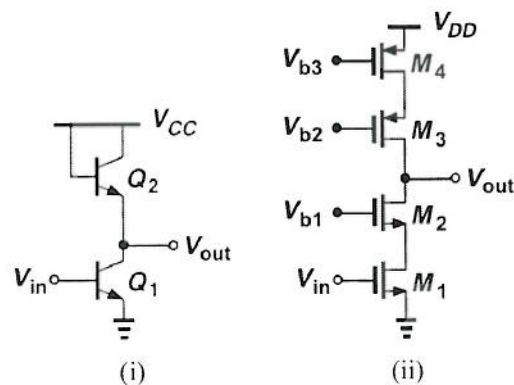
T.G. Constandinou, T.G. Constandinou

Second Marker(s):

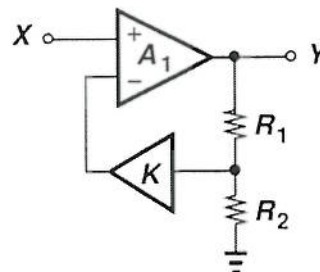
K. Harris, K. Harris

1. This question consists of 10 brief items. Each item can be answered in a few words or a short paragraph with use of a diagram and/or expression where helpful. Please answer all sub-questions, which carry equal marks.

- List four types of *non-ideal behaviour* in a real (as oppose to ideal) operational amplifier. [4]
- List four benefits of applying *negative feedback* to analogue circuits. [4]
- Explain why *device mismatch* poses a challenge in analogue design. Give two techniques in analogue layout design to improve device matching. [4]
- Describe what is meant by the *body effect* and explain how circuits can be designed to eliminate/reduce this. [4]
- With the aid of a diagram describe *Miller's Theorem* and explain where this is useful. [4]
- Derive expressions (by inspection) for the *voltage gain* of the circuits shown below (assuming  $\lambda \neq 0$ , i.e.  $r_o < \infty$ ). State any assumptions made if simplifying the expressions. [4]

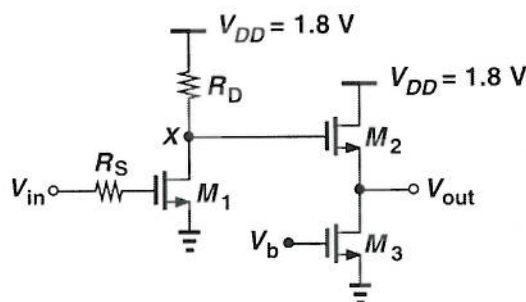


- Calculate the *loop gain* and *closed-loop gain* of the circuit shown below. Assume the op-amp exhibits an open-loop gain of  $A_1$ , but is otherwise ideal. [4]



- Explain what is meant by a *cascode* and how this technique can be applied to improve amplifier performance. [4]
- Explain which amplifier topology (single stage) you would use as a *voltage buffer*. Justify your reasoning. [4]
- Design a  $5K\Omega$  *integrated* polysilicon resistor (i.e. calculate  $W$  and  $L$ ) assuming a maximum current of  $0.5mA$  (given  $R_{poly}=8\Omega/\square$  and  $J_{max}=0.1mA/\mu m$ ). [4]

2. The circuit shown below is a two stage amplifier, specifically a common source stage followed by a source follower stage. Assume  $\lambda > 0$  (i.e.  $R_{out} < \infty$ ) for all devices.

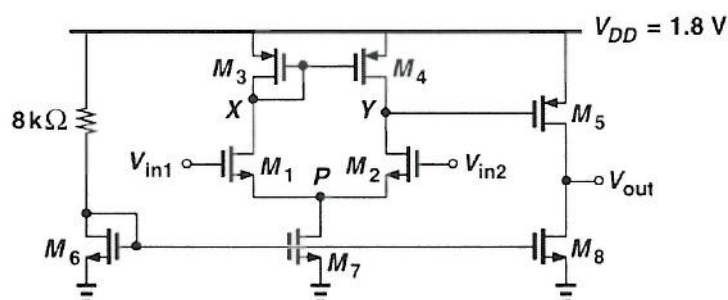


- Redraw the circuit above to: (i) identify the 3 nodes that are associated with poles and (ii) include all the parasitic device capacitances (within  $M_{1,3}$ ). [10]
- Determine an expression for the low frequency voltage gain of the first stage ( $V_x/V_{in}$ ). [2]
- Determine an expression for the resistance seen looking into node X. [2]
- Determine an expression for the DC (i.e. low frequency) voltage gain of the 2<sup>nd</sup> stage ( $V_{out}/V_x$ ). [2]
- Determine an expression for the output resistance. [2]
- Determine expressions for the capacitances (to ground) at each of the nodes identified above by lumping together the parasitic capacitances appearing at each node. Use Miller's theorem to resolve any floating (i.e. ungrounded) capacitances. [6]
- Determine expressions for the three pole frequencies ( $\omega_{p1}$ ,  $\omega_{p2}$  and  $\omega_{p3}$ ). [6]

3. A basic two stage operational amplifier is shown below.

This circuit consists of the differential pair ( $M_1$  and  $M_2$ ), an active current mirror ( $M_3$  and  $M_4$ ) to convert a differential to single-ended output, a second stage common source amplifier ( $M_5$ ), and biasing circuit ( $8k\Omega$  resistor and passive current mirror  $M_6-8$ ).

Assume all devices are in saturation and  $\lambda > 0$  (i.e.  $R_{out} < \infty$ ). Where required, use the following values:  $\mu_n C_{ox} = 200 \mu A/V^2$ ,  $\mu_p C_{ox} = 100 \mu A/V^2$ ,  $V_{TH,n} = 0.4V$ ,  $V_{TH,p} = -0.5V$ ,  $\lambda_n = 0.1V^{-1}$ ,  $\lambda_p = 0.2V^{-1}$ .

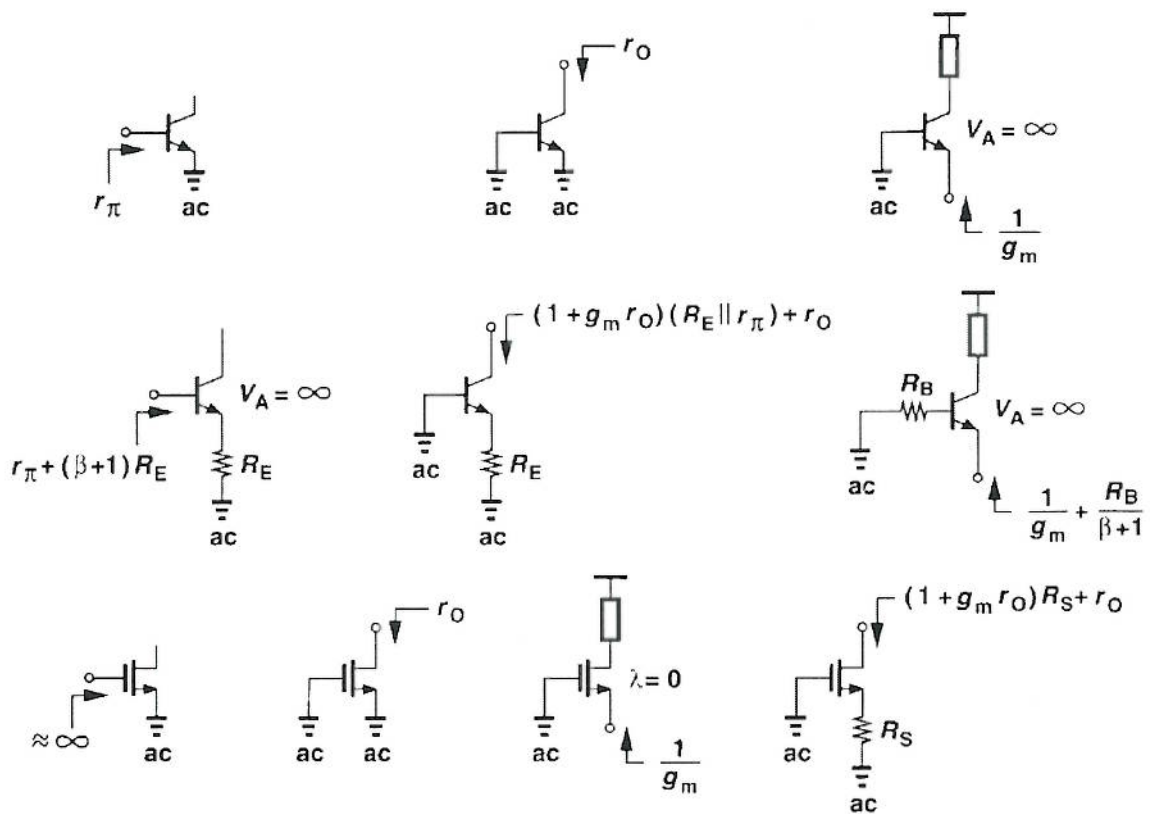


Use the following expression for the drain current of a MOSFET:

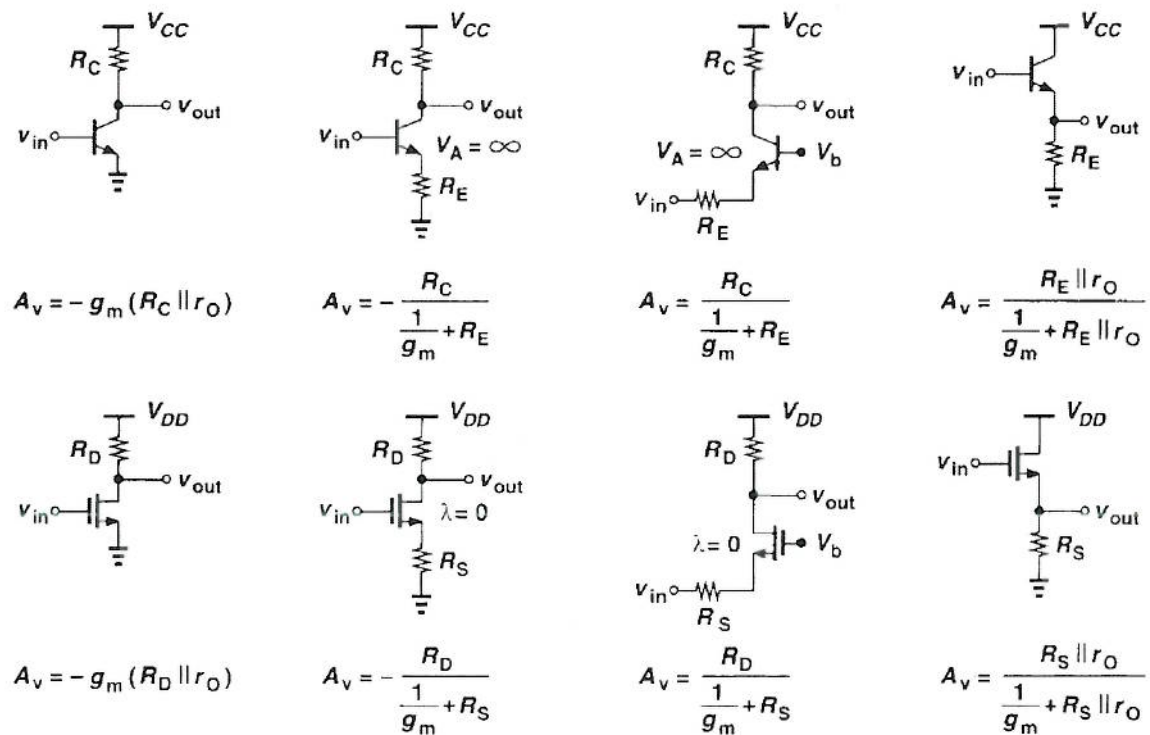
$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

- Calculate the current through device  $M_6$  ( $I_6$ ), given that  $(W/L)_6 = 6.4/0.18$ . [7]
- Given that  $I_7 = 1.5mA$  and  $I_8 = 3mA$ , calculate  $(W/L)_7$  and  $(W/L)_8$ . [2]
- Derive an expression for the differential voltage gain of the first stage ( $A_{v1} = V_y / (V_{in1} - V_{in2})$ ). [5]
- Derive the expressions for the voltage gain of the second stage ( $A_{v2} = V_{out} / V_y$ ) and therefore the total voltage gain ( $A_v = A_{v1} A_{v2} = V_{out} / (V_{in1} - V_{in2})$ ). [3]
- Given that:  $(W/L)_1 = (W/L)_2 = 250/1$   
 $(W/L)_3 = (W/L)_4 = 4/4$   
 $(W/L)_5 = 40/4$   
 Calculate the voltage gain (in dB). [10]
- Give three drawbacks of the bias generator circuit used in this design. [3]

## Input and Output Impedances



## Voltage Gain Equations





- ① (a) (i) offset voltage due to input stage mismatch and finite gain  
 (ii) input bias current (in BJT) - non-zero  
 (iii) finite gain - not infinite  
 (iv) non-zero o/p impedance  
 (v) bandwidth/slew-rate  
 (vi) limited input/output range
- } any 4 of the following
- ④

- (b) (i) gain desensitisation  
 (ii) bandwidth enhancement  
 (iii) modification of input/output impedances  
 (iv) improved linearisation
- ④

- (c) ~~Looking for~~: Device mismatch poses a challenge in analogue design because although devices may be designed to be identical (or scaled), in reality due to processing tolerances there will always be mismatch  $\therefore$  performance will be different to the designed.
- ②

Methods to improve: (i) larger device area

(ii) close proximity

(iii) same orientation

(iv) use common centroid geometry

(v) use dummy devices

} any 2 of the following

②

- (d) The body effect manifests itself as a variation in MOSFET (mosfet) threshold voltage depending on the source-body bias ( $V_{SB}$ ).

The full expression is:  $V_{TH} = V_{TH0} + \gamma(\sqrt{2\phi + V_{SB}} - \sqrt{2\phi})$

where:  $V_{TH0}$  is the  $V_{SB}=0$  threshold voltage

$\gamma$  is the body effect parameter

$2\phi$  is the surface potential parameter.

①

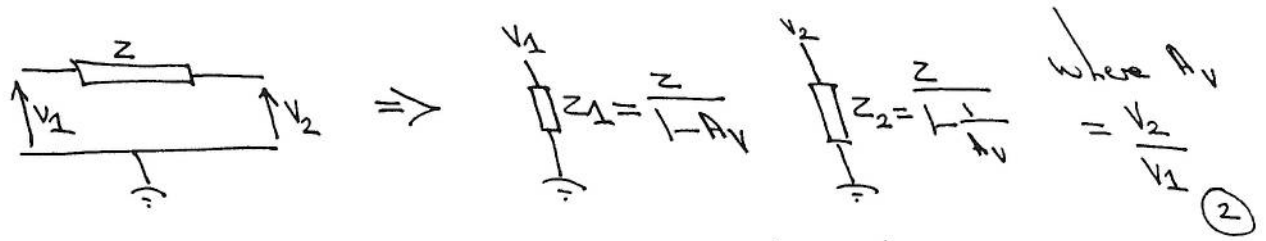
①

①

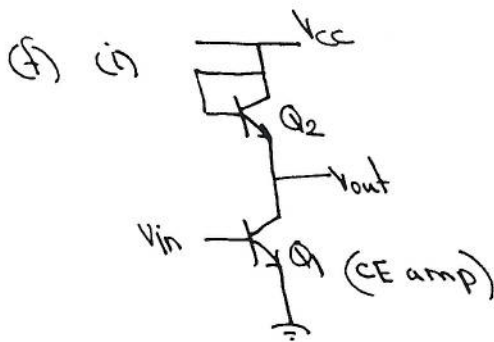
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The body effect can be reduced/eliminated by designing circuits such that all  $V_{SB}=0$ . If any devices have sources that are not connected to the power supply, the circuit should be designed such that these are PMOS devices - since they are in N-wells  $\therefore$  have an independent body terminal.

- (e) Miller's theorem establishes that in a linear circuit, if two nodes are connected by an impedance  $Z$ , this impedance can be replaced by two grounded impedances  $Z_1$  and  $Z_2$  as follows: ①



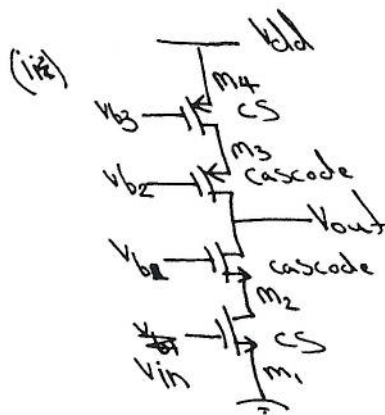
This is particularly useful in analogue circuit analysis for resolving floating impedances, for example parasitic transistor capacitances to grounded impedances at each node. ①



$$A_v = -g_{m1} (r_{o1} \parallel r_{o2} \parallel \frac{1}{g_{m2}})$$

→ assuming  $\frac{1}{g_{m2}} \ll r_{o1}, r_{o2}$

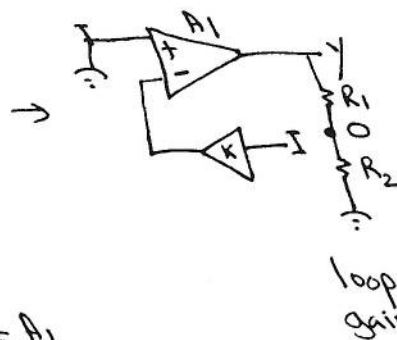
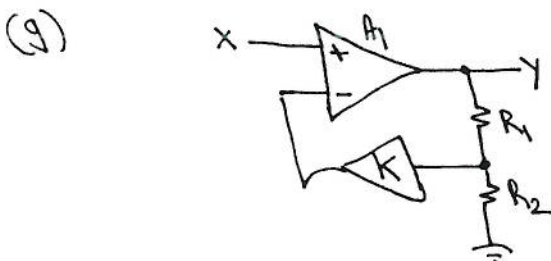
$$A_{v1} \approx \frac{-g_{m1}}{g_{m2}}$$
 ②



$$A_v = -g_{m1} ((g_{m2} r_{o1} r_{o2} + r_{o1} + r_{o2}) \parallel (g_{m3} r_{o3} r_{o4} + r_{o3} + r_{o4}))$$

→ assuming  $g_{m2} r_{o1} r_{o2} \gg r_{o1}, r_{o2}$   
and  $g_{m3} r_{o3} r_{o4} \gg r_{o3}, r_{o4}$

$$A_v \approx -g_{m1} (g_{m2} r_{o1} r_{o2} \parallel g_{m3} r_{o3} r_{o4})$$
 ②



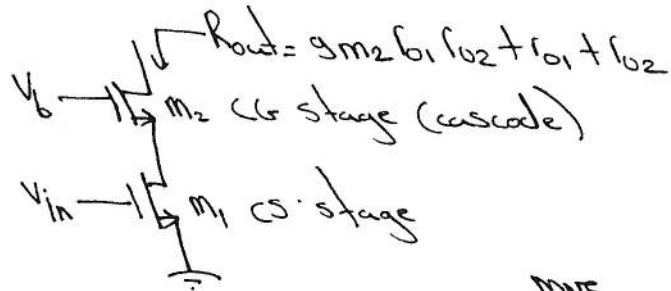
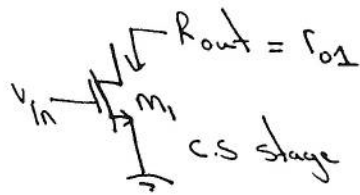
$$0 = I(-A_1)K \frac{R_2}{R_1 + R_2}$$

$$-\frac{0}{I} = K A_1 \frac{R_2}{R_1 + R_2}$$
 ②

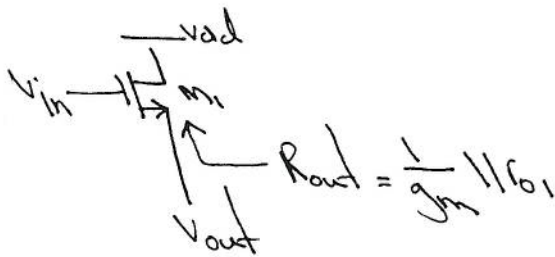
open-loop gain  $= A_{OL} = A_1$

∴ closed-loop gain  $= \frac{A_1}{1 + LG} = \frac{A_1}{1 + K A_1 \frac{R_2}{R_1 + R_2}}$  ②

- (h) A cascode stage is a common-base (or common-gate) amplifier connected to the <sup>the o/p of</sup> common emitter (or common source) amplifier. This can also be viewed as a degenerated common emitter. A cascode stage is often used to boost the output impedance of an amplifier and therefore also the voltage gain.



- (i) The common-collector (or common drain) amplifier, <sup>more</sup> often referred to as emitter (or source) follower is preferred as a voltage buffer. This is because in this configuration the amplifier has a high input impedance and low output impedance and therefore is ideal as a voltage buffer.



- (j) Given  $J_{max} = 0.1 \text{ mA}/\mu\text{m}$ ,  $I_{max} = 0.5 \text{ mA}$   
and  $R_{poly} = 8 \Omega/\square$

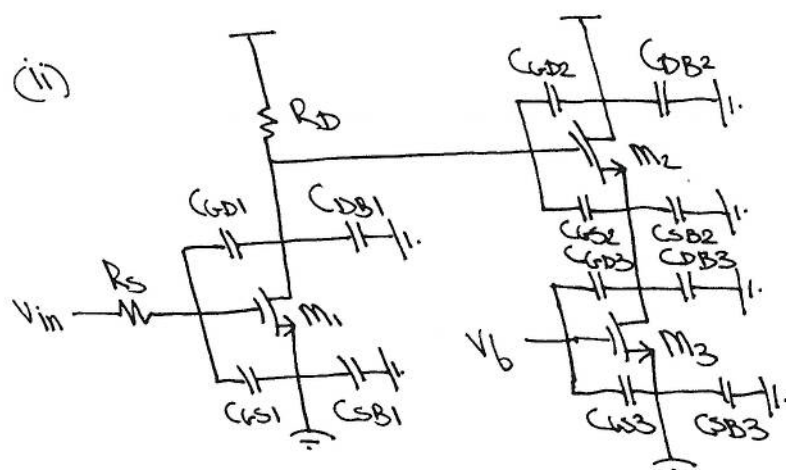
for a 5K $\Omega$  resistor:  $W = \frac{I_{max}}{J_{max}} = 5 \mu\text{m}$

$$\frac{L}{W} = \frac{5000}{8} = 625$$

$\therefore L = 625 \times 5 = 3125 \mu\text{m}$



3



7

②



②





(2)

②

2

$$(9) \quad \omega_{p1} = \frac{1}{R_s \cdot C_{p1}} = \frac{1}{[C_{GS1} + C_{GD1}(1 + g_{m1}(R_D || r_{o1}))]R_s} \quad (2)$$

$$\omega_{p2} = \frac{1}{R_x \cdot C_{p2}} = \frac{1}{[C_{DB1} + C_{GD2} + C_{GD1}(1 + \frac{1}{g_{m1}(R_D || r_{o1})}) + C_{GS2}(1 - \frac{r_{o2} || r_{o3}}{\frac{1}{g_{m2}} + r_{o2} || r_{o3}})](R_D || r_{o1})} \quad (2)$$

$$\omega_{p3} = \frac{1}{R_{out} \cdot C_{p3}} = \frac{1}{[C_{SB2} + C_{DB3} + C_{GD3} + C_{GS2}(1 - \frac{\frac{1}{g_{m2}} + r_{o2} || r_{o3}}{r_{o2} || r_{o3}})] \frac{1}{g_{m2}}} \quad (2)$$

$$(3) (a) \quad V_{GS6} + I_b \cdot (8k\Omega) = 1.8$$

$$V_{GS6} + \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS6} - V_{TH})^2 \quad (8k) = 1.8$$

$$(8k) \frac{200\mu}{2} \cdot \frac{6.4}{0.18} (V_{GS} - 0.4)^2 + V_{GS} = 1.8$$

$$8k (3.5 \times 10^{-3}) (V_{GS}^2 - 0.8V_{GS} + 0.16) + V_{GS} - 1.8 = 0$$

$$28.4V_{GS}^2 - 22.75V_{GS} + 4.54 - 1.8 = 0$$

$$28.4V_{GS}^2 - 21.75V_{GS} + 2.744 = 0$$

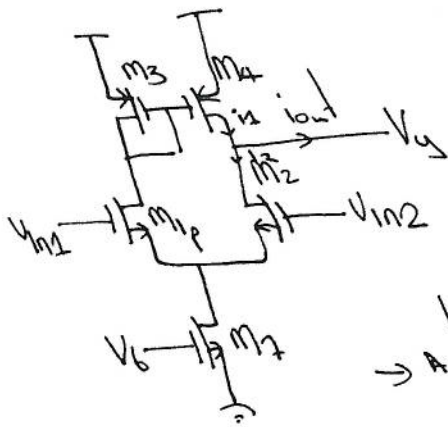
$$V_{GS} = \underline{\underline{0.606}} \text{ and } \underline{\underline{0.189}} \text{ below threshold.}$$

$$\begin{aligned} \therefore I_b &= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \\ &= \frac{1}{2} (200\mu) \frac{6.4}{0.18} (0.606 - 0.4)^2 \\ &= 150\mu A \end{aligned} \quad (2)$$

$$(b) \text{ Given that } I_7 = 1.5mA \Rightarrow \left(\frac{W}{L}\right)_7 = 10 \left(\frac{W}{L}\right)_6 \Rightarrow \frac{64}{0.18} = \left(\frac{W}{L}\right)_7$$

$$I_8 = 3mA \Rightarrow \left(\frac{W}{L}\right)_8 = 20 \left(\frac{W}{L}\right)_6 \Rightarrow \frac{128}{0.18} = \left(\frac{W}{L}\right)_8 \quad (2)$$

(3) (c)



$$i_{out} = i_1 - i_2$$

→ Assuming node P is an AC ground

$$i_1 = g_{m1} V_{in1}$$

$$i_2 = g_{m2} V_{in2}$$

$$\therefore i_{out} = g_{m1} (V_{in1} - V_{in2}) \quad \text{assuming } M_1 \text{ and } M_2 \text{ are identical.}$$

$$V_{out}$$

$$V_{out} = i_{out} \cdot R_{eq}$$

$$R_{eq} = r_{o2} \parallel r_{o4}$$

$$\therefore \frac{V_{out}}{V_{in1} - V_{in2}} = g_{m1} (r_{o2} \parallel r_{o4})$$

(5)

$$(d) \frac{V_{out}}{V_{in}} = -g_{m5} (r_{o5} \parallel r_{o8})$$

$$\frac{V_{out}}{V_{in1} - V_{in2}} = \frac{V_{out}}{V_{in}} \times \frac{V_{in}}{V_{in1} - V_{in2}}$$

$$= -g_{m5} (r_{o5} \parallel r_{o8}) \cdot g_{m1} (r_{o2} \parallel r_{o4})$$

$$|A_v| = g_{m1} g_{m5} (r_{o2} \parallel r_{o4}) (r_{o5} \parallel r_{o8})$$

(36)

$$(e) \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{250}{1}$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \frac{4}{4}$$

$$\left(\frac{W}{L}\right)_5 = \frac{40}{4}$$

$$\text{use } g_m = \sqrt{2I_D \mu C_{ox}}$$

$$g_{m1} = \sqrt{1.5m \left(\frac{250}{1}\right) 200\mu} = 8.66mS$$

$$g_{m5} = \sqrt{6m \left(\frac{40}{4}\right) 100\mu} = 2.45mS$$

$$r_{o2} = \frac{1}{\lambda_n I_{D2}} = \frac{1}{0.1 \cdot 0.75m} = 13.3k$$

$$r_{o4} = \frac{1}{\lambda_p I_{D4}} = \frac{1}{0.2 \cdot 0.75m} = 6.6k$$

$$r_{o2} \parallel r_{o4} = 4.44k$$

$$r_{o5} = \frac{1}{\lambda_p I_{D5}} = \frac{1}{0.2 \cdot 3m} = 1.6k$$

$$r_{o8} = \frac{1}{\lambda_n I_{D5}} = \frac{1}{0.1 \cdot 3m} = 3.3k$$

$$r_{o5} \parallel r_{o8} = 1.11k$$

$$\therefore A_v = (2.45m)(8.66m) 4.44k \cdot 1.11k = 103.6$$

$$= 40.3dB$$

10

(f) PVT  $\longrightarrow$  P = Process

V = Voltage (Power Supply)

T = Temperature

} Need to list the following explaining how it is dependant.

3