IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2015

EEE PART II: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 2

Corrected Copy

Wednesday, 17 June 2:00 pm

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 carry equal marks (30% each).

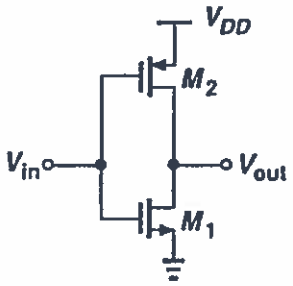
Basic expressions for voltage gain, input and output resistance for single stage amplifiers are given on the last page.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : T. Constandinou
Second Marker(s) : C. Toumazou

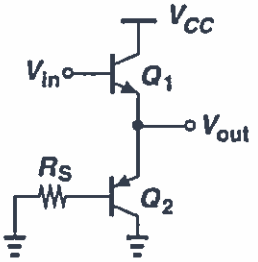
1. This question consists of 4 sub-questions. Each item can be answered in a few words or a short paragraph with use of a diagram and/or expression where helpful. Please answer all sub-questions and simplify expressions where possible stating any assumptions made.

a) Derive expressions (by inspection) for the *voltage gain* of the amplifier circuits shown below (including r_O). [20]



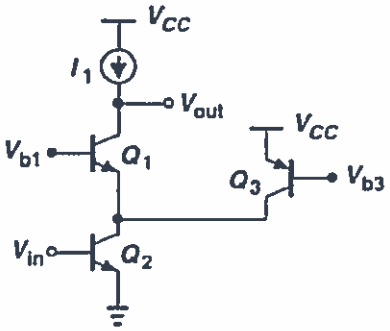
(i)

Fig. 1.1(a)



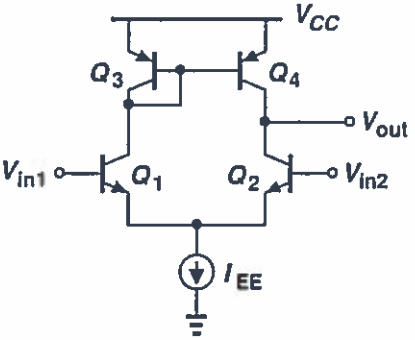
(ii)

Fig. 1.1(b)



(iii)

Fig. 1.1(c)



(iv)

Fig. 1.1(d)

b) Describe the basic principle of operation of a *bandgap voltage reference* circuit. When is such a circuit used? [5]

c) Explain how the circuit implementation of a differential amplifier can affect the following characteristics: (i) *common mode rejection ratio*; and (ii) input offset voltage. [5]

d) Draw the *bode plot* (magnitude only) for a single stage common-emitter amplifier having a capacitively coupled input and resistive load. Include the parasitic capacitances. [5]

e) Explain the differences between *direct* and *capacitive coupling* and identify the related constraints when designing analogue integrated circuits. [5]

2. The circuit shown below in Fig. 2.1 is an interface circuit for a photodiode.

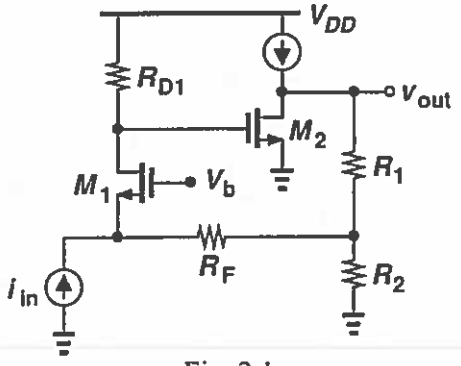


Fig. 2.1

a) State what kind of amplifier this is and what are the ideal input and output impedances. [3]

b) By breaking the loop, determine expressions for the following (including r_0):

i. Open-loop gain [10]

ii. Feedback factor [5]

iii. (Open loop) input and output impedances [5]

iv. (Closed loop) gain, input and output impedances [7]

3. The circuit shown below in Fig. 3.1 is a 3-stage operational amplifier.

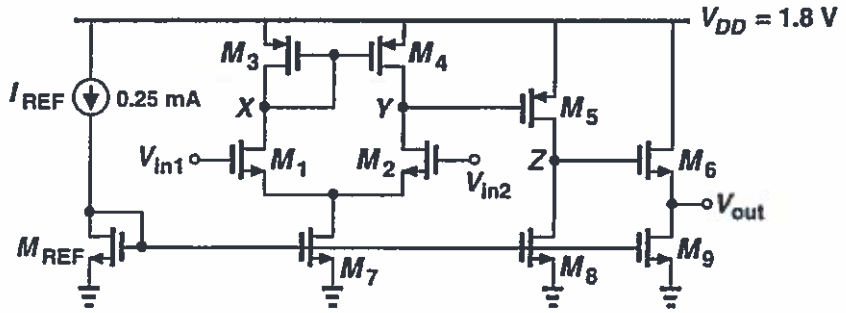


Fig. 3.1

Transistor sizing as follows:

Table 3.1

	M_{REF}	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9
W/L	2/4	250/1	250/1	5/2	5/2	50/1	50/1	8/4	16/4	80/4

Assume all devices are in saturation and $\lambda>0$ (i.e. $R_{out}<\infty$).

Use the following transistor parameters where needed: $\mu_n C_{ox}=200\mu A/V^2$, $V_{THN}=0.4V$, $\lambda_N=0.1V^{-1}$, $\mu_p C_{ox}=100\mu A/V^2$, $V_{THP}=-0.5V$, $\lambda_P=0.2V^{-1}$

a) What is the total power consumption? [4]

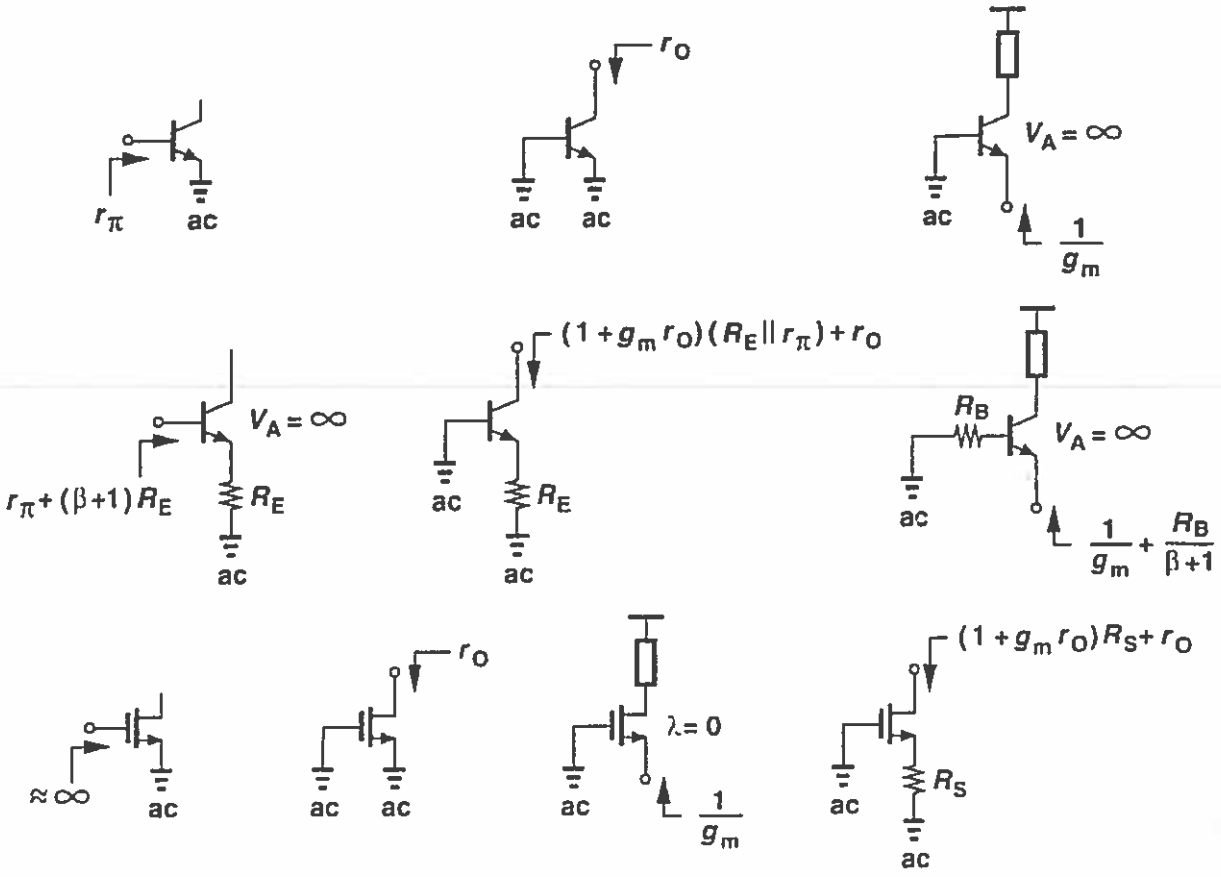
b) Determine an expression for the voltage gain of the amplifier, $A_v=V_{out}/(V_{in2}-V_{in1})$ and evaluate. [10]

c) Determine an expression for the output impedance (R_{out}) of the amplifier and evaluate. [4]

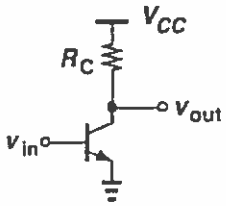
d) Identify the nodes associated with poles and discuss which 2 will dominate the frequency response (excluding nodes V_{in1} and V_{in2}). [2]

e) Determine expressions for these 2 pole frequencies stating any assumptions made and evaluate. Where required, use the following parasitic capacitance values: $C_{GS}=(2/3)WLC_{ox}$, $C_{ox}=20fF/\mu m^2$, $C_{GD}=C_0W$, $C_0=0.5fF/\mu m$, $C_{DB}=C_{SB}=0$. [10]

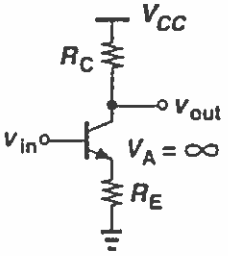
Input and Output Impedances



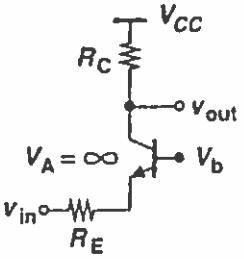
Voltage Gain Equations



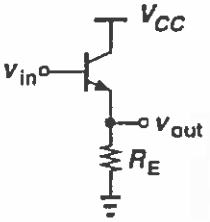
$$A_v = -g_m(R_C \| r_O)$$



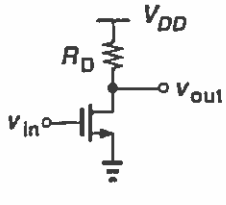
$$A_v = -\frac{R_C}{\frac{1}{g_m} + R_E}$$



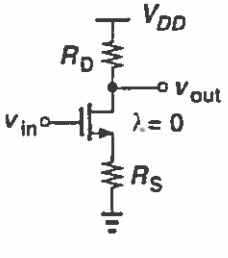
$$A_v = \frac{R_C}{\frac{1}{g_m} + R_E}$$



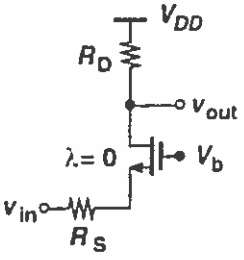
$$A_v = \frac{R_E \| r_O}{\frac{1}{g_m} + R_E \| r_O}$$



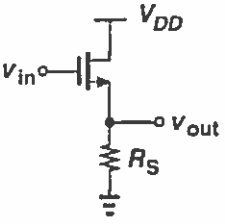
$$A_v = -g_m(R_D \| r_O)$$



$$A_v = -\frac{R_D}{\frac{1}{g_m} + R_S}$$



$$A_v = \frac{R_D}{\frac{1}{g_m} + R_S}$$



$$A_v = \frac{R_S \| r_O}{\frac{1}{g_m} + R_S \| r_O}$$