IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2000

ISE PART I: M.Eng. and B.Eng. and ACGI

**COMPUTER ARCHITECTURE 2**

Monday, May 8 2000, 2:00 pm

There are FOUR questions on this paper.

Answer THREE questions.

All questions carry equal marks.

Time allowed: 1:30 hours

Examiners: Dr W. Luk, Prof P.G. Harrison

1a  Explain what CPI stands for, and how it can be used in a formula for estimating execution time of a program.

b  Explain briefly what are single-cycle datapaths and multi-cycle datapaths. Give one advantage and one disadvantage of each of these datapaths.

c  The executable code for a program P contains m type-A instructions and n type-B instructions.

   i)  What is the execution time for P on a machine containing a single-cycle datapath with a fixed cycle time, given that the propagation delay through the datapath for executing a type-A instruction is $\alpha$ seconds and that for a type-B instruction is $\beta$ seconds? What is the CPI for this machine?

   ii)  If the single-cycle datapath can support variable cycle time, what will be the shortest execution time for P?

   iii)  A machine with a multi-cycle datapath takes x cycles for type-A instructions and y cycles for type-B instructions. Calculate the cycle time for the multi-cycle datapath machine, such that the execution time for the program P is the same as that for the single-cycle datapath machine in i). Based on the information given, what is the CPI for the multi-cycle datapath machine?

*The three parts carry, respectively, 10%, 30% and 60% of the marks.*

2   This question concerns regular combinational circuits formed by replicating a simple unit. For each of the four parts below, provide a circuit diagram and label one of the replicating units using a dotted box.

a   Design an adder for 3-bit unsigned numbers, such that the output will become the largest number whenever overflow occurs. Label the signal value on all the wires in your circuit when adding the two numbers 100 and 110.

b   Design a circuit for comparing two 3-bit unsigned numbers a and b such that the output is 1 when a > b. There should only be one wire connecting two neighbouring replicating units. Label the signal value on all the wires in your circuit when a=100 and b=011.

c   Use your design in part b to develop a circuit which produces the larger of two 3-bit numbers. Label the signal value on all the wires in your circuit when a=100 and b=011.

d   Design a 3-bit circuit which calculates the number of zeroes in the input. Label the signal value on all the wires in your circuit when the input is 010.

*The four parts carry, respectively, 25%, 25%, 25% and 25% of the marks.*

3a   Provide a diagram for the control circuit produced by compiling the
     statement

     `IF B THEN P ELSE Q`

     into hardware using the token-passing method. Your circuit diagram
     should clearly indicate the *start* input for the token to enter, and the
     *finish* output for the exit of the token.

 b   Provide a diagram for the control circuit produced by compiling the
     statement

     `REPEAT P UNTIL B`

     into hardware using the token-passing method.

 c   The `EXIT` statement can be used to terminate a `REPEAT-UNTIL` statement
     before the condition specified in the `REPEAT-UNTIL` statement becomes
     true. Provide a diagram for the control circuit produced by compiling the
     following program into hardware using the token-passing method.

```
REPEAT
  SEQ
    P
    IF B1 THEN Q ELSE EXIT
    R
UNTIL B2
```

   *The three parts carry, respectively, 15%, 25% and 60% of the marks.*

4a Give one advantage and one disadvantage of a direct-mapped cache with one-word blocks.

b What is the total number of bits of storage required for a direct-mapped cache with $2^m$ bytes of data and one-word blocks, given that the address size is $n$ bits and each word contains $2^k$ bytes?

c Provide a diagram of a 64-kilobyte multi-word direct-mapped cache, given that each block contains 4 words, each word contains 4 bytes, and memory addresses are 32 bits. Show clearly on the diagram the tag size and the data size for an entry in the cache, and how a given address can be used to locate its entry in the cache. Show also the hardware for generating the hit signal and the corresponding data when a cache hit occurs.

d Give one advantage and one disadvantage of a direct-mapped cache with multi-word blocks.

e What is the total number of bits of storage required for a direct-mapped cache with $2^m$ bytes of data and multi-word blocks, given that the address size is $n$ bits, each block contains $2^a$ words and each word contains $2^k$ bytes?

*The five parts carry, respectively, 10%, 25%, 30%, 10% and 25% of the marks.*