UNIVERSITY OF LONDON
IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 1997

BEng Honours Degree in Computing Part II
MEng Honours Degrees in Computing Part II
MSc Degree in Computing Science
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the
Diploma of Membership of Imperial College
Associateship of the City and Guilds of London Institute

PAPER 2.4 / M3.31

ARCHITECTURE

Friday, April 25th 1997, 4.00 - 5.30

Answer THREE questions

For admin. only: paper contains 4 questions

1a Explain why MIPS (million instructions per second) is often not a reliable measure of performance.

b The purpose of *synthetic benchmarks* is to have a single artificial benchmark program such that its execution frequency of statements matches the statement frequency in a large set of benchmarks. What are the disadvantages of synthetic benchmarks?

c A subset of the instructions for a machine M can be accelerated by n times using a coprocessor C. Given that a program P is compiled into instructions of M such that a fraction α belongs to this subset, what is the overall speedup that can be achieved using C?

d Given that C costs β times as much as M, calculate the minimum fraction of instructions for programs that C has to accelerate so that the overall system (M and C) is β times faster than M.

e Given that the performance of M is improving by m times per month, how many months will pass before M alone can execute the program P in part c as fast as the current combined system of M and C?

The five parts carry, respectively, 15%, 15%, 20%, 25%, and 25% of the marks.

2a Show how a halfadder can be built using a two-input and-gate and a two-input xor-gate. Hence show how a fulladder can be implemented using two-input logic gates. Given that all two-input logic gates have the same delay T, calculate the propagation delay of a 32-bit ripple-carry adder. How many two-input logic gates are required for this adder?

b Show how a 32-bit carry-select adder can be built using multiplexors and seven 8-bit ripple-carry adders. Given that a multiplexor contains three two-input logic gates and that a two-input logic gate can have one of its inputs inverted without affecting its delay, how many two-input logic gates are required for this carry-select adder? What is the propagation delay of this design?

c Minimise the propagation delay of a 32-bit carry-select adder, if 4-bit, 5-bit, 6-bit and 7-bit ripple-carry adders are available. What is the total number of two-input logic gates in this design?

The three parts carry, respectively, 30%, 35% and 35% of the marks.

3a A datapath containing u control signals has been developed for a set of instructions with v-bit opcode. Provide diagrams to show how control units for this datapath supporting

i) horizontal microinstructions, and

ii) vertical microinstructions

can be implemented using an incrementer, a ROM (Read-Only Memory), a register, address select logic and a decoder. The unencoded microinstructions are k-bits wide. Indicate the size of components in your diagrams whenever possible.

b Describe how the address select logic in part a can be implemented using ROMs and multiplexors. Explain how the number of ROMs in the address select logic relates to the state diagram for the control unit.

Given that the address select logic has a two-bit address select signal, and that it contains two ROMs which are fully utilised, sketch an alternative implementation of the address select logic which involves a single ROM with $(v + 1)$-bit address instead of the two ROMs.

c The microprogram of a control unit has n w-bit microinstructions, some of which are identical. Given that there are m distinct microinstructions in this microprogram, explain how one can reduce the total microprogram storage by reducing the width of the microinstructions while including an additional store of distinct microinstructions of width w. Calculate the reduction in microprogram storage that can be achieved using this approach, and comment on its possible disadvantages.

The three parts carry, respectively, 25%, 35% and 40% of the marks.

Turn over...

4a Calculate the execution time for a machine M1 processing n instructions with d data references per instruction, a clock cycle time t_1, a miss rate r_1 and a miss penalty p. M1 takes c cycles per instruction on average when there are no memory stalls.

b Machine M2 is identical to M1 except that M2 has a shorter cycle time t_2 and a smaller cache which causes a larger miss rate r_2 than M1. Derive a formula for the miss penalty p such that the execution time for M1 is longer than that for M2.

c Show how to configure a three-block cache as

i) a direct mapped cache D,

ii) a fully associative cache F.

What are the advantages and disadvantages of D and F?

d An instruction cache is implemented in two ways using the two caches D and F in part c. LRU replacement is used with cache F. For each of these caches, given the sequence of block addresses

$$1, 2, 3, 4, 1, 2, 3, 4, 1, 2, 3, 4$$

i) show the cache content after each block access,

ii) count the number of hits and misses,

iii) estimate the number of misses for four successive block accesses in the steady state, if the above sequence of block addresses repeats forever.

e Compare your answers to part c and part d, and provide explanations if there are any discrepancies.

The five parts carry, respectively, 15%, 15%, 20%, 40% and 10% of the marks.

End of paper