E3.11
E4.42
AO8

IMPERIAL COLLEGE LONDON

amended total & wtg

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2008

Corrected Copy

ADVANCED ELECTRONIC DEVICES

Wednesday, 7 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer Question ONE and THREE other questions.

Question One carries 40 marks; remaining questions carry 20 marks each.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : K. Fobelets, K. Fobelets
Second Marker(s) : W.T. Pike, W.T. Pike

Special information for invigilators: Q1 is Compulsory. Hand out the answer sheet for Q2.

Information for candidates: Q1 is Compulsory. Q1 carries a total mark of 40, all other questions carry a mark of 20. Use the special answer sheet with the current-voltage characteristics to answer Q2.

Constants and Formulae list

Electron charge:	$e = 1.6\ 10^{-19}$ C
Permittivity of free space:	$\varepsilon_o = 8.85 \times 10^{-12}$ F/m
Permeability of free space:	$\mu_o = 4\pi \times 10^{-7}$ H/m
Relative permittivity:	ε= 11.8 for Si
Relative permittivity:	ε= 4 for SiO_2
Relative permittivity:	ε= 7.5 for Si_3N_4
Thermal energy:	$kT/e = 0.026\ eV$ at $T = 300K$

Formulae

$$\left.\begin{aligned} J_n(x) &= e\mu_n n(x)E(x) + eD_n\frac{dn(x)}{dx} \\ J_p(x) &= e\mu_p p(x)E(x) - eD_p\frac{dp(x)}{dx} \end{aligned}\right\}$$

Drift and diffusion currents in a semiconductor

$$I_{DS} = \frac{\mu C_{ox} W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right)$$

Drain current in MOSFET (Metal-Oxide-Field-Effect-Transistor) for $V_{GS} > V_{th}$.

$$V_{th} = \frac{1}{e}(\phi_b - \phi_n) - \frac{eN_D a^2}{2\varepsilon}$$

Threshold voltage of MESFET (Metal Semiconductor Field Effect Transistor) Note: first term is built-in voltage.

$$V_{th} = \frac{1}{e}[\phi_b - \Delta E_c] - \frac{eN_D d^2}{\varepsilon}$$

Threshold voltage in HEMT (High Electron Mobility Transistor)

$$n = N_C \exp\left[\left(E_F - E_c\right)/kT\right]$$

Free electron concentration

$$S = \left(\frac{d\log(I_{DS})}{dV_{GS}}\right)^{-1}$$

Sub-threshold slope

1. **Compulsory.**

a) What is the type of doping in the Ohmic contact regions of an enhancement mode MOSFET where, in strong inversion, drift is due to electrons? [4]

b) Give two reasons for the use of polySi (poly crystalline silicon) for the gate contact material in MOSFETs. [4]

c) Give the definition of the threshold voltage, V_{th} as a function of carrier concentrations in a MOSFET. [4]

d) Is the magnitude of the source-drain current I_{DS} for $|V_{GS}|<|V_{th}|$ zero in a real enhancement mode MOSFET? Explain your answer briefly. [4]

e) Give two reasons for the use of self-aligned lightly doped drain regions (LDD). [4]

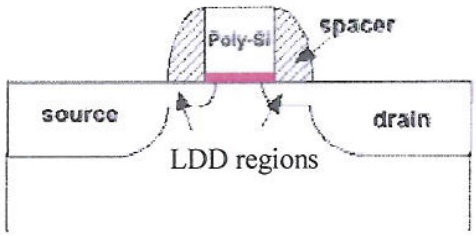

Figure 1.1: Schematic cross section of a MOSFET indicating the LDD regions

f) Draw the cross section of an SOI wafer from top of the wafer to the bottom of the wafer. Define all regions. [4]

g) Explain drain induced barrier lowering (DIBL) in short channel length MOSFETs using an energy band diagram. [4]

h) What is the purpose of modulation doping (e.g. as in a high electron mobility transistor, HEMT)? [4]

i) What is the advantage of a double gated FET (Field Effect Transistor)? [4]

j) Why can an n-channel GaAs MESFET (metal semiconductor field effect transistor) not be used for large positive gate voltages? [4]

2.

a) What is the purpose of introducing tensile strain in the channel of an n-channel MOSFET? [2]

b) The cross section of a surface channel, tensile strained-Si (s-Si) MOSFET is given in fig. 2.1. Sketch E_c and E_F (conduction band and Fermi level) from gate into the virtual substrate along line a-a' for $V_{DS}=V_{GS}=0$V and $V_{th}<0$. V_{th} is the threshold voltage. Neglect the workfunction difference between gate and channel. [5]

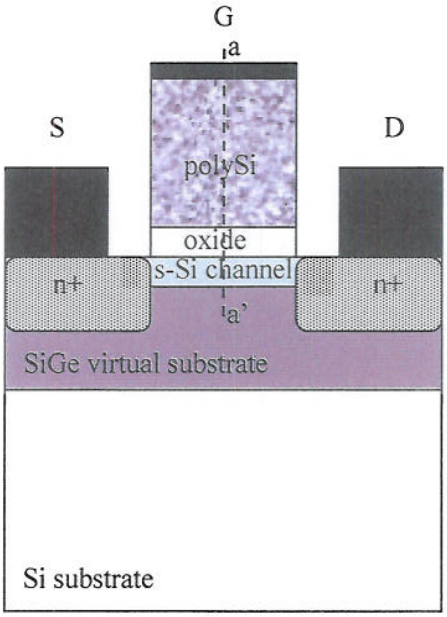

Figure 2.1: Cross section of a surface channel tensile strained Si MOSFET.

c) The transfer characteristics and transconductance, g_m for the device in fig. 2.1 is given in fig. 2.2(a) and fig. 2.2(b) (see next page) for $V_{DS}=0.1$V in the triode region and $V_{DS}=1$V in the saturation region. The gate length is 0.5 μm, gate width 50 μm and the oxide thickness is 4 nm.

i) Extract the threshold voltage of the device in the triode and the saturation region on the answer page with fig. 2.2 (a) & (b) and attach this answer page to your answer book. [7]

ii) Calculate the value of DIBL (drain induced barrier lowering) in this device. [2]

iii) Calculate the maximum value of the mobility μ (in $cm^2/(Vs)$). [4]

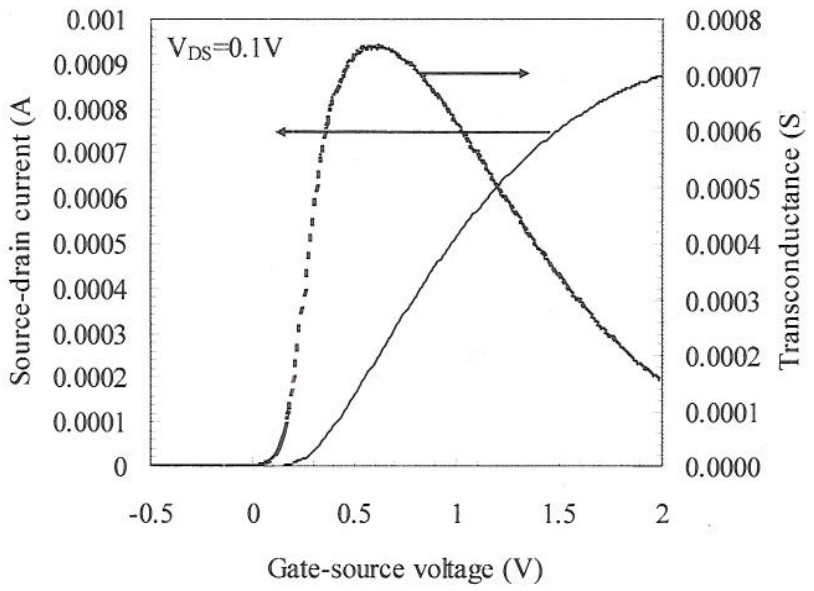

Figure 2.2 (a): The transfer characteristic I_{DS}-V_{GS} of the s-Si MOSFET in the triode region and the transconductance g_m. g_m in bold dashed line.

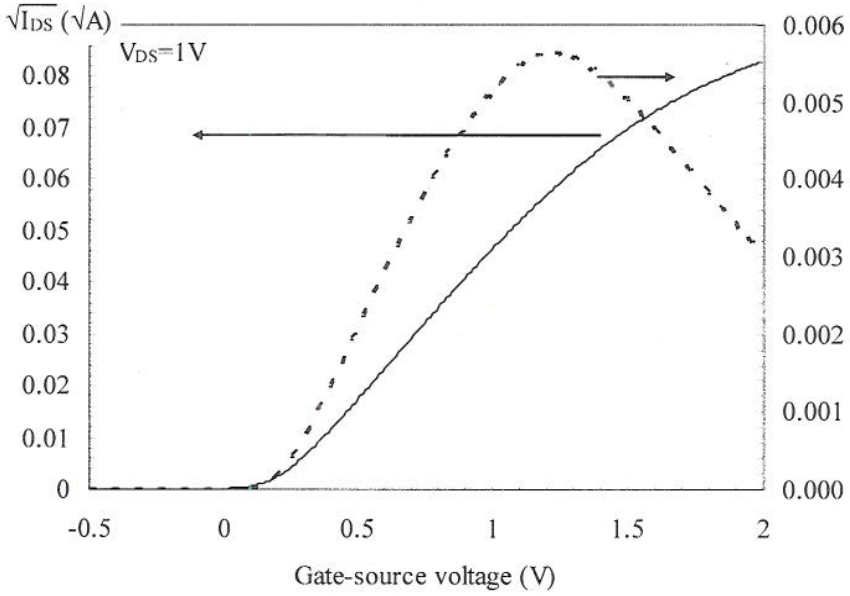

Figure 2.2 (b): The square root of the source-drain current $\sqrt{I_{DS}}$ as a function of gate voltage V_{GS} of the s-Si MOSFET in the saturation region and the transconductance g_m. g_m in bold dashed line.

3.

a) Sketch the material cross section from gate contact to substrate contact, including the Ohmic contact regions, for:

i) a GaAs n-channel MESFET (metal semiconductor field effect transistor). [2]

ii) an AlGaAs/GaAs HEMT (high electron mobility transistor). [4]

b) Sketch the energy band diagram, including E_c, E_v, E_F and E_G, from gate contact into the channel region, including the built-in voltage V_{bi}, for:

i) a GaAs n-channel MESFET (metal semiconductor field effect transistor). [4]

ii) an AlGaAs/GaAs HEMT (high electron mobility transistor). [4]

c) Explain why the built-in voltage V_{bi} in a real GaAs MESFET is not determined by the workfunction difference between the gate metal and the semiconductor channel. [3]

d) Explain the difference in the value of the threshold voltage, V_{th} of an $Al_{0.3}Ga_{0.7}As$ HEMT and an $Al_{0.5}Ga_{0.5}As$ HEMT. [3]

4.

a) Sketch the energy band diagram, including E_c, E_v, E_i, E_F, of an n-channel enhancement mode MOSFET from gate to bulk when V_{DS}= 0V and V_{GS}= V_{th} with V_{th} the threshold voltage. [4]

b) Indicate the parameter $\phi_F = \frac{E_i - E_F}{e}$ in the substrate on your graph in a) and give the expression for the surface potential V_s as a function of ϕ_F at threshold (V_{GS}=V_{th}). (definition of the surface potential at threshold) [4]

c) Assuming the workfunction difference between gate and Si to be zero, write the gate voltage V_{GS} as a function of the voltage across the oxide V_{ox} and semiconductor V_s. [2]

d) Write the expression of charge neutrality for the gate-oxide-semiconductor junction. Define each term in this expression. [5]

e) Based on the previous answers, extract the expression of the threshold voltage V_{th}. You can assume that the oxide is perfect and the channel length long. [5]

5.

a) In fig. 5.1 a 3D sketch of a finFET is given. Draw the material cross section through the gated fin-region as indicated by the plane a-a' in the figure. Ensure all layers are clearly labelled. [4]

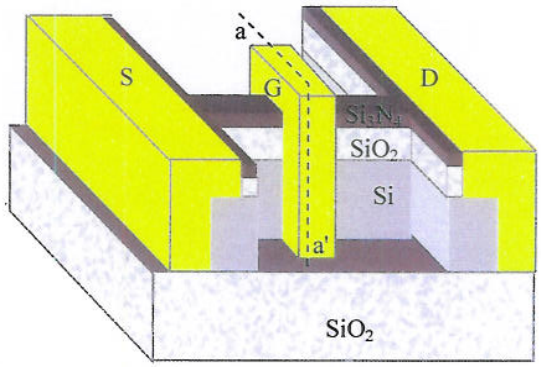

Figure 5.1: 3D sketch of a finFET. SiO_2 and Si_3N_4 are insulators. The gate is made of 1 metal that surrounds the fin. Note that the gate oxide is thin and cannot be seen on this scale.

b) Sketch the energy band diagram, including E_c, E_v, E_F and E_G, from the left to the right part of the gate, across the fin when the workfunction of the metal ϕ_m is larger than the workfunction of the semiconductor ϕ_s. ($\phi_m > \phi_s$). No bias voltages are applied. [4]

c) How many conducting channels does this finFET have at $V_{GS}=V_{th}$? [2]

d) How many channels would the finFET have in the case the top SiO_2 and Si_3N_4 insulators are removed and replaced by a thin layer of SiO_2 with the same thickness as the gate oxide? [2]

e) Give the reasons why the sub-threshold slope of the finFET is near the theoretical minimum of 60mV/dec at room temperature. [4]

f) Explain why DIBL (drain induced barrier lowering) is lower in a finFET than a MOSFET for the same geometrical and material parameters. [4]

6. Essay based on coursework research.

One of the following two subjects/questions can be chosen to write an essay of not more than 200-300 words (1 page):

a) Describe, without using calculations, why a Field Effect Transistor can be used to detect terahertz radiation. How can the FET be optimised to improve the detection efficiency? What are the potential benefits of using FETs as terahertz detectors compared to other existing systems as for instance bolometers.

b) Give the advantages of using GaN technology for both electrical and optical applications. Give a material cross section and energy band diagram of a HEMT consisting of GaN. One of the most significant improvements is based on the field plate connection. Describe what it is and what it does.

[20]