EE4-16 Analogue Signal Processing

Special instructions for students

Unless otherwise stated the following parameters have the following definitions:

V_{DS} : Drain Source Voltage.

V_{GS} : Gate Source Voltage.

V_{TH} : Threshold Voltage.

U_t : Thermal Voltage.

n : Weak Inversion Slope factor.

g_m: Transconductance.

1. a) State two advantages and two disadvantages of using analogue circuits for signal processing.

[bookwork]

- Advantage - Computational capabilities arise from the physics of devices, current, voltage characteristics of NMOS, PMOS, capacitors, diodes, KVL, KCL [1]
- Advantage - One Wire represents many bits of information [1]
- Disadvantage - Sensitive to noise and mismatch [1]
- Disadvantage - Signal is not restored at each stage of computation [1]

[4]

b) The circuit shown in Figure 1.1 has MOS transistors which are operating in the weak-inversion region of operation with a slope factor n = 1.23.

i) Show that the output current $I_{out} = I_1 - I_2$ of the circuit may be given by equation 1. Show all your steps in derivation including the derivation of currents I_1 and I_2.

$$I_{out} = I_{DC}\sinh\left(\frac{V_1 - V_2}{nU_t}\right) (1)$$

[Derivation from notes]

$$I_1 = \frac{I_{DC}}{2} e^{\left(\frac{V_1 - V_2}{nU_t}\right)} \qquad I_2 = \frac{I_{DC}}{2} e^{\left(\frac{-(V_1 - V_2)}{nU_t}\right)}$$

[1+1]

and

$$\sinh(x) = \frac{e^x - e^{-x}}{2}$$ [1]

Thus

$$I_1 - I_2 = I_{DC}\sinh\left(\frac{V_1 - V_2}{nU_t}\right)$$ [1]

[4]

ii) Derive the small signal transconductance and thus derive the transconductance efficiency of the circuit in Figure 1.1 stating all your assumptions. You may use the Taylor series expansion $\cosh x = 1 + \frac{x^2}{2!} + \frac{x^4}{4!} + \cdots$ in your analysis.

Assuming small signals, we only take the first term of the Taylor Expansion [1]

$$Transconductance = \frac{dI_{out}}{dV_{in}} = \frac{I_{DC}}{nU_t}\cosh\left(\frac{V_1 - V_2}{nU_t}\right) \approx \frac{I_{DC}}{nU_t}$$ [2]

$$Transconductance\ efficiency = 1/nU_t$$ [1]

[4]

c) Figure 1.2 shows a cascade of amplifiers where each stage uses the circuit from Figure 1.1. The total noise at the output is given by equation 2. The total stages M = 2 and the constant P = 1 for weak inversion operation. Also assume that the total noise contribution is due to the four input devices of the circuit of Figure 1.1 ($n_i = 4$) and the gain of each stage is given by $G_i = g_m R_{out}$, where g_m is the transconductance derived in question 1.b.ii and $R_{out} = 5\ M\Omega$.

i) Given the bias current I_{DC}=100nA, calculate the minimum area A_1 required by the first stage, such that the total contribution of the noise at the output from the first stage is less than 1mV. You may assume I_1 =100nA, $K_w = 1x10^{-30}\ V^2C$, $K_f = 3.5x10^{-21}\ Hz/F^2$, ΔF =100 Hz, f_h = 100Hz, f_l = 1Hz and the transconductance is constant over a given input voltage.

$$v_{no}^2 = \sum_{i=1}^{i=M} v_{ni}^2 G_i^2 = \sum_{i=1}^{i=M} \left(n_i \frac{K_w}{(I_i / n_i)^p} \cdot \Delta f + n_i \frac{K_f}{(A_i / n_i)} \cdot \ln\left(\frac{f_h}{f_l}\right) \right) G_i^2 \quad (2)$$

Solution:
I_{DC}=100nA
$g_m = I_{DC}/nU_t$ = 100nA/(1.23x0.026) =3.12 uS [1]
Voltage gain $G_1 = g_m R_{out}$ =3.12uS x 5 MΩ = 15.6
Input noise requirement for two stages: $V_{n1}^2 x G_1^2 < (1mV)^2$

$V_{n1}^2 < 4.109e\text{-}17\ V^2 < \left(n_i \frac{K_w}{(I_i / n_i)^p} \cdot \Delta f + n_i \frac{K_f}{(A_i / n_i)} \cdot \ln\left(\frac{f_h}{f_l}\right) \right)$

40.6e-10 V^2<1e-21 +1.61e-20/A
[2]
Solving for A_1 gives $A > 3.96e\text{-}12\ (m)^2$ [1]

[4]

ii) Propose suitable gate widths and lengths for transistors M1 and M2 for a typical 0.18um CMOS process.
Area for one transistor = 3.96e-12 /4=9.91e-13m^2
So suitable size of transistor =0.99umx0.99um

[2]

iii) Given that the system shown in Figure 1.2 operates on a Bluetooth signal at 2.4 GHz, but conveys audio information at 44 kHz, propose one method to reduce the power consumption requirements before quantizing the analogue signal.

[2]

Using a mixer you can downconvert the 2.4GHz signal to 44KHz. This will reduce the quantiser requirements from 4.8Gsamples/sec to just 88Ksamples/sec assuming we are sampling at nyquist. [2]

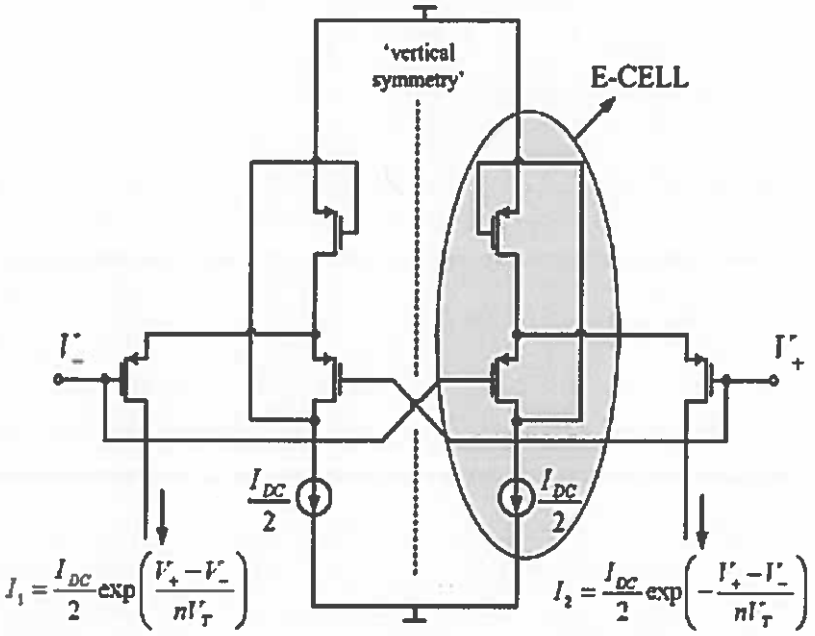


Figure 1.1

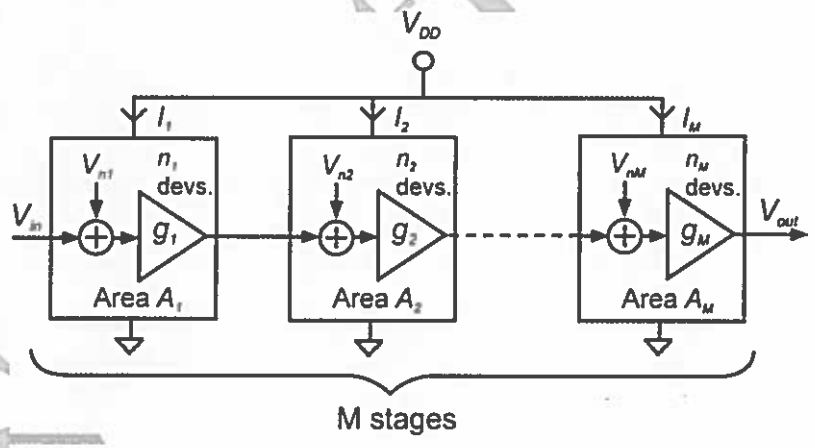


Figure 1.2

2. a) State and derive the translinear principle (TLP) for a loop of MOS transistors working in weak inversion.

[bookwork]

In a closed loop containing an even number of forward biased junctions, arranged so that there are an equal number of clockwise facing and counterclockwise facing polarities, the product of the current densities in the clockwise direction is equal to the product of the current densities in the counterclockwise direction.

[2 points for definition]

Number of Clockwise Junctions (Voltage Rises)=Number of Anticlockwise Junctions (Voltage drops)

$$\sum_{n\in CW} V_n = \sum_{n\in CCW} V_n$$

$$V_n = nU_T \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right)$$

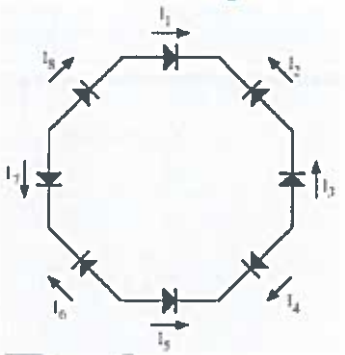
$$\sum_{n\in CW} nU_T \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right) = \sum_{n\in CCW} nU_T \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right)$$

$$\sum_{n\in CW} \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right) = \sum_{n\in CCW} \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right)$$

$$\prod_{n\in CW} \frac{I_n}{\lambda_n I_{DO}} = \prod_{n\in CCW} \frac{I_n}{\lambda_n I_{DO}}$$

$$\prod_{n\in CW} \frac{I_n}{\lambda_n} = I_{DO}^{CW-CCW} \prod_{n\in CCW} \frac{I_n}{\lambda_n}$$

$$\prod_{n\in CW} \frac{I_n}{\lambda_n} = \prod_{n\in CCW} \frac{I_n}{\lambda_n}$$

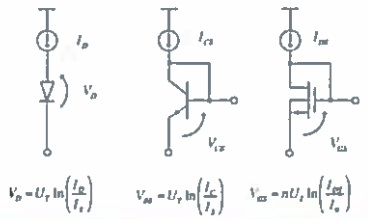


Assumptions: Temperature and saturation currents are all the same [2 points]

[4]

b) Draw three devices which could be used as tranlinear elements justifying your choices.

- The Diode
- The Bipolar Transistor
- The MOS transistor in weak inversion (NB: body effect)



[1 point for each]

[3]

c) Figure 2.1 shows a translinear circuit made up of NMOS transistors biased in weak inversion.

(i) Derive I_{out} as a function of X by applying the translinear principle. Show all necessary steps.

TLP 1: $(1+X)^2 I_0^2 = I_3 \cdot I_7$

TLP 2: $(1-X)^2 I_0^2 = I_4 \cdot I_7$

KCL A: $I_4 = 2 \cdot I_0 - I_3$

Rearranging: $I_7 = (1 + X^2) \cdot I_0$

KCL B: $I_{OUT} = X^2 \cdot I_0$

[4]

(ii) What is the function of the circuit shown in Figure 2.1 ?

This is an absolute circuit.

[1]

d) The equation for a vector normaliser circuit is given as:

$$u = \frac{x}{\sqrt{x^2 + y^2}}$$

Synthesise a translinear circuit to provide this function minimsing the circuit where possible. You may only use Type A cells.

Hint: The function may be decomposed into the functions $u = \frac{x}{r}$ and $r = \sqrt{x^2 + y^2}$.

(d) Equation must be synthesised:

Can treat as two separate equations: $r = \sqrt{x^2 + y^2}, u = \frac{x}{r}$

Represent each variable as a ratio of currents:

$$x = \frac{I_x}{I_1}, y = \frac{I_y}{I_1}, r = \frac{I_r}{I_1}, u = \frac{I_u}{I_1}$$

Substitute these into the original equations:

$$\frac{I_u}{I_1} = \frac{I_x/I_1}{I_r/I_1} \quad I_u I_r = I_x I_1$$

$$\frac{I_r}{I_1} = \sqrt{\left(\frac{I_x}{I_1}\right)^2 + \left(\frac{I_y}{I_1}\right)^2} \quad I_r^2 = I_x^2 + I_y^2$$

$$I_r = \underbrace{\frac{I_x^2}{I_r}}_{I_{r1}} + \underbrace{\frac{I_y^2}{I_r}}_{I_{r2}}$$

Derive the translinear circuits which need to be designed:

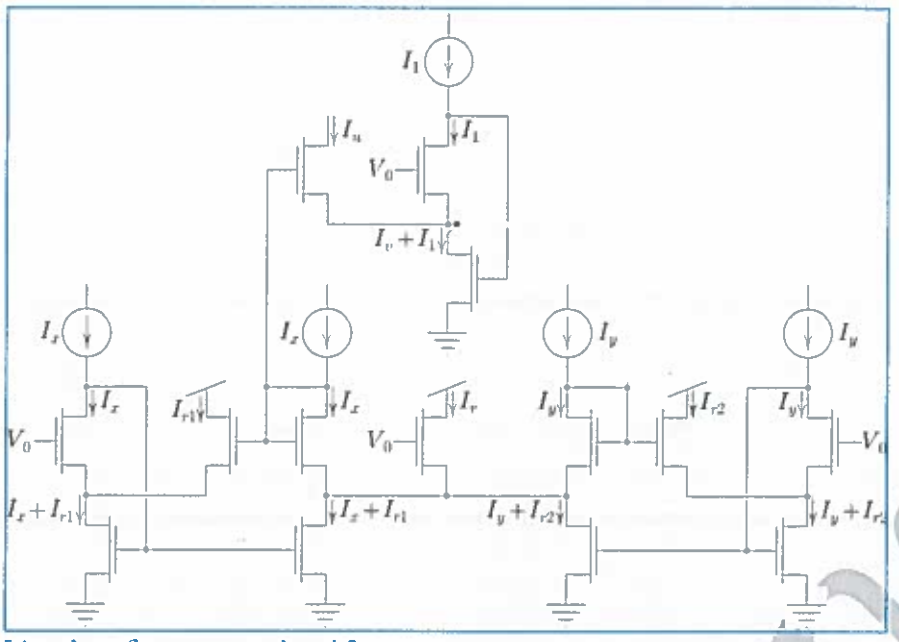
TLP: $I_{r1} I_r = I_x^2$

$I_{r2} I_r = I_y^2$

$I_u I_r = I_x I_1$

KCL: $I_r = I_{r1} + I_{r2}$ [4 points for definition of equations]

Final Circuit after removing redundant loops:



[4 points for correct circuit]

[8]

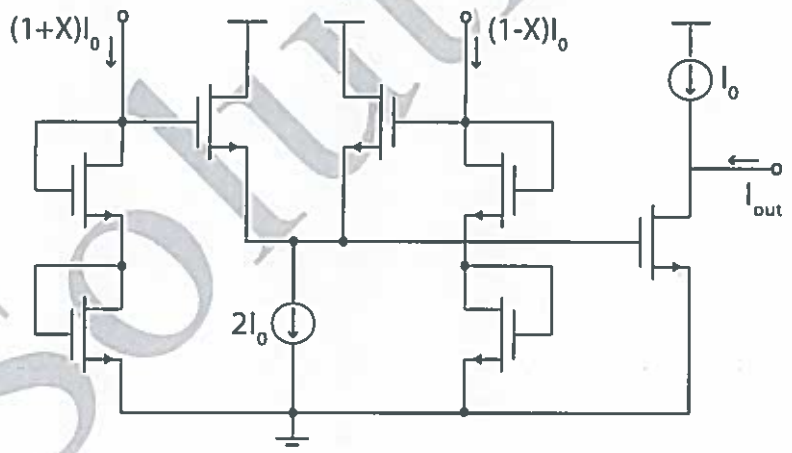


Figure 2.1

3. a) Explain the principle of companding, illustrating how the dynamic range changes through the signal processing chain.

[Bookwork]

Companding can increase the usuable dynamic range through compression of the input signal, processing in the non-linear domain and then expansion. Large signals get compressed, small signals get expanded above the noise floor of the filter resulting in an overall increase in usable dynamic range of a fixed dynamic range of the filter.

[4]

b) Figure 3.1 shows a block diagram of a current-mode integrator, with an input X and an output Y. f() and g() represent non-linear functions which compress and expand the signal such that input-output relationship of the integrator is linear and given by:

$$Y = \tau \int X \cdot dt$$

Given that the expansive function is defined as $g(V_c)=\beta(V_g-V_{th})^2$, derive the function f(x) such that linear integration is achieved. All constants should be grouped to represent a current I_0, with the function f(x) composed of just I_{in}, I_{out} and I_0.

[Derivation of new theory]

$$\frac{dY}{dt} = \tau X$$

$$\frac{dY}{dt} = \frac{d(g(V_C))}{dV_C} \cdot \frac{dV_C}{dt} = \frac{d(g(V_C))}{dV_C} \cdot \frac{I_C}{C} = \frac{d(g(V_C))}{dV_C} \cdot \frac{f(X)}{C}$$

$$\frac{d(g(V_C))}{dV_C} \cdot \frac{f(X)}{C} = \tau X$$

for linear integration.

$$Y = I_{out} = \beta(V_c - V_t)^2 = g(V_C)$$

$$\frac{dY}{dV_C} = \frac{I_{out}}{dV_C} = 2\beta(V_c - V_t) = 2\beta\frac{\sqrt{I_{out}}}{\sqrt{\beta}} = 2\sqrt{\beta I_{out}}$$

$$f(x) = I_C = X\tau C\left(\frac{dY}{dV_C}\right)^{-1} = I_{in}\tau C / 2\sqrt{\beta I_{out}} = I_{in}\sqrt{\frac{I_0}{I_{out}}}$$

$$I_0 = \left(\frac{\tau C}{2\sqrt{\beta}}\right)^2$$

or alternate solution which is acceptable.

$$f(x) = I_{in}\frac{I_0}{\sqrt{I_{out}}}$$

with $I_0 = \left(\frac{\tau C}{2\sqrt{\beta}}\right)$

[6]

c) The transfer function of an oscillator may be defined in state space representation by the following equations:

$$\dot{X}_1 = -\omega_0 X_1 + \omega_0 X_2$$

$$\dot{X}_2 = -2\omega_0 X_1 + \omega_0 X_2 + \omega_0 U$$

$$Y = X_1$$

where Y is the output, U is the input and X_1 and X_2 are the states.

(i) By using the mappings below show how these linear equations can be mapped to non-linear log-domain design equations. You may use the following mapping for constant currents, $I_1 = I_2 = I_\omega$ and $I_U = I_O$.

$$X_1 = I_1 \exp\left(\frac{V_1}{nU_t}\right) \qquad X_2 = I_2 \exp\left(\frac{V_2}{nU_t}\right) \qquad U = I_U \exp\left(\frac{V_U}{nU_t}\right)$$

Appliction of taught methodology.
Should apply state space mapping and derive the following KCL equations:

$$C\dot{V}_1 = -I_\omega + I_\omega \exp\left(\frac{V_2 - V_1}{nU_t}\right)$$

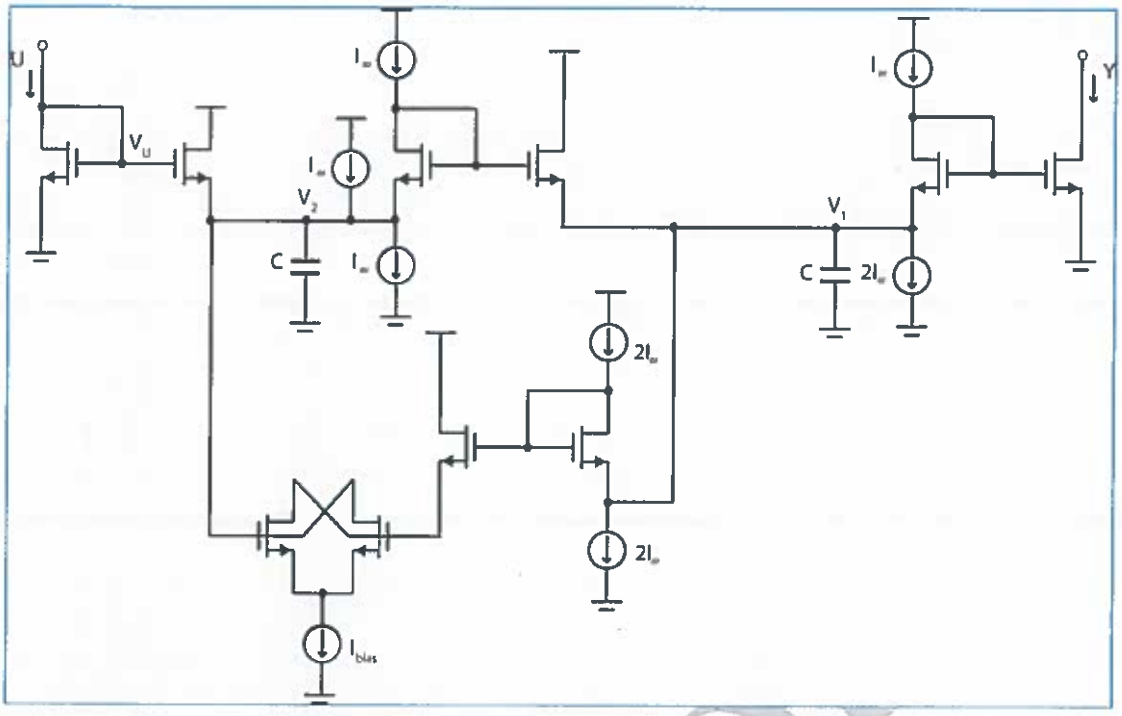
$$C\dot{V}_2 = -2I_\omega \exp\left(\frac{V_1 - V_2}{nU_t}\right) + I_\omega + I_0 \exp\left(\frac{V_U - V_2}{nU_t}\right)$$

$$Y = I_\omega \exp\left(\frac{V_1}{nU_t}\right)$$

[5]

(ii) With these log-domain design equations, sketch a schematic of the final log domain filter using weak inversion MOS transistors.

Drawing of log domain circuit.



[5]

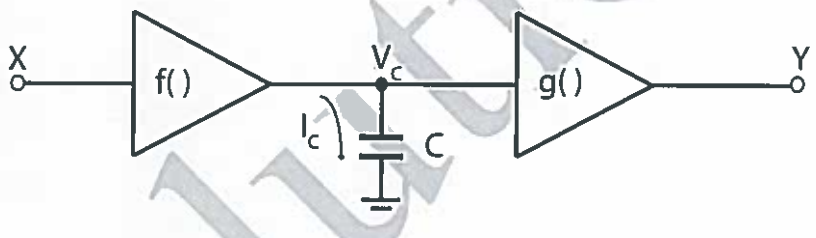


Figure 3.1

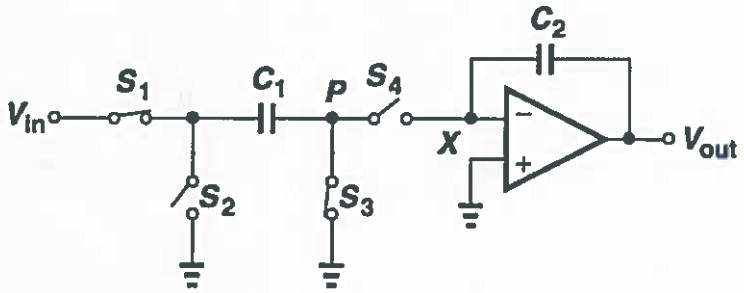
4. This question relates to discreet time integrators.

a) Figure 4.1 shows a continuous time integrator.

i) Draw the circuit of a switch capacitor equivalent which compensates for voltage dependent parasitic capacitances and explain its operation.

[Bookwork]
Switched Capacitor Integrator

- S3 turns OFF first, it introduces only a constant offset, which can be suppressed by differential operation.
- Charge injection or absorption of S1 and S2 contributes no error because the left plate of C1 is "driven".
- Since node X is a virtual ground, the charge injected or absorbed by S4 is constant and independent of Vin.
- The nonlinear junction capacitance of S3 and S4 is reduced by switching from ground to virtual ground. [2 points for explanation]



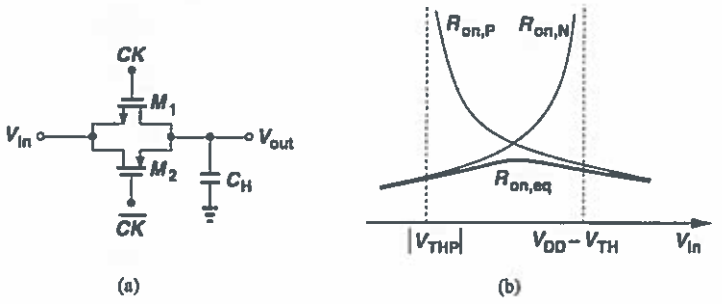
[2 points for circuit diagram]

[4]

ii) For the switches used in your circuit, which configuration leads to the highest speed performance? You are required to prove your answer by deriving the equivalent resistance of the switches.

[Bookwork plus derivation from theory]

- Complementary Switch
- Combine the two in a complementary form.
- Constant low Resistance, Ron,eq which is good for high speed.
- Independent of input voltage



[2 points]

$$R_{on,eq} = R_{on,N} \| R_{on,P}$$

$$= \frac{1}{\mu_n C_{ox}(\frac{W}{L})_N (V_{DD} - V_{in} - V_{THN})} \| \frac{1}{\mu_n C_{ox}(\frac{W}{L})_P (V_{in} - |V_{THP}|)}$$

$$= \frac{1}{\mu_n C_{ox}(\frac{W}{L})_N (V_{DD} - V_{THN}) + [\mu_n C_{ox}(\frac{W}{L})_N - \mu_p C_{ox}(\frac{W}{L})_P] V_{in} - \mu_p C_{ox}(\frac{W}{L})_P V_{THP}}$$

- Interestingly we can cancel out input dependent terms if:

$$\mu_n C_{ox}(W/L) = \mu_p C_{ox}(W/L)$$

[2 points]

[4]

b) Figure 4.2 shows an auto-zeroing switched capacitor integrator capable of removing any offset in the amplifier. Derive the output voltage of the integrator during phase Φ_1 and Φ_2 indicating how the offset is removed by showing the charge on each capacitor during each phase.

[Derivation from notes]
Student should conclude to the following equations showing at each phase how the offset V_{os} gets subtracted.

$$v_{out}^{\Phi 2}(n) = v_{out}^{\Phi 2}(n-1) - (C_1/C_2) v_{in}^{\Phi 2}(n)$$

$$v_{out}^{\Phi 1}(n) = v_{out}^{\Phi 2}(n) + v_{os}$$

[5]

c) Figure 4.3 shows a schematic of switched current integrator.

i) Derive the transfer function of the switched current integrator and show that in the z-domain this may be represented as H(z) = A/(z-1).

Analysis

- On phase Φ2 of clock period (n-1)
- I2(n-1)=2IB+Iin(n-1)-I1(n-1)
- where I1(n-1)=(AIB-I0(n-1))/A =IB-I0(n-1)/A
- Therefore: I2(n-1)=IB+Iin(n-1)+I0(n-1)/A

- On phase Φ1 of clock period (n)
- I1(n)=2IB-I2(n-1)=IB-Iin(n-1)-I0(n-1)/A
- I3(n)=AI1(n)=AIB-I0(n)
- I1(n)=IB-I0(n)/A
- Therefore I0(n)=AIin(n-1)+I0(n-1)

- Taking Z transform gives: I0=Aiin(z-1)+I0(z-1)
- H(z)=(Io/Iin)=Az-1/(1-z-1)=A/(z-1)
- z=exp(jωT)≈(1+jωT) when ωT<<1 where T is the clock period.
- Therefore H(z) ≈A/jωT
- This is a lossless integrator !
- Time constant of which is τ=T/A=1/fcA

[5]

ii) Explain one limitation of the switched current technique that doesn't exist in its voltage mode equivalent.

VDS variations of memory transistors are an issue causing mismatch, need to be compensated [2].

[2]

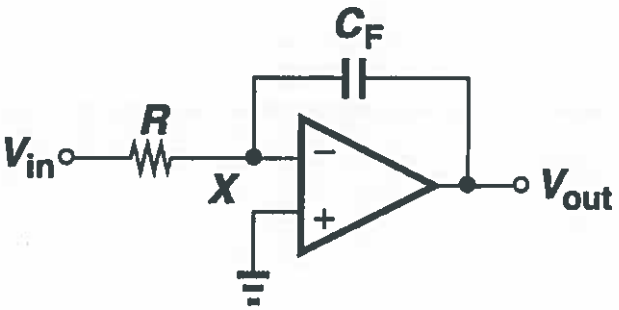


Figure 4.1

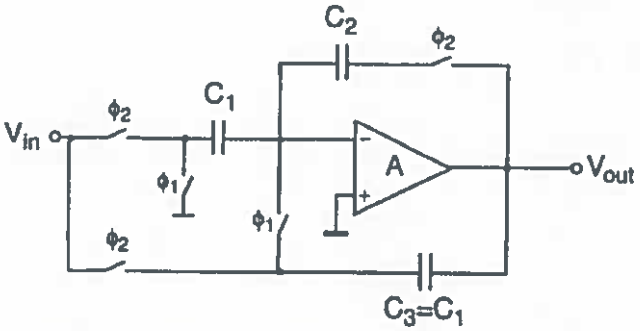


Figure 4.2

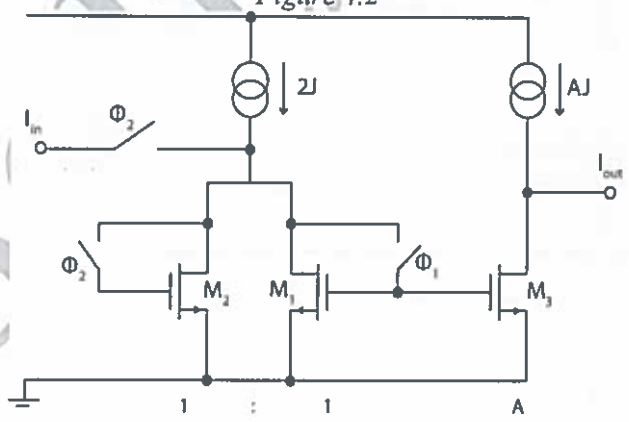


Figure 4.3

5. Figure 5.1 shows an amplifier channel used to measure biomedical signals.

a) Explain one method to make the input signals V_{sig1} and V_{sig2} immune to 1/f noise in the operational amplifier, and draw a block diagram of this method illustrating how the frequency spectrum of the signal changes during each stage.

[bookwork]

Student needs to identify that chopping can be used and explain the principle of chopper stabilization with the following diagrams.

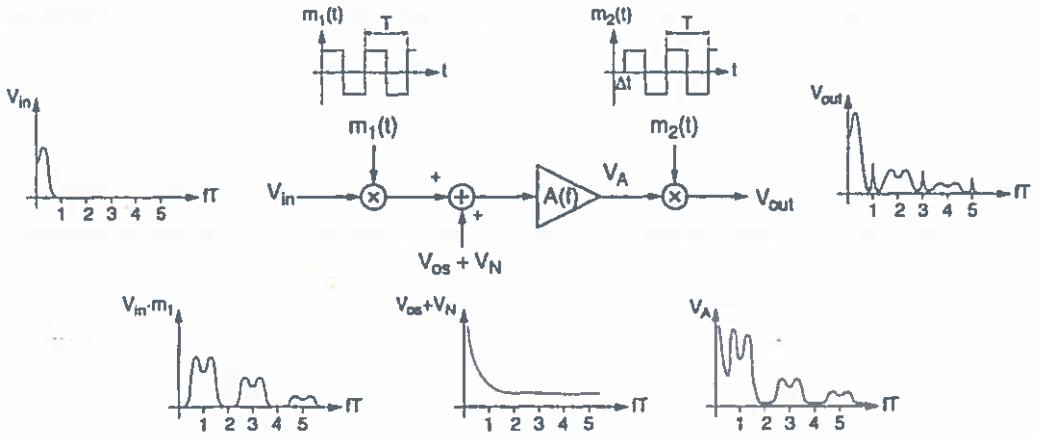


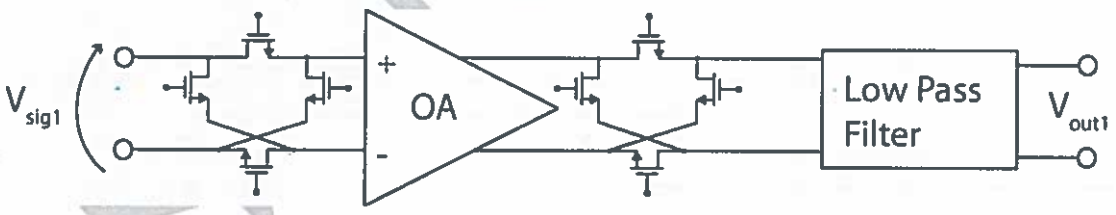
Fig. 9. The chopper amplification principle [19].

[5]

b) Draw a schematic of a suitable front end for this system using the method described in 5.a. You may use the OA symbol as in Figure 5.1 and do not need to show the schematics of this amplifier.

[Application of theory].

Student needs to add chopping switches in input and output and low pass filter block.

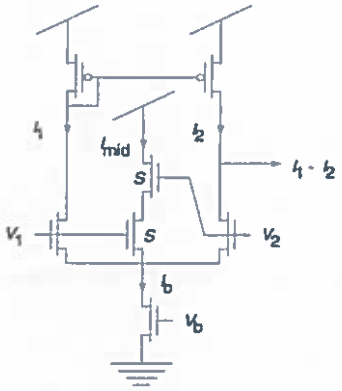


[4]

c) The system in Figure 5.1 uses a V/I converter with improved linearity over a conventional differential pair. Sketch a suitable schematic for the V/I converter explaining why the linearity is greater than the standard differential pair.

[Application of Known Theory]

V/I = Bump transconductor which improves linear range by 2/3 by effectively stealing current from the differential pair in the linear range.

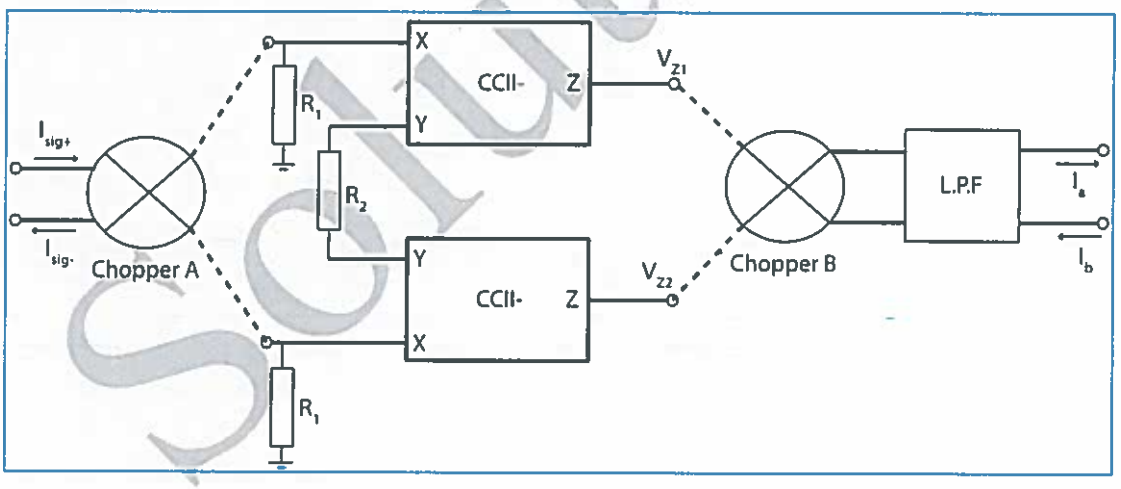


[5]

d) Figure 5.1 is used as part of a system shown in Figure 5.2 which should measure both the voltage and the current using the method described in 5.a. Sketch a suitable circuit using current conveyors which is able to measure differentially input signals I_{sig1} and I_{sig2} and provide a differential output current $I_{out2} = I_a - I_b$ and be immune to 1/f noise of the current conveyor. You are required to explain the operation of the circuit which your draw.

[Design of new circuit]
Use current conveyor instrumentation amplifiers with current gain determined by resistors R1&R2. Using chopping of currents will still perform the same effect as the current conveyors allow bi-directional currents.

[6]



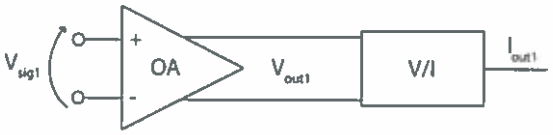


Figure 5.1

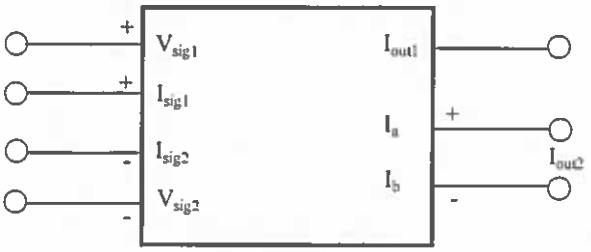
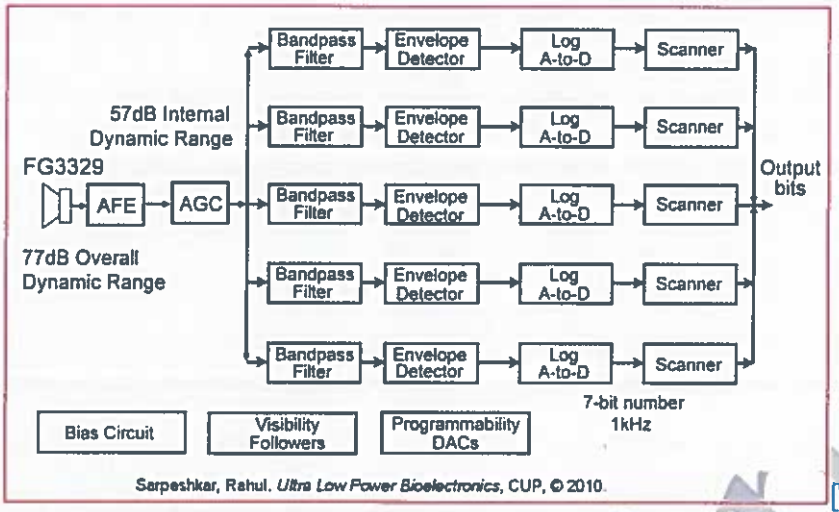


Figure 5.2

6.

a. Sketch the block level architecture of a fully implantable cochlear prosthesis chip and explain the functions of each of the blocks shown in your figure.

From notes:



[5]

- The **Audio Front End** (AFE) feeds audio signals to the **Automatic Gain Control** (AGC) circuit which compresses 80dB of audio to a 60dB electrical signal.
- The output of the AGC is fed to a bank of sixteen spectral-analysis channels that span the audio spectrum.
- Each channel consists of:
  - A **band pass filter** for that frequency.
  - A **envelope detector** to extract the spectral energy.
  - A **logarithmic ADC** to logarithmically compress the spectral energy to 7 bits.
  - A **scanner** which loads the parallel bits onto a serial bus to be sent to stimulator.
  - A **stimulator** which works based on continuous interleaved sampling (CIS) [5]

[Total 10 points]

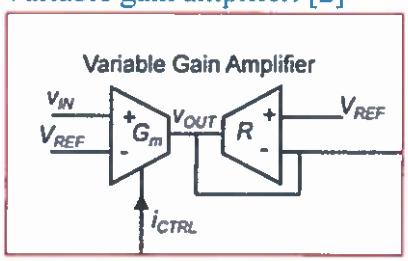
[10]

b. Figure 6.1 shows and automatic gain control system (AGC) typically used in cochlear prosthesis. The rectifier uses a current conveyor to convert the voltage V_{out} to a rectified current. The signals that follow, i_{REC}, i_{ED}, a_f and i_{GAIN} are all based on current mode operation. The translinear controller implements a square root operation $y = \sqrt{x}$. Sketch the full circuit schematic of the AGC stating assumptions where necessary. The varible gain amplifier does not need a transistor level schematic.

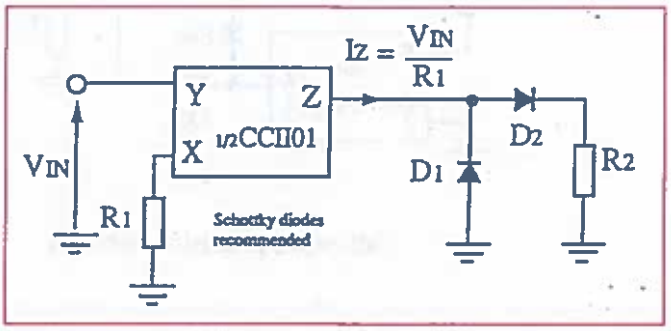
[10]

A connection of the following blocks from the notes:

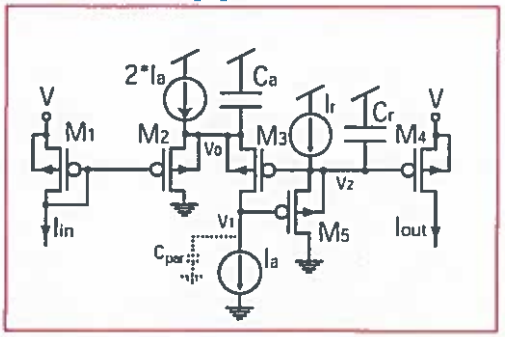
Variable gain amplfier: [2]



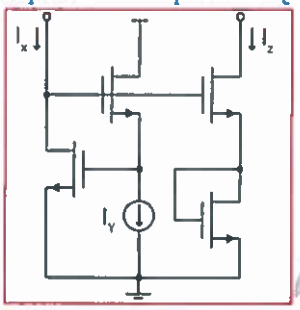
Rectifier: [2]



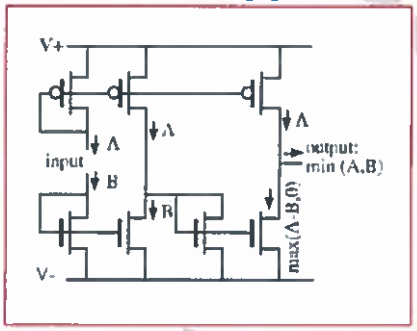
Peak detector: [2]



Square root operator: [2]



Minimum Circuit: [2]



[Total 10 points]

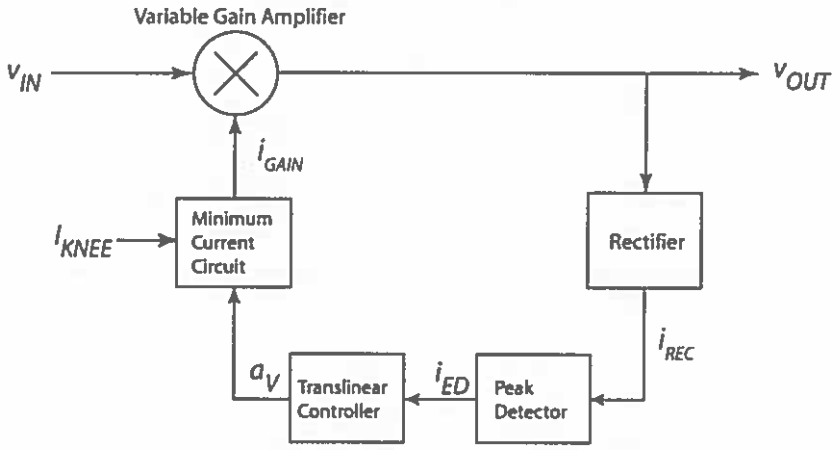


Figure 6.1: Automatic gain control system.