UNIVERSITY OF LONDON

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 1999

BEng Honours Degree in Computing Part II
MEng Honours Degrees in Computing Part II
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER 2.4

ARCHITECTURE II

Friday, May 14th 1999, 2.00 – 3.30

Answer THREE questions

For admin. only:
paper contains 4 questions

1a Given that the variables X, Y and Z are placed in main memory, provide the instruction sequence implementing the statement Z=X+Y for each of the following architectures:

load-store architecture, with n general-purpose registers (n>2),

accumulator architecture,

stack architecture,

memory-memory architecture.

b The instruction sets of four machines, each adopting one of the architectures in part a, have the same opcode size of α bytes, the same memory address size of β bytes, and that all data operands are of γ bytes, where α, β and γ are integers. All instructions are an integral number of bytes in length, and there are 16 registers in the load-store architecture. There are no optimisations to reduce memory traffic, and all variables are placed initially in memory. Provide the instruction code sequence for the program fragment:

$$\begin{aligned} X &= X+Z \\ Y &= X-Y \end{aligned}$$

for each of the 4 architectures, and calculate the code size and the data size for each of the 4 machines.

The two parts carry, respectively, 40% and 60% of the marks.

2 A barrel shifter can be used to shift its data input by an amount given by its control input.

a Provide the circuit diagram of a barrel shifter with 3-bit data input, 7-bit control input and 5-bit output, using a rectangular array of 15 multiplexors. Only one bit of the control input will be high at any time; the 7 possible control input configurations correspond to left shift or right shift from 0 up to 3 places. One or more zeroes will be introduced when the input is shifted for one or more places to the left or right. Label the input data, control input and output values on your circuit diagram, given that the control input is 0000010.

b Show how the 7 possible control input configurations for the barrel shifter in part a can be modified to implement circular shifting, such that the bit or bits "dropped off" from the left will appear on the right, and vice versa. Label the input data, control input and data output on your circuit diagram, given that the control input is 1000010.

c Show how a decoder with a 3-bit input and 7-bit output can be connected to the control input of the barrel shifter in part a, so that the input 000 corresponds to no shift, and 001, 010 and 011 correspond respectively to shifting left 1-3 places, and 111, 110 and 101 correspond respectively to shifting right 1-3 places.

The three parts carry, respectively, 35%, 35%, and 30% of the marks.

[Turn over...

3a Provide the diagram of a 5-bit combinational circuit for implementing the unsigned divide-by-two operation. Label the input and output values on the diagram when the input to this circuit is 01100 (12 in base ten).

b Consider a combinational circuit for implementing a restricted version of a divide-by-three operation, which accepts a 3-bit unsigned number and produces a 1-bit quotient and a 2-bit remainder.

i) Provide the truth table for this circuit, and explain why some input combinations will lead to "don't care" results.

ii) Provide the optimised Boolean equations for the 3 outputs in terms of the 3 inputs.

c The combinational circuit in part b can be used as a repeating unit for an N-bit divide-by-three circuit, by connecting the remainder outputs of one circuit to two of the 3 inputs of another. Draw a circuit diagram of a 3-bit divide-by-three circuit constructed this way, and label the values on the internal and output wires when the input is 111.

The three parts carry, respectively, 20%, 40%, and 40% of the marks.

4a Draw a diagram illustrating how a v-bit virtual address, with an m-bit page offset, is translated by the entries of a page table into a u-bit physical address. Label the following on the diagram: virtual page number, physical page number, page table register.

i) What is the size of each page?

ii) How many entries are there in the page table?

b A two-level page table scheme is adopted for a v-bit virtual address, m-bit page offset and 2^n bytes per page table entry. The virtual page number is divided into two parts: a p-bit page table number, and a q-bit page table offset. The page table number is used to index a first-level page table that provides the physical address for a second-level page table. Both the first- and second-level page tables are in main memory, and the second-level page table occupies exactly one page of memory. The page table offset is used to index into the physical page number.

i) Express q in terms of m and n.

ii) Given that exactly one second-level page table is in memory and a fraction α of its entries are valid, how many bytes of memory in the virtual address space reside in physical memory?

iii) Express p in terms of m, n and v, and compute the number of bytes each program needs to use to store the first-level page table.

The two parts carry, respectively, 40% and 60% of the marks.

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