Final

E4.16
AO5

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2010

MSc and EEE PART IV: MEng and ACGI

CURRENT-MODE ANALOGUE SIGNAL PROCESSING

Monday, 10 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s) :	C. Papavassiliou
	Second Marker(s) :	K. Fobelets

The Questions

1.

a) Define the CCII+ current conveyor.

i) State which terminal voltages/currents are inputs and which are outputs.

ii) Write relations between the inputs and the outputs.

iii) Comment on the design challenges these definitions present.

iv) Comment on the ways such challenges are met.

v) What is the maximum power gain of a CCII+ device?

Make sure to clearly indicate the polarities of voltages and currents in your answers.

[5]

b) Draw schematic diagrams of implementations of the following building blocks using CCII+ current conveyors and passive (R,L,C) components. Indicate inputs and outputs. Assume that bipolar transistors of cut-off frequency f_T are used to implement the CCII+ devices. Estimate the maximum value the first pole frequency for each of these blocks can take.

i) Current Mirror

ii) Voltage follower

iii) Inverting current Mirror

iv) Inverting unity gain voltage amplifier

v) Lossy inverting current integrator with the pole at $f << f_T$

[15]

2.

a)

i) State the static translinear principle for circuits containing bipolar transistors.

[2]

ii) List all the necessary conditions for the translinear equations to be valid.

[3]

iii) Draw schematics of the two basic types of translinear loops.

[2]

iv) Discuss sources of error in a practical implementation of translinear circuits.

[3]

b) Design a translinear circuit that calculates the negative of the cube root of a single ended current entering the circuit. Your design should be complete, and include any necessary voltage and current sources. Write an equation which includes any biasing current sources.

HINT: The output should exit the circuit.

[10]

3.

a) Draw the schematic diagram of a "Bernoulli cell", i.e. a first order open loop log domain filter. Clearly label inputs, outputs and biasing sources.

[5]

b) Write the static translinear equation for this circuit in terms of inputs, outputs and any biasing current sources that appear in the circuit.

[5]

c) Assume the currents appearing in the equation of part (b) are time varying. By relating the capacitor voltage to the output current and taking the Laplace transform of the resulting differential equation derive the transfer function of this circuit.

[5]

c) Evaluate the pole frequency of this circuit if all the transistors are identical and no explicit capacitor is used (i.e. only the base-emitter capacitances of the transistors play a role). The transit frequency, f_T, of the transistors is given and is assumed to be proportional to the collector current.

[5]

4.

a) Draw a block diagram for a current feedback op-amp. Identify inputs and outputs.
[5]

b) Draw a transistor level schematic of a simple transistor circuit which can function as a current feedback op-amp. Refine your model in part (a). Assume that all voltage followers in the block diagram of part (a) are implemented by NPN common collector followers biased at a collector bias current I_C, and any current mirrors are made of PNP transistors. Provide any necessary bias sources so the circuit operates in class A.
[5]

c) A Current feedback op-amp is given with the following transimpedance function:

$$Z_T = \frac{Z_0}{(1+s\tau_1)(1+s\tau_2)}$$

where $Z_0 = 1$ V/μA , $\tau_1 = 159$ ns, $\tau_2 = 1.59$ ns , and current input impedance $Z_n = 100\ \Omega$.

Calculate symbolically the closed loop transfer function of a non-inverting amplifier built using this CFOA. Make any reasonable approximations arising from the numbers given.

HINT: A Tee-Pi transformation in the feedback network can idealise the problem.
[5]

d) Choose the values of external resistors for a voltage gain of 2 and a critically damped response.
[5]

5.

a) List the three modes of circuit operation and their characteristics. Comment on signal sources and sinks used in each mode, frequency of, bandwidth and power dissipation of each mode of circuit operation.

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b) With the aid of an equivalent circuit diagram, explain why a common base amplifier has a higher bandwidth than a common emitter amplifier of the same voltage gain. How does the power gain of the common base amplifier compare to the power gain of the common emitter amplifier of the same voltage gain?

[5]

c) Define the incidence matrix of a circuit and list its uses.

[5]

d) Write the rules that can be used to convert a given circuit into its adjoint. Use these rules to construct a current mode first order RC high pass filter from the well known voltage mode circuit.

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6. An infinite impulse response (IIR) discrete time filter of order K, with input x and output y, has a transfer function given by:

$$y_n = \sum_{k=0}^{K} a_k x_{n-k} - \sum_{k=1}^{K} b_k y_{n-k}$$

a) Write this expression in terms of unit delays (i.e. in z-transform form) and factor it so that only K delay elements are used. Draw a block diagram which implements the form you derived.

[5]

b) Draw schematic diagrams of switched current circuits which can be used to implement an inverting and a non-inverting unit delay. Estimate the maximum switching frequency that can be used so that the settling error of this cell is smaller than 0.1%. The MOSFETs provided by the fabrication process have f_T=5GHz, threshold V_T=0.5V, transconductance parameter $K = 10\mu A/V^2$ and Early voltage V_A=10V. The power supply will be 2.5V .

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c) Design a switched current "branching element" cell which for a given input generates two outputs each equal to half the input. Discuss the effect of transistor mismatch. Show how this branching cell can be used to generate filter coefficients for a switched current filter. How many clock phases are required to specify a coefficient to 0.1% ?

HINT: Think of the binary representation of a number!

[5]

d) Estimate the number of transistors required to implement a general 2nd order filter, and the maximum signal frequency this filter can handle. All sources of error must be constrained to less than 0.1%. Transistor specifications are as in part (c).

[5]

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The ANSWERS 2010

1.

a) Define the CCII+ current conveyor. State which terminal voltages/currents are inputs and which are outputs. Write relations between the inputs and the outputs. Comment on the design challenges these definitions present. What is the maximum power gain of a CCII+ device?

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ii) Voltage follower

iii) Inverting current Mirror

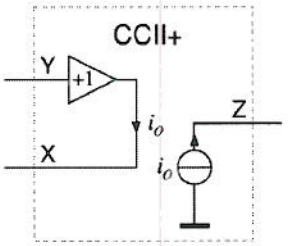
iv) Inverting unity gain voltage amplifier

v) Lossy inverting current integrator with the pole at $f << f_T$

[15]

ANSWER QUESTION 1:

a)(Bookwork)



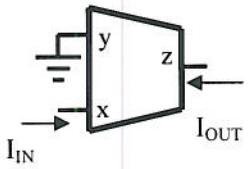
Definitions : $V_x = V_y$, $i_z = i_x$, $i_y = 0$

This definition requires a frequency independent voltage follower and an ideal unity gain and frequency independent current follower. Both are ideal amplifiers of infinite available power gain. The ideally vanishing port impedance at x is usually approximated by use of positive feedback.

[5]

b) A mixture of known and unknown examples, and some interpretation.

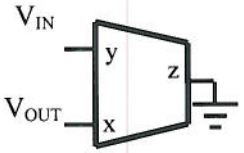
i) Current mirror:



This will have a pole at most at $f_T / 2$

[3]

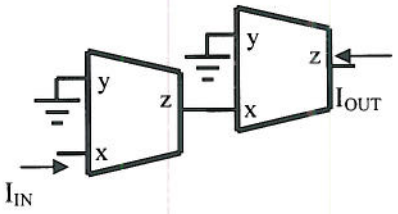
ii) Voltage follower



This will have a pole at most at f_T

[3]

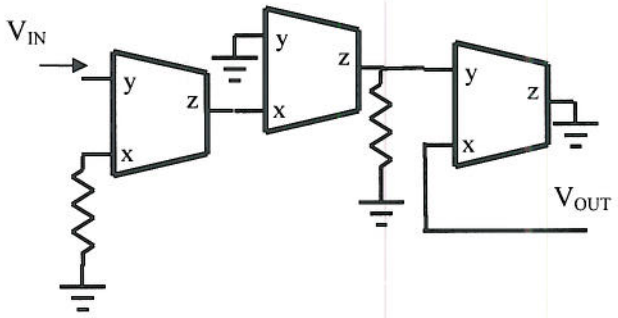
iii) Inverting current Mirror



This will have a pole at most at $f_T / 4$

[3]

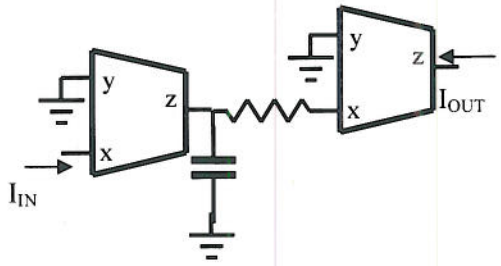
iv) Inverting voltage amplifier. For unity gain the resistors are equal



This will have a pole at most at $f_T / 4$

[3]

v) Lossy inverting integrator



The pole is RC.

[3]

2.

a) State the static translinear principle for circuits containing bipolar transistors. List all the necessary conditions for the translinear equations to be valid. Draw schematics of the two basic types of translinear loops. Discuss sources of error in a practical implementation of translinear circuits.

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b) Design a translinear circuit that calculates the negative of the cube root of a single ended current entering the circuit. Your design should be complete, and include any necessary voltage and current sources. Write an equation which includes any biasing current sources.

HINT: The output should exit the circuit

[10]

ANSWER QUESTION 2.

a) (bookwork)

In a loop consisting of number of bipolar base-emitter junctions, some arranged "clockwise" and some "counter-clockwise", the transistor collector currents satisfy: $\prod_{CW} \frac{I_k}{A_k} = \prod_{CCW} \frac{I_k}{A_k}$ .This equation is valid provided:

i) the number of CW junctions is equal to the number of CCW junctions

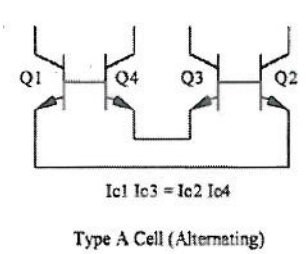
ii) the number of CW npn transistors is equal to the number of CCW npn transistors

iii) the number of CW pnp transistors is equal to the number of CCW pnp transistors

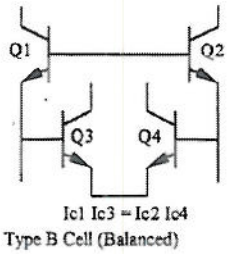
iv) All transistors are at the same temperature (i.e. have the same average power dissipation)

Sources of error: Temperature diffrences, collector voltage diffrences and variation (through the finite collector conductance), beta error.

The two basic types of translinear loops are the balanced and the alternating cells:



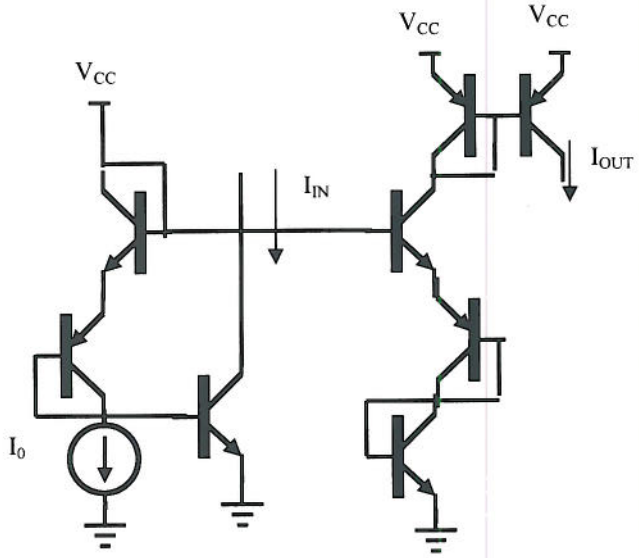
Type A Cell (Alternating)



Type B Cell (Balanced)

[10]

b) [new design exercise] $I_{out}^3 = I_{in} I_0^2$, all transistors of same size.



[10]

3.

a) Draw the schematic diagram of a "Bernoulli cell", i.e. a first order open loop log domain filter. Clearly label inputs, outputs and biasing sources.

[5]

b) Write the static translinear equation for this circuit in terms of inputs, outputs and any biasing current sources that appear in the circuit.

[5]

c) Assume the currents appearing in the equation of part (b) are time varying. By relating the capacitor voltage to the output current and taking the Laplace transform of the resulting differential equation derive the transfer function of this circuit.

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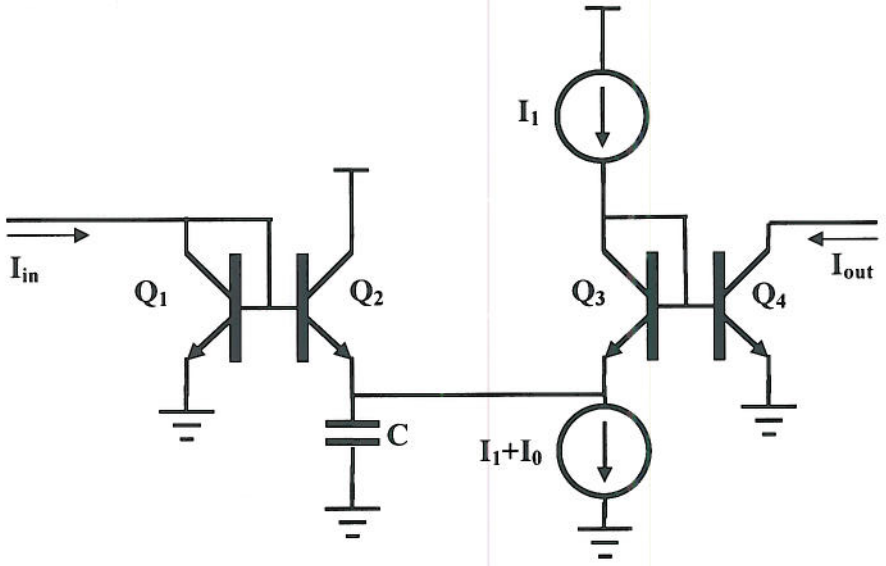
c) Evaluate the pole frequency of this circuit if all the transistors are identical and no explicit capacitor is used. (i.e. only the base-emitter capacitances of the transistors play a role). The transit frequency, f_T of the transistors is given, and is assumed to be proportional to the collector current.

[5]

ANSWER QUESTION 3

a)[alternative derivation of known theory]



[5]

b) Statically this is an alternating loop, so:

$$I_{C1}I_{C3} = I_{C2}I_{C4} \Rightarrow I_{in}I_1 = I_0 I_{out}$$

[5]

c) The key here is to realise that $I_{C2} = I_0 + C\dot{V}_C \Rightarrow \dot{I}_{C2} = C\ddot{V}_C$

and also that $I_{out} = I_1 \exp\left(V_C / V_{th}\right) \Rightarrow V_C = V_{th} \ln\left(\frac{I_{out}}{I_1}\right)$

$$I_{in}I_1 = \left(I_0 + C\dot{V}_C\right)I_{out} = \left(I_0 + CV_{th}\frac{\dot{I}_{out}}{I_{out}}\right)I_{out} \Rightarrow \frac{I_1}{I_0}I_{in} = I_{out} + \frac{CV_{th}}{I_0}\dot{I}_{out} \Rightarrow I_{out}(s) = \frac{I_1}{I_0}\frac{1}{1+s\tau}I_{in}$$

$$\tau = \frac{CV_{th}}{I_0}$$

[5]

d) [computed example]

If there is no explicit capacitor, and f_T is independent of frequency, then C_{BE} is constant and the total capacitance at the integrating node is just C_{BE} (two series combinations of two such capacitors in parallel)

Then $\tau = \frac{CV_{th}}{I_0} = \frac{C_{BE}V_{th}}{I_0} = \frac{1}{\omega_{TQ2}}$

[5]

4.

a) Draw a block diagram for a current feedback op-amp, identifying its inputs and outputs.

[5]

b) Draw a transistor level schematic of a simple transistor circuit which can function as a current feedback op-amp. Refine your model in part (a) Assume that all voltage followers in the block diagram of part (a) are implemented by NPN common collector followers biased at a collector bias current I_C, and any current mirrors are made of PNP transistors. Provide any necessary bias sources so the circuit operates in class A.

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c) A Current feedback op-amp is given with the following transimpedance function:

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where $Z_0 = 1\ \text{V/}\mu\text{A}$, $\tau_1 = 159\ \text{ns}$, $\tau_2 = 1.59\ \text{ns}$, and current input impedance $Z_n = 100\ \Omega$.

Calculate symbolically the closed loop transfer function of a non-inverting amplifier built using this CFOA. Make any reasonable approximations arising from the numbers given.

HINT: A Tee-Pi transformation in the feedback network can idealise the problem.

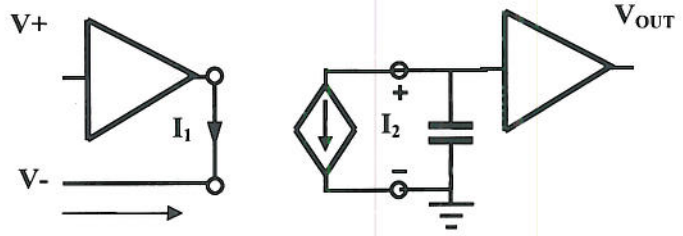
[5]

d) Chose the values of external resistors for a voltage gain of 2 and a critically damped response.

[5]

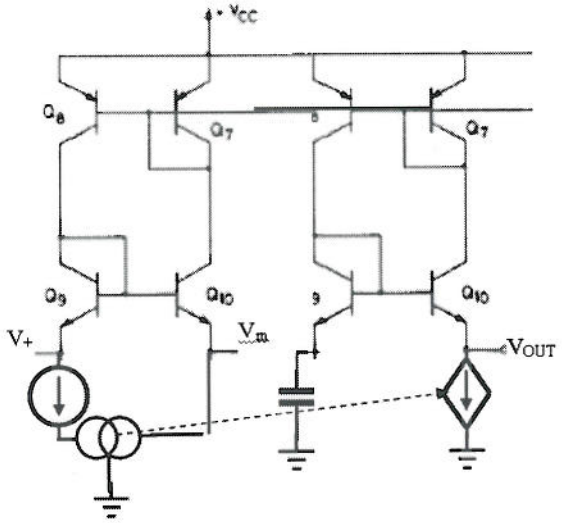
ANSWER QUESTION 4

a) [bookwork]



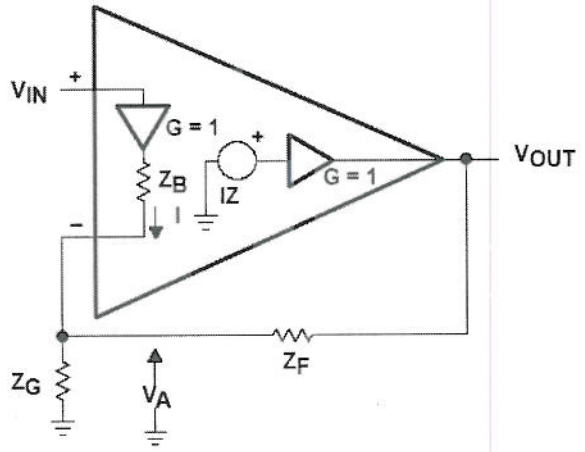
[5]

b) [interpretation of known theory]



[5]

c) [computed example]



Current input resistor can be taken out by a Tee-Pi transformation as hinted.
then

$$R'_G = \frac{Z_B Z_G + Z_B Z_F + Z_F Z_G}{Z_F},$$

$$R'_F = \frac{Z_B Z_G + Z_B Z_F + Z_F Z_G}{Z_G}$$

The third side of the Pi is a load from output to ground.

Now we have the ideal CFOA problem to solve with R'_G, R'_F

The forward path is given, it is the transimpedance. The reverse path transconductance is

$$g_R = \frac{1}{R'_F}$$

The closed loop voltage gain is

$$\frac{V_{out}}{V_{in}} = \frac{R'_G + R'_F}{R'_G R'_F} \frac{Z_T}{1 + Z_T g_R} = \frac{R'_G + R'_F}{R'_G R'_F} \frac{Z_0}{(1 + s\tau_1)(1 + s\tau_2) + Z_0 / R'_F} =$$

$$= \frac{R'_G + R'_F}{R'_G R'_F} \frac{Z_0}{K} \frac{1}{s^2 \tau_1 \tau_2 / K + s(\tau_1 + \tau_2)/K + 1}$$

$$K = 1 + Z_0 / R'_F$$

$$\omega_0 = \sqrt{\frac{K}{\tau_1 \tau_2}}, \zeta = \frac{1}{2}\sqrt{\frac{1}{K}} \frac{\tau_1 + \tau_2}{\sqrt{\tau_1 \tau_2}} \Rightarrow Q = \frac{\sqrt{K}}{\sqrt{\frac{\tau_1}{\tau_2}} + \sqrt{\frac{\tau_2}{\tau_1}}}$$

[5]

d) [computed example]

We are given $\tau_1 / \tau_2 = 100, \Rightarrow Q = \sqrt{K}/10$.

For critical damping $Q = 1/2 \Rightarrow K = 25$.

$$K = 1 + Z_0 / R'_F \Rightarrow R_F = \frac{Z_0}{K - 1} = \frac{10^6}{24} = 41.7 k\Omega$$

The low frequency gain is:

$$G_0 = \frac{R'_G + R'_F}{R'_G R'_F} \frac{Z_0}{K} = \frac{R'_G}{R'_G} \frac{25}{24} = 2 \Rightarrow \frac{R'_G + R'_F}{R'_G} = \frac{48}{25} \Rightarrow R'_G = \frac{25}{23} R'_F = 45.3 k\Omega$$

[5]

5.

a) List the three modes of circuit operation and their characteristics, including types of signal sources and signal sinks, frequencies where they are used, bandwidth and power dissipation.

[5]

b) With the aid of an equivalent circuit diagram, explain why a common base amplifier has a higher bandwidth than a common emitter amplifier of the same voltage gain. How does the power gain of the common base amplifier compare to the power gain of the common emitter amplifier of the same voltage gain?

[5]

c) Define the immitance matrix of a circuit. What can the incidence matrix be used for?

[5]

d) Write the rules that can be used to convert a given circuit into its adjoint. Use these rules to construct a current mode first order RC high pass filter from the well known voltage mode circuit.

[5]

ANSWERS QUESTION 5

a) [bookwork]

- Voltage mode:
  - All signals encoded as time dependent voltages
  - Currents are incidental
  - Basic representation is admittances:
  - Amplification by voltage amplifiers (of Transconductor + Impedance)
  - Used at low frequencies

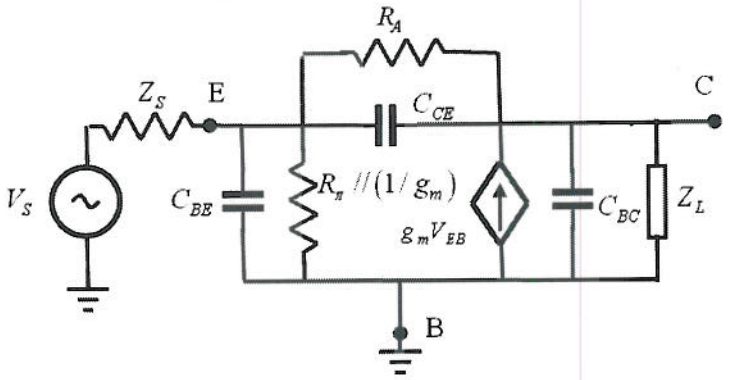
- Current mode:
  - Some signals encoded as time-dependent currents
  - **Voltages** are incidental
  - Basic representation is impedances:
  - Amplification by current amplifiers (or Transimpedance + Admittance)
  - Used at intermediate – high frequencies, broadband.

- "Impedance matched mode"
  - All signals encoded in instantaneous power of travelling EM waves (both V and I)
  - Used in RF, especially narrowband

No particular correlation of mode of operation with power dissipation, which increases with frequency and impedance mismatched. The impedance matched mode is nearly power optimum.

[5]

b) [interpretation]

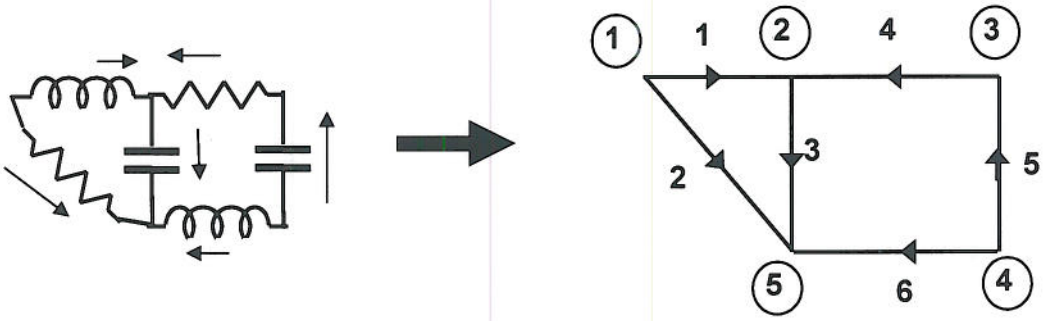


A CB amplifier has lower input impedance than the CE and positive Miller feedback. If driven from a finite Thevenin source the poles will necessarily be at a higher frequency, and it is possible to turn the CB into an oscillator (Colpitts). This is really because the CB operates at a much lower power gain than the CE

[5]

c) [bookwork]

- Abstract a circuit as a directed graph
  - Each circuit element becomes a directed line



- Write the incidence matrix:
  - # nodes as rows
  - # branches as columns
- Entries: 1 if branch leaves node, -1 if branch arrives at node, 0 if no connection

Uses: In circuit analysis and CAD. For example with I the vector of currents, KCL is

- $I^T A=[0]$ (row vector of zeroes, one for each node)
- $AI=[0]$ (column vector of zeroes, one for each node)

The incidence matrix of the above is

$$\begin{array}{c} \\ \text{5 nodes} \end{array} \overbrace{\begin{array}{cccccc} 1 & 2 & 3 & 4 & 5 & 6 \end{array}}^{\text{6 branches}} \begin{array}{c} 1 \\ 2 \\ 3 \\ 4 \\ 5 \end{array} \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & -1 & -1 & 0 & 0 & -1 \end{bmatrix} = \mathbf{A}$$

[5]

d) [bookwork+example]

i) Passives remain the same.

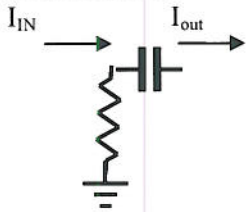
ii) Current sources become voltage loads

iii) Current loads become voltage sources

iv) Voltage amplifiers become reversely connected current amplifiers, and vice versa.

v) Transoconductance amplifiers become reverse transimpedance amplifiers.

A Current mode 1st order RC HPF is:



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a) Write this expression in terms of unit delays (i.e. in z-transform form) and factor it so that only K delay elements are used. Draw a block diagram which implements of the form you derived.

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b) Draw schematic diagrams of switched current circuits which can be used to implement an inverting and a non-inverting unit delay. Estimate the maximum switching frequency that can be used so that the settling error of this cell is smaller than 0.1%. The MOSFETs provided by the fabrication process have f_T=5GHz, threshold V_T=0.5V, transconductance parameter $K = 10\mu A/V^2$ and Early voltage V_A=10V. The power supply will be 2.5V

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c) Design a switched current "branching element" cell which for a given input generates two outputs each equal to half the input. Discuss the effect of transistor mismatch. Show how this branching cell can be used to generate filter coefficients for a switched current filter. How many clock phases are required to specify a coefficient to 0.1% ?

HINT: Think of the binary representation of a number!

[5]

d) Estimate the number of transistors required to implement a general 2nd order filter, and the maximum signal frequency this filter can handle. All sources of error must be constrained to less than 0.1%. Transistor specifications are as in part (c).

[5]

ANSWER QUESTION 6

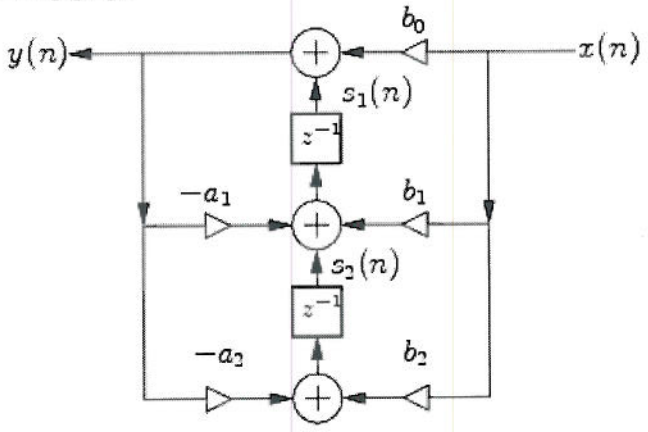
a) [new theory, many know from other courses]

$$y_n = \sum_{k=0}^{K} b_k x_{n-k} - \sum_{k=1}^{K} a_k y_{n-k} \Rightarrow$$

$$y = x\sum_{k=0}^{K} b_k z^{-k} - y\sum_{k=1}^{K} a_k z^{-k} = a_0 x + \sum_{k=1}^{K} z^{-k}\left(b_k x - a_k y\right) =$$

$$= a_0 x + z^{-1}\left(\left(b_1 x - a_1 y\right) + z^{-1}\left(\left(b_2 x - a_2 y\right) + z^{-1}\cdots\right)\right)$$

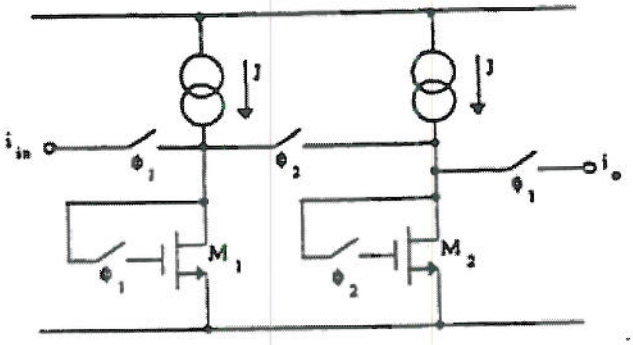
This has the following graph



[5]

b) [bookwork + interpretation]

A delay is TWO cells. Since one cell inverts than the unit delay is non – inverting, and an additional continuous time current mirror is needed for the inversion.



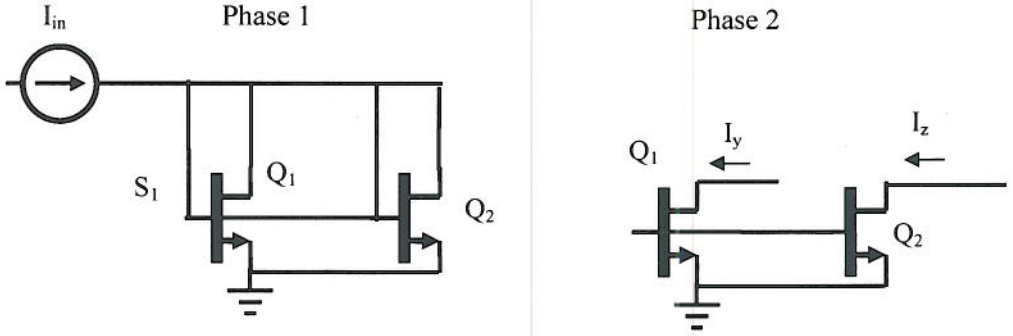
The current copier behaves as a low pass filter with a pole at. ω_T

The settling time limitation is equivalent to requiring the gain of this filter to be within the specified error at the switching frequency. Then

$|1 + j\omega/\omega_T| < 1 + \delta \Rightarrow \omega/\omega_T < \delta \Rightarrow \omega < \delta\omega_T$. The maximum switching frequency is then 5MHz.

[5]

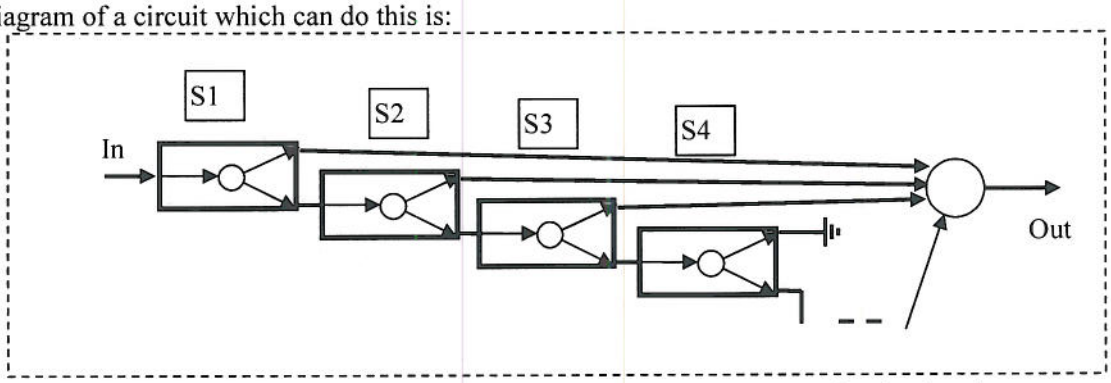
c) [new exercise]



Transistor mismatch has the effect that $I_y = \frac{I}{2}(1+\varepsilon)$, $I_z = \frac{I}{2}(1-\varepsilon)$

A binary representation of a coefficient can be implemented by the branching elements. Each stage needs a separate phase, so an N-bit representation needs N+1 phases. The specified tolerance was 10 bits, so 11 stages are needed.

A block diagram of a circuit which can do this is:



Each coefficient itself needs N+2 phases (1 for each bit, plus an extra one for the signal duplication so that 1 copy is fed to the coefficient and 1 to the delay element.

[5]

d) [new exercise]

The accounting goes:

5 coefficients of 12 splitters each. Each splitter is 2 cells + 6 switches. Assuming a class AB of regulated cascodes and doubled up switches to fight charge injection, each of about 36 transistors (including double switches for charge injection, folded cascodes = 2160, 12 clock phases for each coeffient = 12 flipflops = 24 2 delay cells = 30.

This is a total of well ver 2000 transistors.

The switching frequency of 5 MHz must be further divided by 12 to accommodate the coefficient building.

Then $f_s < 400kHz$ and maximum signal frequencies are about 50kHz (a few times below the Nyquist rate)

[5]