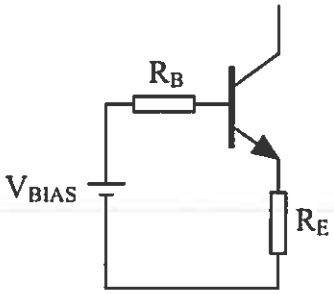
E1.4 SOLUTIONS

Question 1

a) To simplify analysis leading to I_E, replace bias network by Thévenin equivalent:



where $V_{BIAS} = 10 \times 22/(22 + 100) = 1.803$ V

and $R_B = 100k//22k = 18.03$ kΩ

KVL gives: $I_E R_E + V_{BE} + I_B R_B = V_{BIAS}$

$\Rightarrow I_E = (V_{BIAS} - V_{BE})/[R_E + R_B/(1 + \beta)]$

Assuming $V_{BE} = 0.7$ V, this gives $I_E = 1.012$ mA

Assuming transistor active, $\mathbf{I_C = \alpha I_E = 1.007\ mA}$.

Check mode: with I_C = 1.007 mA, V_C = 10 – 1.007m×5.6k = 4.36 V > V_B so active assumption correct. [6]

R_E stabilises the bias current by providing negative feedback. Any change in collector current (for example, due to temperature variations), will produce an opposing change in V_{BE}, via the voltage dropped across R_E. [2]

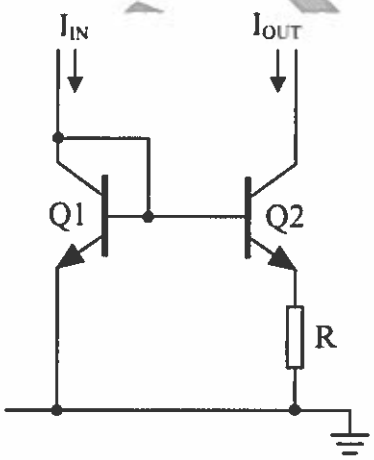
b) Start by assuming both devices are active (for ease of analysis). In this case the upper device, with $V_{GS} = 0$, will have a drain current of $I_D = I_{DSS} = KV_t^2 = 0.2$ mA.

The lower device, for which $V_{DS} = V_{GS} = V$, must be carrying the same current, so we have $0.2m = 0.1m \times (V - 1)^2$. Taking the square root, with +ve sign (since we are assuming the device is above threshold) gives $\mathbf{V = (1 + \sqrt{2}) = 2.414\ V}$.

Lower device: $V_{DS} = V_{GS} > V_t$, so **lower device is ACTIVE.**

Upper device: ($V_{DS} = 5 - 2.414 = 2.586$ V) > ($V_{GS} - V_t = 1$ V), so **upper device is ACTIVE.** [6]

c) Widlar current sink:



Ignoring base current, KVL in the loop including R and the EBJs gives:

$$V_{BE1} = V_{BE2} + I_{OUT}R$$

Using the reduced Ebers-Moll eqn we can express the V_{BE}s in terms of the input and output currents:

$$V_T \ln(I_{IN}/I_S) = V_T \ln(I_{OUT}/I_S) + I_{OUT}R$$

Cleaning this up gives:

$V_T \ln(I_{IN}/I_{OUT}) = I_{OUT}R$ or $I_{IN} = I_{OUT}\exp(I_{OUT}R/V_T)$

schematic + analysis = [4 + 4]

d) According to the resistance reflection rule, the input resistance at the base of a BJT is equal to $[r_{be} + (1 + \beta)\times R]$ where r_{be} is the base-emitter resistance and R is the external resistance between the emitter and ground. In the case of the Darlington shown, the resistance in the emitter of Q1 is the parallel combination of R_E and the r_{be} of Q2. The input resistance at the base of Q1 is therefore:

$$R_i = r_{be1} + (1+\beta_1)(R_E \,//\, r_{be2})$$

Alternative solution based on analysis of the SSEC also acceptable. [6]

e) Initial condition (for $t < 0$): if the input voltage has been +5 V for a long time, the capacitor current will have dropped to zero and the voltage $V_{CAP} = (V_{IN} - V_B)$ across it will be $V_{CAP} = 5 - 0.7 = +4.3$ V. The base will be at 0.7 V because of the base current provided via the 100 kΩ resistor. The value of this current will be $I_B = (5 - 0.7)/100k = 43$ μA. Since $\beta I_B \times 1k = 8.6 > 5$ V, we know that the transistor is saturated, and the output voltage will be $V_{OUT} \approx 0.2$ V.

At $t = 0+$: V_{CAP} cannot change instantaneously, so when V_{IN} falls suddenly to 0 V, V_B will fall suddenly to -4.3 V and the transistor will cut off causing the output to go high.

For $t > 0$: current flowing via the 100 kΩ resistor will charge the capacitor causing V_B to rise. In the absence of the transistor the asymptotic value of V_B would be +5 V. Using the standard result for an RC network, the initial time-variation of V_B is therefore of the form:

$$V_B = 5 + (-4.3 - 5)\exp(-t/\tau)$$

where $\tau = 10n \times 100k = 1$ ms.

The transistor will turn on again, and the output will go low, when V_B reaches ~0.7 V. The pulse duration T will therefore satisfy:

$$0.7 = 5 - 9.3\exp(-T/\tau) \quad \text{or} \quad \mathbf{T = \tau \ln(9.3/4.3) = 0.77\ ms}$$ [8]

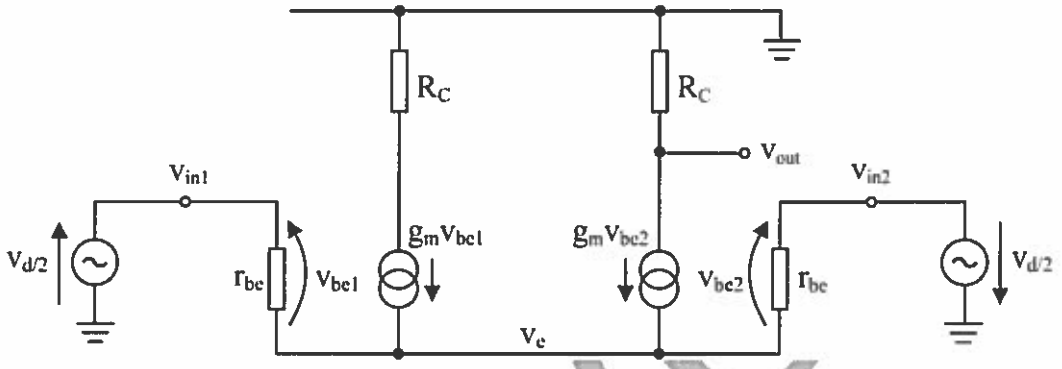
f) The essential elements of a sinusoidal oscillator are a frequency selective block and an amplifying block. These must be connected to form a loop. In order for the circuit to produce stable sinusoidal oscillations, the total gain around the loop must be unity at a unique frequency. [4]

Question 2

a) Assuming $V_{BE} \approx 0.7$ V, the potential at the base/collector of Q3 is -4.3 V, and the input current to the current mirror formed by Q3, Q4 is 4.3/20k = 215 μA. Taking into account the finite beta error, the output current of the current mirror is $\mathbf{I = 215\mu/(1 + 2/\beta) = 211\ \mu A.}$ **[5]**

If $V_{IN1} = V_{IN2}$ then the tail current will divide equally between Q1 and Q2, and the collector currents of these transistors will be $I_{C1} = I_{C2} = \alpha I/2 = 105$ μA. The quiescent output voltage will then be $\mathbf{V_{OUT} = 5 - 20k \times 105\mu = 2.9\ V}$. [3]

b) SSEC:



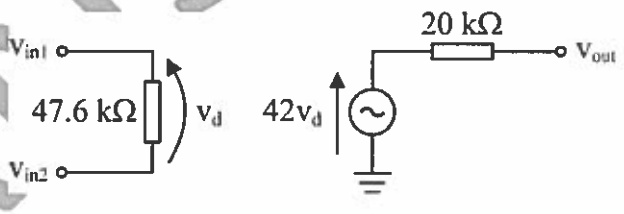
[6]

If the input signal is a purely differential voltage v_d, as shown, then by symmetry we can say that $v_e = 0$. In this case $v_{be2} = -v_d/2$, the output current of Q2 is $-g_m v_d/2$, and the output voltage is $v_{out} = g_m R_C v_d/2$. The single-ended differential gain is then $\mathbf{A_d = v_{out}/v_d = g_m R_C/2}$.

Putting $g_m = I_{C2}/V_T = 4.2$ mS (using $V_T = 25$ mV) gives $\mathbf{A_d = 42}$. [4]

The input currents are $\pm i_{in}$ where $i_{in} = v_d/2r_{be}$. The differential input resistance is therefore $R_i = v_d/i_{in} = 2r_{be} = 2\beta/g_m$, which gives $\mathbf{R_i = 47.6\ k\Omega}$. The output resistance is $\mathbf{R_o = 20\ k\Omega}$. [3]

Macromodel:



[4]

c) Q4 has a finite output resistance given by $r_{o4} = V_A/I$ where V_A is the Early voltage. This needs to be added to the SSEC between the common emitter node of Q1, Q2 and ground.

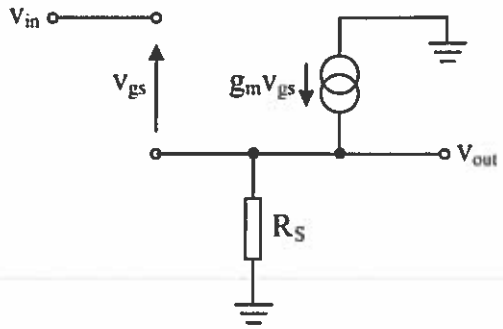
For the common-mode gain calculation, where $v_{in1} = v_{in2} = v_{in}$, we can again exploit the symmetry of the circuit and analyse just the RH half-circuit as a common-emitter stage with a collector resistance R_C and an emitter resistance $2r_{o4}$. Using the standard result (no need to prove it), the common-mode gain is then $A_{cm} = -\alpha R_C/2r_{o4}$. With $V_A = 120$ V and $I = 211$ μA, $r_{o4} = 569$ kΩ and $\mathbf{A_{cm} = -0.0174}$.

The common-mode rejection ratio is then $\mathbf{|A_d/A_{cm}| = 42/0.0174 = 2414}$ (allow for rounding). [5]

Calculation based a standard formula, e.g. $|A_d/A_{cm}| = V_A/2V_T$, is also acceptable.

Question 3

a) SSEC ignoring r_o is:



From the SSEC, we have:

$$v_{out} = g_m v_{gs} R_S = g_m(v_{in} - v_{out})R_S$$

$$\Rightarrow \quad v_{out}(1 + g_m R_S) = g_m R_S v_{in}$$

$$A_v = v_{out}/v_{in} = g_m R_S/(1 + g_m R_S)$$

Applying a test source v_x to the output with $v_{in} = 0$, the current into the output will be:

$$i_x = v_x/R_S + g_m v_x$$

$$\Rightarrow \quad R_o = v_x/i_x = 1/(1/R_S + g_m) = R_S//(1/g_m)$$

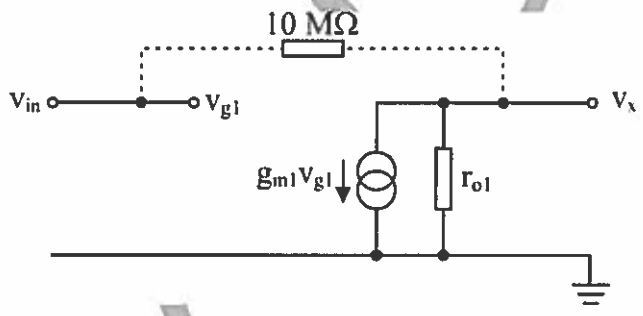
gain + output resistance = [6 + 4]

b)i) The 10 MΩ resistor sets the operating points of Q1 and Q2 by forcing the DC voltages at input and output to be equal (because $I_{G1} = 0$). The quiescent output voltage must therefore be whatever gate voltage is required to give a drain current of 1 mA in Q1. We can therefore write: 1 mA = $K_1(V_{OUT} - V_{t1})^2$, with $K_1 = 0.25$ mA/V^2 and $V_{t1} = 1$ V. Taking the +ve square root (Q1 above threshold) gives $\mathbf{V_{OUT} = 3\ V}$. [4]

With $V_{OUT} = 3$ V, the drain current of Q2 is $\mathbf{I_{D2} = 3\ mA}$. [2]

If Q2 is carrying 3 mA then its gate-source voltage must satisfy 3 mA = $K_2(V_{GS2} - V_{t2})^2$. With $K_2 = 1.5$ mA/V^2 and $V_{t1} = 1$ V, and once again taking the +ve square root, this gives $V_{GS2} = (1 + \sqrt{2})$, implying that $\mathbf{V_X = (4 + \sqrt{2})\ V}$. [2]

b)ii) SSEC in mid-band:



From the SSEC, ignoring the 10 MΩ:

$$v_x = -g_{m1} v_{g1} r_{o1} = -g_{m1} v_{in} r_{o1}$$

$$\Rightarrow \quad A_{v1} = -g_{m1} r_{o1}$$

Putting $g_{m1} = 2\sqrt{(K_1 I_{D1})} = 1$ mA/V and $r_{o1} = V_A/I_{D1} = 100$ kΩ, $\mathbf{A_{v1} = -100}$.

SSEC + analysis = [4 + 4]

b)iii) Using the result given in part a), the gain of the source follower is;

$$A_{v2} = R_S/(R_S + 1/g_{m2}) \quad \text{with } R_S = 1\ \text{k}\Omega$$

With $g_{m2} = 2\sqrt{(K_2 I_{D2})} = 3\sqrt{2}$ mA/V (corresponding to $1/g_m = 236\ \Omega$) this gives $A_{v2} = 0.809$. The overall gain A_v is just the product of the two individual stage gains, so $\mathbf{A_v = -80.9}$.

Using the result from part a), the output resistance is (1k//236) = **191 Ω** [4]