EE3-01
EE9-AC1

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2013

MSc and EEE PART III/IV: MEng, BEng.and ACGI

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Monday, 7 January 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : C. Toumazou
Second Marker(s) : P. Georgiou

1. (a) Figures 1.1 and 1.2 show two constant current generators. What are the key differences between these two circuits?

[4]

(b) Voltage and current-sources are key components in analogue circuit design. Sketch a typical band-gap voltage reference circuit and prove that the temperature coefficient of the output voltage V_0 is zero if $V_0 = 1.283\ V$. Assume the temperature coefficient of V_{BE} to be $-2.5mV/°C$, Boltzmann's constant $k = 1.38 \times 10^{-23}\ J/K$ and electron charge $q = 1.6 \times 10^{-19}\ C$.

[10]

(c) Calculate the fractional temperature coefficient for the constant current generator of Figure 1.1 at room temperature, given that R is a polysilicon resistor with a temperature coefficient of 1500 ppm/°C.

[6]

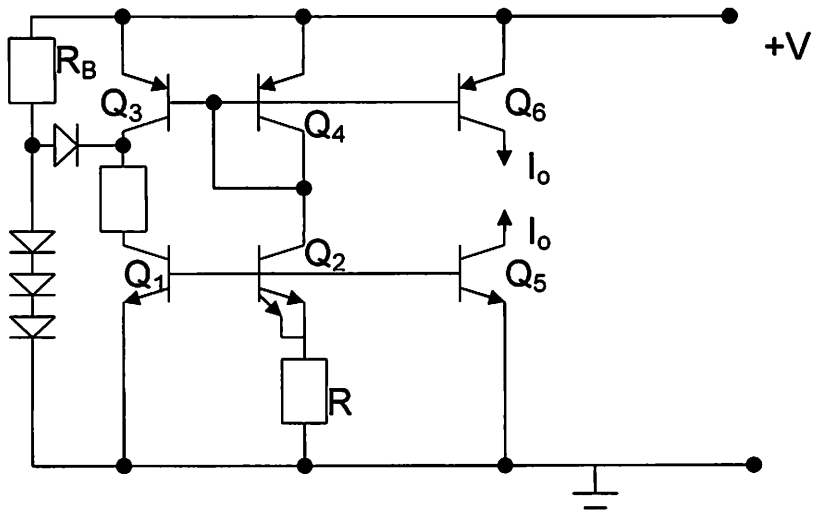


Figure 1.1

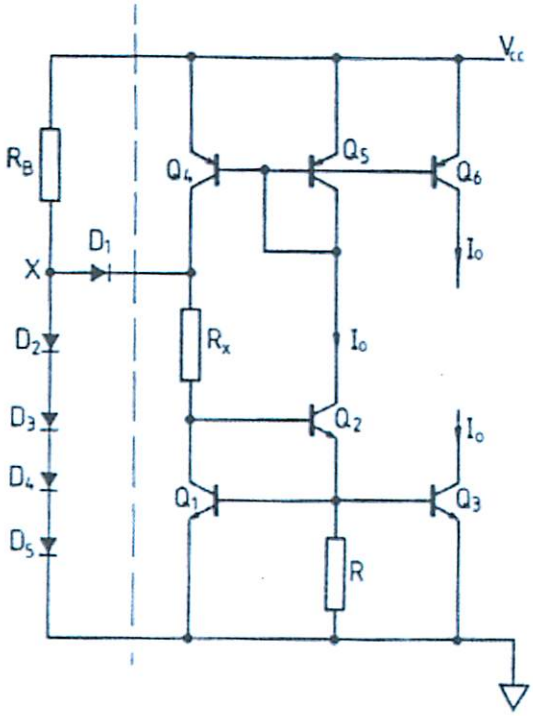


Figure 1.2

2. (a) Figure 2.1 shows a folded cascode connection. What is the main advantage of this design over the more classical cascode connection? Show via a brief sketch how the architecture of Figure 2.1 can be used to form the basis of a single stage fully differential folded cascode operational amplifier (op-amp) with common-mode feedback included.

[6]

(b) Figure 2.2 shows a two-stage CMOS op-amp. Estimate the low-frequency differential voltage gain and the gain-bandwidth product of the amplifier. The aspect ratios of all devices are shown on the circuit. Assume that all bulk effects are negligible. The device model parameters are given below. What is the main advantage and disadvantage of a single-stage compared to a two-stage op-amp ?

[11]

(c) Explain why a resistor in series with the compensation capacitor C in Figure 2.2 can significantly improve the amplifier's phase margin.

[3]

CMOS TRANSISTOR PARAMETERS

MODEL PARAMETERS	$Kp\ (\mu A/V^2)$	$\lambda\ (V^{-1})$	$V_{T0}\ (V)$
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

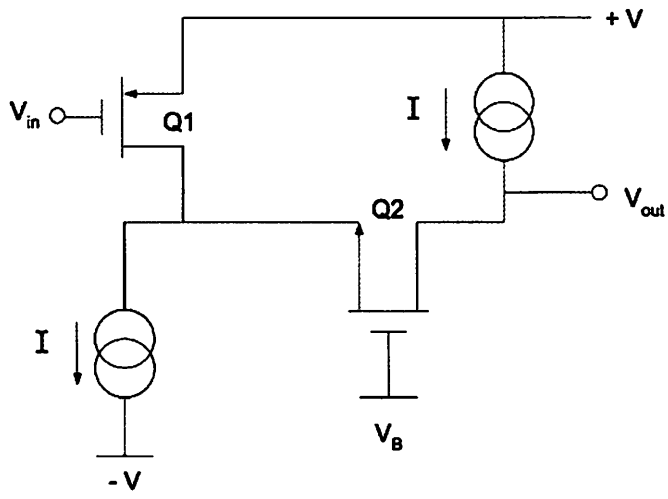


Figure 2.1

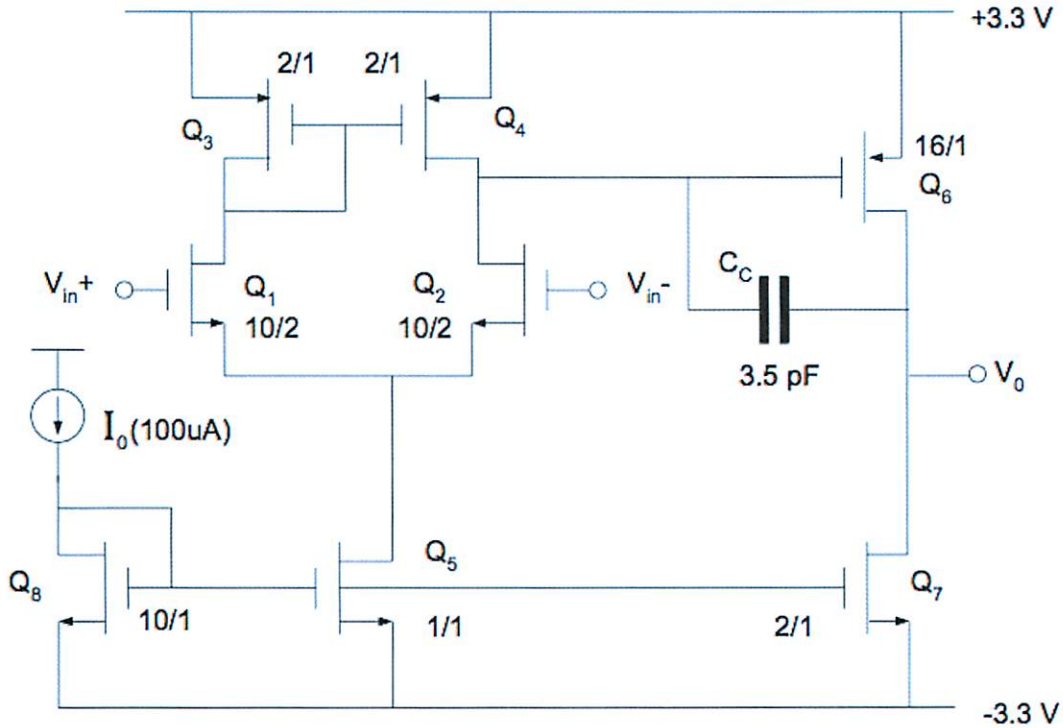


Figure 2.2

3. (a) Sketch a typical architecture of a current-mode algorithmic analogue to digital converter and explain its principles of operation.

[10]

(b) Assume that the maximum resolution of any sampled-data converter is limited by switch noise (kT/C), calculate the maximum resolution of a stereo-audio system running at a sample rate of 40 kHz. You may assume a MOSFET switch aspect ratio $(W/L) = 1/8$, transconductance parameter $Kp = 20\ \mu A/V^2$ and a device threshold voltage $V_T = 1\ V$. The on voltage of the switch is a $5\ V$ reference (i.e. $V_{GS}on = V_{ref} = 5\ V$). You may also assume that the switch settles in $10\ \tau$ (where τ = time constant) over one period of the clock frequency.

Boltzmann's constant $k = 1.38 \times 10^{-23}\ J/K$ and the ambient temperature is $300\ K$.

[10]

4.(a) Under which operating conditions does the MOSFET of Figure 4.1 realise a linear floating resistor between terminals *A* and *B* ? Explain why the bulk is not connected to the source.

[6]

(b) Discuss three sources of non-linearity in the single MOSFET resistor realisation of Figure 4.1 and suggest one suitable circuit design to help to eliminate one or more of these non-linear terms. Show all necessary circuit analysis to confirm your design.

[6]

(c) (i) Show how the two transistor differential integrator shown in Figure 4.2 can be modified to create a double differential integrator. Sketch the new circuit and derive the time constant.

[6]

(ii) Assuming the transistors in your design have a resistance of 200 KΩ in their linear region and a feedback capacitor of 100pF is used, calculate the value of the time constant for your integrator.

[2]

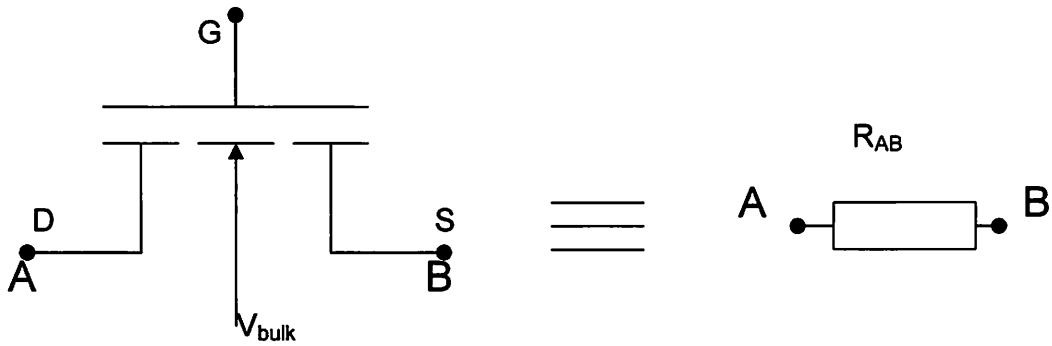


Figure 4.1

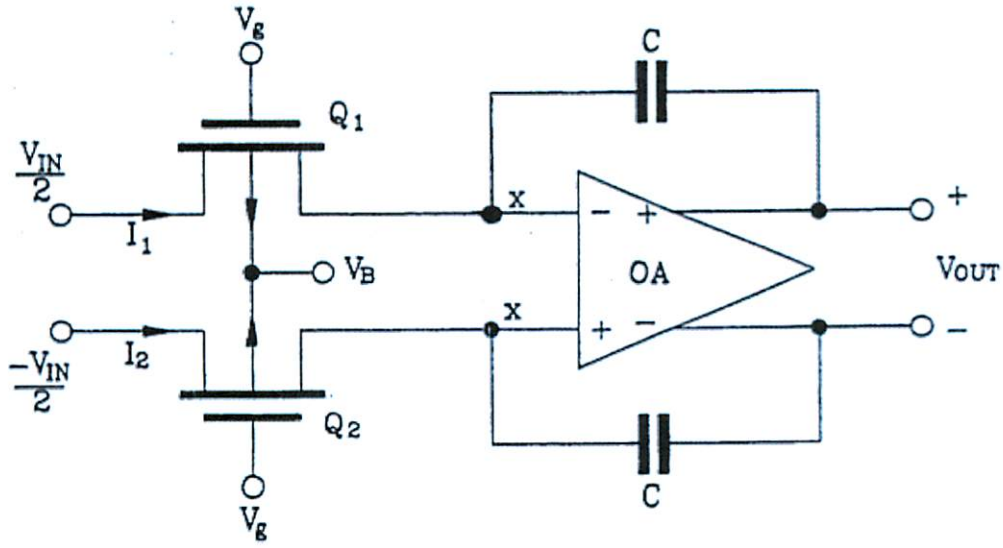


Figure 4.2

5. (a) Sketch a suitable circuit for a regulated cascode current-mirror and explain why the output resistance is larger than the output resistance of a traditional cascode.

[6]

(b) For the current mirror of Figure 5.1 derive the voltage swing in terms of device threshold voltage V_T, clearly stating any assumptions you make.

[7]

(c) With the aid of a macromodel, explain the theoretical concept of current feedback and how it results in constant bandwidth application.

[7]

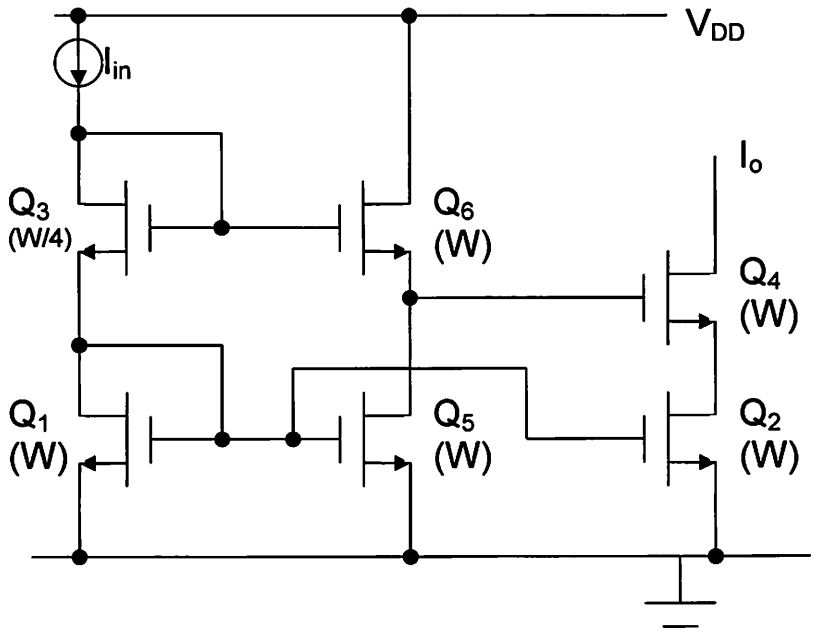


Figure 5.1

6. (a) For a 3rd order Chebyshev switched capacitor low pass filter, calculate the normalised passive component values for the original double terminated LC prototype of the filter shown in Figure 6.1. The filter is to have a cut-off frequency of 10 kHz and assume a clocking frequency of 200 kHz. The values of the integration capacitor for the capacitor-based sections are 10.12 pF, and for the inductive based sections are 6.98 pF. All other switched capacitors are 1pF. All values should be normalised to 1rad/s. You may assume that the clocking frequency is so high that the integrators can be assumed lossless.

[10]

(b) Explain the limitations of switch capacitor filters, showing a graph and a transfer function of how it's response deviates from an ideal integrator. Explain how this imposes a limitation on the clock frequency.

[8]

(c) Explain how the errors due to the limitations explained in part (b) be reduced.

[2]

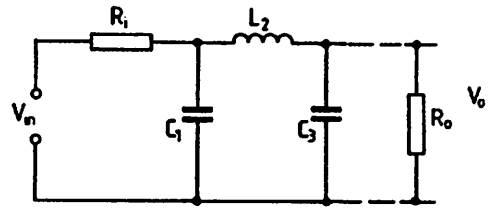


Figure 6.1

Solutions 2013 EE 3-01. EE9-AC1

1. a) Figure 1.1 is a self biased PTAT - generates a current which is proportional to temperature.

$$I_{out} = \frac{V_T \ln[n]}{R}.$$

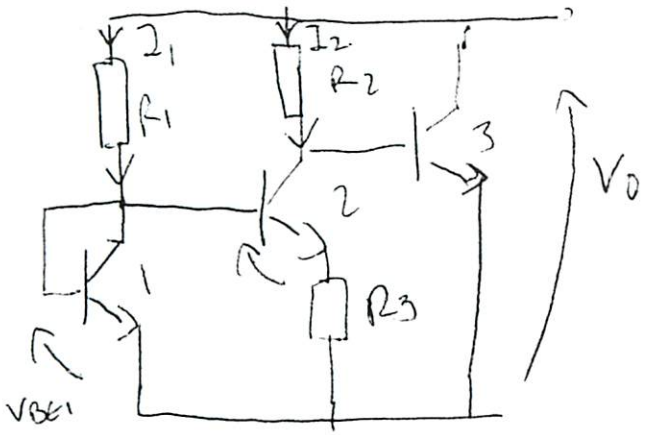
2/4

Figure A.2 is a V_{be} reference current since which is supply independant. Output current is generated from a regulated cascode.

Drawback is it has a large temperature coefficient and needs a large resistor.

2/4

b)



Bandgap

5/10

$$V_{BE1} = V_{BE2} + I_2 R_3$$

Since $V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_1}{I_2}\right)$

then $V_o = V_{BE3} + R_2/R_3 \, V_T \ln\left(I_1/I_2\right)$

$V_{BE3} = V_T \ln\left(\frac{I_3}{I_s}\right)$ -> assume non-temperature independant

for $\frac{dV_o}{dt} = 0$ then $\frac{dV_{BE3}}{dT} = \frac{V_T}{T} \frac{R_2}{R_3} \ln\left(\frac{I_1}{I_2}\right)$

Since $\frac{dV_{BE}}{dt} = -2.5 mV/°C$, $\frac{V_T}{T} = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}}$

then $\left(\frac{R_2}{R_3}\right) \ln\left(\frac{J_1}{J_2}\right) = 29$ and so

$V_o = 1.283\ V.$ 5/10

Temperature Coefficient:

c/b) $TCF = \frac{1}{VT}\frac{\partial V_T}{\partial T} - \frac{1}{R}\frac{\partial R}{\partial T}$

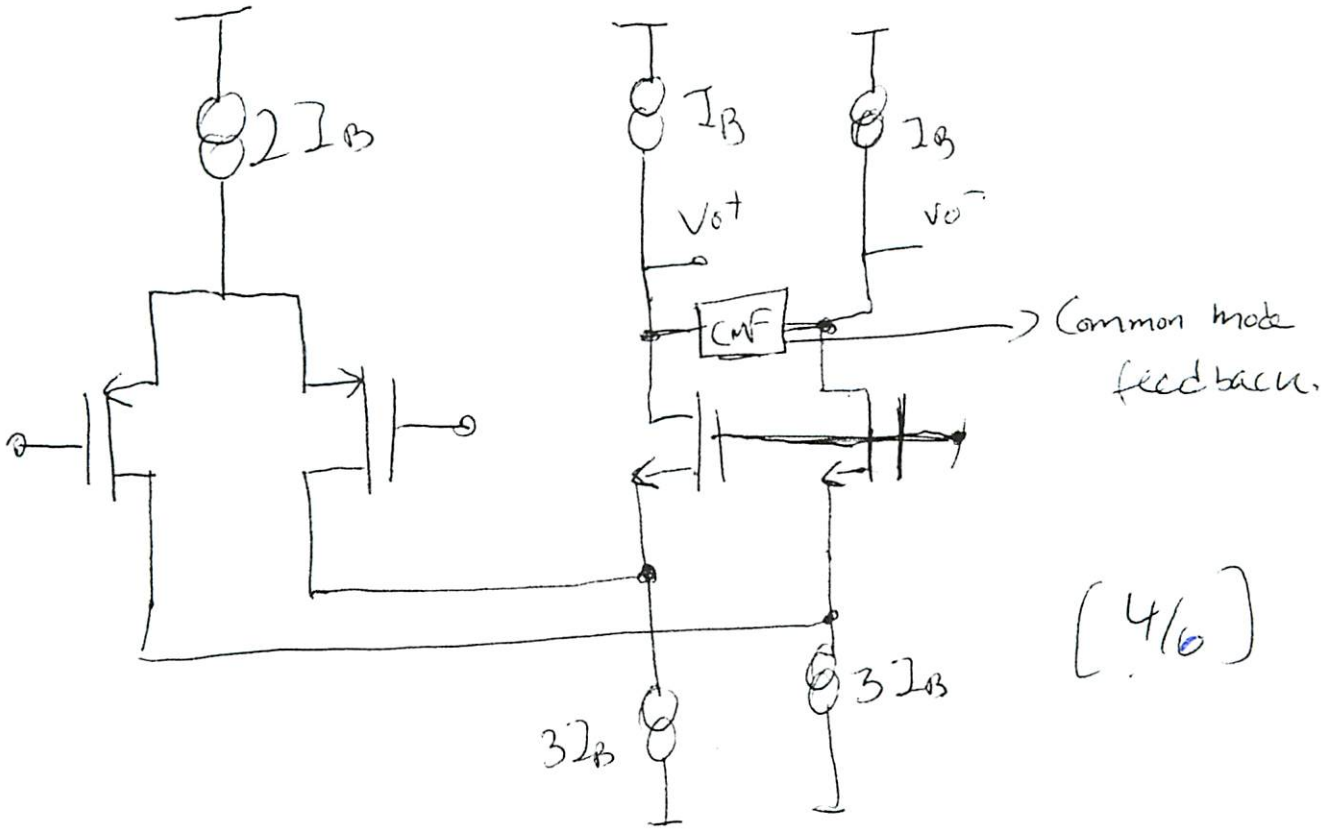
$= \frac{1}{T} = 1500 \times 10^{-6}$ @ Room $T = 1833\ ppm/^oC$

6/6

2.a) Main advantage of the folded cascode is that the signal path is folded giving a balance between input and output allowing the supply voltage to be reduced.

[2/6]

Single stage fully differential amplifier with Cmfb.



[4/6]

b) $A_{v1} = \dfrac{-g_{m2}}{g_{o2}+g_{o4}}$

$(g_{o2}+g_{o4}) = I_{o2}(\lambda_N + \lambda_P) = 5\times10^{-6} \times 0.05 = 2.5\times10^{-7}\,\Omega$

$g_{m2} = 2\sqrt{\beta_2 I_D}$

$\beta_2 = \mu_N \left(\frac{W}{L}\right) = 7.5\times10^{-5}\ A/V$

$g_{m2} = 3.87\times10^{-5}\ S$

$A_{v1} = -154.9$

$A_{v2} = -g_{m6} / (g_{o7}+g_{o6})$

$(g_{o7}+g_{o6}) = I_{o6}(\lambda_N+\lambda_P) = 20\times10^{-6} \times 0.05$

$= 10\times10^{-7}\,\Omega^{-1}$

$g_{m6} = 2\sqrt{\beta_6 I_{o6}}$

$\beta_6 = \mu_N \left(\frac{W}{L}\right)_6 = 1.6\times10^{-4}\ A/V$

$g_{m6} = 1.13\times10^{-4}\ S$

$A_{v2} = -113$

$A_{Total} = A_{v1} \times A_{v2} = 17503$

$G.B_P = \dfrac{g_{m2}}{2\pi C_L} = \dfrac{3.87\times10^{-5}}{2\pi \times 3.5\times10^{-12}} = 1.76\ MHz$

9/11

Single Stage.

Advantage: High Speed
Good Phase margin

Disadvantage :- lower gain.
lower CMVR/ output swing.

2/11.

c) Introducing ~~a~~ resistor R in series improves phase margin

Feed forward Compensation eliminates RHP zero.

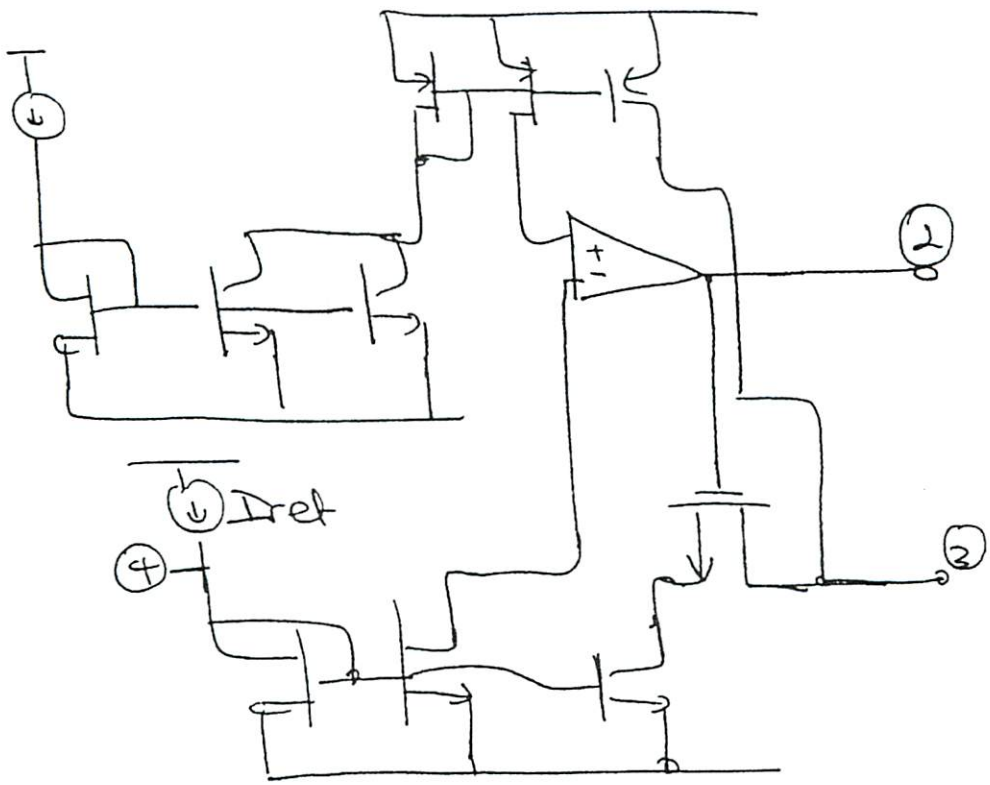
Zero given by $z = \frac{-g_{m6}}{C_C}$.

With $R \Rightarrow z = -1/(1/g_{m6} - R)$.

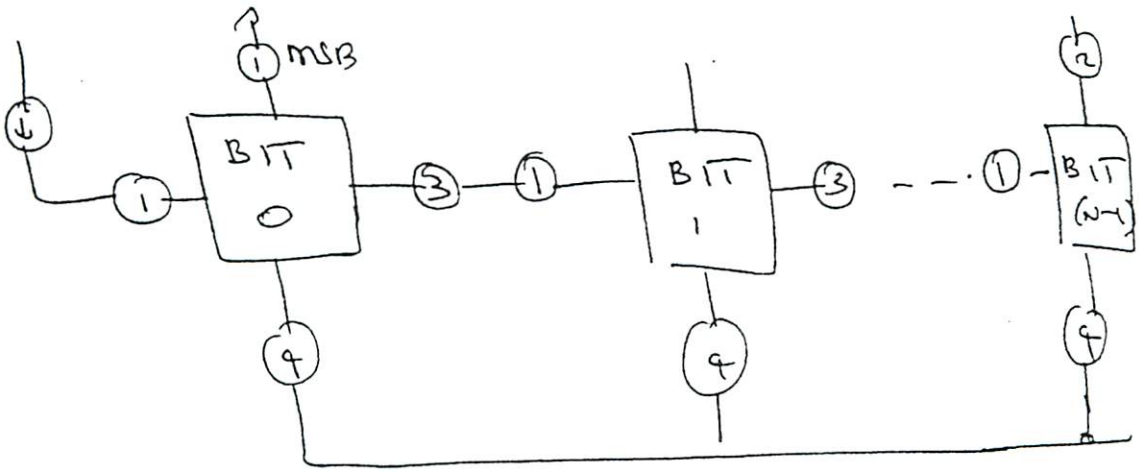
3/3

Question 3

Algorithmic Converter 1 Bit



2/10



BASIC ARCHITECTURE

2/10

Question 3 - continued

If $2I_{IN} < I_{ref}$

Comp goes low, digital output = 0
and analogue output $2I_{IN}$.

If $2I_{IN} > I_{ref}$, comp output goes high, digital = 1

Analogue output $(2I_{IN} - I_{ref})$

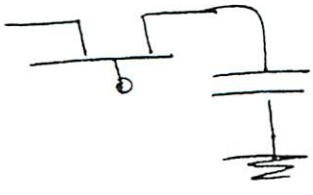
Analogue output feeds into following bit which performs exactly the same function. The process is repeated on many times as necessary to achieve the desired resolution.

6/10

—11—

Last part

$DR \triangleq V_{refl} / Noise = 2^N$



RMS noise of switch capacitor

$\sqrt{\frac{kT}{C}}$

CT

Assume $f_c = \frac{1}{10 \cdot R \cdot C}$, then

Solving for C gives

$$DR = 2^N = V_{rell} / \sqrt{KT\ 10 \cdot R \cdot F_c}$$

$$R_{on} = \frac{1}{2\beta(V_{GS} - V_T)} \simeq \frac{1}{(2\beta \times 4)}$$

$$\beta = \left(\frac{KW}{2L}\right)$$

Can now find DR @ 40kHz.

10/10

GT

Q4 a) Assumption is that if ($V_{DS} \approx 0$) or ($V_{DS} << V_{GS} - V_T$) device acts in linear region. From

$$I_D = \frac{KW}{L}\left[(V_{GS}-V_T)V_{DS} - V_{DS}^2/2\right](1+\lambda V_{DS})$$

for $V_{DS} << (V_{GS}-V_T)$, then $\lambda V_{DS} << 1$

6/6 So $I_D = \frac{KW}{L}(V_{GS}-V_T)V_{DS}$

OR $R_{AB} = V_{DS}/I_D = L/(KW(V_{GS}-V_T))$

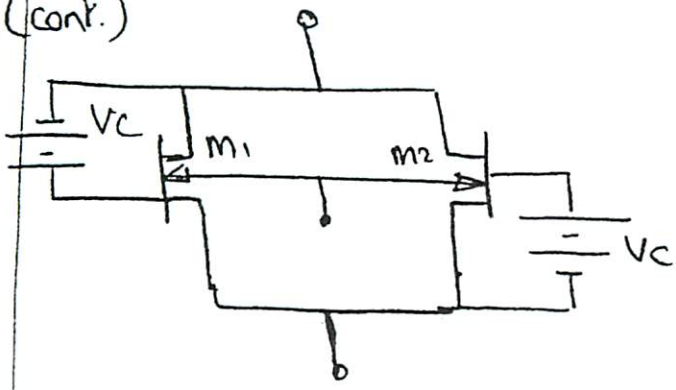
b) Three sources of non-linearity

(i) limited due to V_{BS} changing V_T for resolve V_{DS} due to body effect.
ie. $V_T = V_{TO} + \gamma\left[\sqrt{-V_{BS}+2\phi_F} - \sqrt{2\phi_F}\right]$
γ = bulk threshold parameter
ϕ_F = Fermi-level potential

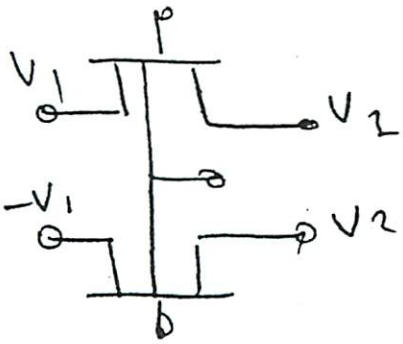
3/6 (ii) limited due to V_{DS} approaching $(V_{GS}-V_T)$ hence saturation region for large positive V_{DS}.

(iii) For large values of V_{DS} the $V_{DS}^2/2$ term comes in making the resistor quite non-linear.

Q4 (cont.)

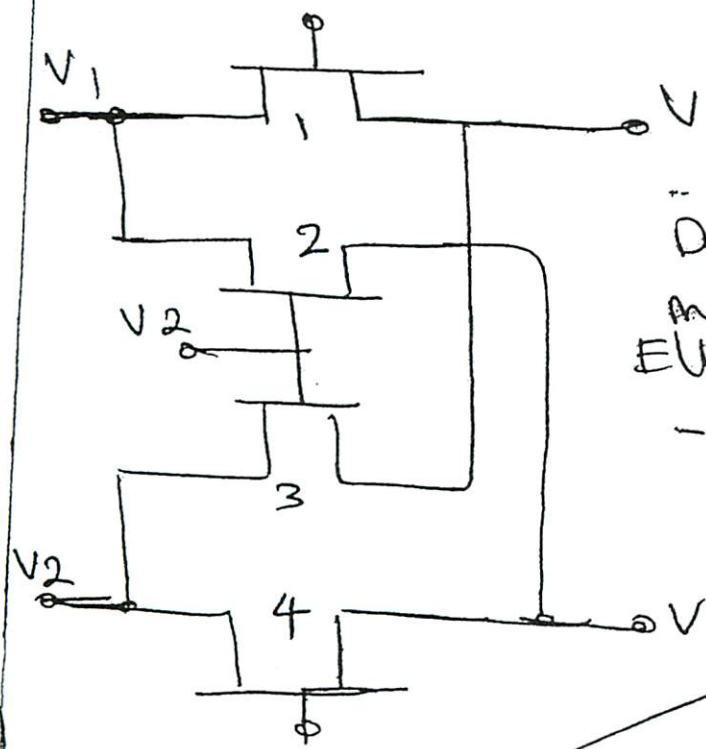


Parallel circuit – eliminates $V_{DS}^2/2$ term.



Differential scheme

Effects of V_{DS} cancelled.

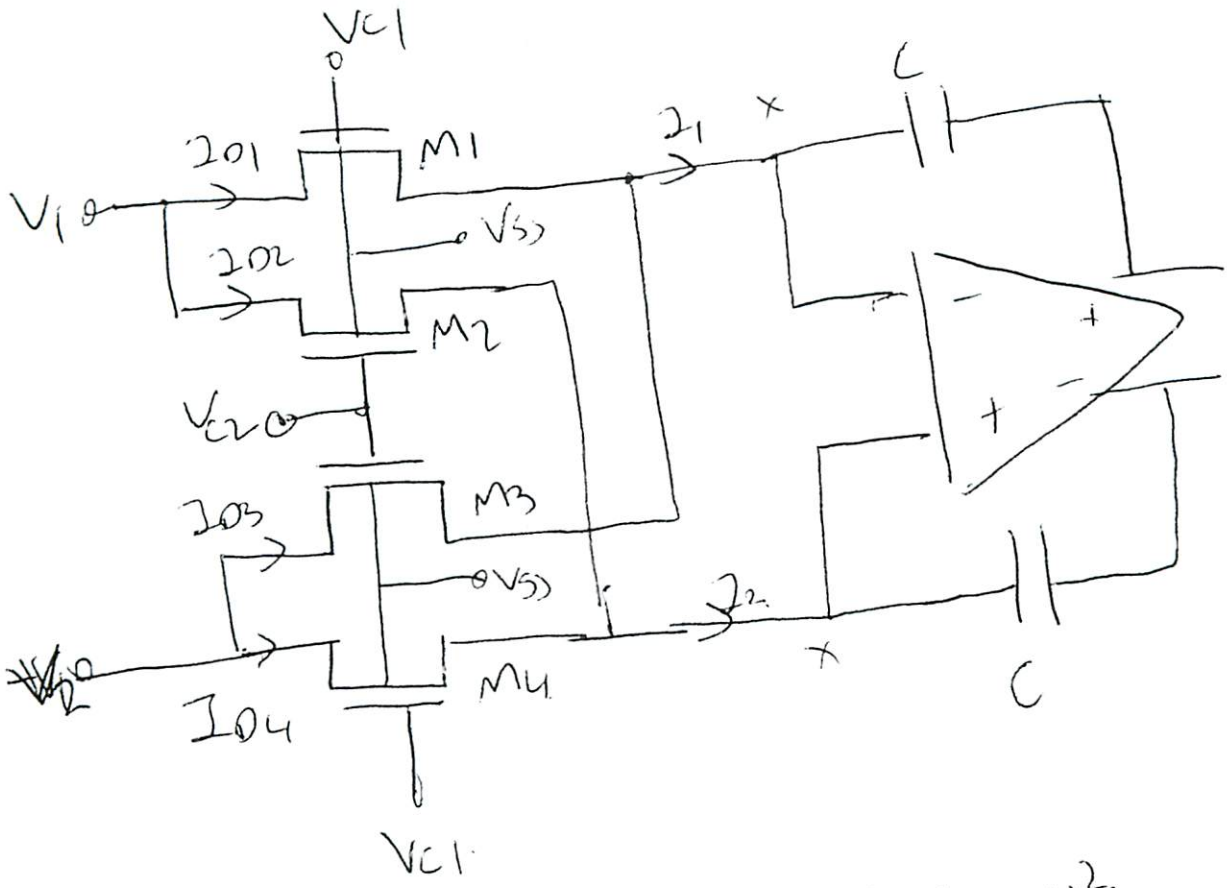


Double differential MOS.
Eliminates $-V_{DS}$ and V_T term.

ANY one of these will do!

3/5

1 C) i) Double differential integrator



(3/6)

$I_{D1} = 2\beta(V_{C1} - V - V_T)(V_1 - V) - 1/2(V_1 - V)^2$

$I_{D2} = 2\beta(V_{C2} - V - V_T)(V_1 - V) - 1/2(V_1 - V)^2$

$I_{D3} = 2\beta(V_{C2} - V - V_T)(V_2 - V) - 1/2(V_2 - V)^2$ [2/6]

$I_{D4} = 2\beta(V_{C1} - V - V_T)V_2 - V_1 - 1/2(V_2 - V_1)^2$

$I_1 = I_{D1} + I_{D3}$ $\quad I_2 = I_{D1} + I_{D3}$

$R = \dfrac{V_1 - V_2}{I_1 - I_2} = 1/2\beta(V_{C1} - V_{C2})$

(1/6)

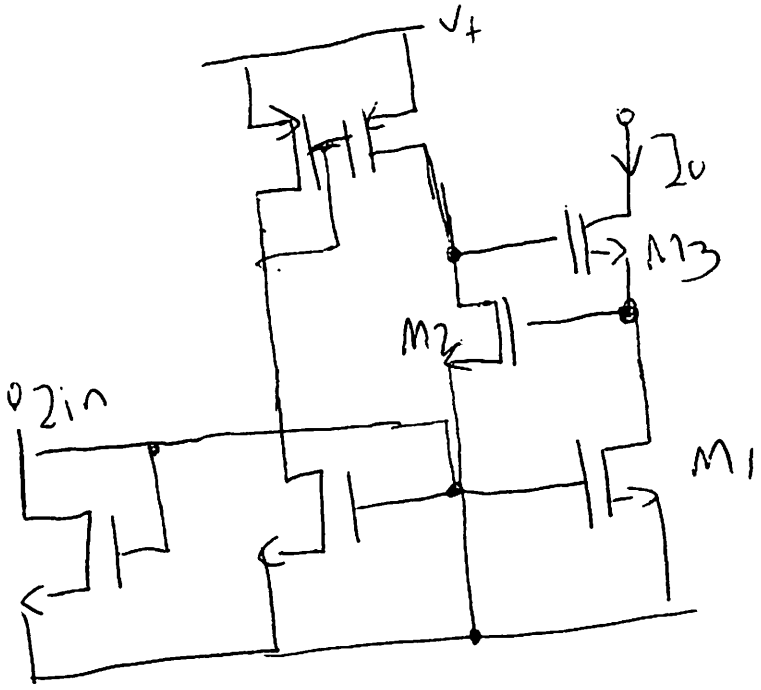
Time constan $\tau = \dfrac{C}{2\beta(V_{C1} - V_{C2})}$

ii) $\dfrac{R}{2} = 200k\Omega$ $\quad R = 100k\Omega$

$\tau = RC = 100\ k\Omega \times 100pf = 0.0000/sec$ 2/2

$= 1 \times 10^{-5}$ sec.

5. a) regulated cascode current mirror



6/6

- Uses feedback through transistor M2 and
- Achieves very high output resistance

$r_{out} = (g_{m3} r_{o3}) \cdot r_{o1} \cdot A$

$r_{out} = (g_{m3} r_{o3}) r_{o1} (g_{m2} r_{o2})$

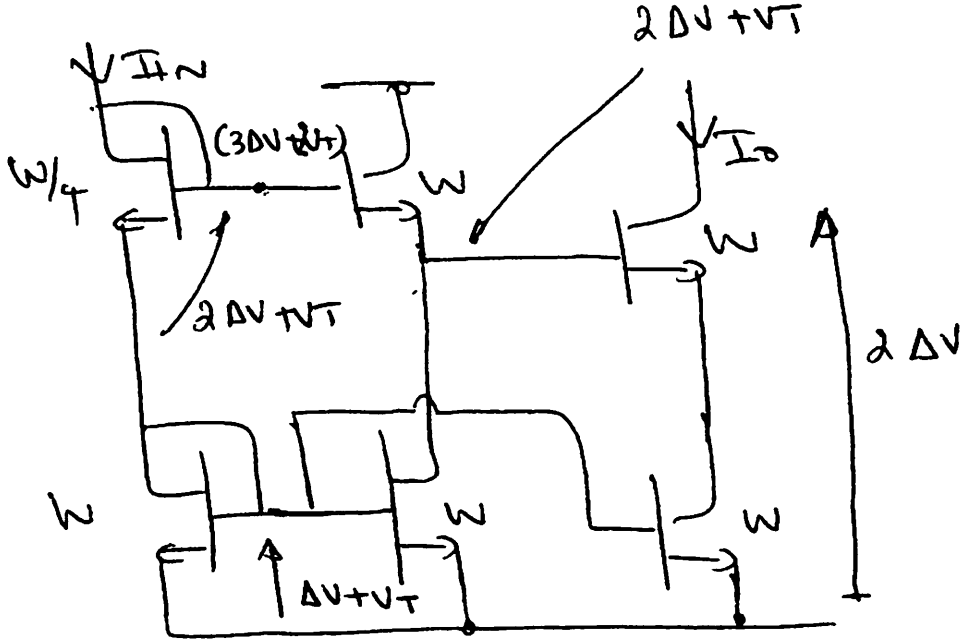
Advantages: high output resistance
high output swing

Disadvantages — inaccuracies of simple current mirror.
— feedback may lead to potential instability.

Q#6 cont

b) output Swing

Circuit includes all saturation Voltages



Assuming equal L's

$I_O = I_{IN}$

$\beta_1 = \beta_2 = \beta_4 \quad \beta_5 = \beta_6 = \beta$

$\beta_3 = \beta/4$ (7/7)

$\therefore V_{sat(3)} = 2(V_{GS} - V_T)$

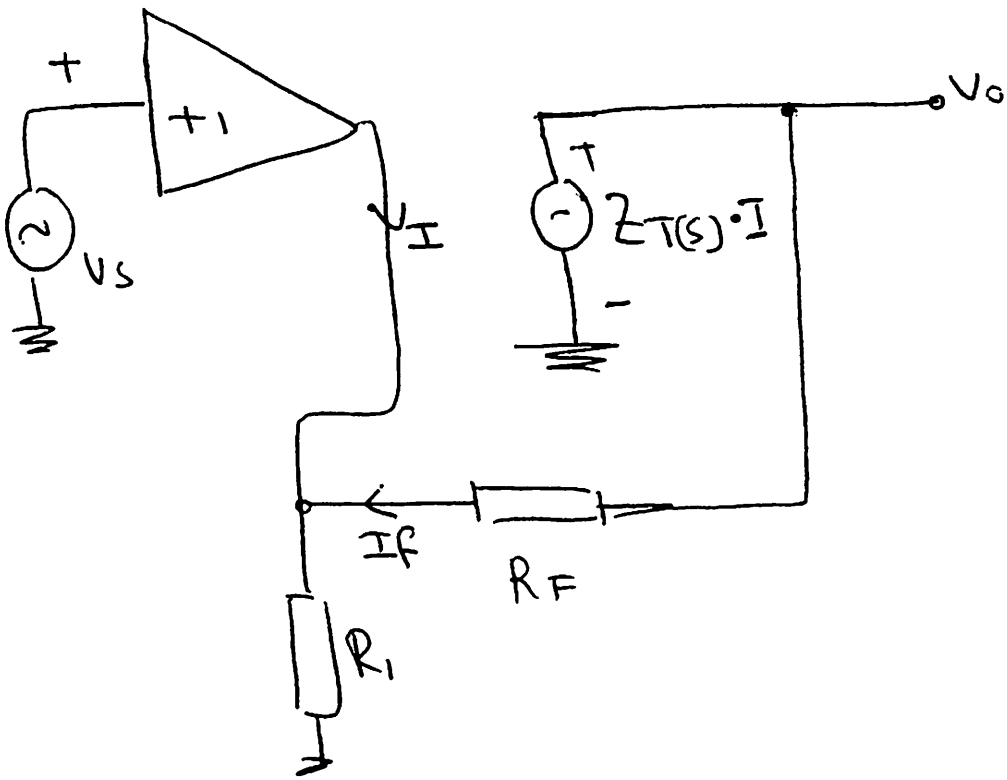
NOTE $\Delta V = (V_{GS} - V_T)$

Swing $\underline{\underline{2\Delta V}}$.

Qu 6 cont

macromodel of Current-feedback op-amp.

c).



$Z_{T(S)} = Z_{TO}/(1+jf/f_p) \Rightarrow f_p$ dominant Pole

From model

$$I_f = (V_o - V_s)/R_F$$

$$I_1 = V_s/R_1$$

$$V_o = Z_{T(S)} I = Z_{(T)}(I_1 - I_f)$$

From above

$$(V_o/V_s) = (1 + R_F/R_1)\left[\frac{Z_{T(S)}}{R_F + Z_{T(S)}}\right]$$

Q4b cont

substitute $Z_{(T)}$s, and assume $Z_{TO} \gg R_F$

$$\left(V_O/V_S\right)_{j\omega} = \left(1 + \frac{R_F}{R_1}\right)\left[\frac{Z_{TO}}{Z_{TO}+R_F}\right]\left(\frac{1}{\left(1+jf/f_p\left(\frac{Z_{TO}+R_F}{R_F}\right)\right.}\right)$$

Assuming $Z_{TO} \gg R_F$

$$\left(\frac{V_O}{V_S}\right)_{j\omega} = \left(1+\frac{R_F}{R_1}\right)\left(\frac{1}{1 + jf/\frac{G.B}{R_F}}\right)$$

where $G.B = f_p Z_{TO}$

f_p closed $= \underline{G.B/R_F} \Rightarrow$ determined by R_F

Gain determined by R_1

$$A_C = \left(1 + \frac{R_F}{R_1}\right)$$

(7/7)

IT

Answers to question 6:

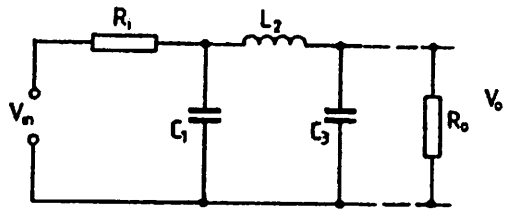
a. General transformation rules for ladder prototypes:

Inductor: $\frac{f_c L_2}{R_s} = \frac{C_{L2}}{C_u}$

Capacitor: $\frac{C_{c3}}{C_u} = f_c R_s C_3$

Resistor Rs=dummy scalar.

The circuit is equivalent to an RLC prototype



[5/10]

For switched capacitor equivalent:
C_{c1}=Cc3=10.12 pF
C_{L2}=6.98 pF.
C_u=1pF
Assume scaling Rs=Ri=Ro=1Ω

Therefore
L2= CL2/fc= $6.98/200\text{x}10^3=3.49\text{x}10^{-5}$ H

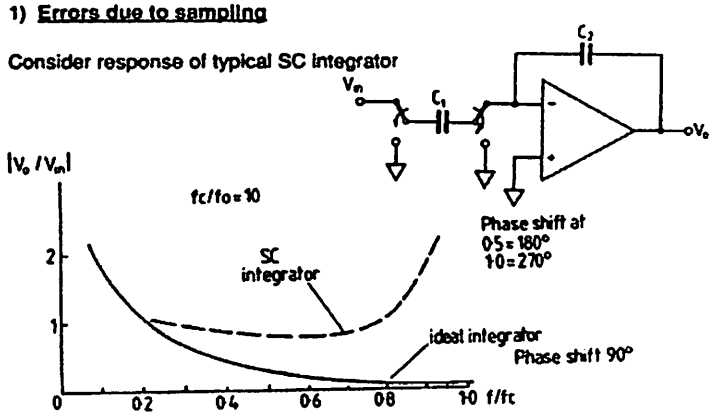
Normalised 1rad/sec we multiply by $2\pi f_0$
L2=$3.49\text{ x}10^{-5}$ x 2π x 10 KHz =2.192 H
C1=C3=Cc3/fc = $10.12/200\text{x}10^3 =5.08\text{x}10^{-5}$ f
Normalised value C1=C3=3.192 f

[5/10]

b) Explain about amplitude and phase error.

1) Errors due to sampling

Consider response of typical SC integrator



Exact expression for SC integrator

$$V_o/V_{in} = \frac{1}{jf/fo} \cdot \left[\frac{\omega/fc}{2\sin\omega/2fc} \right] \cdot \exp(-j\omega/2fc)$$

IDEAL INTEGRATOR — AMPLITUDE ERROR — PHASE ERROR

For f/fc → 0 where $\omega = 2\Pi f$

$V_o/V_{in} = 1/jf/fo$ response ideal and continuous.

For fc > f descrete time - non-ideal.

Limitation on clock frequency:
f_c> 10 x maximum input frequency.

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c)Antialiasing of smoothing filters at the output may be used to filter out the sampling components.

[2/2]