E4.16
AO5

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2005

MSc and EEE PART IV: MEng and ACGI

Corrected Copy

CURRENT-MODE ANALOGUE SIGNAL PROCESSING

Mistake in captions of fig 3.1 fig 6.1

Tuesday, 17 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : E. Drakakis
Second Marker(s) : E. Rodriguez-Villegas

Special instructions for candidates and invigilators

The following mathematical relations are provided:

$$\sinh(x) = \frac{e^{x} - e^{-x}}{2}$$

$$\cosh(x) = \frac{e^{x} + e^{-x}}{2}$$

$$\cosh^{2}(x) - \sinh^{2}(x) = 1$$

The Questions

1 Consider a current feedback op-amp (CFOA) with a transimpedance of

$$Z_T = \frac{Z_0}{(1+s\tau_1)(1+s\tau_2)} \qquad (1)$$

$Z_0 = 1$ V/μA , $\tau_1 = 159$ ns, $\tau_2 = 1.59$ ns , current input impedance $Z_n = 100\ \Omega$ and gain node capacitance $C_{comp} = 1.59$ pF.

(a) Draw an equivalent circuit of this CFOA connected in a non-inverting voltage amplifier configuration. [5]

(b) Calculate symbolically the closed loop transfer function of this inverting amplifier. Make any reasonable approximations arising from the numbers given. [8]

(c) Choose the values of external resistors for a voltage gain of 2 and the greatest possible bandwidth. What is the bandwidth? What is the quality factor of this amplifier? Comment on what would happen if the gain node capacitance was omitted. [7]

2. In this question we investigate the effect of finite transistor speed on SI filter design.

(a) Draw the circuit diagram for a first generation switched current copier with gain $G = i_{out} / i_{in}$.

i What is the sign of the gain?

ii What is the delay of this cell in terms of the switching frequency?

iii. What values of gain would then be achievable if the technology only allows a single transistor size? What would the achievable gain tolerance be? [3]

(b) Calculate the transfer function of a continuous time current mirror with gain G in terms of the signal frequency, the process transit frequency and the gain G. Show that the current mirror is a lossy integrator and calculate its pole frequency. Assume the transistors are operating linearly, so that $i_{ds} = g_m v_{gs}$, and that the transistor transit frequency is approximately $f_T \simeq \frac{g_m}{2\pi C_{gs}}$. How is the transfer function, and pole location modified if the mirror has several outputs? [4]

(c) Consider the SI cell in (a) as a zero order hold. The transfer function of a zero-order hold is: $H(s) = \sin c(s\tau) = \sin(s\tau)/s\tau$, with τ the sampling interval.
The SI cell has N outputs of gain $|G| < 1$

i. Calculate the maximum baseband frequency that will ensure $|G| > 0.99$ (hint: perform a Taylor expansion on the transfer function H) [2]

ii. Taking into account the mirror transfer function calculate the maximum sampling frequency that will lead to a mirror gain $|G| > 0.99$. Express your answer in terms of the transistor transit frequency f_T. [2]

iii Combine your answers in c(i) and c(ii) to deduce the maximum baseband frequency for which the SI cell will have a gain error less than 1%. The transit frequency of the transistors is $f_T = 10$ GHz and only discrete transistor sizing is allowed. [2]

(d) Finally consider using SI cells to implement an IIR filter of order N.

i. Draw a block diagram showing ALL the SI delay elements that will be used. Estimate the number of SI cells needed. [3]

ii. Assuming that the gain error is linearly cumulative, and that the filter coefficients for an order N filter need to be determined to an accuracy of $1/N^2$ %, calculate the maximum SI filter order that can be applied to the standard audio bandwidth of 20 kHz if the transit frequency is $f_T = 10$ GHz. At what frequency would you need to operate the switching elements? [4]

(a) Define any 2 families of the current conveyor. Write the design equation for each in matrix form. Give examples of a single device that approximates each one. [4]

(b) Design a current mode high pass Sallen-Key filter using a current conveyor CII+ as the gain element.

i. Convert the circuit of figure 3.1 to its current mode dual circuit using an appropriate current amplifier. Draw the schematic of this current mode high pass filter. [4]

ii. Draw a schematic of a realization of the necessary current mode amplifier in terms of CII+ elements. Make sure the gain has the correct sign. [4]

iii Derive the current mode transfer function of your circuit if $R_1 = R_2 = R$, $C_1 = C_2 = C$. The generic high-pass filter transfer function is:

$$H(s) = H_0 \frac{s^2/\omega_0^2}{s^2/\omega_0^2 + 2\zeta s/\omega_0 + 1}$$

where $\zeta = \frac{1}{2Q}$ is the damping factor and ω_0 the filter break frequency. H_0 is the maximum gain of the filter occurring at very high frequency. Write expressions for Q and ω_0 in terms of R, C, K. [4]

iv Draw a transistor level representation of a CCII+ current conveyor. On the basis of your schematic deduce the simplest possible form the transfer function your gain element in (ii) above can have. What is the effect of such a transfer function on your current mode filter response? [4]

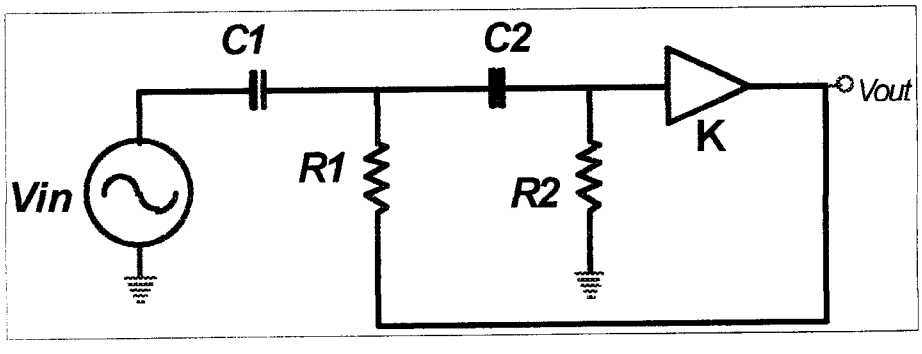


Figure 3.1: A voltage mode Sallen Key High Pass filter for question 2(b)

(a) Derive the bipolar translinear principle with reference to a loop containing an even number n=2*m of base-emitter junctions. State all the assumptions that you make and list the conditions which must be satisfied in order for this principle to be valid. [5]

(b) List the main differences between the Bipolar and the MOS translinear principles. [2]

(c) Figure 4.1 illustrates a translinear circuit. If I_z and I_{in} are the output and input currents respectively and I is a dc current of known value, show that $I_z = |I_{in}|$ (absolute value circuit). [5]

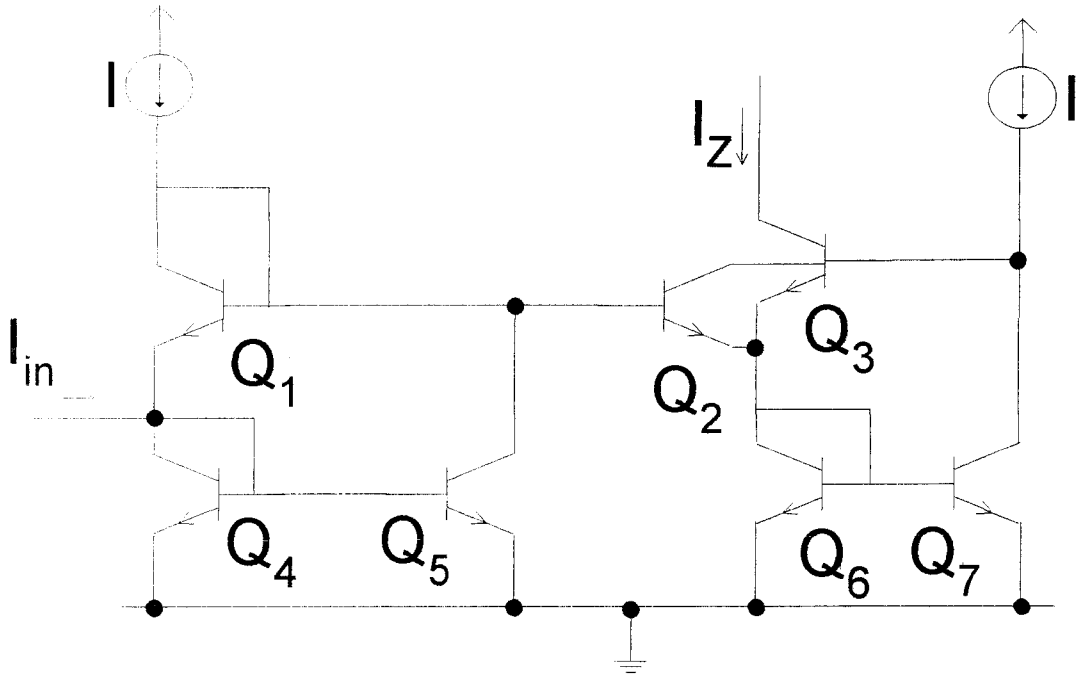


Figure 4.1: Circuit for question 4(c)

(d) Figure 4.2 illustrates a translinear circuit whose differential output realises a trigonometric approximation.

(i) Show that $\frac{I_6}{I_7} = \frac{2(1-X)^2}{(2+X)^2}$ and determine I_6 and I_7 as a function of the modulation index X and the known current I. [2]

(ii) Explain why $\frac{I_9}{I_{10}} = \frac{I_6}{I_7}$ and determine I_9 and I_{10} as a function of X and the known current I. [2]

(iii) Express I_2 and I_3 as a function of X and the known current I. [2]

(iv) Express the differential current output $I_{z_1} - I_{z_2}$ as a function of X and the known current I. [2]

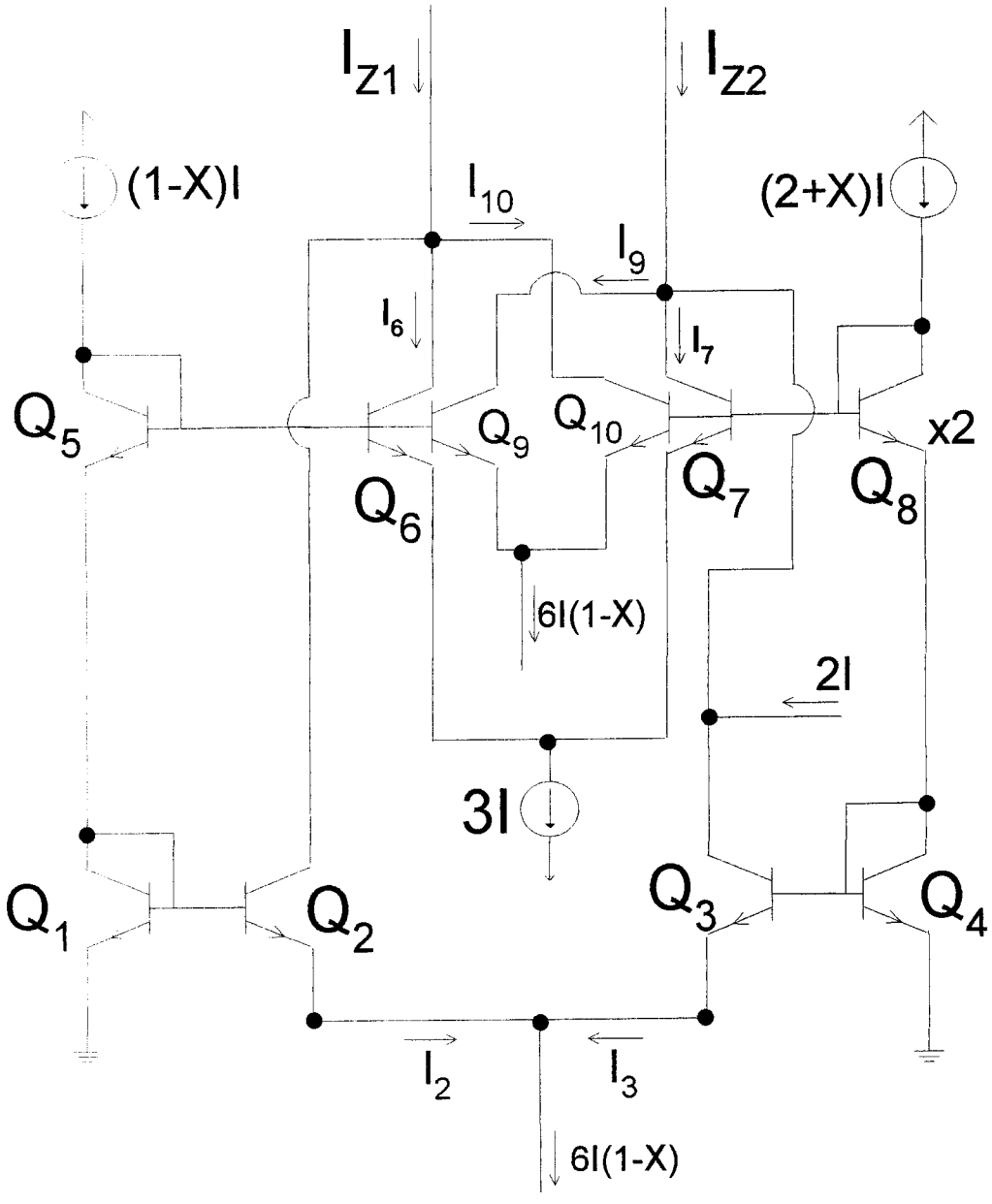


Figure 4.2: Circuit for question 4(d)

5

(a) Figure 5.1 illustrates a general companding circuit.

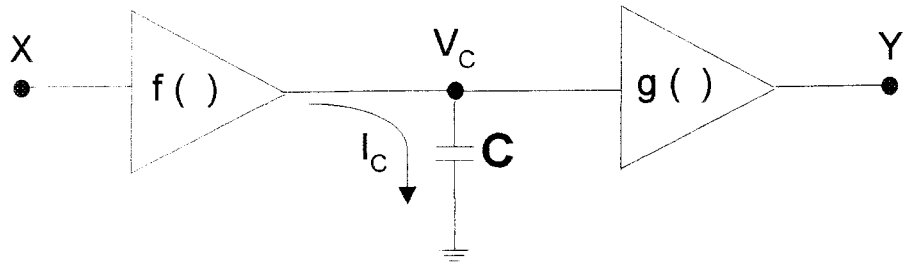


Figure 5.1: A companding circuit for question 5(a)

(i) Derive the condition under which the circuit operates as an input-output linear integrator. [2]

(ii) If the input signal X is a current of value I_{in} and the output signal Y is a current $g(V_C) = I_T \sinh(\alpha V_C)$ with $\alpha = V_T^{-1}$ and I_T a constant with dimensions of current, show that in order for the circuit to operate as an input-output linear companding integrator of the form $Y = \omega_0 \int X\,dt$, the function $f(\ )$ should be of the form: $f(\ ) \propto \left(X \Big/ \sqrt{(I_T)^2 + Y^2} \right)$. [4]

(b) The transfer function for a second order topology has been decomposed into the following state-space equations:

$$\dot{x}_1 = -\left(\frac{\omega_0}{2Q}\right)x_1 - \omega_0\left(1 - \frac{1}{4Q^2}\right)x_2 + \omega_0 U$$

$$\dot{x}_2 = \omega_0 x_1 - \left(\frac{\omega_0}{2Q}\right)x_2$$

$$y_1 = x_1$$

$$y_2 = x_2$$

where y is the output, x_1 and x_2 are state-variables and U is the input (a dot above a variable denotes time-differentiation).

(i) Show that the output y_1 implements a "two-pole-one-zero" frequency response, whereas y_2 implements a second order low-pass transfer function. [2]

(ii) Using the exponential mappings $x_j = I_0 \exp\left(\frac{V_j}{V_T}\right) (j = 1,2)$ and

$U = I_S \exp\left(\frac{V_U}{V_T}\right)$ show that the above linear state-space equations can be transformed into non-linear log-domain design equations. (I_S denotes the reverse saturation current of a bipolar junction transistor).

[5]

(iii) Sketch a transistor-level implementation of a log-domain topology which realises these design equations.

[7]

6

(a) Describe the condition which is satisfied if two networks are "adjoint networks". What is the advantage of using the adjoint network principle to derive current-mode circuits from existing voltage-mode circuits? Show that the adjoint network of a voltage amplifier is a current amplifier, but with the input and output ports interchanged. [4]

(b) Figure 6.1 shows a second order filter implemented using voltage op-amps, where V_{LP}, V_{HP} and V_{BP} are low-pass, high-pass and band-pass outputs respectively. Using the adjoint principle, derive the current-mode equivalent circuit. [3]

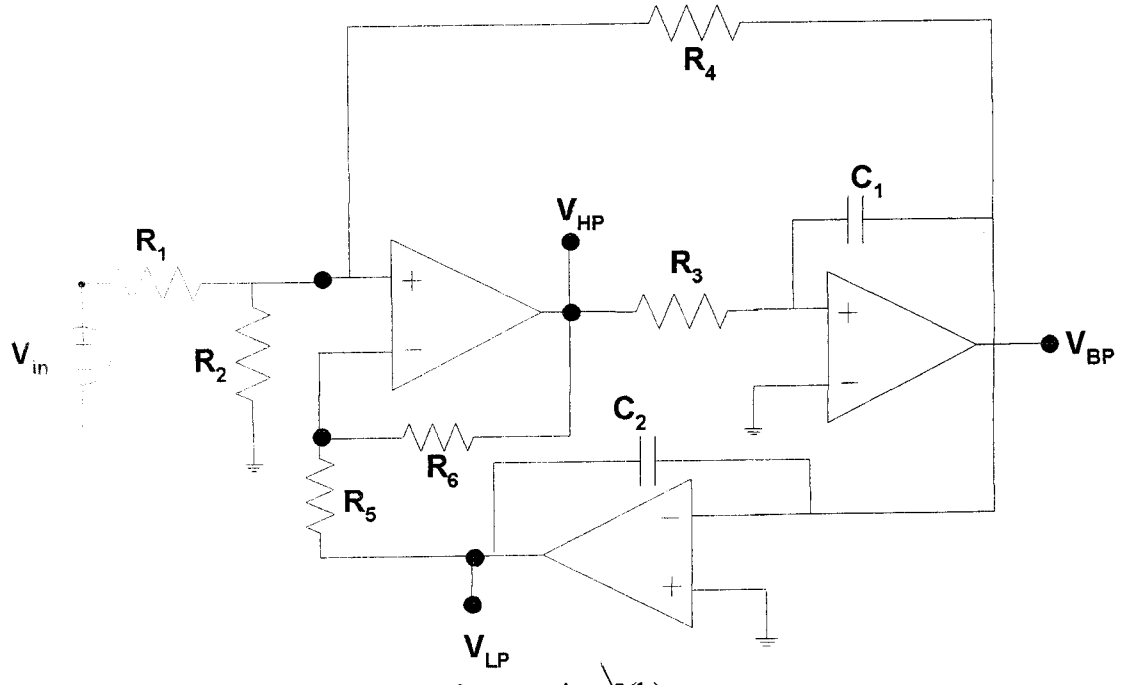


Figure 6.1: Second order filter for question 5(b)

(c) You are required to implement the closed-loop $I - I$ converter shown in Figure 6.2 by means of one of the four "ideal" amplifiers.

(i) State the four "ideal" amplifiers, their open-loop gain function and their ideal input and output impedances. [1]

(ii) Provided that the source and load impedances in Figure 6.2 are unknown, which of the four "ideal" amplifiers you would choose in order to implement the block A? Justify your reasoning. [2]

(iii) Assuming that each of the "ideal" amplifiers has ideal input and output impedance levels but finite open-loop gain and bandwidth, derive an expression for the frequency-dependent closed-loop gain of the configuration you have selected. [3]

(iv) Comment on both the advantage and the disadvantage of the configuration you have selected. [2]

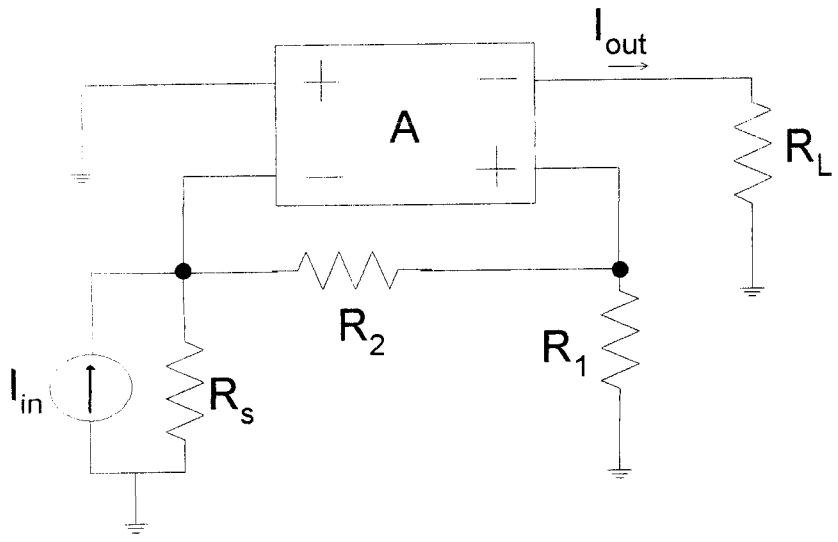


Figure 6.2: I-I converter of question 6(c)

(d) Figure 6.3 shows the architecture of a simple current-follower, where the symbols CM represent current mirrors with an arrow marking the input side. Derive expressions for the D.C. input offset voltage and small-signal input resistance at node X. Explain with the aid of a diagram in each case, how the circuit can be modified to:
Reduce the D.C. offset without increasing the small-signal input resistance [5]

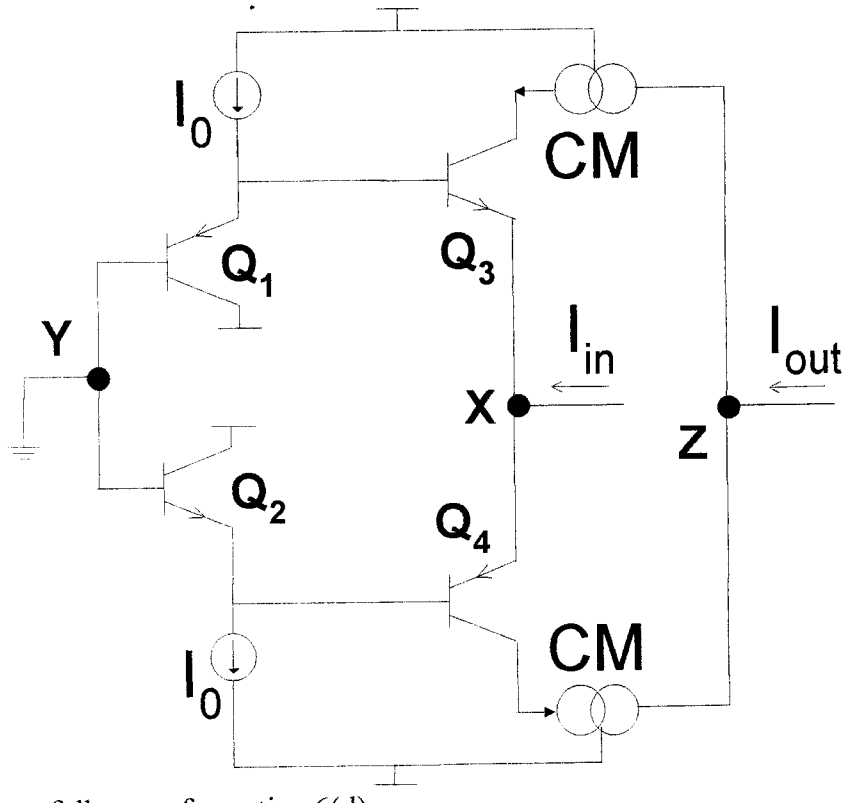


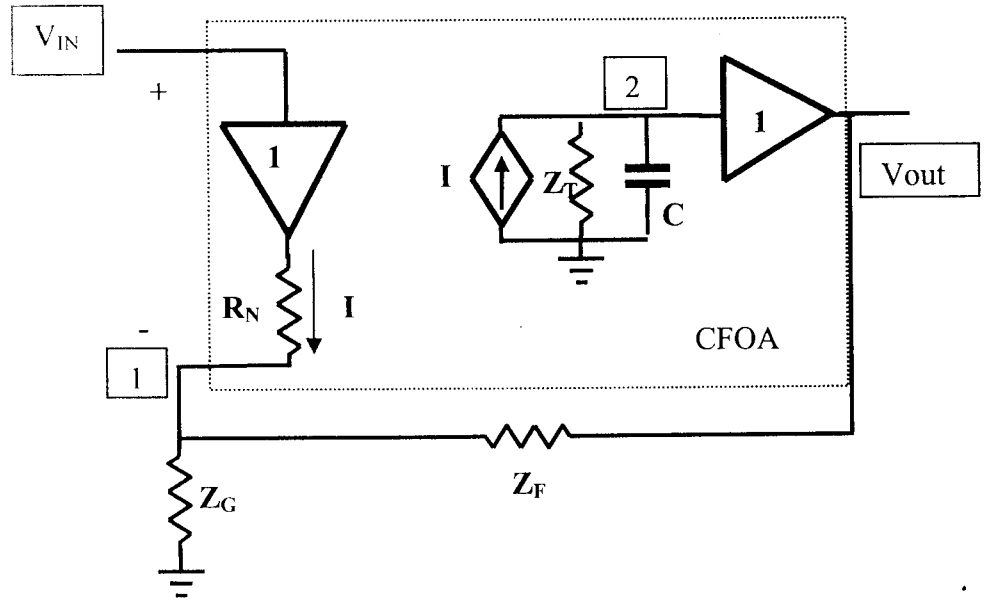
Figure 6.3: Current follower of question 6(d)

2005

E4.16 – AO5: Current Mode Analogue Signal Processing : Model Answers

Q1: **[Application of Theory]**

a)



[5]

b)

$$I_{out} = IZ_T \,//\, sC = I\frac{Z_T}{1+Z_T sC} = I\frac{Z_0}{(1+s\tau_1)(1+s\tau_2)+Z_0 sC}$$

$I = (V_+ - V_-)/R_N$ then,

$$I_{out} = (V_+ - V_-)\frac{Z_0/R_N}{(1+s\tau_1)(1+s\tau_2)+Z_0 sC} =$$

$$= (V_+ - V_-)\frac{Z_0/R_N}{1+s(\tau_1+\tau_2+\tau_3)+s^2\tau_1\tau_2} = G(s)(V_+ - V_-)$$

$\tau_3 = Z_0 C = 1\cdot 10^6 \cdot 1.59\cdot 10^{-12} = 1.59\mu s$

assuming $Z_F, Z_G >> R_N$,

$$V_- = V_{out}\frac{R_G}{R_F+R_G} = HV_{out}$$

putting all together,

$$\frac{V_{out}}{V_{in}} = \frac{G}{1+GH} = \frac{(R_G+R_F)G(s)}{R_G+R_F+R_G G(s)} =$$

$$= \frac{(R_G+R_F)Z_0/R_N}{(R_G+R_F)\left(1+s(\tau_1+\tau_2+\tau_3)+s^2\tau_1\tau_2\right)+R_G Z_0/R_N} =$$

$$= \left(\frac{(R_G+R_F)Z_0/R_N}{(R_G+R_F)+R_G Z_0/R_N}\right)\left(\frac{1}{1+2\zeta s/\omega_0+s^2/\omega_0^2}\right)$$

with

$$\omega_0 = \sqrt{\frac{R_G+R_F+R_G Z_0/R_N}{R_G+R_F}\frac{1}{\tau_1\tau_2}}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{R_G+R_F}{R_G+R_F+R_G Z_0/R_N}}\frac{\tau_1+\tau_2+\tau_3}{\sqrt{\tau_1\tau_2}}$$

[8]

c)

Putting some numbers in, $Z_0/R_N = 10^4$ so

$$\frac{V_{out}}{V_{in}} = \left(\frac{(R_G+R_F)10^4}{(R_G+R_F)+10^4 R_G}\right)\left(\frac{1}{1+2\zeta s/\omega_0+s^2/\omega_0^2}\right) \simeq$$

$$\left(1+\frac{R_F}{R_G}\right)\left(\frac{1}{1+2\zeta s/\omega_0+s^2/\omega_0^2}\right)$$

this is a 2nd order LPF with

$$\omega_0 = \sqrt{\frac{R_G+R_F+R_G Z_0/R_N}{R_G+R_F}\frac{1}{\tau_1\tau_2}} \simeq 10^9\,Hz\sqrt{\frac{R_G}{R_F+R_G}} \simeq 10^9\,Hz\sqrt{G}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{R_G+R_F}{R_G+R_F+R_G Z_0/R_N}}\frac{\tau_1+\tau_2+\tau_3}{\sqrt{\tau_1\tau_2}} \simeq \frac{1}{2}\sqrt{G}$$

Then with a gain of 2, $R_G = R_F$ and $\zeta = \frac{1}{2Q} = 1/\sqrt{2}$ so the amplifier is critically damped.

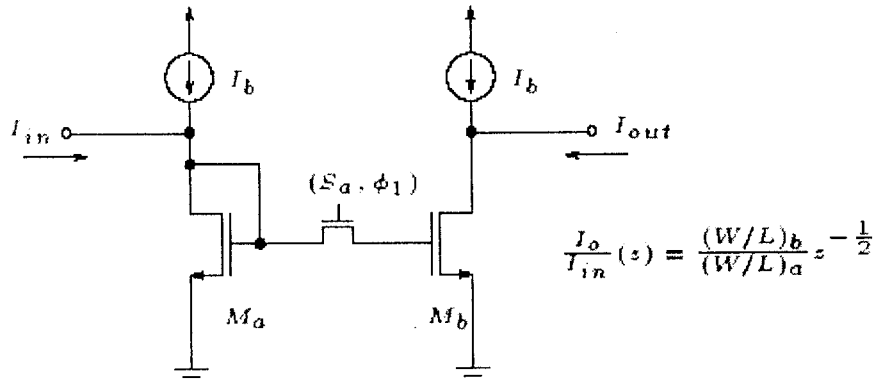
a decrease of the input impedance would lead to a higher Q, since $Q \propto \sqrt{R_N}$, but also to a higher bandwidth. The gain node capacitance contributes to the damping factor, eg for the numbers given the amplifier would have a Q=7 with no gain node capacitance. With the model given the gain node capacitance does not affect the bandwidth.

[8]

2. **[Extension of theory- application problem]**

ANSWER:

a-b)



If arbitrary sizing is not available then a is a shunt connection of M transistors and b a connection of N transistors. The gain is $\frac{W_b}{W_a} = -\frac{N}{M}$ the delay half a period, and the achievable coefficient accuracy is 1/M.

[3]

c) By nodal analysis it follows that

$$i_{out} = i_{in}\frac{g_{mb}}{g_{ma} + s\left(C_{gsa} + C_{gsb}\right)} = i_{in}\frac{W_b}{W_a}\frac{1}{1 + s\frac{(1+G)C_{gsa}}{g_{ma}}} = i_{in}\frac{G}{1 + j(1+G)f/f_T}$$

the pole is clearly at $f_p = f_T/(1+G)$

If the mirror has N outputs then $f_p = f_T/(1+N\max G)$

The gain accuracy is then $\delta G = \frac{1}{2}\frac{f}{f_p}$

[4]

c) A taylor expansion on H(s) gives: $H(s) = \text{sinc}(s\tau) \approx 1 + \frac{1}{6}(s\tau)^2$. Then the required 1% accuracy is obtained if $\frac{1}{6}(s\tau)^2 < 0.01 \Rightarrow s\tau < \sqrt{0.06} = 0.244 \Rightarrow f_b < \frac{1}{2\pi} f_s 0.244 = 0.04 f_s$

[2]

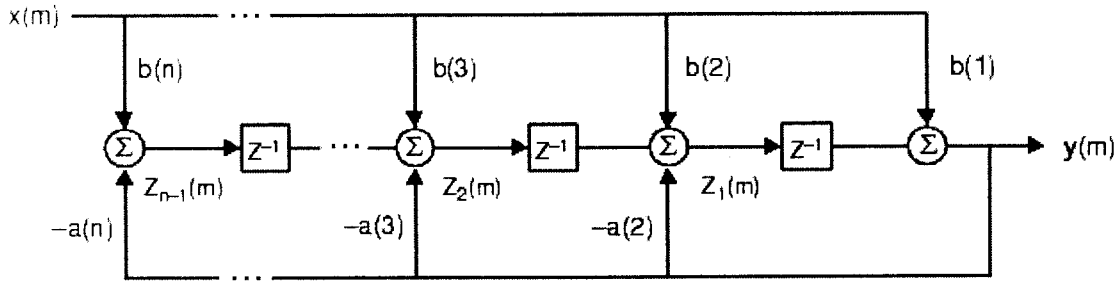
At the same time, we wish $\delta G = \frac{1}{2}\frac{f_s}{f_p} < 0.01 \Rightarrow f_s < 0.02 f_p < 0.02 f_T/(1+N)$

[2]

combining, we get $f_b < 0.0008 f_T / N$ or approx 4MHz for a single output SI mirror

[2]

(d) many possible topologies, for example:



[3]

The signal path now has approx 2N elements (at half a period per element) and N output elements are also needed. (plus CT sign inversions, but the student will miss this) This means that we are going for

$f_c < 0.0008 f_T / 2N^4$ substituting $f_T = 10GHz$ and $f_b = 20kHz$ we get $N < \sqrt[4]{20 \cdot 10^2} \approx 6.7$.

We would need to switch this filter at approximately $f_s = f_b / 0.04 = 500kHz$.

[4]

3. [some bookwork, applications problem-theory verification]

a) First generation – finite current at current input – BJT

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

Second generation – zero input current – FET

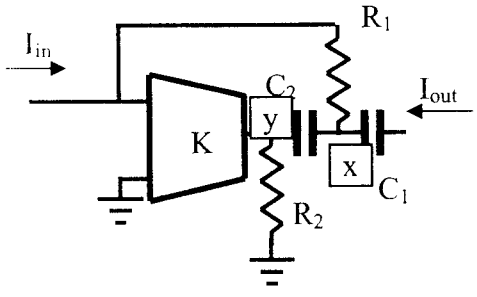
$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

Third generation as first generation but negative unity current at voltage input. Ideal current meter.

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

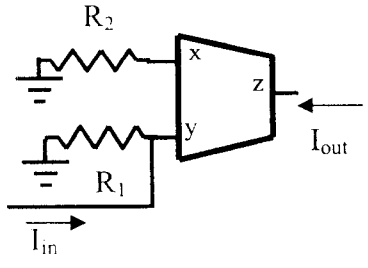
[4]

b) i) The circuit is as given with a current amp replacing the voltage amp, its input at the voltage amp output. The voltage source becomes the load.



[4]

ii) But we need a current amp of gain K, so we need to synthesize this first:



Since $V_x = V_y = I_{in}R_1$

$I_{out} = -V_x / R_2 = -I_{in}R_1 / R_2$

This amplifier is inverting, suitable for a positive feedback connection (the sense of the current flow is not reversed.

[4]

iii) Nodal analysis on node x

$$-V_x\left(sC+R\right)+\left(V_y-V_x\right)sC=0\Rightarrow V_x\left(2sC+R=V_ysC\right)\Rightarrow$$

$$V_x\left(1+2s\tau\right)=V_ys\tau$$

Nodal analysis on node y:

$$K\left(I_{in}+V_x/R\right)+\left(V_y-V_x\right)sC+V_yR=0\Rightarrow$$

$$KI_{in}R+V_x\left(K-s\tau\right)+V_y\left(1+s\tau\right)=0$$

eliminate V_y :

$$KI_{in}R+V_x\left(K-s\tau\right)+V_x\left(1+2s\tau\right)\left(1+s\tau\right)/s\tau=0\Rightarrow$$

$$KI_{in}R+V_x\left(Ks\tau-s^2\tau^2+1+2s\tau+2s^2\tau^2\right)/s\tau=0$$

but $V_x=-I_{out}sC$ so :

$$KI_{in}=I_{out}\frac{\left(Ks\tau+1+2s\tau+s^2\tau^2\right)}{s^2\tau^2}\Rightarrow$$

$$\frac{I_{out}}{I_{in}}=\frac{Ks^2\tau^2}{s^2\tau^2+\left(2+K\right)s\tau+1}$$

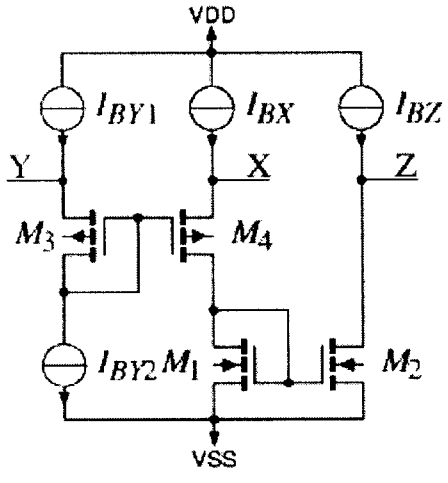
$$\omega_0=1/RC$$

With K<0 as designed. We get : $\zeta=1/2Q=2-\left|K\right|$

$$H_0=K$$

[4]

iv) The simplest possible CCII+ is a FET, but this is a CCI-. We need to add a current mirror to turn it into a CCII+. All considered, two current mirrors suffice:



There are two mirrors, one with a pole at $f_{Tp}/2$ and the other at $f_{Tn}/2$ the p and n channel f_T respectively. If K has 2 poles, the filter becomes 4th order, 2 zeroes and 4 poles, and as a result it has a low pass characteristic!

[4]

Question 4

(a) Assumptions & conditions:

(BookWork) Equal number of CW & ACW npn junctions

" " " " " " " " pnp " "

Same V_T (i.e. temperature) for all devices

All npn (pnp) devices have the same current density J_{sn} (J_{sp}) (matching of n & p devices)

When the above hold:

$$CW \sum_{j=1}^{m} V_{be_j} = ACW \sum_{j=1}^{m} V_{be_j} \Rightarrow$$

$$\Rightarrow CW \sum_{j=1}^{m} V_T \ln\left[\frac{I_{c_j}}{J_{s_j} A_j}\right] = ACW \sum_{j=1}^{m} V_T \ln\left[\frac{I_{c_j}}{J_{s_j} A_j}\right] \Rightarrow$$

$$\Rightarrow CW \prod_{j=1}^{m}\left[\frac{I_{c_j}}{J_{s_j} A_j}\right] = ACW \prod_{j=1}^{m}\left[\frac{I_{c_j}}{J_{s_j} A_j}\right] \Rightarrow$$

$$\Rightarrow CW \prod_{j=1}^{m}\left[\frac{I_{c_j}}{A_j}\right] = ACW \prod_{j=1}^{m}\left[\frac{I_{c_j}}{A_j}\right] \quad [5]$$

Bipolar translinear principle

(b) MOS TLP: $$CW \sum_{j=1}^{m} \sqrt{\frac{I_{D_j}}{K_j}} = ACW \sum_{j=1}^{m} \sqrt{\frac{I_{D_j}}{K_j}}$$

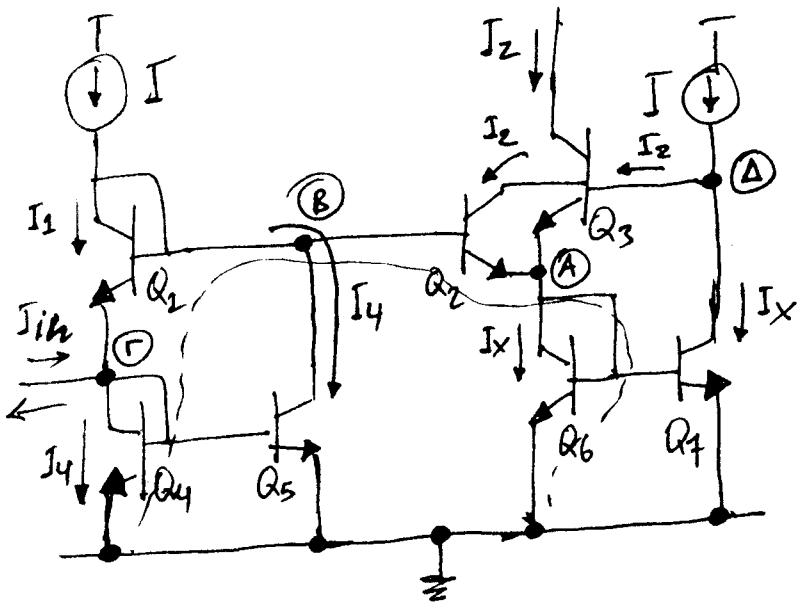
$$K_j = \frac{\mu C_{ox}}{2} \frac{W}{L}$$

(BookWork)

Differences of MOS TLP vs BJT TLP:

- "Sum of roots" vs bipolar "products"
- MOS $()^2$ law holds over a smaller current range than the bipolar exponential law
- process parameters do not cancel (need of balancing) automatically for "mixed" (NMOS & PMOS) TL loops [2]
- no suffering from beta errors.

(c)



Exercise based on tought material

KCL at (A): $I_z + I_2 = I_x$

KCL at (Δ): $I_x + I_2 = I$

KCL at (B): $I = I_1 + I_4$

KCL at (Γ): $I_1 + I_{in} = I_4$

$\Rightarrow$ $I_2 = \frac{I - I_z}{2} \Rightarrow I_x = \frac{I + I_z}{2}$

$I_4 = \frac{I + I_{in}}{2} \Rightarrow I_1 = \frac{I - I_{in}}{2}$

TLP along $Q_4 Q_1 Q_2 Q_6 \Rightarrow I_4 I_1 = I_2 I_x \Rightarrow$

$\Rightarrow \frac{I + I_{in}}{2} \frac{I - I_{in}}{2} = \frac{I - I_z}{2} \frac{I + I_z}{2} \Rightarrow$

$\Rightarrow I^2 - I_{in}^2 = I^2 - I_z^2 \Rightarrow$

$\Rightarrow I_z = |I_{in}| \Rightarrow$ absolute value circuit

[5]

(Exercise based on taught material)

(d) i) & ii)

TLP along $Q_1 Q_5 Q_6 Q_7 Q_8 Q_4$ $\Rightarrow$

$$\Rightarrow (1-x)I\,(1-x)I\,I_7 = \frac{(2+x)I}{2}\,(2+x)I_6 \Rightarrow$$

$$\Rightarrow \frac{I_6}{I_7} = \frac{2(1-x)^2}{(2+x)^2}$$

TLP along $Q_6 Q_9 Q_{10} Q_7$ $\Rightarrow$

$$\Rightarrow I_6\, I_{10} = I_9\, I_7 \Rightarrow \frac{I_6}{I_7} = \frac{I_9}{I_{10}}$$

$$I_9 + I_{10} = 6I(1-x)$$

$$I_6 + I_7 = 3I$$

$$\frac{I_6}{I_7} = \frac{2(1-x)^2}{(2+x)^2} \Rightarrow \frac{\overbrace{I_6+I_7}^{3I}}{I_7} = \frac{2(1-x)^2+(2+x)^2}{(2+x)^2} \Rightarrow$$

$$\Rightarrow \boxed{I_7 = \frac{(2+x)^2}{2(1-x)^2+(2+x)^2}\,3I} \Rightarrow$$

$$\Rightarrow \boxed{I_6 = 3I - I_7 = \frac{2(1-x)^2}{(2+x)^2+2(1-x)^2}\,3I}$$

$$\frac{I_9}{I_{10}} = \frac{I_6}{I_7} = \frac{2(1-x)^2}{(2+x)^2} \Rightarrow$$

$$\frac{\overbrace{I_9+I_{10}}^{6I(1-x)}}{I_{10}} = \frac{2(1-x)^2+(2+x)^2}{(2+x)^2} \Rightarrow \boxed{I_{10} = \frac{(1-x)(2+x)^2}{2(1-x)^2+(2+x)^2}\,6I} \Rightarrow$$

$$\Rightarrow \boxed{I_9 = \frac{2(1-x)^3}{2(1-x)^2+(2+x)^2}\,6I}$$

[4]

iii) TLP along $Q_1 Q_2 Q_3 Q_4$ =>

=> $(1-X)I_3 = I_2 (2+X)$ =>

=> $\frac{I_2}{I_3} = \frac{1-X}{2+X}$ => $\frac{I_2+I_3}{I_3} = \frac{1-X+2+X}{2+X}$ => $6I(1-X)$

$I_2 + I_3 = 6I(1-X)$ => $I_3 = \frac{2+X}{3}(1-X)\frac{2}{6}I$ =>

=> $\boxed{I_3 = (2+X)(1-X)\,2I}$ =>

=> $\boxed{I_2 = (1-X)^2\,2I}$

[2]

iv) $I_{Z_1} = I_2 + I_6 + I_{10} = \ldots\ldots$

$I_{Z_2} = I_9 + I_7 + (I_3 - 2I) = \ldots\ldots$

$I_2, I_6, I_{10}, I_9, I_7$ & I_3 are given as a function of I & X in i), ii) & iii) above.

[2]

Question 5

a) (Exercise based on taught material)

i) $Y = g(V_c)$

$f(x) = I_c = C\frac{dV_c}{dt}$

For linear integration

$Y = K\int x\,dt \Rightarrow$

$\Rightarrow \frac{dY}{dt} = Kx \Rightarrow$

$\Rightarrow \frac{dY}{dV_c}\frac{dV_c}{dt} = Kx \Rightarrow \frac{dg(V_c)}{dV_c}\frac{f(x)}{C} = Kx$

$\Rightarrow f(x) = \frac{KCX}{\left[\frac{dg(V_c)}{dV_c}\right]} = \frac{\omega_o C X}{\left[\frac{dg(V_c)}{dV_c}\right]}$ when $K = \omega_o$ rad/sec [2]

$\sinh(\alpha V_c) = \frac{e^{\alpha V_c} - e^{-\alpha V_c}}{2}$

ii) when $g(V_c) = I_T \sinh\left(V_c/V_T\right) \Rightarrow$ (Y)

$\frac{dg(V_c)}{dV_c} = \frac{I_T}{V_T}\cosh(\alpha V_c) \Rightarrow$

$\frac{dg(V_c)}{dV_c} = \frac{I_T}{V_T}\cdot\sqrt{1+\sinh^2(\alpha V_c)} \Rightarrow$

$\Rightarrow \frac{dg(V_c)}{dV_c} = \frac{I_T}{V_T}\sqrt{1+\frac{Y^2}{I_T^2}} = \frac{\sqrt{I_T^2+Y^2}}{V_T} \Rightarrow$

$\Rightarrow f(x) = \frac{\omega_o C X}{\frac{\sqrt{I_T^2+Y^2}}{V_T}} = \frac{(\omega_o C V_T)\,X}{\sqrt{I_T^2+Y^2}}$ (I_o) [4]

(Exercise based on tought material)

b) i)

$$\left.\begin{aligned} \dot{x}_1 + \left(\frac{w_0}{2Q}\right) x_1 + w_0\left(1-\frac{1}{4Q^2}\right) x_2 &= w_0 v \\ -w_0 x_1 + \dot{x}_2 + \left(\frac{w_0}{2Q}\right) x_2 &= 0 \\ y_1 = x_1 \\ y_2 = x_2 \end{aligned}\right\} \Rightarrow$$

$$\left[s+\frac{w_0}{2Q}\right] X_1(s) + w_0\left(1-\frac{1}{4Q^2}\right) X_2(s) = w_0 V(s)$$

$$-w_0 X_1(s) + \left[s+\frac{w_0}{2Q}\right] X_2(s) = 0$$

$$D = \begin{vmatrix} s+\frac{w_0}{2Q} & w_0\left(1-\frac{1}{4Q^2}\right) \\ -w_0 & s+\frac{w_0}{2Q} \end{vmatrix} = s^2 + \left(\frac{w_0}{Q}\right)s + w_0^2 .$$

$$D_{X_1} = \begin{vmatrix} w_0 V(s) & w_0\left(1-\frac{1}{4Q^2}\right) \\ 0 & s+\frac{w_0}{2Q} \end{vmatrix} = w_0\left(s+\frac{w_0}{2Q}\right) V(s)$$

$$D_{X_2} = \begin{vmatrix} s+\frac{w_0}{2Q} & w_0 V(s) \\ -w_0 & 0 \end{vmatrix} = w_0^2 V(s)$$

$$\frac{Y_1(s)}{V(s)} = \frac{X_1(s)}{V(s)} = \frac{w_0\left(s+\frac{w_0}{2Q}\right)}{s^2+\left(\frac{w_0}{Q}\right)s+w_0^2}$$ "2 pole - 1 zero"

$$\frac{Y_2(s)}{V(s)} = \frac{X_2(s)}{V(s)} = \frac{w_0^2}{s^2+\left(\frac{w_0}{Q}\right)s+w_0^2}$$ "LP biquad" [2]

ii)

$$\left.\begin{aligned} x_1 &= I_0 e^{V_1/V_T} \\ x_2 &= I_0 e^{V_2/V_T} \end{aligned}\right\} \Rightarrow \left.\begin{aligned} \dot{x}_1 &= x_1 \frac{\dot{V}_1}{V_T} \\ \dot{x}_2 &= x_2 \frac{\dot{V}_2}{V_T} \end{aligned}\right.$$

$$\left.\begin{aligned} x_1 \frac{\dot{V}_1}{V_T} + \left(\frac{\omega_0}{2Q}\right) x_1 + \omega_0 \left(1 - \frac{1}{4Q^2}\right) x_2 &= \omega_0 v \\ -\omega_0 x_1 + x_2 \frac{\dot{V}_2}{V_T} + \left(\frac{\omega_0}{2Q}\right) x_2 &= 0 \end{aligned}\right\} \Rightarrow$$

$$\left.\begin{aligned} \frac{\dot{V}_1}{V_T} + \left(\frac{\omega_0}{2Q}\right)^{V_T} + \omega_0^{V_T} \left(1 - \frac{1}{4Q^2}\right) {}^{x_2}/_{x_1} &= \omega_0^{V_T} {}^{v}/_{x_1} \\ \frac{\dot{V}_2}{V_T} - \omega_0^{V_T} {}^{x_1}/_{x_2} + \left(\frac{\omega_0}{2Q}\right)^{V_T} &= 0 \end{aligned}\right\} \Rightarrow$$

$$C\dot{V}_1 + \frac{(\omega_0 C V_T)}{2Q}^{I_0} + (\omega_0 C V_T)^{I_0} \left(1 - \frac{1}{4Q^2}\right) e^{\frac{V_2 - V_1}{V_T}} = \frac{(\omega_0 C V_T)^{I_0}}{I_0} I_s e^{\frac{V_1 - V_1}{V_T}} \Rightarrow$$

$$C\dot{V}_2 + \frac{(\omega_0 C V_T)^{I_0}}{2Q} = (\omega_0 C V_T) e^{\frac{V_1 - V_2}{V_T}}$$

$$\Rightarrow \quad C\dot{V}_1 + \frac{I_0}{2Q} + I_0 \left(1 - \frac{1}{4Q^2}\right) e^{\frac{V_2 - V_1}{V_T}} = I_s e^{\frac{V_1 - V_1}{V_T}}$$

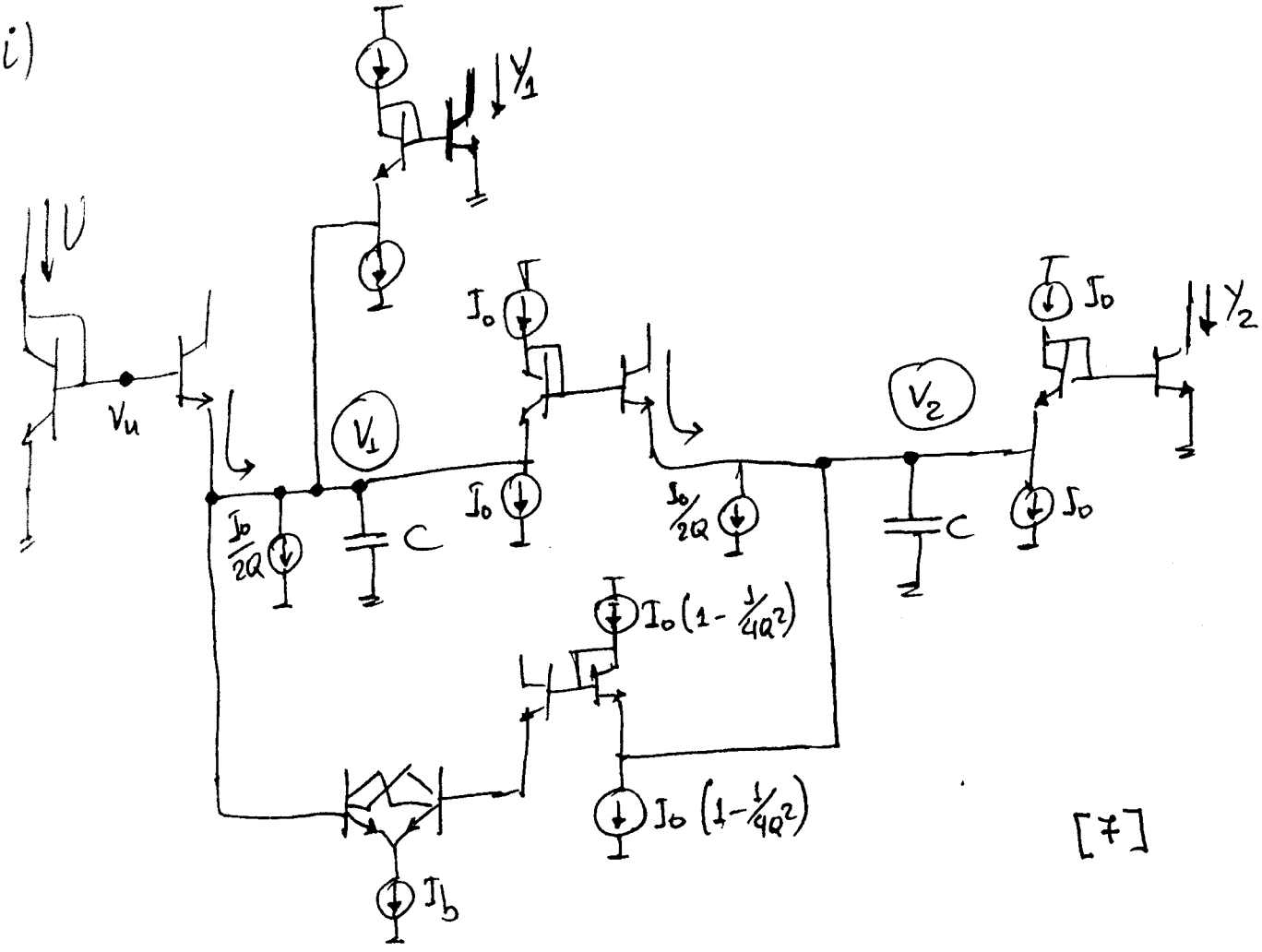
$$C\dot{V}_2 + \frac{I_0}{2Q} = I_0 e^{\frac{V_1 - V_2}{V_T}}$$

$$Y_1 = I_0 e^{V_1/V_T}$$

$$Y_2 = I_0 e^{V_2/V_T}$$

[5]

iii)


V
V_1
V_u
V_1
I_o
I_o
$\frac{I_o}{2Q}$
C
$I_o(1-\frac{1}{4Q^2})$
$I_o(1-\frac{1}{4Q^2})$
I_b
$\frac{I_o}{2Q}$
V_2
C
I_o
I_o
V_2

[7]

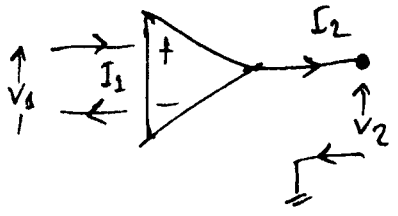
Question 6

a) Two N-port networks (A+B) are adjoint (Bookwork)

$$\sum_{n=1}^{N} \left(V_n^A I_n^B - I_n^A V_n^B \right) = 0$$

Adjoint circuits are equivalent in the voltage-mode & current-mode domain; the circuits give identical transfer functions when input & output ports are interchanged. The adjoint circuit has the same sensitivity properties as the original network; hence we can directly exploit "optimum" voltage-mode designs which already exist

Voltage Ap.



$$V^A = [V_1^A \; V_2^A] = [V_{in} \; AV_{in}]$$

$$I^A = [I_1^A \; I_2^A] = [0 \; X]$$

Adjoint Circuit: $[V_1^B \; V_2^B]$, $[I_1^B \; I_2^B]$

Hence $V_{in} I_1^B + AV_{in} I_2^B - 0\, V_1^B - \times V_2^B = 0 \Rightarrow$

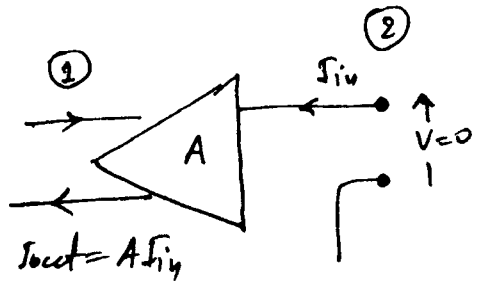
$I_1^B = -A I_{in}$

$I_2^B = I_{in}$

$V_1^B = X$

$V_2^B = 0$

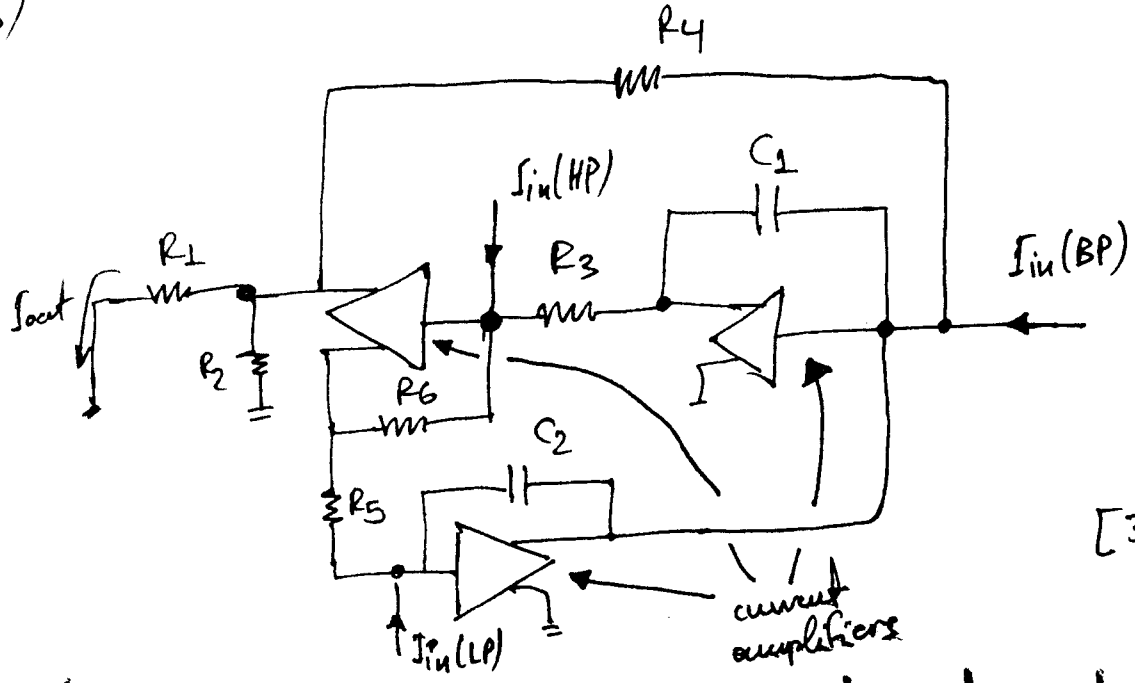
$\Rightarrow$



[4]

(Exercise based on taught material)

b)



[3]

(Design equations & Exercise based on taught material)

c)

i) Voltage amp: O/L voltage gain, $R_{in}=\infty$, $R_{out}=0$

Current amp: O/L current gain, $R_{in}=0$, $R_{out}=\infty$

Transimpedance amp: O/L transimpedance gain, $R_{in}=R_{out}=0$

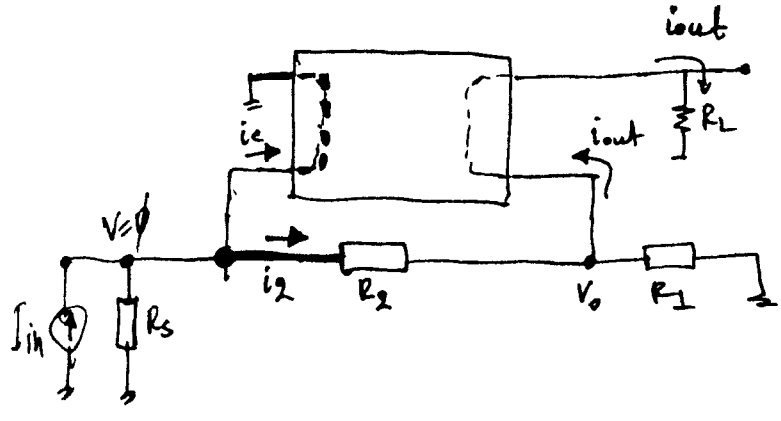
Transconductance amp: O/L transconductance gain, $R_{in}=R_{out}=0$

[1]

ii) Current amplifier should be chosen because its input & output impedance levels ensure that the resulting closed-loop TF is independent of R_S & R_L

[2]

iii)



$$i_{in} = i_e + i_2 = \frac{i_{out}}{A} - \frac{V_o}{R_2}$$

$$i_{out} + \frac{V_o}{R_1} = -\frac{V_o}{R_2} \Rightarrow i_{out} = -V_o\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

$$\rightarrow \quad I_{in} = \frac{i_{out}}{A} + \frac{i_{out}}{R_2(1/R_1 + 1/R_2)} = \left[\frac{1}{A} + \frac{1}{1 + R_2/R_1}\right] i_{out} \Rightarrow$$

$$\Rightarrow \quad \frac{i_{out}}{i_{in}} = \frac{1}{\frac{1}{A} + \frac{1}{1+R_2/R_1}} = \frac{(1+R_2/R_1)}{1 + \frac{(1+R_2/R_1)}{A}} \Rightarrow$$

$$\left.\begin{aligned} \frac{i_{out}}{i_{in}} &= (1+R_2/R_1)\,\frac{A}{A + (1+R_2/R_1)} \\ \text{for} \quad A &= \frac{A_0}{1+s/\omega_0} \simeq \frac{A_0\omega_0}{s} = \frac{GB}{s} \end{aligned}\right\} \Rightarrow$$

$$\Rightarrow \quad \frac{i_{out}}{i_{in}} = (1+R_2/R_1)\,\frac{GB/s}{\frac{GB}{s} + (1+R_2/R_1)} = \frac{(1+R_2/R_1)}{1 + \frac{(1+R_2/R_1)}{[GB]} \cdot s} \qquad [3]$$

iv) Advantage : C/L bandwidth independent of R_s & R_L

Disadvantage : C/L bandwidth × gain =

$$\frac{GB}{(1+R_2/R_1)} \times (1+R_2/R_1) = \text{constant} =$$

= gain-bandwidth product (C/L gain inversely proportional to gain $1+R_2/R_1$) [2]

d) When $I_{in}=\phi$ $\Rightarrow I_{C3}=I_{C4}$ & due to the TLP $\Rightarrow$

(Bookwork)

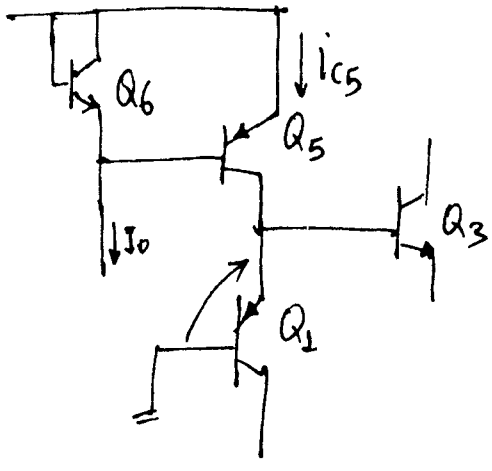
$I_o = I_{C3} I_{C4} \Rightarrow I_{C3}=I_{C4}=I_o \Rightarrow$

$$V_{,offset} = V_T \ln\left[\frac{I_o}{I_{S,P}}\right] - V_T \ln\left[\frac{I_o}{I_{S,n}}\right] \Rightarrow$$

$$V_{,offset} = V_T \ln\left[\frac{I_{Sn}}{I_{Sp}}\right]$$

$$r_x = r_{e2} // r_{e3} \simeq \frac{1}{2}\frac{V_T}{I_o}$$

i) using scaled current sources



$$V_{be6} = V_T \ln\left[\frac{I_o}{I_{Sn}}\right]$$

$$i_{C5} = I_{Sp} \exp\left[\frac{V_T \ln I_o/I_{Sn}}{V_T}\right] \Rightarrow$$

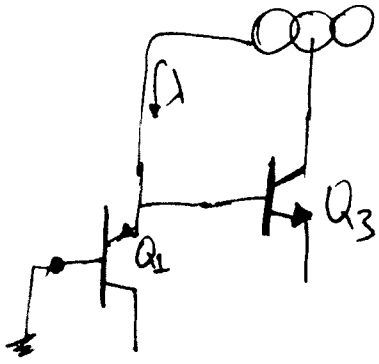
$$i_{C5} = I_o \frac{I_{Sp}}{I_{Sn}} \simeq i_{C1} \Rightarrow$$

$$\Rightarrow V_{be1} = V_T \ln\left[\frac{I_o I_{Sp}/I_{Sn}}{I_{Sp}}\right] = V_T \ln\left[\frac{I_o}{I_{Sn}}\right] \Rightarrow$$

$\Rightarrow$ Q_2 "looks" like an n device despite being a p! $\Rightarrow$

$\Rightarrow$ it matches $Q_3 \Rightarrow$ (offset $\to 0$) [5]

(2) Local current feedback.



$$r_x = \frac{V_x}{i_x} = \frac{V_{be1} - V_{be3}}{i_x} \Rightarrow$$

$$r_x = \frac{V_T \ln\left[\frac{\lambda i_{c3}}{I_{sp}} \frac{I_{sn}}{i_{c3}}\right]}{i_x} = \frac{V_T \ln\left[\lambda \frac{I_{sn}}{I_{sp}}\right]}{i_x} \to 0$$