EE4-20
EE9-AC3

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2013

MSc and EEE/EIE PART IV: MEng and ACGI

Corrected Copy

FULL CUSTOM INTEGRATED CIRCUIT DESIGN

Friday, 10 May 10:00 am

Time allowed: 2:00 hours

There are FOUR questions on this paper.

Answer THREE questions.

All questions carry equal marks.

This is an OPEN BOOK examination.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : T. Constandinou
Second Marker(s) : C. Mehring

Information for Invigilators:

Students may bring any written or printed aids to the examination.

Information for Candidates:

1. Students may need a ruler and coloured pens (red, green, blue and black).

2. Use the following expressions where appropriate:

MOSFET drain current: $$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{Th})^2$$

Standard deviation of threshold voltage mismatch: $$\sigma(\Delta V_{Th}) = \frac{AV_{Th}}{\sqrt{WL}}$$

3. For the expressions above, use the following parameters for 0.18μm CMOS Technology:

$\mu_n C_{ox} = 200\mu A/V^2$
$\mu_p C_{ox} = 80\mu A/V^2$
$V_{Th(NMOS)} = 0.4V$
$V_{Th(PMOS)} = -0.5V.$
$AV_{Th(NMOS)} = 4.0mV\mu m$
$AV_{Th(PMOS)} = 4.5mV\mu m$

1. A full-custom layout design is shown below in Figure 1.1 for an integrated circuit implemented in a commercially available 0.18μm 1P6M CMOS technology (only 2 metal layers used in design).

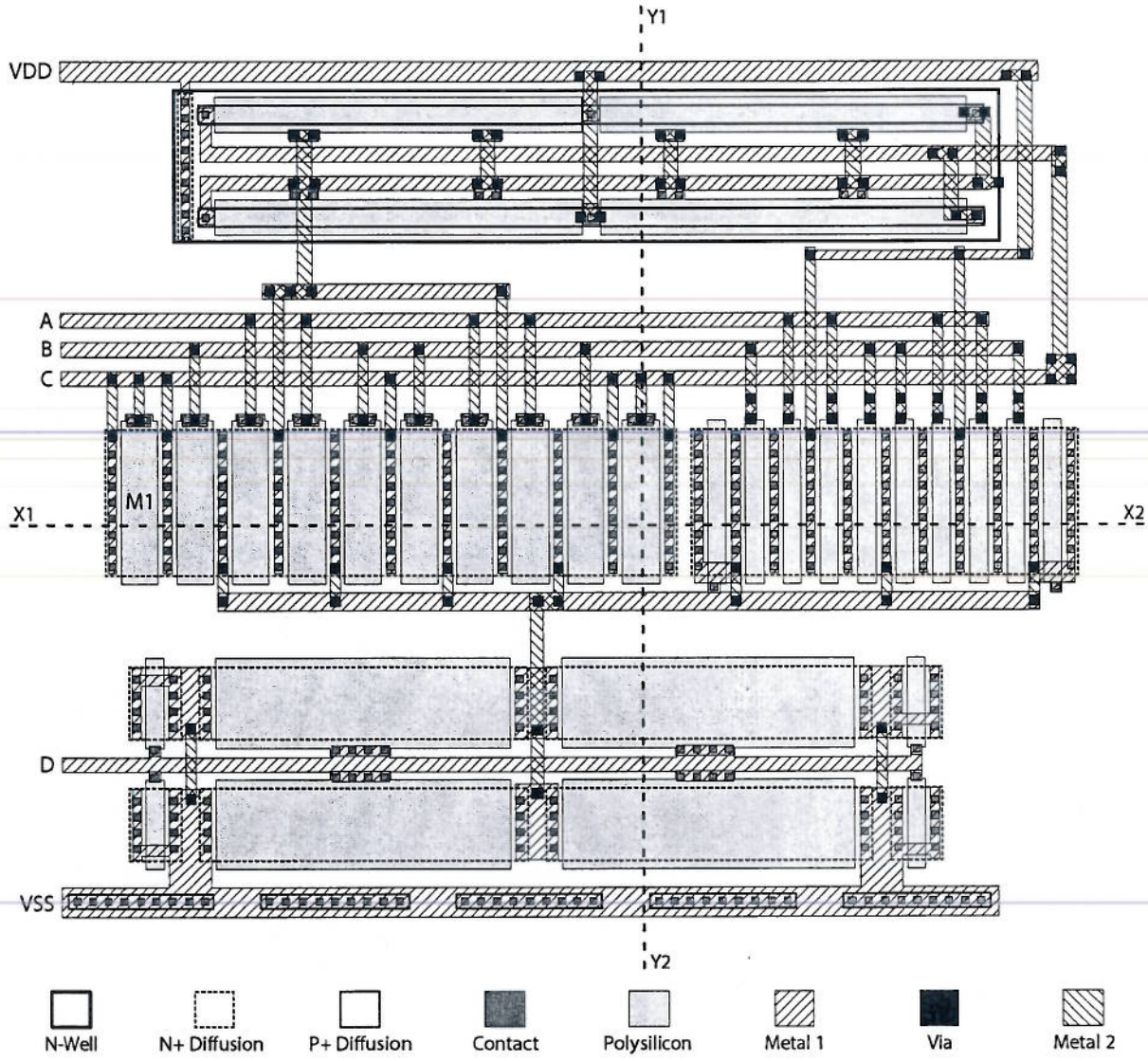


Figure 1.1

a) Extract and draw the transistor-level circuit schematic for this design showing the nodes VDD, VSS, A, B, C, D.

Given that the transistor labelled M1 is of size W/L = (4μm/1μm), label all transistors in this circuit with their sizes. Hint: Several of the devices are constructed use a multi-fingered layout (i.e. using multiple identical devices connected in parallel).

[10 marks]

b) Draw the vertical cross-sections along the lines X1-X2 and Y1-Y2. Label your diagrams indicating the n-well region and the different structures (eg. Metal1, Metal2), types and levels of doping (eg. P+, N+, etc).

[8 marks]

c) What function does this circuit perform?

[2 marks]

2. The cross-section of commercially available 0.35μm 2P3M CMOS technology is shown below in Figure 2.1.

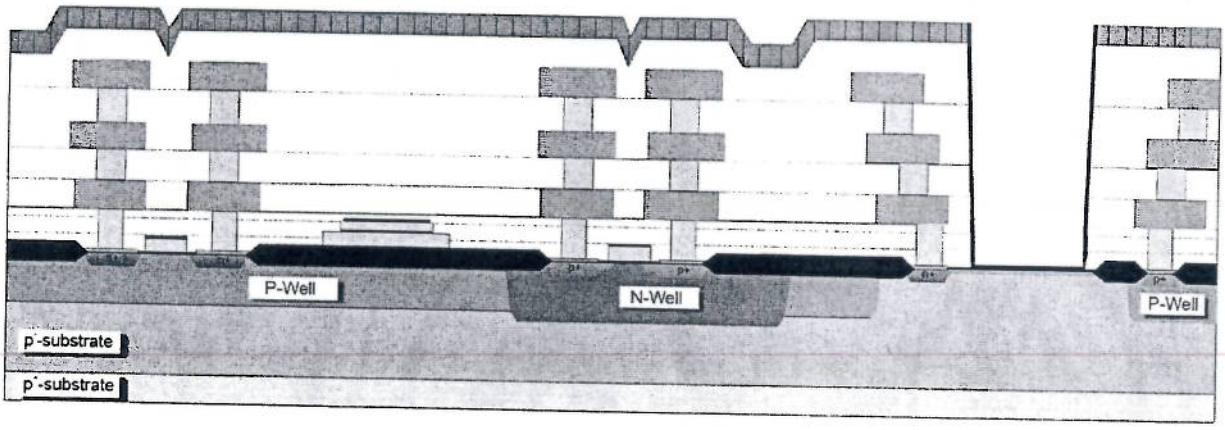


Figure 2.1

a) List 8 different devices (i.e. either passive or active integrated components) that can be fabricated in this technology. For each device, sketch its cross-section (i.e. structure) and comment on any limitations.

[12 marks]

b) Given that in this technology a 3T APS Pixel would occupy a 5μm x 5μm footprint, a 25mm^2 die size is required per megapixel (excluding column amplifiers, data converter and any other circuits outside the imaging array). How would this imager architecture scale to a 32nm CMOS technology? What (if any) are the limitations in scaling image sensors?

[4 marks]

c) Using the fact that the penetration depth of light in Silicon reduces with wavelength (by the Beer Lambert law), describe how a standard CMOS technology can be exploited to provide spectrally selective photodiodes (without colour filters).

[4 marks]

3. The design of a N-bit binary-weighted current-steering Digital-to-Analogue (DAC) converter is shown below in Figure 3.1. is to be implemented in a standard 0.18μm CMOS technology.

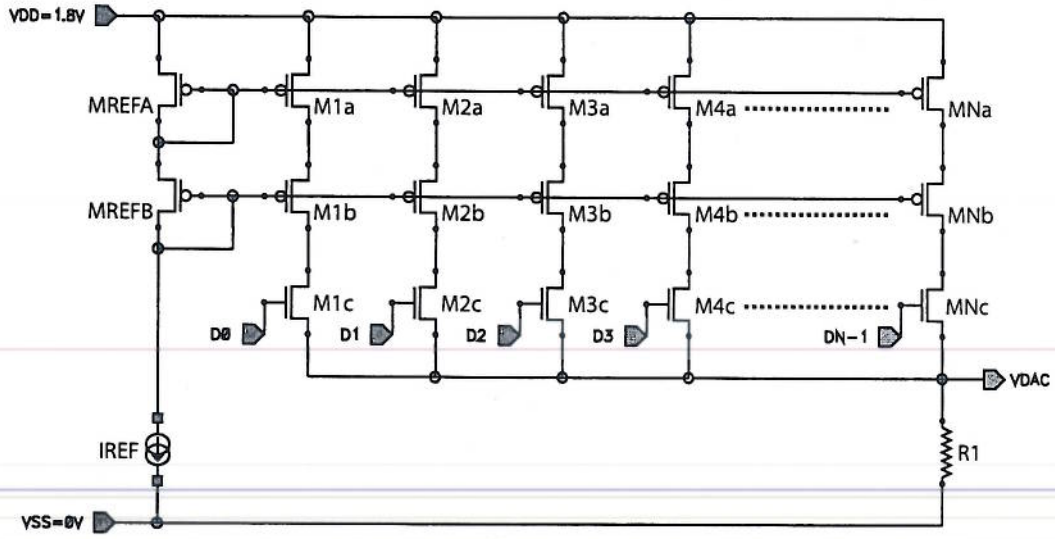


Figure 3.1

For this question, use the expressions provided in page 1 where appropriate.

a) Given that N=8, I_{REF}=2μA and R1=10KΩ calculate the ratio between device aspect ratios (i.e. W/L's) for MREFa:M1a:...M8a given that a 1V output range is required.

[4 marks]

b) Sketch how you would arrange the critically matched devices (i.e. current mirrors) in a layout design to improve the matching. Show only the devices corresponding to the 4 LSB's (i.e. D0, D1, D2 and D3).

Note that a detailed layout is not required – you are only required to sketch the arrangement (i.e. order/orientation and placement of the devices).

[4 marks]

c) Compare this DAC topology to that of an R-2R ladder. State (and explain) two advantages of each topology compared to the other.

[4 marks]

d) Given that $(W/L)M_{REFA}=(W/L)M_{REFB}$=25μm/25μm, and assuming that all devices are in strong inversion (and saturation), determine the worst case for the *Effective Number Of Bits (ENOB)* of the converter.

[8 marks]

4. The design of a clock generation circuit (i.e. oscillator) is shown below in Figure 4.1. This uses a Schmitt trigger to alternate between charging and discharging a capacitor using a constant current source/sink. The current generator is based on a beta-multiplier reference.

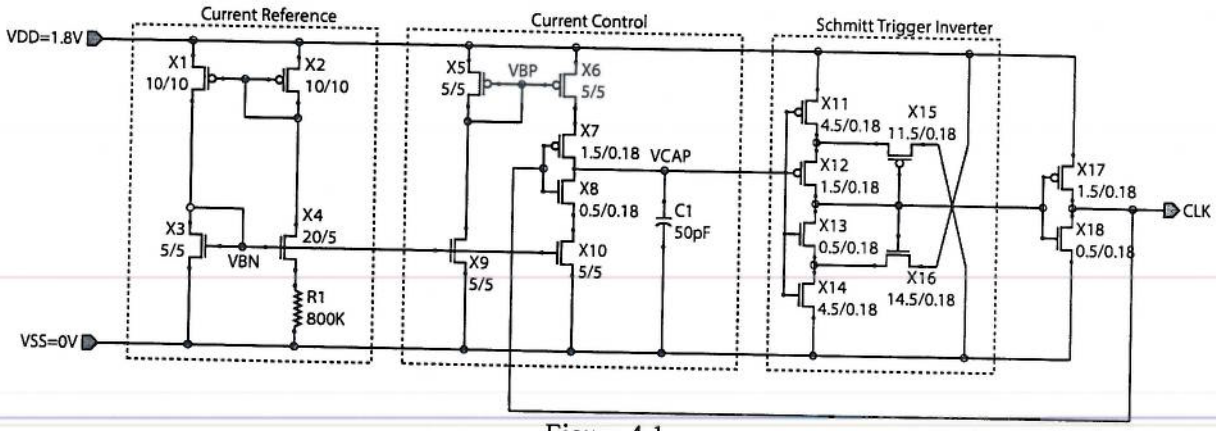


Figure 4.1

For this question, use the expressions provided in page 1 where appropriate.

a) Assuming devices X1-X4 are all in saturation and operating in strong inversion, derive an expression for I_{REF} in terms of component parameters, for example: R, $(W/L)_1$, etc. and show that this is independent of power supply.

[5 marks]

b) Using your answer to (a), evaluate the bias current (I_{REF}).

[2 marks]

c) Determine the switching points (V_{SLH} and V_{SHL}) of the Schmitt trigger inverter.

[5 marks]

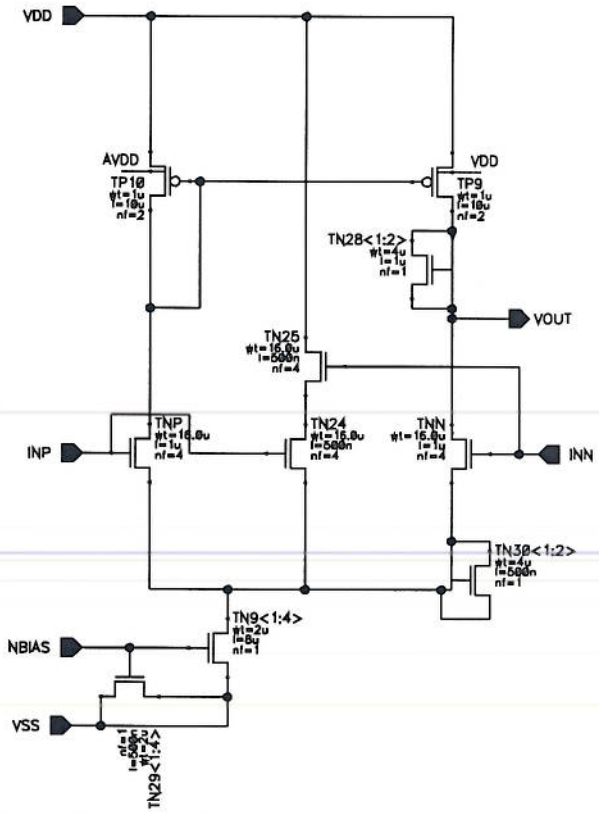
d) Determine the oscillation frequency.

[2 marks]

e) Given that this will be implemented in a 0.18μm CMOS technology with MIM capacitors and a high resistance poly module, estimate the silicon area required to implement this circuit. Use the following technology parameters: C_{MIM}=0.7fF/μm^2, R_{POLYH}=1KΩ/□.

[4 marks]

1. (a)

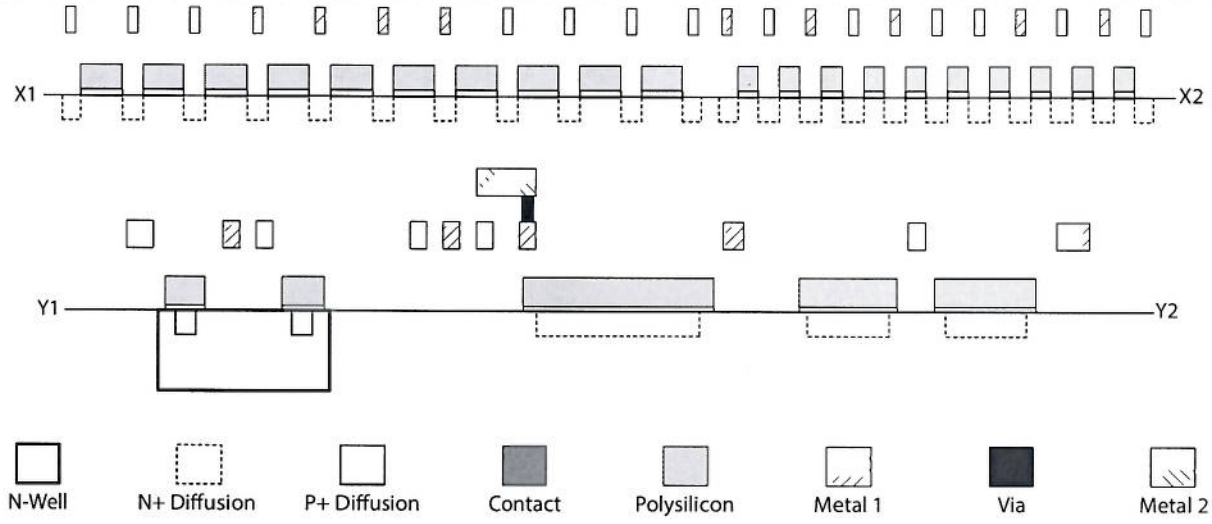


A=INP, B=INN, C=VOUT, D=NBIAS and device M1=TN28<1>

(4 marks for identifying device W/L's correctly, 1 mark for identifying dummy devices, 4 marks for correct netlist, 1 mark for correct pin identification)

[10 marks]

(b)



[8 marks]

(c) This circuit is a single stage OTA (operational transconductance amplifier) with bump linearlisation (devices TN24 and TN25). By "stealing" current from the differential pair the middle branch the (linear) input voltage range is increased.

(1 mark for identifying OTA topology, 1 mark for bump linearization)

[2 marks]

2. (a)

Any 6 of the following with corresponding cross-sections (standard):

- MOSFET (NMOS and PMOS) – native devices so good performance.
- Lateral PNP bipolar transistor (p-substrate/n-well/p+) – limitation is gain (beta). Use is limited to bandgap reference and diode.
- Poly1-poly2 capacitor – typically 0.5-1fF/sq. um
- Parasitic p-n junction diodes (n-well/p-sub, p+/n-well, n+/p-sub) – can be used as photodiodes.
- Poly resistor – high value resistors hard to realize (even if technology supports a high resistance poly).
- Lateral (flux) interconnect capacitors. Generally capacitance is less than poly1-poly2.
- Photodiode (n+/p-epi/p-substrate).
- ISFET – leaving floating gate connected up to M3 and using passivation surface as sensing membrane.

(For each: ½ mark for identifying topology + ½ for description + ½ for limitations + ½ for cross-section)

[12 marks]

(b)

- Generally pixel size has scaled with Moore's law if you look at Mpixels/mm^2 over the past decade or so.

[1 mark]

- Components within 3T pixels are typically photodiode (or photogate) and 3x Transistors. Transistors scale linearly with technology, and therefore so do dimensions of structures used to design photodiode (or photogate). However, dark current gets worse (with scaling) so good performance imagers are harder to make in smaller technologies.

[1.5 marks]

- Imaging plane (i.e. pixel array) would scale from 350nm to 32nm with Moores law (i.e. in a 32nm technology pixel size could be expected to be <1um x 1um. However- auxillary circuits are the fundamental bottleneck to scaling. For example a 200Mpixel imager (at 5 frames per second) and 10 bit resolution data converter corresponds to a datarate of 10Gbps! So as the imaging array scales the requirements on the FSM, column amplifiers, array amplifier, data converter, etc increase.

[1.5 marks]

(c)

Using fact that shorter wavelength light is absorbed at shallower depths means that longer wavelength light penetrates deeper into the silicon (before being absorbed). If the designer can exploit the depth of different type of junctions (for example, wells are typically at 1-2 micron depth, whereas diffusion is shallow – 100-200nm) such as to separate an electron-hole pair and create a photocurrent, then different depth junctions can be used to detect different wavelengths of light. Specifically- diffusion should be sensitive to all wavelengths, whereas shallow wells only to red+green and deep wells only red. Foveon (X3 imagers) actually exploit this phenomenon to achieve vertically stacked pixels (i.e. detect R + G + B within every pixel) as oppose to using colour filters in a Bayer pattern and then interpolating the "missing pixels".

(2 marks for general understanding and identifying that different structures sensitive to different wavelengths, 1 mark for specific examples (and giving numbers), 1 mark for example with Foveon, etc)

[4 marks]

3. (a)

- If a 1V output is required given 10K resistance this corresponds to a 100uA current (full scale).
- Therefore if I(LSB) x (2^N-1) = 100uA then I(LSB)=0.4uA.
- Given IREF is 2uA then the ratio (MREFA:M1A:M2A:M3A:...M8A and MREFB:M1B:M2B:M3B:...M8B) should be: 5:1:2:4:8:16:32:64:128

(2 marks for method + 2 marks for answer)

[4 marks]

(b) Design question so no unique answer. Looking for the following:

- For first 4 LSBs need ratio 5:1:2:4:8 giving a total of 21 LSB devices. Could arrange in a 3x7 array or alternatively 5x9 array (with dummy devices around). Large devices should be made from identical unit devices.
- Use of either common centroid or interdigitation (1D or 2D)
- Currents should flow in same direction (and devices orientated similarly).

(2 marks for demonstrating good layout practice + 2 marks for correct answer)

[4 marks]

(c)

Advantages of current-steering over R-2R

- Current output (if application requires a current) is MOSFET only.
- In general (for same area) MOSFETs match better than Rs or Cs.
- Using currents, can be much lower power than resistors (since large resistors cannot be integrated).

Advantages of R-2R over current steering.

- Not binary weighted- therefore less total unit components (3R x (N+1)) vs. 2^N-1.
- Easier to match since all passives are either R or 2R.
- Voltage output does not depend on absolute resistance value (as in case of current-steering).

(4 marks for 4/6 items from above)

[4 marks]

(d)

$V_{GS}=V_{TH}+\sqrt{(2I_D/\mu C_{ox}W/L)}$

1. If $(W/L)M_{REF}$ = 25/25, $V_{GS}=0.5+\sqrt{(2*2\mu A/80\mu)}$ = 0.7236V.
2. Since ratio of M_{REF}: M_{LSB}=5:1 then $(W/L)_{LSB}$ = 5/25.
3. $\sigma(\Delta V_{TH})=AV_{TH}/\sqrt{(WL)}$ = 4.5mV/$\sqrt{(20)}$ = 0.4mV => $3\sigma(\Delta V_{TH})$=1.21mV (worst case).
4. $\Delta I_D(LSB, max)=|I_{DLSB}(V_{GS}-V_{TH})-I_{DLSB}(V_{GS}-V_{TH}-\Delta V_{TH})|=|0.4\mu A-0.389\mu A|$ =4.31nA.
5. For mismatch not to effect DAC, 2^{N}-1 x $\Delta I_D(LSB, max)<0.5*I_{LSB}$
6. 2^{N}-1 x $\Delta I_D(LSB, max)$ = 1.1μA > $0.5*I_{LSB}$!!!
7. ENOB= $\log2(0.5xI_{LSB}/\Delta I_D(LSB, max))$ = log2(200nA/4.31nA)=4.54bits

(4 marks for method, 1 mark for 3sigma worst case, 3 marks for ENOB)

[8 marks]

4. (a)

$$V_{GS1} = V_{GS2} + I_{out}R_S$$

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}} + V_{TH1} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox} K(W/L)_N}} + V_{TH2} + I_{out}R_S$$

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}}\left(1 - \frac{1}{\sqrt{K}}\right) = I_{out}R_S$$

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N}\frac{1}{R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

(3 marks for Iout derivation, 2 marks for expression, 1 mark for it being independent of VDD)

[6 marks]

(b)

Iout=$(1/800K)^2$*$(1-0.5)^2$*2/(200u)=3.9nA.

(1 mark for correctly identifying K and 1 mark for result)

[2 marks]

(c)

$\beta_{14}/\beta_{16}=(W_{14}L_{16}/L_{14}W_{16})=[(V_{DD}-V_{SPH})/(V_{SPH}-V_{THN})]^2=4.5/14.5=0.31 \Rightarrow \sqrt{(\beta_{14}/\beta_{16})}=0.56$
$\beta_{11}/\beta_{15}=(W_{11}L_{15}/L_{11}W_{15})=[(V_{SPL})/(V_{DD}-V_{SPL}-V_{THP})]^2=\beta_{11}/\beta_{15}=4.5/11.5=0.39 \Rightarrow \sqrt{(\beta_{11}/\beta_{15})}=0.62$

0.56=(1.8-VSPH)/(VSPH-0.4) =>VSPH=1.3V
0.62=(VSPL/(1.8-VSPL-0.5) => VSPL=0.5V

(2 marks for each correct expression + 1 mark for evaluating each)

[6 marks]

(d)

t1=C(VSPH-VSPL)/I=50p(0.8)/3.9n=10.26ms
t2=C(VSPH-VSPL)/I=50p(0.8)/3.9n=10.26ms

fclk=1/(t1+t2)=48.75Hz

(1 mark for correct expression + 1 mark for evaluating)

[2 marks]

(e)

Area=Area(MOSFET) + Area(Cap) + Area (Resistor) + Routing

1. Area(MOSFET)=7*10*10+5*5+3*0.18*2+2*4.5*0.18+11.5*0.18+14.5*0.18=732.4um2. Add 200% overhead for contacts+spacing = 2200um2
2. Area(Cap)=50pF/0.7fF=71428um2
3. Assuming Resistor = (L/W)=800/1 with W=1um. Area(Resistor) = 800um2
4. Add extra 50% for routing. Total area = (2200+71428+800) * 1.5 = 111642um2 = 0.11mm2

(1 mark for cap, 1 mark for resistor, 1 mark for MOSFETs+assumptions, 1 mark for final result)

[4 marks]