IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2014

EEE/EIE PART I: MEng, BEng and ACGI

Corrected Copy

DIGITAL ELECTRONICS 1

Monday, 2 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 each carry 30%.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : Z. Durrani
Second Marker(s) : J.V. Pitt

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Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X[7:0] is an eight bit bus with X7 being the MSB and X0 the LSB.

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

Question 1

1. a) Simplify the following Boolean expressions using Boolean algebra and/or De Morgan's theorem.

i) $\overline{\left(A+\overline{B}\right)\left(\overline{A\overline{C}\overline{D}}\right)}$

[3]

ii) $\left(\overline{\overline{A}\oplus\overline{BC}}\right)\left(\overline{A+B+\overline{C}}\right)$

[3]

b) Simplify the following Boolean equation, in sum-of-products form, using a Karnaugh map. Here, A is the MSB and D the LSB.

$$f\left(A,B,C,D\right)=\Sigma\left(0,2,4,5,6,7,8,10,15\right)$$

[4]

c) Simplify the following Boolean equation, in product-of-sums form, using a Karnaugh map.

$$f=A\overline{B}\overline{C}+B\overline{C}\overline{D}+\overline{A}\overline{B}C+\overline{B}C\overline{D}+\overline{A}\overline{B}\overline{C}D$$

[4]

d) Assuming that all numbers are 8 bits wide, complete the missing entries, which are not shaded, in the following table. (No marks will be awarded for this question unless you show how the solution is derived.)

[8]

Hexadecimal	Octal	Signed binary	Signed decimal
?		?	-105
?	275		?

e) For the circuit shown in Fig. 1.1, complete the timing waveforms for signals X, Y and Z for 6 clock cycles. You may assume that initially, the values of X, Y and Z are zero.

[6]

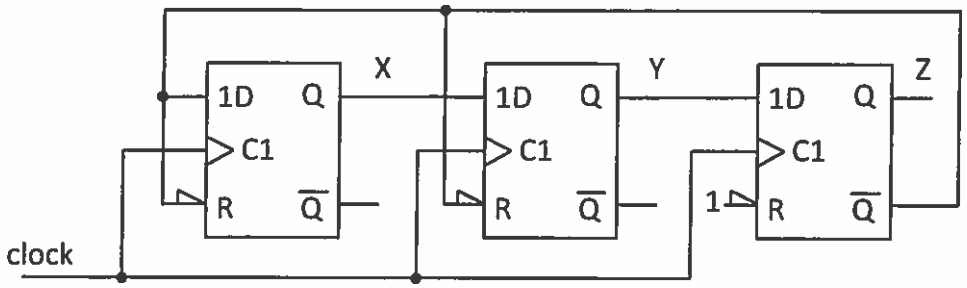


Figure 1.1

f) A full-adder is shown in Fig. 1.2. For inputs A, B and C_{in}, and outputs Σ and C_{out}:

(i) Draw the truth table for the circuit.

[3]

(ii) Hence, derive Boolean expressions for Σ and C_{out}.

[3]

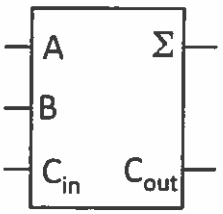


Figure 1.2

g) A 64 × 4 read-only memory (ROM) (Fig. 1.3(a)) is to be used to simultaneously implement the Boolean functions:

$$f = \overline{X}\overline{Y}Z + \overline{X}Y\overline{Z} + X\overline{Y}\overline{Z} + XYZ$$

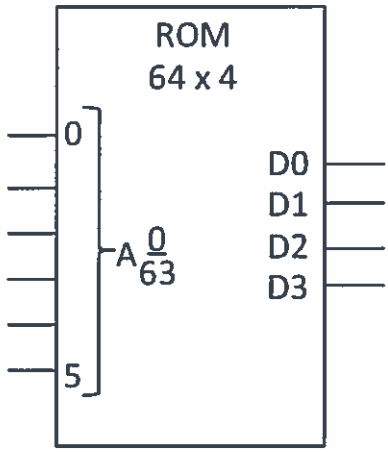
$$g = XZ + \overline{Y}Z + X\overline{Y}$$

(i) Complete the missing entries in the part of the ROM data table shown in Fig. 1.3(b).

[4]

(ii) Show how you would connect input and output variables to the terminals of the ROM.

[2]



(a)

A[5:0]	D[3:0]
00	0
01	C
02	8
03	0
04	?
05	?
06	?
07	?

(b)

Figure 1.3

Question 2

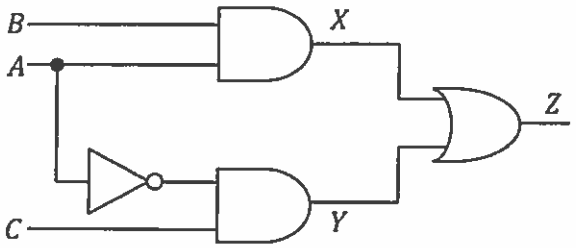
2. a) In the circuit shown in Fig. 2.1(a), the propagation delay in each gate is 0.1 μs.

i) For this circuit, given the timing diagram for the input signals *A*, *B* and *C* shown in Fig. 2.1(b), sketch the timing diagram for signals *X*, *Y* and *Z*. Your diagram should include any glitches.

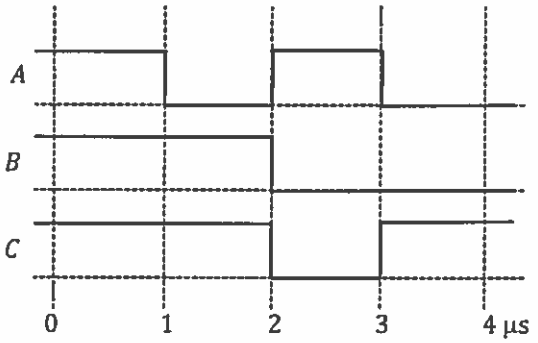
[6]

ii) Show how the circuit of Fig. 2.1(a) can be redesigned to prevent static '1' hazards from occurring.

[4]



(a)



(b)

Figure 2.1

b) Figure 2.2 shows an SR flip-flop:

i) Sketch the state diagram for this flip-flop.

[4]

ii) Hence, derive characteristic Boolean equations for next states Q^+ and $\overline{Q^+}$.

[4]

iii) Show that by using these equations, the flip-flop can be implemented using only two NOR gates.

[4]

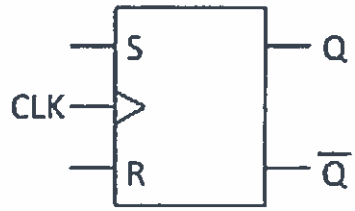


Figure 2.2

c) Figure 2.3 shows a finite state machine (FSM), defined by the states A, B and C. The machine is initially in the state ABC = 000.

i) Write down Boolean equations for variables X and Y.

[4]

ii) Hence, draw the Moore state diagram for this FSM.

[4]

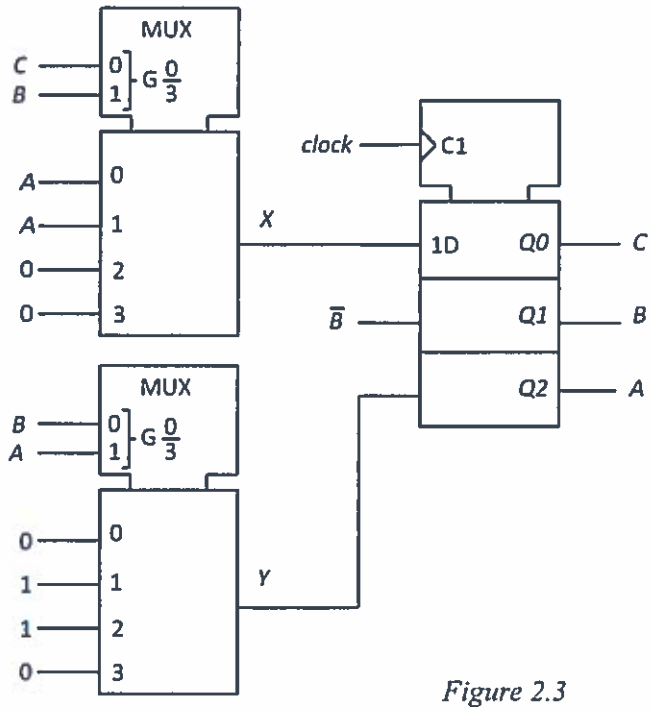


Figure 2.3

3. Figure 3.1 shows a sequence detector using a finite state machine (FSM), with input signal X and output signal Y. The FSM is required to detect the serial bit sequence 1001.

   a) Draw a Mealy state diagram for the FSM.

   [8]

   b) Draw the state transition table for the FSM.

   [8]

   c) The FSM is to be implemented using J-K flip-flops and a combinational logic circuit. Derive the Boolean expressions necessary for this implementation.

   [10]

   d) Sketch the circuit diagram for your design. This should show the J-K flip-flops, the gate-level circuit diagram for the combinational logic circuit, and any interconnections.

   [4]

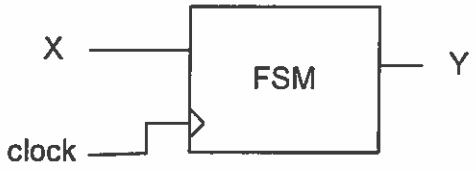


Figure 3.1

[THE END]