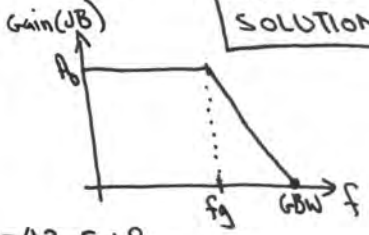
SAMPLE 2 WORKED SOLUTIONS

(1) (a) The gain-bandwidth product (GBW) is defined as $GBW = A_0 \times f_g$

where: A_0 is the open-loop gain

f_g is the -3dB frequency (bandwidth).



The GBW product remains constant in closed-loop.

if GBW = 15MHz → Gain (@ 100kHz) = $\frac{15000}{100} = 150 \rightarrow = 43.5dB$

(b) (i) $R_{out} = [R_D + r_{o3} \| r_{o2} \| 1/g_{m2}] \| r_{o1}$

(ii) $R_{out} = R_c \| [g_{m1} r_{o1} (\frac{1}{g_{m2}} \| r_{o2} \| r_{\pi 1} \| r_{\pi 2}) + r_{o1} + (\frac{1}{g_{m2}} \| r_{o2} \| r_{\pi 1} \| r_{\pi 2})]$

Assuming $1/g_m \ll r_o$ ~~and g~~

→ (i) $R_{out} = (R_D + \frac{1}{g_{m2}}) \| r_{o1}$

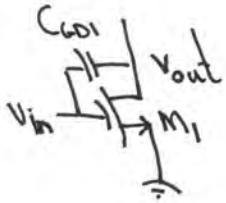
(ii) $R_{out} = R_c \| [g_{m1} r_{o1} (\frac{1}{g_{m2}} \| r_{\pi 1} \| r_{\pi 2}) + r_{o1} + (\frac{1}{g_{m2}} \| r_{\pi 1} \| r_{\pi 2})$

(c) (i) $\frac{V_{out}}{V_{in}} = g_{m1} R_{out} = g_{m1} [(R_D + \frac{1}{g_{m2}}) \| r_{o1}]$

(ii) $\frac{V_{out}}{V_{in}} = \frac{-R_c \| R_{out}}{r_{o1} \| \frac{1}{g_{m1}} + \frac{1}{g_{m2}} \| r_{o2}} \quad \frac{-R_c}{\frac{1}{g_m} + R_E}$ (emitter degen. gain)

$\rightarrow \frac{V_{out}}{V_{in}} = -\frac{R_c}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$ (if $r_o = \infty$)

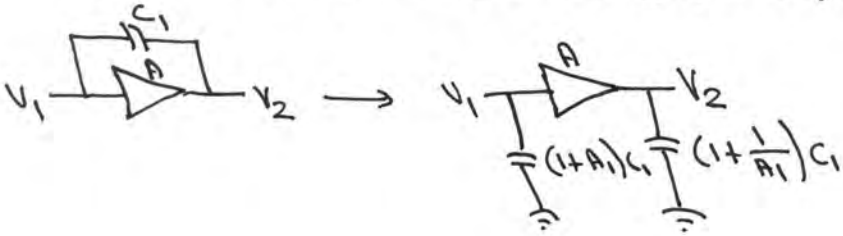
(d)



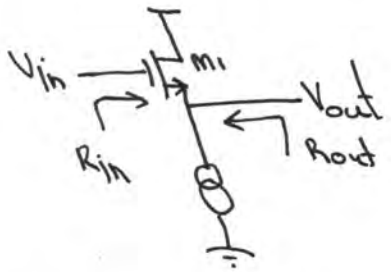
In C.S. amplifier stage, C_{GD} appears between input and output (i.e it is a floating capacitor) and therefore cannot be analysed easily.

Millers theorem can be used to split this into two grounded capacitor such than input and output nodes can be analysed seperately.

In general, Millers theorem states (for capacitors)



(e) The most appropriate amplifier stage to use as a voltage buffer is the source follower (or emitter follower for BJT). This has a high input impedance and low output impedance which is ideal when used as a voltage buffer.



$R_{in} = \infty$

$R_{out} = 1/g_{m1} \,||\, r_{o1} \simeq 1/g_{m1}$

(f) The "body effect" represents the dependance of the MOSFET threshold voltage (V_{TH}) on the source-body (or source-bulk) bias, i.e V_{SB}.

The expression for this is: $V_{TH} = V_{T\phi} + \gamma\left(\sqrt{V_{SB} - 2\phi} - \sqrt{2\phi}\right)$

where: $V_{T\phi}$ is the zero V_{SB} value of threshold voltage
γ is the body effect parameter
2ϕ is the surface potential parameter.

In amplifier design, the body effect can be eliminated by ensuring $V_{SB} = 0$. for transistors with source terminals not connected to power supply rails (i.e. V_{DD} for Pmos and V_{SS} for Nmos), Pmos devices are preferable. This is because they are fabricated within an "isolated" n-well and therefore is a true 4-terminal device (Nmos devices have a shared body contact — the substrate).

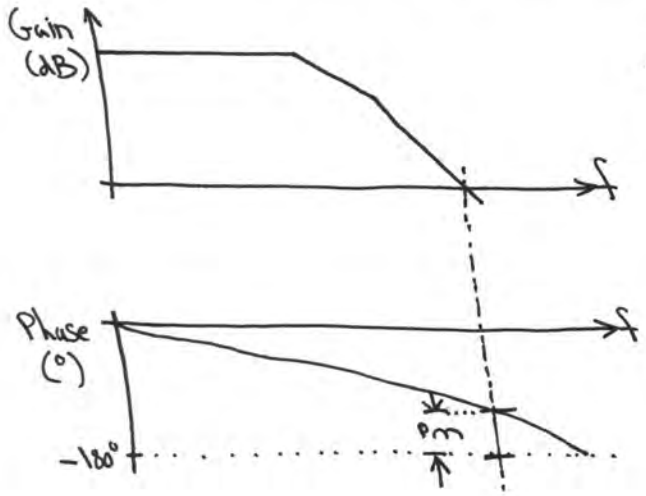
(g) 2 challenges:

(1) passive components have limited range of values on-chip, particularly large values, eg resistors < 1MΩ, capacitors < 1nF, etc.

(2) Prototyping — ICs take several months (at the very least) to complete and fabricate a design whereas discretes (eg PCBs) can be developed in days/weeks. Also with ICs there is no flexibility for modification once fabricated.

(3) Process variation — In ICs component values (absolute) may vary up to 20% — eg. resistors. Discrete components however can be obtained to good tolerances → eg. 0.1% for Resistors. or 1%

(h) The phase margin provides a measure of how much margin a design has to the point of instability.



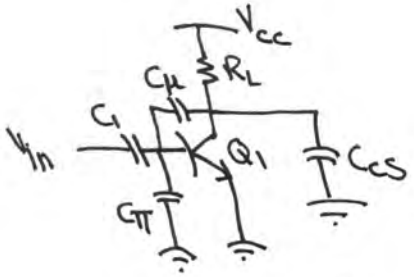
This is defined as the difference between the phase response (when the gain) is unity and 180°.

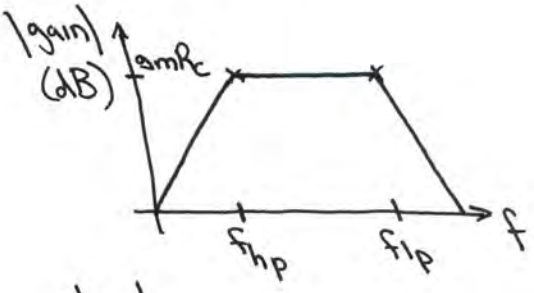
This is important in analogue design as this provides a method for ensuring ~~stress~~ robust circuit design. As design parameters may vary (eg. due to process variation, temperature, etc) it is crucial to design a sufficient phase margin.

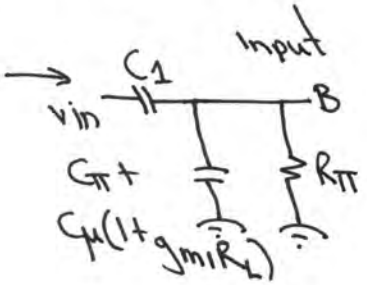
(i) Common-Mode Rejection (CMR) is the ability of an amplifier to suppress/attenuate (reject) the common mode. This can be quantified by CMRR (common-mode rejection ratio which is defined as: $CMRR = \frac{A_{v(d.m)}}{A_{v(c.m)}}$ i.e differential gain over common-mode gain.

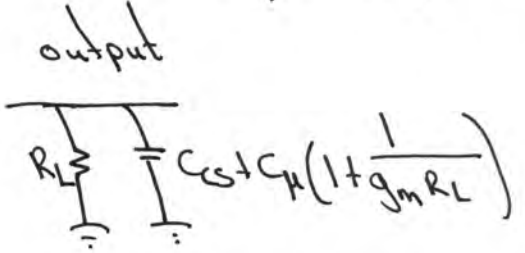
It is essential ~~that~~ in analogue design to achieve good CMR (i.e a high CMRR) so that any noise in the power supply, for example, cannot couple through to the signal path.

(j)









where ~~f_{hp}~~ $\frac{R_\pi + \frac{1}{j\omega(C_\pi + C_\mu(1+g_{m1}R_L))}}{R_\pi + \frac{1}{j\omega[C_\pi + C_\mu(1+g_{m1}R_L)]} + \frac{1}{j\omega C_1}} = \frac{V_B}{V_{in}}$

f_{hp} is defined by:

and $f_{lp} = \frac{2\pi}{R_L \cdot \left(C_{cs} + C_\mu\left(1+\frac{1}{g_m R_L}\right)\right)}$

(2) (a) $V_x = 0.9V$, $I_9 = 1mA$ and $\left(\frac{W}{L}\right)_{5-12}$ are identical. $P = 2.25mW$.

$P = 2.25mW = V_{DD} \times I_{total}$. $I_{total} = I_9 + I_{10} \Rightarrow I_{10} = 0.25mA$

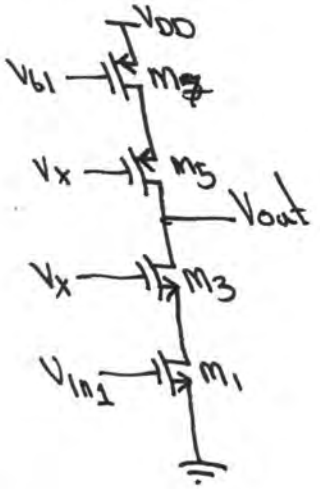
$V_{GS10} = 0.9 - 1k\Omega(0.25mA) = 0.65V$

$\left(\frac{W}{L}\right)_{10} = \frac{2I_D}{\mu_n C_{ox}(V_{GS}-V_{TH})^2} = \frac{2(0.00025)}{200\mu(0.25)^2} = 40$

→ for $\left(\frac{W}{L}\right)_{PMOS} \Rightarrow 0.9 = 2V_{GSP}$

$\therefore \left(\frac{W}{L}\right)_{PMOS} = \frac{2I_D}{\mu_p C_{ox}(V_{GS}-V_{TH})^2} = \frac{2(0.00025)}{100\mu(0.05)^2} = 2000$

(b) Half circuit

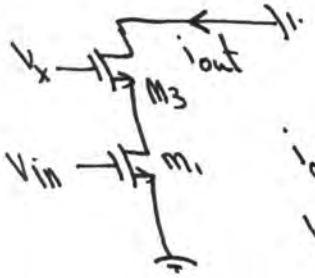


Assuming node P is an ac gnd (for small signals) due to symmetry → also $m_5 = m_6 = m_7 = m_8$, $m_1 = m_2 = m_3 = m_4$

$R_{out} = g_{m3}r_{o3}r_{o1} \| g_{m5}r_{o5}r_{o7}$

(assuming $g_{m3}r_{o3}r_{o1} >> r_{o1}, r_{o3}$ and $g_{m5}r_{o5}r_{o7} >> r_{o5}, r_{o7}$)

(c) $G_m = g_{m1}$



$i_{out} = g_{m1}V_{GS1}$

$i_{out} = g_{m1}V_{in}$

$G_m = \frac{i_{out}}{V_{in}} = g_{m1}$

$A_v = -G_m R_{out}$

$\frac{V_{out}}{V_{in1}-V_{in2}} = g_{m1}\left(g_{m3}r_{o3}r_{o1} \| g_{m5}r_{o5}r_{o7}\right)$

(d) $g_{m1-4} = 10mS$

$I_{D1-4} = 0.5mA$ (assuming $I_7 = I_8$ and $I_7 + I_8 = I_9$)

$$g_{m1-4} = \sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}}$$

$$= \sqrt{1m(200\mu)\frac{W}{L}} \rightarrow \left(\frac{W}{L}\right)_{1-4} = 2000$$

$$g_{m5} = \sqrt{2 I_D \mu_p C_{ox} \frac{W}{L}} \rightarrow 20mS$$

$$r_{out(n)} = \frac{1}{\lambda_n I_D} = \frac{1}{0.1 \times 0.5mA} = 20k\Omega$$

$$r_{out(p)} = \frac{1}{\lambda_p I_D} = \frac{1}{0.2 \times 0.5mA} = 10k\Omega.$$

$$A_V = g_{m1}\left(g_{m5} r_{05} r_{07} \| g_{m3} r_{01} r_{03}\right)$$

$$= 0.02\left(0.02(10K)^2 \| 0.02(20K)^2\right)$$

$$= 32000$$

$$= 90.1dB$$

(e) Need to ensure the following: ① $L > W$

② LW is minimum (area)

③ W is sufficient for the current to be conducted.

∴ Select R_{poly} type: $R_{poly} = 50\Omega/\square$

$$\left(\frac{L}{W}\right)_{1K} = \frac{1K}{50\Omega} = 20$$

$$W = \frac{I_{max}}{J_{poly}} = \frac{0.25}{0.1} = 2.5\mu m$$

$$\therefore L = \left(\frac{L}{W}\right) \times W = 20 \times 2.5\mu m = 50\mu m$$

(f) (m_1 and m_2) differential pair — must match (most important pair)

→ also mirrors: m_9/m_{10}, $m_{12}/m_7/m_8$, $m_{11}/m_5/m_6$ and m_3/m_4

3 techniques to improve matching:

(1) Design devices to have close proximity (small spacing)

(2) Use common centroid layout — to ensure common axis of symmetry

(3) Place dummy devices around the pair/group to be matched to ensure surrounding area to all active devices is identical

(9) (Remember PVT)

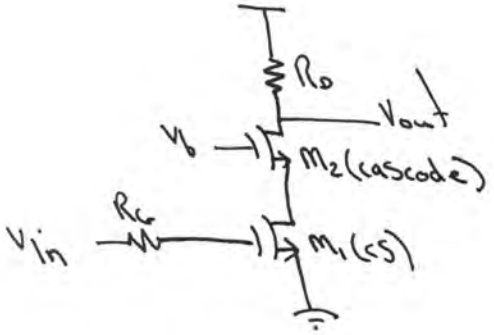
P = Process — V_{GS}/I_D characteristics as well as absolute value of 1K resistor will change with process variation ∴ bias will also change.

V = Voltage (Power Supply) — bias is ultimately derived from PS ∴ any noise/fluctuation/drift will couple through.

T = Temperature — MOSFET characteristics (eg. V_{GS}/I_D relationship) are temp. dependant ∴ change in temp will cause a change in bias temperature.

In general, a designer must aim to engineer the bias circuit such that it is immune to PVT (as much as possible).

(3)



$\omega_{pin} = 2\pi(5G)$

$\omega_{pout} = 2\pi(10G)$

$L_1 = L_2 = 0.18\mu m$

$I_D = 0.5mA$

$V_{GS} - V_{TH} = 200mV$

$\lambda = 0$

$C_{GS} = \frac{2}{3} C_{ox} WL$

$C_{ox} = 12ff/\mu m^2$

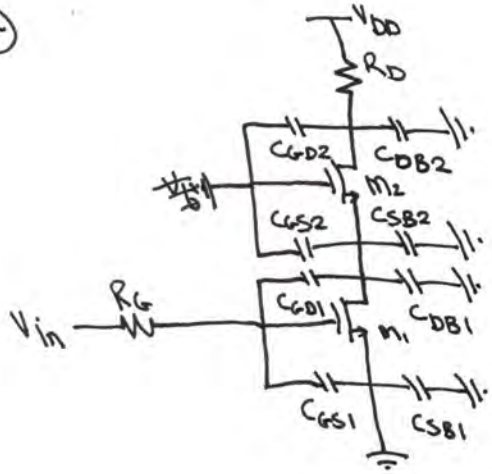
$C_{DB} = C_{SB} \approx 0$

$\mu_n C_{ox} = 200\mu A/V^2$

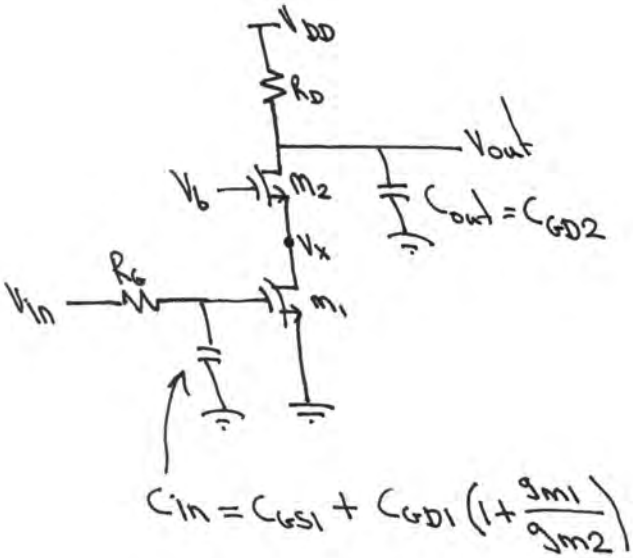
$C_{GD} = C_0 W$

$C_0 = 0.2ff/\mu m$

(a)



(b)



$$C_{in} = C_{GS1} + C_{GD1}\left(1 + \frac{g_{m1}}{g_{m2}}\right)$$

(c) $I_D = \frac{1}{2}\left(\frac{W}{L}\right)_1 \mu_n C_{ox}(V_{GS}-V_{TH})^2$

$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{2I_D}{\mu_n C_{ox}(V_{GS}-V_{TH})^2} = \frac{1m}{200\mu(0.2)^2} = 250$

$\therefore$ If $L_1 = L_2 = 0.18\mu m \rightarrow W_1 = W_2 = 250 \times 0.18 = 45\mu m.$

$g_{m1} = g_{m2} = \frac{W}{L}\mu_n C_{ox}(V_{GS}-V_{TH}) = 250(200\mu)0.2 = 5mS$

(d) $C_{GD1} = C_{GD2} = C_{OW} = 9fF$

$C_{GS1} = C_{GS2} = \frac{2}{3}WLC_{ox} = 64.8fF$

$\omega_{pin} = 2\pi(5G) = \frac{1}{R_G C_{in}} = \frac{1}{R_G\left[C_{GS1} + C_{GD1}\left(1+\frac{g_{m1}}{g_{m2}}\right)\right]}$

$\Rightarrow R_G = 384\Omega$

$\omega_{pout} = 2\pi(10G) = \frac{1}{R_D . C_{out}} = \frac{1}{R_D C_{GD2}}$

$\Rightarrow R_D = 1.768K\Omega$

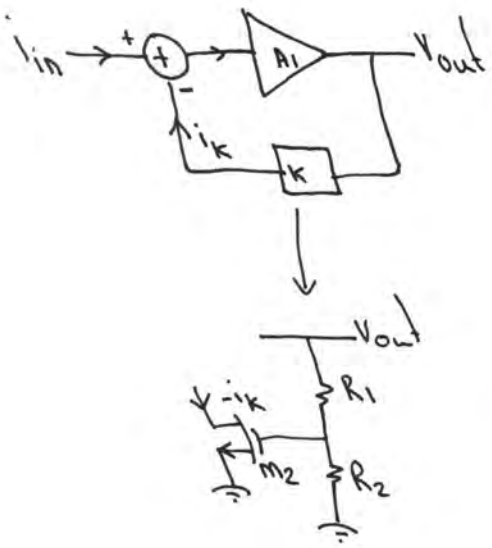
$\therefore A_V = -g_{m1}R_D = -8.84$ (remember $\lambda = 0$) $\hookrightarrow \therefore r_o = \infty$

(e) Current in, voltage out $\therefore$ transimpedance amplifier

Ideally $R_{in} = 0$

$R_{out} = 0$

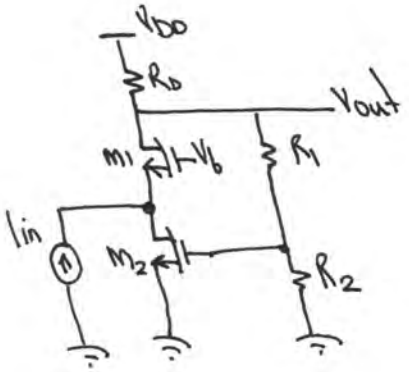
(f) feedback network consists of R_1, R_2 and M_2



$K = \frac{i_K}{V_{out}}$ (S)

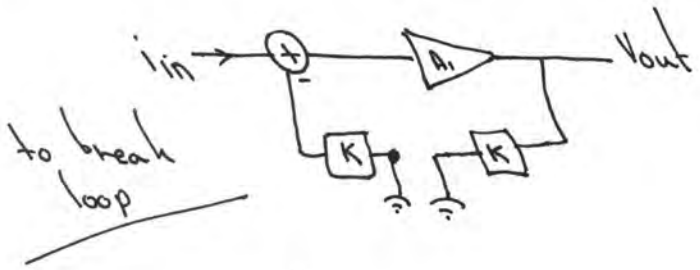
$i_K = V_{GS2}g_{m2}$

$= \frac{V_{out}R_2 . g_{m2}}{R_1+R_2} \Rightarrow K = + \frac{R_2 g_{m2}}{R_1+R_2}$

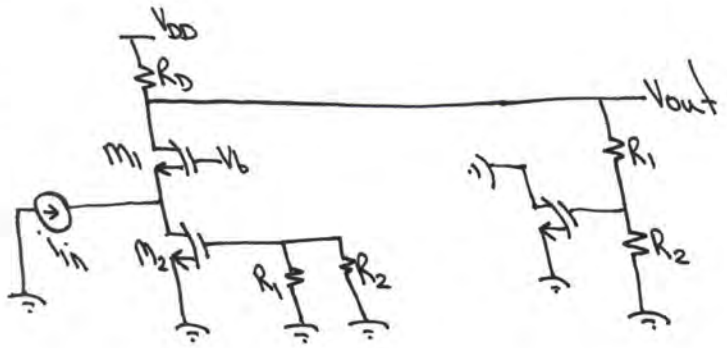


Note: $R_{in} = \frac{1}{g_{m_1}} \| r_{o1} \| r_{o2}$

$R_{out} = R_D \| (R_1 + R_2) \| r_{o1}$



$\therefore$



Since $i(m_2) = 0$.

$i(m_1) = i_{in}$

$\therefore V_{out}(o.L) = i_{D1} R_{out}$

$= i_{in} (R_D \| r_{o1} \| (R_1 + R_2))$

$$\frac{v_{out}}{i_{in}} = R_D \| r_{o1} \| (R_1 + R_2)$$

(9) $$R_{in(CL)} = \frac{R_{in(OL)}}{1 + A_1 K} = \frac{\frac{1}{g_{m_1}} \| r_{o1} \| r_{o2}}{1 + \left[R_D \| r_{o1} \| (R_1 + R_2)\right]\left[\frac{R_2 g_{m2}}{R_1 + R_2}\right]}$$

$$R_{out(CL)} = \frac{R_{out(OL)}}{1 + A_1 K} = \frac{R_D \| (R_1 + R_2) \| r_{o1}}{1 + \left[R_D \| r_{o1} \| (R_1 + R_2)\right]\left[\frac{R_2 g_{m2}}{R_1 + R_2}\right]}$$