E4-16
EE9-AC6

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2016

MSc and EEE PART IV: MEng and ACGI

ANALOGUE SIGNAL PROCESSING

Corrected copy

Monday, 16 May 10:00 am

Time allowed: 3 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s):	P. Georgiou
	Second Marker(s):	K. Fobelets

Special instructions for students

Unless otherwise stated the following parameters have the following definitions:

V_{DS}: *Drain Source Voltage.*

V_{GS}: *Gate Source Voltage.*

V_{TH}: *Threshold Voltage.*

U_t: *Thermal Voltage.*

n : *Weak Inversion Slope factor.*

g_m: *Transconductance.*

1.

a. State two advantages and two disadvantages of encoding analogue signals in time rather than amplitude. [4]

b.

i. Draw a circuit that encodes a current mode signal in a domain that is continuous in time but discrete in amplitude. [4]

ii. Explain its operation using both equations of the relationship between the input and output signals as well as time domain plots of the amplitude of an encoded analogue signal. [4]

c. For the cascade of amplifiers shown in Figure 1.1, derive the output referred noise and explain what factors can be optimized to improve the signal to noise ratio. [6]

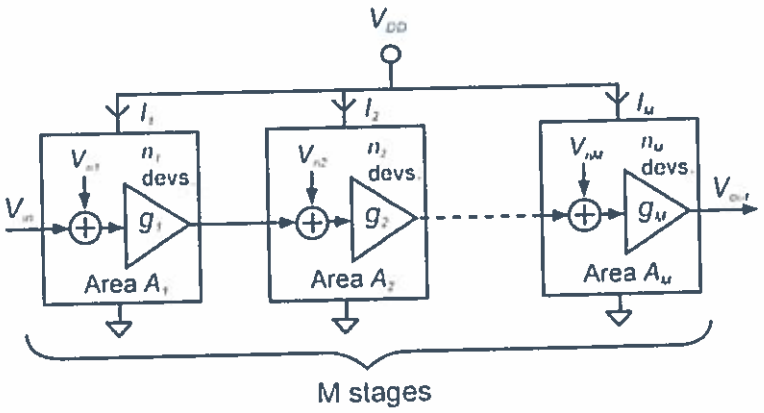

Figure 1.1: Cascade of amplifiers

2.

a.

i. Explain why MOSFETs operating in weak-inversion make suitable translinear elements. [2]

ii. Give two limitations when using these in translinear circuits (may apply specifically to weak inversion operation). [2]

b. Figure 2.1 shows a translinear circuit.

i. Derive the function of the circuit using the translinear principle. I_z is the output and I_x is the input. [2]

ii. Show how, with the addition of a few transistors, the circuit can be modified to calculate the function:

$$I_Z = \frac{(I_X)^4}{I_0^3} - I_x$$

[5]

iii. A capacitor is added between the point A on the circuit in Figure 2.1 and ground. Derive the new transfer function of the circuit stating the gain and time constant. The final equation of the transfer function should be represented in the s-domain. [5]

c. The equation for calculating the harmonic mean of a signal is given by:

$$Z = \frac{2XY}{X+Y}$$

Show how this equation can be re-arranged to design and implement the translinear circuit shown in Figure 2.2 deriving also the out current I_z. [4]

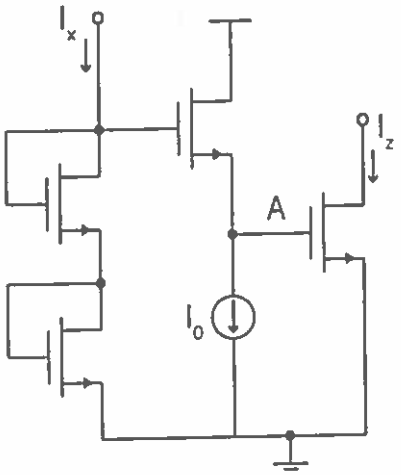

Figure 2.1: Translinear circuit (2b).

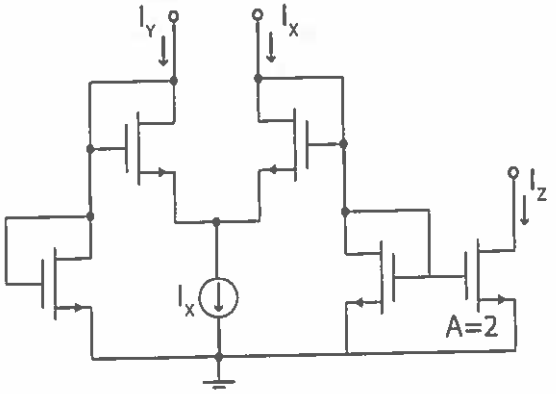

Figure 2.2: Translinear circuit (2c).

3. The transfer function of a second order topology has been decomposed into the following state-space equations:

$$\dot{X}_1 = -\frac{\omega_0}{Q} X_1 + \omega_0 X_2$$

$$\dot{X}_2 = -\omega_0 X_1 + \omega_0 U$$

$$Y_1 = X_1$$

$$Y_2 = X_2$$

whereby Y_1 and Y_2 are the outputs and X_1 and X_2 are the state-variables and U is the input.

a. Show that the output Y_1 can be used to implement a second order lowpass transfer function and the output Y_2 can be used to implement a "two-pole one-zero" second order transfer function.

[4]

b. By using the mappings below, show how these state space equations can be mapped to non-linear log-domain design equations. State any assumptions you make.

$$X_1 = I_1 \exp\left(\frac{V_1}{nU_t}\right) \qquad X_2 = I_2 \exp\left(\frac{V_2}{nU_t}\right) \qquad U = I_U \exp\left(\frac{V_U}{nU_t}\right)$$

[6]

c. With these log-domain design equations, sketch a schematic of the final log domain topology which realises the two outputs Y_1 and Y_2 using weak inversion MOS transistors.

[8]

d. Given that the low pass biquad filter output at Y_1 has a cut-off frequency, f_0 = 4 kHz, select a suitable value for the tuning current I_ω given that the filter capacitor is C = 10 pF, n = 1.23 and U_t = 25 mV.

[2]

4.

a. Figure 4.1 depicts a switched current memory cell.

i. State two limitations of the circuit shown in figure 4.1 and draw an improved schematic which compensates for these.

[4]

ii. Using your schematic from part 4.a.i, design a unit delay cell proving a z^{-1} function and derive the equation for its operation.

[4]

iii. Figure 4.2 depicts an FIR filter architecture. Using your unit delay cell from part 4.a.ii, sketch a full circuit schematic that implements this function. You may assume the current is unidirectional and use only pMOS current mirrors to copy the current.

[6]

iv. What is the function of the FIR filter shown in Figure 4.2 ?

[2]

b. Figure 4.3 shows a schematic of a switched current integrator. Derive the transfer function of the switched current integrator and show that in the z-domain this may be represented as $H(z) = A/(z-1)$.

[4]

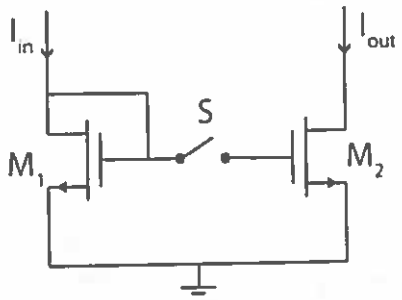

Figure 4.1: Switched current memory cell

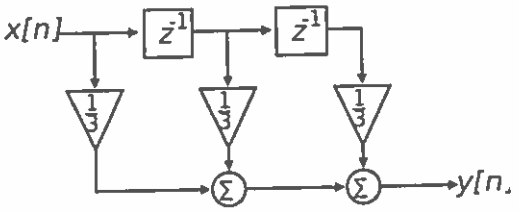

Figure 4.2: FIR filter architecture

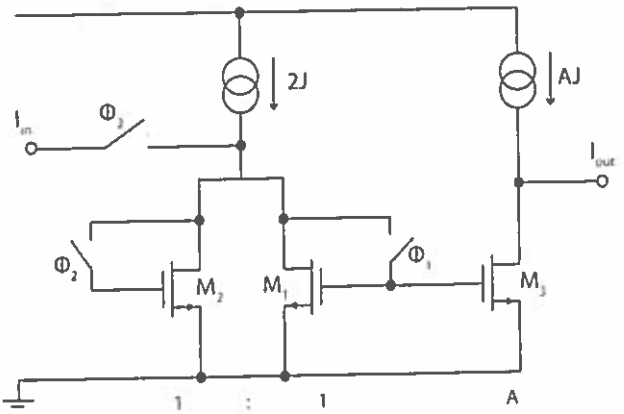

Figure 4.3: Switched current integrator

5. Figure 5.1 shows a multistage autozeroing amplifier.

a. Explain how this amplifier performs an autozeroing operation. Sketch the timing diagrams of the switches and derive the voltages V_1, V_2 and the voltages across the capacitors C_1 and C_2 for each clock phase. You may use only three stages in your explanation

[8]

b. Derive an equation for the input referred offset, $V_{os\text{-}res}$ for your cascade of amplifiers in Figure 5.1.

[2]

c. For your derivation in part 5.a, assuming a three stage cascade of autozeroing amplifiers, each with a gain $A = 100$ and an offset $V_{os} = 50$ mV, calculate the value of the storage capacitor, $C_1 = C_2 = C_3$, such that the total input referred offset, $V_{os\text{-}res} < 100$ μV. You may assume that a charge of $q_{inj} = 6\text{x}10^{-12}$ C is inserted each time the switch closes.

[2]

d. For a generic operational amplifier, desribe a technique which allows detection of very small voltage signals which exist below the *1/f* noise floor of the amplifier. Include diagrams showing the operation of this technique and how the frequency spectrum of the signal and noise is shaped at each stage.

[6]

e. Sketch a circuit that implements the method used in part 5.d to provide amplification using discrete op-amps.

[4]

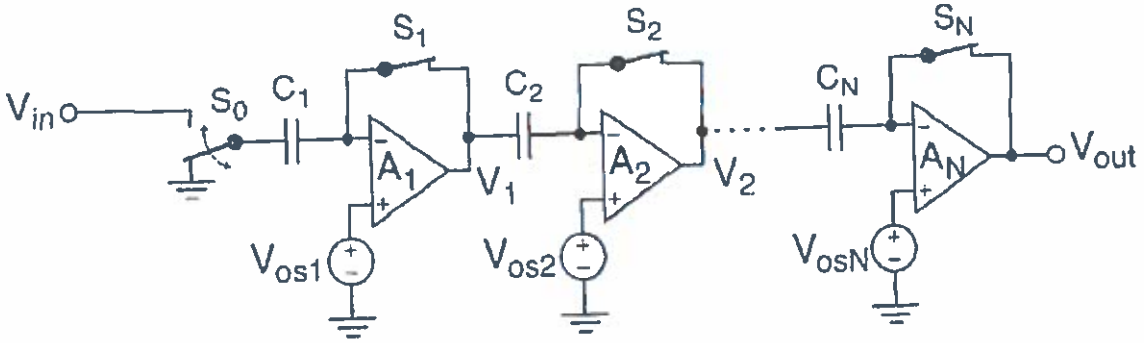

Figure 5.1: Multistage autozeroing amplifier.

6.

a. Sketch the block level architecture of a fully implantable cochlear prosthesis chip and explain the functions of each of the blocks shown in your figure. [10]

b. Figure 6.1 shows and automatic gain control system (AGC) typically used in cochlear prosthesis. The rectifier uses a current conveyor to convert the voltage V_{out} to a rectified current. The signals that follow, i_{REC}, i_{ED}, a_V and i_{GAIN} are all based on current mode operation. The translinear controller implements a square root operation $y = \sqrt{x}$. Sketch the full circuit schematic of the AGC stating assumptions where necessary. The varible gain amplifier does not need a transistor level schematic. [10]

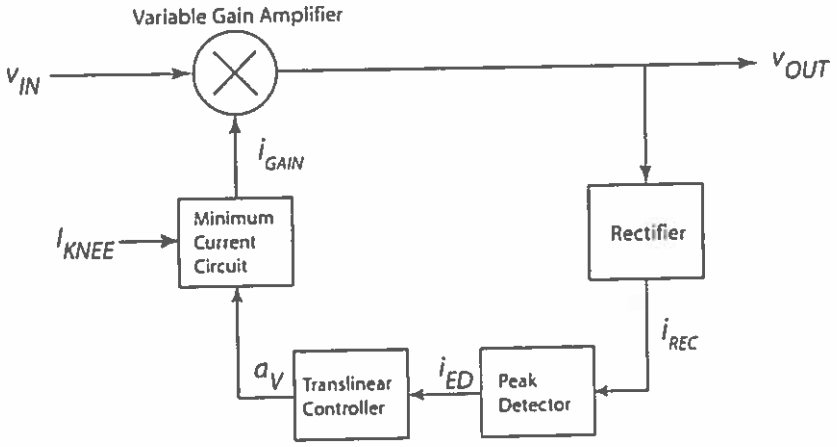

Figure 6.1: Automatic gain control system.