1. This question consists of 5 sub-questions. Each item can be answered in a few words or a short paragraph with use of a diagram and/or expression where helpful. Please answer all sub-questions and simplify expressions where possible stating any assumptions made.

a) Which of the topologies shown below in Fig. 1.1 would have better performance? Explain why. [5]

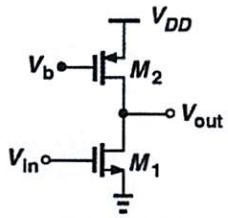


Fig. 1.1(a)

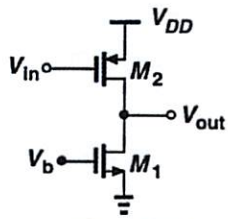


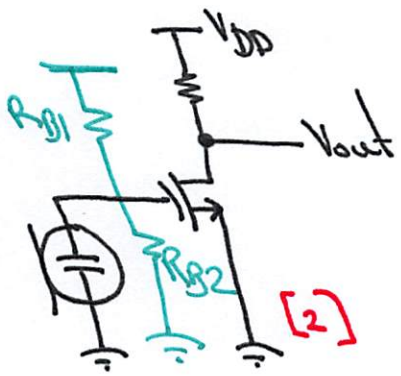
Fig. 1.1(b)

Although both the circuits have the same function [1] — common source amplifier with active load ($A_v = -g_{mx}(r_{o1} \| r_{o2})$ with x = CS amplifier transistor), [1] in cct. (a) amplifier is NMOS whereas in (b) is PMOS. Assuming device sizes are identical design (a) would be preferable. This is because $\mu_n > \mu_p$ (approx. x3) [1] and therefore g_m(NMOS amp) > g_m(PMOS amp) [1] ∴ A_v also higher. [1]

Most students identified fact that topologies are the same → but attributed difference to body effect and not mobility. Body effect is not relevant as $V_{SB} = 0$ for both.

b) Propose a *circuit topology* (e.g. common source amplifier with resistive load), for each of the following applications, in each case justifying your selection, and sketching the circuit schematic.

(i) A pre-amplifier to interface to a capacitive microphone. [5]

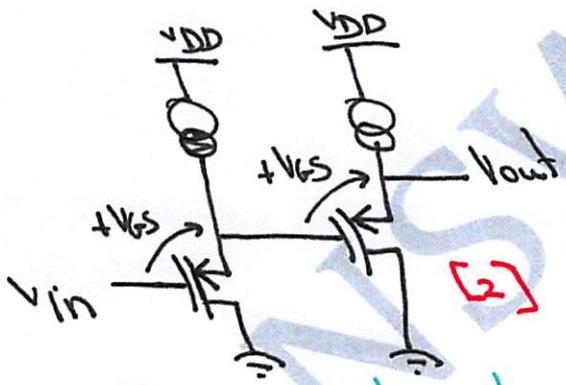


[2]

A capacitive microphone would have a very high impedance ∴ [1] can provide no output current so amp with very high Z_{in} [1] needed not to load. Such an amp. is CS amplifier (MOSFET) [1] also to provide moderate voltage gain.

Many students incorrectly ~~attempted to~~ proposed a circuit for good high frequency performance.

(ii) A circuit to increase the DC level of a signal by 1V. [5]

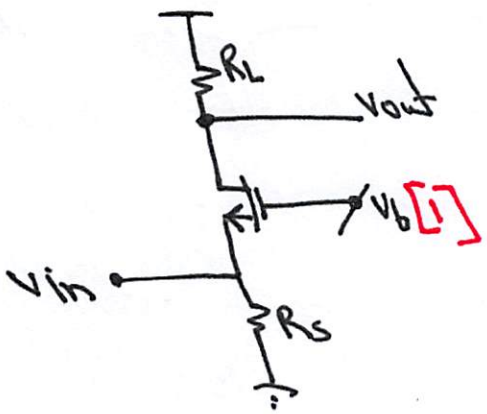


[2]

CD (or source follower) stage(s) biased with constant current - appropriate for level shift. [1] Each stage can achieve +VGS DC level shift. Suggest 2 stages [1] identical → each +0.5V (Amos) [1]

Surprisingly about 1/2 students proposed CS topology. Very few mentioned 2 stages.

(iii) A high frequency amplifier providing relatively high isolation between the input and output. [5]



[1]

CG (or CB) amplifier exhibit very good high frequency response as there is no parasitic capacitance between i/p and o/p. [1] As a result does not suffer from the Miller effect [1] furthermore CG amp can be designed to match a 50Ω load (since $Z_{in} \approx 1/g_m$).

Most correct. Confused by "isolation" [1]

c) An inverting amplifier must provide a nominal gain of 20 with a gain error of 0.5%. Determine the minimum required op-amp gain.

[5]

$$\text{Gain error} = \frac{1}{A_0}\left(1+\frac{R_1}{R_2}\right)$$ [3] - 2 for deriving 1 for expression

$$\frac{1}{A_0}(1+20) = 0.5\% \rightarrow A_0 = 4200$$ [1] [1]

very well answered.

d) Determine the closed loop gain of the circuit shown below in Fig. 1.2. Assume $\lambda = 0$.

[5]

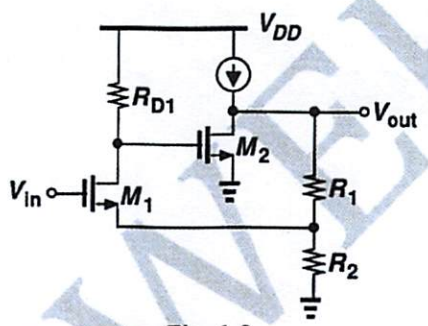
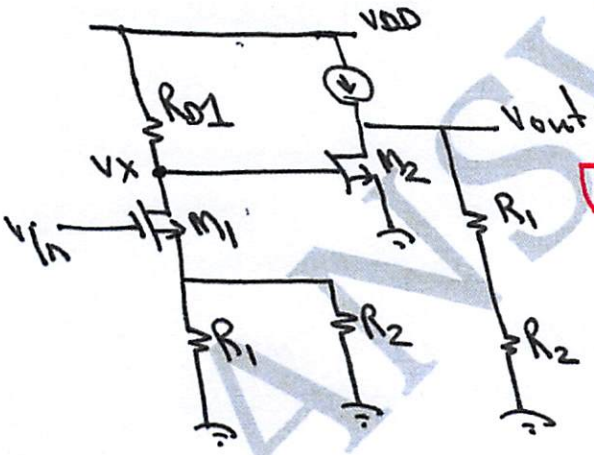


Fig. 1.2

Break the loop:



[2]

$$\left.\frac{V_{out}}{V_{in}}\right|_{\text{open-loop}} = \frac{V_{out}}{V_x}\cdot\frac{V_x}{V_{in}} = \frac{-R_{D1}}{\frac{1}{g_{m1}}+R_1\|R_2} \times -g_{m2}(R_1+R_2)$$

$$= \frac{g_{m1}g_{m2}R_{D1}(R_1+R_2)}{1+g_{m1}(R_1\|R_2)}$$ [2]

$$k = \frac{R_2}{R_1+R_2}$$

$$\therefore \left.A_v\right|_{\text{closed loop}} = \frac{A_v(OL)}{1+kA_v(OL)} = \frac{\frac{g_{m1}g_{m2}R_{D1}(R_1+R_2)}{1+g_{m1}(R_1\|R_2)}}{1+\frac{g_{m1}g_{m2}R_{D1}R_2}{1+g_{m1}(R_1\|R_2)}}$$ [3]

Likewise. Most answered correctly

e) Derive expressions (by inspection) for the *output resistance* of the amplifier circuits shown below in Fig. 1.2 (including r_o).

[10]

(i)

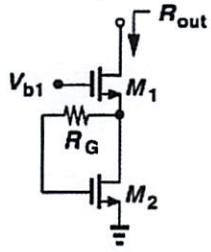


Fig. 1.2(a)

(ii)

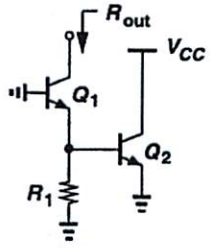
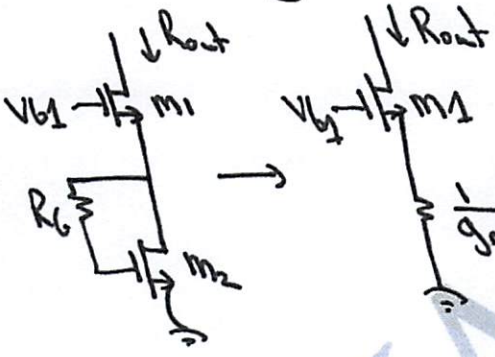


Fig. 1.2(b)

(i) R_G effectively makes M_2 diode connected [1]



[1]

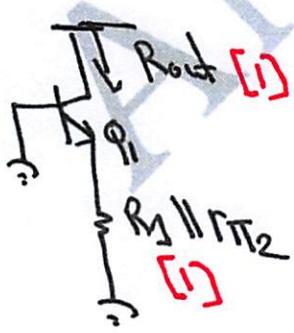
Many students identified no current through R_G so removed. Only about ¼ identified that it makes M_2 effectively diode-connected.

$\therefore R_{out} = g_{m1} r_{o1} \left(\frac{1}{g_{m2}} \| r_{o2}\right) + r_{o1} + \frac{1}{g_{m2}} \| r_{o2}$ [1]

$\approx g_{m1} r_{o1} \left(\frac{1}{g_{m2}} \| r_{o2}\right)$ [1]

(assuming 1st term greater than others) [1]

(ii)



[1]

[1]

$R_{out} = r_{o1} + g_{m1}(R_1 \| r_{\pi 2} \| r_{\pi 1}) r_{o1} + R_1 \| r_{\pi 1} \| r_{\pi 2}$

$= r_{o1} + (1 + g_{m1} r_{o1})(r_{\pi 1} \| R_1 \| r_{\pi 2})$

[1]

[1]

Answered well

1 mark for not simplifying/approximating

2. The circuit shown below in Fig. 2.1 is a single-stage fully differential amplifier with corresponding transistor dimensions shown in Table 2.1.

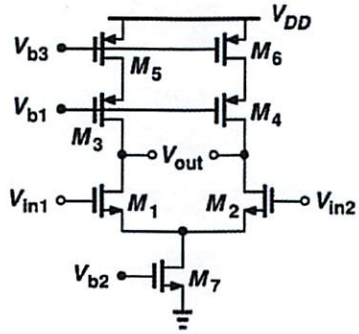


Fig. 2.1

Table 2.1. Transistor sizes

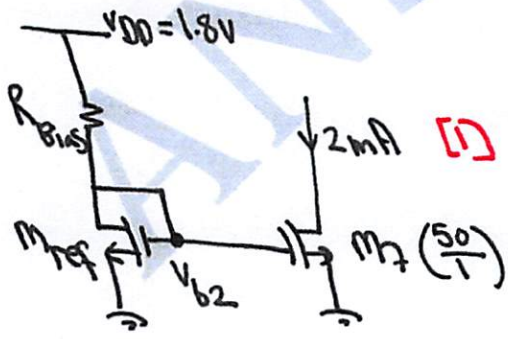
M_1	M_2	M_3	M_4	M_5	M_6	M_7
200/0.5	200/0.5	9/0.18	9/0.18	50/1	50/1	50/1

Assume all devices are in saturation and assume $\lambda \neq 0$. Use the following expression for the large signal drain current of a MOSFET (in saturation) with corresponding transistor parameters:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$\mu_n C_{ox} = 200\mu A/V^2$ $\quad V_{THN} = 0.4V$ $\quad \lambda_N = 0.1V^{-1}$
$\mu_p C_{ox} = 100\mu A/V^2$ $\quad V_{THP} = -0.5V$ $\quad \lambda_P = 0.2V^{-1}$

a) Design a voltage reference circuit to generate V_{b2} from a 1.8V supply such that $I_{D7} = 2mA$. [5]



[1]

$$V_{b2} = V_{GS7} = \sqrt{\frac{2I_{D7}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_7}} + V_{TH}$$ [1]

$$= \sqrt{\frac{2(2mA)}{200\mu A/V^2 (50)}} + 0.4$$

$$= 1.03V$$ [1]

Assuming 1:1 mirror $M_{ref}\left(\frac{W}{L}\right) = \frac{50}{1}$ [1]

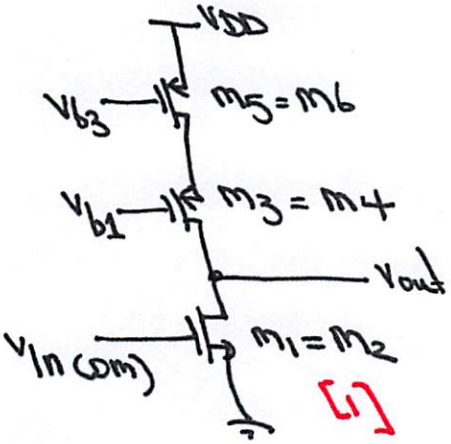
$$R_{Bias} = \frac{1.8 - 1.03}{2mA} = 385\Omega$$ [1]

most students designed a potential divider → ok → but I expected mention of sensitivity to VDD variation

b) Determine an expression for the differential voltage gain of the amplifier.

[5]

Assuming perfect symmetry → equivalent ½ cct approx. [1]



[1]

∴ CS amplifier

$A_v = -g_m(R_D \| r_o)$ [1]

$= -g_{m1}(r_{o1} \| (g_{m3}r_{o3}r_{o5} + r_{o3} + r_{o5}))$ [1]

$\approx -g_{m1}r_{o1}$

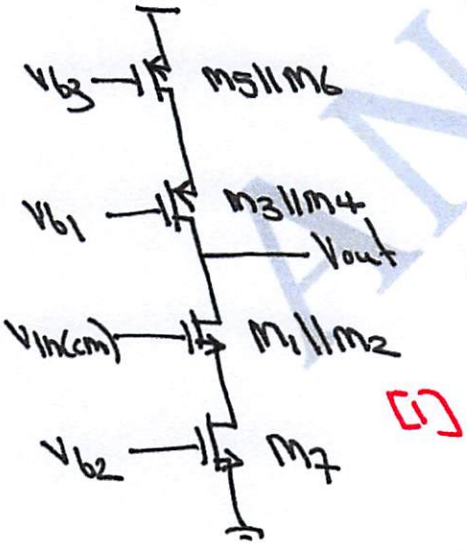
(since $r_{o1} \ll g_{m3}r_{o3}r_{o5}$) [1]

many students missed this

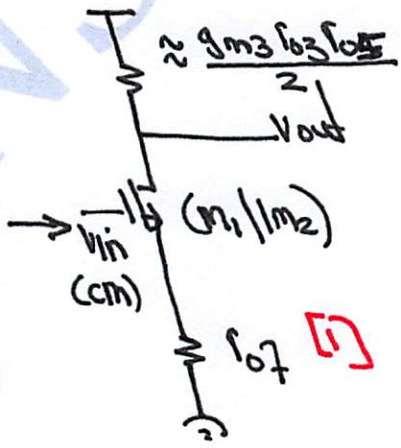
c) Determine an expression for the common-mode voltage gain of the amplifier.

[5]

Short $v_{in1} = v_{in2}$ and draw equ. cct. for CM gain



[1]



[1]

Here several students incorrectly used $G_m = g_{m1}$.

A_v = CS with degen.

$= \frac{-R_D}{\frac{1}{g_m} + R_S}$ [1]

$= \frac{\frac{-g_{m3}r_{o3}r_{o5}}{2}}{\frac{1}{2g_{m1}} + r_{o7}}$

$= \frac{-2g_{m1}g_{m3}r_{o3}r_{o5}}{2(1 + 2g_{m1}r_{o7})}$ [1]

↓ Since $g_m r_o \gg 1$

$\approx \frac{-g_{m3}r_{o3}r_{o5}}{2r_{o7}}$ [1]

d) Use your answers to parts (b) and (c) to evaluate the common-mode rejection ratio.

[10]

$CMRR = \frac{A_{v(DM)}}{A_{v(CM)}}$ [1]

$A_{v(DM)} = -g_{m1} r_{o1}$

$g_{m1} = \sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}}$

$= \sqrt{2(1mA)\,200\mu(400)} = 12.6mS$

$r_{o1} = 1/\lambda_n I_D = 1/(0.1)(1m) = 10k\Omega$

$\therefore A_v = -126.49$ [1] [2]

$A_{v(CM)} = \frac{-g_{m3} r_{o3} r_{o5}}{2 r_{o7}}$

$g_{m3} = \sqrt{2(1m)(100\mu)(50)} = 3.16mS$

$r_{o3} = 1/\lambda_p I_{D3} = 1/0.2(1m) = 5k\Omega$

$r_{o5} = 1/\lambda_p I_{D5} = 1/0.2(1m) = 5k\Omega$ [3]

$r_{o7} = 1/\lambda_n I_{D7} = 1/0.1(2m) = 5k\Omega$

$A_{v(CM)} = -\frac{3.16mS\,(5k)(5k)}{2(5k)}$

$= -7.9$ [1]

$CMRR = \frac{126.49}{7.9} = 16.01$ [1]

$= 20\log(16.01) = 24.1dB$ [1]

Good

e) State the function of transistors $M_1 - M_2$, $M_3 - M_4$, $M_5 - M_6$, and M_7 and comment on the specified device sizes.

[5]

M_1/M_2 – differential pair [1]. Large $\frac{W}{L}$ → large g_m → large $A_{v(DM)}$ [1]

M_3/M_4 – cascode [1] → minimize W.L → minimize capacitance

M_5/M_6, M_7 } current sources/sinks [1]. Large $\frac{W}{L}$ to generate relatively large I_D for acceptable V_{GS} [1]

only about 1/2 students commented on device sizes.

3. The circuit below in Fig. 3.1 illustrates a cascade of two identical common source stages.

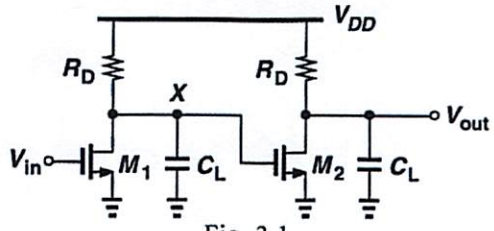


Fig. 3.1

a) Neglecting channel-length modulation and other capacitances, construct the Bode plot of V_{out}/V_{in} including both the magnitude and phase responses.

[8]

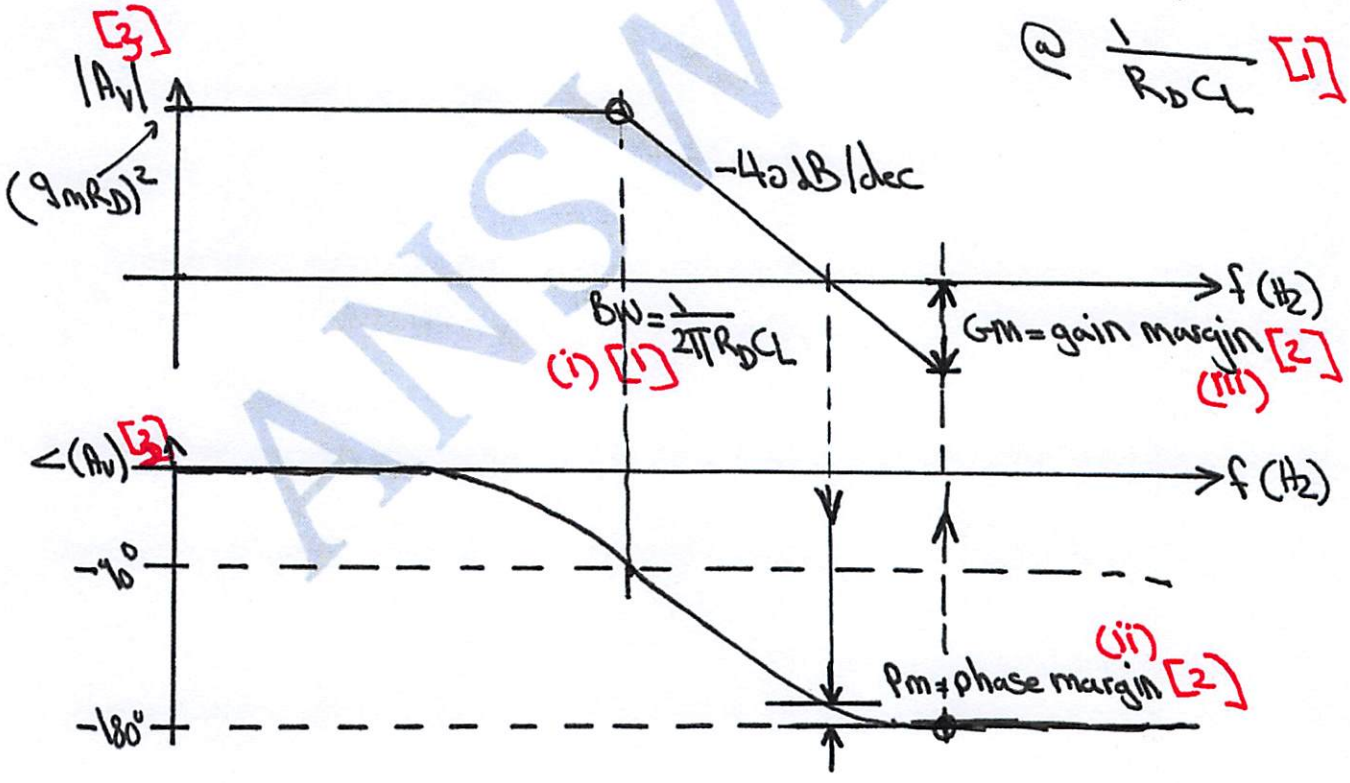
Assuming $\lambda = 0$ and neglecting other capacitances.

DC gain: $\frac{V_x}{V_{in}} = -g_{m1}R_D$

$\frac{V_{out}}{V_x} = -g_{m2}R_D$

$A_V = \frac{V_{out}}{V_{in}} = (g_m R_D)^2$ [1]

with 2 poles @ $\frac{1}{R_D C_L}$ [1]



b) Annotate your plot with the following: (i) *Bandwidth*; (ii) *Phase margin*; (iii) *Gain Margin*.

[5]

Also PM + GM annotated horizontally (in freq)

I was not annotated correctly instead of BW → GBP

c) Derive the transfer function of the circuit, substitute $s = j\omega$, and obtain an expression for $|V_{out}/V_{in}|$. Determine the -3dB bandwidth of the circuit.

[10]

$$\frac{v_x}{v_{in}}(s) = -g_m\left(R_D \parallel \frac{1}{C_L s}\right) = -g_m\left(\frac{R_D}{R_D C_L s + 1}\right)$$ [1]

$$\frac{v_{out}}{v_x}(s) = -g_m\left(\frac{R_D}{R_D C_L s + 1}\right)$$ [1]

$$H(s) = \frac{v_x}{v_{in}}(s) \cdot \frac{v_{out}}{v_x}(s) = \left(\frac{g_m R_D}{R_D C_L s + 1}\right)^2$$ [1]

$$s \to j\omega \quad H(j\omega) = \left(\frac{g_m R_D}{1 + R_D C_L j\omega}\right)^2$$

$$|H(j\omega)| = \frac{(g_m R_D)^2}{1 + (R_D C_L \omega)^2}$$ [1]

-3dB bandwidth:

$$\frac{(g_m R_D)^2}{1 + (R_D C_L \omega)^2} = \frac{(g_m R_D)^2}{\sqrt{2}}$$ [2]

$$\Rightarrow (R_D C_L \omega)^2 + 1 = \sqrt{2}$$

$$\Rightarrow \omega = \frac{\sqrt{\sqrt{2} - 1}}{R_D C_L} = \frac{0.6436}{R_D C_L} \text{ (rad/s)}$$ [1]

$$2\pi f = \frac{0.6436}{R_D C_L} \Rightarrow f = \frac{0.1024}{R_D C_L} \text{ (Hz)}$$ [2]

Most students missed these last steps.

i.e. Solving for -3dB BW

d) Using your answers to parts (b) and (c), design the two-stage amplifier for a total voltage gain of 15 and $-3dB$ bandwidth of 1.8GHz. Assume each stage carries a bias current of 1mA, CL=40fF, and $\mu_n C_{ox} = 200\mu A/V^2$. [7]

Bias current = 1mA (each stage)

C_L = 40ff

$\mu_n C_{ox} = 200\mu A/V^2$, $A_v = 15$, $-3dB$: 1.8GHz

DC gain: $(g_m R_D)^2 = 15$ [1]

$-3dB$ BW: $\frac{0.1 \text{ or } 243}{R_D C_L} = 1.8GHz$ [1]

Since C_L = 40ff $\rightarrow$ $R_D = 1422.6\Omega$ [1]

$(g_m R_D)^2 = 15 \Rightarrow g_m = 0.0027S = \frac{2I_D}{V_{GS} - V_{TH}}$ [1]

$\Rightarrow V_{GS} - V_{TH} = 0.741V$ [1]

$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) \Rightarrow \frac{W}{L} = \frac{g_m}{\mu_n C_{ox}(V_{GS} - V_{TH})}$ [1]

$= 18.2$ [1]

$\therefore$ $R_D = 1.42k\Omega$

$C_L = 40ff$

$V_{GS} - V_{TH} = 0.741V$

$\frac{W}{L} = 18.2$

Method mostly ok. Very few numerically correct answers.