EE2-2

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2013

EEE PART II: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 2

Wednesday, 12 June 2013 2:00pm

Time allowed: 2 hours

There are THREE questions on this paper.

ALL questions are compulsory.
Question 1 carries 40% of the marks and Questions 2 and 3 carry 30% each.

Any special instructions for invigilators and information for candidates are on page 1.

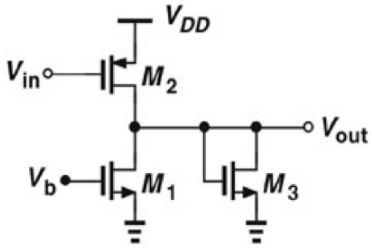
Basic expressions for voltage gain, input and output resistance for single stage amplifiers are given on the last page.

Examiners responsible	First Marker(s):	T.G. Constandinou
	Second Marker(s):	C. Toumazou

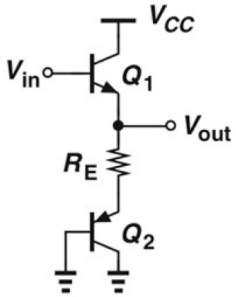
1. This question consists of 6 sub-questions. Each item can be answered in a few words or a short paragraph with use of a diagram and/or expression where helpful. Please answer all sub-questions and simplify expressions where possible stating any assumptions made.

   a) Draw the *small signal model* of a bipolar transistor with parasitic capacitances and explain what limits its high frequency performance when configured as a *common emitter* amplifier. [5]

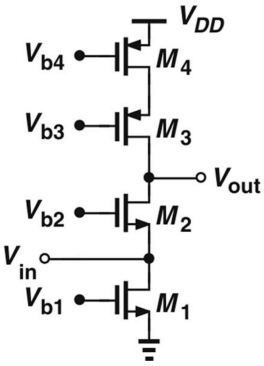
   b) Derive expressions (by inspection) for the *voltage gain* of the amplifier circuits shown below (assuming $\lambda \neq 0$ and $V_A > 0$, i.e. including r_O). [15]



(i)



(ii)

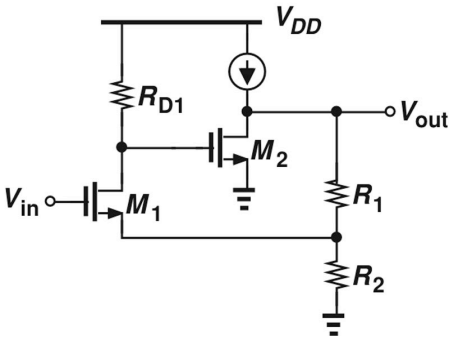


(iii)

   c) Describe what is meant by *common mode rejection ratio (CMRR)* and by using an example application, explain why this is important. [5]

   d) Describe (using a diagram) what is meant by the term *phase margin*. What is a typical phase margin target (in degrees)? [5]

   e) Derive expressions for the *closed loop gain* of the circuit below. Assume $\lambda = 0$. [5]



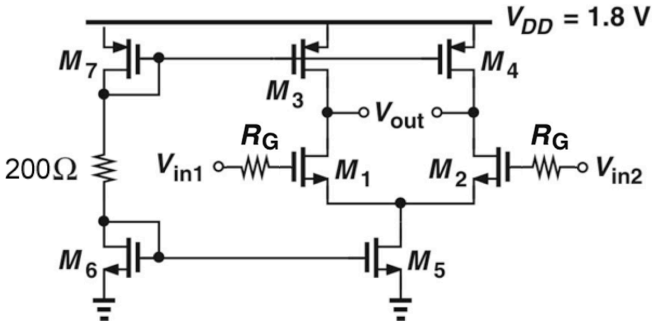
   f) Given an operational amplifier has a *gain-bandwidth product* of 100MHz, an *open-loop gain* of 80dB, maximum *slew rate* of 100kV/s, and rail-to-rail output range, calculate: (i) the -3dB bandwidth, (ii) the full-power bandwidth for a ±3.3V power supply. [5]

2. The circuit shown below is a single-stage fully differential amplifier.

Assume all devices are in saturation and $\lambda>0$ (i.e. $R_{out}<\infty$). Use the following expression for the large signal drain current of a MOSFET (in saturation) with corresponding transistor parameters:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS}-V_{TH}\right)^2$$

$\mu_n C_{ox} = 200\mu A/V^2$ $\quad V_{THN} = 0.4V$ $\quad \lambda_N = 0.1V^{-1}$
$\mu_p C_{ox} = 100\mu A/V^2$ $\quad V_{THP} = -0.5V$ $\quad \lambda_P = 0.2V^{-1}$



a) Determine expressions for the *differential gain* and *common-mode gain* stating any assumptions made. [6]

b) Calculate $(W/L)_3$, $(W/L)_4$ and $(W/L)_7$ given $I_{D5}=2I_{D6}=2mA$ and $(W/L)_5=2(W/L)_6=100/1$. [4]

c) Calculate $(W/L)_1=(W/L)_2$ for a differential gain of 15. [3]

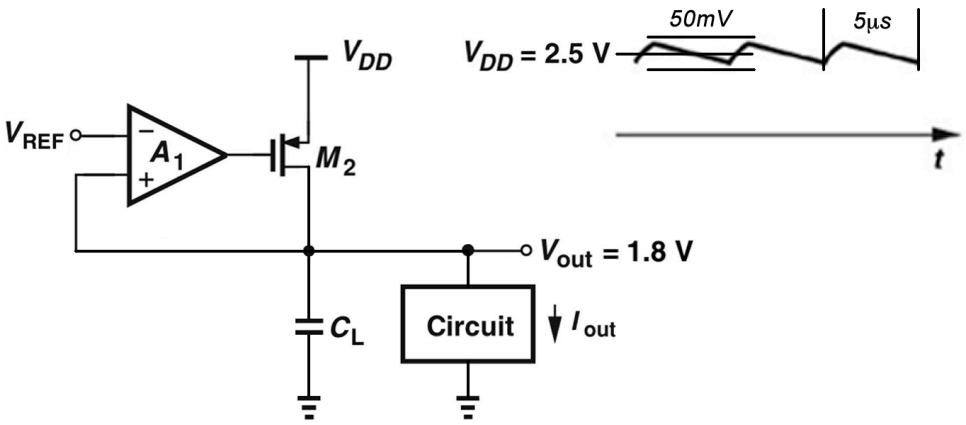
d) Using a half circuit approximation, redraw the differential amplifier circuit above to: (i) identify any nodes that are associated with poles and (ii) include all the parasitic device capacitances. [5]

e) Determine expressions for the pole frequencies stating any assumptions made. Where required, use the following parasitic capacitance values: $C_{GS} = (2/3)WLC_{ox}$, $C_{ox} = 12fF/\mu m^2$, $C_{GD} = C_0W$, $C_0 = 0.2fF/\mu m$, $C_{DB} = C_{SB} = 0$. [5]

f) Given all device lengths ($L_1=L_2=L_3=L_4=L_5=L_6=L_7$) are 1μm and $R_G=2k\Omega$, evaluate the pole frequencies and sketch the bode plot (magnitude response only) for the amplifier. [7]

3. The circuit shown below is a *low dropout (LDO) voltage regulator* for providing a stable DC voltage supply to a load circuit. The required output voltage (V_{out}) is 1.8V with a maximum supply current of 100mA.

   Use the same transistor expressions/parameters given previously in Question 2.



   a) Determine expressions for the *open loop gain* and *feedback factor* of the regulator circuit. [4]

   b) Calculate the low frequency *output impedance* of the voltage regulator, assuming $(W/L)_2$=100/1 and A_1=85dB. [5]

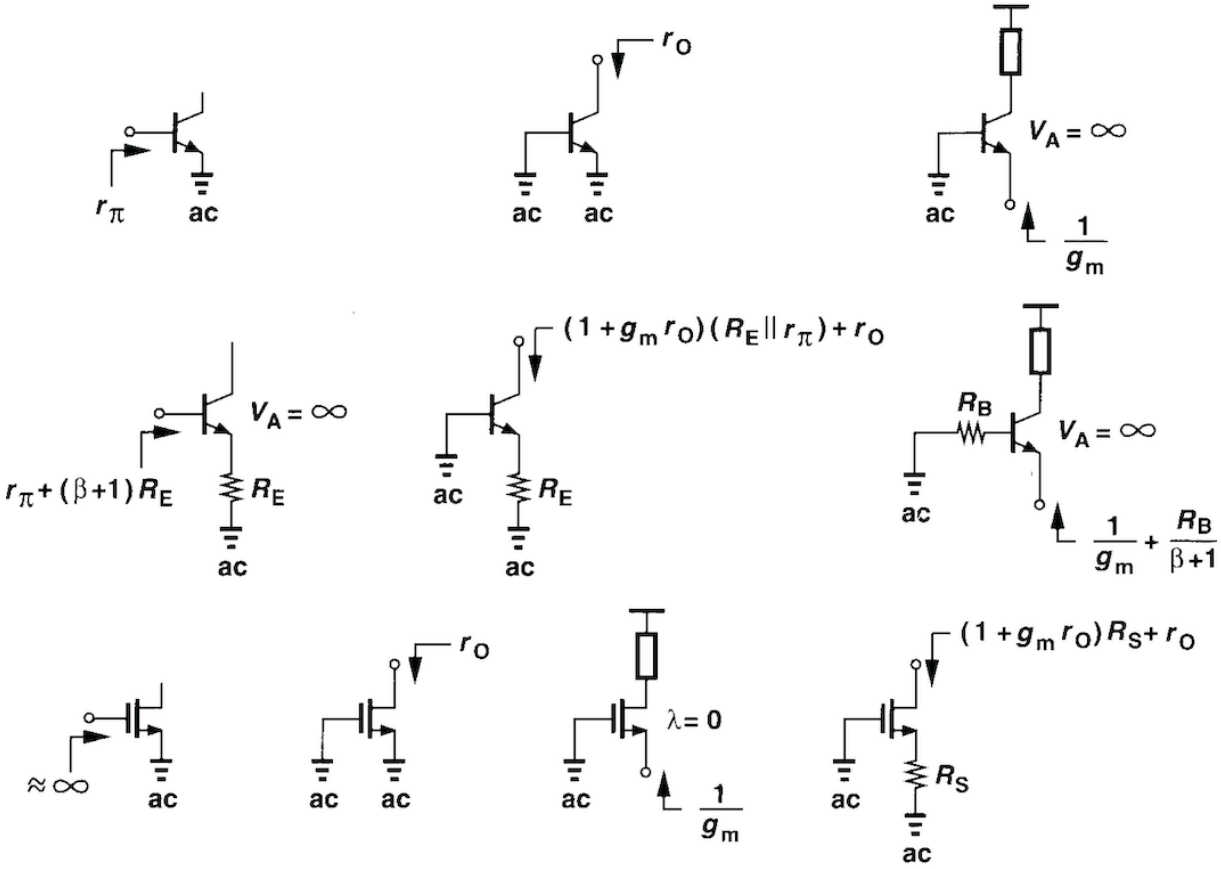
   c) Discuss how the specifications of the operational amplifier need to be selected such that the ripple (shown on right of Figure) is rejected at the regulated output (V_{out}). [5]

   d) Discuss how should the value of C_L be selected? [6]

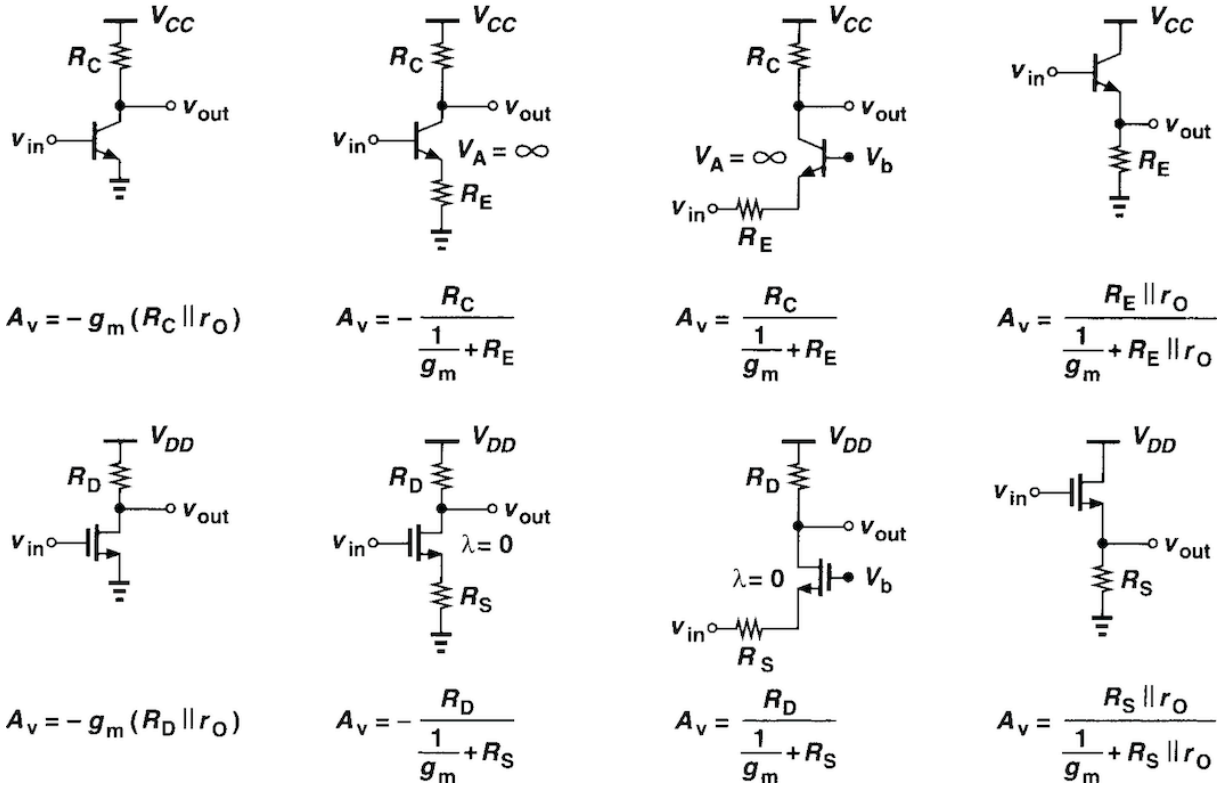
   e) State three fundamental challenges in designing circuits that generate a reference voltage or current. Describe a reference generator circuit design that overcomes one of these. [6]

   f) A voltage regulator circuit can also be implemented using an NMOS source follower output transistor (for M_2) if the input terminals to the op-amp are swapped (i.e. by connecting V_{REF} to V_+ and feedback to V_-). Give one advantage of each topology. [4]

Input and Output Impedances



Voltage Gain Equations



IMPERIAL COLLEGE LONDON

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EXAMINATIONS 2013

EEE PART II: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 2 (SOLUTIONS)

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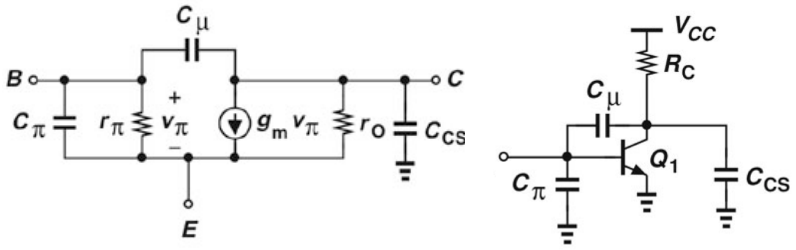
Solutions annotated as follows:

Black – model answers
Red – marking scheme
Blue – examiners feedback after marking

Question 1 – mostly bookwork (a), (c), (d) or new calculation of new example (b), (e), (f)

1. (a) When configured as a CE amplifier there are two poles (at the input and output nodes). The high frequency response is generally limited by the floating capacitance (Cμ) that is connected across the inverting amplifier stage. This therefore appears as a ("magnified") grounded capacitance at the input. i.e. Cin=Cπ+ Cμ (1+Av) due to the Miller effect. The input pole is therefore said to be the dominant.



Marking: Diagrams [3 marks], description [1 mark], mentioning HF response is Miller limited [1 mark].

[Some answers did not annotate parasitic capacitances on small signal model. Also did not identify the fact that the floating capacitance (Miller) appears amplified at the input thus limiting HF response]

1. (b)

(i)	Common Source (M2)	From formula sheet: $A_v = -g_m\left(R_D \parallel r_O\right)$ $A_v = -g_{m2}\left(r_{O1} \parallel r_{O2} \parallel r_{O3} \parallel 1/g_{m3}\right)$ Assuming: $1/g_{m3} << r_{O1}, r_{O2}, r_{O3}, \rightarrow A_v \approx -g_{m2}/g_{m3}$
(ii)	Emitter Follower (Q1)	From formula sheet: $A_v = \dfrac{R_E \parallel r_O}{R_E \parallel r_O + 1/g_m}$ $A_v = \dfrac{\left(R_E + (1/g_{m2}) \parallel r_{O2} \parallel r_{\pi 2}\right) \parallel r_{O1}}{(1/g_{m1}) + \left(R_E + (1/g_{m2}) \parallel r_{O2} \parallel r_{\pi 2}\right) \parallel r_{O1}}$ Assuming: $1/g_{m2} << r_{O2}, r_{\pi 2}, \rightarrow A_v \approx \dfrac{\left(R_E + 1/g_{m2}\right) \parallel r_{O1}}{1/g_{m1} + \left(R_E + 1/g_{m2}\right) \parallel r_{O1}}$
(iii)	Common Gate (M2)	From formula sheet: $A_v = +g_m(r_O \parallel R_D)$ $A_v = +g_{m2}\left[r_{O2} \parallel \left(g_{m3} r_{O3} r_{O4} + r_{O3} + r_{O4}\right)\right]$ Assuming: $g_m r_O >> 1, \rightarrow A_v = +g_{m2} r_{O2}$

Marking: For each circuit: [1 mark] for identifying amplifier topology, [1 mark] for identifying load, [2 marks] for full answer, [1 mark] for simplifying & assumption.

[Approximately half of all answers were incomplete due to: (1) not stating assumptions, (2) not simplifying fully].

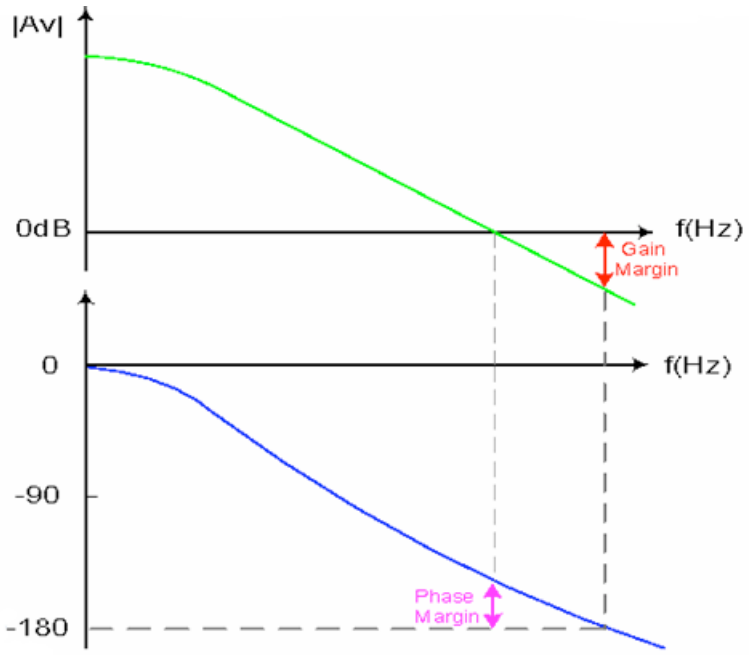
1. (c) The common-mode rejection ratio (CMRR) of a differential amplifier is defines as the ratio of differential gain to common mode gain. This provides a measure of the ability of the amplifier to "reject" any common mode signal applied to both input terminals but still amplify a differential signal. A high CMRR is important in applications where the signal of interest is represented by a small voltage fluctuation superimposed on a (possibly large) voltage offset, or when relevant information is contained in the voltage difference between two signals. One example is in sensing biopotential

signals- for example an electrocardiogram (ECG), where the differential signal is typically much smaller than the common mode signal (typically 50Hz pickup). In such an application if the common mode signal is not rejected then the maximum gain possible (to avoid the output saturated) will be limited by the common mode signal. Also audio amplifier with “hum” another possible app.

Marking: For defining CMRR [1 mark], description [1 marks], high CMRR is desirable [1 mark], example [1 mark], why important [1 mark].

[Application example generally not answered here].

1. (d) Phase margin is the difference between the phase when gain is unity (0 dB) and 180º. If at 0 dB the phase lag is greater then 180º, then the amplifier is unstable. This is because once there has been a 180º phase shift, the feedback is actually going to be positive.



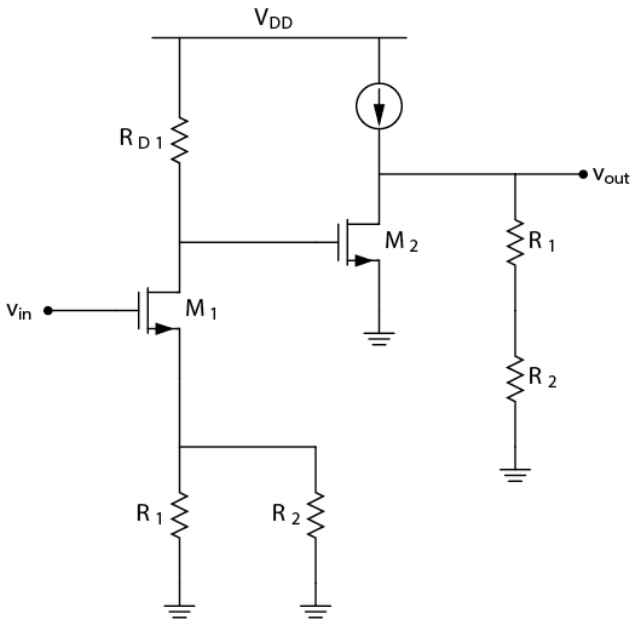
A commonly accepted design goal is a 45º phase margin.

Marking: For PM margin definition [1 marks], diagram [2 marks], reference to stability [1 mark], typical value [1 mark].

[This was generally answered well].

1. (e)

We can break the feedback network as shown here:



$$A_{OL} = \frac{g_{m1} g_{m2} R_{D1} (R_1 + R_2)}{1 + g_{m1} (R_1 \parallel R_2)}$$

$$K = \frac{R_2}{R_1 + R_2}$$

$$\frac{v_{out}}{v_{in}} = \boxed{\frac{\frac{g_{m1} g_{m2} R_{D1} (R_1 + R_2)}{1 + g_{m1} (R_1 \parallel R_2)}}{1 + \frac{g_{m1} g_{m2} R_{D1} R_2}{1 + g_{m1} (R_1 \parallel R_2)}}}$$

$$R_{in,open} = R_{in,closed} = \boxed{\infty}$$

$$R_{out,open} = R_1 + R_2$$

$$R_{out,closed} = \boxed{\frac{R_1 + R_2}{1 + \frac{g_{m1} g_{m2} R_{D1} R_2}{1 + g_{m1} (R_1 \parallel R_2)}}}$$

Marking: For breaking look [1 mark], for open loop gain [2 marks], feedback factor [1 mark], closed loop gain [1 mark].

[Answered well].

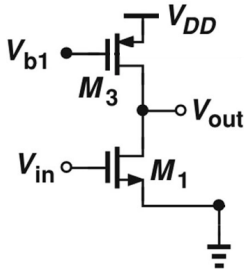
1. (f) (i) GBP=100MHz = Gain x BW -> BW = 100Mhz/10^4 = 10kHz (ii) wFP=SR/(vmax-vmin/2) = 100kV/s/(2x3.3V) = 15.15kHz.

Marking: GBP expression [1 mark] + evaluating [1 mark], wFP exp. [1 mark] + evaluating [2 marks]

[Many answers used wrong expression for full power bandwidth].

Question 2 – new theoretical application and calculation of new example

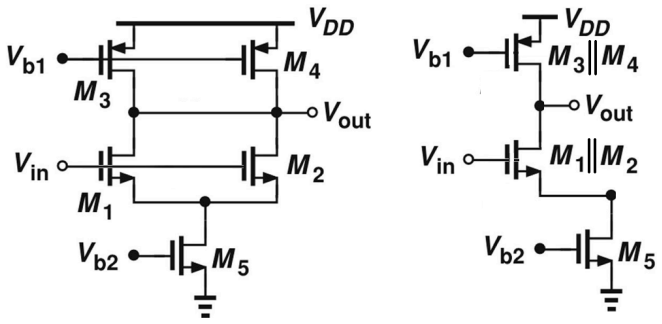
2. (a) For differential gain, due to symmetry can assume that node V_{S1}=V_{S2} is an ac ground and therefore can make half circuit approximation.



From formula sheet for CS amplifier: $A_v = -g_m(R_D \parallel r_O) \rightarrow A_{v(diff)} = -g_{m1}(r_{O1} \parallel r_{O3})$

[Approximately 10-20% of students did not assume the AC gnd and thus exclude current source transistor from half model. However, most students answered correctly].

For common-mode gain, connect inputs together and outputs together and draw the equivalent circuit.



Use: $A_v = -G_m R_{out}$, where $G_m = \frac{i_{out}}{V_{in}}$ and $i_{out} = v_{gs1} g_{m1}$ and $v_{gs1} = v_{in(CM)}\left(\frac{1/2g_{m1}}{1/2g_{m1} + r_{O5}}\right)$ (since vin and vgs are not the same). $R_{out} = R_{up} \parallel R_{down} \approx R_{up}$ (since $g_m r_O >> 1$).

$$\therefore R_{out} \approx r_{O3} \parallel r_{O4} \text{ and } A_{v(CM)} = -\frac{-2g_{m1}(1/2g_{m1})(r_{O3} \parallel r_{O4})}{(1/2g_{m1}) + r_{O5}} = -\frac{r_{O3} \parallel r_{O4}}{(1/2g_{m1}) + r_{O5}} \approx \frac{r_{O3} \parallel r_{O4}}{r_{O5}}$$

Marking: Half circuit [1 mark], differential gain [1 mark], CM equivalent circuit [1 mark], CM gain [2 marks], assumptions and simplification (CM gain) [1 marks]

[This was generally answered well- although not fully simplified / applied assumptions].

2. (b) If I_{D5}=2mA, then I_{D6}=I_{D7}=1mA

$V_{GS6} = V_{THN} + \sqrt{2I_D/(\mu_n C_{ox} W/L)} = 0.4 + \sqrt{2(1m)/(200\mu(100))} = 0.716V$

KVL across left branch: V_{DD}=V_{GS6}+I_{D6}R+V_{GS7} $\rightarrow 1.8 = 0.716 + 1m(200) + V_{GS7} \rightarrow V_{GS7} = 0.884V$

$$\left(\frac{W}{L}\right)_7 = \frac{2I_D}{\mu_p C_{ox}(V_{GS} - V_{THP})^2} = \frac{2(1m)}{100\mu(0.884 - 0.5)^2} = 148$$

Since I_{D5}=2I_{D6}, therefore I_{D3}=I_{D4}=I_{D5}/2(=I_{D6}=I_{D7}), so (W/L) of M3, M4, M7 are 148

Marking: KVL [1 mark], VGS6, VGS7 [1 mark], (W/L)s [2 marks]

[Mostly answered correctly – some errors using mobility of NMOS instead of PMOS]

2. (c) If differential gain is $|A_{v(diff)}| = g_{m1}(r_{O1} \parallel r_{O3}) = 15$, need g_{m1}, r_{O1}, r_{O3}. Since I_{D1}=I_{D3}=1mA,

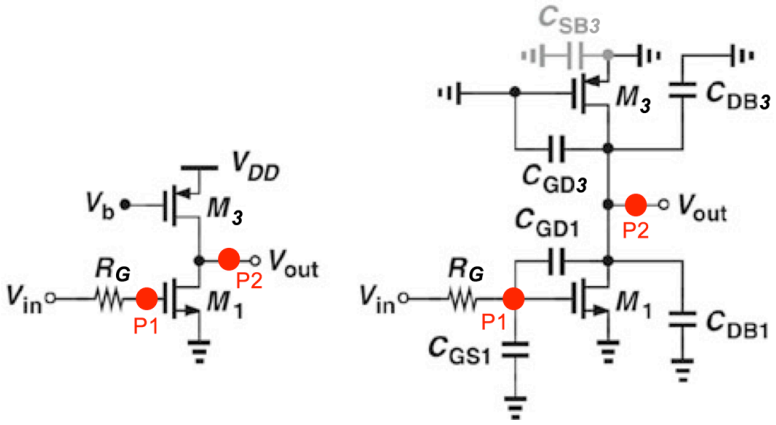
$$r_{O1} = \frac{1}{\lambda_N I_D} = \frac{1}{(1m)0.1} = 10k\Omega,\ r_{O3} = \frac{1}{\lambda_P I_D} = \frac{1}{(1m)0.2} = 5k\Omega$$

Gm1=15/(10k||5k)=4.5mS, $g_{m1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}} \rightarrow \left(\frac{W}{L}\right)_1 = \frac{(g_{m1})^2}{2\mu_n C_{ox} I_{D1}} = \frac{(4.5mS)^2}{2(200\mu)1m} = 50.5$

Marking: ro1, ro3 [1 mark], gm1 [1 mark], W/L [1 mark]

[Mostly answered correctly]

2. (d)



Marking: half circuit [1 marks], identifying poles [1 mark], drawing parasitic capacitances [2 marks], removing redundant capacitances [1 mark].

[This question was answered well. Some answered failed to remove redundant capacitors (eg. CSB3). Also some answers incorrectly identified 3 poles (also node VB)].

2. (e)

$$FP1: f_{P1} = \frac{1}{2\pi R_G\left(C_{GS1} + C_{GD1}\left(1+|A_v|\right)\right)}$$

$$FP2: f_{P2} = \frac{1}{2\pi\left[C_{GD3} + C_{DB3} + C_{GD1}\left(1+1/|A_v|\right)\right](r_{O1} \parallel r_{O2})}$$

Where: $|A_v| = g_{m1}(r_{O1} \parallel r_{O3})$

Marking: fp1 [2 marks], fp2 [3 marks]

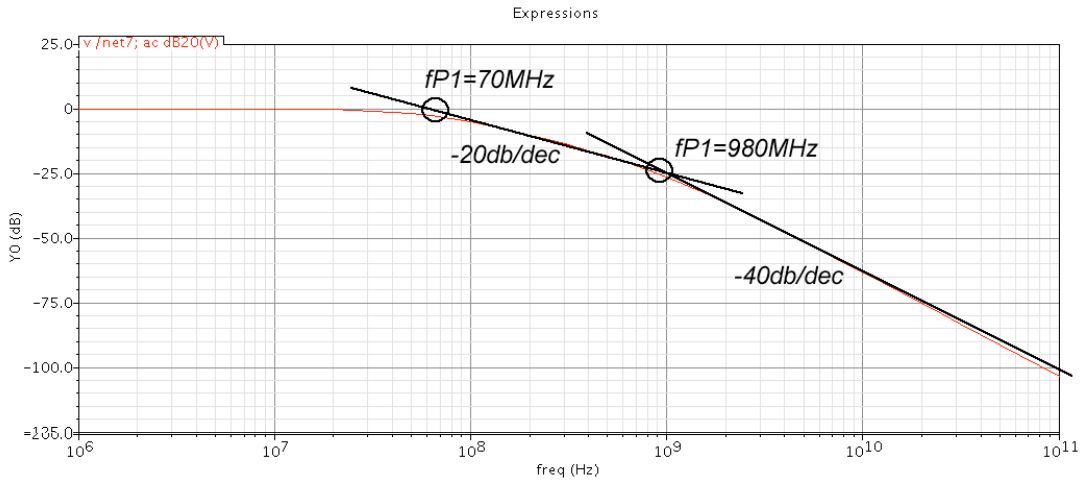
[Many answers here did not state FP1, FP2 expressions – but continued to evaluate capacitances].

2. (f)

$$FP1: f_{P1} = \frac{1}{2\pi(2k)\left(\frac{2}{3}(1)(101.25)12f + (101.25)0.2f(16)\right)} = 70.17MHz$$

$$FP2: f_{P2} = \frac{1}{2\pi\left[(135.6)0.2f + (101.25)0.2f(1+1/15)\right](5k \parallel 10k)} = 980.02MHz$$

[Many answers made some numerical error although method generally OK].



Marking: fP1 [2 marks], fp2 [2 marks], bode plot [3 marks]

[Many answers drew bode plot to have a bandpass res[onse (instead of 2nd order low pass)].

Question 3 – new theoretical application and bookwork

3. (a) $A_v(OL) = G = A_1 \times g_{m2} r_{O2}$, $K = 1$

Marking: breaking + terminating loop + redrawing [2 marks], K [1 mark], G [1 marks]

[Surprisingly many answers here confused K and G].

$$R_{out}(OL) = r_{O2} = \frac{1}{\lambda_P I_D} = \frac{1}{(100m)0.2} = 50\Omega$$

3. (b) $g_{m2} = \sqrt{2\mu_p C_{ox} \frac{W}{L} I_D} = \sqrt{2(100\mu)(100)100m} = 45mS$

$$G = A_1 \times g_{m2} r_{O2} = 10^{85/20} \times 45mS \times 50 = 40011$$

$$R_{out}(CL) = r_{O2} / (1 + KG) = 50 / (1 + 40011) = 1.25m\Omega$$

Marking: Rout(OL) [1 mark], gm [1 mark], G [1 mark], Rout(CL) [2 marks]

[Some answers here incorrectly tried to compute output impedance using Vout/Iout. Remember- It is important to exclude the load when calculating output impedance].

3. (c) Loop gain will reduce with BW, so need to ensure op-amp has sufficient GBP to have BW at the ripple frequency. From the plot of the ripple, it can be observed to be 50mV ptp at 200kHz (period=5us). Therefore, if the GBP=10MHz (for example), then open loop gain will fall to 50 at 200kHz. This will impact the output resistance (closed loop) as it is a function of loop gain.

Marking: fact that closed loop gain will drop with frequency [1 mark], GBP [1 mark], ripple frequency [1 mark], example [1 mark], mention specifications that are affected [1 mark].

[This answer was generally answered as giving a list of op-amp non-idealities instead of being specific to the circuit given in the question].

3. (d) Output impedance (at ripple frequency) is given by $1/2\pi R_{out} C_L$ where R_{out} is the closed loop output resistance (of the regulator), which is a function of frequency (as the loop gain drops with frequency). The value of C_L therefore defines the output pole but should also be selected to "smooth out" any residual output ripple that isn't rejected by the regulation circuit.

Simply using a large capacitance isn't effective as large capacitors (eg. electrolytics) typically have a large ESR (equivalent series resistance). The larger the capacitance typically so is the higher the ESR.

The value of CL should therefore be selected such that its impedance is much smaller than the output resistance of the regulator at the ripple frequency. i.e. Z(CL)<<Rout.

Assuming a GBP=10MHz, Loop gain=50*45mS*50ohm=112.5 and therefore Rout=0.4Ohms. If Rout=10xZ(CL) -> Z(CL)=0.04Ohms = 1/(2*pi*f*CL) = > CL>=8uF.

Marking: output impedance is function of frequency [1 mark], that CL should be used to smooth residual ripple [1 mark], mentioning ESR for larger capacitances [1 mark], identifying Z(CL)<<Rout and developing argument [3 marls]

[Most students incorrectly assumed that the output capacitance is used to completely smooth out the output ripple and did not appreciate that through the feedback, it was actually the op-amp that was rejecting this.]

3. (e) 3 main challenges are P=process variation, V=power supply voltage, T=temperature. (1) For power supply- reference mustn't be derived from power supply (eg. as a potential divider). There are circuits that can achieve this. (2) For process variation- it is generally preferred to design circuits such that an operating point, gain or output quantity is defined as the ratio of components rather than the absolute component value itself. (3) For temperature- describe basics of a bandgap reference- that two quantities are needed such that one has a positive temperature coefficient and the other a negative temperature coefficient.

Can describe bandgap fundamentals or power supply independent generator **(bookwork)**

Marking: PVT [3 marks], Reference generator circuit [3 marks].

[Correctly answered in general]

3. (f) Topology that is shown (LDO) has advantage that VDS can be very small (i.e. down to approximately 200mV) and therefore is called a low dropout regulator.

Topology proposed (with source follower output) on the other hand has a much smaller output resistance and hence does not need such a high loop gain – but suffers in that the output voltage has to be at least V_{DD}-V_{GS}.

Marking: LDO [2 marks], standard regulator [2 marks].

[Most answers compared output impedances of Common source and source follower, but failed to identify difference in VGS drop. Also many students answered mentioning body effect (although this is not relevant here)].

General feedback:

Generally, student answers to question 1 was too extensive (more description given than needed), and therefore had to rush questions 2 and 3 (where descriptions/analyses were too brief). In answering question 1 it is essential to mention the key points concisely as possible to answer the question. Some students used a full booklet for Q1 alone, whereas other students answering Q1 in just 2 pages achieved near full marks. Highest marks were achieved by students with concise and accurate answers. Q2 generally answered well with exception of calculating pole frequencies (most answers had some numerical error along the way). Q3 in general was answered too generally- i.e. without specific reference to the circuit given.