

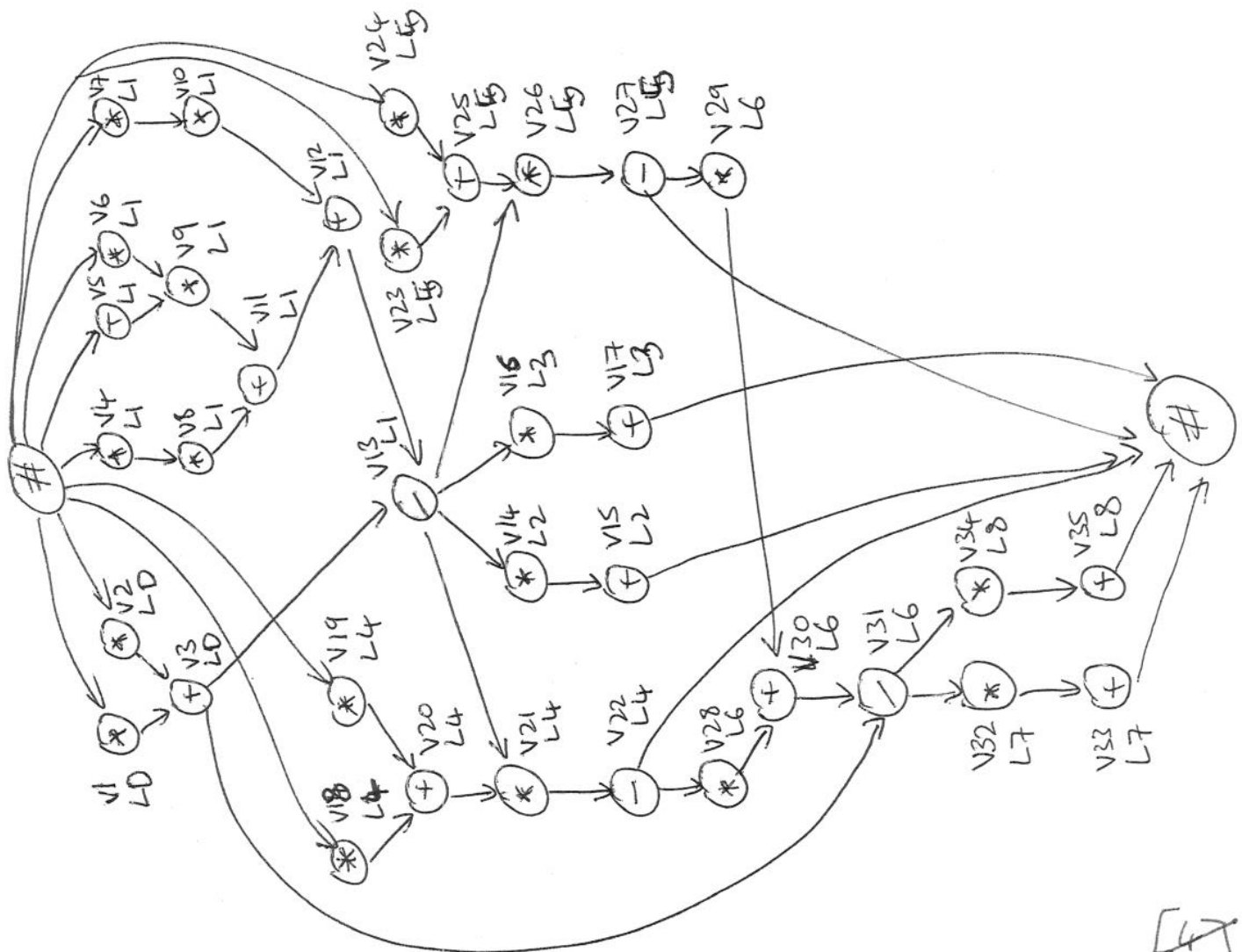
1a)

A01

1/8

## SYNTHESIS OF DIGITAL ARCHITECTURES

SOLUTIONS 2008

[4]  
[5]

# 1.b) Resource constrained list scheduling.

2/8

ALAP	Times	(for URGENCY)	- coded in reverse, i.e.
SOURCE 13			0 is high ALAP, greater # ⇒ more urgent.
-V1	10	-V19	9
-V2	10	-V20	8
-V3	9	-V21	7
-V4	12	-V22	6
-V5	12	-V23	9
-V6	12	-V24	9
-V7	11	-V25	8
-V8	11	-V26	7
-V9	11	-V27	6
-V10	10	-V28	5
-V11	10	-V29	5
-V12	9	-V30	4
-V13	8	-V31	3
-V14	2	-V32	2
-V15	1	-V33	1
-V16	2	-V34	2
-V17	1	-V35	1
-V18	9	-SINK	0

SCHEDULE	CANDIDATES	CHOSEN
Time 0 :	V1, V2, V4, V5, V6, V7, V18, V19, V23, V24	V4, V5, V6, V7, V1
1 :	V2, V18, V19, V23, V24 V8, V9, V10	V8, V9, V2, V10
2 :	V18, V19, V23, V24, V11, V3	V11, V3, V18, V19, V23, V24
3 :	V12, V20, V25	V12, V20, V25
4 :	V13	V13
5 :	V21, V14, V16, V26	V21, V14, V16, V26
6 :	V22, V15, V17, V27	V22, V15, V17, V27
7 :	V28, V29	V28, V29

1 b) [Continued]

3/8

		CAND.	CHOSEN
TIME	8:	v30	v30
	9:	v31	v31
	10:	v32, v34	v32, v34
	11:	v33, v35	v33, v35

[4]

[5]

c) Consider each node i.d. as the label for its output register. Then

TIME	REQ REQ'D	
0		
1	↑ v1	↓ v4 ↓ v5 ↓ v6 ↓ v7
2	↓	↑ v2 ↓ v8 ↓ v9 ↑ v10
3	↑	↓ v11 ↓ v18 ↓ v19 ↓ v23 ↓ v24
4		↑ v12 ↑ v20 ↑ v25
5		↓ v13 ↓ v21
6	↓ v3	↑ v14 ↓ v16 ↓ v21 ↓ v26
7		↑ v15 ↑ v17 ↑ v22 ↑ v27
8		↓ v28 ↓ v29
9		↑ v30
10		↓ v31
11	↑ <del>v32</del>	↓ v32 ↓ v34
12	↑ v33	↑ v35

1. c) [Continued]

4/8

$$\chi(G) = \kappa(G) = 7.$$

~~[4]~~ [5]

d)

Node	Binding	Node	Binding
$v_1$	$(*, 1)$	$v_{19}$	$(*, 2)$
$v_2$	$(*, 4)$	$v_{20}$	$(+, 2)$
$v_3$	$(+, 1)$	$v_{21}$	$(*, 1)$
$v_4$	$(*, 2)$	$v_{22}$	$(+, 1)$
$v_5$	$(+, 1)$	$v_{23}$	$(*, 3)$
$v_6$	$(*, 3)$	$v_{24}$	$(*, 4)$
$v_7$	$(*, 4)$	$v_{25}$	$(+, 3)$
$v_8$	$(*, 1)$	$v_{26}$	$(*, 4)$
$v_9$	$(*, 2)$	$v_{27}$	$(+, 4)$
$v_{10}$	$(*, 3)$	$v_{28}$	$(*, 1)$
$v_{11}$	$(+, 2)$	$v_{29}$	$(*, 2)$
$v_{12}$	$(+, 1)$	$v_{30}$	$(+, 1)$
$v_{13}$	$(/, 1)$	$v_{31}$	$(/, 1)$
$v_{14}$	$(*, 2)$	$v_{32}$	$(*, 1)$
$v_{15}$	$(+, 2)$	$v_{33}$	$(+, 1)$
$v_{16}$	$(*, 3)$	$v_{34}$	$(*, 2)$
$v_{17}$	$(+, 3)$	$v_{35}$	$(+, 2)$
$v_{18}$	$(*, 1)$		

4   \*  
 4   + / -  
 1   ÷

~~[4]~~  
 [5]

$$2. a) \quad \text{Min.:} \quad \sum_{t=\text{ASAP}_v}^{\text{ALAP}_v} t \cdot x_{vt}$$

6/9  
5/8

$$\text{s.t.} \quad \forall v \in V: \sum_{t=\text{ASAP}_v}^{\text{ALAP}_v} x_{vt} = 1$$

$$\forall (u,v) \in E: \sum_{t=\text{ASAP}_v}^{\text{ALAP}_v} t \cdot x_{vt} \geq \sum_{t=\text{ASAP}_u}^{\text{ALAP}_u} t \cdot x_{ut} + d_u$$

$$\forall r \in R, \forall t \in \{0, \dots, \lambda\}$$

$$\sum_{v \in V: T(v)=r} \sum_{t' \in \{t-d_v+1, \dots, t\} \cap \{\text{ASAP}_v, \dots, \text{ALAP}_v\}} x_{vt'} \leq a_r$$

$$\sum_{r \in R} c_r a_r \leq A$$

[10]

$$2. b) \quad \text{Min: } \sum_{t=ASAP_{v_2}}^{ALAP_{v_2}} \sum_{q=1}^4 t \cdot x_{v_2 t q}$$

7/9  
6/8

$$\text{s.t. } \forall v \in V \quad \sum_{t=ASAP_v}^{ALAP_v} \sum_{q=1}^4 x_{v t q} = 1$$

$$\forall (u, v) \in E \quad \sum_{t=ASAP_v}^{ALAP_v} \sum_{q=1}^4 t \cdot x_{v t q} \geq$$

$$\sum_{t=ASAP_u}^{ALAP_u} \sum_{q=1}^4 t \cdot x_{u t q} + d_u + \underbrace{\epsilon_{uv}}_{\text{communication latency variable}}$$

$$\forall v \in V \quad \forall q \quad \underbrace{y_{vq}}_{\text{placement variable}} = \sum_{t=ASAP_v}^{ALAP_v} x_{v t q}$$

$$\forall (u, v) \in E \quad \forall q \quad \epsilon_{uv} \geq y_{vq} - y_{uq} \quad \parallel \quad \text{Ensure } \epsilon_{uv} \geq 1 \text{ if in different quadrants.}$$

$$\forall r \in R, \forall t \in \{0, \dots, 1\}, \forall q$$

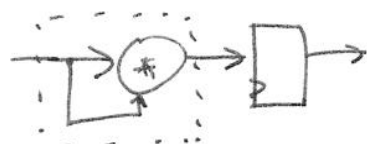
$$\sum_{v \in V: T(v)=r} \sum_{t' \in \{t-d_v^{-1}, \dots, t\} \cap \{ASAP_v, \dots, ALAP_v\}} x_{v t' q} \leq \underline{a_{rq}} \quad \leftarrow \text{per-quadrant basis.}$$

$$\forall q \quad \sum_{r \in R} c_r a_{rq} \leq A/4$$

[10]

3. a) Need to find an appropriate initial state for registers, e.g.

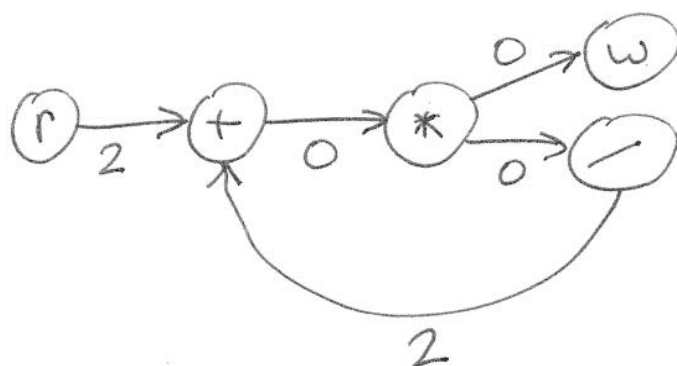
8/9  
7/8



If this register is initialised to  $-1$ , there is no corresponding initial state before the squarer (taking the dashed line as enclosing a "black box").

[2]

b)



[3]

c) Min:  $L + \alpha \sum_{v \in V} r_v \leftarrow \# \text{regs at o/p of node } v$

s.t.  $\forall (u,v) \in E$   
 ~~$\forall v \in V$~~   $r_v \geq w_r(v,u)$   
 ~~$\forall u \in V$~~

→ NEW CONSTRAINT.  
CAN RE-USE  
REGISTERS.

$\forall (u,v) \in E \quad S_v \geq S_u + d(u) + w_r(u,v)N$

$\forall v \in V \quad S_v + d(v) \leq L$

$\forall (u,v) \in E \quad w_r(u,v) = w(u,v) + r(v) - r(u) \geq 0$

$r(v) \in \mathbb{Z}$  for all  $v \in V$ .

As per  
note.

[10]

3 d) Code for (a):

```

while (true)
begin
  read x;
  y = x2 + z1;
  q = y * 3;
  z = 5/q1;
  write q;
  x2 = x1;
  x1 = x;
  z1 = z;
  q1 = q;
end

```

Code for (b):

```

while (true)
begin
  read x;
  y = x1
  z = 5/q1;
  y = x1 + z;
  q = y1 * 3;
  write q;
  q1 = q;
  x1 = x;
  y1 = y;
end

```

9/9  
8/8

For (a),  $N = 4$ . For (b),  $N = 3$ .

For (a),  $T_{\text{clk}} \geq 3$  (limited by divider)

For (b),  $T_{\text{clk}} \geq 4$  (divider - adder chain)

~~$\Rightarrow \alpha_2$~~  Further it is clear that  $\alpha_2 > \alpha_1$ .

~~Also  $3 + 4\alpha$~~

(5)