IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2014

EEE PART IV: MEng and ACGI

Corrected Copy

HVDC TECHNOLOGY AND CONTROL

Tuesday, 6 May 10:00 am

Time allowed: 3:00 hours

There are FIVE questions on this paper.

Answer FOUR questions.

All questions carry equal marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : B. Chaudhuri
Second Marker(s) : B.C. Pal

Answer any 4 questions out of 5

1. a) Explain why AC cables cannot be used for electric power transmission at high voltage levels and over long distances.

[5]

b) For a six-pulse line commutated converter (LCC), derive an expression for reduction in the average DC voltage due to commutation overlap. The expression should be in terms of no-load ideal voltage, firing angle (α) and extinction angle (δ). Assume commutation overlap angle $\mu < 60°$.

[5]

c) A family of *P-Q* capability curves (only the part for positive P is shown) for a typical VSC HVDC converter is shown in Fig. 1.1 for three different values (U = 1.1 pu, 1.0 pu and 0.9 pu) of AC system voltage U. Explain the following:

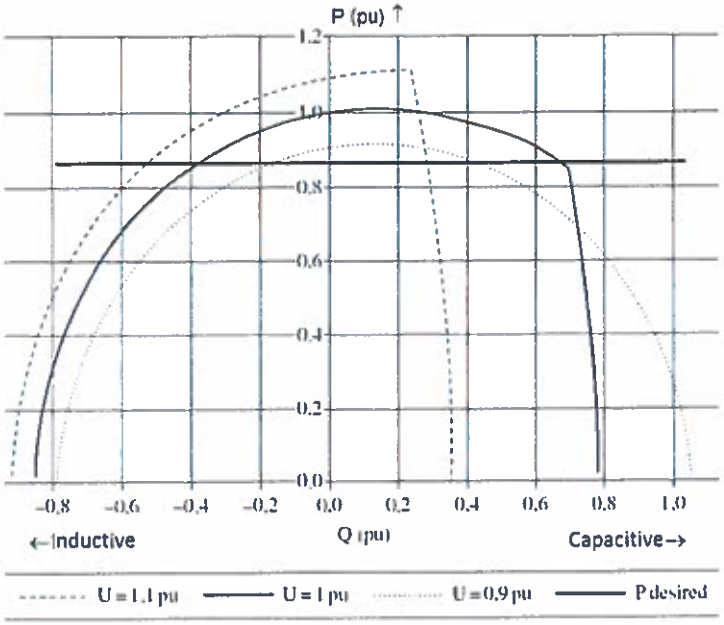

Figure 1.1: P-Q capability curves of a VSC

i) Why does reactive power generation capacity increase with decreasing AC system voltage?

[3]

ii) Why does MVA capacity reduce with AC system voltage?

[2]

d) Explain the implications of selecting a low or high droop constant (β_j) in the power-voltage droop control (shown in Fig. 1.2) used in converters to achieve autonomous power sharing within a DC grid.

[5]

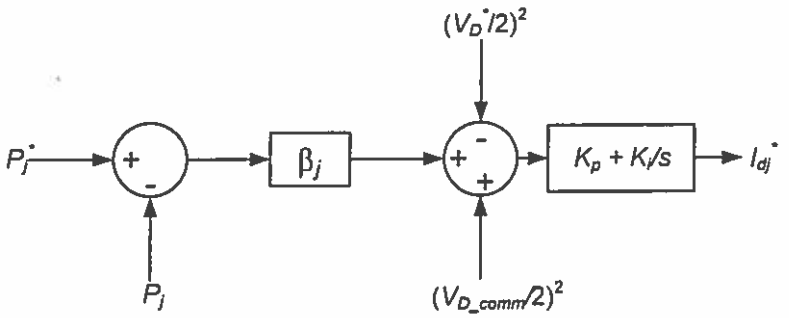

Figure 1.2: Power-voltage droop control for DC grid converters

2. a) What are the consequences of interrupting the firing pulses to the thyristors without bypassing the converter bridge while attempting to block a LCC HVDC converter.

[4]

b) Describe the typical steps involved in ramping up the power level of an LCC HVDC link up to the rated condition starting from a completely de-energised state.

[5]

c) Justify the range of acceptable values of firing angle (α) at the rectifier and extinction advance angle (γ) at the inverter end of an LCC HVDC link under normal operation.

[4]

d) The rectifier station of a bipole LCC HVDC link is connected to a 400 kV (line-to-line) 3-phase AC system through 400/200 kV transformers. Two 6-pulse converters are connected in series on the DC side. Under normal operation, each converter operates with a firing angle α=16° and overlap angle μ=22° which causes 1.8 kA current to flow through the DC line.

i) Calculate the commutating resistance (R_c).

[4]

ii) Determine the reactive power consumed by each converter.

[3]

3. a) A point-to-point LCC HVDC link is embedded within an interconnected AC system. Describe using a block diagram how power flow analysis is carried out for such an AC/DC system. There is no need to use any equation.

[5]

b) State the main advantage and disadvantage of equidistant pulse control (EPC) approach over individual phase control (IPC) in the context of firing angle control of LCC HVDC systems.

[4]

c) For a point-to-point LCC HVDC link, explain why the rectifier side is usually set up to control the current while the inverter side controls the voltage under normal operation.

[4]

d) A monopolar LCC HVDC link is operating with a rectifier terminal voltage V_{dr} = 500 kV and rated current I_d = 2.0 kA flowing through the DC line. The following information is available:

Minimum limit for firing angle $\alpha_{min} = 4°$,
Minimum limit for extinction advance angle $\gamma_{min} = 10°$,
Resistance of DC line $R_{line} = 2.0\ \Omega$,
Firing angle $\alpha = 18°$,
Extinction advance angle $\gamma = 18°$,
Margin current $I_m = 180$ A

The commutating resistance for both rectifier and inverter is $R_c = 3.0\ \Omega$. Due to a remote short circuit in the rectifier side AC system, the AC voltage at the rectifier end drops by 20%. Calculate the percentage increase in reactive power drawn by the inverter from pre-fault condition. Assume no change in inverter side AC voltage as a result of the above fault.

[7]

4. a) Explain how a proactive hybrid DC circuit breaker is able to interrupt DC fault currents very fast while ensuring minimal power losses under normal operation.

[4]

b) What are the main considerations towards designing the compensator *H(s)* used within a phase-locked loop (PLL), shown in Fig. 4.1, which is used for tracking the reference angle $\theta_s(t)$.

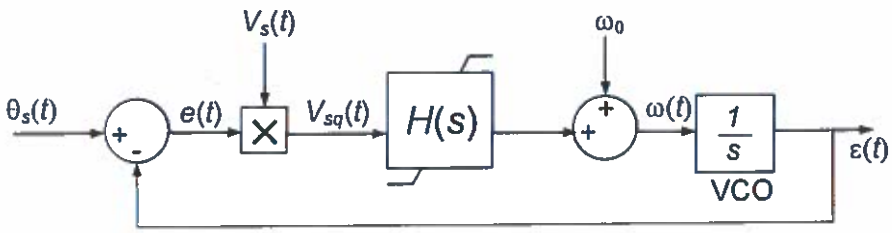

Figure 4.1: Block diagram of a phase-locked loop (PLL)

[4]

c) Justify the use of inner-loop current control instead of voltage control for VSC HVDC systems.

[4]

d) Why VSC HVDC is the preferred option for connecting remote offshore wind farms to the onshore grid?

[4]

e) A remote offshore wind farm is connected to the onshore grid through a point-to-point VSC HVDC link. Which variables are likely to be controlled by the outer loop control of the offshore and onshore converters and why?

[4]

5. a) Explain the difference between a half-bridge and full-bridge modular multi-level converter (MMC) in terms of the following:

i) DC fault current interruption capability and

[3]

ii) Power losses

[3]

b) Mention three main challenges towards protecting a VSC HVDC system.

[3]

c) Explain why VSC is preferred over LCC for sub-sea HVDC cables.

[4]

d) The current control loop of an active and reactive power controller is to be designed for one end of a 2-level VSC HVDC converter. The DC side is interfaced to the AC system through a phase reactor having resistance R_c = 0.75 mΩ and inductance L_c = 100 μH. The VSC uses PWM with 3.4 kHz switching frequency. Assume ideal phase-locked loop (PLL) and use of appropriate feed-forward resulting in two decoupled control loops. The objective is to make the VSC follow a given active and reactive power reference command. Calculate the proportional and integral gains (K_p, K_i) required for the PI compensators in the current control loop to achieve fastest possible reference tracking performance. Ensure that the closed-loop bandwidth is limited to one-tenth of the switching frequency. Neglect the on-state resistance of IGBTs and diodes.

[7]