E3.11
E4.42
AO8

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2003

MSc and EEE PART III/IV: M.Eng., B.Eng. and ACGI

**ADVANCED ELECTRONIC DEVICES**

Thursday, 8 May 10:00 am

Time allowed: 3:00 hours

**There are FIVE questions on this paper.**

**Answer THREE questions.**

**Corrected Copy**

**Any special instructions for invigilators and information for candidates are on page 1.**

Examiners responsible First Marker(s) : K. Fobelets
Second Marker(s) : A.S. Holmes

**Special Information for Invigilators: none**

**Information for Candidates:**

**Constants:**

| Quantity | Symbol | Value |
|---|---|---|
| Boltzman constant | k | $1.38066\ 10^{-23}$ J/K |
| Elementary charge | q | $1.60218\ 10^{-19}$ C |
| Electron rest mass | $m_0$ | $0.91095\ 10^{-30}$ kg |
| Electron volt | eV | $1eV = 1.60218\ 10^{-19}$ J |
| Permeability in vacuum | $\mu_0$ | $1.25663\ 10^{-8}$ H/cm |
| Permittivity in vacuum | $\varepsilon_0$ | $8.85418\ 10^{-14}$ F/cm |
| Planck constant | h | $6.62617\ 10^{-34}$ Js |
| Reduced Planck constant | $\hbar$ | $1.05458\ 10^{-34}$ Js |
| Thermal voltage (300K) | kT/q | 0.0256 V |
| Speed of light in vacuum | c | $2.99792\ 10^{10}$ cm/s |

1. Consider Figure 1.1, where a processed device is shown.

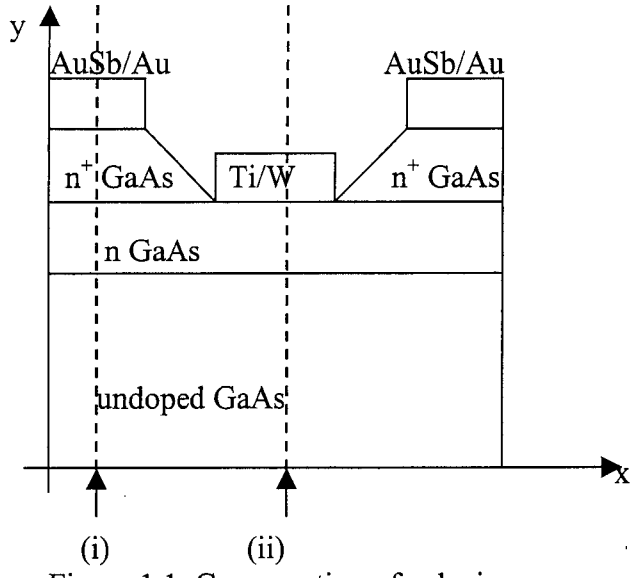


Figure 1.1: Cross section of a device.

a) Give the name of the device presented in Figure 1.1. [2]

b) In which layer does the conduction occur? [2]

c) Why is the middle contact defined in a recess? [3]

d) Sketch the energy band diagrams in the y-direction from contact to bulk at points (i) and (ii) at equilibrium when no bias voltages are applied. Give the type of the contact in each case. [5]

e) Determine the minimum thickness ($a_{min}$) of the conducting layer for depletion mode operation at room temperature. The parameters of the device are: [8]

$N^+_D = 5\ 10^{18}$ cm$^{-3}$ (donor concentration in the n$^+$-GaAs layer)
$N_D = 10^{17}$ cm$^{-3}$ (donor concentration in the n-GaAs layer)
$N_C = 4.7\ 10^{17}$ cm$^{-3}$ (effective density of states in GaAs)
$\Phi_m$=4.57 V (metal workfunction of AuSb/Au contacts)
$\Phi_m$=3.57 V (metal workfunction of Ti/W contact)
$\chi_{GaAs}$=3.05 V (electron affinity of n-GaAs)
$\varepsilon_r = 10$ (relative permittivity of GaAs)
$w_{depl} = [2\ q\ V_{po}/(e\ N_D)]^{1/2}$ (depletion width for a one-sided junction, $V_{po}$: channel pinch-off voltage)

2. Consider Figure 2.1, which shows a biased Si MOSFET with $V_{GS}>V_{th}$ and $V_{DS}=V_{GS}-V_{th}$.

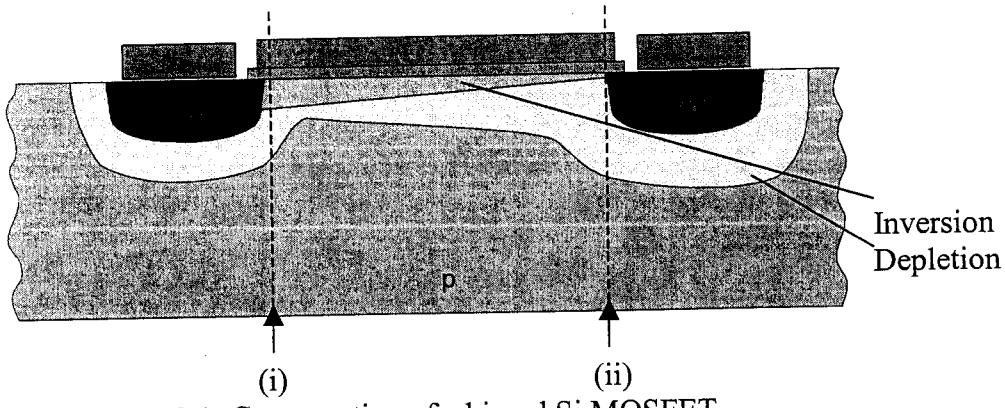


Figure 2.1: Cross section of a biased Si MOSFET.

a) How is the gate oxide fabricated in a Si MOSFET? [2]

b) Why are the areas under the source and drain contact highly doped? [2]

c) Sketch the energy band diagram from gate through the channel to the substrate at points (i) and (ii). Make sure the relative dimensions are correct and indicate regions of accumulation, depletion and inversion in the band diagram. [5]

d) In a MOSFET with a gate length $l_g=0.12\mu m$, the electric field $E_{sat}$ at which the drift velocity saturates, is smaller than the electric field at pinch-off $E_{po}=(V_{GS}-V_{th})/l_g$. Describe briefly what happens in the device at saturation and how this influences the current-voltage characteristics. [5]

e) Calculate the extrinsic transconductance of a long gate length MOSFET at $V_{GS}=2V$ and $V_{DS}=2V$. The MOSFET parameters are: [6]

$V_{th}=1V$ (threshold voltage)
$L=2\mu m$ (gate length)
$t_{ox}=10nm$ (oxide thickness)
$W=50\mu m$ (gate width)
$\mu_n=500\ cm^2/Vs$ (electron mobility)
$R_s= R_d=100\Omega$ (source and drain resistance)
$R_g=1\Omega$ (gate resistance)
$\varepsilon_{ox} = 4$ (relative permittivity of $SiO_2$)
$I_{DS} = (\mu\ W\ C_{ox}/L)\ ((V_{GS}-V_{th})\ V_{DS} - V_{DS}^2/2)$

3.

a) What is the advantage of fabricating SOI using oxygen implantation (SIMOX) compared to the bonded-etch-back fabrication method? [2]

b) Sketch a simplified schematic cross-section of a Si-CMOS structure for each of the following configurations: [4]

(i) p-type substrate (bulk)
(ii) fully depleted SOI

c) Explain briefly, using sketches of the regions of interest, why the parasitic capacitances are reduced in the SOI configuration compared to the bulk approach. [4]

d) Why is the off-current in a fully depleted SOI MOSFET lower than in a bulk MOSFET? [2]

e) In Figure 3.1, a 3-D sketch of a planar finFET is shown.

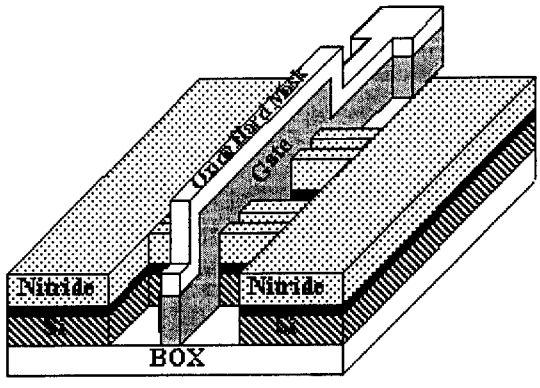


Figure 3.1: A 3-D view of a planar finFET

(i) How many conducting channels does this finFET have? [2]

(ii) Sketch a cross-section through one of the fins and indicate the gate length. [4]

(iii) Explain briefly why the fin width is important. [2]

4.

a) What is the advantage of introducing a composition gradient in the base layer of an HBT? [3]

b) Why is the gain in an npn HBT larger than in a npn BJT for the same dimensions and doping concentrations? [3]

c) Sketch an idealized energy band diagram for a $p^+np$ HBT with no bias applied. [4]

d) What is the effect of the base spreading resistance on the emitter current in a planar bipolar transistor? [3]

e) Determine the base doping $N_{AB}$ and base spreading resistance $r_{bb'}$ of an AlGaAs/GaAs HBT when the following parameters are given: [7]

$\beta_{HBT} = 500$ (current gain of the HBT)
$\exp[\Delta E_g/kT] = 10$ (assume the valence band offset equal to $\Delta E_g$)
$\mu_e/\mu_h = 2$ and $\mu_e = 500 cm^2/Vs$ (electron and hole mobilities)
$l_e = 1\mu m$ (emitter length)
$t_e = 100\mu m$ (emitter width)
$d_{EB} = 2\mu m$ (emitter-base distance)
$N_{DE} = 10^{18}\ cm^{-3}$ (emitter doping)
$C_{diffEB} = 8\ 10^{-12}$ F @ $I_e$=10mA (diffusion capacitance of the forward biased emitter-base junction)
$C_{diffEB} = 4\ 10^{-12}$ F @ $I_e$=5mA
$\beta_{BJT} = \mu_e L_E N_{DE}/(\mu_h W_B N_{AB})$
$\sigma = e\ n\ \mu_e + e\ p\ \mu_h$ (total conductivity)

5.

a) Why is there a strong interest in sub-threshold operation of FETs? [2]

b) Why is the current $I_{DS}$ below the threshold voltage $V_{th}$ non-zero? [2]

c) What do you understand by sub-threshold voltage swing? [2]

d) Why does a Si MOSFET on SOI have a better sub-threshold performance than a bulk MOSFET? [2]

e) What might be the advantage of Si:SiGe MODFETs for sub-threshold operation and why? [2]

f) What is a DTMOS (dynamic threshold MOSFET)? To explain, give an answer to the next two points:

   (i) Sketch a schematic cross-section with biasing of the DTMOS on SOI. What is unusual in this configuration. [3]

   (ii) Why is the DT configuration of the FET good for sub-threshold operation? [3]

g) Sketch the graph $\log(I_{DS})$ versus $V_{GS}$, for one value of $V_{DS}$, for gate voltages well below and well above the threshold voltage $V_{th}$ and indicate the region of weak inversion, i.e. the sub-threshold region. [4]