

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2006

MSc and EEE PART III/IV: MEng, BEng.and ACGI

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Tuesday, 9 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s) :	C. Toumazou
	Second Marker(s) :	D.G. Haigh

1. (a) Figures 1(a) and 1(b) show two popular biasing schemes typically used in analogue integrated systems. Briefly outline the main feature of each of these circuits.

[3]

For the bandgap voltage reference circuit of Figure 1(a), show that $\delta V_0 / \delta T = 0$ (where T is temperature) if $(R_2/R_3) \ln [I_1/I_2] = 29$ for $V_0 = 1.283$ V. Assume the temperature coefficient of V_{BE} to be $-2.5\text{mV}/^\circ\text{C}$, the collector current of transistor Q_3 is $100\mu\text{A}$ and the device saturation current is $I_S = 1.2 \times 10^{-13}\text{A}$. Boltzmann's constant $k = 1.38 \times 10^{-23}\text{J/K}$ and the electron charge is $q = 1.6 \times 10^{-19}\text{C}$.

[6]

- (b) Calculate the fractional temperature coefficient in $\text{ppm}/^\circ\text{C}$ for the current generator of Figure 1(b) at room temperature, given that R is a polysilicon resistor with a temperature coefficient of $1500\text{ppm}/^\circ\text{C}$.

[3]

- (c) Show that the circuit of Figure 1(b) can be developed into a current source with output current directly proportional to absolute temperature and virtually independent of supply voltage. It is likely that on power-up the output current will fall into a zero current state. Sketch a suitable start-up circuit that ensures that this condition will not occur and explain the operation of the circuit.

[8]

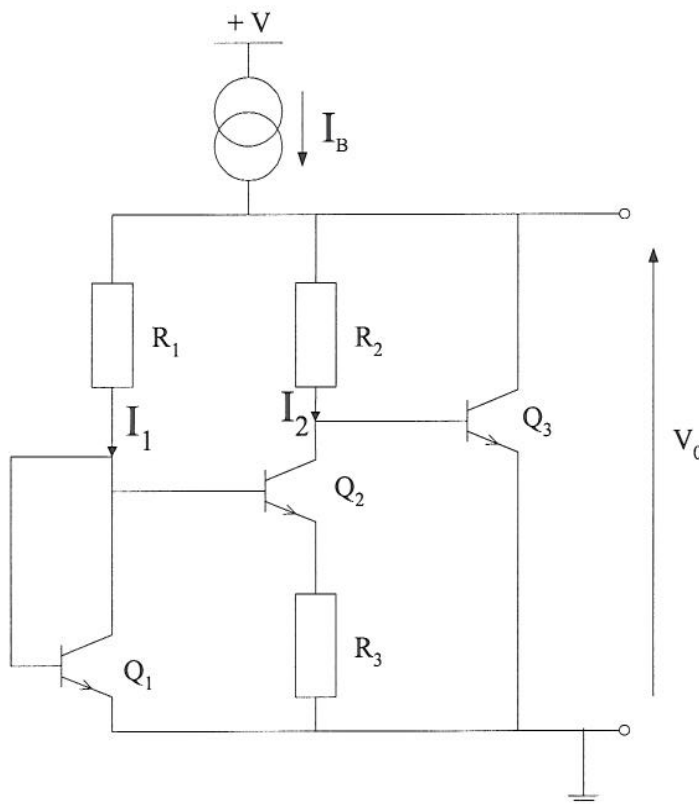


Figure 1(a)

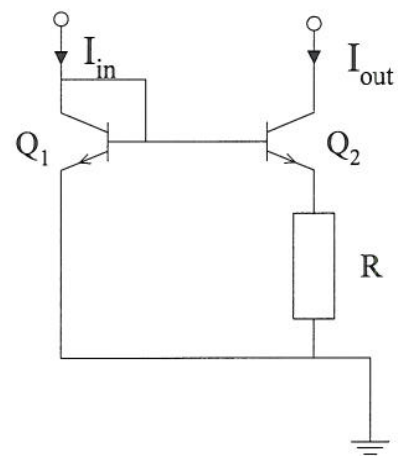


Figure 1(b)

2. Figure 2 shows the basic design of two analogue sampled-data precision integrators. Figure 2(a) is a switched-capacitor integrator and Figure 2(b) a switched-current integrator.

- (a) Derive an expression for the transfer function of both integrators. Assume that the integrators are driven by non-overlapping clocks and that the switches are ideal.

[10]

- (b) (i) Sketch the basic design of a 3rd-order Chebyshev low pass switched-capacitor ladder filter.
- (ii) Explain the function of all components in the circuit. The filter is to have a cut-off frequency of 5kHz. Assume a clocking frequency of 100 kHz. The values of integration capacitive for the capacitor based sections are 5.06pF, inductive and the section is 3.49pF. All other switched capacitors are 1pF.
- (iii) From the circuit, estimate normalised passive component values for the original double-terminated LC prototype of the filter. All values should be normalised to 1 rad/s. You may assume that the clocking frequency is so high that the integrators can be assumed lossless.

[10]

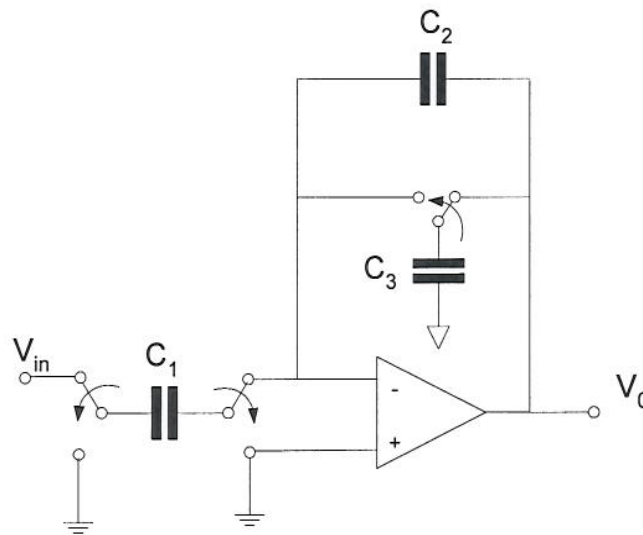


Figure 2(a)

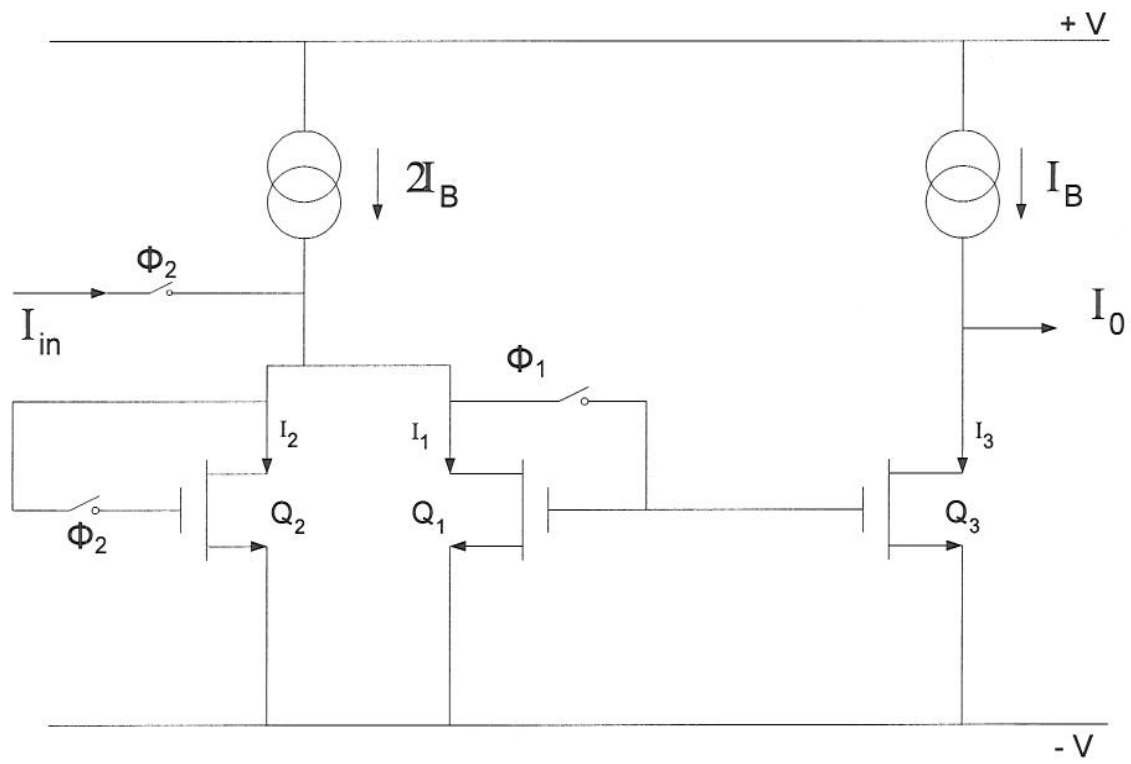


Figure 2(b)

3. (a) In mixed-mode ASIC design, the process technology is chosen to optimise digital performance specifications. Give one example of the constraints this places upon analogue circuit design performance.

[2]

- (b) A fundamental limitation imposed on the Dynamic Range (DR) of any high performance A/D converter will ultimately be switch noise. Prove that the fundamental limit is given by,

$$DR = \frac{V_{ref}}{\sqrt{(10kTRf_c)}}$$

where V_{ref} is the reference voltage, k is the Boltzmann's constant, T is absolute temperature, R is switch resistance and f_c is the clock frequency of the switch. You may assume that the system settles in 10τ (where τ is the time constant), over one period of the clock frequency.

[6]

- (c) A very high resolution analogue-to-digital converter is the oversampling converter sometimes referred to as the sigma-delta modulator. Sketch a typical architecture for such a converter and explain its principles of operation, in particular the feedback noise shaping mechanism.

[12]

4. (a) Under what operating conditions does the MOSFET of Figure 4(a) realise a linear floating resistor between terminals A and B? Show that under these conditions the equivalent resistance R_{AB} can be approximated by

$$R_{AB} = \frac{L}{KW(V_{GS} - V_T)}$$

stating any assumptions. All symbols have their usual meaning.

[5]

- (b) Discuss three sources of non-linearity in the single MOSFET resistor realisation of Figure 4(a) and suggest one suitable circuit design to help eliminate one or more of these non-linear terms showing the necessary circuit analysis to confirm your design.

[5]

- (c) For the current mirror of Figure 4(b), derive the expression for minimum output voltage while still maintaining saturated devices. Derive this voltage in terms of device threshold voltage V_T clearly stating any assumptions you make.

[4]

- (d) Sketch a regulated cascode current-source and explain why the output resistance of the current source is higher than a standard cascode mirror.

[6]

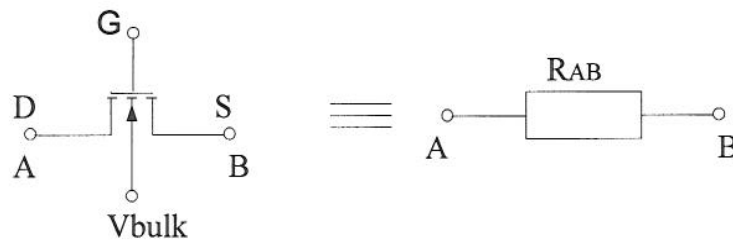


Figure 4(a)

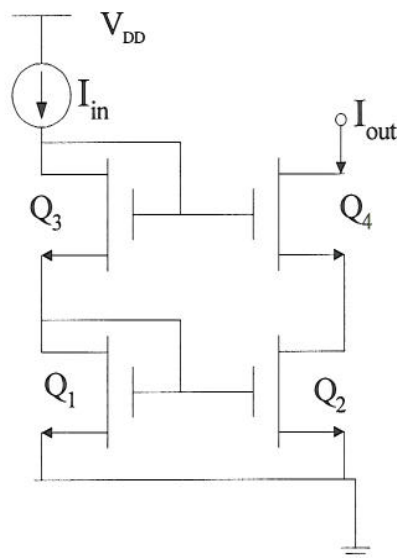


Figure 4(b)

5. Figure 5 shows a partially-designed two-stage CMOS op-amp required to give a voltage gain of approximately 80 dB, a slew-rate of $5 \text{ V}/\mu\text{s}$ and a gain-bandwidth product of 3 MHz.

- (a) Given that the technology is a fixed $5 \mu\text{m}$ double metal CMOS process, design the channel widths of transistors Q1, Q2 and Q6 for the op-amp to meet the above performance specifications. Aspect ratios of all other devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below.

[15]

- (b) Give a reason why the introduction of a single integrated resistor in series with the compensation capacitor should significantly improve the amplifier's phase margin.

[5]

CMOS TRANSISTOR MODEL PARAMETERS

MODEL PARAMETERS	$K_p (\mu\text{A}/\text{V}^2)$	$\lambda (\text{V}^{-1})$	$V_{T0} (\text{V})$
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

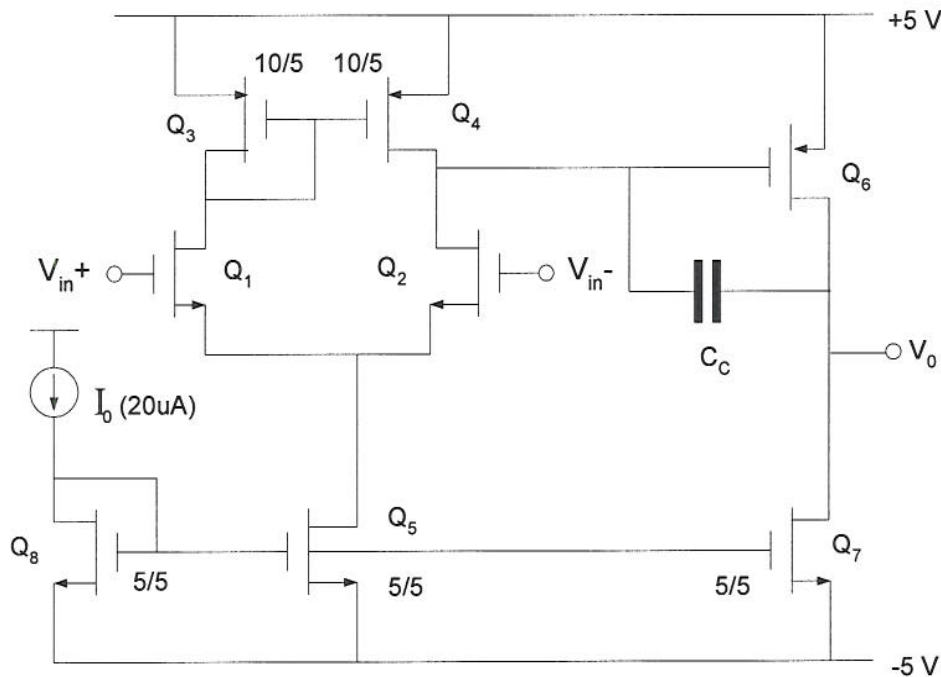


Figure 5

6. (a) Give two advantages of current-mode analogue signal processing compared to traditional voltage-mode processing.

[2]

- (b) With the aid of a suitable macromodel, explain the theoretical concept of current feedback and how it results in constant bandwidth amplification. Using a current-feedback op-amp, design a closed-loop non-inverting gain stage with a bandwidth of 10 MHz for a fixed voltage gain of 100. Assume an internal compensation capacitance of 4pF and that the open-loop transresistance gain of the amplifier is very much larger than the amplifier feedback resistor.

[13]

- (c) The circuit shown in Figure 6 is a single bit cell of a current-mode algorithmic analogue to digital converter. Briefly describe the operation of the cell and give reasons why this converter is particularly suitable for mixed analogue and digital VLSI.

[5]

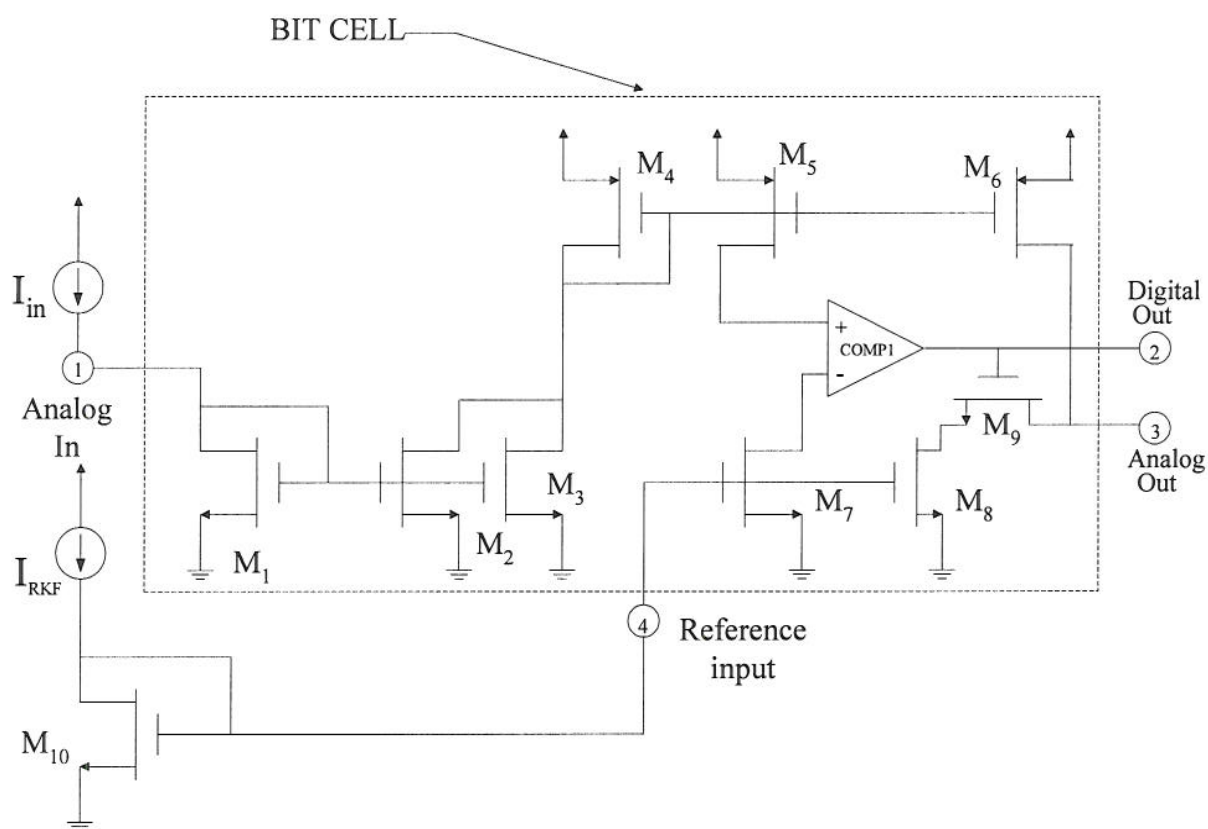


Figure 6

2006 EXAM

original.

3rd Analogue Integrated Circuits
and Systems

EJ.01/

ACI

SOLUTIONS

1st MARKER

C. Toumazou

2nd MARKER

D. Haigh

Q1/ Bandgap voltage reference circuit has almost zero temperature coefficient. Used mainly as stable voltage reference in ICs.

PTAT (Proportional to absolute temperature) current generator. Output current usually proportional to power supply voltage. Used as a biasing circuit in most precision ICs.

For BG reference :- $V_{BE1} = V_{BE2} + I_2 R_3$ ($\beta \gg 1$)

Since $V_{BE1} - V_{BE2} = V_T \ln(I_1/I_2)$

Then $V_0 = V_{BE3} + (R_2/R_3) V_T \ln(I_1/I_2)$
 \uparrow
 $V_T \ln(I_3/I_5) \rightarrow$ assume room temp.

For $dV_0/dT = 0$, then $dV_{BE3}/dT = \frac{V_T R_2}{T R_3} \ln \frac{I_1}{I_2}$

Since $\frac{dV_{BE}}{dT} = -2.5 \text{ mV}/^\circ\text{C}$, $\frac{V_T}{T} = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}}$

Then $\left(\frac{R_2}{R_3}\right) \ln\left(\frac{I_1}{I_2}\right) = 29$ and so

$$V_0 = 1.283 \text{ V}$$

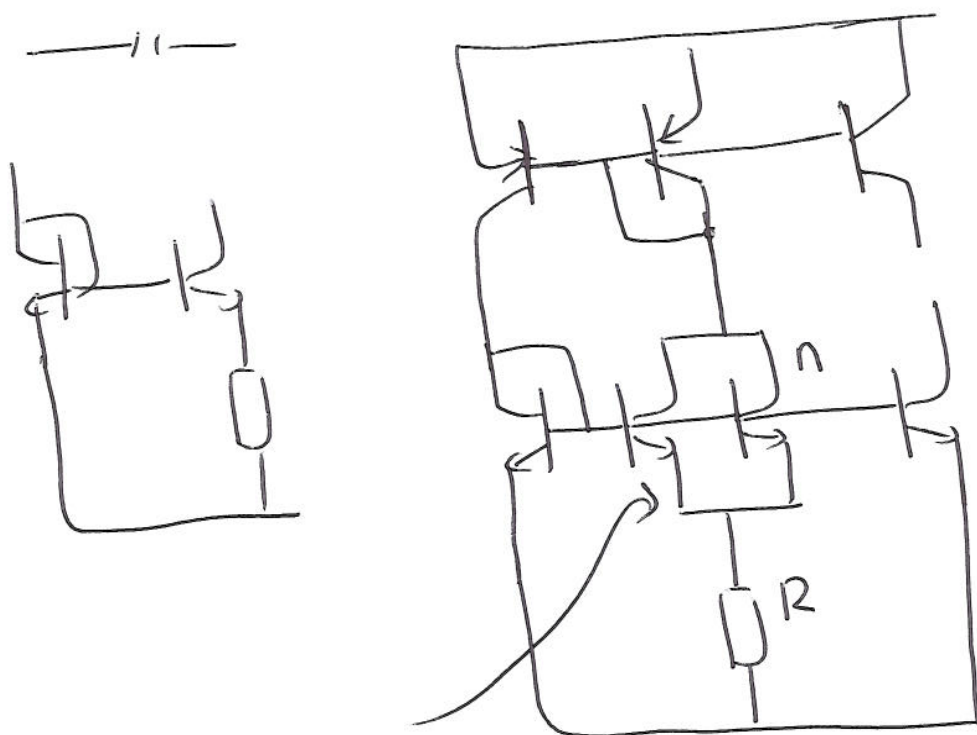
For PTAT temperature coefficient
 V_T cancels with negative temperature
 coefficient of resistor

$$\therefore T_{CF} = \frac{1}{V_T} \frac{\partial V_T}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T}$$

$$= \frac{1}{T} - 1500 \times 10^{-6} \text{ @ } T_{room} = 1833$$

ppm/°C

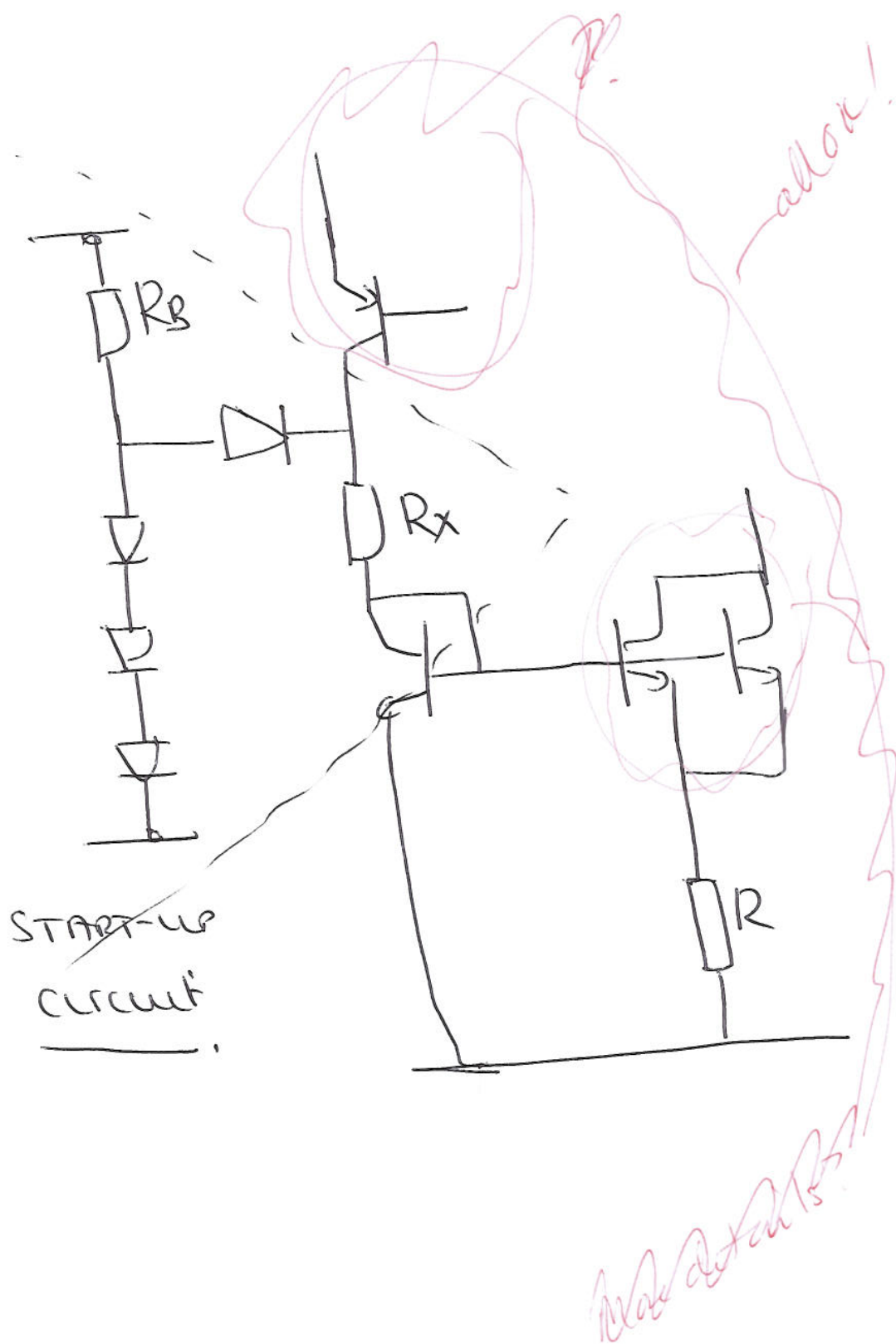
3



n-emitter
 self biasing scheme
 requires start-up

$$I_0 = V_T \ln [n/R]$$

4



4

OK!

HAHA

GT

Q2/

Fig 2a lossy Integrator

During ϕ_1 of switch, $I_{aw} = C_1 V_{in} / T$

$$\phi_2 \quad - C_1 V_{in} / T = V_o [j\omega C_2] + \frac{C_3 V_o}{T}$$

Transfer of charge

recovery yields

$$V_o / V_{in} = -C_1 / C_3 \left[\frac{1}{1 + j\omega \frac{C_2}{C_3} T} \right]$$

$$= -\frac{C_1}{C_3} \frac{1}{(1 + j\omega / f_p)}$$

$$f_p = \frac{1}{2\pi \frac{C_2}{C_3}} f_c.$$

5

Fig 2b - Switched current, ideal integrator

During ϕ_2 of period $(n-1)$, Q_2 samples
 Q_1 holds

$$I_2(n-1) = I_B + I_{in}(n-1) + I_o(n-1)$$

During ϕ_1 of period n , Q_1 samples, Q_2 holds

$$I_1(n) = 2I_B - I_2(n-1) = I_B - I_{in}(n-1) - I_o(n-1)$$

$$\Rightarrow I_o(n) = I_{in}(n-1) + I_o(n-1)$$

In Z domain

$$\log(z) [1 - z^{-1}] = \log(z) z^{-1}$$

$$H(z) = \left(\log / \log \right)_z = \frac{z^{-1}}{(1 - z^{-1})}$$

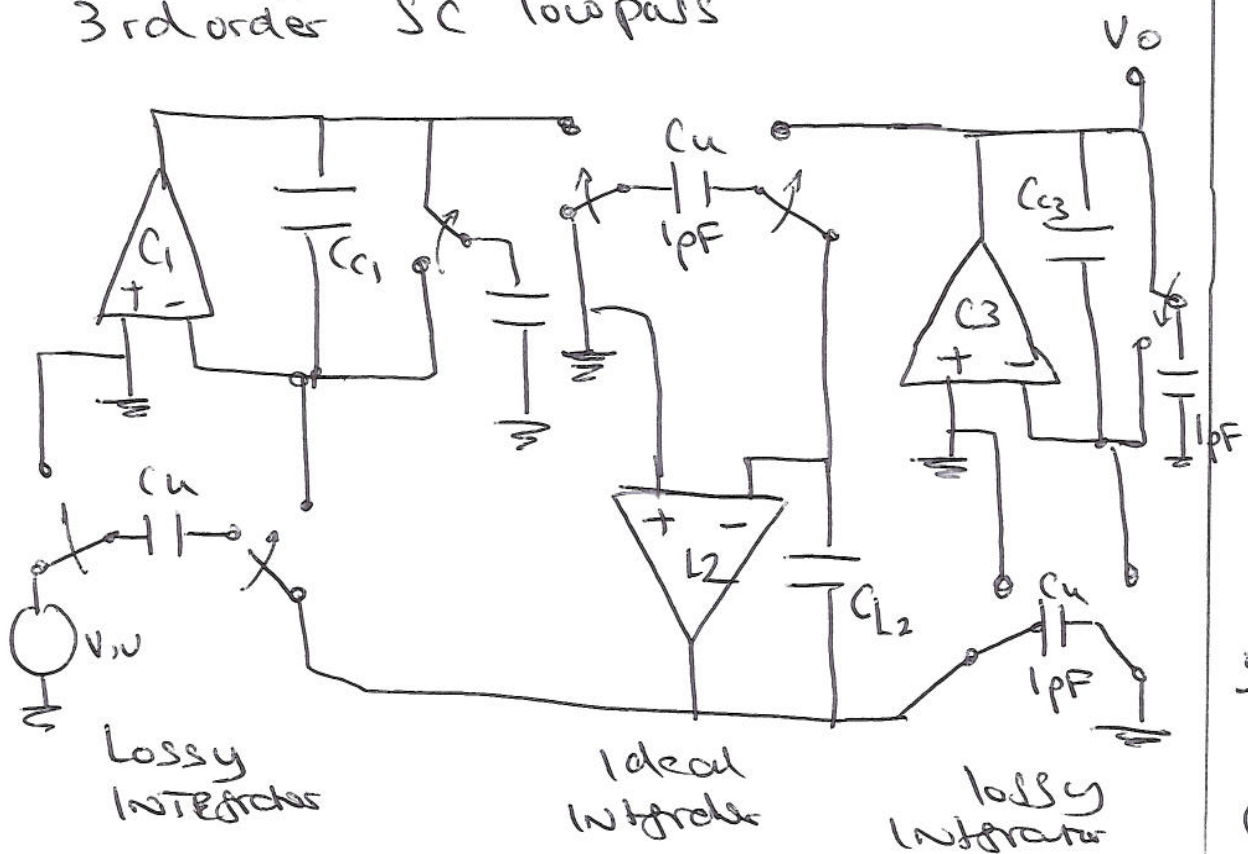
$$= \frac{1}{z - 1}$$

Since $z = e^{j\omega T} \approx (1 + j\omega T)$ for $\omega T \ll 1$

$\therefore H(z) = \frac{1}{j\omega T}$ lossless integrator.

5

c) 3rd order SC lowpass



General transformation rules

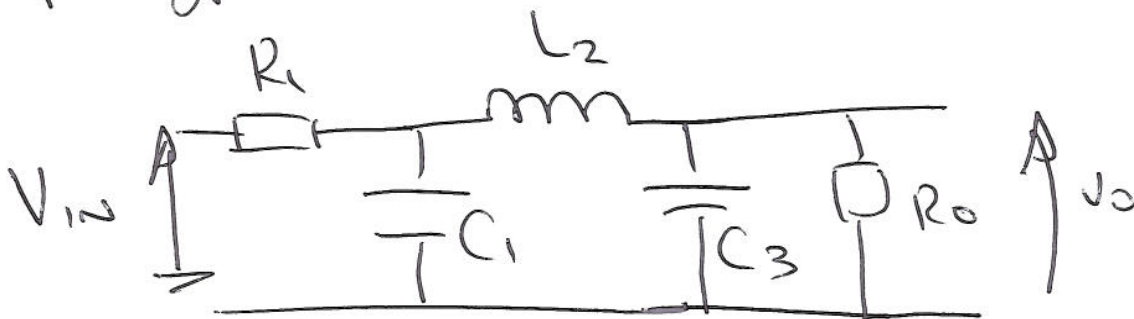
$$\frac{f_c L_2}{R_s} = \frac{C_{L2}}{C_u}, \quad C_{C3}/C_u = f_c R_s C_3$$

\uparrow
inductors

\uparrow
capacitors

R_s (dummy scaling resistor)

Problemo



From Sc equivalent

$$C_1 = C_3 = 5.08 \text{ pF}, \quad L_2 = 3.49 \text{ pF}$$

$$C_u = 1 \text{ pF}$$

$$\text{Assume } R_s = R_1' = R_o = 1 \Omega$$

$$\therefore L_2 = C_{L2}/f_c = 3.49 \times 10^{-5}$$

$$\text{normalized} (\times 2\pi f_0) = \underline{\underline{1.096}}$$

$$C_1 = C_3 = C_{C3}/f_c = 5.08/100 \times 10^3 = 5.08 \times 10^{-5}$$

$$\text{normalized} \times 2\pi f_0 = \underline{\underline{1.596}}$$

5

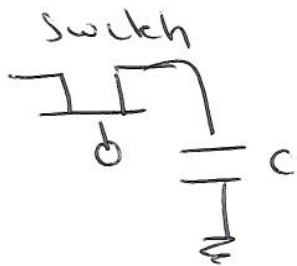
6

Q3/ Constraints

- a) 1/ low voltage - low dynamic Range
 2/ Non-Linear process technology - Distortion.

2

b) Dynamic Range $\Delta V_{ref}/noise = 2^N$



Rms noise of switch
 driving capacitor
 $= \sqrt{\frac{kT}{C}}$

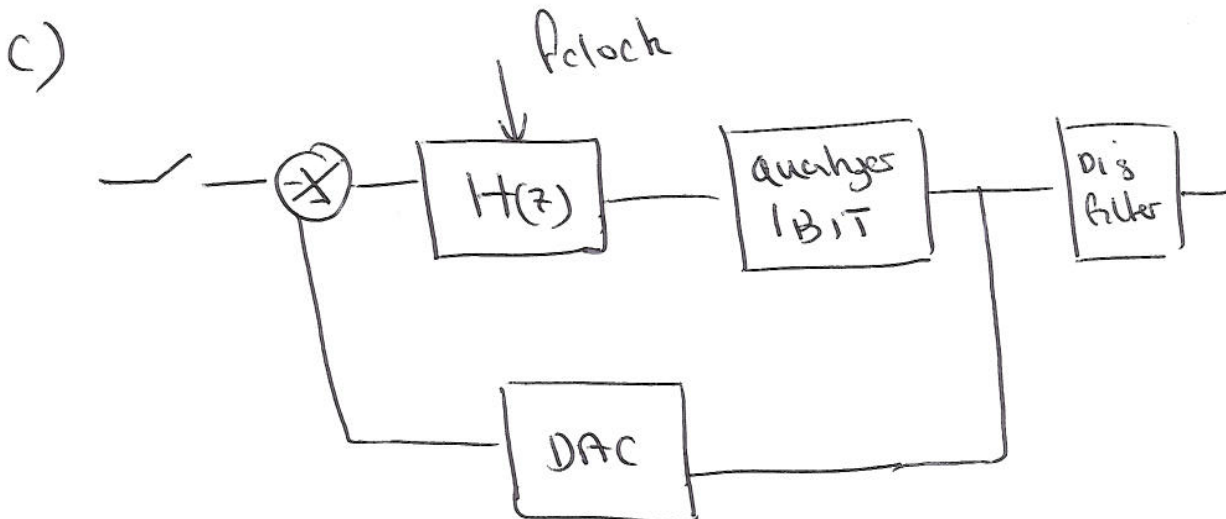
$\therefore DR = \frac{V_{ref}}{\sqrt{\frac{kT}{C}}} = 2^N$

Assume $f_c = 1/(10RC)$

then solving for C gives

$$DR = 2^N = V_{ref} / \sqrt{kT \cdot 10RC}$$

6



Basic idea is that coarse quantization noise gets shaped by $1/(H(z))$ via feedback

Generally $1/f$ in an Integrator so noise is shaped differentially. This reduces requirements upon component accuracy. The architecture includes a negative feedback loop producing the coarse estimate that oscillates about the true value of input, the digital filter averages this coarse estimate to produce a finer approximation. The feedback DFE and forward integrator force the quantization error to have a high frequency spectrum. The output of the digital filter is downsampled and gives a multibit digital representation. High frequency quantization noise is reduced. Noise shaped away very high (S/N) at low frequency.

Q4/

Assumption is that if $(V_{DS} \geq 0)$ or $(V_{DS} < (V_{GS} - V_T))$ device acts in linear region. From

$$I_D = \frac{k_n W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] [1 + \lambda V_{DS}]$$

for $V_{DS} \ll (V_{GS} - V_T)$, then $\lambda V_{DS} \ll 1$

$$\text{So } I_D = \frac{k_n W}{L} (V_{GS} - V_T) V_{DS}$$

$$\text{OR } R_{AB} = V_{DS} / I_D = L / (k_n W (V_{GS} - V_T)) \quad 5$$

Three sources of non-linearity

(i) Limited due to V_{GS} change V_T
for negative V_{GS} due to body-effect.

$$\text{i.e. } V_T = V_{T0} + \gamma \left[\sqrt{-V_{BS} + 2\phi_F} - \sqrt{2\phi_F} \right]$$

γ = bulk threshold parameter

ϕ_F = Fermi-level potential

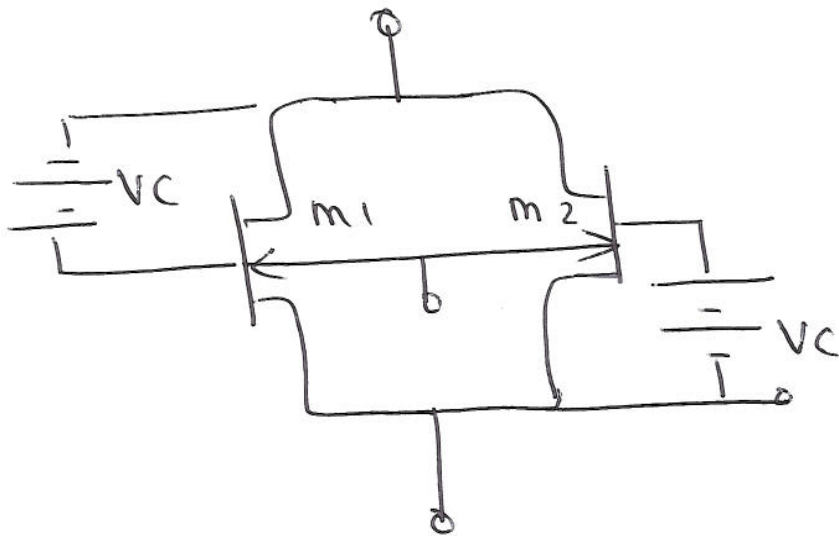
(ii) Limited due to V_{DS} approaching $(V_{GS} - V_T)$ hence saturation region for large positive V_{DS} .

(iii) For large values of V_{DS} the $V_{DS}^2/2$ term introduces large non-linearity.

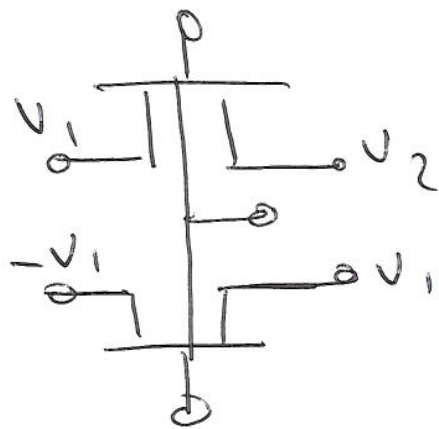
3

65

4 cont

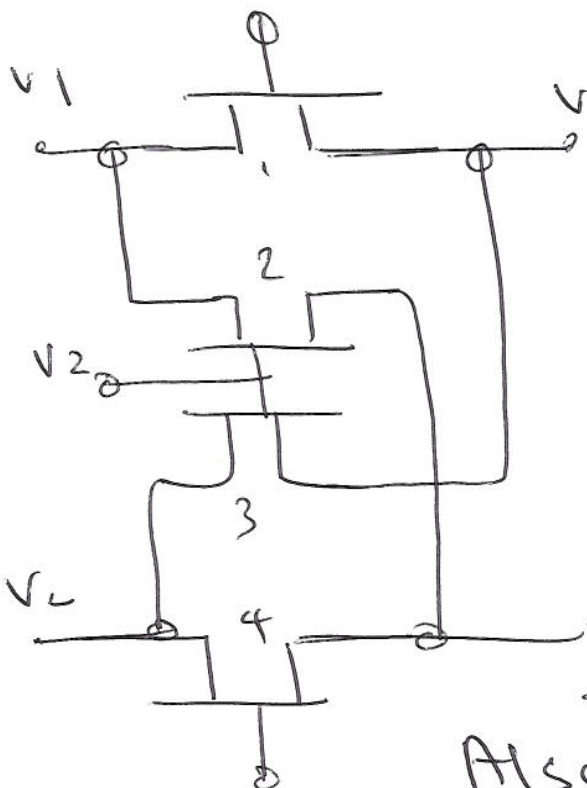


Parallel current - eliminates $V_{DS}^2/2$ term.



Differential scheme

Effects of V_{DS} cancelled.



Double differential MOS

Eliminates

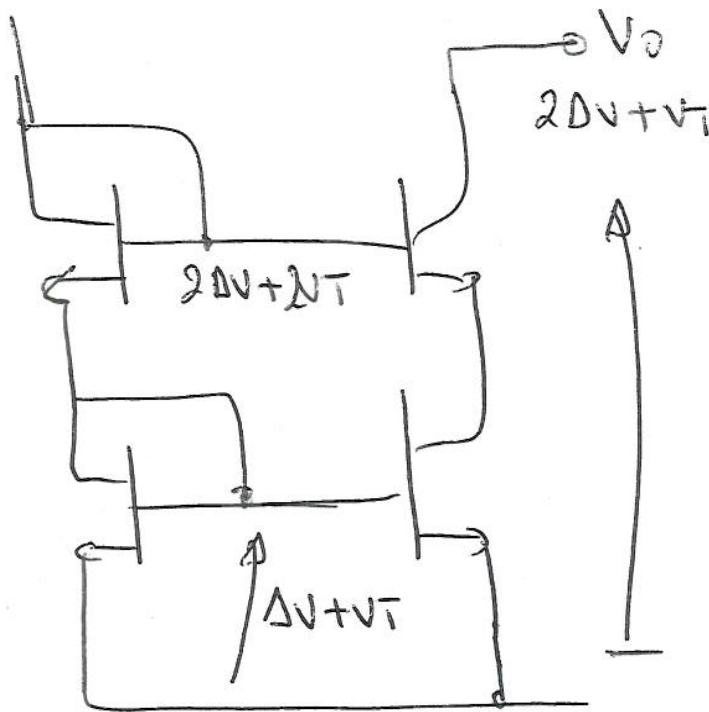
$-V_{DS}$ and V_T term

Anyone
can do

Also expect analysis
of particular cell.

2

4 cont

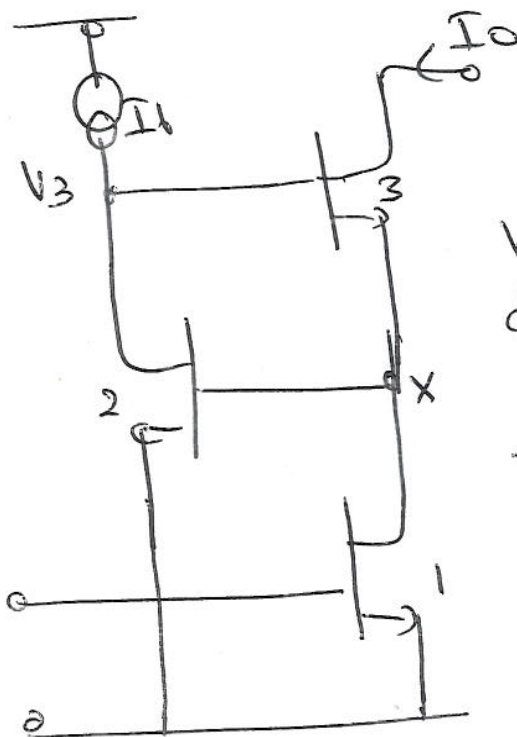


Assume
 $\Delta V = V_{GS} - V_T$
 For sat
 $V_{DS} \geq V_{GS} - V_T$

$$(V_0)_{mn} = 2(\Delta V + V_T) - V_T$$

$$= \underline{2\Delta V + V_T}$$

4



Q_3 cascodes Q_1
 hence output resistance
 due to Q_3 is
 $R_{o3} \approx r_{ds1} \parallel g_{m3} r_{ds3}$

Transistor Q_2 senses
 change in voltage at
 node (X) and
 reduces these changes
 by the loop gain

of the amplifier (Q_2 and I_b) hence this further
 increases the output resistance of the circuit to
 $R_{out} = R_{o3} \parallel g_{m2} r_{ds2} \parallel g_{m3} r_{ds3} r_{ds1} \approx (g_{m2}^2 / g_{o3})$
 Assuming equal g_{m1} and g_{o1} .

6

17

5 // Specs $A = 80 \text{ dB}$, $S.R = 5 \text{ V}/\mu\text{s}$, $GB = 3 \text{ MHz}$

$$\begin{aligned} A_1 &= g_{m2} / (g_{o4} + g_{o2}) \Rightarrow (g_{o2} + g_{o4}) \\ &= I_{D2} (1/r_n + 1/r_p) \\ &= 10 \times 10^{-6} [0.05] \\ &= 5 \times 10^{-7} \text{ } \Omega^{-1} \end{aligned}$$

$$g_{m2} = 2 \sqrt{\beta_2 I_{D2}} \Rightarrow \text{but } G.B = \frac{g_{m2}}{2\pi C_c}$$

require C_c . From $S.R = I_D / C_c$

$$\text{Then } C_c = 4 \text{ pF} \Rightarrow g_{m2} = 7.54 \times 10^{-5}$$

$$\therefore A_1 = 150.8$$

$$\text{From } g_{m2} = g_{m1} = 2 \sqrt{\beta I_D}$$

$$\beta_2 = \beta_1 = 1.42 \times 10^{-4} = \frac{K_W}{2L}$$

$$\therefore (W/L)_n = (W/L)_p = 9.46$$

$$= \underline{\underline{47/5}}$$

$$\text{Since } A_1 = 150.8, \quad A_2 = 10^4 / (150.8) = 66$$

$$A_2 = g_{m6} / (g_{o6} + g_{o7})$$

$$(g_{o6} + g_{o7}) = I_{D6} (1/r_6 + 1/r_7)$$

(5) cont

$$(g_{m6} + g_{o7}) = 20 \times 10^{-6} (0.05) = 1 \times 10^{-6} \text{ s}^{-1}$$

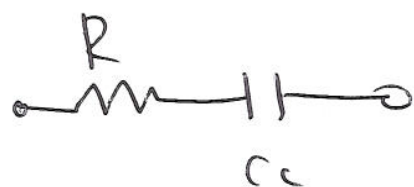
$$\text{given } g_{m6} = 6.63 \times 10^{-5}$$

$$\Rightarrow \beta_6 = \left(\frac{g_{m6}}{2} \right)^2 \frac{1}{I_{o6}} = 5.5 \times 10^{-5}$$

$$\text{This gives } (W/L)_6 = 5.5 = \underline{\underline{27/5}}$$

5

—||—



Function of R is to provide feedforward compensation and eliminate RHP zero from transfer function of OP-Amp.

$$\text{With } R \Rightarrow \text{zero} = g_{m6}/C_c,$$

$$\text{With } R \quad Z = \frac{1}{(1/g_{m6} - R) C_c}$$

① $R = 1/g_{m6} \rightarrow$ remove zero
improve ϕ

5

② $R \Rightarrow$ non-dominant pole cancels with zero.
 $\rightarrow > 1/g_{m6}$

CT

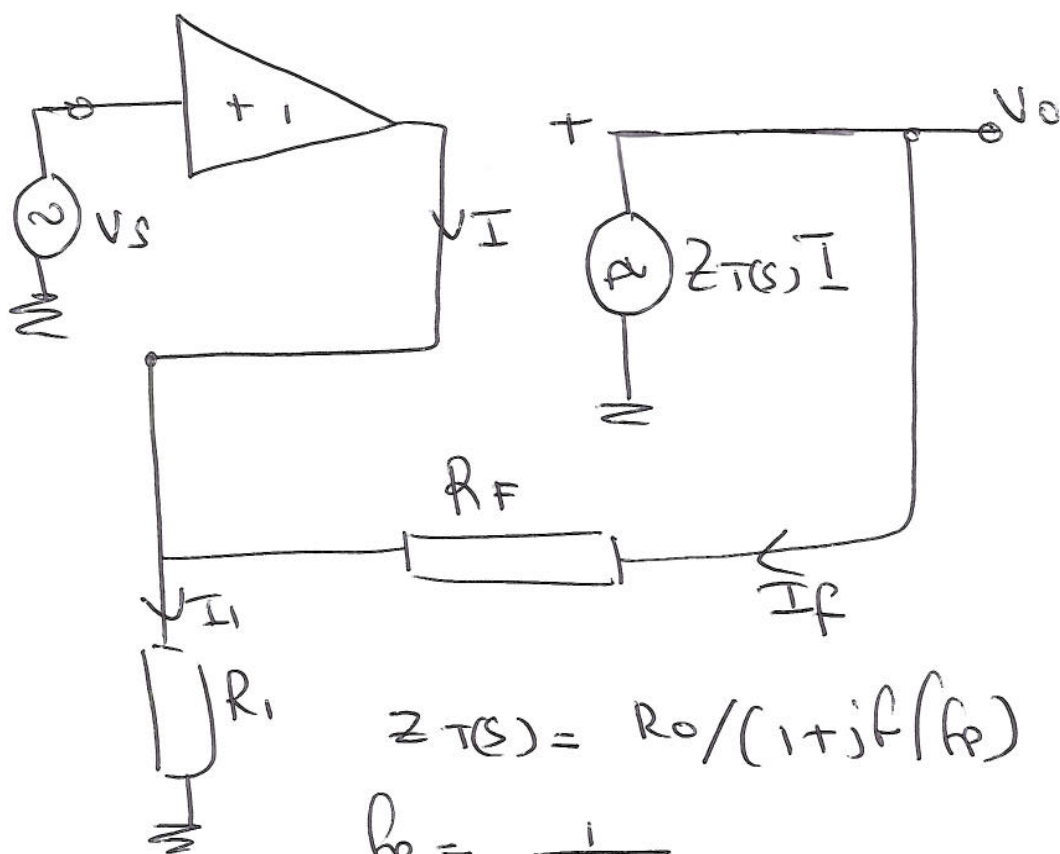
6/

Advantages of Current-mode

1) High frequency performance, wide dynamic range

low power supply voltages

2



$$Z_T(s) = R_O / (1 + jf/f_p)$$

$$f_p = \frac{1}{2\pi R_O C}$$

C = compensation capacitor

3 equations

$$I_F = (V_O - V_S) / R_F \quad - (1)$$

$$I_1 = V_S / R_I \quad - (2)$$

$$V_O = Z_T(s) I = Z_T(s) [I_1 - I_F] \quad - (3)$$

8

CT

Subs ① and ② into ③ gives,

$$(V_o/V_s) = (1 + R_F/R_i) Z_T(s) / (R_F + Z_T(s))$$

Subs for $Z_T(s)$

gain

$$(V_o/V_s)_{BW} = (1 + R_F/R_i) \left[\frac{R_o}{R_o + R_F} \right]$$

$$\times \frac{1}{\left(1 + jf / \underbrace{f_p \left[\frac{R_o + R_F}{R_F} \right]}_{BW} \right)}$$

Assuming $R_o \gg R_F$ BW

then

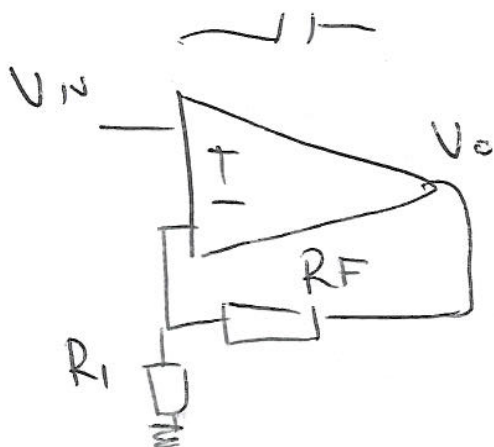
Closed loop gain $\approx (1 + R_F/R_i) - *$

$$\text{Closed loop Bandwidth} \approx \frac{f_p R_o}{A F} = \frac{1}{2\pi R_F C}$$

Hence R_F sets the amplifier
constant BW

Lx.

and R_i chosen to set the gain



$$BW = \frac{1}{2\pi R_F C} = 10 \text{ MHz}$$

$$\therefore \text{ given } C = 4 \text{ pF}$$

$$R_F = 3.98 \text{ k}\Omega$$

$$\text{Since } A = (1 + R_F/R_i) = 100$$

$$R_i = 44 \text{ }\Omega$$

5

CT

Analogue Converter

$2I_{in}$ on +ve terminal of comparator
compared to I_{ref} (-ve) terminal

If $2I_{in} < I_{ref}$, comp output goes low

digital output = 0 and analogue
output = $2I_{in}$

If $2I_{in} > I_{ref}$, comp output goes high
digital output = 1, analogue output
 $2I_{in} - I_{ref}$

Analogue output consequently feeds
into following 'bit' which
performs exactly the same function.
The process is repeated as many times
as necessary to achieve desired
resolution.

Digital VLSI — small size,
low-power
supply voltages
less stringent
upon analogue accuracy

5

CK