UNIVERSITY OF LONDON
IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 1996

BEng Honours Degree in Computing Part III
MSc Degree in Computing Science
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the
Diploma of Membership of Imperial College
Associateship of the City and Guilds of London Institute

PAPER 3.18

CUSTOM COMPUTING
Friday, May 10th 1996, 10.00 - 12.00

Answer THREE questions

For admin. only: paper contains
4 questions
3 pages (excluding cover page)

1. A VHDL test bench for a finite impulse response (FIR) filter chip is shown in *Figure 1a*. In addition to the `FIR` module which is being tested, it consists of three modules: the clock generator module `CLKGEN`, the input stimulus module `PRBS` and the output monitor module `ROM`.

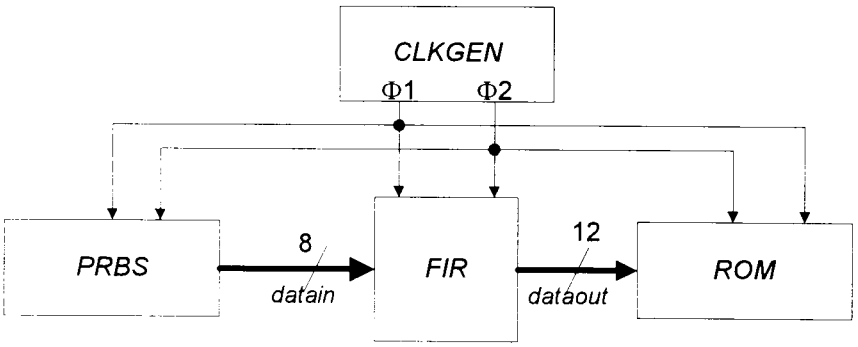

Figure 1a

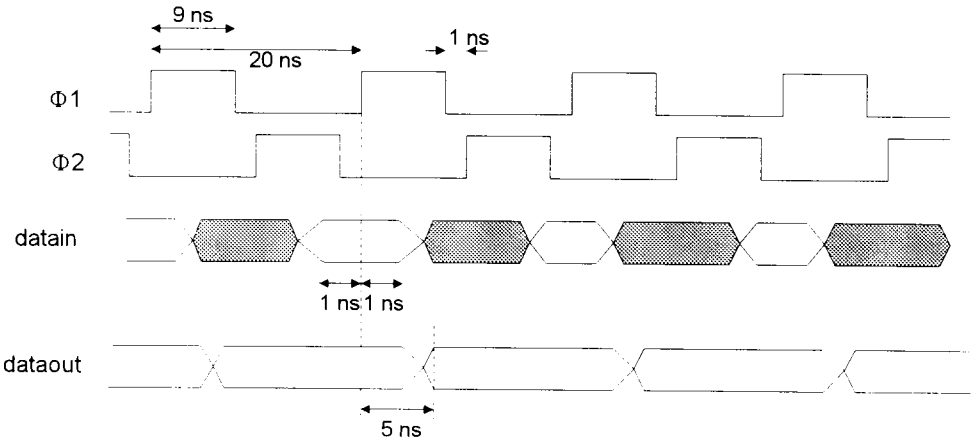

Figure 1b

a) The clock generator produces two phase non-overlapping clock signals Φ1 and Φ 2 with periods of 20ns, pulse-width of 9ns and a period of non-overlap of 1ns as shown in *Figure 1b*. Write the VHDL code segment for the *CLKGEN* module.

b) The FIR filter module latches the input data (8-bit wide) on the rising edge of Φ1 as shown in *Figure 1b* with setup and hold times of 1ns. The *PRBS* module produces a pseudo-random binary sequence of length 1023, implementing the primitive polynomial: $1 + x^3 + x^{10}$. Write the VHDL code segment for the *PRBS* module.

c) The output produced by the *FIR* module is checked against a set of expected results stored in an array emulating a ROM in the *ROM* module. The output delay from the *FIR* module must be 5ns or lower as shown in *Figure 1b*. Write the VHDL code segment for the *ROM* module. Do not specify the actual contents of the ROM table.

You may assume that a reset signal is available for initialising all the modules to a known state and that all the registers used inside the *FIR* module are reset asynchronously.

The three parts carry, respectively, 25%, 35% and 40% of the marks.

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2. *Figure 2a* shows the entity declaration for a finite state machine that detects the binary sequence 1000. The state machine is synchronised to the rising edge of the clock signal *clk*. The output signal *sync* goes high for one cycle after the sequence 1000 is detected in the input signal *data*. The *rst* signal synchronously resets the finite state machine to the idle state. *Figure 2b* shows the timing diagram of the state machine.

```
ENTITY detector_fsm IS
   PORT (data, clk, rst : IN std_logic;
         sync           : OUT std_logic);
END detector_fsm;
```

Figure 2a

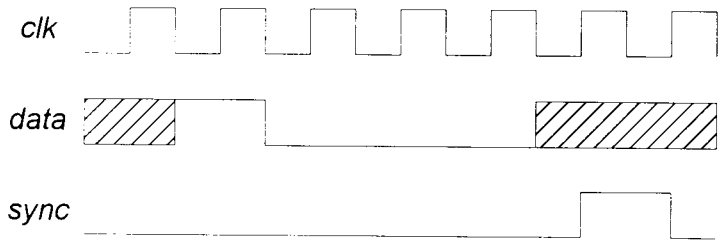

Figure 2b

a) Derive the state diagram and the state transition table for the finite state machine.

b) Implement the finite state machine as an algorithmic VHDL model using transition table in the data structure.

Turn over ...

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3 The definition of the σ operator is given by:

$$x\ (\sigma\ R)\ y \quad \Leftrightarrow \quad \exists s : \langle x, s\rangle\ R\ \langle s, y\rangle.$$

a Show that:

$$\sigma\ (Q \leftrightarrow R) \quad = \quad \sigma\ Q\ ;\ \sigma\ R.$$

b State the inductive definition of the row operator, and show that

$$\sigma\ (\mathsf{row}_n\ R) \quad = \quad (\sigma\ R)^n.$$

c Describe the state transition function of a sorter using a row of components each of which sorts a pair of numbers. Explain how the transformation in Part (b) can be used in deriving a pipelined sorter.

The three parts carry, respectively, 20%, 45% and 35% of the marks.

4a Define *series composition*, *parallel composition* and *converse*. Derive an alternative expression involving P^{-1} and Q^{-1} for:

i) $(P\ ;\ Q)^{-1}$,

ii) $[P, Q]^{-1}$.

b Given that $R\backslash S = S^{-1}\ ;\ R\ ;\ S$, use the results in Part (a) to show that:

i) $(R\backslash S)^{-1} = (R^{-1})\backslash S$,

ii) $(P\backslash Q)\backslash R = P\backslash(Q\ ;\ R)$.

c Given that $R\backslash\backslash[S, T] = [T, S]^{-1}\ ;\ R\ ;\ [S, T]$ and *swap* is a relation which reverses the position of the elements in a pair, use the results in Part (a) and Part (b) to show that:

i) $R\backslash\backslash S = (S^{-1})\backslash swap\ ;\ R\ ;\ S$,

ii) $(P\backslash\backslash Q)\backslash\backslash R = P\backslash\backslash(Q\ ;\ R)$.

d State Horner's Rule for a row of components using the $\backslash\backslash$ operator. Sketch a picture to illustrate this transformation when the row has four components, and explain how this transformation can be used to pipeline a circuit.

The four parts carry, respectively, 25%, 20%, 30% and 25% of the marks.

End of paper