Analogue Electronics II (E2.2) - 2018

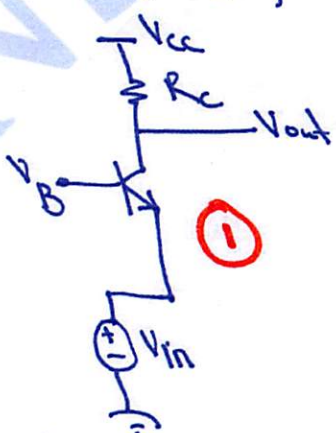
(1) a) Integrated circuit
- high integration density – complex circuits, many components (1)
- low power consumption (and silicon area) (1)
- low cost (for high volume production) (1)

PCB
- low prototyping cost (ICs cost £k's) (1)
- Quick development time (ICs take months/years) (1)
- can debug after manufacture (1)
  - chips cannot modify anything.

any 5

answered well

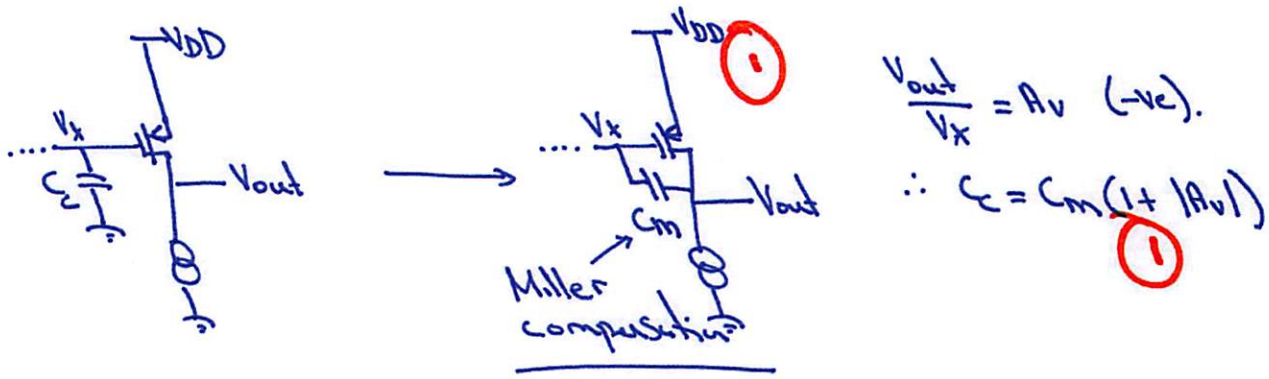
b) CB amplifier takes its input from emitter terminal, output from collector. Base terminal is at AC ground (DC bias) (1) Best to describe CB stage as a unity-gain current amplifier as current gain ≈ 1 ($A_I = \frac{\beta}{\beta+1}$) (1). Voltage gain similar (but +ve) to CE amp ($A_V = +g_m(R_C \| r_o)$) (1). It has low I/P impedance ($\approx 1/g_m$) and moderate R_{out} (r_o) (1)



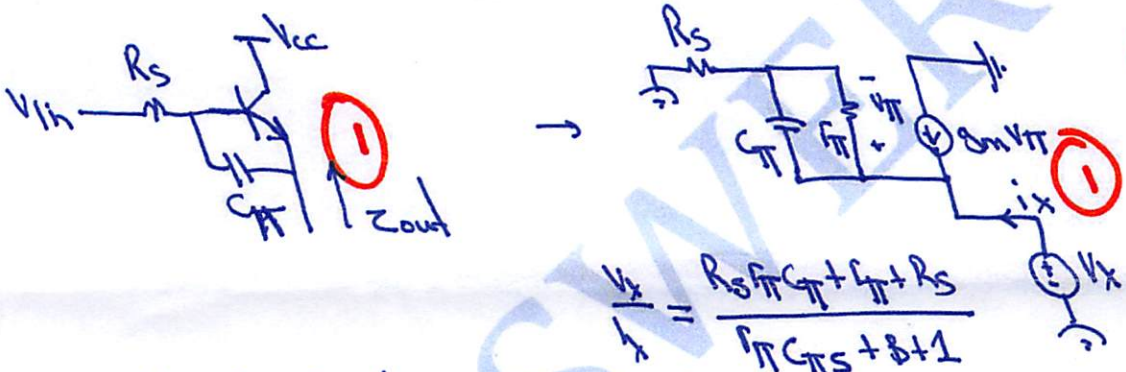
(1)

c) Typically in op-amp design, phase margin can be improved by inserting a compensation capacitor to limit $B\omega_t$ (1) such that sufficient ~~B\omega_t~~ P.M. can be achieved (1). By exploiting Miller's theorem this cap. value can be reduced if inserted across an inverting amplifier (1)

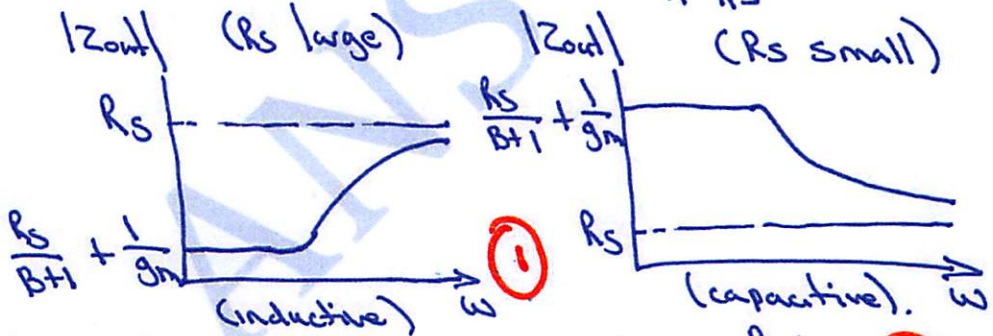
Generally students here just describes PM or Miller's theorem but not how to apply one to improving the other.



d) If we consider the frequency response of the output impedance of a source-follower (or emitter follower) this exhibits an increase in impedance with frequency (similar to an inductor).

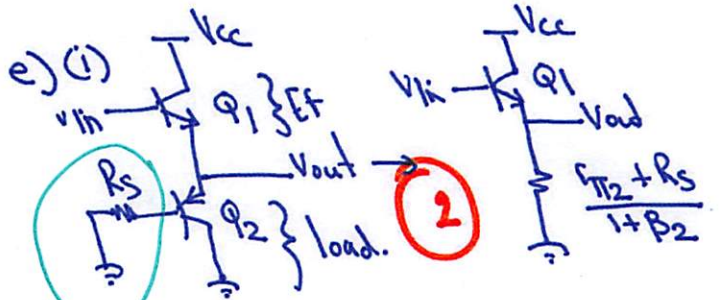


Most students described an op-amp based implementation question specifically asks for transistor approach



For this to be the case $R_s > 1/g_m + R_s/\beta+1$

e) (i)



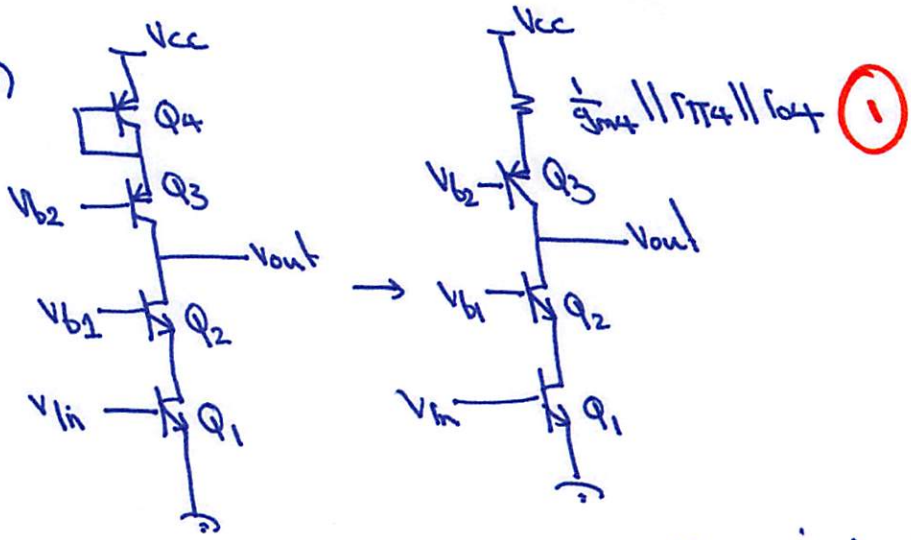
for EF

$A_v = \frac{R_E}{1/g_m + R_E}$

$\therefore A_v = \frac{\frac{r_{\pi 2} + R_s}{1+\beta_2}}{1/g_{m1} + \frac{r_{\pi 2} + R_s}{1+\beta_2}}$

Many students missed this and just considered $R_E = 1/g_{m2} || r_{\pi 2} || R_2$ instead of →

c) (ii)



Use $A_v = -G_m R_{out}$ $G_m = g_{m1}$ (since $i_{out} = i_{ds1}$, $V_{in} = v_{gs1}$)

$R_{out} = R_{up} \| R_{down}$

$R_{up} = \left[1 + g_{m3}\left(\frac{1}{g_{m4}} \| r_{o4} \| r_{\pi 4} \| r_{\pi 3}\right)\right] r_{o3} + \left[\frac{1}{g_{m4}} \| r_{o4} \| r_{\pi 4} \| r_{\pi 3}\right]$

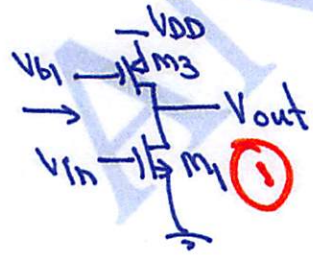
$R_{down} = \left[1 + g_{m2}(r_{o2} \| r_{\pi 2})\right] r_{o2} + (r_{o1} \| r_{\pi 2})$

$A_v = -g_{m1}(R_{up} \| R_{down})$

assuming $R_{up} << R_{down}$.

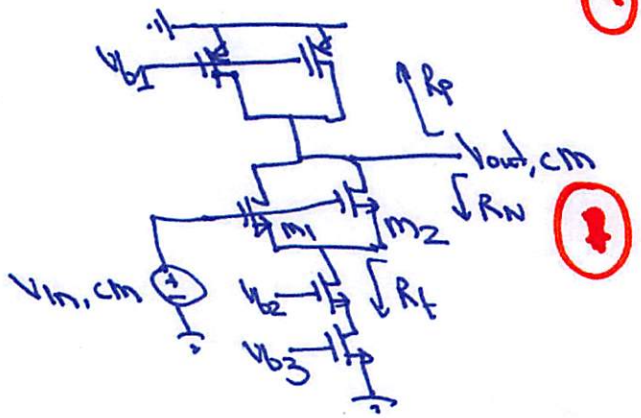
$\therefore A_v \approx -g_{m1}(R_{up})$

f) for DM gain → half ckt approximation due to symmetry.



$A_{v,DM} = -g_{m1}(r_{o1} \| r_{o3})$

for CM gain → connect i/ps together:



$R_P = r_{o3} \| r_{o4} = \frac{r_{o3}}{2}$ (1)

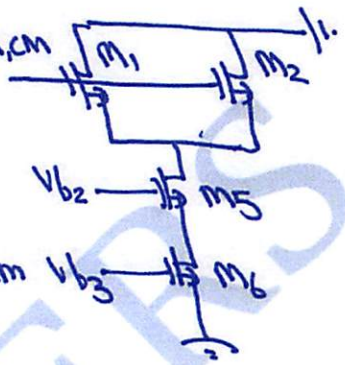
$R_N = \frac{r_{o1}}{2} + R_t + g_{m1}\frac{r_{o1}}{2} \cdot R_t \approx g_{m1} r_{o1} R_t$

$\approx g_{m1} r_{o1} (g_{m5} r_{o5} r_{o6})$

$R_{out} = R_P \| R_N = \frac{r_{o3}}{2} \| g_{m1} g_{m5} r_{o1} r_{o5} r_{o6} \approx \frac{r_{o3}}{2}$ (1)

To calculate G_m:

$G_m = \frac{i_o}{v_{in,cm}} = \frac{2 g_{m1} V_{gs1}}{v_{in,cm}}$ (1)



$= \frac{2 g_{m1}}{v_{in,cm}} \cdot \frac{\frac{1}{2 g_{m1}}}{\frac{1}{2 g_{m1}} + R_t} \cdot v_{in,cm}$

$\therefore G_m \approx \frac{1}{R_t}$ (1)

$\rightarrow A_{v_{cm}} = -G_m R_{out} = -\frac{r_{o3}}{R_t} = -\frac{r_{o3}}{2 g_{m5} r_{o5} r_{o6}}$ (1) ✓

ANSWERED VERY WELL → SEVERAL STUDENTS TRIED TO OVERSIMPLIFY

(2) a) The inverter topology is actually two CS amplifiers connected in parallel (i.e. NMOS and PMOS) (1)

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Advantages: – increased g_m $(=g_{mN}+g_{mP})$ (1)

– easy to cascade to multiple stages / simple topology (1)

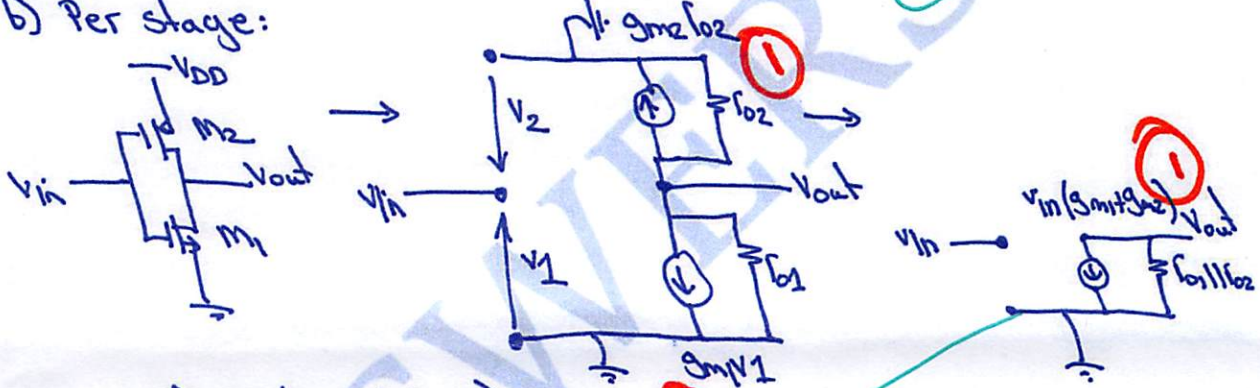
Disadvantages: – Tricky to bias – small linear range (1)

KEY POINT MISSED

– operating in "short circuit" region potentially high power (1)

– suffers from extra "Miller" (1)

b) Per stage:



$\therefore A_v = -(g_{m1}+g_{m2})\cdot r_{o1}\|r_{o2}$ (1)

$\rightarrow A_v(2\text{-stages}) = (g_{m1}+g_{m2})^2 (r_{o1}\|r_{o2})^2$ (1) (non-inverting) (1)

c) $I_{D1} = I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1}-V_{TN})^2 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS2}-|V_{THP}|)^2$

$\rightarrow 200\mu(10)(V_{IN}-0.4)^2 = 100\mu(20)(1.8-V_{IN}-0.5)^2$

$(V_{IN}-0.4)^2 = (1.3-V_{IN})^2 \rightarrow V_{IN} = 0.85V$ (1)

$I_{D1} = \frac{1}{2}(200\mu)(10)(0.85-0.4)^2 = 202.5\mu A$

many students didn't start with this

$g_{m1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_D} = \sqrt{2(200\mu)10.202.5\mu A} = 900\mu S$ (1)

$g_{m2} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_2 I_D} = 900\mu S$

$r_{o1} = \frac{1}{\lambda_n I_D} = \frac{1}{0.1(202.5\mu A)} = 49.4k\Omega$ (1)

$r_{o2} = 24.7k\Omega$.

$\therefore A_v = A_{v1}\cdot A_{v2} = (1.8mS)^2\cdot(49.4k\|24.7k)^2$

$= 879$ (1) $(= 58.9dB)$ (1)

NOT ALL STUDENTS PROVIDED GAIN IN DB

d). $f_{px} = \frac{1}{2\pi C_x \cdot (r_{o1} \| r_{o2})}$ (1) and $f_{p_{out}} = \frac{1}{2\pi C_{out} \cdot (r_{o3} \| r_{o4})}$ (1)

$r_{o1} \| r_{o2} = r_{o3} \| r_{o4} = 24.8k \| 49.4k = 16.5k\Omega$ (1) (1)

$C_x = C_{GD1}\left(1 + \frac{1}{|A_{v1}|}\right) + C_{GD2}\left(1 + \frac{1}{|A_{v1}|}\right) + C_{DB1} + C_{DB2} + C_{GS3} + C_{GS4} + C_{GD3}(1 + |A_{v2}|) + C_{GD4}(1 + |A_{v2}|)$ (1)

$C_{out} = C_{GD3}\left(1 + \frac{1}{|A_{v2}|}\right) + C_{GD4}\left(1 + \frac{1}{|A_{v2}|}\right) + C_{BD3} + C_{BD4}$ (1)

$C_x = 0.5f(5)\left(1 + \frac{1}{29.6}\right) + 0.5f(10)\left(1 + \frac{1}{29.6}\right) + 2f\left(\frac{2}{3}\right)(5 \times 0.5) + 2f\left(\frac{2}{3}\right)(10 \times 0.5) + 0.5f(5)(1+29.6) + 0.5f(10)(1+29.6)$

$= (7.75f + 100f + 229.5f)f = 337.25ff$ (1)

$C_{out} = 7.75ff$ (1)

$f_{px} = \frac{1}{2\pi(337.5f) \cdot 16.5k} = 28.7\,MHz$ (1)

$f_{p_{act}} = \frac{1}{2\pi(7.75f) \cdot 16.5k} = 1.25\,GHz$ (1)

Method generally ok

NOT ANSWERED CORRECT

e) - Power consumption due to S.C. current can be limited by utilising current source/sink devices between inverter and power supply connections — i.e. current starved inverter. (2)
- use feedback to bias ~~or~~ DC bias network with capacitive coupling for signal path. (2)
- reduce drain capacitance to reduce Miller. Smaller gate area or width if possible. (1)

(3) a) A key challenge in cascading high gain stages would be the input offset saturating the output (i.e. hitting the supply). Also a low gain bandwidth product may mean a limited bandwidth when trying to achieve high gain (+also potentially gain errors)

→ for example in circuit given. $A_V = (100)^2 = 10{,}000$. for offset of 1mV → 10V at o/p.

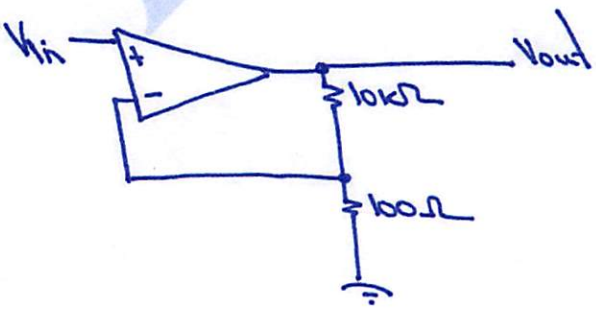
Also GBP = 2MHz → BW (@ A_V=100) = $\frac{2\text{MHz}}{100} = 20\text{kHz}$

b) it is likely this op-amp is CMOS based due to:

1. I/P impedance being relatively high (would expect BJT-based lower.
2. I/P bias also very low → BJT base current expected orders of magnitude higher.

would expect this op-amp to have an NMOS differential pair. This is because both I/P and O/P CMVR require at least 0.5V from GND whereas 0.2V margin from VDD. This tends to suggest a NMOS bias transistor to the diff. pair

c) Considering 2nd stage only



$A_{OL} = 60\text{dB} = 1000$

$k = \frac{100}{10100}$

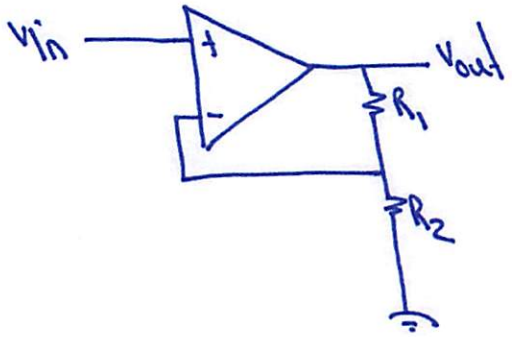
$A_{CL} = \frac{1000}{1 + \frac{100}{10100} \times 10000}$

$= 91.73$

$\therefore R_{out(CL)} = \frac{R_{out(OL)}}{1 + LG} = \frac{65\Omega}{1 + \frac{100}{10100} \times 1000}$

$= 5.96\Omega$

d) Gain error - first expression for A_v considering a finite A_0



$$V_{out} = (V_{in1} - V_{in2}) \cdot A_0$$

$$V_{in2} = \frac{R_2}{R_1 + R_2} \cdot V_{out}$$ (1)

$$\frac{V_{out}}{V_{in}} = \frac{A_0}{1 + \frac{R_2}{R_1+R_2} \cdot A_0}$$ (1)

(see previous answer to part c – $A_v = 91.73$) (1)

$$\therefore \text{Gain error} = \frac{(1 + R_1/R_2)}{A_0} = 0.101 \quad (= 10.1\% \text{ error})$$ (2)

e) (i) –3dB bandwidth is limited by the dominant pole (node that is associated with the low frequency pole). (1)

(ii) Slew rate is limited by the amount of current the output stage can sink/source in combination with the output capacitance. If op-amp output stage is simply for example a CS with current source load slew up would be limited by the current sunce and slew down by the sinking ability of the CS itself (2)

(iii) CMRR and PSRR can be improved by increasing the output resistance of the bias transistor to the differential pair – or by adopting a fully differential topology (differential in, differential out). Both CMRR and PSRR are affected (and typically limited) by and assymetry in the implementation (eg. mismatch) (2)

Many students did not know what PSRR is of mention re: assymetry/mismatch.

f) generally everything is a trade-off in analogue design and power cannot be reduced by not giving something (eg. gain or BW or noise) however selection of ckt. topology may help.
eg. in op-amp design. (1)
- output stage - eg. class B instead of class A (1)
- gain stage - reusing current bias, eg. cascode instead of cascades stages. (1) (1)