Final.

E1.4

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2010

EEE/ISE PART I: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 1

Monday, 7 June 10:00 am

Time allowed: 2:00 hours

There are FOUR questions on this paper.

Q1 is compulsory.
Answer Q1 and any two of questions 2-4.
Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : A.S. Holmes, A.S. Holmes

Second Marker(s) : S. Lucyszyn, S. Lucyszyn

1. **This question is compulsory**. You should attempt all six parts. State clearly any assumptions made in your calculations.

   a) For the circuit in Figure 1.1, determine the operating mode of the MOSFET and the value of the voltage V.

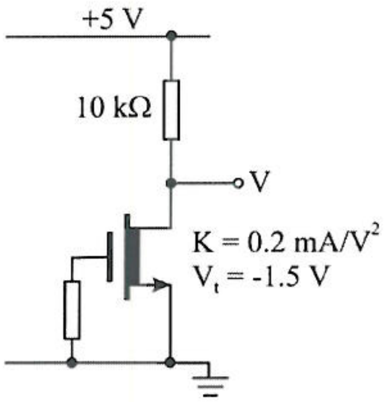

Figure 1.1 [6]

   b) Assuming the transistors in Figure 1.2 are matched, and ignoring base currents, derive a relationship between the currents I_1, I_2 and the resistor R. Hence determine the value of R that will give $I_2 = 10\ \mu A$ when $I_1 = 1$ mA.

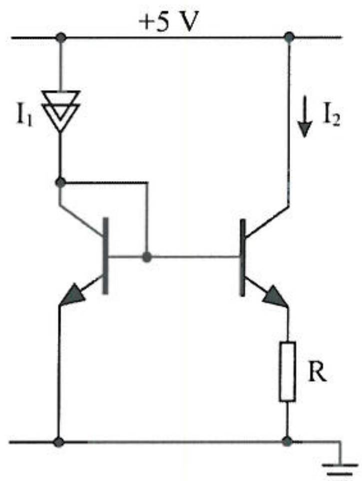

Figure 1.2 [8]

   c) A grounded common emitter amplifier is constructed using a BJT with an Early voltage of 120 V. The load resistance at the collector is 20 kΩ, and the transistor is biased at a collector current of 0.25 mA. What is the small-signal voltage gain of the circuit? [6]

Question 1 continues on the next page...

Question 1 continued

d) State the operating modes of the MOSFETs in Figure 1.3 and determine the value of the voltage V.

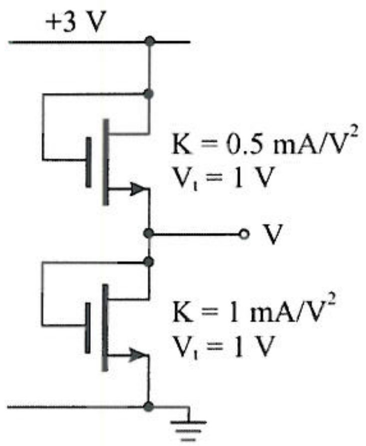

Figure 1.3 [6]

e) Derive a large-signal relationship between the differential input voltage ($V_{IN1} - V_{IN2}$) and the output voltage V_{OUT} for the amplifier in Figure 1.4, assuming the transistors are matched and both are active. Draw a dimensioned sketch showing this relationship for differential input voltages in the range -100 mV to + 100 mV.

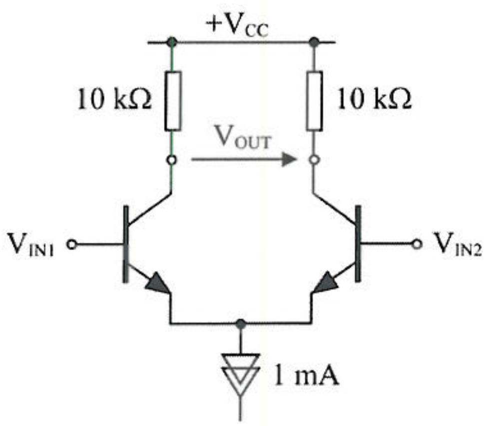

Figure 1.4 [10]

f) The characteristic equation for a Hartley oscillator is of the form:

$$(1+\beta)L_1L_2Cs^3 + (L_1 + L_2)Cr_{be}s^2 + L_1s + r_{be} = 0$$

where L_1, L_2 and C are the reactive components, β and r_{be} are the usual transistor small-signal parameters, and s is the complex frequency. Derive an expression for the frequency of stable oscillation. [4]

2. a) Determine the collector bias current and quiescent output voltage for the amplifier in Figure 2.1, stating clearly any assumptions you make. Your calculation should take into account the base current of the transistor. [8]

b) Draw a small-signal equivalent circuit of the amplifier, and hence determine the small-signal macromodel parameters i.e. input resistance, output resistance and voltage gain. You may neglect the transistor's small-signal output resistance. [12]

c) Two amplifiers similar to that shown in Figure 2.1 are cascaded and inserted between a signal source and a load, as shown in Figure 2.2. Determine the overall voltage gain v_L/v_S for this arrangement at frequencies for which all the coupling capacitors are effectively short-circuit. [10]

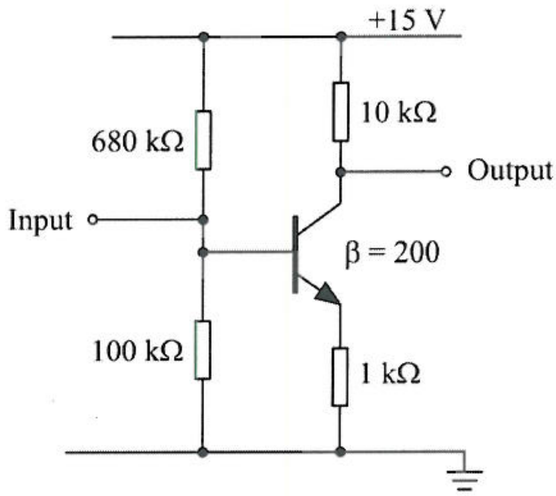

Figure 2.1

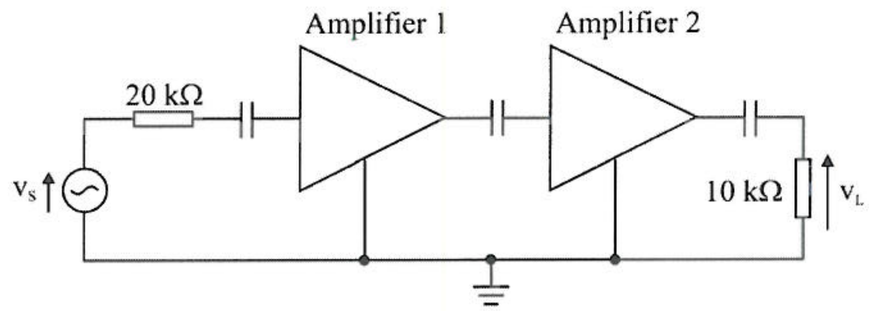

Figure 2.2

3. Figure 3 shows a single-stage amplifier in which a depletion MOSFT provides the active load for an enhancement MOSFET.

   a) Assuming both MOSFETs are active, and that the current in the bias network is small, show that the quiescent output voltage may be expressed as:

$$V_{OUT} = \left(1+\frac{R_{G1}}{R_{G2}}\right)\cdot\left(V_{t1} - V_{t2}\sqrt{\frac{K_2}{K_1}}\right)$$

   Hence determine the value of R_{G1} that will give a quiescent output voltage of +5 V. Verify that both MOSFETs are active under these conditions, and also evaluate the quiescent drain current. [10]

   b) Draw a small-signal equivalent circuit of the amplifier, including all components, and hence calculate its mid-band small-signal voltage gain. You should assume the value of R_{G1} you calculated in part a).

   Also determine the mid-band small-signal input resistance of the circuit, and hence choose a value for the input capacitor C such that the lower cut-off frequency of the mid-band is at 20 Hz. [16]

   c) Describe the *body effect*, and explain its implications for a circuit of the kind shown in Figure 3 when implemented in integrated form using NMOS technology. [4]

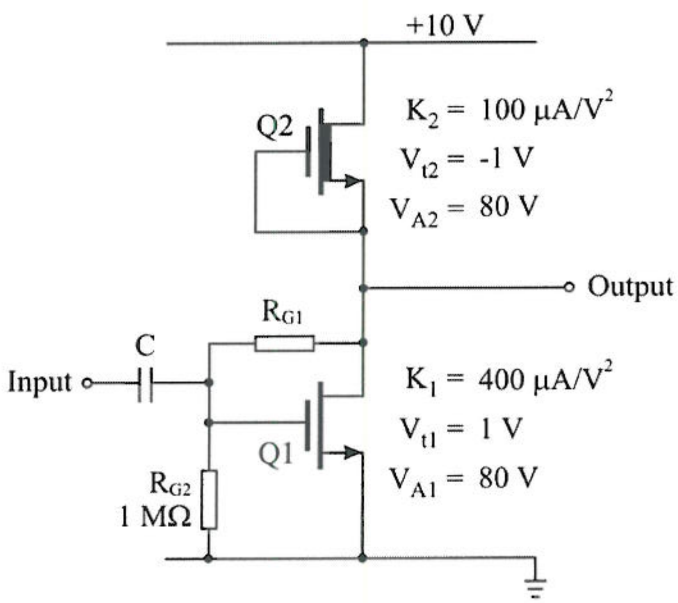

Figure 3

4. a) Briefly discuss the relative merits of class A, class B and class AB output stages. [6]

b) It is proposed that the class AB configuration shown in Figure 4 be used as the output stage of an operational amplifier. The transistors Q1-Q4 are matched, with saturation currents of 5×10^{-14} A and β values of 200.

Explain why all four transistors necessarily have the same collector bias current when Vin = 0 and the amplifier is connected to a resistive load as shown. Calculate the value of this current, stating any simplifying assumptions made in your calculation.

What is the absolute maximum load current that the output stage can deliver at an output voltage of +10V? [12]

c) Making use of the large signal BJT equation, $I_C = I_S\exp(V_{BE}/V_T)$, calculate values for the base voltage of Q3 and the input voltage Vin when the output stage is delivering +10 V into a 500 Ω load. In this calculation you should assume that Q4 has negligible emitter current.

By evaluating the base-emitter voltage of Q2 under same load conditions, show that the above assumption about Q4 is justified. [12]

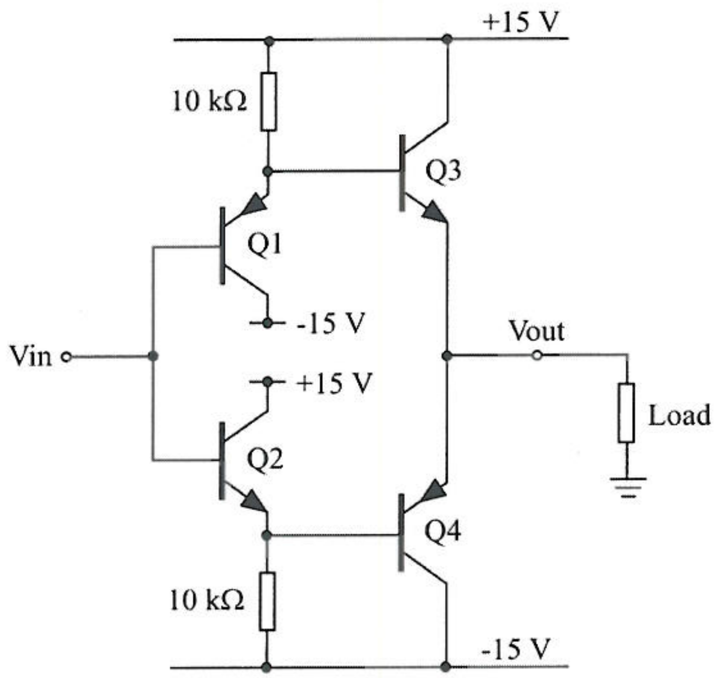

Figure 4

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1 a) Assume active mode initially (easier)

$V_{GS} = 0$, so $I_D = K(-V_t)^2 = 0.2m \times (1.5)^2 = 0.45\,mA$

But this would imply $V = 5 - 0.45 \times 10 = 0.5 < (V_{GS} - V_t)$

$\Rightarrow$ Active assumption wrong and MOSFET in TRIODE

Now need to solve $(5 - V)/10k = 0.2m\,[2V(1.5) - V^2]$

$$5 - V = 2(3V - V^2) \quad \Rightarrow \quad 2V^2 - 7V + 5 = 0$$

$$(2V - 5)(V - 1) = 0, \quad V = 1V \text{ or } V = 2.5V$$

Higher root can be neglected as $> (V_{GS} - V_t)$, so $V = 1V$ [6]

b) Applying KVL to loop containing EBJs and R:

$$V_{BE1} = V_{BE2} + I_2 R \qquad (\text{LH } Q1,\ \text{RH } Q2)$$

But from Ebers Moll we have:

$$V_{BE1} = V_T \ln(I_1/I_S) \quad ; \quad V_{BE2} = V_T \ln(I_2/I_S)$$

Combining the above relations:

$$V_T \ln(I_1/I_S) = V_T \ln(I_2/I_S) + I_2 R$$

$$\Rightarrow \quad V_T \ln(I_1/I_2) = I_2 R \quad \Rightarrow \quad R = \frac{V_T}{I_2} \ln\left(\frac{I_1}{I_2}\right)$$

Putting $V_T = 25\,mV$, $I_2 = 10\,\mu A$, $\frac{I_1}{I_2} = 100$ $\Rightarrow$ $R = 11.51\,k\Omega$ [8]

c) The small-signal voltage gain is

$$A_v = -g_m(r_o \| R_c) \qquad (\text{may be quoted})$$

For amplifier in question we have:

$g_m = I_C/V_T = 0.25\,mA/25\,mV = 10\,mS$

$r_o = V_A/I_C = 120V/0.25\,mA = 480\,k\Omega$

$R_c = 20\,k\Omega$

$$\Rightarrow \quad A_v = -0.01 \times (480k \| 20k) = -192$$ [6]

d) MOSFETs are both D-G connected, and $V_{DD} > (V_{t1} + V_{t2})$

(Upper Q2, lower Q1) $\Rightarrow$ Both ACTIVE

Drain currents are equal, so:

$$k_1(V - V_{t1})^2 = k_2(V_{DD} - V - V_{t2})^2$$

$$1.(V - 1)^2 = 0.5(3 - V - 1)^2$$

1 d) cont'd

Taking $\sqrt{\ }$ both sides, with +ve signs (both FETs above threshold)

$$\sqrt{2}(V-1) = (2-V) \quad \Rightarrow \quad (1+\sqrt{2})V = 2+\sqrt{2}$$

$$\Rightarrow \quad \underline{\underline{V = \sqrt{2}\ V}}$$ [6]

e) Collector currents are given by: (LH Q1, RH Q2)

$$I_{C1} = I_S \exp\left(\frac{V_{IN1} - V_E}{V_T}\right) \quad ; \quad I_{C2} = I_S \exp\left(\frac{V_{IN2} - V_E}{V_T}\right)$$

$V_D = V_{IN1} - V_{IN2}$

where V_E = common emitter voltage $\Rightarrow \frac{I_{C1}}{I_{C2}} = \exp(V_D/V_T)$ .. ①

Also, neglecting I_Bs, $I_{C1} + I_{C2} = I_0$, $I_0 = 1\,mA$ .. ②

① & ② $\Rightarrow$ $I_{C1} = I_0/[1 + \exp(-V_D/V_T)]$; $I_{C2} = I_0/[1 + \exp(V_D/V_T)]$

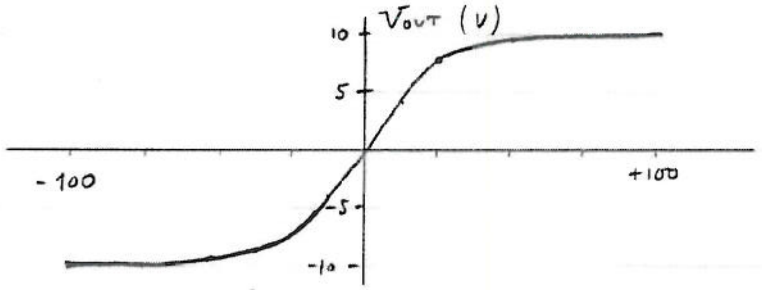
Now, $V_{C1} = V_{CC} - R_C I_{C1}$ and $V_{C2} = V_{CC} - R_C I_{C2}$ $R_C = 10\,k\Omega$

$$\Rightarrow V_{OUT} = (V_{C2} - V_{C1}) = R_C(I_{C1} - I_{C2})$$

$$= R_C I_0 \left[\frac{1}{1+\exp(-V_D/V_T)} - \frac{1}{1+\exp(V_D/V_T)}\right]$$

$$= \underline{\underline{10.\tanh\left(V_D/2V_T\right)\ V}}$$

assuming both Qs remain active, and $V_T = 25\,mV$



[10]

f) For stable oscillation, characteristic equation must have a root with $s = j\omega$. Substituting this form for s gives:

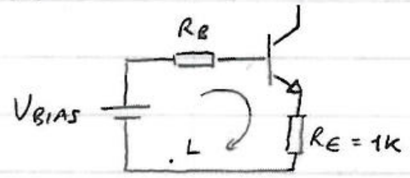
$$-j(1+\beta)L_1L_2C\,\omega^3 - (L_1+L_2)C\,r_{be}\,\omega^2 + jL_1\omega + r_{be} = 0$$

$\mathrm{Re} = 0 \quad \Rightarrow \quad \omega^2(L_1+L_2)C = 1$ .. ①

$\mathrm{Im} = 0 \quad \Rightarrow \quad (1+\beta)L_2C\,\omega^2 = 1 \quad \Rightarrow$ (with ①) $\cdot\ \beta = \frac{L_1}{L_2}$ .. ②

① defines the oscillation frequency while ② defines the threshold gain. So, frequency is $\underline{\underline{\omega = \frac{1}{\sqrt{(L_1+L_2)C}}}}$ [4]

2 a) Bias cct:



where $V_{BIAS} = 15 \times 100/(100 + 680) = 1.923\,V$

$R_B = 680k // 100k = 87.2\,k$

KVL in loop L: $I_E R_E + V_{BE} + I_B R_B = V_{BIAS}$

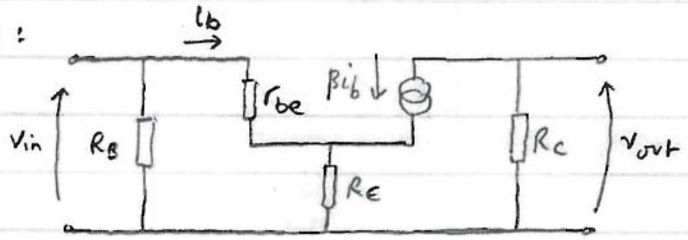
using $I_E = (1+\beta) I_B \Rightarrow I_E = (V_{BIAS} - V_{BE})/(R_E + R_B/(1+\beta))$

Assuming $V_{BE} = 0.7V$, $I_E = (1.92 - 0.7)/(1k + \frac{87.2k}{201}) = 0.853\ mA$

$I_C = \alpha I_E = \frac{200}{201} \times 0.85 = \underline{\underline{0.849\ mA}}$

$V_{OUT} = 15 - 0.847 \times 10 = \underline{\underline{6.51\ V}}$ [8]

b) SSEC:



$r_{be} = \beta/g_m = \frac{\beta V_T}{I_C}$
$= 5.89\ k\Omega$

KVL on i/p side $\Rightarrow$ $V_{in} = i_b r_{be} + i_e R_E = i_b[r_{be} + (1+\beta)R_E]$

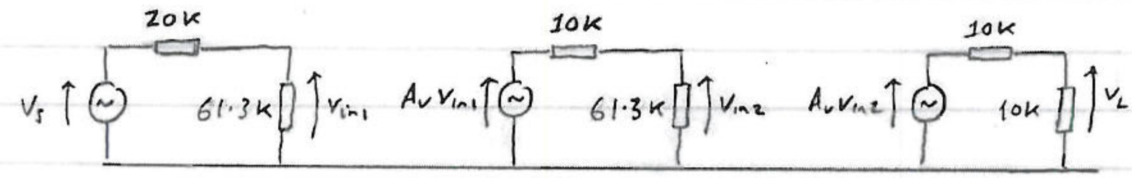
And $V_{out} = -\beta i_b R_C \Rightarrow A_V = \frac{V_{out}}{V_{in}} = -\beta R_C/[r_{be} + (1+\beta)R_E]$

$= -200 \times 10k/206.9k = \underline{\underline{-9.67}}$

$R_i = R_B // (V_{in}/i_b) = 87.2k // 206.9\,k = \underline{\underline{61.3\,k\Omega}}$

$R_o = R_C = \underline{\underline{10k\Omega}}$ [12]

c) Overall SSEC in mid-band:



Working R→L, overall gain is:

$$\frac{V_L}{V_S} = \frac{10k}{10k + 10k} \cdot A_V \cdot \frac{61.3k}{61.3k + 10k} \cdot A_V \cdot \frac{61.3k}{61.3k + 20k}$$

$$= 0.5 \times (-9.67) \times 0.86 \times (-9.67) \times 0.75$$

$$= \underline{\underline{+30.3}}$$ [10]

3 a) Neglecting current in bias network, drain currents are equal. With both MOSFETs active, this implies:

$$K_1 (V_{G1} - V_{t1})^2 = K_2 (0 - V_{t2})^2$$

Taking $\sqrt{\ }$ both sides, with +ve signs (both FETs above threshold)

$$V_{G1} - V_{t1} = \sqrt{K_2/K_1}\,(-V_{t2}) \quad \text{--- ①}$$

But bias network ensures $V_{OUT} = (1 + R_{G1}/R_{G2}) V_{G1}$ ②

① & ② $\Rightarrow$ $V_{OUT} = (1 + R_{G1}/R_{G2}) \cdot (V_{t1} - \sqrt{K_2/K_1}\, V_{t2})$ as req.

With $K_1 = 4K_2$, $V_{t1} = 1V$, $V_{t2} = -1V$, $V_{OUT} = 5V$ we have

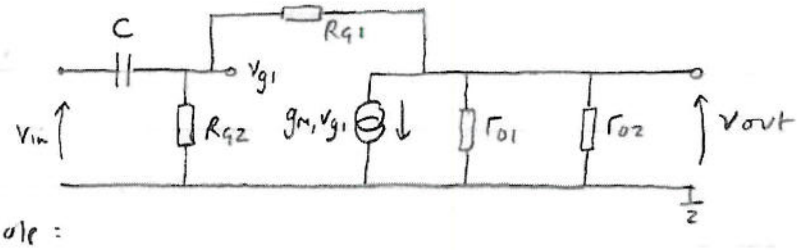
$5 = (1 + R_{G1}/R_{G2}) \cdot (3/2) \Rightarrow R_{G1} = 7/3 \cdot R_{G2} = \underline{\underline{2.33\ M\Omega}}$

Q1 has $V_{GS} = 3/2\ V$, $V_t = 1V$, $V_{DS} = 5V \Rightarrow V_{DS} > V_{GS} - V_t$ ∴ ACTIVE

Q2 has $V_{GS} = 0$, $V_t = -1V$, $V_{DS} = 5V \Rightarrow$ " "

$I_D = I_{DSS2} = K_2 V_{t2}^2 = 0.1m \times (-1)^2 = \underline{\underline{0.1\ mA}}$ [10]

b) SSEC:



KCL @ o/p:

$$g_{m1} v_{g1} + v_{out}/r_{o1} + v_{out}/r_{o2} + (v_{out} - v_{g1})/R_{G1} = 0$$

and $v_{g1} = v_{in}$ in mid-band

$$\Rightarrow \quad A_V = v_{out}/v_{in} = -\left(g_{m1} - \frac{1}{R_{G1}}\right) \cdot (r_{o1} \,\|\, r_{o2} \,\|\, R_{G1})$$

$g_{m1} = 2\sqrt{K_1 I_D} = 0.4\ mA/V$, $r_{o1} = r_{o2} = V_A/I_D = 800\ k\Omega$

$$A_V = -\left(4\times10^{-4} - \frac{1}{2.33M}\right) \cdot (800k \,\|\, 800k \,\|\, 2.33M) = \underline{\underline{-137}}$$

Current in R_{G1} is $i_{RG1} = (v_{in} - v_{out})/R_{G1} = v_{in}(1 - A_V)/R_{G1}$

$\Rightarrow R_{G1}$ presents an input resistance of $R_{G1}' = R_{G1}/(1 - A_V)$

and overall i/p resistance is $R_i = R_{G2} \,\|\, \frac{R_i}{1 - A_V} = 1M \,\|\, 16.9k = \underline{\underline{16.6\ k\Omega}}$

Cut-off frequency given by $\omega R_i C = 1$.

Putting $R_i = 16.6k$, $\omega = 2\pi \times 20 \Rightarrow \underline{\underline{C = 480\ nF}}$ [16]

c) Body effect is modulation of channel conductivity due to variations in voltage between source and substrate (= body). In NMOS body is common to all devices and at signal ground. For cct in Fig 3, modulation of Q2's channel due to signal voltage between body (ground) and source (V_{out}) significantly lowers o/p resistance and hence voltage gain. [4]

4 a) Class A : No cross-over distortion, but high power dissipation
Class B : Low power, but with severe distortion at cross-over
Class AB : Good compromise, with slightly higher power than Class B but much lower distortion [6]

b) Because the cct is symmetrical, and the transistors are matched, we know that $V_{OUT} = 0$ when $V_{IN} = 0$.
It follows that all four transistors have the same V_{BE}, and hence the same I_C.
Ignoring base currents, I_{C1} = current in upper $10k\Omega$ resistor. Assuming $V_{BE1} \sim 0.7V$, this gives

$$I_C \simeq (15 - 0.7)/10k = \underline{1.43\ mA}$$

At maximum output current, $I_{C1} \to 0$. If $V_{OUT} = 10V$ then we have $I_{B3} = (15 - 10 - 0.7)/10k = 430\ \mu A$
and $I_{LOAD} = (1+\beta)\, I_{B3} = 201 \times 430\mu A = \underline{\underline{86\ mA}}$ [12]

c) When $V_{OUT} = +10V$ with $500\ \Omega$ load, $I_{E3} \simeq 20\ mA$
$\Rightarrow I_{B3} = I_{E3}/1+\beta = 100\ \mu A$ and $V_{BE3} = V_T \ln(I_{C3}/I_S)$
with $V_T = 25mV$, $I_S = 5 \times 10^{-14}\ A$ $\Rightarrow$ $V_{BE3} = 668\ mV$
So, $V_{B3} = 10 + 0.668 = \underline{\underline{10.668\ V}}$
Now, $I_{E1} = (15 - 10.668)/10k - I_{B3} = 333\ \mu A$
$\Rightarrow V_{BE1} = -V_T \ln(I_{C1}/I_S) = -565\ mV$

$\Rightarrow V_{IN} = V_{B3} + V_{BE1} = 10.668 - 0.565 = \underline{\underline{10.103\ V}}$
Ignoring the base current of Q4, the emitter current of Q2 is: $I_{E2} \simeq (10.103 - 0.7 - (-15))/10k = 2.44\ mA$
$\Rightarrow V_{BE2} = V_T \ln(I_{C2}/I_S) \simeq 615\ mV$
$\Rightarrow V_{B4} \simeq 10.103 - 0.615 = 9.488\ V$
$\Rightarrow V_{BE4} \simeq 9.488 - 10 = -512\ mV$
and the collector current in Q4 at this V_{BE} would be $I_{C4} = I_S \exp\left(\frac{512\ mV}{V_T}\right) = 40\ \mu A$ ie small [12]