

1. (a) The circuit shown in Figure 1.1 is a single-stage inverting voltage amplifier using two CMOS FETs. Write a simple SPICE programme which will compute a small signal gain and phase frequency response analysis of the circuit over the frequency range 10 kHz to 10 MHz. The .OPTIONS card and the transistor model process parameters QP and QN are already built into the SPICE Library. [6]
- (b) Sketch and label typical phase and gain characteristics of the amplifier. What effect does cascoding have on amplifier performance in particular amplifier phase margin. [6]
- (c) What is the function of the passive components C_1 , R_1 and R_2 shown on the circuit? [4]

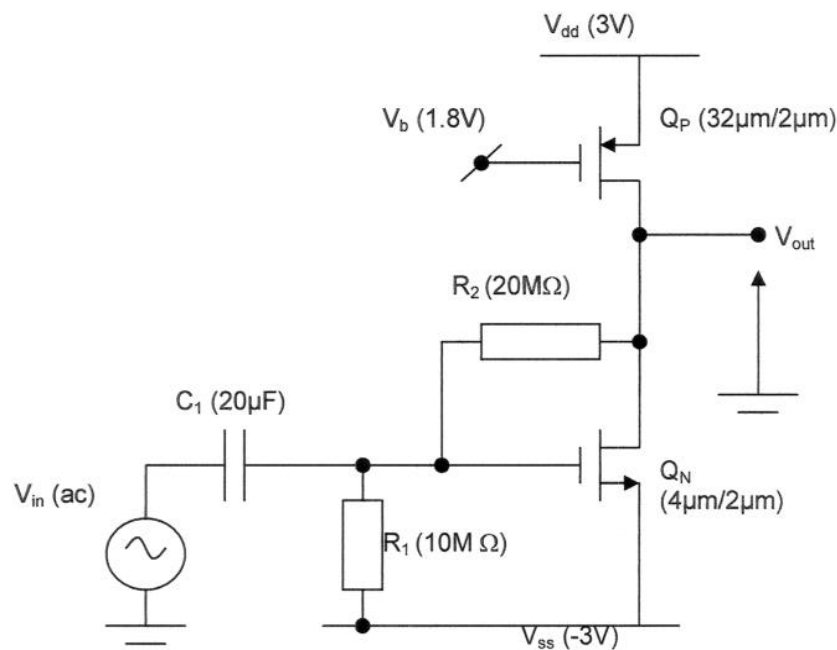


Figure 1.1

- d) In practice voltage reference V_b is provided by an on-chip voltage reference circuit similar to the one shown in Figure 1.2. Explain qualitatively why such a four transistor reference circuit can have smaller chip area than an equivalent two transistor circuit with the same power consumption

[4]

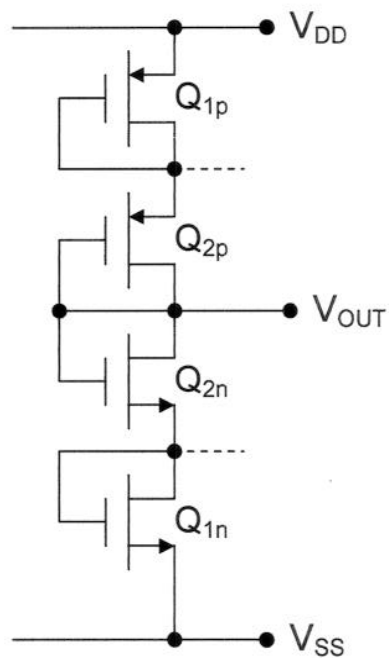


Figure 1.2

2. (a) Voltage and current-sources are key components in analogue circuit design. Sketch a typical band-gap voltage reference circuit and prove that the temperature coefficient of the output voltage V_o is zero if $V_o = 1.283$ V. Assume the temperature coefficient of V_{BE} to be $-2.5\text{mV}/^\circ\text{C}$, Boltzmann's constant $k = 1.38 \times 10^{-23} \text{ J/K}$ and electron charge $q = 1.6 \times 10^{-19} \text{ C}$.

[11]

- (b) Calculate the fractional temperature coefficient for the constant current generator of Figure 2 at room temperature, given that R is a polysilicon resistor with a temperature coefficient of $1500 \text{ ppm}/^\circ\text{C}$. What is the function of the four diodes ?

[5]

- (c) Explain why transistor Q_2 in figure 2 has two emitters and also why the output current I_o is directly proportional to absolute temperature.

[4]

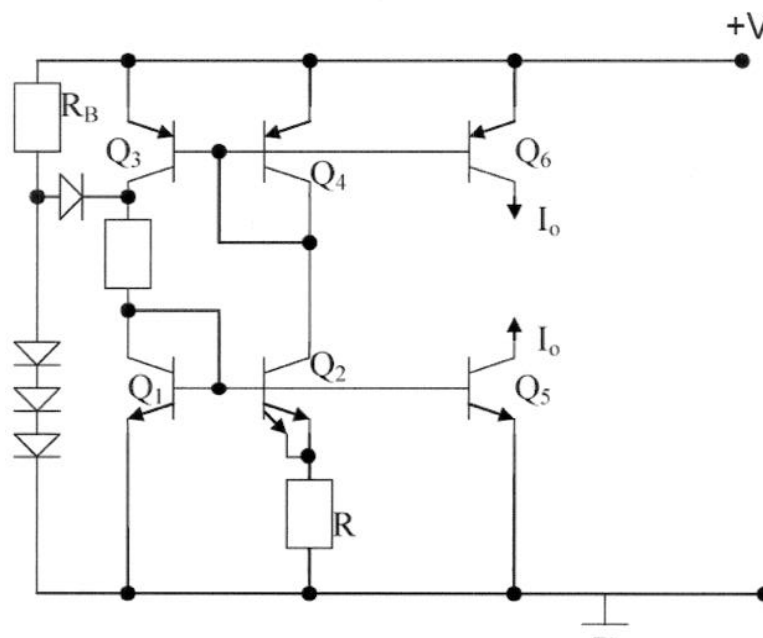


Figure 2

3. (a) Sketch a typical circuit diagram for a single-stage fully differential folded cascode CMOS op-amp. Why is the folded cascode op-amp regarded as a single stage design? Finally briefly explain the concept of common-mode feedback with reference to your folded cascode op-amp.

[8]

- (b) Estimate the low-frequency differential voltage gain, slew rate and gain-bandwidth product of the two-stage CMOS op-amp shown in Figure 3.1. Aspect ratios of all devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below.

[10]

- (c) Explain qualitatively why the addition of a resistor in series with compensation capacitor C_c improves amplifier stability.

[2]

CMOS TRANSISTOR PARAMETERS

MODEL PARAMETERS	K_p ($\mu\text{A}/\text{V}^2$)	λ (V^{-1})	V_{T0} (V)
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

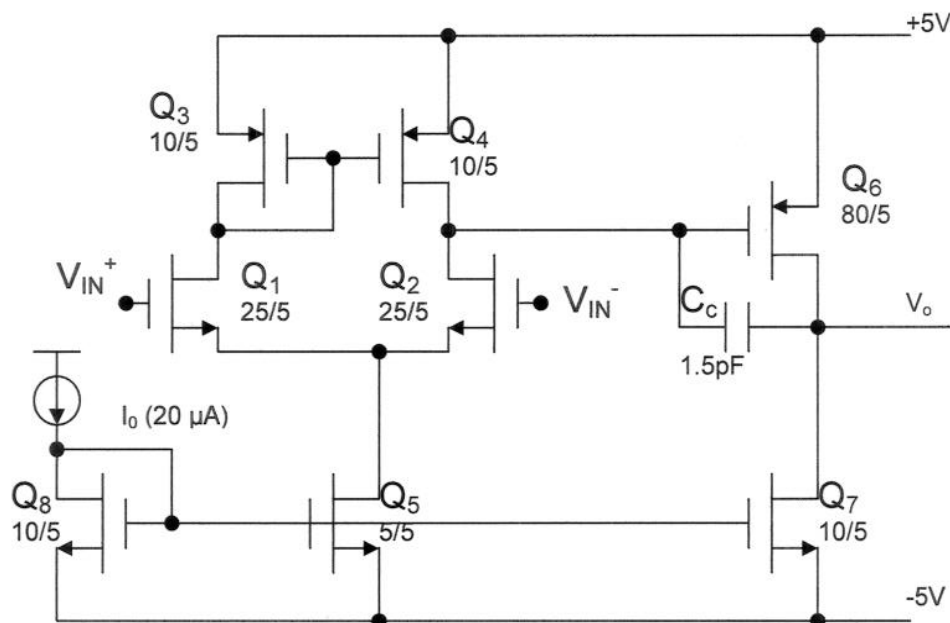


Figure 3.1

4. (a) Under what operating conditions does the MOSFET of Figure 4.1 realise a linear floating resistor between terminals A and B? Show that under these conditions the equivalent resistance R_{AB} can be approximated by

$$R_{AB} = \frac{L}{KW(V_{GS} - V_T)}$$

stating any assumptions. All symbols have their usual meaning.

[6]

- (b) Discuss three sources of non-linearity in the single MOSFET resistor realisation of Figure 4.1 and suggest one suitable circuit design to help eliminate one or more of these non-linear terms. Show all necessary circuit analysis to confirm your design.

[6]

- (c) Figure 4.2 shows a fully differential continuous time integrator using a balanced double differential linear active transresistor. Derive an expression for the time constant of the integrator. You may ignore all bulk effects, and assume all MOSFETs are operating in the triode region.

[8]

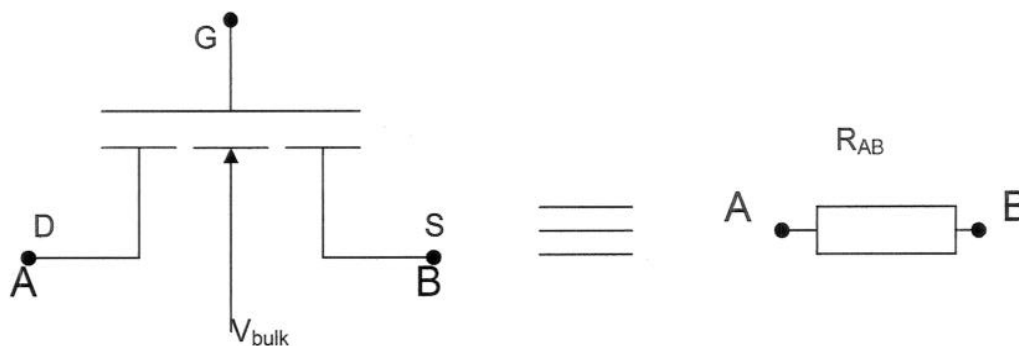


Figure 4.1

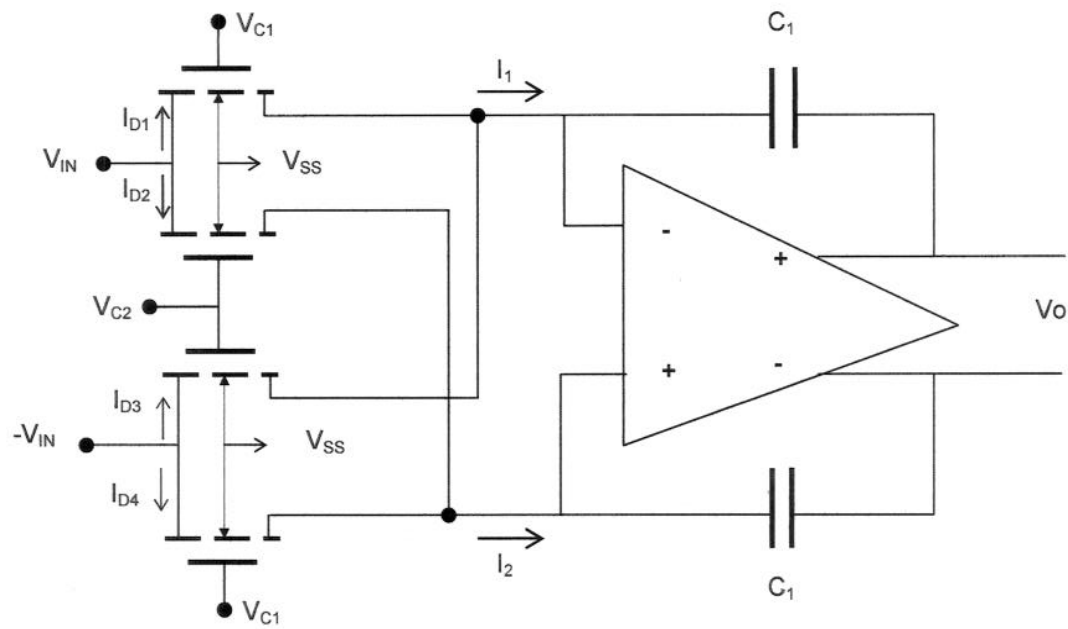


Figure 4.2

5. (a) Sketch circuits for both a Lossy and differential switched-capacitor integrator and derive an expression for the transfer function of each implementing switches by MOSFETs of equal size and assuming that the integrators are driven by non-overlapping clocks with a clock frequency much higher than the maximum input signal frequency. Also assume the switches are ideal.

[10]

- (b) Figure 5.1 shows one section of a switched capacitor ladder filter. Based on this filter structure, design a 3rd-order Chebyshev low-pass filter with a cut-off frequency of 5 kHz and a 1.0 dB pass band ripple. Assume a clock frequency of 100 kHz. Passive component values for the LC prototype, normalised to 1 rad/s, are $C_1 = C_3 = 2.0236$, $L_2 = 0.994$. In your analysis assume all integrators to be lossless.

[10]

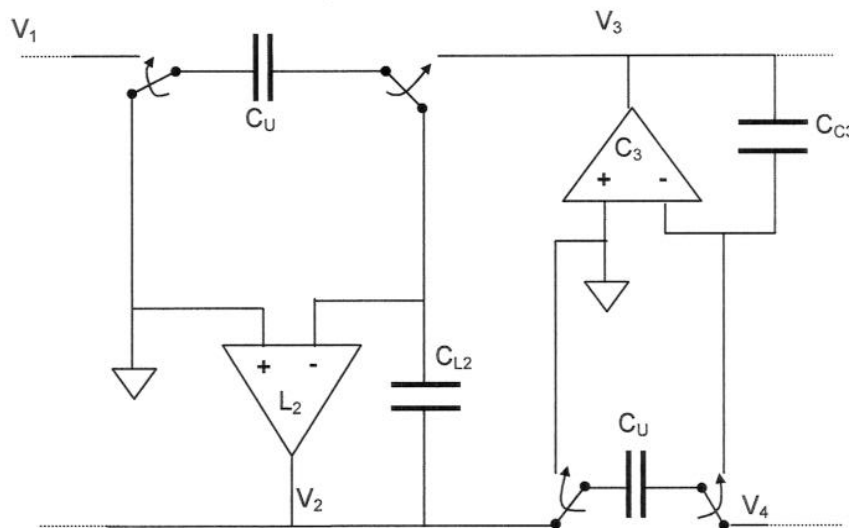


Figure 5.1

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6. (a) Give one advantage and one disadvantage of each of the three CMOS current mirror circuits shown in Figures 6.1, 6.2 and 6.3. [6]
- (b) For the current mirror of Figure 6.2 derive the voltage swing in terms of device threshold voltage V_T , clearly stating any assumptions you make. [7]
- (c) With the aid of a macromodel, explain the theoretical concept of current feedback and how it results in constant bandwidth application. [7]

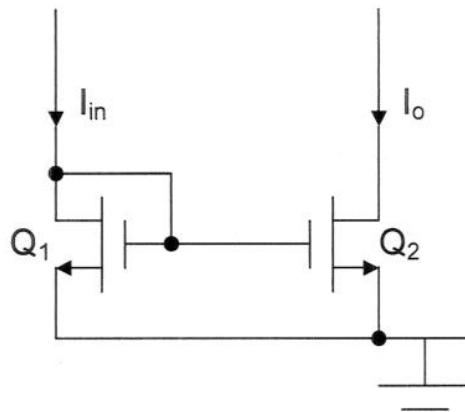


Figure 6.1

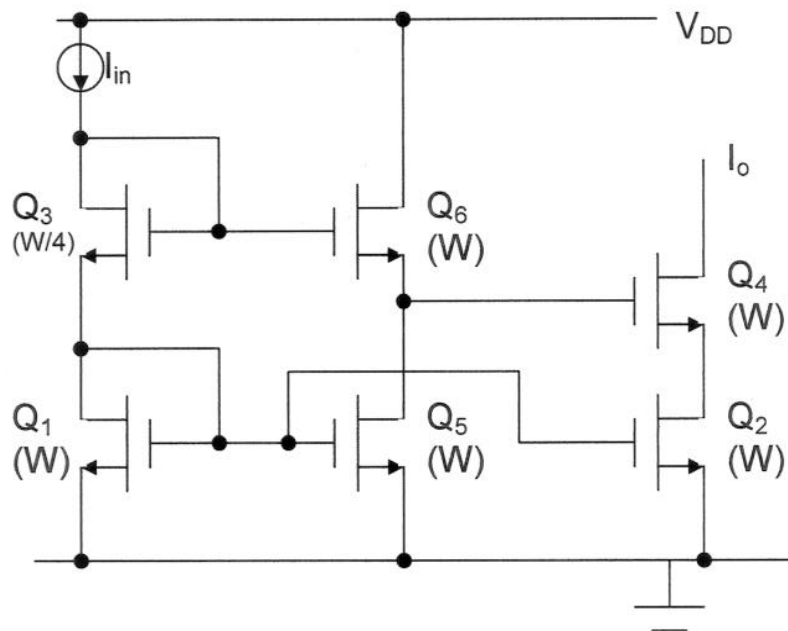


Figure 6.2

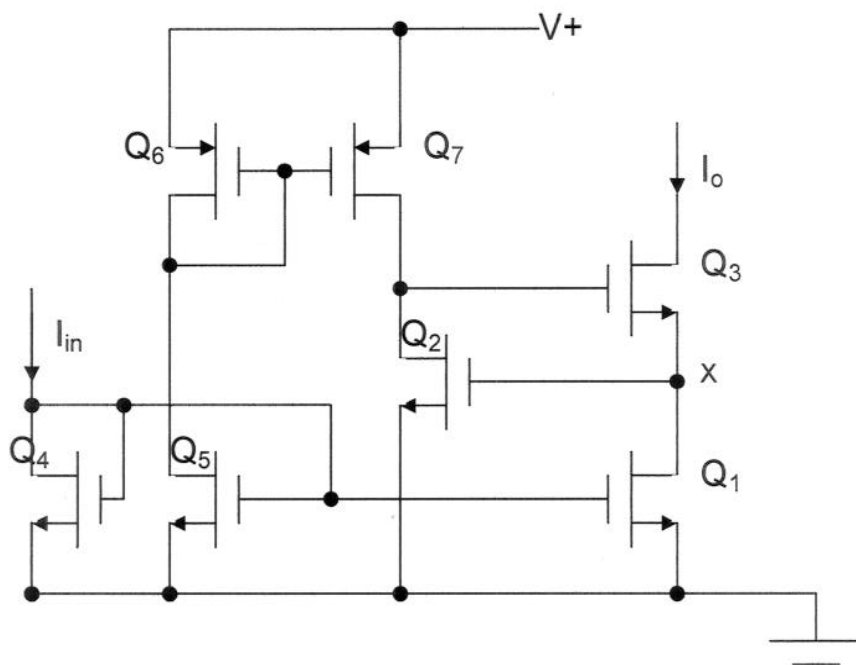


Figure 6.3

2007 Exam.

E3.01/AC1

original.

3rd Year / Msc

Analogue Integrated Circuits
or Systems

E3.01/AC1

SOLUTIONS

1st Marker

C. Toumazou

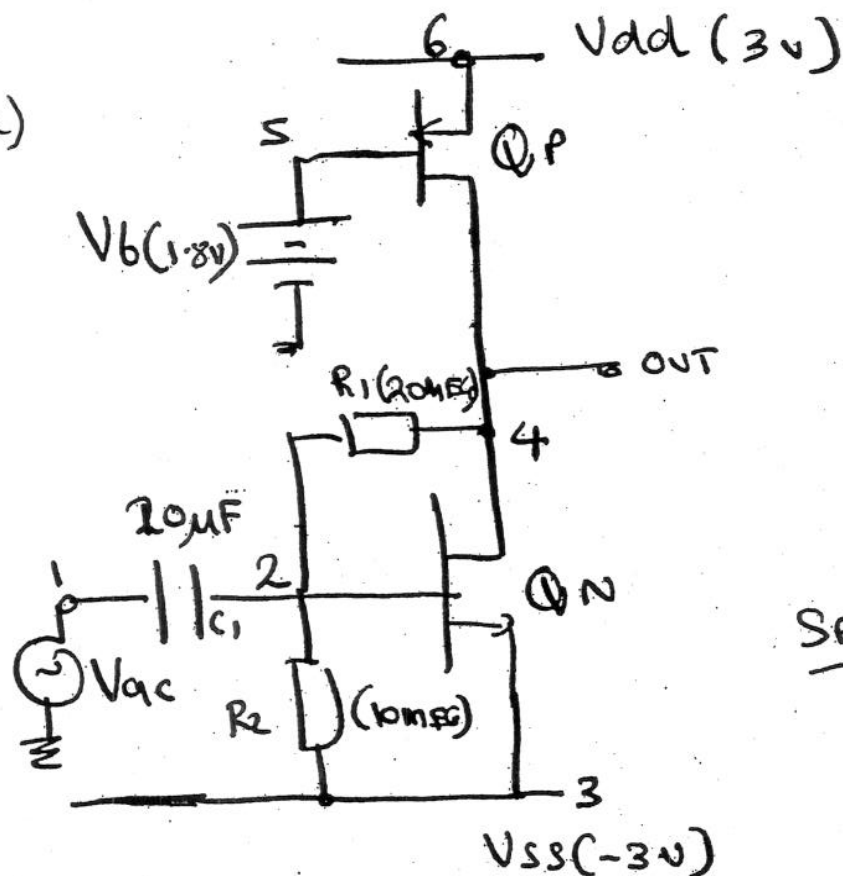
2nd Marker

D. Haigh

Q1

①
21

a)

SPICE NETLIST

• Title inverting CMOS Amplifier.

Component Netlist {

C1	1	2	20 E-6		
R1	2	4	20 MEG		
R2	2	3	10 MEG		
M1	4	2	3	QN	W=4u L=2u
M2	4	5	6	QP	W=32u L=2u
Vdd	6	0	3V		
Vss	3	0	-3V		
Vb	5	0	1.8V		
Vac	1	0	ac 1		

} sources

• model QN, QP
 • op all
 • option post
 • ac dec 10% 10K 10MEG
 • PRINT ac VdB(4)
 • PRINT ac VP(4)
 • END.

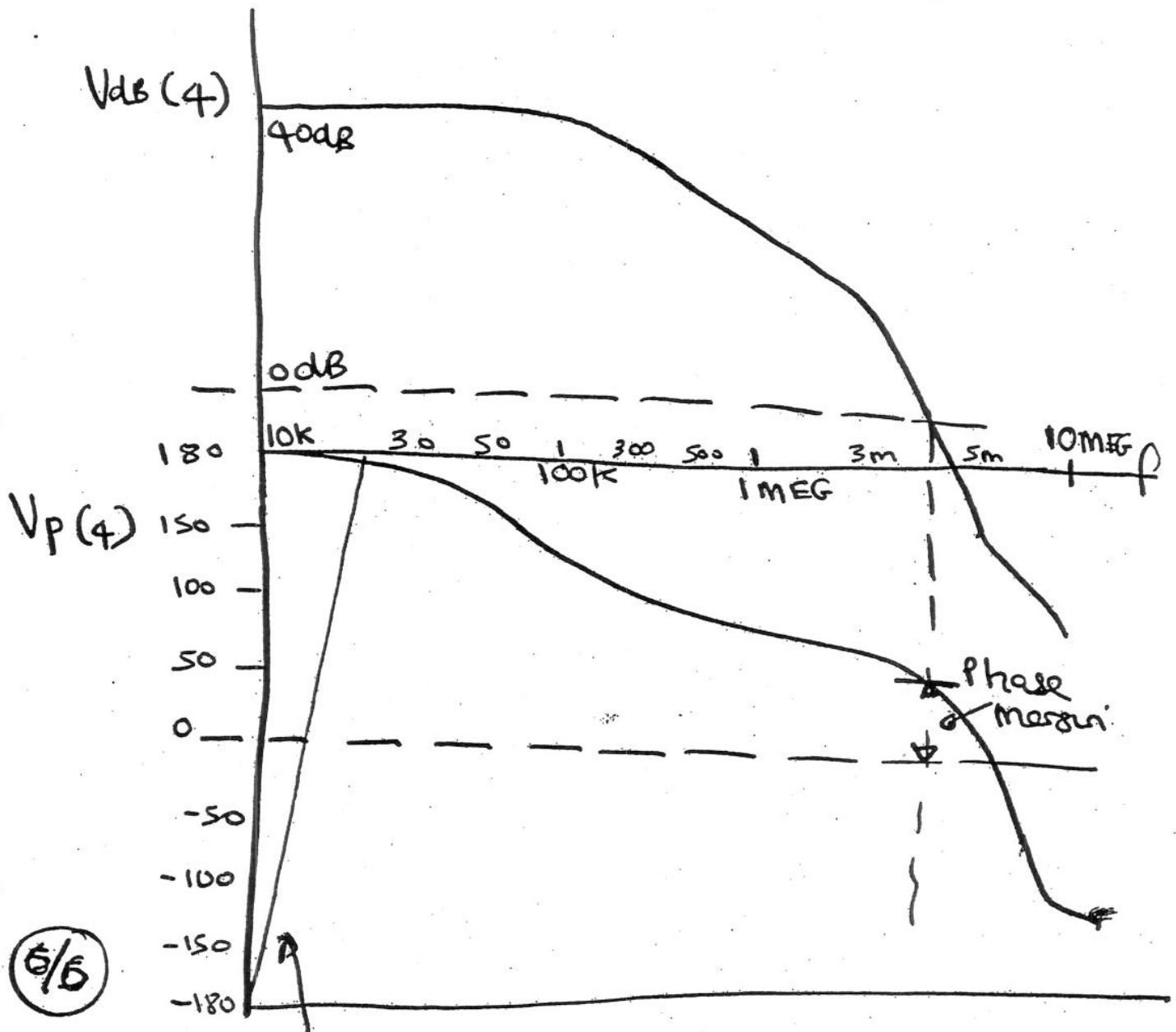
} Analysis Print

6/6

CT

Typical SPICE output Plot.

(2)



Autoscaling in SPICE

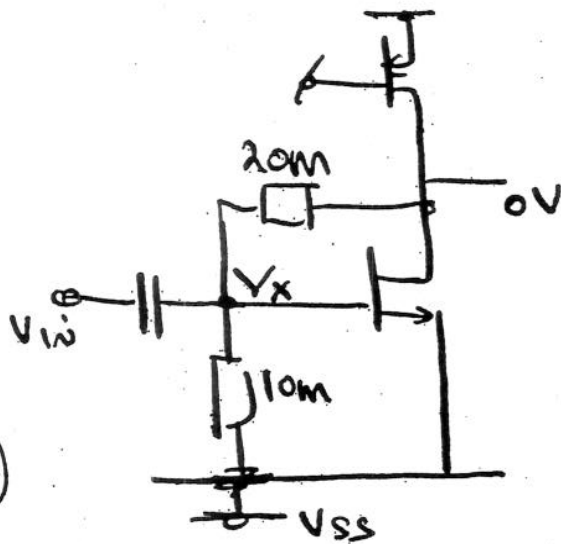
Likely that theory and Simulated will differ because of approximations generally assumed in theory. Models for transistors in SPICE have inaccuracy. Also inaccuracy in parameter extraction for SPICE models.

Cascoding will increase amplifier gain but will compromise phase margin due to added capacitance at output.

Q1 (cont.)

3

Large Passive Components used for DC biasing. Sets high impedance output of amplifier at DC bias close to 0V. Large values of R used so that input and output impedance levels are not loaded. 10μF capacitor used to AC couple input. Typically



$$V_x = V_{ss} + \left(\frac{-V_{ss}}{3} \right)^2$$

$$= \left[\frac{V_{ss}}{3} \right]$$

4/4

CT

Figure Q1 d)

Q1 cont

(4)

$$\text{Since } I \approx \frac{KW}{2L} (V_{GS} - V_T)^2$$

then if V_{GS} is small $\approx V_T$

then (W/L) large.

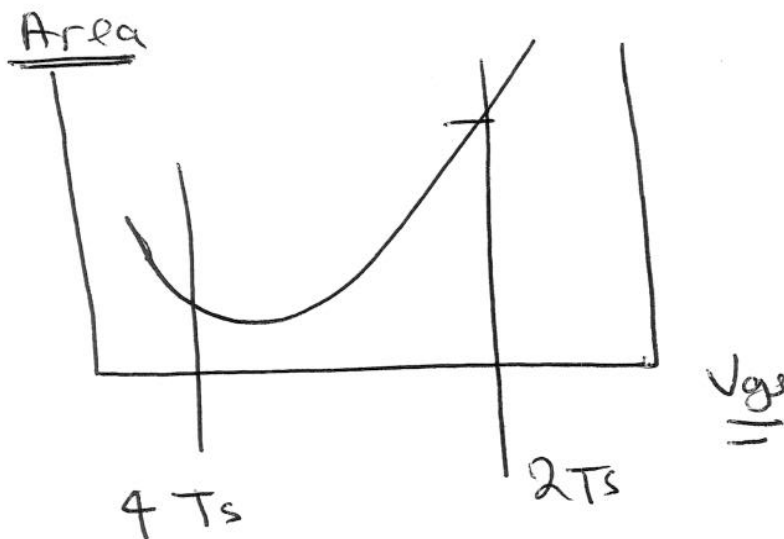
if $V_{GS} \gg V_T$, then (W/L) small

small (W/L) gives large chip area

\therefore Two transistor PD has

larger V_{GS} / transistor than

one transistor PD for same supply

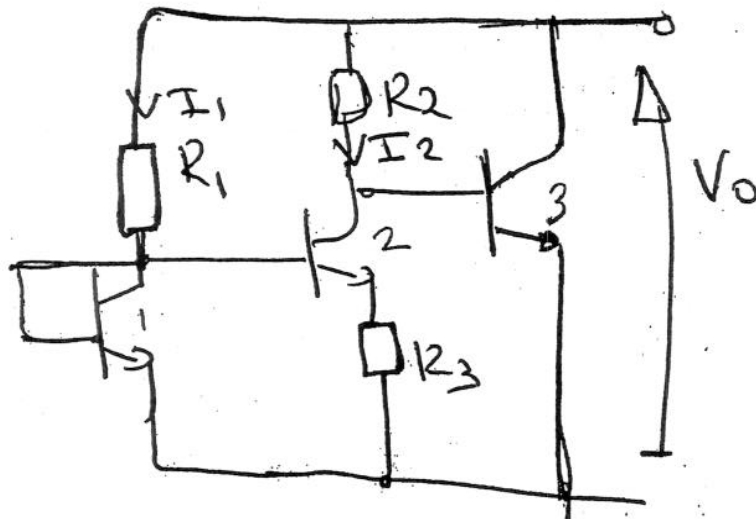


(4/4)

Ans 2

5

Q2



$$V_{BE1} = V_{BE2} + I_2 R_3$$

$$\beta \gg 1$$

Since $V_{BE1} - V_{BE2} = V_T \ln(I_1/I_2)$
 Then $V_0 = V_{BE3} + R_2/R_3 V_T \ln(I_1/I_2)$
 $V_T \ln(I_3/I_3) \rightarrow \text{assume}$
 Now - temp

for $dV_0/dT = 0$, then dV_{BE3}/dT
 $= \frac{V_T}{T} \frac{R_2}{R_3} \ln\left(\frac{I_1}{I_2}\right)$

Since $\frac{dV_{BE}}{dT} = -2.5 \text{ mV}/^\circ\text{C}$, $\frac{V_T}{T} = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}}$

Then $\left(\frac{R_2}{R_3}\right) \ln\left(\frac{I_1}{I_2}\right) = 29$ and so

$$V_0 = 1.283 \text{ V}$$

6/6

b) For PTAT temperature coefficient of V_T cancels with negative temp coefficient of Resistor

Ct

Q2 cont

(6)

$$T_{CF} = \frac{1}{V_T} \frac{\partial V_T}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T}$$

$$= \frac{1}{T} - 1500 \times 10^{-6} \text{ @ Room T}$$

$$= 1833 \text{ ppm}/^\circ\text{C}$$

(3/3)

The diodes are part of a start-up circuit which will conduct when the PTAT is in its 'zero' operating state

TOTAL
(20/20)

An injection of current is provided by R_B which starts-up the current switching off the diode connected to the collector of Q_3 .

(2/2)

(4/4)

c). since $I_0 = \frac{(V_{be1} - V_{be2})}{R}$ Prop to temperature

$$\approx \frac{V_T}{R} \ln \left[\frac{I_1}{I_0} \frac{I_{s2}}{I_{s1}} \right] \approx \frac{V_T}{R} \ln 2$$

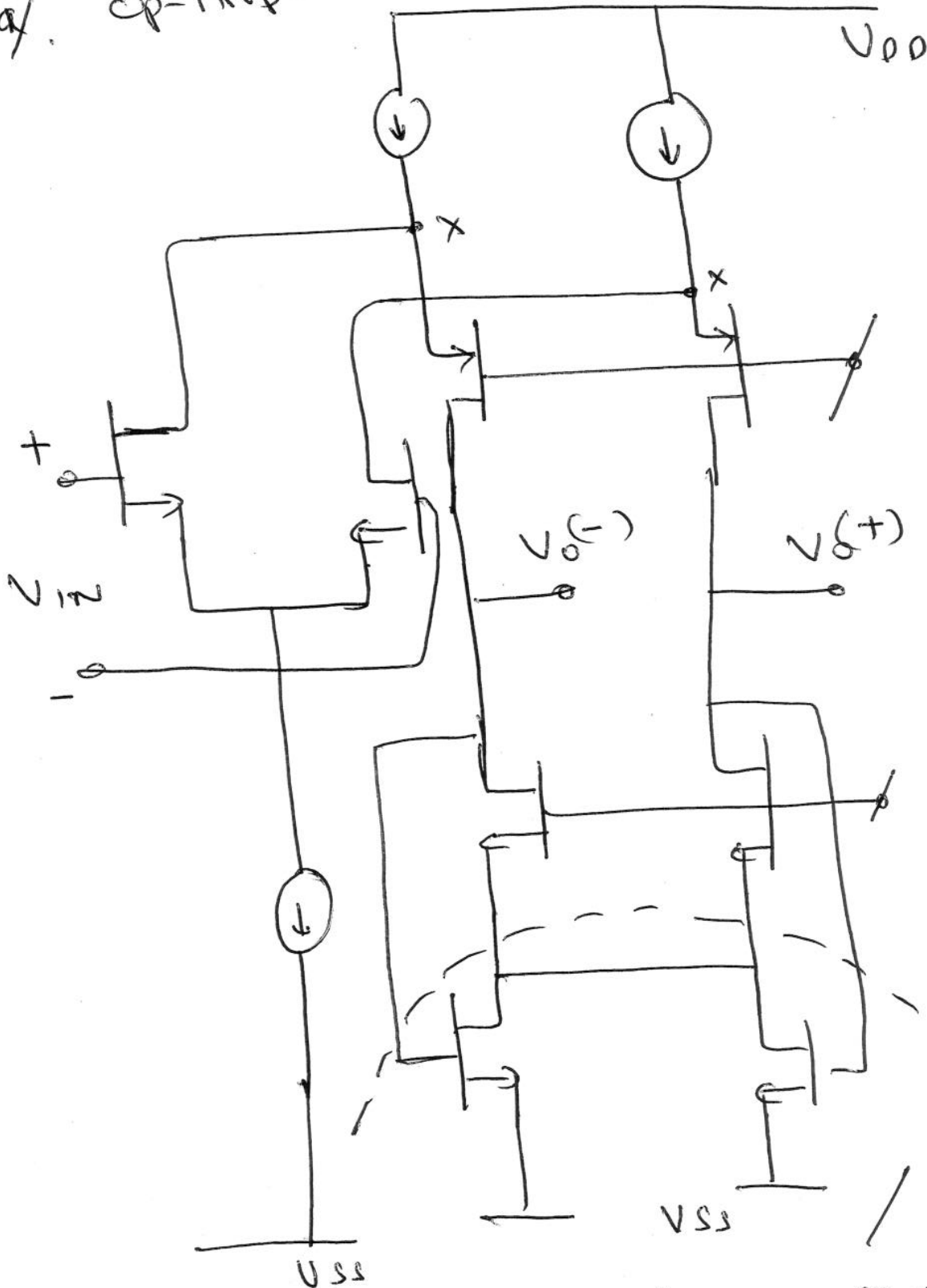
If $I_{s2} = I_{s1}$,
and $I_0 = I_1$ then $I_0 \approx 0$ Important for $I_{s2}/I_{s1} = n = 2$ in this case.

Q43

7

Architecture of folded-cascode

a/. op-Amp.



$$A \approx \left(\frac{1}{2}\right) \left(\frac{g_m}{g_{o1}}\right)^2$$

Common-mode feedback.

(T

4

Qn 3 cont

⑧

Single-stage because one current path from input to output.

Node X is low impedance and so very small voltage swing is generated. Only high impedance

node is at the output. (2)
Not necessary to pole split since dominant pole at output not two stages.

Diff output op-amps with high gain have no way of stabilisation since outputs are undefined (voltage that is).

Common-mode feedback - senses

common-mode output and via negative feedback controls the current through the output stage to ensure stable quiescent operating point. Circuit shown in the figure. (2)

b/. OP-Amp

$$\textcircled{2/2} \quad A_{v1} = -g_{m2} / (g_{o2} + g_{o4})$$

$$(g_{o2} + g_{o4}) = I_{D2} (\lambda_n + \lambda_p) \\ = 5 \times 10^{-6} \times 0.05 = 2.5 \times 10^{-7} \text{ s}^{-1}$$

$$g_{m2} = 2 \sqrt{\beta_2 I_D} \Rightarrow \beta_2 = \frac{k_n}{2} \left(\frac{W}{L} \right)_2$$

$$\beta_2 = 7.5 \times 10^{-5} \text{ A/V}$$

$$\therefore g_{m2} = 3.87 \times 10^{-5} \text{ s}$$

$$\textcircled{2/2} \quad A_1 = \underline{\underline{-154.9}}$$

$$A_2 = -g_{m6} / (g_{o7} + g_{o6})$$

$$(g_{o6} + g_{o7}) = I_{D6} (\lambda_{np} + \lambda_n) \\ = 20 \times 10^{-6} \times 0.05 \\ = 10 \times 10^{-7} \text{ s}^{-1}$$

$$\textcircled{2/1} \quad g_{m6} = 1.13 \times 10^{-4}, \quad A_2 = -113. \\ A_T = A_1 A_2 = 17503$$

Q3 cont

10

$$G.B_p = \frac{g_{m2}}{2\pi C_c} = 4.1 \text{ MHz} \quad - (2)$$

$$S.R = I_0 / C_c = \left(\frac{1.0}{1.5} \right) \text{ V}/\mu\text{s} \quad - (2)$$

— Total 10/10

——/——

c. Introduce R in series with C_c \times



provides feedforward compensation and eliminates RHP Zero in the op-amp's transfer function.

Zero is given by $Z = - - g_{m6} / C_c$ with R

$$Z = - \frac{1}{(1/g_{m6} - R) C_c} \quad \text{Improves } \phi$$

by setting $Z = P_2 = 2nd \text{ pole}$ with R .

(2/2)

(T

Q4

a. Assumption is that if $(V_{DS} \geq 0)$ or $(V_{DS} < (V_{GS} - V_T))$ device acts in linear region. From

$$I_D = \frac{\kappa W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] (1 + \lambda V_{DS})$$

for $V_{DS} < (V_{GS} - V_T)$, then $\lambda V_{DS} \ll 1$

$$\text{So } I_D = \frac{\kappa W}{L} (V_{GS} - V_T) V_{DS}$$

6/6

$$\text{OR } R_{AB} = V_{DS} / I_D = L / (\kappa W (V_{GS} - V_T))$$

b) Three sources of non-linearity

(i) limited due to V_{BS} changing V_T for negative V_{DS} due to body effect.
ie. $V_T = V_{T0} + \gamma \left[\sqrt{-V_{BS} + 2\phi_F} - \sqrt{2\phi_F} \right]$
 γ = bulk threshold parameter
 ϕ_F = Fermi-level potential

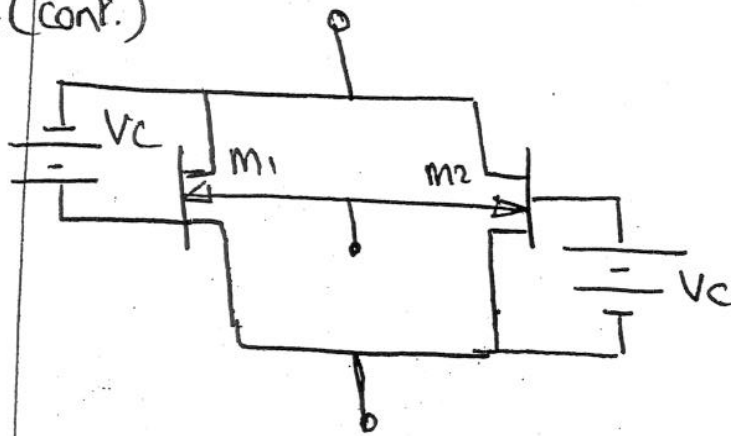
(ii) limited due to V_{DS} approaching $(V_{GS} - V_T)$ hence saturation region for large positive V_{DS} .

(iii) For large values of V_{DS} the $V_{DS}^2/2$ term comes in making the results quite non-linear.

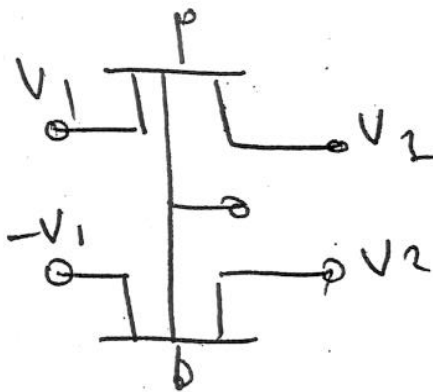
4/4

Q4 (cont.)

12

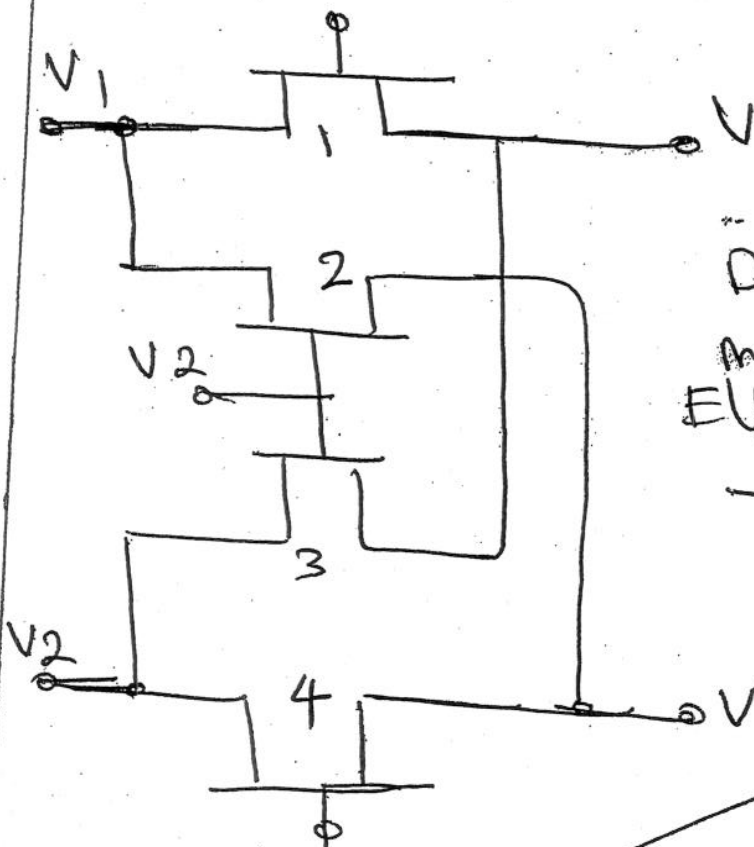


Parallel circuit - eliminates $V_{ds}^2/2$ term.



Differential scheme

Effects of V_{ds} cancelled.



Double differential
mos.
Eliminates
- V_{ds} and V_T
term.

Any one
of these
will do!

2/2

Q4 (cont)

(13)

Double differential integrals

$$I_{D1} = 2\beta [(V_{C1} - V - V_T)(V_1 - V) - \frac{1}{2}(V_1 - V)^2]$$

$$I_{D2} = 2\beta [(V_{C2} - V - V_T)(V_1 - V) - \frac{1}{2}(V_1 - V)^2]$$

$$I_{D3} = 2\beta [(V_{C2} - V - V_T)(V_2 - V) - \frac{1}{2}(V_2 - V)^2]$$

$$I_{D4} = 2\beta [(V_{C1} - V - V_T)(V_2 - V) - \frac{1}{2}(V_2 - V)^2]$$

Expanding it can be shown that:-

$$(V_1 - V_2)(I_1 - I_2) = \frac{1}{2}\beta(V_{C1} - V_{C2}) = R$$

Independent of both V_T and V_{DS} terms

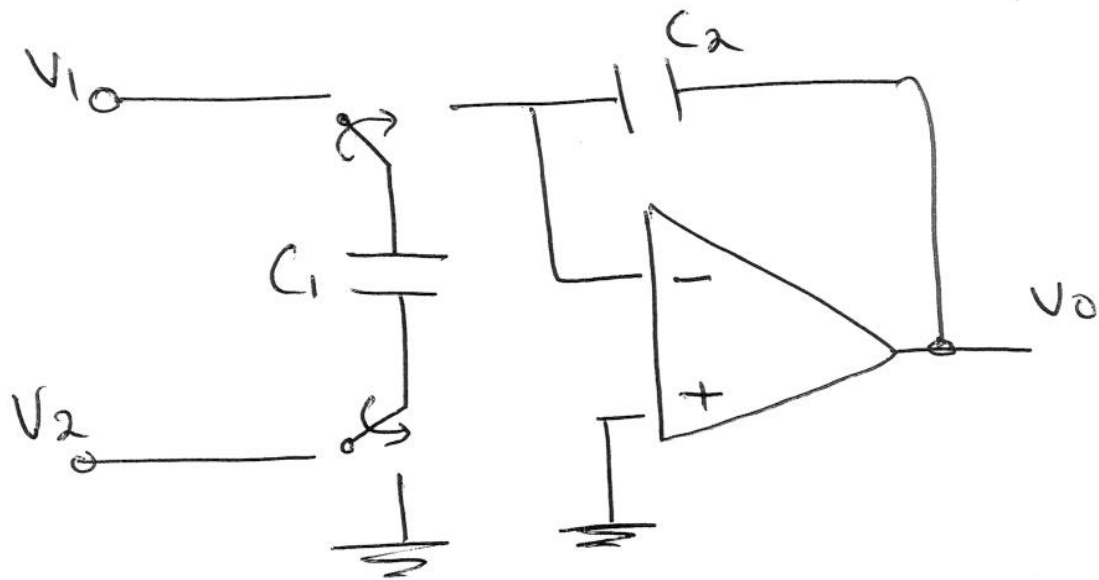
$$\text{Hence } N = \frac{2CR}{1} = \left[\frac{C}{\beta(V_{C1} - V_{C2})} \right]$$

(8/8)

—————//—————

Qus/.

a) Differential Integrator



During ϕ_1 $Q = C_1 [V_1 - V_2]$

$$I_{av} = f_c C_1 [V_1 - V_2]$$

f_c = clock frequency

During $\phi_2 \Rightarrow I_{av} = -f_c (V_1 - V_2) C_1$

$$\therefore V_0 = \frac{-1}{j\omega C_2} f_c C_1 [V_1 - V_2]$$

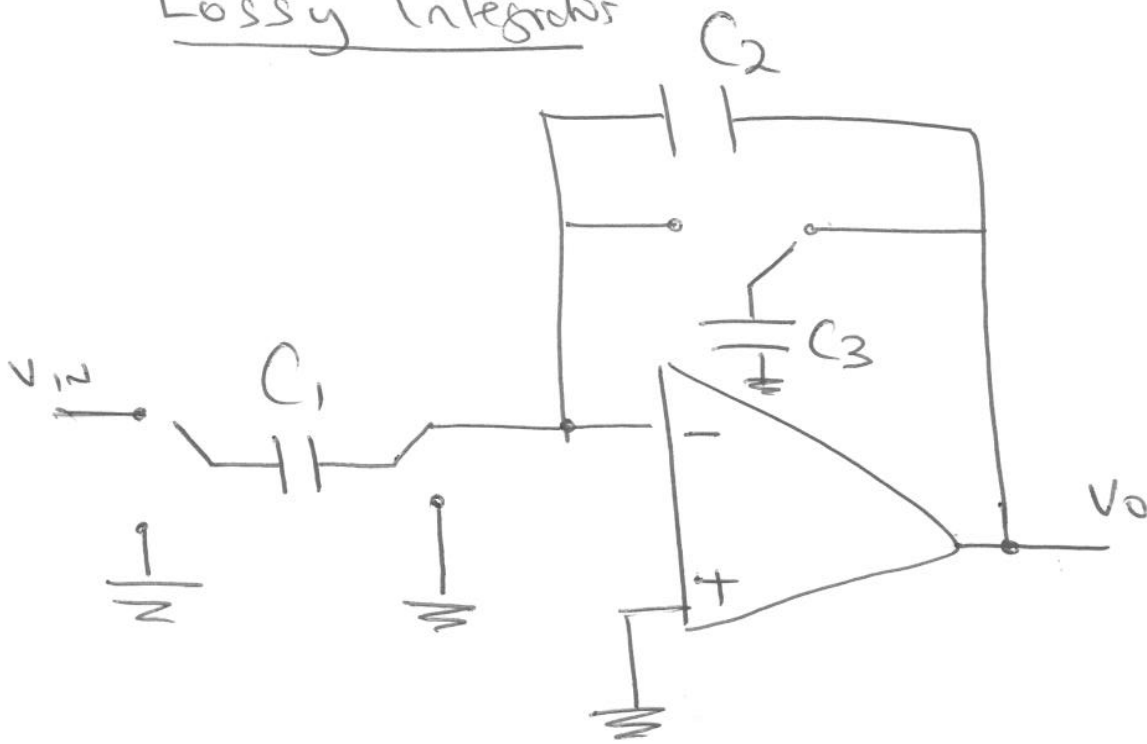
$$\therefore \frac{V_0}{(V_1 - V_2)} = -\frac{f_c}{j\omega} \frac{C_1}{C_2} \approx T = \frac{C_2}{C_1} f_c$$

(5/5)

Qus cont

15

Lossy Integrator



During ϕ_1 $Q = C_1 V_{in} \Rightarrow I_{avg} = f_c C_1 V_{in}$

During ϕ_2

$$I_{avg} = -[f_c (C_3 V_o + j\omega C_2 V_o)]$$

$$\therefore f_c C_1 V_{in} = -[f_c (C_3 V_o + j\omega C_2 V_o)]$$

$$V_{in} = -\left[\frac{C_3 V_o}{C_1} + \frac{j\omega C_2 V_o}{C_1 f_c} \right]$$

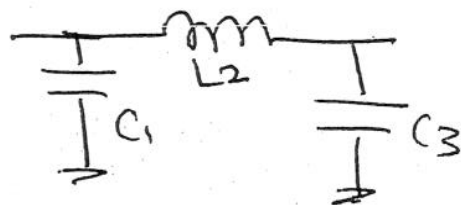
$$\therefore \frac{V_o}{V_{in}} = -\frac{C_1}{C_3} \left(\frac{1}{1 + \frac{C_2 j\omega}{C_3 f_c}} \right)$$

5/5

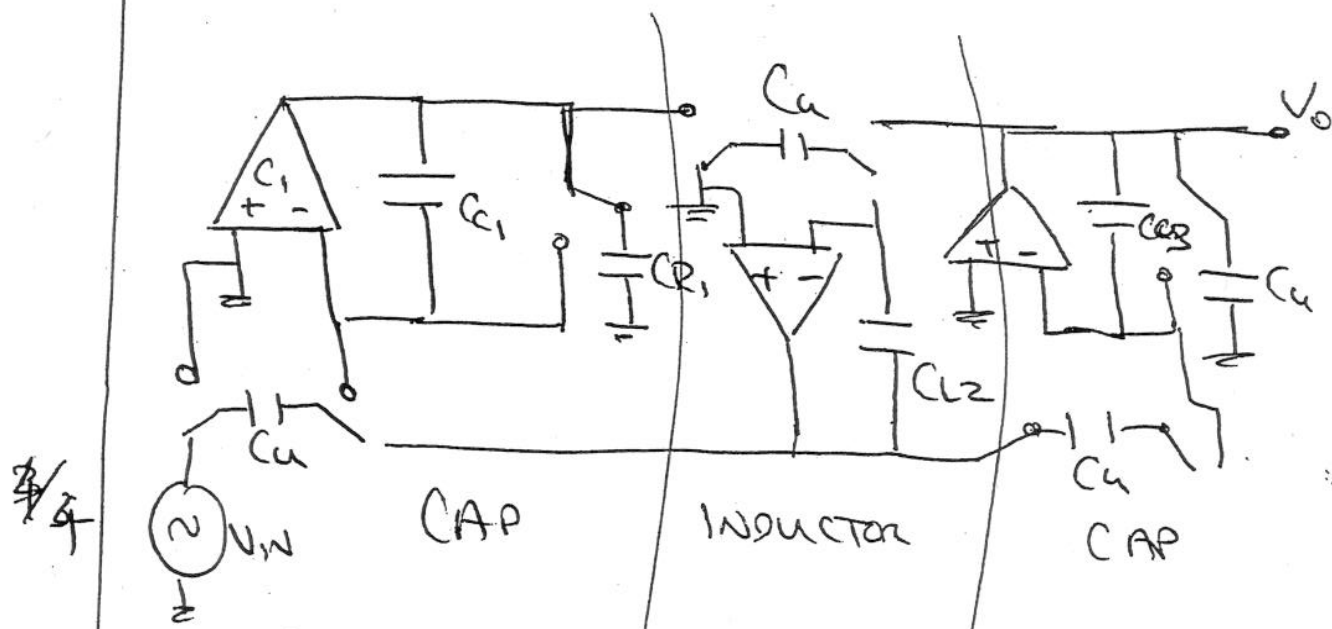
$$\therefore T = \left(\frac{C_2}{C_3} \right) \frac{1}{f_c}$$

Qn 5 Cont
section of LCR prototype.

16



General transformation Rules (not really required but the bright students may include)



Conversion into differential integrator.

Inductor transformation

$$(L_2/R_3)f_c = C_{12}/C_u$$

Capacitor Transformation.

$$C_3/C_u = f_c R_2 C_3$$

where R_2 is normalizing during scaling
resistor. Assuming $R_2 = 1$

$$\left. \begin{aligned} C_1/C_u &= f_c C_1 \\ C_3/C_u &= f_c C_3 \\ C_{12}/C_u &= f_c L_2 \end{aligned} \right\} \text{general transformation}$$

Qus cont

(17)

Table values of C_1 , L_2 and C_3
are normalized to $1 \text{ rad/s} \div 2\pi f_p$

$$f_p = 5 \text{ kHz}$$

$$C_1 = C_3 = 2.0236 / (2\pi 5 \times 10^3) \\ = 6.44 \times 10^{-5} \text{ F}$$

$$C_{L2} = 0.994 / (2\pi 5 \times 10^3) \\ = 3.164 \times 10^{-5} \text{ F}$$

For termination R_s

assume $C_{u1} = C_{R1} = C_{R0} = 1 \text{ pF}$

Then

$$\left[\begin{array}{l} C_{L1} = C_{L3} = 6.44 \text{ pF} \\ C_{L2} = 3.164 \text{ pF} \end{array} \right]$$

(6/6)

Tom (20/20)

Qn 6/.

a)

Fig 6.1 - Simple mirror

Advantages - High frequency
- High output swing

② Disadvantage - very inaccurate

Fig 6.2 - High Swing Cascode

Advantage - Higher output swing than cascode

② Disadvantage - Complex, poor frequency performance.

Figure 6.3 - Regulated Cascode

Advantage - Highest output swing
Highest output resistance

Disadvantage - inaccuracy of input
current - mirror

- feedback leading
to potential instability.

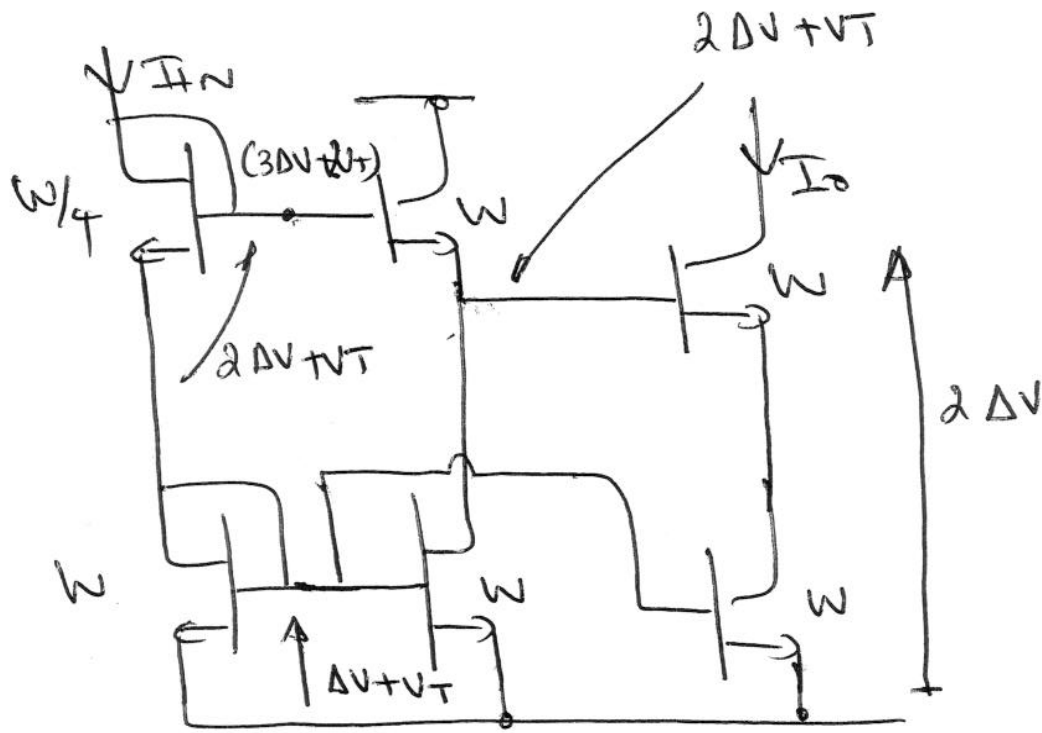
②

6/6

Qn 6 cont

output Swing

Current includes all saturation Voltages



Assuming equal L_s

$$I_0 = I_{12}$$

$$\beta_1 = \beta_2 = \beta_4 \quad \beta_5 = \beta_6 = \beta$$

$$\beta_3 = \beta/4$$

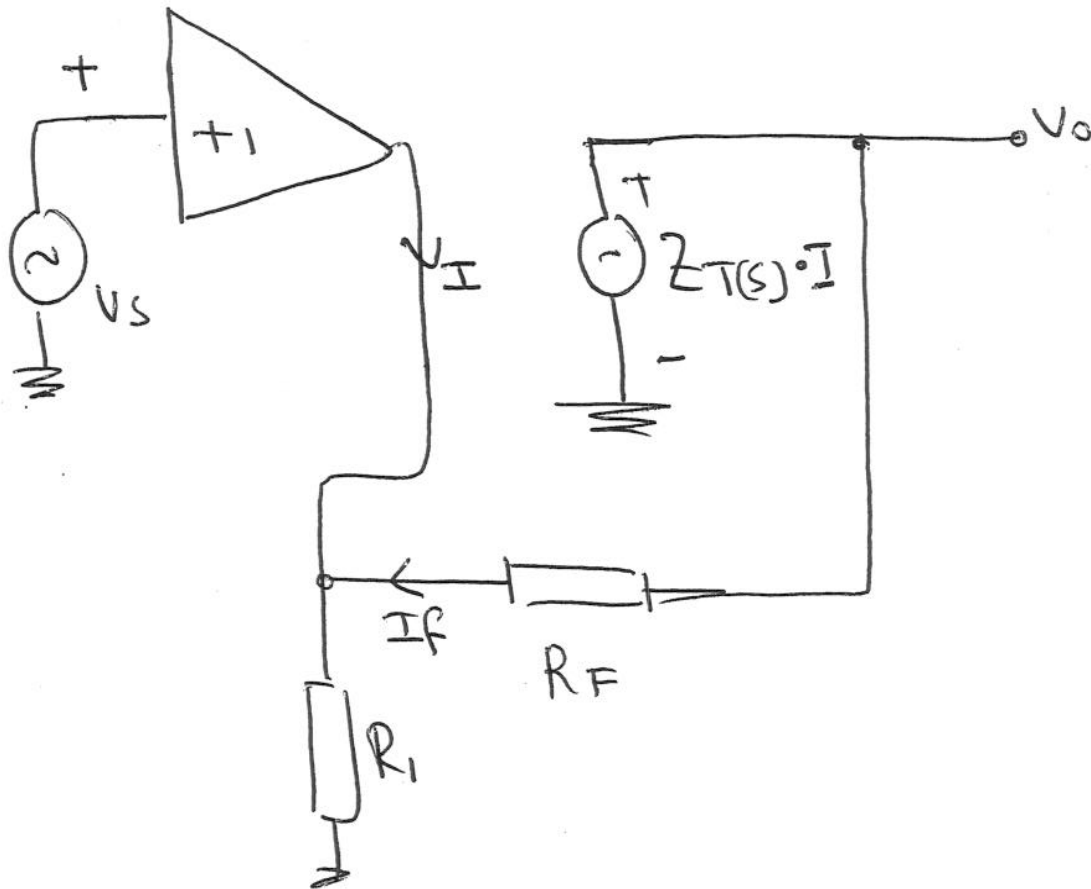
$$\therefore V_{sat} = 2(V_{gs} - V_T)$$

NOTE $\Delta V = (V_{GS} - V_T)$

Swing 2ΔV

Ques cont

macromodel of Current-feedback op-amp.
c).



$$Z_T(s) = Z_{T0} / (1 + s f / h_e) \Rightarrow h_e \text{ dominant Pole}$$

From model

$$I_f = (V_o - V_s) / R_F$$

$$I_1 = V_s / R_1$$

$$V_o = Z_T(s) I = Z_T(s) (I_1 - I_f)$$

From above

$$(V_o / V_s) = (1 + R_F / R_1) \left[\frac{Z_T(s)}{R_F + Z_T(s)} \right]$$

Qn6 cont

(21)

substitute $Z(s)$ s, and assume $Z_{TO} \gg R_F$

$$\left(\frac{V_o}{V_s}\right)_{j\omega} = \left(1 + \frac{R_F}{R_1}\right) \left[\frac{Z_{TO}}{Z_{TO} + R_F} \right] \left(\frac{1}{1 + jf/f_p \frac{(Z_{TO} + R_F)}{R_F}} \right)$$

Assuming $Z_{TO} \gg R_F$

$$\left(\frac{V_o}{V_s}\right)_{j\omega} = \left(1 + \frac{R_F}{R_1}\right) \frac{1}{1 + jf/\frac{GB}{R_F}}$$

where $G.B = f_p Z_{TO}$

$$f_{p \text{ closed}} = \underline{\underline{G.B/R_F}} \Rightarrow \text{determined by } R_F$$

Gain determined by R_1

$$\underline{\underline{A_c = \left(1 + \frac{R_F}{R_1}\right)}}$$

(7/7)

(T