EE4-16
EE9-AC6

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2014

MSc and EEE PART IV: MEng and ACGI

Corrected Copy

ANALOGUE SIGNAL PROCESSING

Monday, 12 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

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Second Marker(s) : K. Fobelets

Special instructions for students

Unless otherwise stated the following parameters have the following definitions:

V_{DS} : Drain Source Voltage.

V_{GS} : Gate Source Voltage.

V_{TH} : Threshold Voltage.

U_t : Thermal Voltage.

n : Weak Inversion Slope factor.

g_m: Transconductance.

Useful identities:

$$cos^2 A + sin^2 A = 1$$

$$cos^2 A - sin^2 A = cos(2A)$$

1. a) State two advantages of representing signals in the current-mode rather than voltage mode domain when trying to achieve low-power operation.

[2]

b) Sketch current mode topologies that implement the following functions, where x represents an input current, z represents an input voltage, A and B are constants and y the output current. Identify A and B in equations (iii), (iv) and (vi).

i) $y = 3x$ [2]

ii) $y = x_1.x_2/x_3$ [2]

iii) $y = \mathrm{A}\exp\left(\frac{\mathrm{z}}{\mathrm{B}}\right)$ [2]

iv) $y = \mathrm{A}\tanh\left(\frac{\mathrm{z}}{\mathrm{B}}\right)$ [2]

v) $y = \min(x_1, x_2)$ [3]

vi) $y = A\int x\,dt$ [3]

c) Equation 1.1, below, shows the noise resource equation which represents the output noise from a cascade of M amplifiers of gain G. Each amplifier i contains n_i devices of area A_i and a bias current I_i.

$$v_{no}^2 = \sum_{i=1}^{i=M} v_{ni}^2 G_i^2 = \sum_{i=1}^{i=M}\left(n_i \frac{K_w}{\left(I_i / n_i\right)^p}\cdot\Delta f + n_i \frac{K_f}{\left(A_i / n_i\right)}\cdot \ln\left(\frac{f_h}{f_l}\right)\right) G_i^2 \qquad (1.1)$$

i) What does equation 1.1 tell us about where the most emphasis should be given in order to reduce noise and why when trying to detect very small signals using a M amplifier cascade?

[2]

ii) Propose two methods to improve noise performance for a fixed supply current.

[2]

2. a) State and derive the translinear principle (TLP) for a loop of MOS transistors working in weak inversion. Give all assumptions you make.

[5]

b) Show how short channel effects in MOS transistors operating in weak inversion, lead to multiplicative errors in output currents of translinear circuits.

[3]

c) The translinear circuit, shown in figure 2.1, is used to solve the quadratic equation:

$$x^2 + bx + c = 0 \qquad (2.1)$$

i) Derive the circuit's function to show it does indeed represent equation 2.1. (Hint: $c=-I_c^2$).

[3]

ii) Derive the equation for the output current I_x which gives the positive root of the quadratic equation.

[2]

d)

i) For the circuit shown in Figure 2.2, show that the output current is given by:

$$I_{out} = I_1 - I_2 = \frac{I_3^2 - I_4^2}{\sqrt{I_3^2 + I_4^2}}$$

[5]

ii) State the function of this circuit for $I_3 = I_A|\cos \omega t|$ and $I_4 = I_A|\sin \omega t|$.

[2]

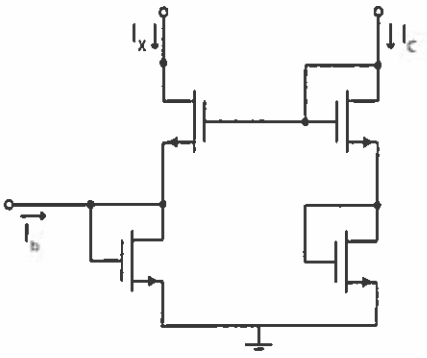


Figure 2.1 for question 2c.

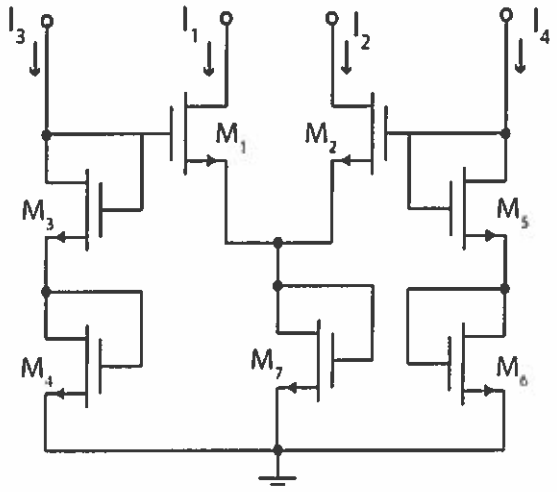


Figure 2.2 for question 2d

3. a) The transfer function of a biquad filter is defined in state space representation by the following equations:

$$\dot{X}_1 = -\omega_0 X_2 + \omega_0 U_1$$

$$\dot{X}_2 = \omega_0 X_1 - \frac{\omega_0}{Q} X_2 + \omega_0 U_2$$

$$Y = X_2$$

whereby Y is the output; U_1 and U_2 are the inputs; and X_1 and X_2 are the states.

i) Show that these state equations can be used to implement either a lowpass or a bandpass transfer function (represented in the Laplace domain) and explain the role of the two inputs U_1 and U_2.

[4]

ii) By using the mappings below show how these linear equations can be mapped to non-linear log-domain design equations. You may assume $I_1=I_2=I_\omega$. Give any other assumptions you make.

$$X_1 = I_1 \exp\left(\frac{V_1}{nU_t}\right) \qquad X_2 = I_2 \exp\left(\frac{V_2}{nU_t}\right)$$

$$U_1 = I_{U1} \exp\left(\frac{V_{U1}}{nU_t}\right) \qquad U_2 = I_{U2} \exp\left(\frac{V_{U2}}{nU_t}\right)$$

[6]

iii) With these log-domain design equations, sketch a schematic of the final log domain filter using MOS transistors operating in weak inversion.

[6]

iv) Given the biquad filter has cut-off frequency, $\omega_0 = 2\pi.10000$ rad/s, select a suitable current for I_1 given that the filter capacitor is C = 10 pf , n = 1.23 and U_t = 25mV.

[1]

b) The log-domain filter is classed as a companding filter. Explain why companding is advantageous in such filters.

[3]

4. a) Figure 4.1 shows a NMOS sampling switch to be used in a switched capacitor circuit. The parameters of M1 are $(W/L)_1 = 10\mu m/1\mu m$, $C_{ox} = 7$ fF/μm^2, $V_{th} = 0.7$ V, CK = $V_{DD} = 3$ V and $C_H = 1$ pf. The total charge in the inversion layer, when the switch is on, is given by:

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{th})$$

i) Explain the errors caused due to charge injection and clock feed. Derive equations that show how the output voltage will change due to these errors, assuming the charge injection is split equally between the source and the drain. [4]

ii) Using the output voltage equations derived in 4i), calculate the total change in output voltage due to charge injection and the total change due to clock feed-through. Based on your result, specify which is more significant. You may assume the overlap capacitance $C_{ov} = 0.08$ fF and an input voltage $V_{in} = 0$ V. [2]

iii) Show that the output voltage contribution due to charge injection results in a non-unity gain error and constant offset. Plot a graph indicating the value of the offset and the slope. [3]

iv) Propose a single method that reduces both charge injection and clock feed-through. Draw schematics and show equations to justify your answer. [4]

b) Figure 4.2 shows a circuit diagram of a switched capacitor non-inverting amplifier.

i) Explain the necessity of bottom plate sampling in this design and draw a schematic of the amplifier indicating which sides of the capacitors are the bottom plates. [4]

ii) Draw an equivalent circuit of Figure 4.2, which has a gain of 2 and a lower gain error. Explain its operation. [3]

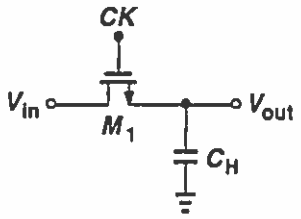


Figure 4.1 for question 4a)

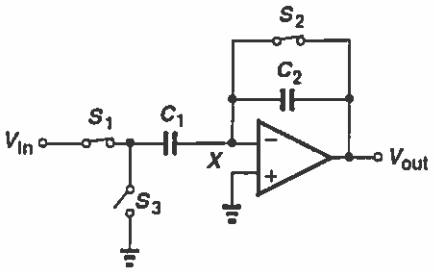


Figure 4.2 for question 4b)

5. a) Figure 5.1 depicts a switched current memory cell.

i) State two limitations of the circuit shown in figure 5.1 and draw an improved schematic which compensates for these and has improved output resistance. [4]

ii) Using your schematic from part 5.a.i, design a memory cell that is non-inverting. [3]

iii) Figure 5.2 depicts a switched capacitor memory cell capable of error compensation. Explain its operation, stating the drain currents of M1 and M2 during each phase of the clock and derive the compensated output current. [4]

iv) Figure 5.3 depicts a switched current cell. Derive its input/output characteristic and identify which function this block performs. You are required to state the transfer function in the z-domain. [5]

b) This question concerns current conveyors. Design, using CCII+ current conveyors, a voltage mode and a current mode differentiator. [4]

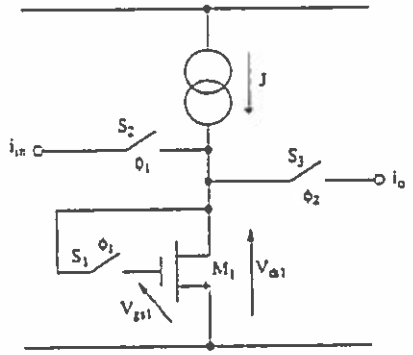
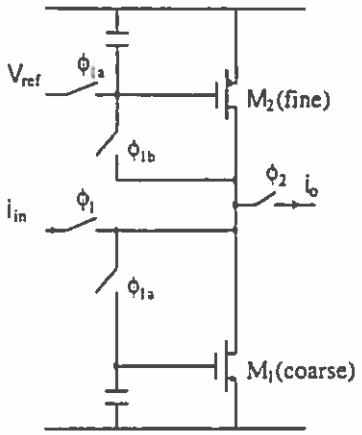


Figure 5.1



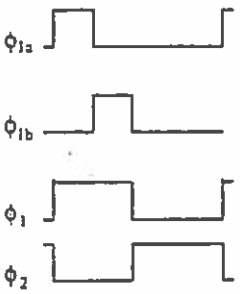


Figure 5.2

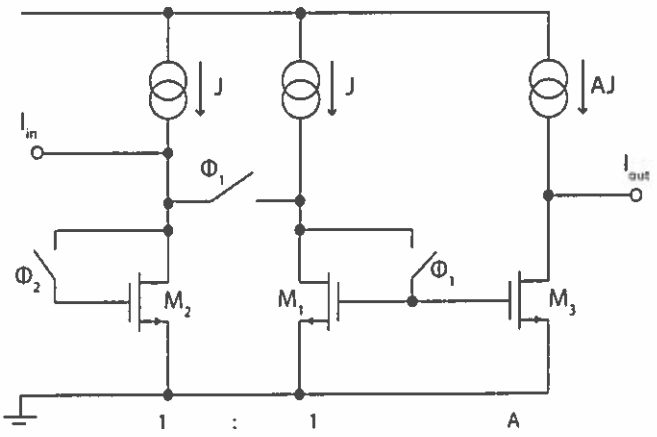


Figure 5.3

6. Figure 6.1 shows a voltage measurement system which uses an operational amplifier (OA) and a novel integrating analogue to digital converter to encode detected voltage signals. The detected signal are first converted to a current through a voltage to current converter (V/I) and then to a spike train through an integrate and fire neuron (I/F). The 8 bit counter is used to count the number of spikes in a fixed period T_{reset} which is then stored in memory. The whole system works off a 1 V supply.

a) Desribe a technique which allows detection of very small voltage signals which exist below the 1/f noise floor of the operational ampifier. Include diagrams showing the operation of this technique and how the frequency spectrum of the signal and noise is shaped in each stage.

[5]

b) Sketch an integrate and fire circuit which can be used in this design and describe its operation. Derive equations for the pulse width and frequency.

[5]

c)

i) Given that the maximum output current is limited to I_{out} = 100 nA, chose a suitable capacitor value for your integrate and fire circuit such that the spike frequency is always less than 5 kHz. You may assume the refractory current I_r=1nA.

[3]

ii) Calculate the maximum allowable reset time T_{reset} such that the counter never overflows for this current.

[2]

d) Explain why this method of integration is more efficient in area when integrating over a very long period (time constant τ = 1 sec). Show how the system, shown in figure 6.1, can be modified to achieve this integration.

[5]

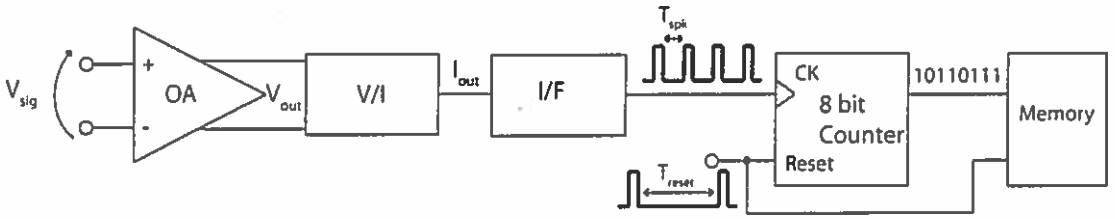


Figure 6.1