IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2006

EEE/ISE PART I: MEng, BEng and ACGI

DIGITAL ELECTRONICS 1

Corrected Copy

Monday, 22 May 10:00 am

Time allowed: 2:00 hours

There are FOUR questions on this paper.

Q1 is compulsory.
Answer Q1 and any two of questions 2-4.
Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung,
Second Marker(s) : K. Masselos,

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X[7:0] is an eight bit bus with X7 being the most significant bit (MSB) and X0 the least significant bit (LSB).

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

[Question 1 is compulsory]

1. a) Simplify the following Boolean expressions using De Morgan's theorem and/or Boolean algebra.

i) $\overline{(A+B)}\,(\overline{A}+\overline{B})$

[2]

ii) $\overline{A}\,\overline{C}+\overline{A}\,B\,C+\overline{B}\,C$

[4]

b) Simplify the following Boolean equation using Karnaugh map.

i) $x = A\,\overline{B}\,\overline{C}+A\,\overline{B}\,C+A\,B\,C+\overline{A}\,B\,\overline{C}$

ii) $y\,(a,b,c,d) = \sum(0, 2, 6, 7, 9, 13, 14)$

[6]

c) Derive the truth tables for the circuits shown in *Figure 1.1* and *Figure 1.2*.

[8]

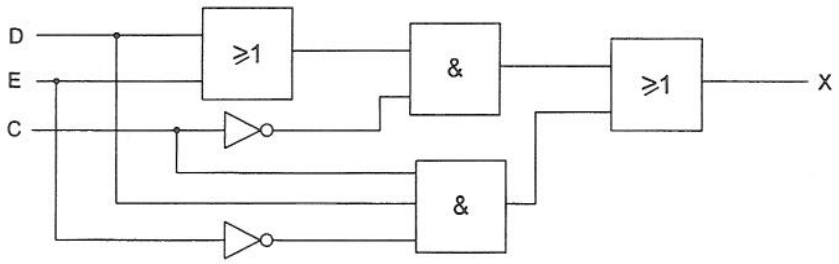


Figure 1.1

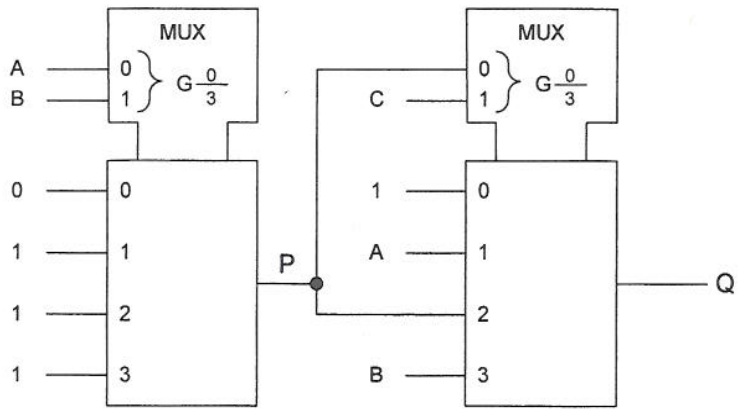


Figure 1.2

d) Given that the hexadecimal code for the ASCII character 'a' is 61, and assuming that all numbers are represented using 8 bits, complete the missing entries which are not shaded in the following table. (No marks will be awarded for this question unless you show how the solutions are derived.)

Binary	Hexadecimal	Unsigned Decimal	Signed Decimal	ASCII
?		105		?
	C5	?	?	

[8]

e) Draw a state transition table for the Mealy finite state machine (FSM) specified by the state diagram shown in *Figure 1.3*.

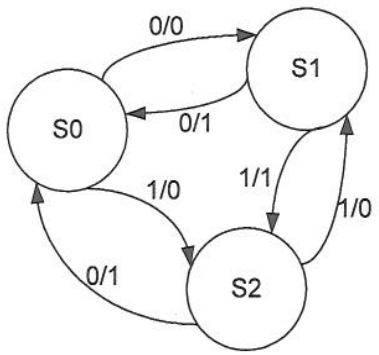


Figure 1.3

[6]

f) Draw the state diagram of a D flip-flop.

Figure 1.4 shows the timing of the input signals *D* and *CLOCK* to a negative edge-triggered D flip-flop with asynchronous $\overline{CLR}$ and $\overline{PRESET}$ inputs (low active). Draw the timing diagram of the Q output.

[6]

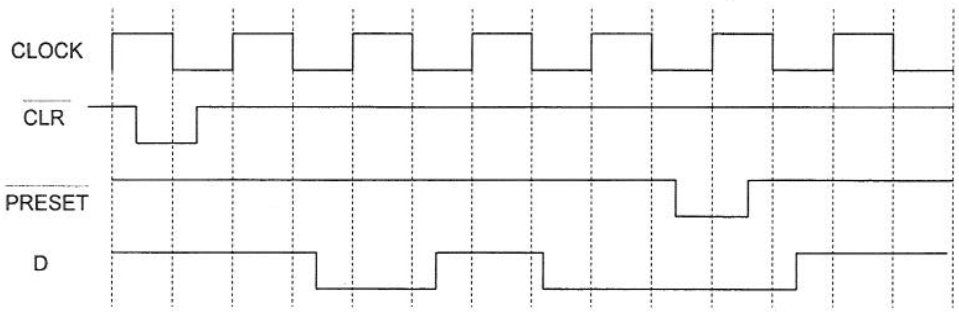


Figure 1.4

2. The truth table for a 1-bit binary subtractor is shown in *Figure 2.1*. It computes the difference D and the borrow-from-left BL of the two inputs A and B.

a) Design the truth table for a 1-bit combinational binary full subtractor with two data inputs A and B, and a borrow from the right input BR. It produces a borrow request to the left output BL and a difference output D.

[8]

b) Design the 1-bit combinational binary full subtractor. You may show your answer in Boolean equation form or in form of circuit schematics.

[8]

c) Show how the design in b) can be cascaded to form a 4-bit binary subtractor.

[6]

d) Verify the function of your circuit with the following two sets of inputs by showing the values of all the signals in your circuit (including internal values of BL/BR). State with justifications whether the subtractor works correctly for signed numbers in 2's complement form.

i) A = 0111 B = 0101

ii) A = 1001 B = 1110

[8]

A	B	D	BL
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Figure 2.1

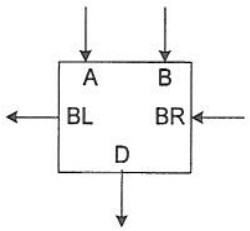


Figure 2.2

3. a) *Figure 3.1* shows a sequential circuit with a number of gates and an edge-triggered D flip-flop.

i) Derive the Boolean equation for the signal D in terms of A and B.

[6]

ii) Draw the truth-table (next state table) for the entire circuit.

[8]

iii) Hence, or otherwise, state the function of this circuit.

[4]

b) The sequential circuit in a) is represented by the schematic shown in *Figure 3.2*. Design a 3-bit binary up counter using this sequential circuit and gates.

[12]

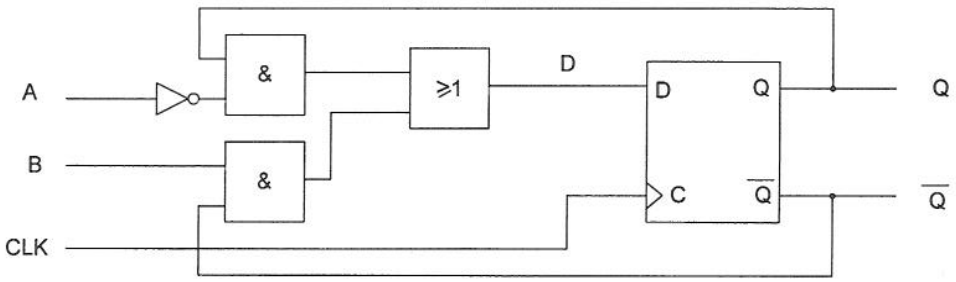


Figure 3.1

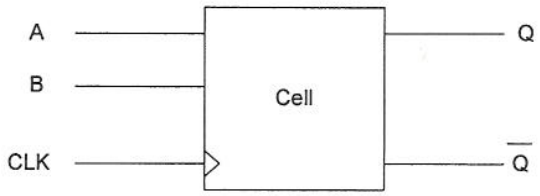


Figure 3.2

4. *Figure 4.1* shows a Moore finite state machine (FSM) with two inputs X1, X2 and one output Z. The output of the FSM remains a constant value unless one of the following input sequences occurs:

   i) The input sequence X1 X2 = 00, 11 causes the output to become 0.
   ii) The input sequence X1 X2 = 01, 11 causes the output to become 1.
   iii) The input sequence X1 X2 = 10, 11 causes the output to change value (i.e. to toggle).

   a) Given that the FSM is implemented with 4 states (S0, S1, S2, S3), draw the state diagram for this FSM.

   [14]

   b) Assume that the 4 states are encoded using 4 binary values (Q3 Q2 Q1 Q0). Using the following state assignment, derive the state transition table for the FSM.

State	Q3	Q2	Q1	Q0
S0	0	0	0	1
S1	0	0	1	0
S2	0	1	0	0
S3	1	0	0	0

   [8]

   c) Derive the Boolean equations for the FSM in sum-of-product form.

   [8]

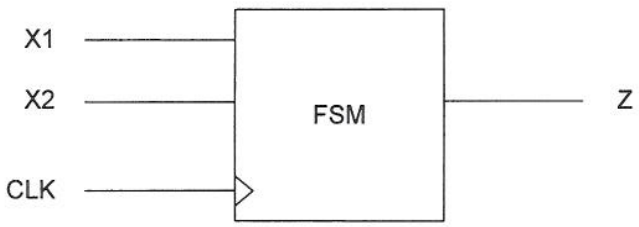


Figure 4.1

[THE END]

Master copy - Aug 06

E1.2 Digital Electronics 1
Solutions 2006

All questions are unseen.

Question 1 is compulsory.

1. a)

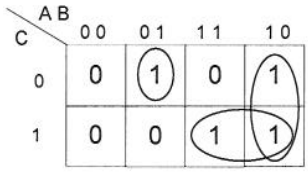
i) $\overline{(A+B)}\,(\overline{A}+\overline{B}) = \overline{A}\,\overline{B}(\overline{A}+\overline{B})$
$= \overline{A}\,\overline{B}+\overline{A}\,\overline{B} = \overline{A}\,\overline{B}$

[2]

ii) $\overline{A}\,\overline{C}+\overline{A}\,B\,C+\overline{B}\,C = \overline{A}\,\overline{C}+C(\overline{A}B+\overline{B})$
$= \overline{A}\,\overline{C}+C(\overline{A}+\overline{B}) = \overline{A}(C+\overline{C})+\overline{B}C = \overline{A}+\overline{B}C$

[4]

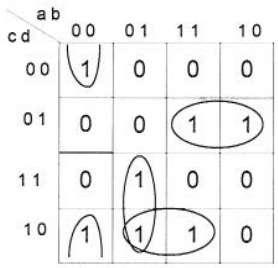
b) i)



$F = \overline{A}\,B\,\overline{C}+A\,C+A\,\overline{B}$

[3]

ii)



$y = \overline{a}\,\overline{b}\,\overline{d}+a\,\overline{c}\,d+\overline{a}\,b\,c+b\,c\,\overline{d}$

[3]

c)

c	d	e	g
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

[4]

A	B	C	P	Q
0	0	0	0	1
0	0	1	0	0
0	1	0	1	0
0	1	1	1	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	1	1

[4]

d)

Binary	Hexadecimal	Unsigned Decimal	Signed Decimal	ASCII
0110 1001		105		**'i'**
	C5	**197**	**-59**	

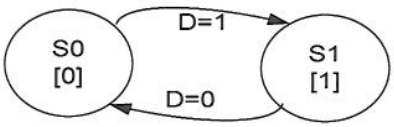
[8]

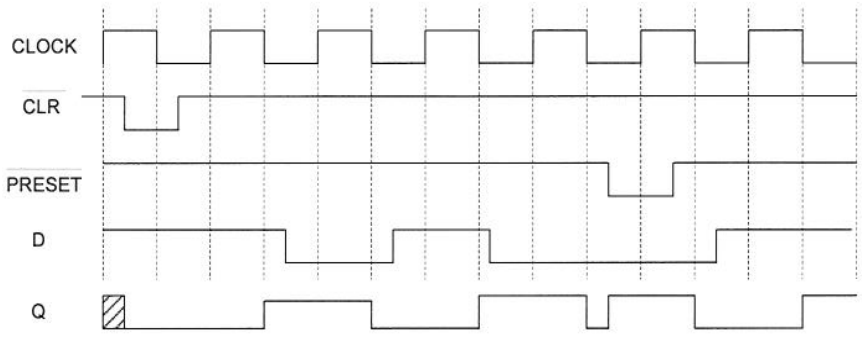
e)

Current State	Input	Next State	Output
S0	0	S1	0
S0	1	S2	0
S1	0	S0	1
S1	1	S2	1
S2	0	S0	1
S2	1	S1	0

[6]

f)





[6]

2. a)

A	B	BR	D	BL
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

[8]

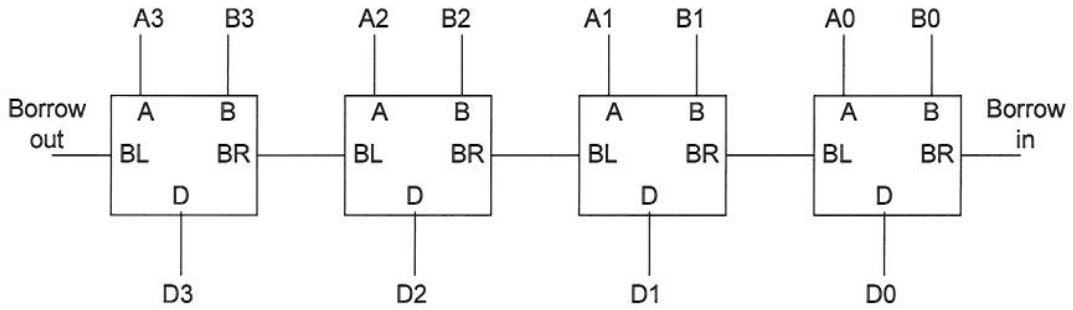
b)

$$D = A \oplus B \oplus BR$$

$$BL = A \bullet \overline{B} + A \bullet BR + \overline{B} \bullet BR$$

[8]

c)



[6]

d) i) when A = 0111 (7), B = 0101 (5), D = 0010 (2)
ii) when A = 1001 (either +9 or -7), B = 1110 (either +14 or -2), D = 1011 (or -5)

Therefore this circuit works with 2's complement signed numbers.

[8]

3. a) i)

$$D = \overline{A}\,Q + B\,\overline{Q}$$

[6]

ii)

A	B	Q	D/Q+
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

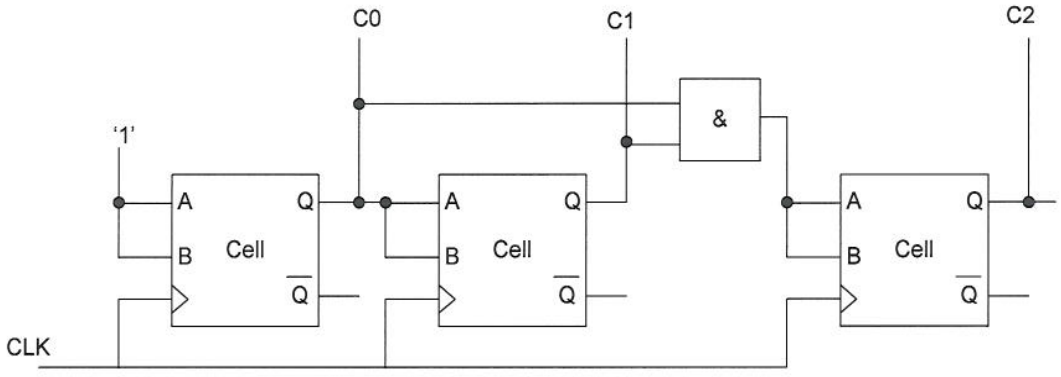
[8]

iii) This is a J-K flip-flop implemented using a D flip-flop. A=K, B=J.

[4]

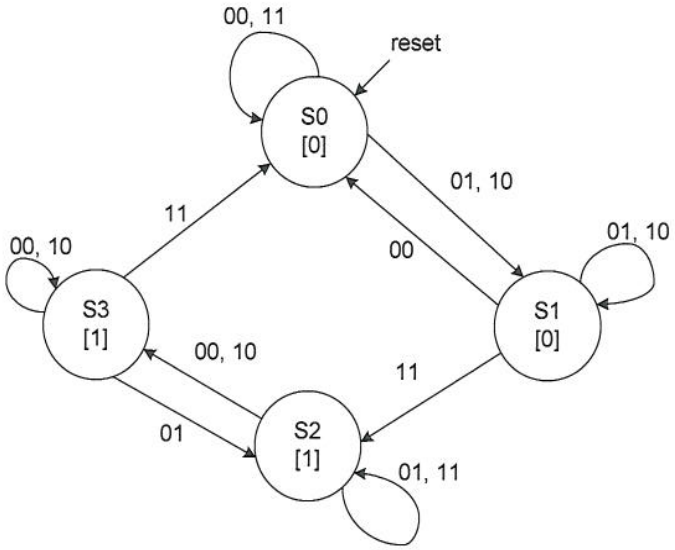
b)
The state transition table of a 3 bit binary up counter is:

Q2	Q1	Q0	Q2+	Q1+	Q0+
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0



[12]

4. a)



[14]

b)

Current Q3 Q2 Q1 Q0	X1 X2	Next N3 N2 N1 N0	Output Z
0001	00	0001	0
0001	01	0010	0
0001	10	0010	0
0001	11	0001	0
0010	00	0001	0
0010	01	0010	0
0010	10	0010	0
0010	11	1000	0
0100	00	1000	1
0100	01	0100	1
0100	10	1000	1
0100	11	0100	1
1000	00	1000	1
1000	01	0100	1
1000	10	1000	1
1000	11	0001	1

[8]

c)

Z = Q2 + Q3

N0 = Q0 X1 X2 + Q0 !X1 !X2 + Q1 !X1 !X2 + Q3 X1 X2

N1 = Q0 !X1 X2 + Q0 X1 !X2 + Q1 !X1 X2 + Q1 X1 !X2 + Q2 X2 + Q3 !X1 X2

N2 = Q1 X1 X2 + Q2 X2 + Q3 !X1 X2

N3 = Q2 !X2 + Q3 !X2

[8]