

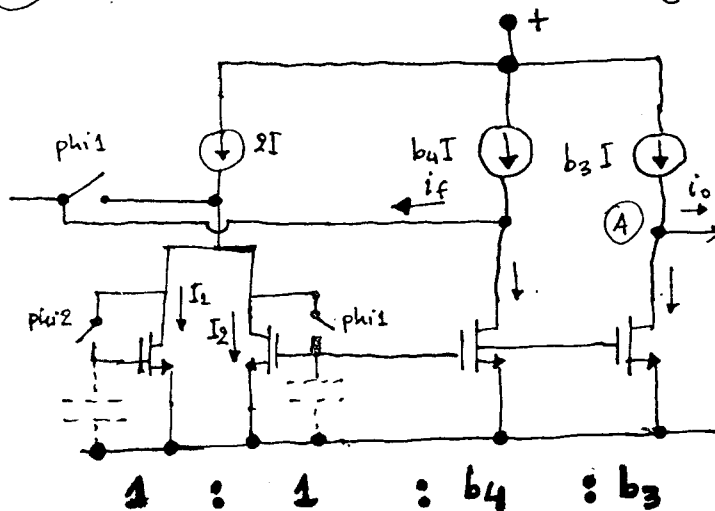
Question 1

A05

(a) [Bookwork] Current-Mode Analogue Sig. Proc. 2007

- The switched-capacitor (SC) technique requires linear floating capacitors; these can be implemented as poly-poly structures but the cost of such processes is high. Cheap digital processes do not offer two layers of polysilicon. For the switched-current (SI) technique we do not need linear capacitors; the memory action can be performed by means of the non-linear C_{gs} capacitor of a MOS device.
- SC circuits use op-amps; SI circuits do not need op-amps (less complex designs)
- The trend towards low power-supply levels means that it is difficult to achieve high-speed and increased dynamic range SC designs since it is difficult to have low-voltage, high-speed op-amps. SI circuits operate in current-mode, voltage swings are smaller (mitigating the reduction of the power supply voltage) allowing low power-supply voltage operation and have the potential for high-speed and low-power operation. Hence, the SI technique is an analogue technique for digital technology.

(b) [New exercise based on taught theory]

During $\phi_2(n-1)$:

$$I_2(n-1) + I_3(n-1) = 2I$$

From KCL at node A:

$$b_3 I_2(n-1) + i_0(n-1) = b_3 I \Rightarrow$$

$$\Rightarrow I_2(n-1) = I - \frac{i_0(n-1)}{b_3} \Rightarrow I_3(n-1) = I + \frac{i_0(n-1)}{b_3}$$

$\phi_{i2}(n)$

During

:

$$\begin{aligned}
 I_1(n) + I_2(n) &= i_{in}(n) + 2I + i_f \\
 i_f &= b_4 I - b_4 I_2(n) \\
 \text{from KCL at (A)} \rightarrow b_3 I_2(n) + i_o(n) &= b_3 I \Rightarrow \\
 \Rightarrow I_2(n) &= I - \frac{i_o(n)}{b_3}
 \end{aligned}
 \left. \vphantom{\begin{aligned} I_1(n) + I_2(n) &= i_{in}(n) + 2I + i_f \\ i_f &= b_4 I - b_4 I_2(n) \\ \text{from KCL at (A)} \rightarrow b_3 I_2(n) + i_o(n) &= b_3 I \Rightarrow \\ \Rightarrow I_2(n) &= I - \frac{i_o(n)}{b_3} \end{aligned}} \right\} \Rightarrow i_f = \left[\frac{b_4}{b_3} \right] i_o(n) \Rightarrow$$

$$\begin{aligned}
 \Rightarrow I_1(n) + I_2(n) &= i_{in}(n) + 2I + i_f \\
 i_f &= \left[\frac{b_4}{b_3} \right] i_o(n) \\
 I_2(n) &= I - \frac{i_o(n)}{b_3} \\
 I_2(n) &= (\text{due to memory action}) = I_2(n-1) = I + \frac{i_o(n-1)}{b_3}
 \end{aligned}
 \left. \vphantom{\begin{aligned} I_1(n) + I_2(n) &= i_{in}(n) + 2I + i_f \\ i_f &= \left[\frac{b_4}{b_3} \right] i_o(n) \\ I_2(n) &= I - \frac{i_o(n)}{b_3} \\ I_2(n) &= (\text{due to memory action}) = I_2(n-1) = I + \frac{i_o(n-1)}{b_3} \end{aligned}} \right\} \Rightarrow$$

$$\cancel{I} + \frac{i_o(n-1)}{b_3} + \cancel{I} - \frac{i_o(n)}{b_3} = i_{in}(n) + \cancel{2I} + \frac{b_4}{b_3} i_o(n) \Rightarrow$$

$$\Rightarrow i_o(n-1) - i_o(n) = b_3 i_{in}(n) + b_4 i_o(n) \Rightarrow$$

$$\Rightarrow z^{-1} i_o(z) - i_o(z) = b_3 i_{in}(z) + b_4 i_o(z) \Rightarrow$$

$$\Rightarrow H(z) = \frac{i_o(z)}{i_{in}(z)} = \frac{-b_3}{(1+b_4) - z^{-1}} = - \frac{\frac{b_3}{1+b_4}}{1 - \frac{z^{-1}}{1+b_4}} \quad \left\{ \begin{array}{l} \text{inverting} \\ \text{damped} \\ \text{integrator} \end{array} \right.$$

$$\text{for } z = e^{sT} = e^{j\omega T} \Rightarrow z^{-1} \approx 1 - j\omega T \text{ when } \omega T \ll 1 \Rightarrow$$

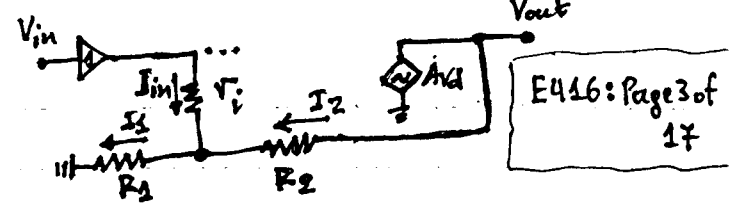
$$H(j\omega) \approx - \frac{b_3}{1+b_4 - j\omega T} = - \frac{(b_3/b_4)}{1 + j\omega(T/b_4)} \Rightarrow$$

$$\Rightarrow \text{time constant} = T/b_4 \quad (\& \text{ dc-gain} = b_3/b_4)$$

Question 2

[Bookwork]

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$$(a) \quad \left. \begin{array}{l} \text{KVL} \rightarrow I_1 R_1 + I_2 R_2 = V_{out} \\ \text{KCL} \rightarrow I_2 = I_1 - I_{in} \end{array} \right\} \Rightarrow (R_1 + R_2) I_1 - R_2 I_{in} = V_{out} \Rightarrow$$

$$\Rightarrow I_1 = \frac{V_{out}}{R_1 + R_2} + \frac{R_2}{R_1 + R_2} I_{in}$$

$$\text{Hence, } I_2 = \frac{V_{out}}{R_1 + R_2} - \frac{R_1}{R_1 + R_2} I_{in}$$

$$\text{But } \begin{array}{c} V_{in} \\ \downarrow \\ V_+ \end{array} - \begin{array}{c} I_1 R_1 \\ \downarrow \\ V_- \end{array} = I_{in} V_i \Rightarrow$$

$$V_{in} - \frac{R_1}{R_1 + R_2} V_{out} - \frac{R_1 R_2}{R_1 + R_2} I_{in} = I_{in} V_i \Rightarrow$$

$$\Rightarrow I_{in} = \frac{V_{in} - \frac{R_1}{R_1 + R_2} V_{out}}{V_i + \frac{R_1 R_2}{R_1 + R_2}} = \frac{(R_1 + R_2) V_{in} - R_1 V_{out}}{V_i (R_1 + R_2) + R_1 R_2}$$

$$\text{Hence } V_{out} = A I_{in} V_i = \frac{A (R_1 + R_2) V_i V_{in} - A V_i R_1 V_{out}}{V_i (R_1 + R_2) + R_1 R_2} \Rightarrow$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = \frac{\frac{A (R_1 + R_2) V_i}{V_i (R_1 + R_2) + R_1 R_2}}{\frac{V_i (R_1 + R_2) + R_1 R_2 + A V_i R_1}{V_i (R_1 + R_2) + R_1 R_2}} = \frac{A (R_1 + R_2) V_i}{V_i (R_1 + R_2) + R_1 R_2 + A V_i R_1} =$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = \left(1 + \frac{R_2}{R_1} \right) \frac{A V_i}{V_i \left(1 + \frac{R_2}{R_1} \right) + R_2 + A V_i} \Rightarrow$$

$$\Rightarrow \left(\text{setting } 1 + \frac{R_2}{R_1} = G \right) \frac{V_{out}}{V_{in}} = G \frac{A}{A + G + R_2/V_i}$$

$$\text{For the CFOA, } R_2/V_i \gg G \Rightarrow \frac{V_{out}}{V_{in}} \approx \frac{G A}{A + R_2/V_i}$$

Assuming α dependence $A = \frac{A_0}{1+jf/f_0}$

$$\frac{V_{out}}{V_{in}} = \frac{G \frac{A_0}{1+jf/f_0}}{\frac{A_0}{1+jf/f_0} + \frac{R_2}{V_i}} = \frac{G A_0}{A_0 + R_2/V_i} \frac{1}{1+j \frac{f \cdot R_2}{f_0 V_i} \frac{1}{A_0 + R_2/V_i}} \Rightarrow$$

$$\Rightarrow \frac{V_{out}}{V_{in}} \approx \left(A_0 \gg \frac{R_2}{V_i} \right) G \frac{1}{1+j \frac{f}{\left[\frac{A_0 f_0 V_i}{R_2} \right]}}$$

Hence gain = $1 + \frac{R_2}{R_1}$

whereas bandwidth = $\frac{A_0 f_0 V_i}{R_2}$

Setting R_2 we set the bandwidth and
setting R_1 we set the gain for the
determined bandwidth.

[Bookwork]

⑥ $V_{out} = A I_{in} V_i = [A V_i] I_{in} = Z_t I_{in} \Rightarrow$

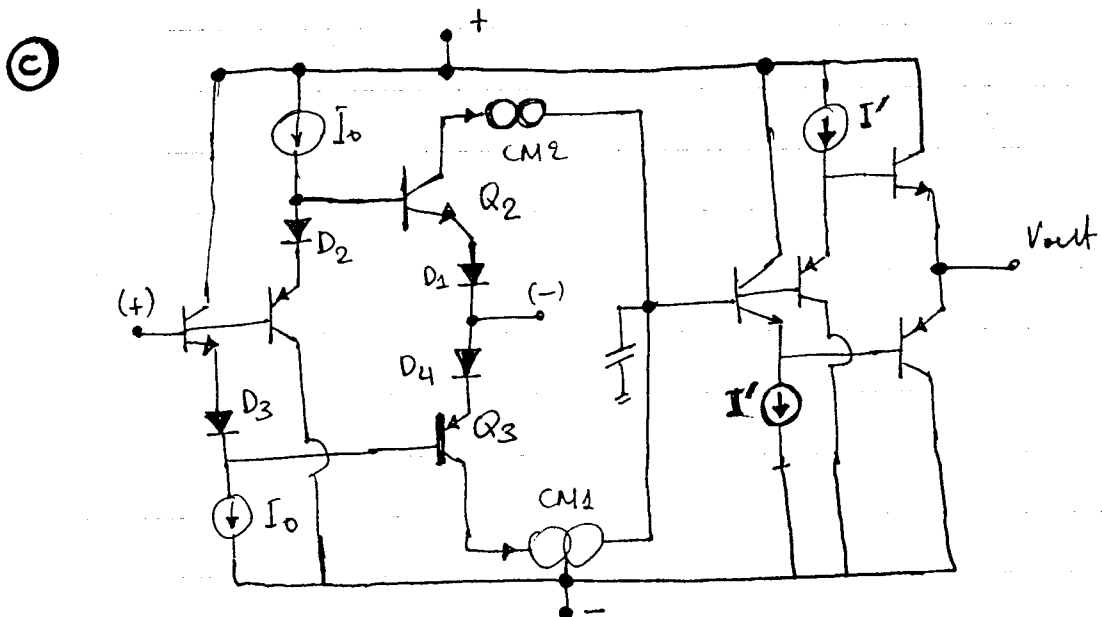
$\Rightarrow V_{out}$ can be considered as the output
of a transimpedance amplifier of
gain $Z_t = A V_i$

Hence, $\frac{V_{out}}{V_{in}} \approx \frac{A G}{A + R_2/V_i} = \frac{(A V_i) G}{(A V_i) + R_2} = G \frac{Z_t}{Z_t + R_2}$

When $Z_t = R_0 \parallel \frac{1}{j\omega C_0} = \frac{R_0}{1+jf/f_0}$ with $R_0 C_0 = \frac{1}{2\pi f_0}$

$$\frac{V_{out}}{V_{in}} = G \frac{R_0}{R_0 + R_2} \frac{1}{1+j \frac{f}{\left(\frac{R_0 (R_0 + R_2)}{R_2} \right)}}$$

bandwidth



Reduced offset voltage can be achieved by including the diodes (diode-connected BJT devices) D_1, D_2, D_3 & D_4 . When

D_1 is implemented with p-type BJT
 D_2 " " " " " " n-type BJT
 D_3 " " " " " " p-type BJT
 and D_4 " " " " " " n-type BJT


then $V_+ - V_- \approx 0$ because from (+) terminal to (-) we meet two n-type base-emitter junctions & two p-type base-emitter junctions \Rightarrow matching. However, the small signal offset at the (-) terminal increases because the output resistance at the (-) terminal increases: $R_- = (r_{e2} + r_{D1}) // (r_{e3} + r_{D4})$. Hence voltage offset is reduced but the r_i value of the **CMOA** is increased and the amplifier becomes more susceptible to "bandwidth roll-off with gain" for given values of R_1, R_2 .

Question 3

[Bookwork]

$$\textcircled{a} \text{ (i) } V_+ = \frac{R_4}{R_4 + R_3} V_2$$

$$V_- = V_+ \Rightarrow \text{current through } R_1 = \frac{V_1 - \frac{R_4}{R_4 + R_3} V_2}{R_1}$$

$$\text{Hence, } V_{out} = \left(\frac{R_4}{R_4 + R_3} V_2 \right) - \left[\frac{V_1 - \frac{R_4}{R_4 + R_3} V_2}{R_1} \right] R_2 \Rightarrow$$


$$\Rightarrow V_{out} = -\left(\frac{R_2}{R_1}\right) V_1 + \left(1 + \frac{R_2}{R_1}\right) \frac{R_4}{R_4 + R_3} V_2 \Rightarrow$$

$$\Rightarrow V_{out} = K_2 V_2 - K_1 V_1$$

In order to have a difference amplifier the following condition should hold:

$$\left(1 + \frac{R_2}{R_1}\right) \frac{R_4}{R_4 + R_3} = \frac{R_2}{R_1} \Rightarrow$$

$$\Rightarrow \frac{1 + \frac{R_2}{R_1}}{1 + \frac{R_3}{R_4}} = \frac{R_2}{R_1} \Rightarrow$$

$$\Rightarrow \boxed{\frac{R_2}{R_1} = \frac{R_4}{R_3}} \leftarrow \text{condition for difference amplifier.}$$

For practical reasons (minimise output offset due to input bias current) it is better if $R_2 = R_4$ & $R_1 = R_3$.

(ii) Common-mode only

$$V_2 = V_1 \Rightarrow \left[\begin{array}{l} V_{diff} = V_2 - V_1 = 0 \\ V_c = \frac{V_1 + V_2}{2} = V_1 \end{array} \right] \Rightarrow V_{out} = (K_2 - K_1) V_1 \Rightarrow$$

$$\boxed{A_c = K_2 - K_1}$$

↑ common-mode gain

Differential-mode only

$$\begin{array}{l} V_2 = V_d/2 \\ V_1 = -V_d/2 \end{array} \Rightarrow \left[\begin{array}{l} V_{diff} = V_d \\ V_c = \frac{V_1 + V_2}{2} = 0 \end{array} \right] \Rightarrow V_{out} = \frac{K_2 + K_1}{2} V_d \Rightarrow$$

$$\Rightarrow \boxed{A_d = \frac{K_2 + K_1}{2}}$$

↑ differential gain

Hence $CMRR = \frac{A_d}{A_c} = \frac{1}{2} \frac{K_2 + K_1}{K_2 - K_1}$

$$K_2 + K_1 = \frac{1 + \frac{R_2}{R_1}}{1 + \frac{R_3}{R_4}} + \frac{R_2}{R_1} = \frac{R_1 R_4 + 2 R_4 R_2 + R_2 R_3}{R_1 R_3 + R_1 R_4} \Rightarrow$$

$$K_2 - K_1 = \frac{1 + \frac{R_2}{R_1}}{1 + \frac{R_3}{R_4}} - \frac{R_2}{R_1} = \frac{R_4 R_1 - R_2 R_3}{R_2 R_3 + R_1 R_4}$$

$$\Rightarrow CMRR = \frac{1}{2} \frac{R_1 R_4 + 2 R_4 R_2 + R_2 R_3}{R_4 R_1 - R_2 R_3} \Rightarrow$$

 \Rightarrow CMRR infinite when

$$\frac{R_4}{R_3} = \frac{R_2}{R_1} \quad \text{which is the same condition for}$$

the op-amp to implement a difference amplifier.

A high CMRR value depends strongly upon resistor matching. Due to the finite tolerances of the resistors the CMRR will drop significantly. Resistor of very low tolerance ($\pm 0.1\%$) and temperature coefficient cost.

[Bookwork]

- ⑥ The circuit depicts a current-mode instrumentation amplifier.

Differential-mode :

The circuit operation is based on the supply-current sensing technique. When $V_1 > V_2$ a current $I = \frac{V_1 - V_2}{R_1}$ is drawn from

OA1 (from its +ve power supply when its output stage operates in class B) and through the action of the current mirrors CM1 & CM2 is reflected/recreated at the -ve input terminal of OA3 giving $V_{out} = \frac{R_2}{R_1} (V_1 - V_2)$. When $V_2 > V_1$ then a current $I = \frac{V_2 - V_1}{R_1}$ is fed into the output of OA1 (into its -ve power supply when its output stage operates in class B) and is again reflected/recreated at the -ve input terminal of OA3.

Common-mode : When $V_1 = V_2$ then $I = 0 \Rightarrow V_{out} = 0$.

The main advantage of this instrumentation amplifier is that it achieves a high CMRR value without the need for precise matched resistors (as for the traditional 3-op-amp instrumentation amplifier). Simplicity and wider bandwidth is a secondary advantage.

The gain accuracy is limited by the accuracy of the current-mirrors; if λ is the current transfer of the current mirrors then $V_{out} = \lambda \frac{R_2}{R_1} (V_1 - V_2)$. The CMRR performance is mainly limited by gain bandwidth (GB) mismatching product between OA1 & OA2; it can be shown that the common-mode gain $\sim (GB_{OA1} - GB_{OA2})$.

Question 4

[Bookwork]

(α) Assumptions & conditions:

equal number of CW & ACW npn junctions

-n- -n- -n- -n- -n- pnp -n-

Same V_T (i.e. temperature) for all devicesAll npn (pnp) devices have same current density I_{sn} (I_{sp})

When the above hold:

$$CW \sum_{j=1}^m V_{bej} = ACW \sum_{j=1}^m V_{bej} \Rightarrow$$

$$\Rightarrow CW \sum_{j=1}^m V_T \ln \left[\frac{I_{Cj}}{I_{sj} A_j} \right] = ACW \sum_{j=1}^m V_T \ln \left[\frac{I_{Cj}}{I_{sj} A_j} \right] \Rightarrow$$

$$\Rightarrow CW \prod_{j=1}^m \left[\frac{I_{Cj}}{I_{sj} A_j} \right] = ACW \prod_{j=1}^m \left[\frac{I_{Cj}}{I_{sj} A_j} \right] \Rightarrow$$

$$\Rightarrow CW \prod_{j=1}^m \left[\frac{I_{Cj}}{A_j} \right] = ACW \prod_{j=1}^m \left[\frac{I_{Cj}}{A_j} \right]$$

BIPOLAR TRANSLINER PRINCIPLE

[Bookwork]

MOS TRANSLINER PRINCIPLE:

*

$$CW \sum_{j=1}^m \sqrt{\frac{I_{Dj}}{K_j}} = ACW \sum_{j=1}^m \sqrt{\frac{I_{Dj}}{K_j}}$$

Question shortened by the 2nd marker

$$K_j = \frac{\mu C_{ox}}{2} \frac{W}{L}$$

Disadvantages: — "Sum of roots" is not as widely useful as bipolar "products"

— MOS square law holds over a smaller current range than the bipolar exponential law

— process parameters do not cancel

~~automatically for "mixed" (NMOS & PMOS) TL loops.~~

~~Advantage: MOS TL circuits do not suffer from beta errors~~

(b) [New exercise based on taught theory]

Applying the TLP:

$$(i) \left[\frac{I - I_x}{2} \right]^2 I_4 = I_3 \left[\frac{I + I_x}{2} \right]^2 \Rightarrow$$

$$\frac{I_4}{I_3} = \left[\frac{I + I_x}{I - I_x} \right]^2 \Rightarrow \left. \begin{aligned} I_4 &= \frac{I(I + I_x)^2}{(I - I_x)^2 + (I + I_x)^2} \\ I_3 &= \frac{I(I - I_x)^2}{(I - I_x)^2 + (I + I_x)^2} \end{aligned} \right\}$$

But also (KCL) $I_3 + I_4 = I$

$$(ii) \left. \begin{aligned} I_2 &= \frac{I - I_x}{2} + \frac{I(I + I_x)^2}{(I - I_x)^2 + (I + I_x)^2} \\ I_1 &= \frac{I + I_x}{2} + \frac{I(I - I_x)^2}{(I - I_x)^2 + (I + I_x)^2} \end{aligned} \right\} \Rightarrow$$

$$I_2 - I_1 = -I_x + \frac{4I^2 I_x}{2(I^2 + I_x^2)} \Rightarrow$$

$$I_2 - I_1 = \frac{-I_x 2I^2 - I_x 2I_x^2 + 4I^2 I_x}{2(I^2 + I_x^2)} \Rightarrow$$

$$I_2 - I_1 = \frac{I^2 I_x - I_x^3}{I^2 + I_x^2}$$

When $I_x = y I$, then $I_2 - I_1 = I \frac{y - y^3}{1 + y^2}$

[New exercise based on taught theory]

(c) (i) Applying the TLP & KCL yields:

$$(2I + I_x + I_2) I = (I + I_x) (0.92I + I_2) \Rightarrow$$

$$\Rightarrow I_2 = \frac{(2I + I_x + I_2) I}{I + I_x} - 0.92I$$

$$(ii) \quad (I + I_x) [3I - (I + I_x)] = \frac{2/3 I}{A} \frac{(2I + I_x + I_z) I - 0.92 I}{I + I_x} \rightarrow$$

$$\Rightarrow \frac{A^2 (I + I_x)(2I - I_x)}{[2/3] I} + 0.92 I = \frac{(2I + I_x + I_z) I}{I + I_x} \Rightarrow$$

$$\Rightarrow \left(\frac{3A^2 (I + I_x)(2I - I_x)}{2I} + 0.92 I \right) \frac{I + I_x}{I} = 2I + I_x + I_z \Rightarrow$$

$$\Rightarrow I_z = \left(\frac{3A^2 (I + I_x)(2I - I_x)}{2I} + 0.92 I \right) \frac{I + I_x}{I} - 2I - I_x$$

$$(iii) \quad I_z = \frac{\{3A^2(2I^2 + II_x - I_x^2) + 1.84I^2\}(I + I_x) - 4I^3 - 2I^2I_x}{2I^2} \rightarrow$$

$$I_z = (3A^2 - 1.08) I + \left(\frac{9A^2 - 0.16}{2} \right) I_x - \frac{3A^2}{2} \frac{I_x^3}{I^2}$$

$$\text{When } \frac{3A^2}{2} = 0.54 \Rightarrow A = 0.6 \quad \text{then}$$

$$\text{indeed } I_z = 1.54 I_x - 0.54 \frac{I_x^3}{I^2}$$

Question 5

[New exercise based on taught theory]

(a) from the given state-space relations:

$$\left. \begin{aligned} \left[s + \frac{\omega_0}{Q} \right] \bar{X}_1(s) - \omega_0 \bar{X}_2(s) &= 0 \\ \omega_0 \bar{X}_1(s) + s \bar{X}_2(s) &= \omega_0 \bar{V}(s) \end{aligned} \right\} \Rightarrow$$

$$D_{\bar{X}_1} = \begin{vmatrix} 0 & -\omega_0 \\ \omega_0 \bar{V}(s) & s \end{vmatrix} = \omega_0^2 \bar{V}(s), D_{\bar{X}_2} = \begin{vmatrix} s + \frac{\omega_0}{Q} & 0 \\ \omega_0 & \omega_0 \bar{V}(s) \end{vmatrix} = \omega_0 \left(s + \frac{\omega_0}{Q} \right) \bar{V}(s)$$

$$D = \begin{vmatrix} s + \frac{\omega_0}{Q} & -\omega_0 \\ \omega_0 & s \end{vmatrix} = s^2 + \left(\frac{\omega_0}{Q} \right) s + \omega_0^2$$

Hence, $\frac{\bar{V}_1(s)}{\bar{V}(s)} = \frac{\bar{X}_1(s)}{\bar{V}(s)} = \frac{\omega_0^2}{s^2 + \left(\frac{\omega_0}{Q} \right) s + \omega_0^2}$, Lowpass response

$\frac{\bar{V}_2(s)}{\bar{V}(s)} = \frac{\bar{X}_2(s)}{\bar{V}(s)} = \frac{\omega_0 \left(s + \frac{\omega_0}{Q} \right)}{s^2 + \left(\frac{\omega_0}{Q} \right) s + \omega_0^2}$, "two-pole one-zero" response

(b)

$$\begin{aligned} x_1 &= I_0 e^{V_1/V_T} \Rightarrow \dot{x}_1 = x_1 \frac{\dot{V}_1}{V_T} \\ x_2 &= I_0 e^{V_2/V_T} \Rightarrow \dot{x}_2 = x_2 \frac{\dot{V}_2}{V_T} \end{aligned}$$

Hence :

$$\left. \begin{aligned} x_1 \frac{\dot{V}_1}{V_T} &= - \left(\frac{\omega_0}{Q} \right) x_1 + \omega_0 x_2 \\ x_2 \frac{\dot{V}_2}{V_T} &= - \omega_0 x_1 + \omega_0 u \end{aligned} \right\} \Rightarrow$$

$$C \dot{V}_1 = - \frac{(\omega_0 C V_T)}{Q} + (\omega_0 C V_T) e^{\frac{V_2 - V_1}{V_T}}$$

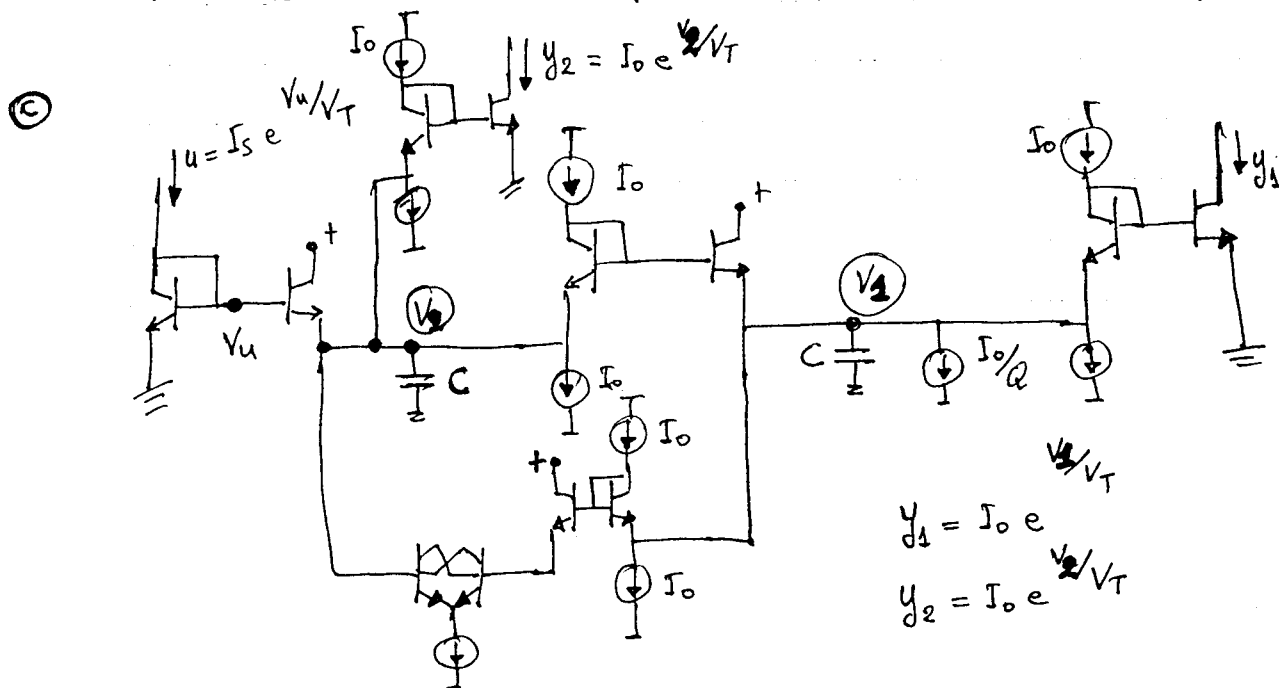
$$C \dot{V}_2 = - (\omega_0 C V_T) e^{\frac{V_1 - V_2}{V_T}} + (\omega_0 C V_T) \frac{I_s}{I_0} e^{\frac{V_u - V_2}{V_T}}$$

Setting $\omega_0 C V_T = I_0 = \text{biasing current} \Rightarrow$

$$C\dot{V}_1 + \frac{I_0}{Q} = I_0 e^{\frac{V_2 - V_1}{V_T}}$$

$$C\dot{V}_2 + I_0 e^{\frac{V_1 - V_2}{V_T}} = I_0 e^{\frac{V_u - V_2}{V_T}}$$

Non-linear log-domain design equations which can be interpreted as KCL relations involving capacitor currents, constant current sources & bipolar transistor collector currents operating according to their non-linear (exponential) V-I characteristic.



The above topology satisfies the non-linear design equations.

$$W_0 C V_T = I_0 \Rightarrow$$

$$\Rightarrow I_0 = (2\pi \times 4 \times 10^6) \cdot 20 \times 10^{-12} \times 0.026 \Rightarrow$$

$$\Rightarrow I_0 \approx 13 \mu A$$

[Bookwork]

- (a) Two N -port networks A & B must satisfy the following relation in order to be adjoint:

$$\sum_{n=1}^N (V_{A_n} I_{B_n} - V_{B_n} I_{A_n}) = 0$$

with V_{A_n} denoting the voltage of the n -th port of network A , etc....

- (i) Resistor

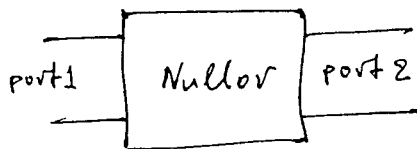
$$V_A = R_A I_A, \text{ one port}$$

$$V_A I_B - V_B I_A = 0 \Rightarrow \frac{V_B}{I_B} = \frac{V_A}{I_A} \Rightarrow \text{But } \frac{V_A}{I_A} = R_A$$

$$V_B = I_B \cdot \underset{R_B}{R_A}, \text{ Hence the adjoint}$$

network of a resistor is a resistor of the same value.

- (ii)



$$V_A = [V_{A1} \ V_{A2}] = [0 \ X]$$

$$I_A = [I_{A1} \ I_{A2}] = [0 \ X]$$

X denotes "any value"

$$\text{Hence I want: } \underset{0}{V_{A1}} \underset{0}{I_{B1}} - \underset{0}{V_{B1}} \underset{0}{I_{A1}} + \underset{X}{V_{A2}} I_{B2} - V_{B2} \underset{X}{I_{A2}} = 0$$

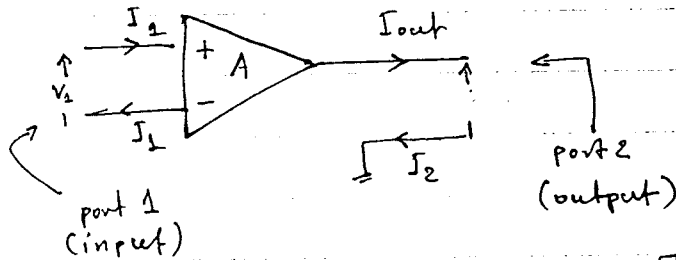
$$\text{Hence when } V_B = [V_{B1} \ V_{B2}] = [X \ 0]$$

$$\text{and } I_B = [I_{B1} \ I_{B2}] = [X \ 0]$$

the relation is satisfied.

Thus, the adjoint network of a nullor is another nullor with its input & output ports interchanged

(iii) voltage amplifier



$$V_A = [V_{A1} \ V_{A2}] = [V_{in} \ A V_{in}]$$

$$I_A = [I_{A1} \ I_{A2}] = [0 \ X]$$

Hence

$$\underbrace{V_{A1}}_{V_{in}} I_{B1} - \underbrace{V_{B1}}_0 I_{A1} + \underbrace{V_{A2}}_{A V_{in}} I_{B2} - \underbrace{V_{B2}}_X I_{A2} = 0$$

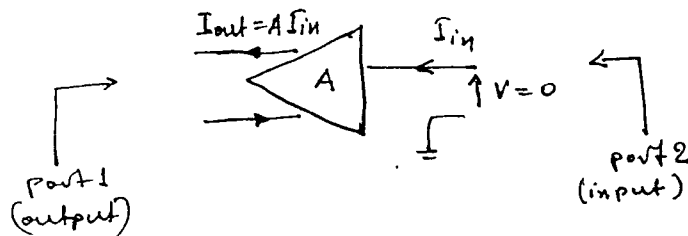
and when

$$V_B = [V_{B1} \ V_{B2}] = [X \ 0]$$

$$I_B = [I_{B1} \ I_{B2}] = [-A I_{in} \ I_{in}]$$

then the relation is satisfied

Thus, the adjoint network of an ideal voltage amplifier is a current amplifier with input and output ports interchanged:



[New exercise based on taught theory]

(b)

To find its current-mode equivalent we only need to find its adjoint bearing in mind that

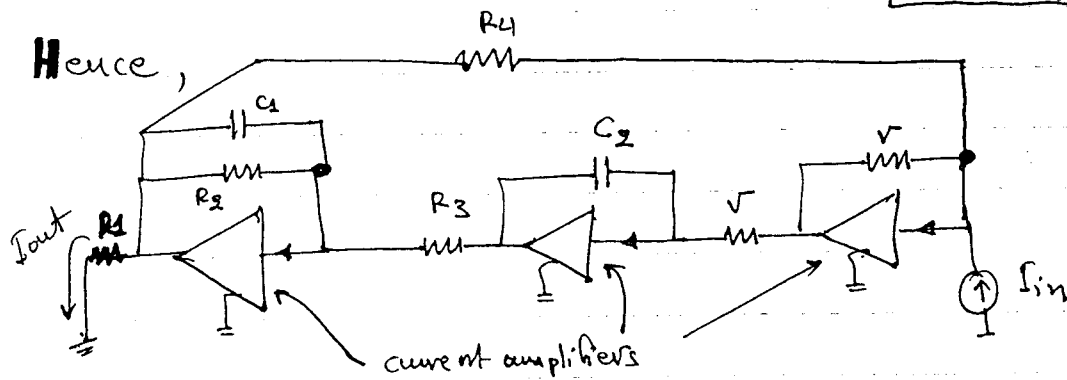
R is transformed to R

C —||— C

* a voltage amplifier

—||—

to a current amplifier with its input & output ports interchanged



high-gain [BOOKWORK]

- (c) (i) if "ideal amplifiers" are available, it doesn't matter what kind of amplifier you use
- (ii) if practical amplifiers are available then for an I-I converter we should use a current-amplifier (CCCS) because with this choice the closed-loop bandwidth becomes independent of the source & load impedance levels. The price paid for this ^{case} is that the I-I converter bandwidth cannot be set independently of its gain (gain-bandwidth conflict).
- (iii) When high performance Cfs & Vfs are available then we should choose any other amplifier except from a current amplifier. For, if we choose a buffered transresistance amplifier (CCVS) or a transconductance amplifier (VCCS) or a voltage amplifier (VCVS) then the closed loop bandwidth of the converter can be set independently from the closed-loop gain.

(d) [New Combinatorial exercise based on Tinsley theory]

$$(i) \quad V_{cap} + V_T \ln \left(\frac{I_0}{I_S} \right) = V_T \ln \left(\frac{I_{out1}}{I_S} \right) \Rightarrow$$

$$i_{cap} = C \dot{V}_{cap} = C V_T \frac{\dot{I}_{out1}}{I_{out1}}$$

(ii) Applying TLP:

$$u \cdot (2 I_{out1}) = (2 I_{out1}) \cdot I_d \Rightarrow$$

↓ Due to p-type current mirror
 ↓ Due to p- & the n-type current mirrors

$$\Rightarrow u = 2 I_d$$

(iii) Applying TLP:

$$I_{in} I_0 = \left(\underset{\substack{\downarrow \\ u}}{2 I_d} + C V_T \frac{\dot{I}_{out1}}{I_{out1}} \right) I_{out1} \Rightarrow$$

$$I_{in} I_0 = (2 I_d) I_{out1} + C V_T \dot{I}_{out1} \Rightarrow$$

$$\Rightarrow \frac{I_{out1}(s)}{I_{in}(s)} = \frac{(I_0 / C V_T)}{s + (2 I_d / C V_T)}$$

However, $I_{out2} = 3 I_{out1} \Rightarrow$

$$\frac{I_{out2}(s)}{I_{in}(s)} = \frac{\frac{3 I_0}{C V_T}}{s + (2 I_d / C V_T)}$$

$$s \rightarrow 0 \Rightarrow \text{gain} = \frac{3 I_0 / C V_T}{2 I_d / C V_T} = \frac{3}{2} \frac{I_0}{I_d} = 1 \Rightarrow I_0 = \frac{2 I_d}{3} = \frac{20}{3} \mu A$$

$$\omega_0 = \frac{2 I_d}{C V_T} \Rightarrow C = \frac{2 I_d}{\omega_0 V_T} = \frac{2 \times 10 \times 10^{-6}}{2 \pi \times 1 \times 10^6 \times 0.026} \approx 122 \text{ pF}$$