E3.01
AC1

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2003

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Wednesday, 30 April 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer Question 1 and three others

Corrected Copy

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : C. Toumazou
Second Marker(s) : S. Lucyszyn

1. Figure 1.1 shows a single-stage double cascode CMOS amplifier.

(a) Write a simple SPICE program that will compute a small signal gain and phase frequency response of the circuit over the frequency range 1 kHz to 10 MHz. Assume all bulks are internally connected to the source of the MOSFETs. [10]

The OPTIONS card and the transistor model process parameters QP and QN are already built into the SPICE library.

(b) Given that the threshold voltage V_T of the CMOS technology is 1 V estimate the maximum output swing of the amplifier. [4]

(c) What effects does cascoding have on the amplifier's phase margin? [3]

(d) Finally, why are the passive components in the circuit very large? [3]

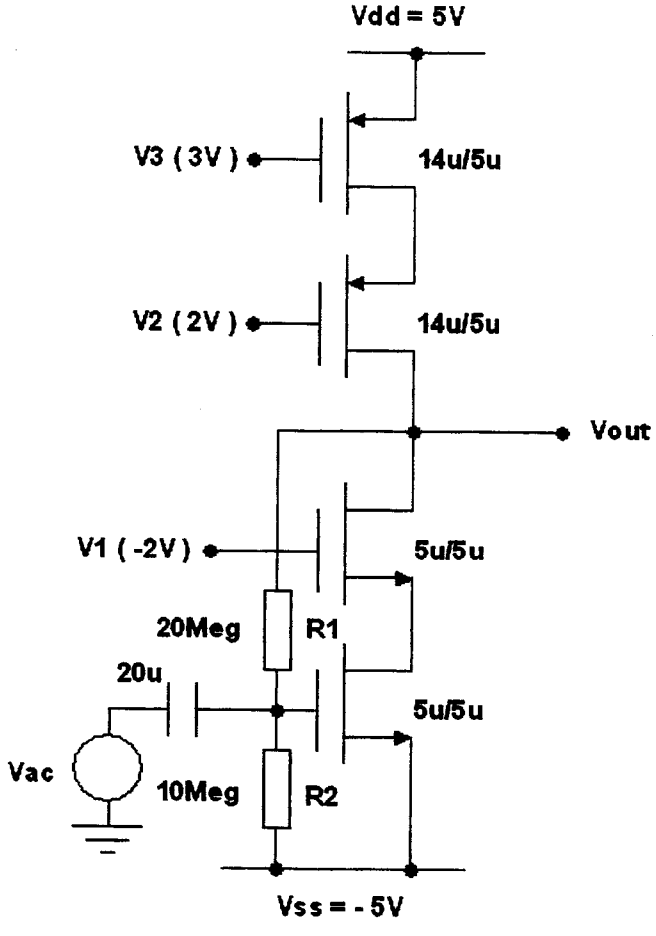

Figure 1.1

2. (a) Briefly describe the function of each of the three biasing circuits in Figures 2.1–2.3, giving reasons for their suitability in an integrated circuit application. [8]

(b) For the bandgap voltage reference circuit of Figure 2.1, show that $\delta V_0/\delta T = 0$ (where T is temperature) if $(R_2/R_3)\ \ln\ (I_1/I_2) = 29$, and that this condition occurs if $V_0 = 1.283$ V.

Assume the temperature coefficient of V_{BE} to be –2.5 mV/°C. Boltzmann constant $k = 1.38 \times 10^{-23}$ J/K and electron charge $q = 1.6 \times 10^{-19}$ C. [4]

(c) Calculate the fractional temperature coefficient for the constant current generator of Figure 2.2 at room temperature, given that R is a polysilicon resistor with a temperature coefficient of 1500 ppm/°C. [4]

(d) Explain qualitatively why the four-transistor voltage potential divider of Figure 2.3 can have significantly less active-chip area than an equivalent two-transistor voltage potential divider with the same power consumption. [4]

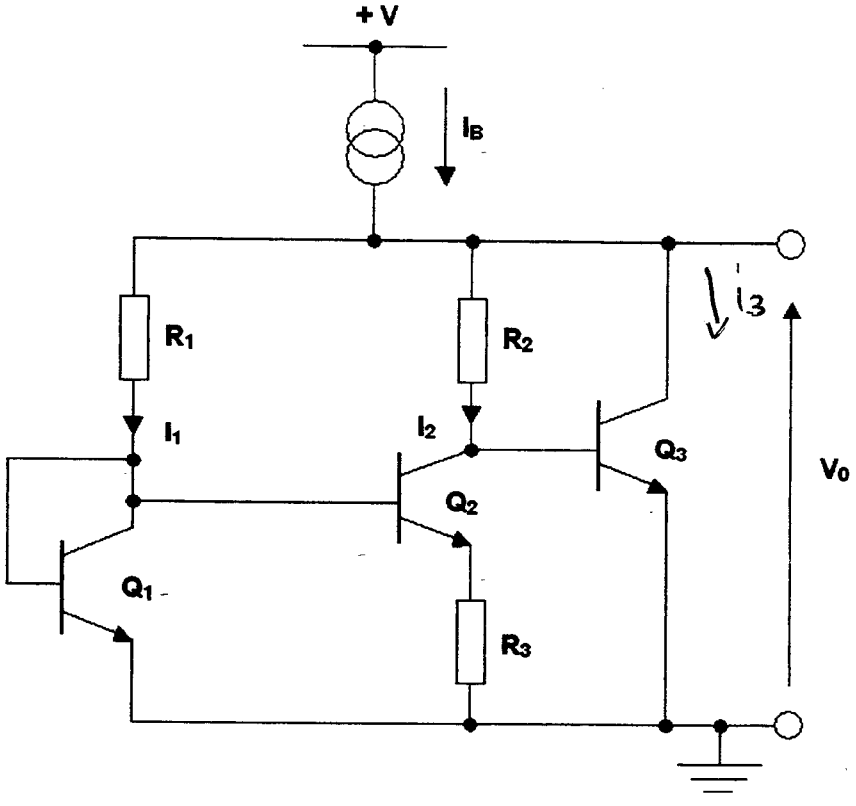

Figure 2.1

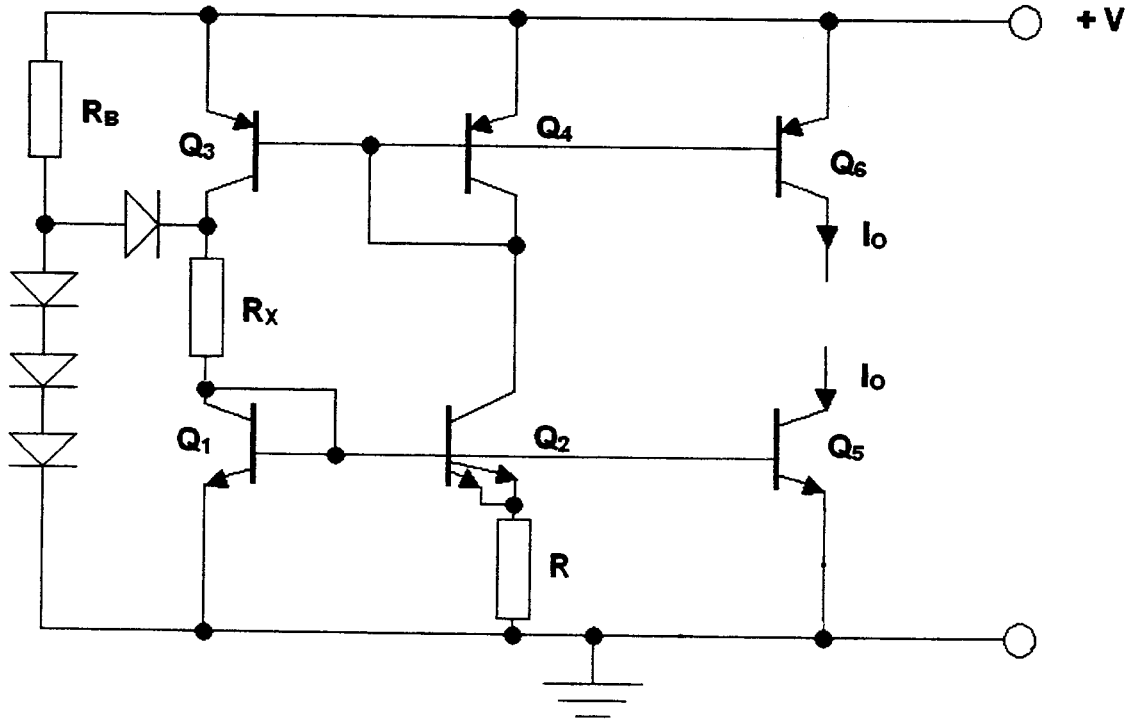

Figure 2.2

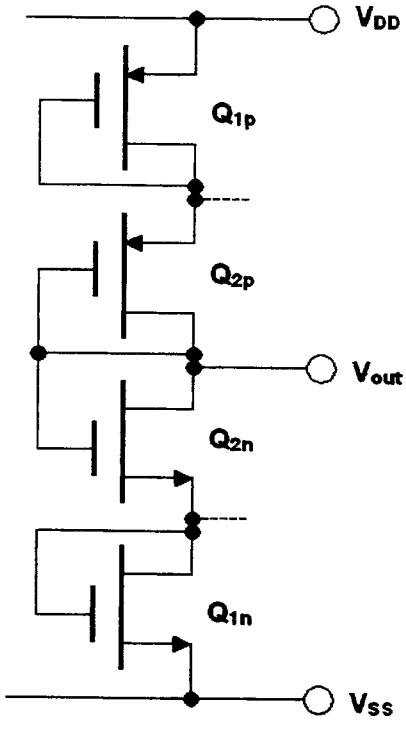

Figure 2.3

3. (a) Figure 3.1 shows a fully differential continuous time integrator using a balanced double differential linear active transresistor. Derive an expression for the time constant of the integrator. You may ignore all bulk effects, and assume all MOSFETs are operating in the triode region. [9]

(b) For the current mirror of Figure 3.2, estimate the minimum output voltage while still maintaining saturated devices. Derive this voltage swing in terms of the device threshold voltage, V_T, clearly stating any assumptions you make. [5]

(c) Sketch a regulated cascade current-source and explain why the output resistance of the current-source is higher than a standard cascode mirror. [6]

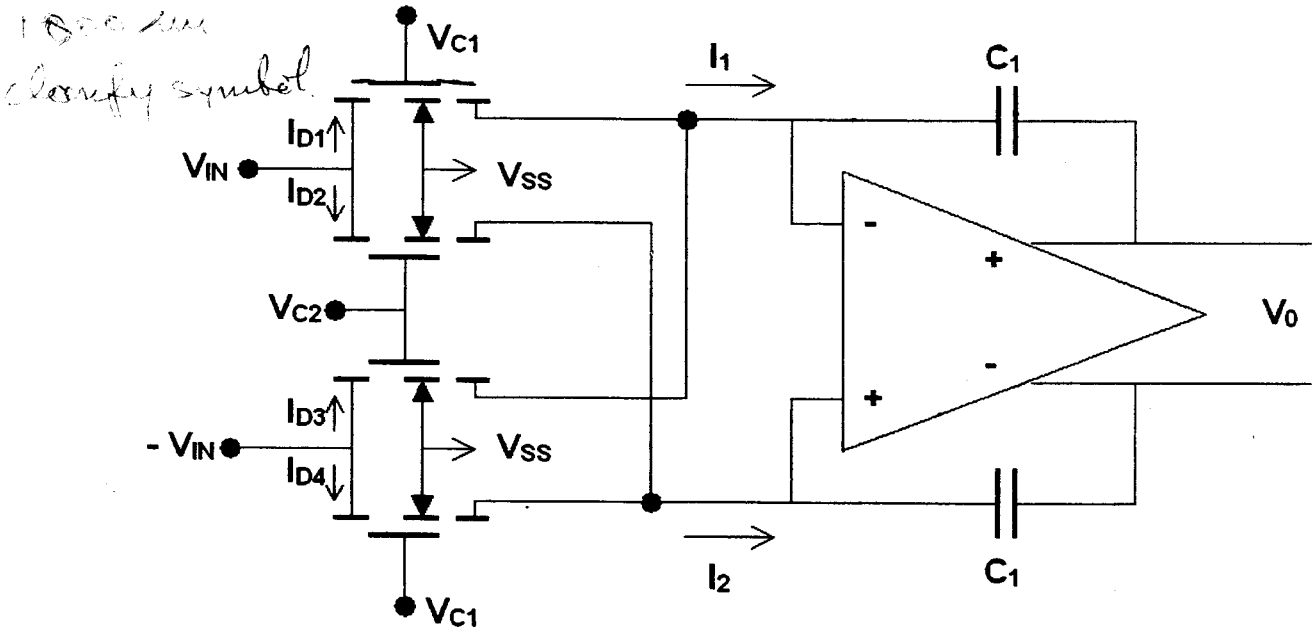

Figure 3.1

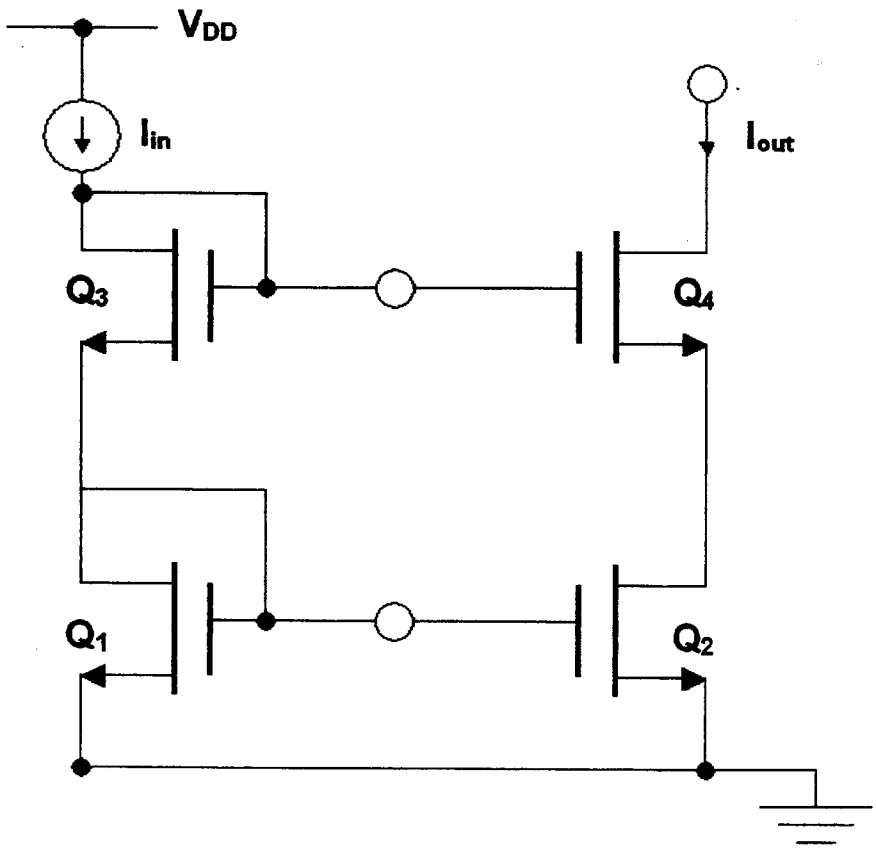

Figure 3.2

4. (a) Figure 4.1 shows a folded cascode connection. What is the main advantage of this design over the more classical cascode connection? Show using a simple sketch how the architecture of Figure 4.1 can be used to form the basis of a single stage folded cascode operational amplifier (op-amp). Give an expression for the approximate small signal voltage gain of the op-amp. [10]

(b) Give one advantage and one disadvantage of a single stage over a two-stage op-amp. Figure 4.2 shows a two-stage CMOS op-amp. Estimate the low-frequency differential voltage gain and gain-bandwidth product of the amplifier. Aspect ratios of all devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below. [7]

(c) Answer **ONE** of the following:

The gain-bandwidth product, voltage gain and slew rate of the op-amp of Figure 4.2 are below the desired specification. Explain qualitatively a minimum sequence of parameter changes so that the op-amp design satisfies all of its specifications.

OR

Explain why a resistor in series with the compensation capacitor C in Figure 4.2 can significantly improve the amplifier's phase margin. [3]

CMOS TRANSISTOR PARAMETERS

MODEL PARAMETERS	Kp ($\mu A/V^2$)	λ (V^{-1})	V_{T0} (V)
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

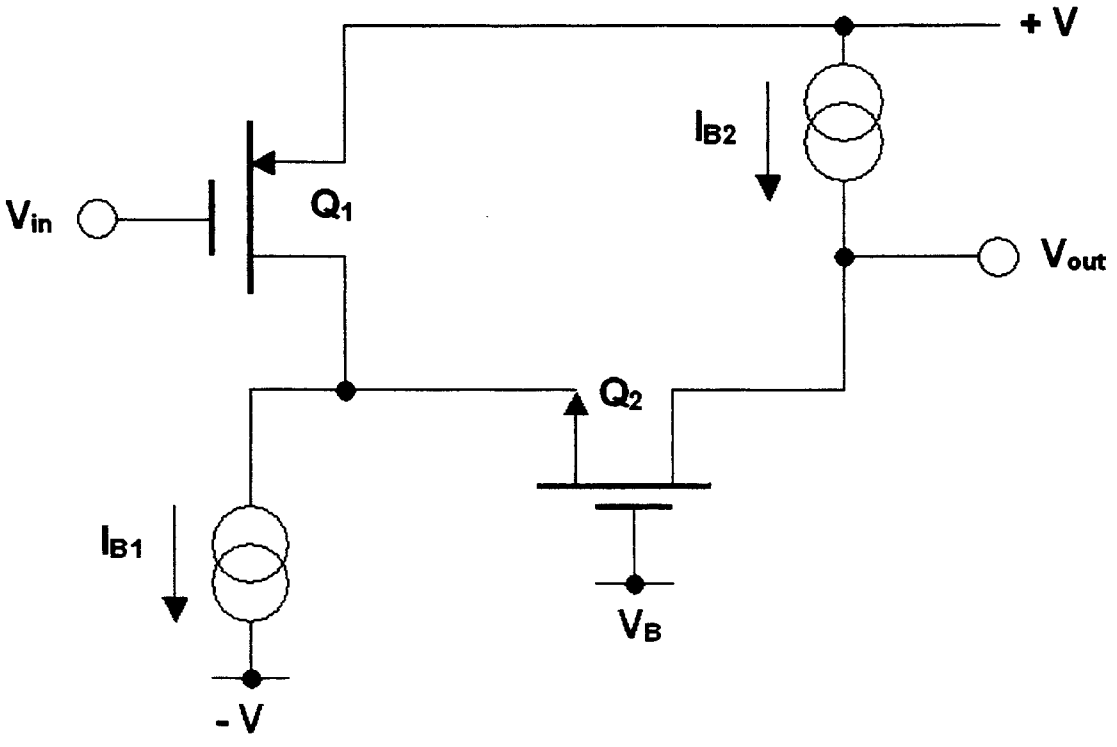

Figure 4.1

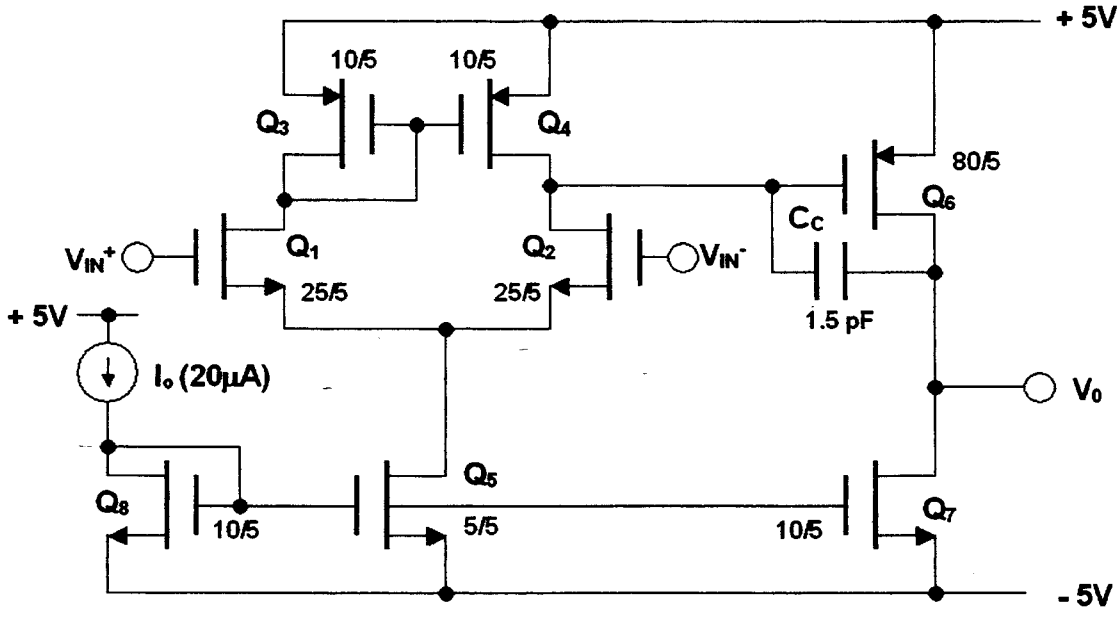

Figure 4.2

5 (a) Give one advantage and one disadvantage of integrated continuous-time filters compared with discrete-time sampled-data filters. [2]

(b) Figures 5.1-5.3 show three sampled-data integrator building blocks. Derive an expression for the transfer function of the integrators of Figure 5.1 and Figure 5.2. All switches are implemented by MOSFETs of equal size. Assume that the integrators are driven by non-overlapping clocks with a clock frequency much higher than the maximum input signal frequency. Also assume the switches are ideal. [10]

(c) Figure 5.3 shows one section of a switched-capacitor ladder filter. Based on this filter structure design a 3rd-order Chebyshev low-pass switched-capacitor filter with a cut-off frequency of 5 kHz and a 1.0 dB pass-band ripple. Assume a clocking frequency of 100 kHz. Passive component values for the L-C prototype, normalised to 1 rad/s, are $C_1 = C_3 = 2.0236$, $L_2 = 0.994$. In your analysis you may assume all integrators to be lossless. [8]

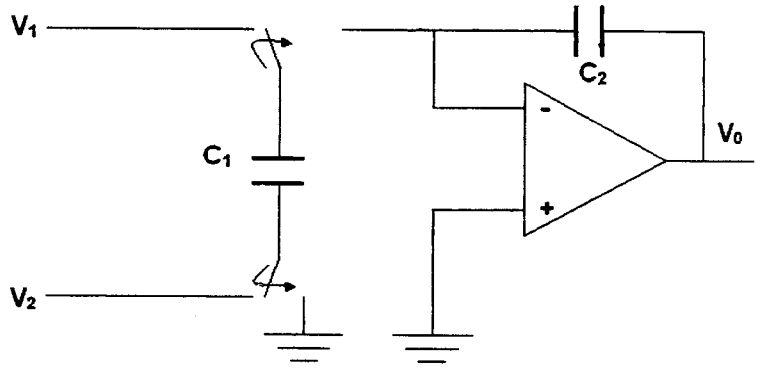

Figure 5.1

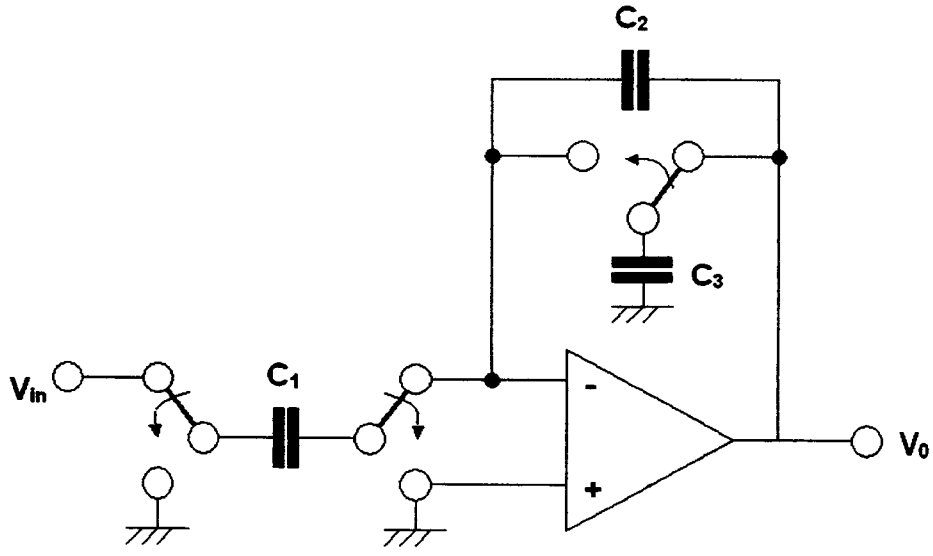

Figure 5.2

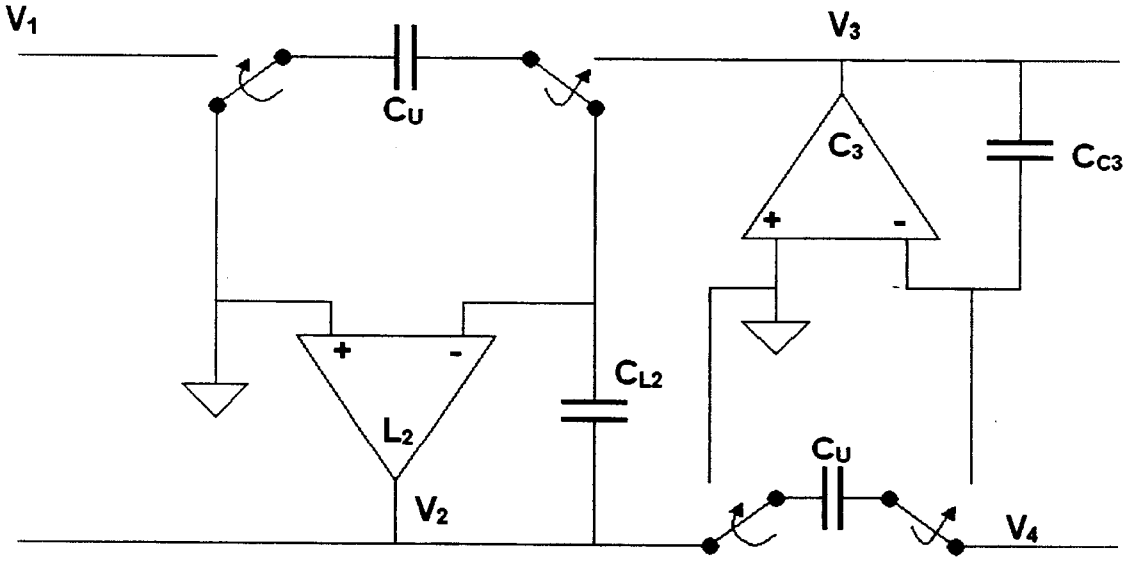

Figure 5.3

6. (a) Two high-performance analogue-to-digital converters are the current-mode algorithmic converter and the sigma-delta converter. Sketch a typical architecture for ONE of these converter types and explain its principles of operation. [9]

(b) Assuming that the maximum resolution of any sampled-data converter is limited by switch noise (KT/C), calculate the maximum resolution of a stereo-audio system running at a sample rate of 40 kHz. Assume a MOSFET switch aspect ratio (W/L) = 1/8, transconductance parameter Kp = 20 $\mu A/V^2$ and a device threshold voltage $V_T = 1$ V. The *on* voltage of the switch is a 5 V reference (i.e. $V_{GS}on = V_{ref} = 5$ V). You may also assume that the switch settles in 10 τ (where τ = time constant) over one period of the clock frequency.

Boltzmann constant $k = 1.38 \times 10^{-23}$ J/K and the ambient temperature is 300 K. [11]

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DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2003

MSc and EEE PART III/IV: M.Eng., B.Eng. and ACGI

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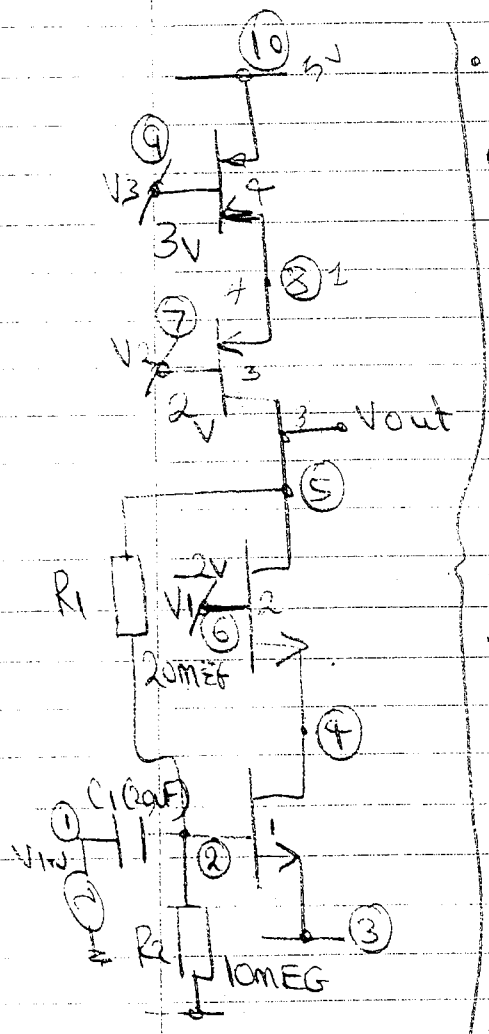
(1) Solutions 2003 3E ANALOG. (1)

Question 1




```
* TITLE INVERTING CMOS AMPLIFIER

C1  1  2    20 E 6
R1  5  2    20MEG
R2  2  3    10 MEG

M1  4  2  3  3  QN  W=5u  L=5u
M2  5  0  4  4  QN  W=5u  L=5u
M3  5  1  8  8  QP  W=14u L=5u
M4  8  9  5  5  QP  W=14u L=5u

Vdd  10  0   5V
Vss   3  0   0V
V1    6  0  -2V
V2    7  0   2V
V3    9  0   3V
Vac   1  0   ac 1

* OP all
* option post
* ac dec 10 1K 10MEG
* PRINT ac VDB(5)
* PRINT ac VP(5)
* END
```

10/10

To calculate output swing assume saturation

$|V_{DS}| \geq |V_{SS}| - |V_{TT}|$ CT

$|V_{DS}|_{Q4} = 1V$, $V_5 = 4V$, $V_2 = 2V$.

Question 1 continued

$|V_{OS}|_{Q3} = 1$

$\therefore V_{O\,max} = (5 - 2) = 3V$

Similarly for negative

$|V_{OS}|_2 = |V_{OS}|_1 = 1,$ (4/4)

$\therefore V_{O(min)} = (-5+2) = -3V$

Cascoding will improve phase margin since the Miller capacitance at the input is reduced thus increasing the non-dominant pole frequency. Also since the output resistance increases the dominant pole frequency will reduce hence the poles will spread and hence the phase-margin will increase. (3/3)

The large passive components are used for DC biassing. Set high output resistance of amplifier at DC bias voltage close to 0 volts. Large values of R are used so that input and output impedance levels are not loaded. 20μF capacitor used to ac couple input. (3/3)

TOTAL 20/20

CF

Q2) Figure 2a is a bandgap voltage - reference, The function is to give a output voltage ref independent of temperature. The function relies upon the band-gap temperature coefficient of V_{BE} $\approx -2.5mV/°C$, under certain conditions that $V_O = 1.283V$, then $dV_O/dt = 0$ This is an important circuit for IC design since it is important that parameter/Performance of a circuit does not drift with temperature, particularly for precision circuit such as data converters.

Fig2b - PTAT (Proportional to Absolute temp) the output current is unduly insensitive to power supply voltage, and the circuit has a low temperature coefficient. Stable operation of ICs is expected over a wide supply voltage range, using a PTAT as the main current reference in a circuit will help achieve this.

Figure 2c is a low headroom CMOS voltage potential divider. The dimensions of the transistors are set to establish the required biasing voltages for a set power supply current.

8/8

For bandgap reference :- $V_{BE1} = V_{BE2} + I_2R_3$ ($\beta \gg 1$)

Since $V_{BE1} - V_{BE2} = V_T \ln(I_1/I_2)$

then $V_O = V_{BE3} + R_2/R_3 V_T \ln I_1/I_2$

4/4

For $dV_O/dt = 0$, then $dV_{BE3}/dT = (V_T/T)\frac{R_2}{R_3}\ln I_1/I_2$

Since $dV_{BE}/dT = -2.5mV°/K$, $V_T/T = K/Q = 1.38\times10^{-23}/1.6\times10^{-19}$

then $(R_2/R_3)\ln(I_1/I_2) = 29$ and so $V_O = 1.283V$. CT

Q2(cont)

TCF of PTAT :-

Ans- PTAT temp coefficient of V_T cancels with negative temperature coefficient of Resistor.

$\therefore$ Tcf $= \frac{1}{V_T}\frac{\partial V_T}{\partial T} - \frac{1}{R}\partial R/\partial T$

$= \frac{1}{T} - 1500\times10^{-6}$ @ room temp

$= 1833 ppm/^{\circ}C$

(4/4)

In the voltage PD of (2c), the magnitude of V_{gs} across each device will determine the active area of that device : $I = \beta(V_{gs} - V_T)^2$, for a fixed current I, the smaller the V_{gs} the larger the value of β. Since $\beta = k'W/2L$ the (W/L) increases. Large V_{gs} values are limited by the supply voltage and so β values can be quite small, leading to small W/L ratios. Small (W/L)s lead to large (WxL) and large active area. Each device in the 4-branch divider will have a smaller V_{gs} than if just two branches are utilized, hence lower active chip area.

CT (4/4)

(3) DDI

$$I_{D1} = 2\beta\left[(V_{C1}-V-V_T)(V_1-V)-\tfrac{1}{2}(V_1-V)^2\right]$$

$$I_{D2} = 2\beta\left[(V_{C2}-V-V_T)(V_1-V)-\tfrac{1}{2}(V_1-V)^2\right]$$

$$I_{D3} = 2\beta\left[(V_{C2}-V-V_T)(V_2-V)-\tfrac{1}{2}(V_2-V)^2\right]$$

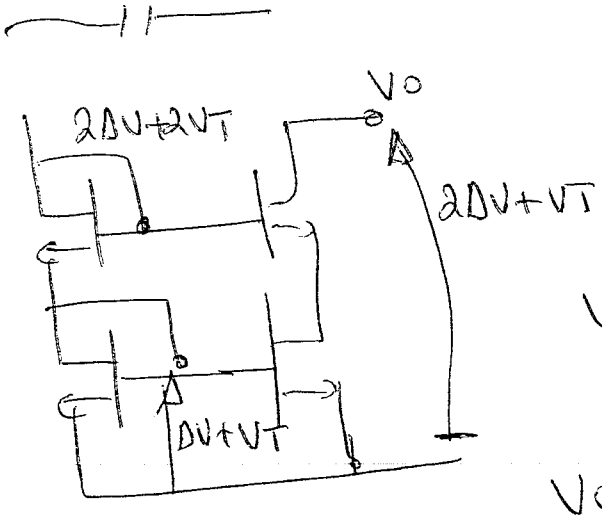
$$I_{D4} = 2\beta\left[(V_{C1}-V-V_T)(V_2-V)-\tfrac{1}{2}(V_2-V)^2\right]$$

Expanding it can be shown that

$$(V_1-V_2)/(I_1-I_2) = \tfrac{1}{2}\beta(V_{C1}-V_{C2}) = R$$

independent of both V_T and V_{DS} terms

Hence $\tau = 2CR = \dfrac{C}{\beta(V_{C1}-V_{C2})}$ (9/9)



Assume

$\Delta V = V_{GS} - V_T$ for sat

$V_{DS} \geq (V_{GS} - V_T)$

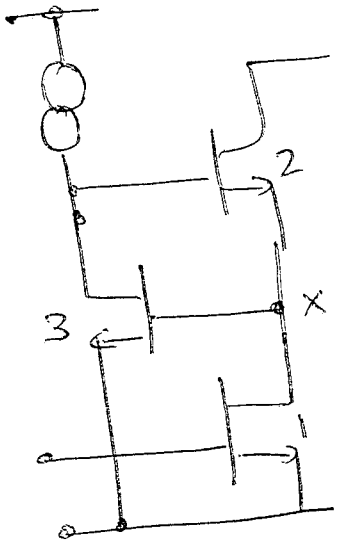
$V_O = V_S - V_T$

$V_{O(max)} = 2(\Delta V + V_T) - V_T$

$= 2\Delta V + V_T$ (5/5)

CT

Qu3 (cont)



Assume standard cascode ensure Vx is reduced in such that Rout $\approx r_{ds1}(g_{m2} r_{ds2})$. By regulating the cascode node x by loop amplifier ($g_{m3} r_{ds3}$) then node x becomes a much better virtual ground. Vx is reduced by a further gain term $g_{m3} r_{ds3}$ increasing Rout

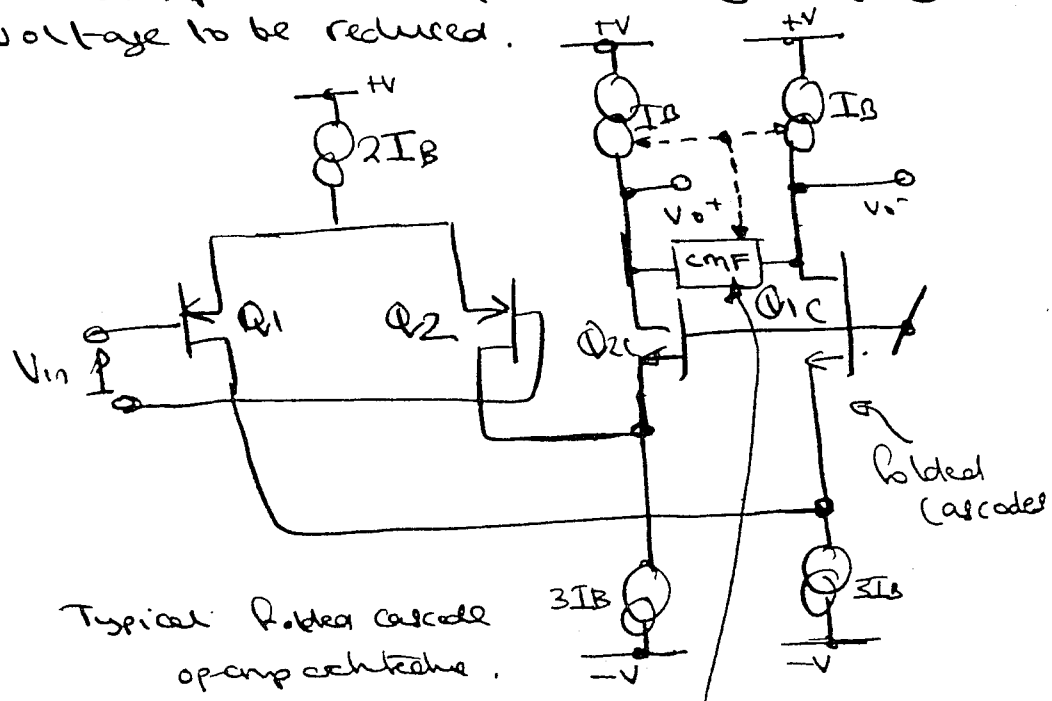
$$\approx r_{ds1} g_{m2} r_{ds2} g_{m3} r_{ds3}$$

$$\approx r_{ds} (g_m r_{ds})^2$$

assuming equal g_m and r_{ds}. (6/6)

CT

Q4. Main advantage of folded cascode is that signal path is folded giving a balance between input and output allowing supply voltage to be reduced. (3/3)



Typical folded cascode op-amp architecture. (5/5)

(2/2) Gain = single-ended $\frac{g_{m1}}{2}\left[\frac{g_{m1c}}{g_{o1c}} \cdot \frac{1}{g_{o1}}\right] \approx \left(g_m/g_o\right)^2 \times \frac{1}{2}$.

Extra marks if common-mode feedback circuit connected.

Single-stage

(1/1) Advantage: High speed
Good phase margin

(1/1) Disadvantage: Lower gain
Low CMVR / output swing

OP-AMP - Figure 4(b)

(1/1) (1/1) Voltage Gain $= -g_{m2}/(g_{o2}+g_{o4})$

$(g_{o2}+g_{o4}) = I_{D2}(\lambda_N+\lambda_P) = 5\times10^{-6} \times 0.05 = 2.5\times10^{-7}$

(1/1) (1/1) $g_{m2} = 2\sqrt{\beta_2 I_{D2}} \Rightarrow \beta_2 = \frac{k'_{pp}}{2}\left(W/L\right)_2 = 7.5\times10^{-5}$ A/V²

CT

$g_{m2} = 3.87 \times 10^{-5} S$, $A_1 = -154.9$.

$A_2 = -g_{m6}/(g_{o7} + g_{o6})$

$(g_{o7} + g_{o6}) = I_{D6}(\lambda_N + \lambda_P) = 20 \times 10^{-6} \times 0.05$
$= 10 \times 10^{-7} \Omega^{-1}$ (1/1) (2/2)

$g_{m6} = 2\sqrt{\beta_6 I_{D6}} \Rightarrow \beta_6 = \frac{K_P}{2}\left(\frac{W}{L}\right)_6 = 1.6 \times 10^{-4} A/V^2$

$g_{m6} = 1.13 \times 10^{-4}$, $A_2 = -113$.

(1/1) (2/2) $A_{TOTAL} = A_1 A_2 = 17503 \triangleq 86$ dB.

(1/1) (2/2) G.B product: $g_{m2}/2\pi C_c = 4.1$ MHz.

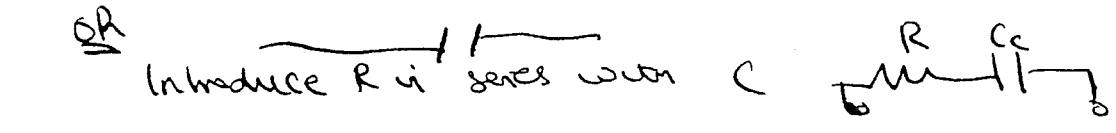
Last Part

To increase gain and G.B product then W1 and W2 should be increased. To increase Slew-rate Is ~~reduced~~ increased OR Cc reduced (either).

(3/3) Sequence

1/ Increase Is → slew rate increases
2/ Increase Ws → increase gain and G.B product.

OR



Introduce R in series with C

(3/3) Its function is to provide feedforward compensation and eliminate the R.H.P zero in the op-amps transfer function. Zero is given by $Z = -g_{m6}/C_c$ → with R given $Z = -1/(g_{m6} - R)C_c$. Improves ϕ by setting $Z = P_2 = 2nd$ Pole.

4 + 2 FBs

CT

Q4 5/6 (9)

Advantages of Continuous-time
speed, simplicity, power consumption

disadvantages
Accuracy, linearity, noise

2/2

Figure 6(a) 5

During ϕ_1 $\quad Q = C_1[V_1 - V_2]$

$I_{av} = f_c C_1 [V_1 - V_2]$

f_c = clock frequency

$\phi_2 \Rightarrow$

$I_{av} = -f_c C_1 [V_1 - V_2]$

$\therefore V_o = \left(\frac{-1}{j\omega C_2}\right) f_c C_1 [V_1 - V_2]$

$\therefore \frac{V_o}{(V_1 - V_2)} = \left[\frac{-f_c C_1}{j\omega C_2}\right] \Rightarrow \tau = \frac{C_2}{C_1 f_c}$

5/6

Accuracy determined by capacitor ratio.

Figure 6(b) 5

During ϕ_1 $\quad Q = C_1(V_{IN}) \Rightarrow I_{AV} = f_c C_1 V_{IN}$

During ϕ_2

$$I_{av} = -[f_c C_3 V_o + j\omega C_2 V_o]$$

$$\therefore f_c C_1 V_{IN} = -[f_c C_3 V_o + j\omega C_2 V_o]$$

$$V_{IN} = -\left[\frac{C_3}{C_1} V_o + \frac{j\omega C_2}{f_c C_1} V_o\right]$$

5/6

CT

(10)

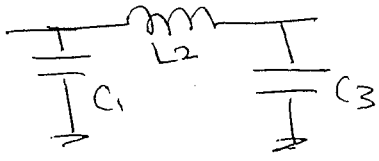
Cont
5
Reorge

$$\frac{V_o}{V_{in}} = \left(\frac{C_1}{C_3}\right) \frac{1}{\left(1 + \frac{C_2 j\omega}{C_3 f_c}\right)}$$

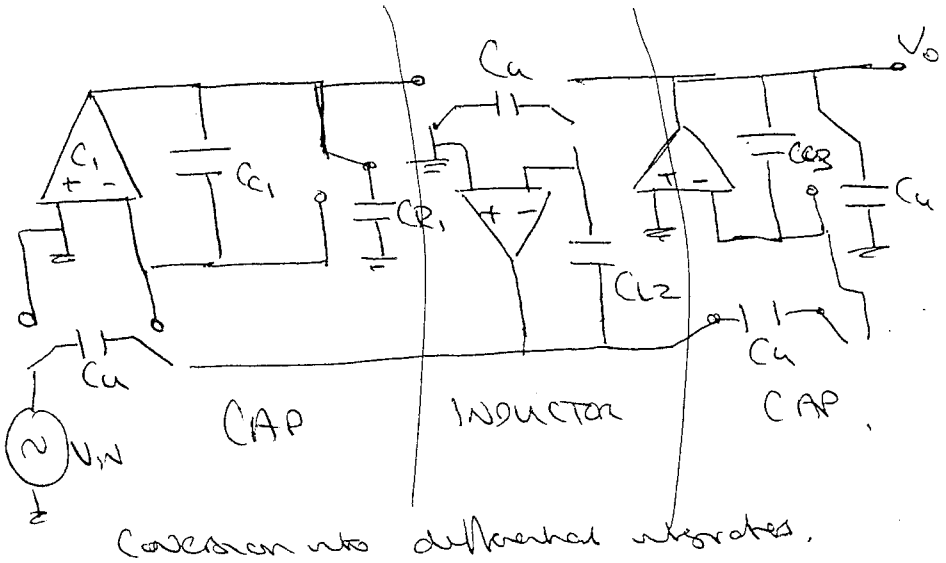
$$\therefore \gamma = \frac{C_2}{C_3 f_c}$$

Q4 / 5

Section of LCR prototype.



General transformation Rules (not really required but the bright students may include)



3/4

Conversion into different integrates.

Inductor transformation

$(L_2/R_S) f_c = C_{L2}/C_u$

Capacitor Transformation.

$C_3/C_u = f_c R_S C_3$

where R_S is normalising during scaling resistor. Assuming $R_S = 1$

$C_1/C_u = f_c C_1$
$C_{C3}/C_u = f_c C_3$
$C_{L2}/C_u = f_c L_2$

} general transformation.

CT

Q4 Q5. (12)

Table values of C_1, L_2 and C_3 are normalized to 1 rad/s $\div 2\pi f_p$ ($f_p = 5\,kHz$)

$$C_1 = C_3 = 2.0236/(2\pi 5\times10^3) = 6.44\times10^{-5}\,F$$
$$L_2 = 0.1994/(2\pi 5\times10^3) = 3.164\times10^{-5}\,F$$

for termination resistors assume $C_{in} = C_{R1} = C_{RO} = 1pF$

then $\begin{bmatrix} C_1 - C_3 = 6.44pF \\ C_2 = 3.164pF \end{bmatrix}$ ∴

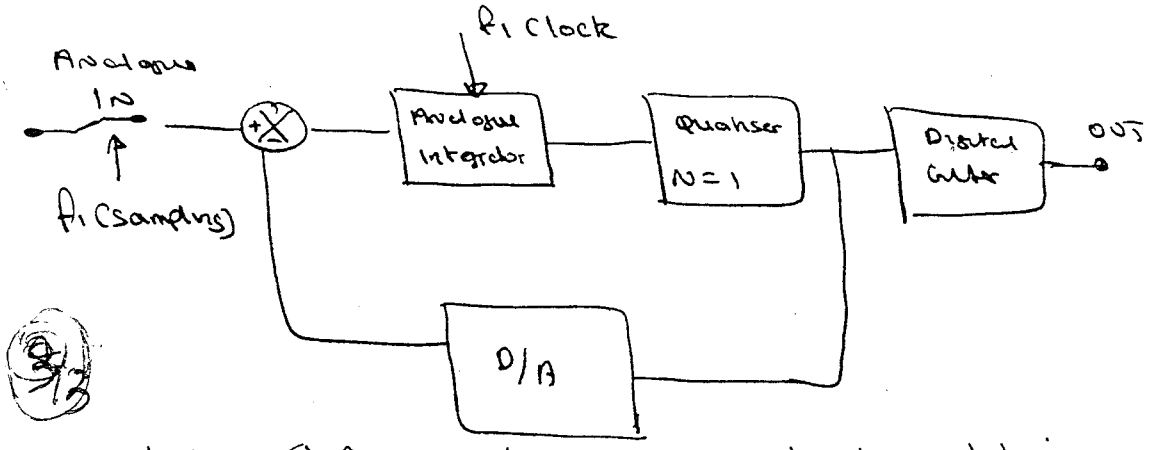
4/4

20/20

CT

Q u 5 6 (13)

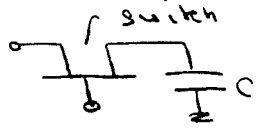
Σ-Δ oversampled - Converter.



(8/12)

In the Σ-Δ modulator, coarse quantisation at high sampling rate is combined with negative feedback and digital filtering to achieve increased resolution at low sampling rates. This reduces requirements upon component accuracy. The circuit includes a negative feedback loop producing a coarse estimate that oscillates about the true value of input, the digital filter averages this coarse estimate to produce a finer approximation. The feedback A/D and integrator force the quantisation error to have a high frequency spectrum. The (6/6) output of the digital filter is down sampled and gives a multi bit digital representation. All high frequency quantisation noise is strongly reduced.

Dynamic Range $\triangleq V_{ref}/Noise = 2^N$.



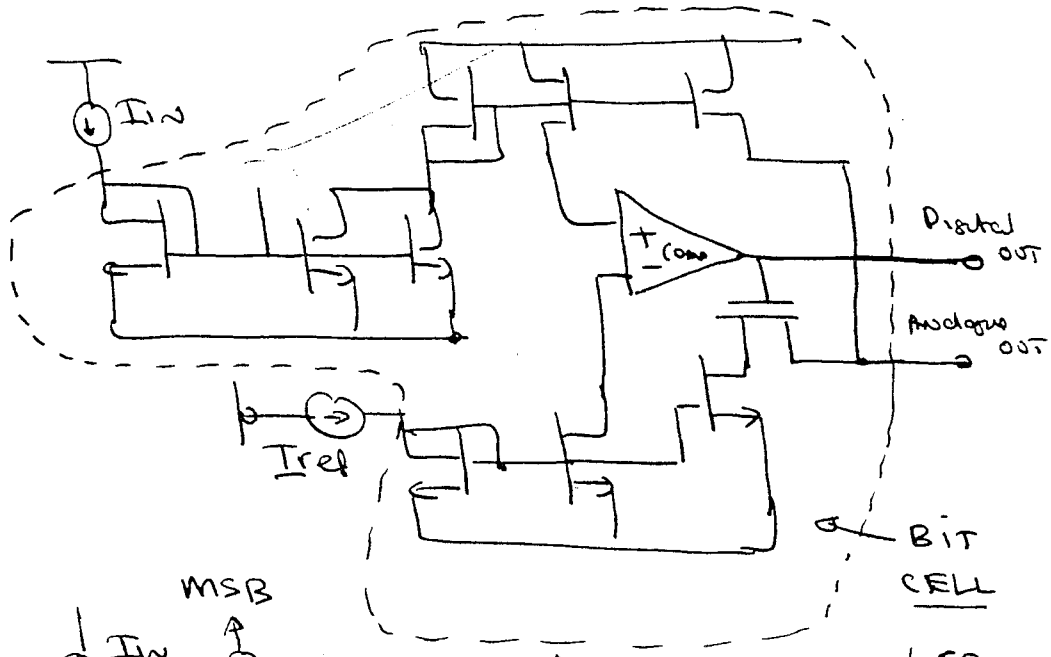
RMS noise of switch $= \sqrt{\frac{KT}{C}}$ $\therefore DR = \frac{V_{ref}}{\sqrt{KT/C}} = 2^N$

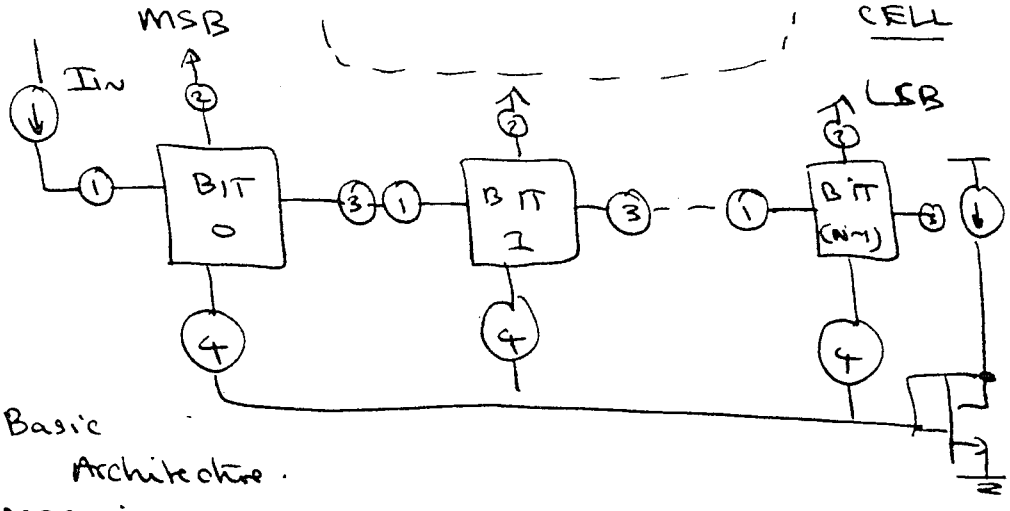
(6/6) Assume $f_c = (1/10RC)$ for switch ie switch settles within 5 time constants/, over which time of pairs can solving for C gives, $2^N = D.R = V_{ref}/\sqrt{KT \times 10 \times R f_c}$ ⇒ next page.

CT

Q5 (6) cont

Algorithmic Current-mode Converter





Basic Architecture.

OPERATION

2 I_{IN} or +ve terminal of comparator compares with Iref (-ve) terminal. If $2I_{IN} < I_{ref}$, comp output goes low, digital output = 0 and Analogue output = $2I_{IN}$. If $2I_{IN} > I_{ref}$, comp output goes high, digital output = 1, analogue output $2I_{IN} - I_{ref}$. Analogue output continuously feeds into following bit cell which performs exactly the same function. The process is continued as many times as necessary to achieve the desired resolution.

CT

Q6 (cont)

R = on resistance of switch which from triode region

$$I = 2\beta(v_{gs} - V_T)(v_{ds})$$

(3) $-\partial I/\partial v_{ds} = 1/R_{on} = 2\beta(v_{gs} - V_T)$

$\beta = \left(\frac{KW}{2L}\right) = 1.25 \times 10^{-6}$, $v_{gs} = 5V$

$R_{on} = 400K\Omega$

(2) $\therefore 2^N = DR \approx 388 \times 10^3 \Rightarrow$ 18.56 bits

OR 19 bits

acceptable.

TOTAL 20/20

CT