UNIVERSITY OF LONDON

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 1998

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
BSc Honours Degree in Mathematics and Computer Science Part I
MSci Honours Degree in Mathematics and Computer Science Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the
Associateship of the Royal College of Science
Associateship of the City and Guilds of London Institute

PAPER 1.4 / MC1.4

ARCHITECTURE I

Monday, May 11th 1998, 4.00 - 5.30

Answer THREE questions

For admin. only: paper contains 4 questions

1a List 6 features of main memory.

b Define the terms big-endian and little-endian when applied to main memory. For each case show how the hex value D1C2B3A4 would be stored at byte address 40.

c Suppose that a 8 Megabyte memory is built using 512K x 8-bit RAM chips and that memory words are 16-bit. The memory is byte-addressable.

For this organisation of memory evaluate:

i) the number of RAM chips

ii) the number of banks

iii) the number of address lines needed for a RAM chip

iv) the number of address lines needed for the 8 Megabyte memory

In which bank would the memory word with byte address 44 be found when the memory system uses:

v) high-order interleave?

vi) low-order interleave?

Assume banks are numbered from 0.

d Suppose that an architecture has a 16-bit instruction register and all instructions are 16-bits. What would the effect of an 8-bit data bus be? How could the architecture exploit a 32-bit data bus?

The four parts carry, respectively, 30%, 20%, 30% and 20% of the marks.

2a For each of the following Intel x86 addressing modes, give the assembler syntax; describe its meaning in English; and give a situation when it is typically used:

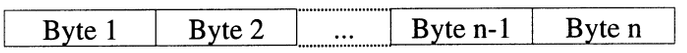
i) Register Relative

ii) Based Index

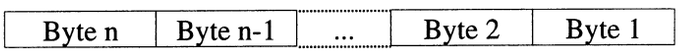
iii) Based Relative Index

b The instruction set for Tiny-8086 is defined below. Write a sequence of *commented* Tiny-8086 instructions to reverse the bytes in a memory block:

Memory Block Before Reversal



Memory Block After Reversal



Assume that register SI holds the offset in the data segment of the first byte in the memory block and that register AX holds the number of bytes in the memory block.

Tiny-8086 supports a subset of the 8086 architecture. Tiny-8086 is limited to registers AX, SI, and DI. The only addressing modes supported are Register, Register Indirect and Immediate. The only instructions supported are:

```
MOV dest, src    (dest := src)
ADD dest, src    (dest := dest + src)
SUB dest, src    (dest := dest – src)
CMP dest, src    (Compare dest and src)
JG  label        (Jump to label if Greater)
JMP label        (Jump to label)
```

The two parts carry, respectively, 45% and 55% of the marks

Turn over ...

3 Suppose that the IEEE defined a new 16-bit floating point format called Tiny Precision that is the same as the IEEE Single Precision format except that the Exponent is 5 bits and held as Bias 15 and the Significand is 10 bits.

	1 bit	5 bits	10 bits
Tiny Precision Format	Sign S	Exponent E	Significand M

a For this format give:

i) the formula for representing decimal values in terms of S, E and M

ii) the approximate number of decimal digits of precision

iii) the unbiased exponent range.

b Convert the decimal number 5.25 to Tiny Precision format indicating clearly the steps taken.

c Convert the decimal number 3.1 to Tiny Precision format indicating clearly the steps taken.

d Carry out the subtraction 5.25 – 3.1 in Tiny Precision format indicating clearly the steps taken. Note: Conversion of the result from Tiny Precision format back to decimal is NOT required.

e Why might floating point arithmetic not be suitable for monetary (e.g. £12.45) calculations? What alternative representation could be used?

The five parts carry, respectively, 20%, 20%, 20%, 20% and 20% of the marks.

4a Describe how an interrupt is handled by the Intel x86 architecture from the time an I/O controller is ready for a transfer to the time that its interrupt handler is called.

b Identify the key problem with interrupt-driven I/O.

c Explain why a DMA controller has priority over the CPU when both request a memory transfer.

d Suppose that I/O devices can be assigned priorities e.g. between 0 (Low) and 7 (High). How might a CPU use such priorities for interrupt processing. Order the priorities for the following three I/O devices: a hard disk, a modem and a printer and give a reason for your order.

The four parts carry, respectively, 30%, 20%, 20% and 30% of the marks.

End of paper