EE4-17
EE9-AO4

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2016

MSc and EEE PART IV: MEng and ACGI

Corrected copy

HIGH PERFORMANCE ANALOGUE ELECTRONICS

Tuesday, 10 May 10:00 am

Time allowed: 3:00 hours

There are FOUR questions on this paper.

Answer ALL questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s) :	E. Rodriguez-Villegas
	Second Marker(s) :	P. Georgiou

The Questions

1. (a) Explain the concept of Noise Factor (NF).

[4]

(b) Explain mathematically why the first block in system is the most critical one in terms of noise.

[4]

(c) Find an expression for the Noise Factor of a cascade of four circuit blocks, each with consecutive Noise Factors F1, F2, F3 and F4, and respective power gains of G1, G2, G3 and G4.

[4]

(d) Find an expression for the NF of a circuit which:

- is built with an input n-type MOS transistor;
- has a resistor of 1kHz as a load; changed to 1kΩ at 10.16
- and is driven by a voltage source with a 50Ω impedance;

Use the small signal parameters and assume that:

- The bandwidth of operation of the circuit is between 100kHz and 150kHz.
- There is no gate leakages.
- The transistor is operating in the strong inversion saturation region.

[4]

(e) As a designer, what would you do to improve the noise performance of the circuit described in (d)? Briefly justify your answer.

[4]

2. (a) Explain why having a differential configuration can be beneficial when designing transconductors.

[4]

(b) Explain how you would build a transconductor with one transistor, two transistors and four transistors, and what are the advantages and disadvantages of each topology. You can use other components in addition to the transistors if you wish.

[5]

(c) A comparator is a two input circuit that produces a larger voltage if one specific input is larger than the other and a low voltage if the opposite happens. How would you build a comparator using a transconductor as a core block?

[2]

(d) How would you design an integrator with:

1- Two n-type MOS core transistors with gm=200nA/V.
2- A biasing current of 100nA.
3- A transfer function equal to 1/(10s).

Give the value of the integrating capacitance. Transistors sizes are optional.

[5]

(e) The input referred noise of the integrator in (d) is 2μVrms, integrated in a 100kHz to 150kHz band. What would be the value of the input referred noise for the same circuit but in the 100kHz to 200kHz band?

[4]

3. (a) Draw the schematic of a differential pair with source degeneration.

[3]

(b) The current for an n-channel MOS transistor biased in the weak inversion saturation region with its source and bulk grounded and its drain voltage $V_{DS}>4U_T$ is approximately given by:

$$I_D = I_s \exp(\frac{V_{GS}}{\eta U_T})$$

The transistors in a differential pair with source degeneration are operating in the weak inversion region. The biasing current for the circuit is 1uA, η is approximately 1 and U_T=25mV. Which one of the following three values of resistances would you choose for the degeneration, and why: 1kΩ, 100kΩ and 1000kΩ.

[3]

(c) For the circuit in (b) give general expressions for the power spectral density of significant noise sources in the input transistors. Do not give expressions for those sources that can be neglected. Assume that:

- The transistors have no leakage currents
- The bandwidth of operation is between 40Hz and 50Hz
- The thermal noise of the transistors is negligible.

[3]

(d) Without making any calculation, how much bigger is the input referred noise in the circuit in (b) if 100k and 1000M resistances are used instead of a 1kΩ one. Assume that:

- The transistors have no leakage currents
- The bandwidth of operation is between 40KHz and 50KHz
- The thermal noise of the transistors is negligible.

[3]

(e) Can the circuit in (b) be used as a mixer? If your answer is yes explain how. If your answer is no explain why.

[3]

(f) Draw the schematic of a bipolar mixer built with differential pairs.

[3]

(g) The circuit in (e) is built with MOS transistors in weak inversion as opposed to bipolar (refer to (b)), and it operates in a 10Hz to 50Hz bandwidth. If you were not area limited, how would you dimension your transistors to improve your noise performance. Briefly explain why.

[2]

4. (a) Briefly explain the superheterodyne principle

[4]

(b) The RF signal received by a receiver is centred in 10.7MHz and has a bandwidth of 10KHz. The local oscillator used to downconvert the signal generates a tone at 11MHz. What is the frequency range of the image signal?

[4]

(c) What would be the theoretical optimum length of an antenna which has to receive a signal centred at 2.4GHz.

[4]

(d) Briefly explain the basis of a direct conversion receiver.

[3]

(e) Briefly explain why filters are used between the local oscillator and the mixer.

[3]

(f) Explain how a subsampling receiver works.

[2]