EE3-11
EE9-AO8

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2015-16

MSc and EEE PART III/IV: MEng, BEng and ACGI

ADVANCED ELECTRONIC DEVICES

Corrected copy

Tuesday, 8 December 9:00 am

Time allowed: 3:00 hours

There are FIVE questions on this paper.

Answer Question One and THREE other questions.

All questions carry equal marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : K. Fobelets
Second Marker(s) : S. Lucyszyn

Special instructions for invigilators

Q1 is compulsory

Special instructions for students

Q1 is compulsory.

Constants

permittivity of free space:	$\varepsilon_o = 8.85 \times 10^{-12}$ F/m
permeability of free space:	$\mu_o = 4\pi \times 10^{-7}$ H/m
intrinsic carrier concentration in Si:	$n_{i\,Si} = 1.45 \times 10^{10}$ cm^{-3} at $T = 300$ K
intrinsic carrier concentration in GaAs:	$n_{i\,GaAs} = 1.79 \times 10^{6}$ cm^{-3} at $T = 300$ K
intrinsic carrier concentration in InAs:	$n_{i\,InAs} = 1 \times 10^{15}$ cm^{-3} at $T = 300$ K
intrinsic carrier concentration in $Al_xGa_{1-x}As$:	$n_{i\,AlGaAs} = 2.1 \times 10^{3}$ cm^{-3} for x = 0.3 at $T = 300$ K
dielectric constant of SiO_2:	$\varepsilon_{ox} = 4$
dielectric constant of Si:	$\varepsilon_{Si} = 12$
dielectric constant of GaAs:	$\varepsilon_{GaAs} = 13$
dielectric constant of InAs:	$\varepsilon_{InAs} = 15$
dielectric constant of $Al_xGa_{1-x}As$:	$\varepsilon_{AlGaAs} = 13 - 2.84\ x$
electron affinity of Si	$\chi_{Si} = 4.05$ eV
electron affinity of GaAs	$\chi_{GaAs} = 4.1$ eV
electron affinity of InAs	$\chi_{InAs} = 4.9$ eV
electron affinity of AlAs	$\chi_{AlAs} = 3.6$ eV
electron affinity of $Al_xGa_{1-x}As$	$\chi_{AlGaAs} = 4.07 - 1.1\ x$ eV for $x < 0.45$
band gap of Si:	$E_{G\,Si} = 1.12$ eV
band gap of GaAs:	$E_{G\,GaAs} = 1.42$ eV
band gap of InAs:	$E_{G\,InAs} = 0.36$ eV
band gap of $Al_xGa_{1-x}As$:	$E_{G\,AlGaAs} = 1.42 + 1.247\ x$ eV for $x < 0.45$
effective density of states of Si:	$N_{C\,Si} = 2.8 \times 10^{19}$ cm^{-3}
	$N_{V\,Si} = 1.04 \times 10^{19}$ cm^{-3}
effective density of states of GaAs:	$N_{C\,GaAs} = 4.72 \times 10^{17}$ cm^{-3}
	$N_{V\,GaAs} = 9.0 \times 10^{18}$ cm^{-3}
effective density of states of InAs:	$N_{C\,InAs} = 8.7 \times 10^{16}$ cm^{-3}
	$N_{V\,InAs} = 6.6 \times 10^{18}$ cm^{-3}
effective density of states of $Al_xGa_{1-x}As$:	$N_{C\,AlGaAs} = 7.5 \times 10^{18}\ (0.063+0.083\ x)^{3/2}$ cm^{-3} for $x < 0.41$
	$N_{V\,AlGaAs} = 1.76 \times 10^{19}\ (0.51+0.25\ x)^{3/2}$ cm^{-3}
thermal voltage:	$kT/e = 0.026$V at $T = 300$ K
charge of an electron:	$e = 1.6 \times 10^{-19}$ C (1 eV)

Table 0: Workfunction of metals

metal	ϕ (eV)
Al	4.08
Ni	5.01
Ti	4.33
W	4.6

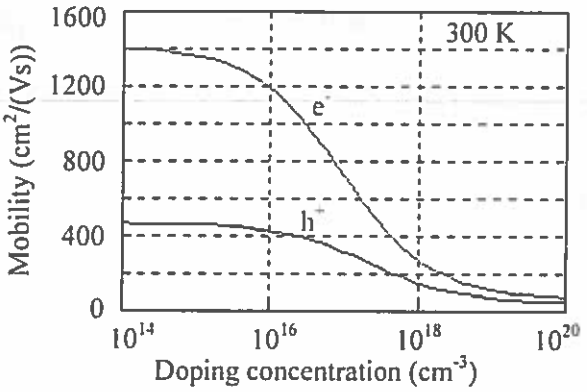

Figure 0: Electron and hole mobility in Si as a function of doping concentration.

Formulae list

$$p = N_v e^{(E_v - E_F)/kT}$$
$$n = N_c e^{(E_F - E_c)/kT}$$

Carrier density – Fermi-Dirac statistics

$$J_n(x) = e\mu_n n(x)E(x) + eD_n \frac{dn(x)}{dx}$$
$$J_p(x) = e\mu_p p(x)E(x) - eD_p \frac{dp(x)}{dx}$$

Drift – diffusion current density equations for electrons, J_n and holes, J_p

$$I_{DS} = \frac{\mu C_{ox} W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right)$$

Strong inversion MOSFET current

$$V_{th} = \phi_m - \phi_s + 2\times\phi_F + \gamma\times\sqrt{2\times\phi_F}$$

Threshold voltage

$$\phi_F = \frac{kT}{e}\ln\left(\frac{N_A}{n_i}\right)$$

Fermi potential

$$\gamma = \frac{\sqrt{2e\varepsilon_s N_A}}{C_{ox}}$$

Body effect coefficient

$$J = \frac{eD_n n_p}{L_n}\left(e^{\frac{eV}{kT}} - 1\right) + \frac{eD_p p_n}{L_p}\left(e^{\frac{eV}{kT}} - 1\right)$$

Diode diffusion current density

$$V_{bi} = \frac{kT}{e}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Built-in voltage pn diode

$$W_{depl}(V) = \left[\frac{2\varepsilon(V_{bi} - V)}{e}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]^{1/2}$$

Depletion width in pn diode

$$S = \frac{dV_{GS}}{dLog(I_{DS})}$$

Sub-threshold swing

$$c = c_0 \exp\left(\frac{eV}{kT}\right) \text{ with } \begin{cases} c = p_n \text{ or } n_p \\ c_0 \text{ bulk minority carrier concentration} \end{cases}$$

Minority carrier injection under bias V

$$\delta c = \Delta c \exp\left(\frac{-x}{L}\right) \text{ with } \begin{cases} \delta c = \delta p_n \text{ or } \delta n_p \\ \Delta c \text{ the excess carrier concentration} \\ \text{at the edge of the depletion region} \end{cases}$$

Excess carrier concentration as a function of distance

$$L = \sqrt{D\tau}$$

Diffusion length

$$D = \frac{kT}{e}\mu$$

Einstein relation

1. Compulsory question.

a) Sketch the energy band diagram, including E_F, E_c, E_v and E_i, of an n-channel enhancement mode MOSFET at threshold. Label energy bands and axes. [4]

b) Give the voltage and charge balance equations across the gate for the MOSFET in question 1a). Explain the origin and sign of all parameters that you use. [4]

c) For the MOSFET in 1a), give the expression for the surface potential, V_s and the surface carrier density, n_s as a function of the Fermi potential, $\phi_F = E_i - E_F$. Define all parameters that you use. [4]

d) Figure 1.1 gives the material cross section of a planar MOSFET. [4]

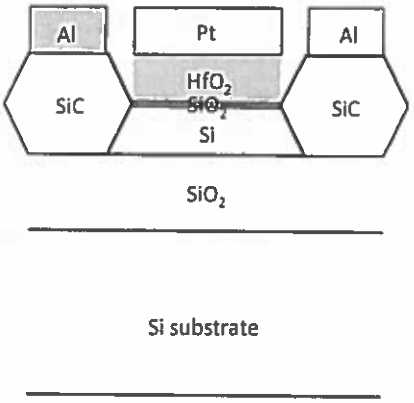

Figure 1.1: Planar MOSFET.

Different adaptations are implemented to the MOSFET in Figure 1.1 compared to the classical MOSFET. Identify these adaptations and briefly explain the mechanism that underpins the speed benefit in each case. [8]

e) Give the main reason for the higher electron carrier mobility in an AlGaAs/GaAs HEMT, when compared to a GaAs MESFET, with the same gate geometry and ohmic contact doping. [1]

2. JFET & MESFET

A JFET and a MESFET are both defined on a substrate of intrinsic GaAs with the same geometrical structure and doping. The channel layer is 200 nm thick GaAs with a doping density of $N_D = 10^{17}$ cm^{-3}. The ohmic contact regions are doped $N_D = 10^{20}$ cm^{-3} to a depth of 200 nm. The gate of both devices is deposited to be self-aligned to the source and drain regions.

The gate for device A is a 100 nm GaAs layer with a doping of $N_A = 10^{20}$ cm^{-3}.

The gate for device B is a 100 nm tungsten (W) layer.

a)

i) Identify devices A and B. [2]

ii) Show that the gate leakage current in the JFET is lower than that in the MESFET by comparing their built-in voltages. [4]

b)

i) Derive the expression for the pinch-off voltage V_p for $V_{DS} = 0$ V. [5]

ii) Calculate the threshold voltage, V_{th} for the JFET. [4]

c)

i) Draw the energy band diagram of both the JFET and the MESFET from gate to bulk for forward and reverse bias. Indicate the carrier flow across the junction in all cases. [8]

ii) Which of the two devices has the highest switching speed? Give a brief reason. [2]

3. Consider a HEMT.

a) The workfunction of intrinsic InAs and intrinsic GaAs is 5.02 eV and 4.78 eV respectively. Calculate the work function of n-doped $Al_{0.3}Ga_{0.7}As$ with $N_D = 5\ 10^{17}\ cm^{-3}$. [5]

b) Sketch the variation of the conduction band, E_c with respect to the Fermi level, E_F of an n-AlGaAs/un-GaAs n-channel HEMT (unbiased). The energy band diagram should be drawn from gate into the bulk. [5]

c) Sketch the variation of the conduction band, E_c with respect to the Fermi level, E_F of an n-AlGaAs/un-InAs/un-GaAs n-channel HEMT (unbiased). Ignore any strain effects. The energy band diagram should be drawn from gate into the bulk. [5]

d) Which of the two HEMTs, (b) or (c), will have:

i) The highest threshold voltage? [3]

ii) The highest speed? [2]

Give a brief reason in each case.

e) Give a practical implementation (the material cross section) for a Si-based n-channel heterojunction FET that exploits the operation principle of the HEMT. [5]

4. MOSFET TCAD and performance parameters.

```
    # MOSFET script
1   math numThreads = 2
2   line x loc=0 spa=0.1 tag=top
3   line x loc=4 spa=0.1 tag=bottom
4   line y loc=0 spa=0.1 tag=left
5   line y loc=3 spa=0.1 tag=right
6   region Silicon xlo=top xhi=bottom ylo=left yhi=right
7   init concentration=1e16 field=Boron wafer.orient=100
8   diffuse temp=900 time=0
9   struct smesh=substrate
10  refinebox min={0 0} max={1.0 3} xrefine=0.1  yrefine=0.1
11  refinebox min={0 0} max={0.5 3} xrefine=0.05 yrefine=0.05
12  refinebox min={0 0} max={0.3 3} xrefine=0.02 yrefine=0.02
13  grid remesh
14  mask name=source_drain_mask left=1 right=2
15  mask name=gate_mask         left=1 right=2 negative
16  deposit material={Oxide} type=anisotropic Phosphorus conc=5e21 thickness=1
17  photo mask=source_drain_mask thickness=1
18  etch material={Oxide} type = anisotropic thickness=1
19  strip Photoresist
20  diffuse temp=1000 time=60<s>
21  etch material={Oxide} type=anisotropic thickness=1
22  deposit material={Oxide} type=anisotropic thickness=0.01
23  refinebox min={-0.02 0.95} max={0.01 1.05} xrefine=0.005 yrefine = 0.005
24  grid remesh
25  photo mask=gate_mask thickness=0.01
26  etch material= {Oxide} type= anisotropic thickness=0.01
27  strip Photoresist
28  contact name=bulk   box silicon  bottom
29  contact name=source box silicon  xlo=0     xhi=0     ylo=0   yhi=0.5
30  contact name=drain  box silicon  xlo=0     xhi=0     ylo=2.5 yhi=3
31  contact name=gate   box Oxide    xlo=-0.02 xhi=-0.01 ylo=1   yhi=2
32  refinebox min={-0.02 0} max={-0.01 3} xrefine=0.005 yrefine=0.005
33  grid remesh
34  struct smesh=MOSFET_2D
```

Figure 4.1: TCAD MOSFET script with line numbers at the left of the box.

a) TCAD questions related to the script in Figure 4.1.

i) Draw the *x*-*y* axis and add the dimensions of the substrate. [2]

ii) Give the thickness of the gate oxide. [2]

iii) What does the command "`grid remesh`" mean? [1]

iv) Rewrite the lines that need to be adapted to define a self-aligned MOSFET with a gate length of 500 nm. Ensure the device remains symmetric. [5]

QUESTION IS CONTINUED ON NEXT PAGE

V_{th} lin	V_{th} sat	DIBL	SS	g_o	I_{ON}/I_{OFF}
0.545 V	0.495 V	34 mV / V	72 mV / dec	3.78 µS	$6.3*10^9$

Figure 4.2: The simulated performance parameters of the MOSFET. V_{th} threshold voltage, lin: linear region, sat: saturation region, DIBL: drain induced barrier lowering, SS: sub-threshold swing, g_o: output conductance and I_{ON}/I_{OFF} the ratio of the on over the off currents.

b) Parameters extracted from MOSFET characteristics are given in Figure 4.2.

i) Give the formula to calculate DIBL. [2]

ii) Plot appropriate current-voltage characteristics for the MOSFET to illustrate the impact of DIBL. [3]

iii) Derive the expression of SS in function of MOSFET capacitances when no interface charge is present in the oxide. [5]

iv) Give the difference between the minimum possible value of SS at 300K and the measured value of SS. [2]

v) Sketch the appropriate current-voltage characteristics that identifies the difference between an ideal MOSFET and the measured MOSFET with respect to g_o. [3]

5. Read the paper and answer the questions. The figures are withheld on purpose.

CMOS Scaling for the 22nm Node and Beyond: Device Physics and Technology

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ABSTRACT

This paper reviews options for CMOS scaling for the 22nm node and beyond. Advanced transistor architectures such as ultra-thin body (UTB), FinFET, gate-all-around (GAA) and vertical options are discussed. Technology challenges faced by all architectures (such as variation, resistance, and capacitance) are analyzed in relation to recent research results. The impact on the CMOS scaling roadmap of system-on-chip (SOC) technologies is reviewed.

ADVANCED TRANSISTOR OPTIONS

For the past 40 years, relentless focus on Moore's Law transistor scaling has delivered ever-increasing transistor performance and density (Figs. 1 and 2, [1]). Maintaining Moore's Law density scaling will require continued improvement in transistor short channel properties. A variety of device architectures to improve short channel effects (SCE) are being evaluated. The most straightforward are devices which provide SCE improvement by using a planar, thin body (T_{si}), silicon-on-insulator (SOI) architecture (Fig. 3). (a) These include ultra-thin body (UTB) SOI, extremely-thin (ET) SOI and fully-depleted (FD) SOI devices. UTB SOI devices possess improved SCE, potential for improved random dopant fluctuation (RDF) and the possibility for body bias (with thin buried oxide, BOX). (b) Challenges of UTB SOI include thin T_{si} effects (external resistance, R_{ext}, scattering, and quantum confinement changes in threshold voltage, V_T), as well as difficulties in inducing strain and manufacturing challenges with the thin T_{si}. More complex are multiple gate FET (MuGFET) devices. These include (see Fig. 4) (c) FinFET, Trigate, Pi-gate and Omega-FET devices. All the MuFGET devices have similar SCE and RDF advantages over planar (Fig. 5) as do the UTB SOI devices. In addition, the increased confinement in comparison with UTB devices relaxes the manufacturing constraints (width, $W_{si} \sim 2T_{si}$). Furthermore, tying the gates together provides nearly ideal sub-threshold slope. Note also that independent gate (d) operation is possible in some of these architectures. However, MuGFET devices share the strain and R_{ext} challenges of UTB devices. In addition, these devices face challenges posed by the vertical topography, tight diffusion pitches and complex gate patterning. Even more complex than MuGFETs are gate-all-around (GAA) devices (Fig. 6). GAA devices offer the best potential solution to SCE challenges. However, these devices face significant challenges. Not only do they have the strain, R_{ext}, vertical topography, tight pitch, and complex gate patterning challenges of the MuGFET devices, they also face new challenges with gate conformality, excess parasitic capacitance and small-dimension scattering effects. Finally, 3'D devices (Fig. 7) represent an alternative scaling solution, with a potential 50% improvement in density, reduced capacitance, and enablement of new materials and circuit concepts. However, vertical devices share many of the challenges of MuGFET devices, plus the additional challenges of 3'D thermal processing, lithography and contact fabrication.

CHALLENGES

Maintaining the scaling roadmap will require innovative solutions to the critical challenges of mobility, resistance, capacitance and (b) random variation [2]. First, note that strain has been a critical mobility enhancement in advancing the transistor scaling roadmap (Fig. 8). More exotic channel materials (Ge, III-V, etc. [3,4]) and different crystal orientations (110, 111) will need to compete with advancements in e-SiGe, e-SiC, contact-etch-stop layer, stress-memorization, stressed gate metal, and stressed contact metal techniques. Second, note that traditional resistive and capacitive elements (Figs. 9-10) will become more significant at the reduced dimensions of advanced technologies. Elements previously neglected (interface and epi resistance, contact-to-gate and epi-to-gate fringe capacitance) as well as new elements associated with the advanced transistor architectures will become critical. New doping techniques (molecular doping, plasma doping), new annealing techniques (sub-melt, superactivation, etc.) new architectures (metal S/D, etc.), and new materials (SiBCN, etc.) are promising innovations for resistance and capacitance challenges. Finally, in recent years, the importance of random variation has increased due to the importance of maintaining low random variation to achieve low minimum operating voltages (V_{ccmin}) for memory elements such as SRAMs and register file arrays (Fig. 11). New materials (such as HiK) and new architectures (such as UTB SOI) offer potential mitigation strategies for random variation challenges (See Fig. 12 [5]).

CMOS SYSTEM-ON-CHIP (SOC)

System-on-chip (SOC) processes are increasing in importance due to rapid expansion in mobile wireless products [6]. SOC processes have the challenging requirements of integrating digital CMOS with radio-frequency (RF) and analog components in a low-cost process. The continued advancements in CMOS devices also have benefit to SOC processes. For example, integration of RF transistors into a CMOS process has been challenging historically due to the degraded cut-off frequency (f_T) of Si CMOS as compared to III-V materials. However, in recent years, Moore's Law scaling has resulted in devices equivalent or better in f_T to III-V devices (Fig. 13 and 14). Similarly aggressive scaling of gate oxide (required for short-channel-control) has had significant benefit on both the flicker noise and thermal noise characteristics (see Fig. 15).

REFERENCES

[1] Natarajan, S., et al., *IEDM 2008*, pp. 941–943
[2] Kuhn, K., et al., *SSDM 2009*, and *IWJT 2010*, pp. 1-6
[3] Radosavljevic, M., et al., *IEDM 2010*, pp. 126-129.
[4] Pillarisetty, R., et al., *IEDM 2010*, pp. 150-153
[5] Kuhn, K., et al., *Trans. Elec. Dev.*, to be published 2011.
[6] Jan, C-H., et al., *IEDM 2010*, pp. 604-607.

QUESTIONS ON NEXT PAGE

a) Write down the equation that gives the limit on the Si body thickness T_{Si} in order to avoid the kink effect in thin body SOI? [4]

b) External resistance R_{ext}.

i) Prove that a large source resistance reduces the measured transconductance, g_m. [4]

ii) Give one reason why the carrier mobility in ultra-thin body MOSFETs (UTB) is lower than in an equivalent bulk MOSFET. [2]

c) MuGFETs on SOI.

i) Sketch the material cross section through the channel of a finFET perpendicular to the carrier flow. [3]

ii) Sketch the material cross section through the channel of a Trigate perpendicular to the carrier flow. [3]

iii) Give 1 advantage of a Trigate compared to a finFET. [2]

d) Independent gate operation.

i) What is meant by "independent gate operation"? Illustrate your answer with a sketch of the structure. [3]

ii) How can independent gate operation be used? Give one example and illustrate your example with an energy band diagram sketch. [4]