IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2016

EEE/EIE PART I: MEng, BEng and ACGI

Corrected copy

DIGITAL ELECTRONICS 1

Wednesday, 8 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 each carry 30%.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : Z. Durrani
Second Marker(s) : J.V. Pitt

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X[7:0] is an eight bit bus with X7 being the MSB and X0 the LSB.

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

Question 1

a) Simplify the following Boolean expressions using De Morgan's theorem and/or Boolean algebra.

(i) $\overline{A}\left(\overline{B+A\overline{C}}\right)$

[4]

(ii) $B+(C\oplus\overline{B})(AB+\overline{C})$

[4]

b) Simplify the following Boolean equation, in sum-of-products form, using a Karnaugh map.

$f = A\overline{B}+C(\overline{D}\oplus(A\oplus B))+A\overline{C}D$

[6]

c) Simplify the following Boolean equation, in product-of-sums form, using a Karnaugh map.

$f = \overline{A}\overline{B}\overline{C}+CD+ABC+\overline{A}BC$

[4]

d) Assuming that all numbers are 16 bits wide, complete the non-shaded, missing entries in the following table. (No marks will be awarded for this question unless you show how the solution is derived).

[8]

Decimal	Hexadecimal	Signed binary	Octal
-2049	?		
		?	3726
?	0FAB		
?		1100 0111 1001 1000	

e) Determine the number of bits needed to represent the range of results obtained when two *N*-bit signed numbers are multiplied together.

[4]

f) Figure 1.1 shows the Moore state diagram for a finite-state machine (FSM). Draw the state transition table corresponding to this diagram.

[4]

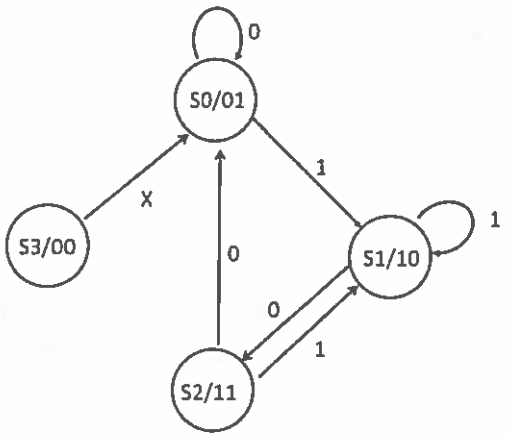
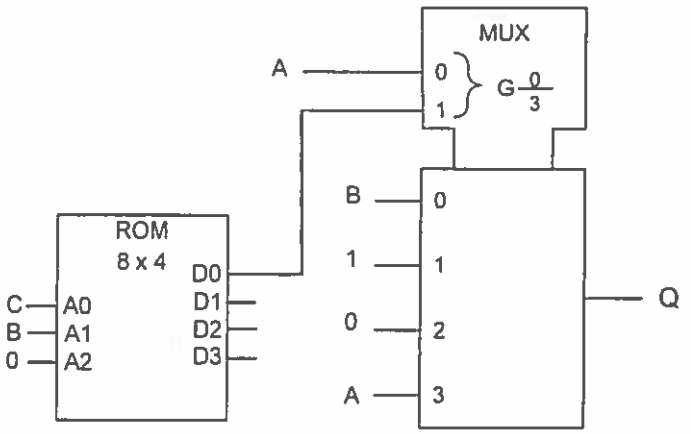


Figure 1.1

g) Write down the truth table for the functions D0 and Q in the circuit shown in Figure 1.2(a) below. The ROM contents are given in Figure 1.2(b) below.

[6]



(a)

Address	Data
0	0
1	3
2	A
3	D
4	1
5	0
6	C
7	F

(b)

Figure 1.2

Question 2

a) A duodecimal (base-12) input is to be encoded in binary, using active-low input and active-high output terminals.

(i) For this encoder, write down the truth table.

[6]

(ii) Hence, write the Boolean expressions for the output terminals. You do not need to draw the circuit.

[8]

b) (i) Figure 2.1 shows a J-K flip-flop with an asynchronous $\overline{CLEAR}$ terminal. By using flip-flops such as this, design an asynchronous binary counter, which counts the sequence:

0, 1, 2, ... A, 0, 1, 2, ... A, 0, 1,.... indefinitely

[6]

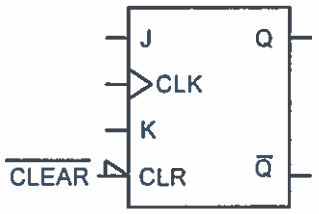


Figure 2.1

c) Consider the Boolean function:

$$f = \overline{A}\overline{B} + AB + \overline{A}C$$

(i) Implement this function using one 4 × 1 multiplexer, with the restriction for this design that the variable A cannot be connected to a multiplexer select line.

[4]

(ii) Implement f again, this time using two 2 × 1 multiplexers.

[6]

Question 3

A Moore finite state machine (FSM), with two inputs X1, X2, and one output Z, is shown in Figure 3.1. The FSM is initially reset to the state with Z = 0. The output of the FSM does not change unless one of the following sequences occurs at the input terminals:

(i) The input sequence X1X2 = 00, followed by X1X2 = 11, causing the output to become 0.
(ii) The input sequence X1X2 = 01, followed by X1X2 = 11, causing the output to become 1.
(iii) The input sequence X1X2 = 10, followed by X1X2 = 11, causing the output to toggle.

a) The FSM is to be implemented using 4 states (S0, S1, S2, S3). Draw the state diagram for this implementation.

[12]

b) A '1-hot' encoding system is to be used to encode the states, using 4 binary values (Q3 Q2 Q1 Q0) per state, as shown in the table below. Using this encoding system, derive the state transition table for the FSM.

State	Q3	Q2	Q1	Q0
S0	0	0	0	1
S1	0	0	1	0
S2	0	1	0	0
S3	1	0	0	0

[8]

c) Derive the Boolean equations for the FSM in sum-of-product form.

[10]

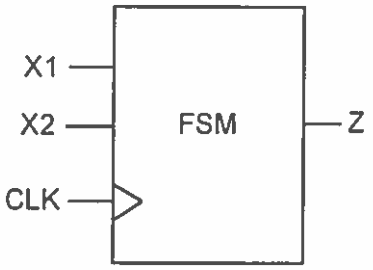


Figure 3.1

[THE END]