E3.01
AC1

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2009

MSc and EEE PART III/IV: MEng, BEng.and ACGI

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Wednesday, 13 May 10:00 am

Time allowed: 3:00 hours

Corrected Copy

c6

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : C. Toumazou
Second Marker(s) : E. Rodriguez-Villegas

1. (a) Voltage and current-sources are key components in analogue circuit design. Sketch a typical band-gap voltage reference circuit and prove that the temperature coefficient of the output voltage V_o is zero if $V_o = 1.283\ V$. Assume the temperature coefficient of V_{BE} to be $-2.5mV/°C$, Boltzmann's constant $k = 1.38 \times 10^{-23}\ J/K$ and electron charge $q = 1.6 \times 10^{-19}\ C$.

[11]

(b) Calculate the fractional temperature coefficient for the constant current generator of Figure 1.1 at room temperature, given that R is a polysilicon resistor with a temperature coefficient of 1500 ppm/°C.

[5]

(c) Explain qualitatively why the four-transistor voltage potential divider of Figure 1.2 can have smaller chip area than an equivalent two-transistor voltage potential divider with the same power consumption.

[4]

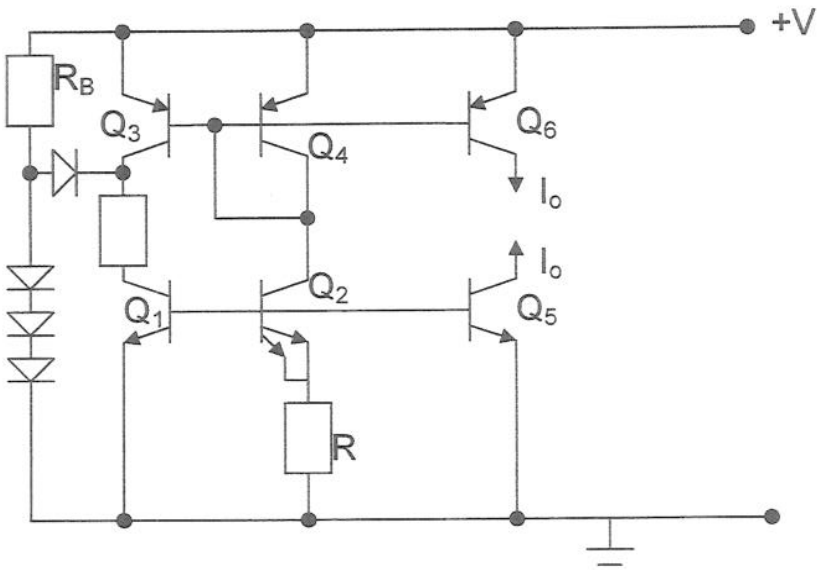

Figure 1.1

This question is continued on page 2.

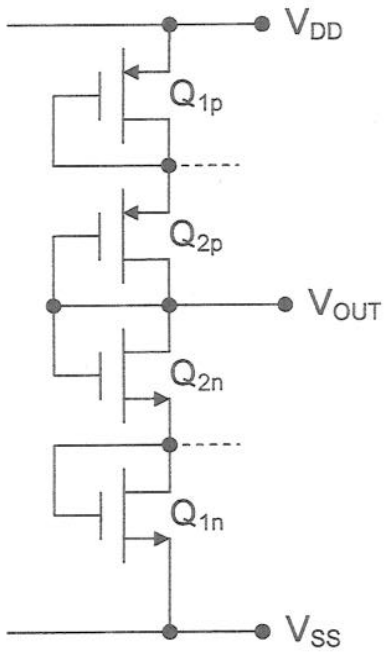

Figure 1.2

2.

(a) A fundamental limitation imposed on the Dynamic Range (DR) of any high performance A/D converter will ultimately be switch noise. Prove that the fundamental limit is given by,

$$DR = \frac{V_{ref}}{\sqrt{(10kTRf_c)}}$$

where V_{ref} is the reference voltage, k is the Boltzmann's constant, T is absolute temperature, R is switch resistance and f_c is the clock frequency of the switch. You may assume that the system settles in 10τ (where τ is the time constant), over one period of the clock frequency.

[8]

(b) A very high resolution analogue-to-digital converter is the oversampling converter sometimes referred to as the sigma-delta modulator. Sketch a typical architecture for such a converter and explain its principles of operation, in particular the feedback noise shaping mechanism.

[12]

3. (a) Sketch typical circuit diagrams for a two-stage cascoded and a single-stage CMOS op-amp. Explain why the single-stage design has potentially much higher bandwidth than the two-stage design and in particular why it is not necessary to Miller compensate the single-stage architecture. Give one advantage and one disadvantage of the cascoded op-amp.

[8]

(b) Estimate the low-frequency differential voltage gain, and, gain-bandwidth product of the two-stage CMOS op-amp shown in Figure 3.1. Aspect ratios of all devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below.

[10]

(c) Explain qualitatively why the addition of a load capacitor to the output of a two-stage op-amp degrades amplifier stability, whereas an additional load capacitor connected to the output of a single-stage op-amp improves amplifier stability.

[2]

CMOS TRANSISTOR PARAMETERS

MODEL PARAMETERS	*Kp (μA/V2)*	$\lambda(V^{-1})$	$V_{T0}(V)$
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

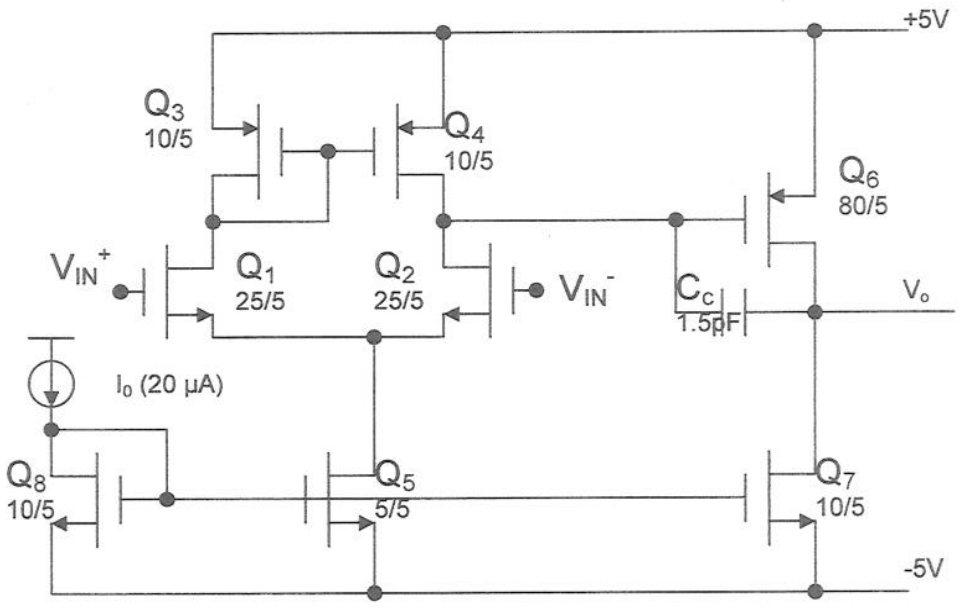

Figure 3.1

4. (a) Give one advantage and one disadvantage of each of the two CMOS current mirror circuits shown in Figures 4.1 and 4.2

[6]

(b) For the current mirror of Figure 4.2 derive this voltage swing in terms of device threshold voltage V_T, clearly stating any assumptions you make.

[7]

(c) With the aid of a macromodel, explain the theoretical concept of current feedback and how it results in constant bandwidth application.

[7]

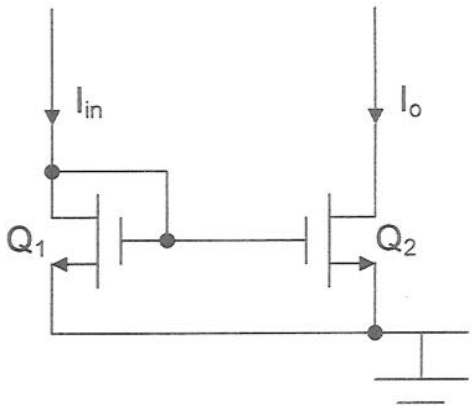

Figure 4.1

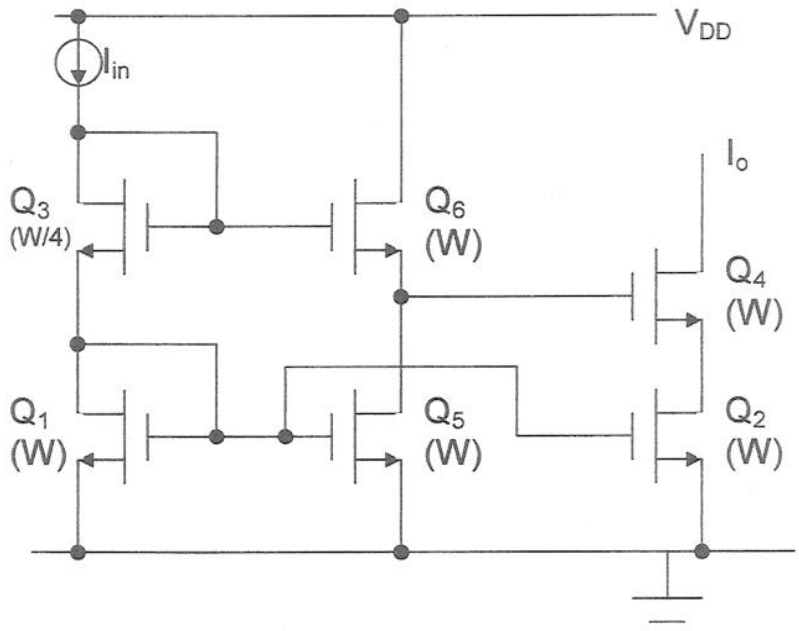

Figure 4.2

5. (a) Sketch the circuit for a differential switched-capacitor integrator and derive an expression for its transfer function.

[10]

(b) Figure 5.1 shows one section of a switched capacitor ladder filter. Based on this filter structure, design a 3rd-order Chebyshev low-pass filter with a cut-off frequency of 5 kHz and a 1.0 dB pass band ripple. Assume a clock frequency of 100 kHz. Passive component values for the LC prototype, normalised to 1 rad/s, are $C_1 = C_3 = 2.0236$, $L_2 = 0.994$. In your analysis assume all integrators to be lossless.

[10]

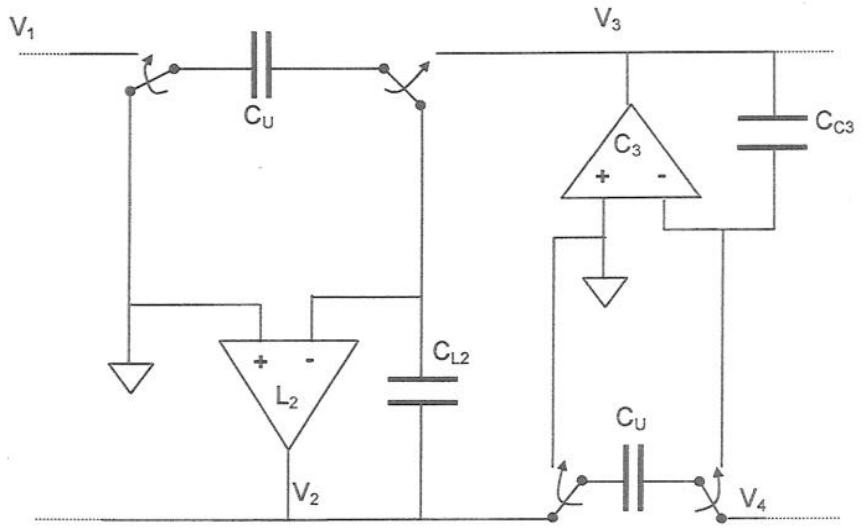

Figure 5.1

6. (a) Under what operating conditions does the MOSFET of Figure 6(a) realise a linear floating resistor between terminals *A* and *B*? Show that under these conditions the equivalent resistance R_{AB} can be approximated by

$$R_{AB} = \frac{L}{KW(V_{GS} - V_T)}$$

stating any assumptions. All symbols have their usual meaning.

[5]

(b) Discuss three sources of non-linearity in the single MOSFET resistor realisation of Figure 4(a) and suggest one suitable circuit design to help eliminate one or more of these non-linear terms showing the necessary circuit analysis to confirm your design.

[5]

(c) For the current mirror of Figure 6(b), derive the expression for minimum output voltage while still maintaining saturated devices. Derive this voltage in terms of device threshold voltage V_T clearly stating any assumptions you make.

[4]

(d) Sketch a regulated cascode current-source and explain why the output resistance of the current source is higher than that of a standard cascode mirror.

[6]

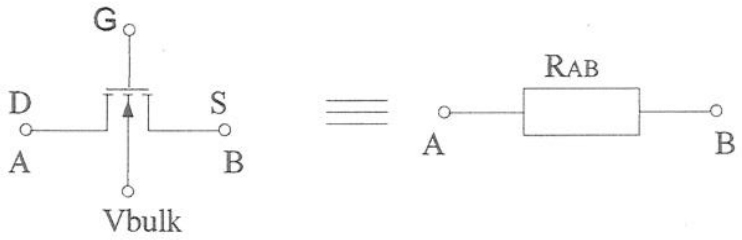

Figure 6(a)

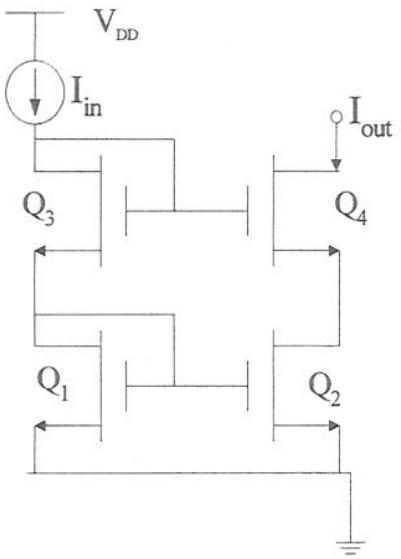

Figure 6(b)

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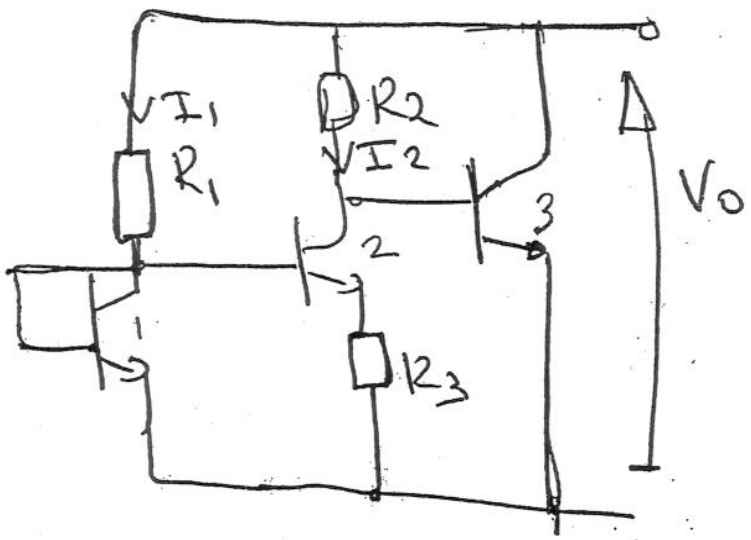
SOLUTIONS

1st Marker C. Toumazou

2nd Marker E. Rodriguez

Question 1

Q1



Bandgap.

1/18

5/5

$V_{BE1} = V_{BE2} + I_2 R_3$

$\beta >> 1$

Since $V_{BE1} - V_{BE2} = V_T \ln(I_1/I_2)$

Then $V_o = V_{BE3} + R_2/R_3 V_T \ln(I_1/I_2)$

$V_T \ln(I_3/I_s)$ → assume Non-temp

for $dV_o/dt = 0$, then dV_{BE3}/dT

$$= \frac{V_T}{T} \frac{R_2}{R_3} \ln\left(\frac{I_1}{I_2}\right)$$

Since $\frac{dV_{BE}}{dt} \approx -2.5 mV/°C$, $\frac{V_T}{T} = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}}$

Then $\left(\frac{R_2}{R_3}\right) \ln\left(\frac{I_1}{I_2}\right) = 29$ and so

6/6

$V_o = 1.283 V$

//

For PTAT temperature coefficient of V_T cancels with negative temp coefficient of Resistor

5/5

$\therefore TCF = \frac{1}{V_T} \partial V_T/\partial T - 1/R \, \partial R/\partial T$

$= 1/T - 1500 \times 10^{-6}$ @ RoomT $= 1833$ ppm/°C

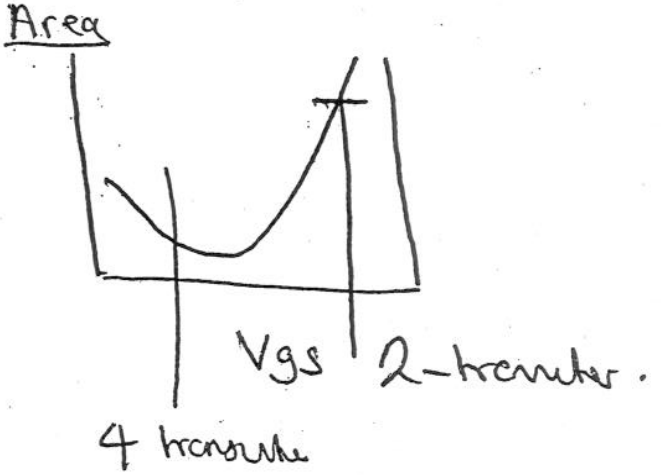
Figure 1(b).

Since $I = \frac{KW}{2L}(V_{GS} - V_T)^2$

then if V_{GS} is small $\approx V_T$
then (W/L) large.

If $V_{GS} >> V_T$
then (W/L) small
Small (W/L) gives large Chip area

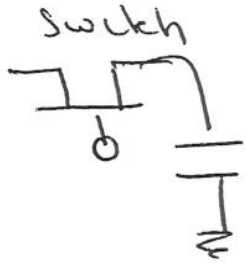
2©
∴ Two transistor P.D
has larger V_{GS} / transistor
than four transistor P.D has same
supply.



4/4

Q2 / Constraints

a) Dynamic Range $\triangleq V_{ref}/Noise = 2^N$



RMS noise of switch driving capacitor

$$= \sqrt{\frac{kT}{C}}$$

$$\therefore DR = \frac{V_{ref}}{\sqrt{\frac{kT}{C}}} = 2^N$$

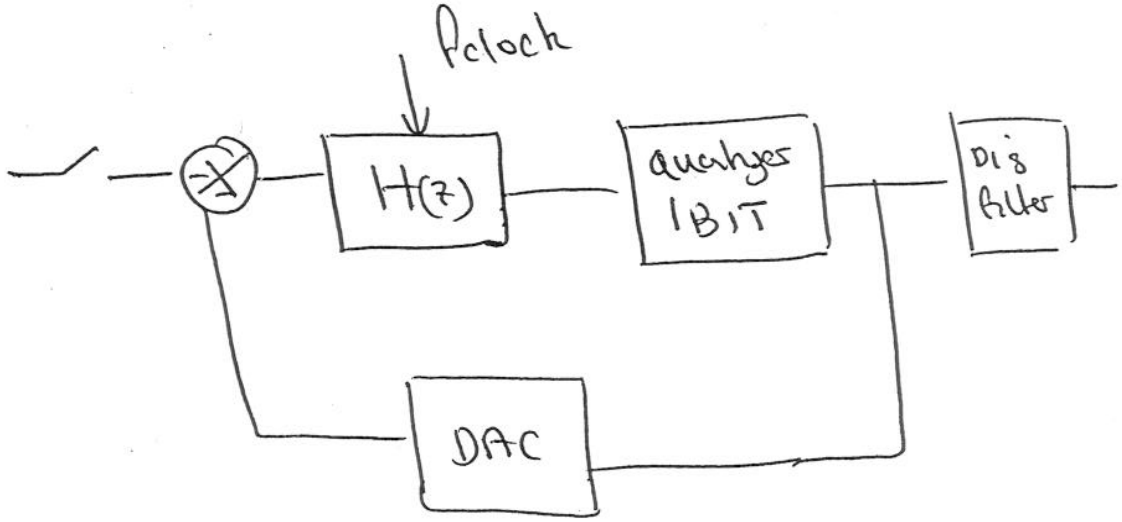
Assume $f_c = 1/(10RC)$

then solving for C gives

$$DR = 2^N = V_{ref}/\sqrt{kT10RC}$$

8/8

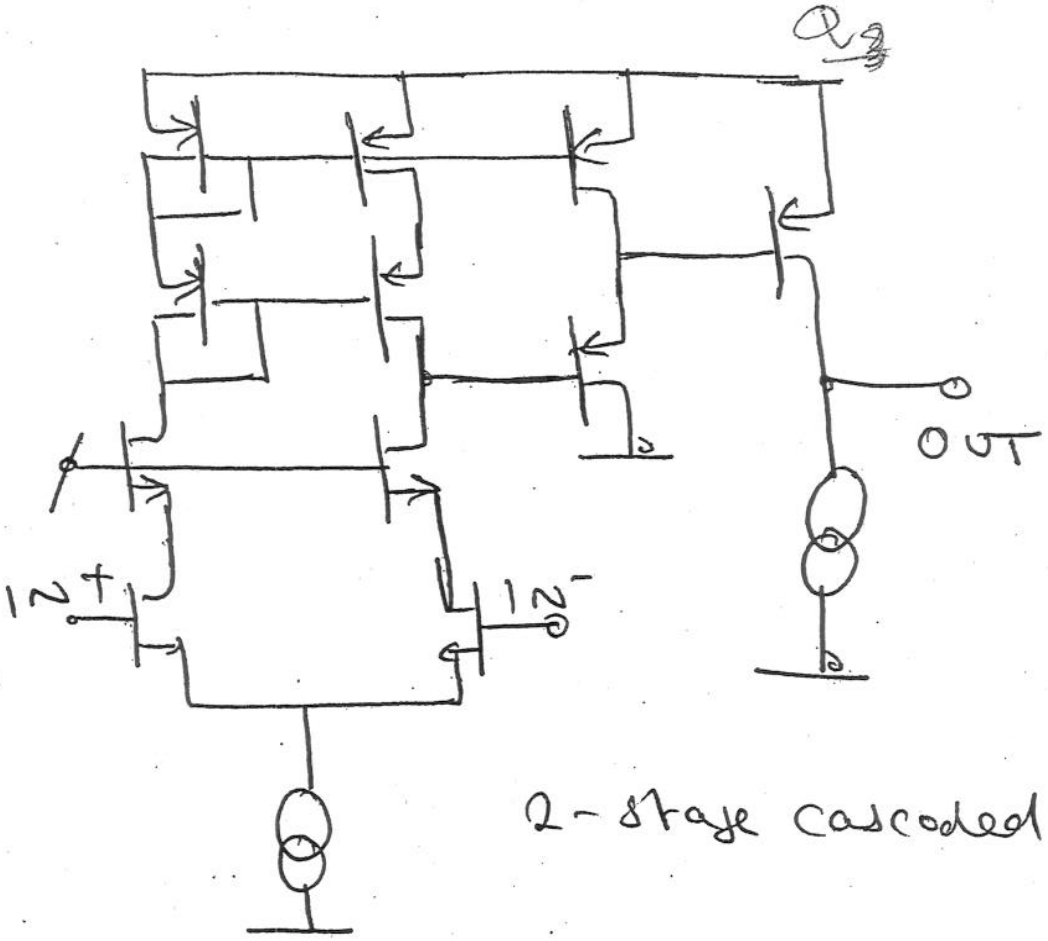
b)



Basic idea is that coarse quantization noise gets shaped by $1/(Hz)$ via feedback

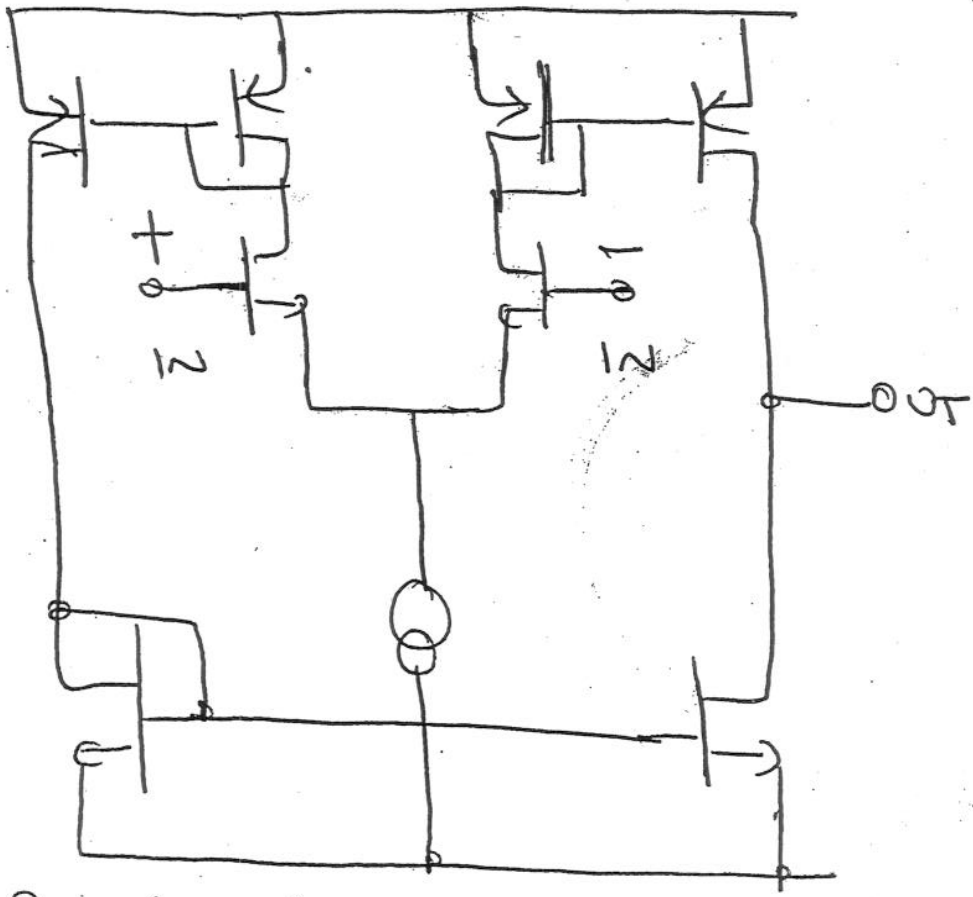
Generally H(z) is an integrator so noise is shaped differentially. This reduces requirements upon component accuracy. The architecture includes a negative feedback loop around the coarse estimate that oscillates about the true value of input, the digital filter averages this coarse estimate to produce a finer approximation. The feedback DAC and forward integrator force the quantization error to have a high frequency spectrum. The output of the digital filter is downsampled and given a multibit digital representation. High frequency quantization noise is reduced. Noise shaped giving very high (S/N) at low frequency.

Q3.



2-stage cascoded.

3/3



3/3

Single-stage.

Q3 (cont)

In a single-stage the main high impedance node is at the output. Compensation is then provided via a load capacitance at the output. The internal poles at the lower impedance nodes are now secondary and so will only affect the phase margin of the amplifier.

In a two-stage design, the requirement for a single high internal impedance to achieve voltage gain means that the amplifier requires internal frequency (Miller) compensation to be stable. Because of this compensation the bandwidth is reduced.

(2/2) The main advantage of a cascoded op-amp is voltage gain, the main disadvantage is CMVR or signal swing limitations.

Op-Amp

(3/3) $A_{V1} = -g_{m2}/(g_{O2}+g_{O4})$

$(g_{O2}+g_{O4}) = I_{D2}(\lambda_n + \lambda_p) =$

$5\times10^{-6}\times0.05 = 2.5\times10^{-7}\ \Omega^{-1}$

(2/2) $g_{m2} = 2\sqrt{\beta_2 I_D} \Rightarrow \beta_2 = \frac{k_n'}{2}\left(\frac{W}{L}\right)_2 = 7.5\times10^{-5}\ A/V$

$g_{m2} = 3.87\times10^{-5}\ S$, $A_1 = -154.9$

$A_2 = -g_{m6}/(g_{O7}+g_{O6})$

Q3- Cont.

$(g_{06} \| g_{07}) = I_{D6}(\lambda_{Np} + \lambda_N) = 20 \times 10^{-6} \times 0.05$

$= 10 \times 10^{-7} \Omega^{-1}$

(3½) $g_{m6} = 2\sqrt{\beta_6 I_{D6}} \Rightarrow \beta_6 = \frac{k_p}{2}\left(\frac{W}{L}\right)_6 = 1.6 \times 10^{-4} A/V^2$

$g_{m6} = 1.13 \times 10^{-4}$, $A_2 = 113$

$A_{TOTAL} = A_1 A_2 = 17503$

(2½) $G.B_p = g_{m2}/2\pi C_c = 4.1\ MHz$

- In 2-stage load is 2nd Pole here reducing load increases stability. With single stage load forms dominat Pole here reducing load increases bandwidth (2½)

Question 4

Qu4/.

a)

Fig 4.1 – Simple mirror

Advantages – High frequency
– High output swing

(2) Disadvantage – very inaccurate

Fig 4.2 – High swing Cascode

Advantage – Higher output swing than cascode

(2) Disadvantage – Complex, poor frequency performance.

Figure 4.3 – Regulated Cascode

Advantage – Highest output swing
Highest output resistance

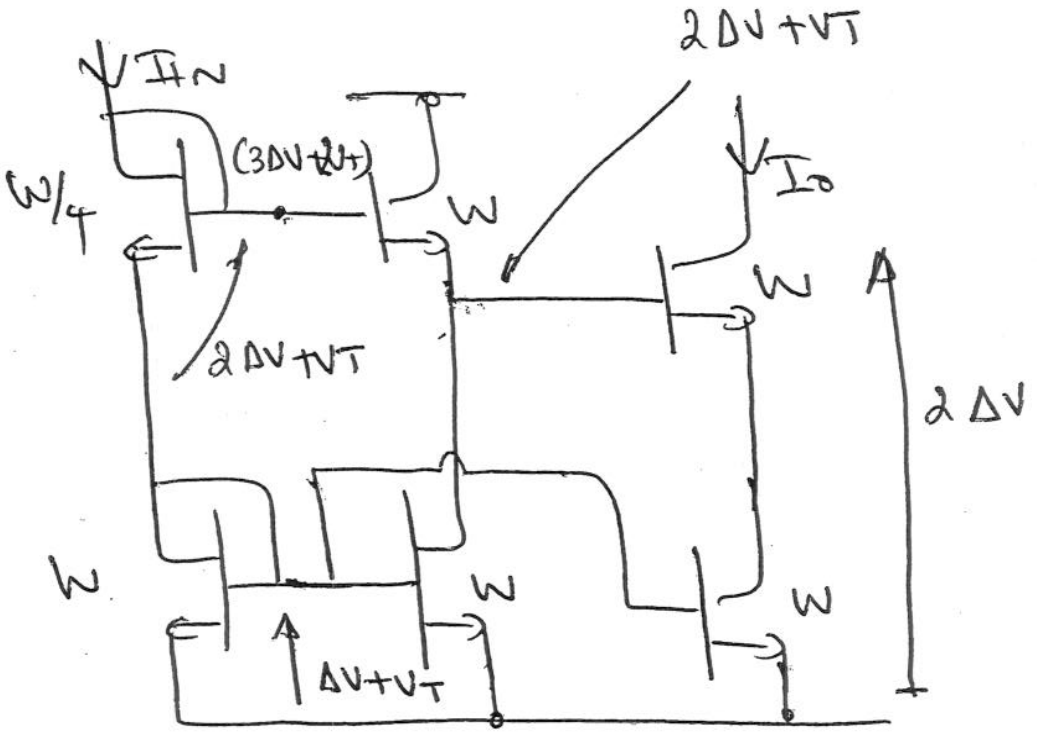
(2) Disadvantage – inaccuracy of simple current-mirror
– feedback leading to potential instability.

6/6

Qu 4- Cont.

output Swing

Cuscut includes all saturation Voltages



Assuming equal L's

$$I_O = I_{IN}$$

$$\beta_1 = \beta_2 = \beta_4 \quad \beta_5 = \beta_6 = \beta$$

$$\beta_3 = \beta/4$$

7/7

$$\therefore V_{sat(3)} = 2(V_{GS} - V_T)$$

NOTE $\Delta V = (V_{GS} - V_T)$

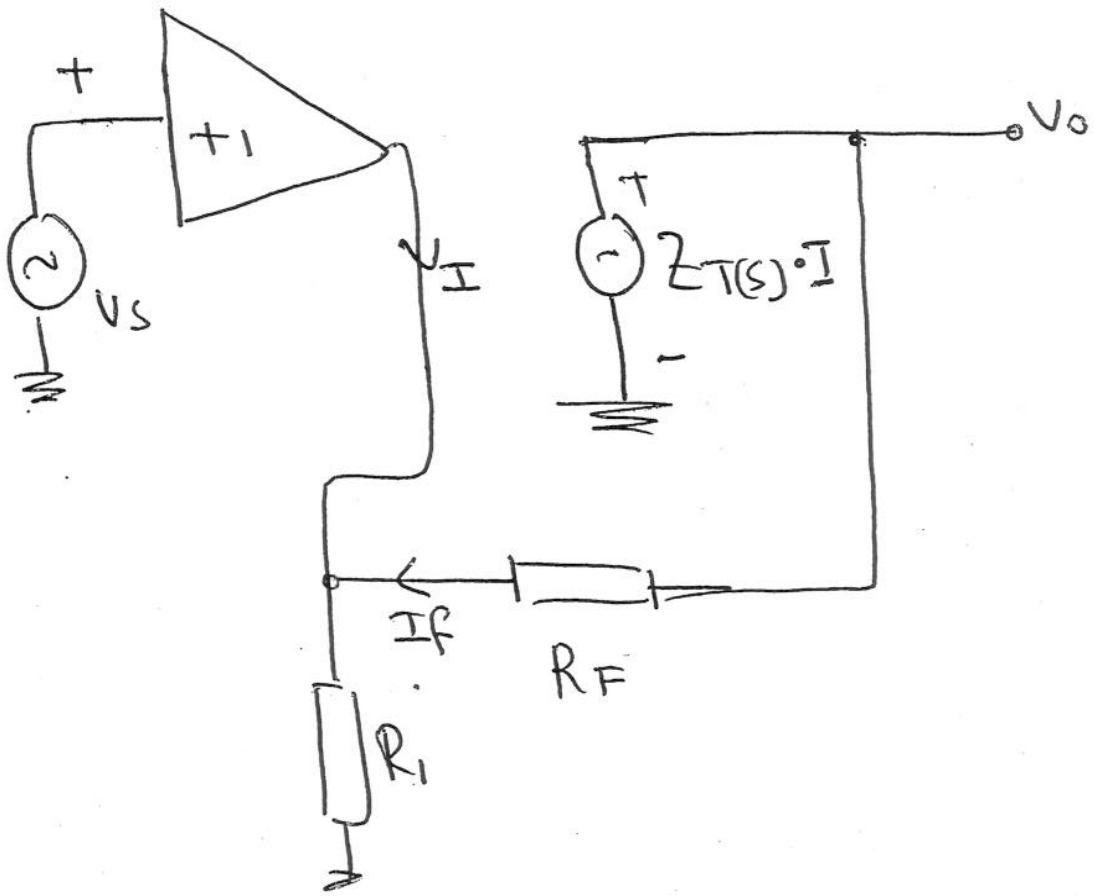
Swing $\underline{\underline{2\Delta V}}$.

CT p.9

Qu 4 cont

Macromodel of Current-feedback op-amp.

c).



$Z_{T(S)} = Z_{TO}/(1+jf/f_p) \Rightarrow f_p$ dominant Pole

From model

$$I_f = (V_O - V_S)/R_F$$

$$I_1 = V_S/R_1$$

$$V_O = Z_{T(S)} I = Z_{(T)}(I_1 - I_f)$$

From above

$$(V_O/V_S) = (1 + R_F/R_1)\left[\frac{Z_{T(S)}}{R_F + Z_{T(S)}}\right]$$

Qu 4 cont.

substitute $Z(T)$s, and assume $Z_{TO} \gg R_F$

$$\left(V_O/V_S\right)_{j\omega} = \left(1 + \frac{R_F}{R_1}\right)\left[\frac{Z_{TO}}{Z_{TO}+R_F}\right]\left(\frac{1}{\left(1+jf/f_p\left(\frac{Z_{TO}+R_F}{R_F}\right)\right)}\right)$$

Assuming $Z_{TO} \gg R_F$

$$\left(\frac{V_O}{V_S}\right)_{j\omega} = \left(1+\frac{R_F}{R_1}\right)\frac{1}{\left(1 + jf/\frac{GB}{R_F}\right)}$$

where $G.B = f_p Z_{TO}$

f_p closed $= \underline{G.B/R_F} \Rightarrow$ determined by R_F

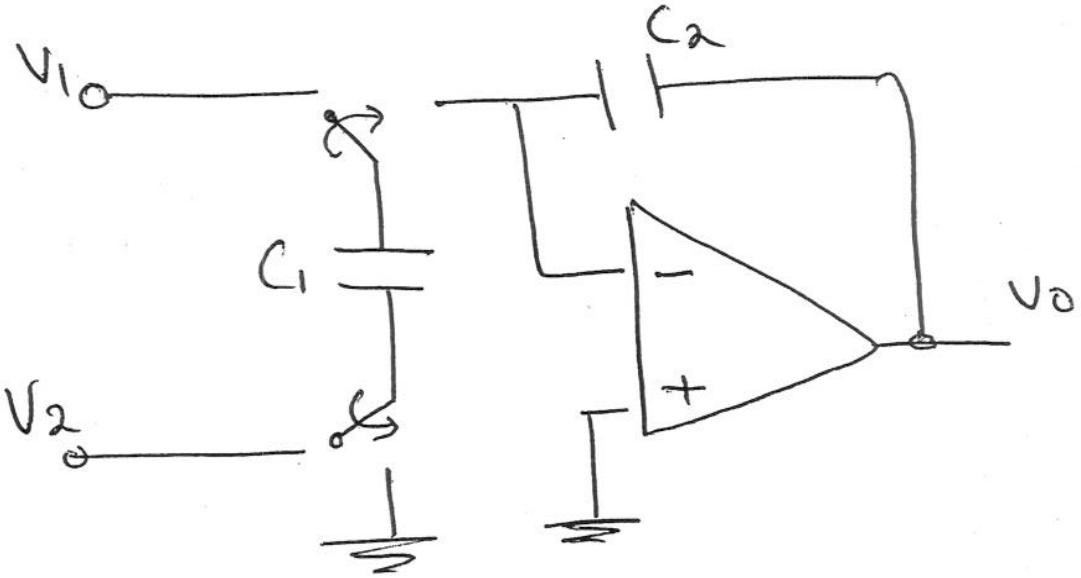
Gain determined by R_1

$$A_C = \left(1 + \frac{R_F}{R_1}\right)$$

7/7

Qu5/.

a) Differential integrator



During ϕ_1 $\quad Q = C_1[V_1 - V_2]$

$$I_{av} = f_c C_1 [V_1 - V_2]$$

f_c = clock frequency

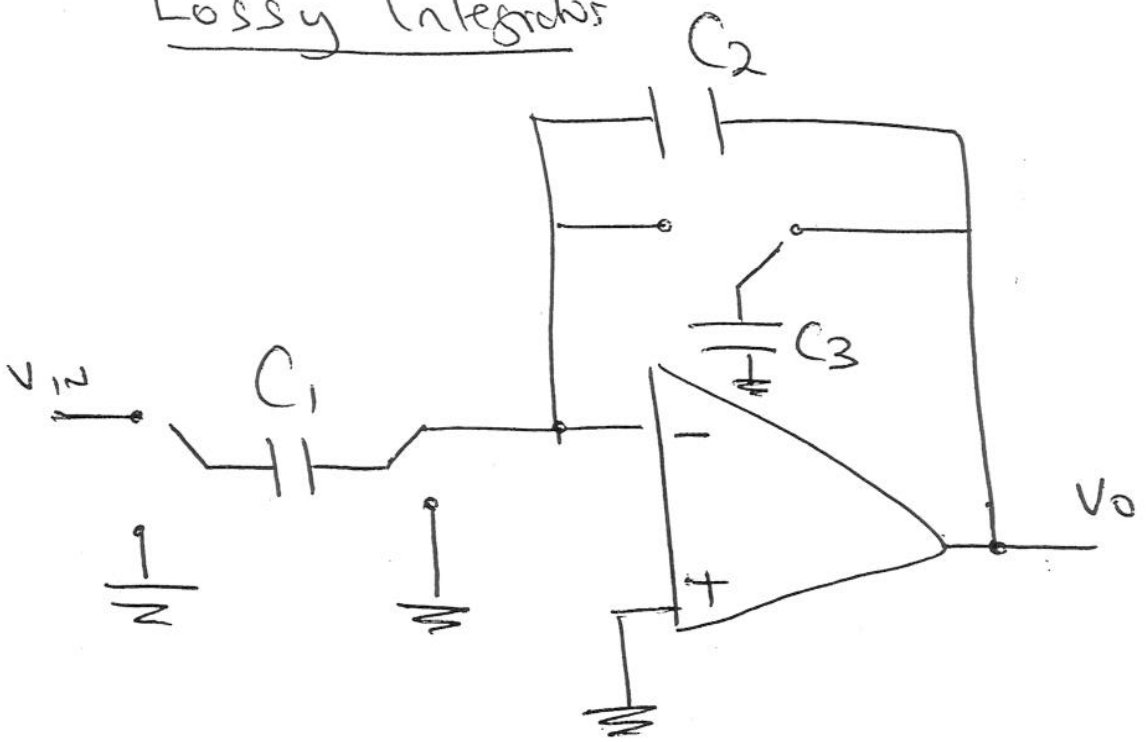
During $\phi_2 \Rightarrow \quad I_{av} = -f_c (V_1 - V_2) C_1$

$$\therefore V_0 = \frac{-1}{j\omega C_2} f_c C_1 [V_1 - V_2]$$

$$\therefore \frac{V_0}{(V_1 - V_2)} = -\frac{f_c}{j\omega} \frac{C_1}{C_2} \approx \tau = \frac{C_2}{C_1 f_c}$$

5/5

Lossy Integrator



During ϕ_1 $\quad Q = C_1 V_{IN} \Rightarrow I_{AV} = f_c C_1 V_{IN}$

During ϕ_2

$$I_{AV} = -\left[f_c (C_3 V_O + j\omega C_2 V_O\right]$$

$$\therefore f_c C_1 V_{IN} = -\left[f_c (C_3 V_O + j\omega C_2 V_O\right]$$

$$V_{IN} = -\left[\frac{C_3}{C_1} V_O + \frac{j\omega C_2 V_O}{C_1 f_c}\right]$$

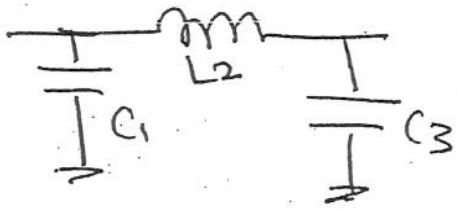
$$\therefore \frac{V_O}{V_{IN}} = -\frac{C_1}{C_3}\left(\frac{1}{\left(1 + \frac{C_2}{C_3} j\omega/f_c\right.}\right)$$

5/5

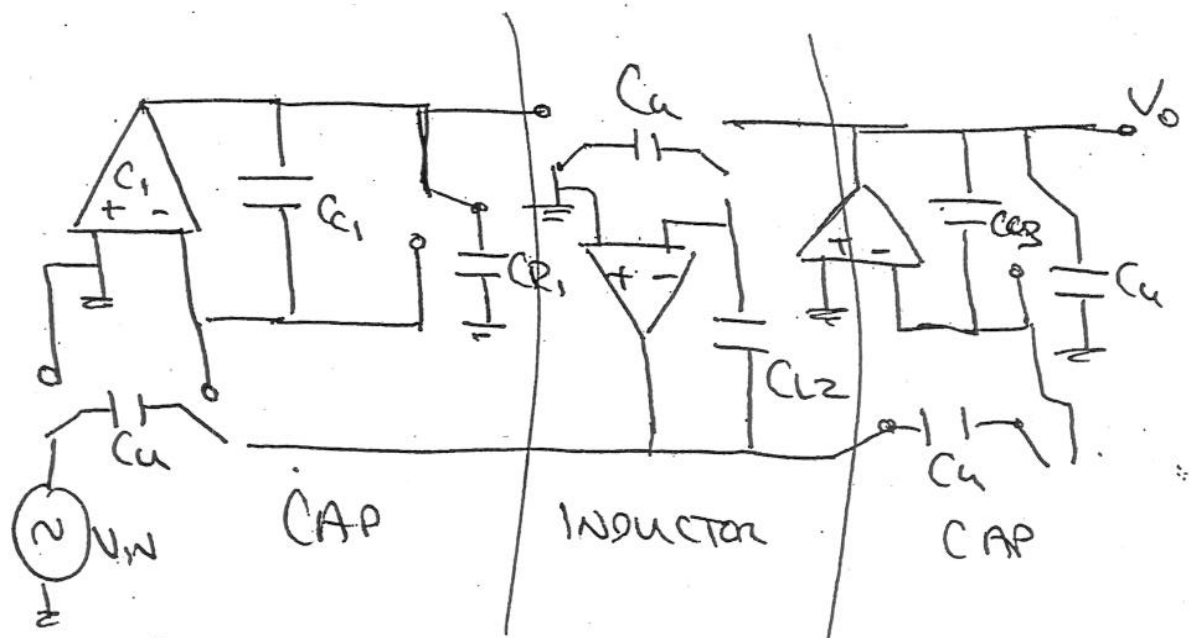
$\Rightarrow \tau = \left(C_2/C_3\right)\frac{1}{f_c}$

Qu 5 Cont

Section of LCR prototype.



General transformation Rules (not really required but bar bright students may include)



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Conversion into differential integrates.

Inductor transformation

$$(L_2/R_S)f_c = C_{L2}/C_4$$

Capacitor Transformation.

$$C_3/C_4 = f_c R_S C_3$$

where R_S is normalising during scaling transform. Assuming $R_S = 1$

$$\left.\begin{aligned} C_1/C_4 &= f_c C_1 \\ C_{C3}/C_4 &= f_c C_3 \\ C_{L2}/C_4 &= f_c L_2 \end{aligned}\right\} \text{ general transformation}$$

CT

Qu 5 cont

Table values of C_1, L_2 and C_3 are normalized to 1 rad/s $\div 2\pi f_p$

$f_p = 5\text{kHz}$

$$C_L = C_3 = 2.0236 / (2\pi \, 5\times10^3) = 6.44\times10^{-5}\text{F}$$

$$C_{L2} = 0.994 / (2\pi \, 5\times10^3) = 3.164\times10^{-5}\text{F}$$

For termination R_s

assume $C_{in} = C_{R_i} = C_{R_o} = 1\text{pF}$

Then $\left[\begin{array}{l} C_{L_1} = C_{L_3} = 6.44\text{pF} \\ C_{L2} = 3.164\text{pF} \end{array} \right]$

6/6

TOTAL 20/20

CT

Question 6.

Q6 (Q6)

Assumption is that if ($V_{DS} \approx 0$) or ($V_{DS} << V_{GS} - V_T$) device acts in Linear region. From

$$I_D = \frac{kW}{L}\left[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2\right][1 + \lambda V_{DS}]$$

for $V_{DS} << (V_{GS} - V_T)$, then $\lambda V_{DS} << 1$

so $$I_D = \frac{kW}{L}(V_{GS} - V_T)V_{DS}$$

OR $$R_{AB} = V_{DS}/I_D = L/(kW(V_{GS} - V_T)$$ 5

Three sources of Non-linearity

(i) Limited due to V_{BS} changing V_T for negative V_{BS} due to body-effect.

ie $$V_T = V_{TO} + \gamma\left[\sqrt{-V_{BS} + 2\phi_F} - \sqrt{2\phi_F}\right]$$

γ = bulk threshold parameter

ϕ_F = Fermi-level potential

(ii) Limited due to V_{DS} approaching $(V_{GS} - V_T)$ hence saturation region for large positive V_{DS}.

(iii) For large values of V_{DS} the $V_{DS}^2/2$ term introduces large Non-linearity. 3

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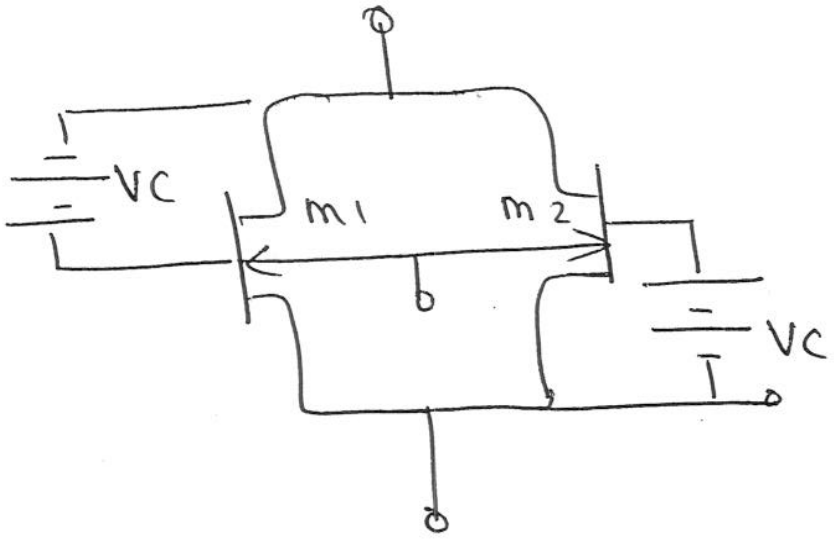
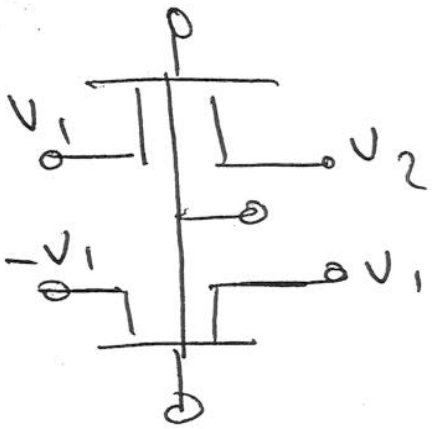
a

(cont

Q6 cont.

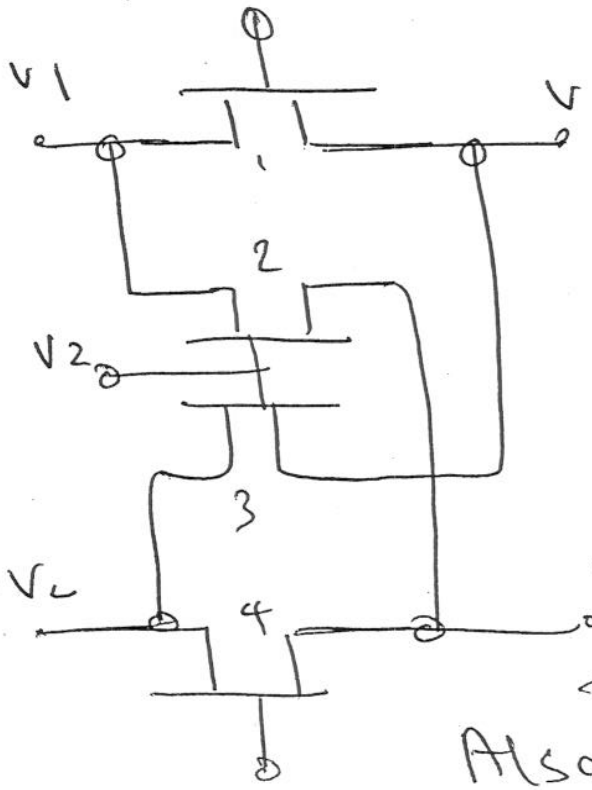


Parallel circuit - eliminates $V_{DS}^2/2$ term.



Differential scheme

Effects of V_{DS} cancelled.



Double differential MOS

Eliminates

$-V_{DS}$ and V_T term

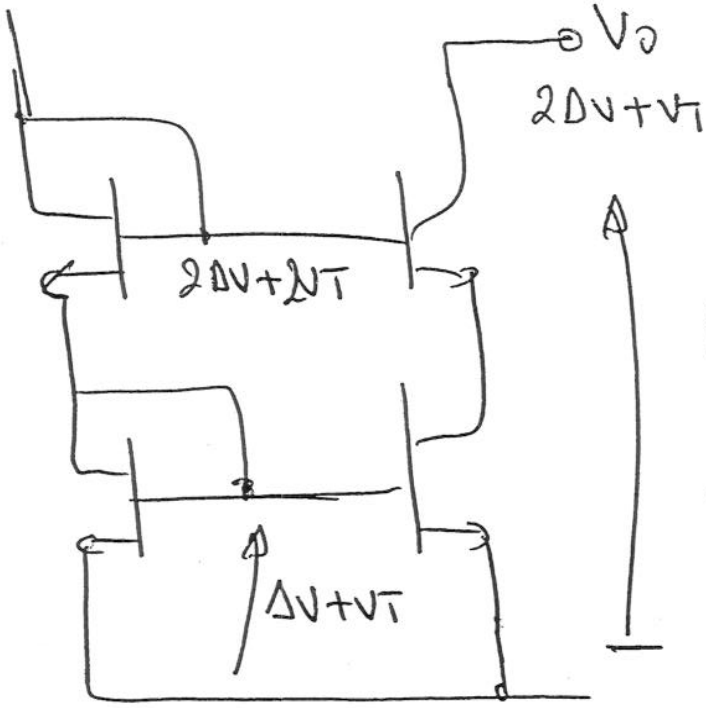
2

Any one will do

Also expect analysis of particular cell.

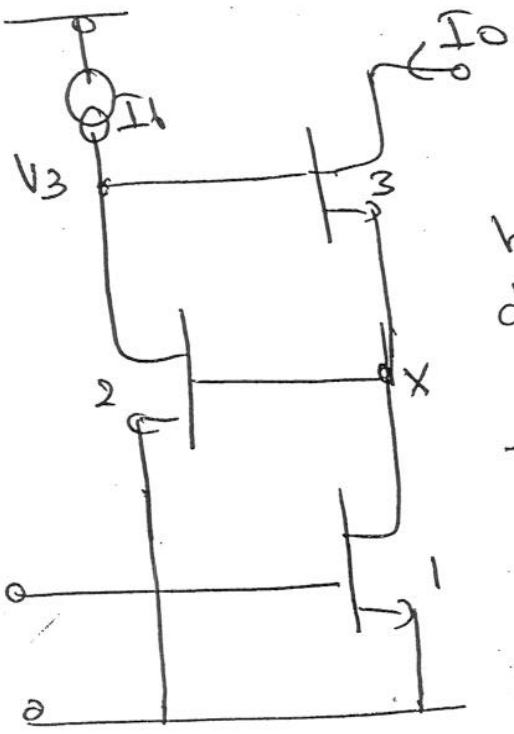
p17.
CT

Q6 cont.



Assume
$\Delta V = V_{GS} - V_T$
for sat
$V_{DS} \geq V_{GS} - V_T$

$$(V_o)_{min} = 2(\Delta V + V_T) - V_T \quad 6$$
$$= 2\Delta V + V_T$$



Q_3 cascodes Q_1 hence output resistance due to Q_3 is
$R_{o3} \approx r_{ds1} g_{m3} r_{ds3}$

Transistor Q_2 senses change in voltage at node (X) and reduces these changes by the loop gain of the amplifier (Q_2 and I_b) hence this further increases the output resistance of the circuit to
$R_{out} = R_{o3} g_{m2} r_{d2} g_{m3} r_{ds3} r_{ds1} \approx (g_m^2/g_o^3)$ 6
Assuming equal g_m and g_{o1}.