

Paper Number(s): **E3.01**
AC1

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2001

MSc and EEE PART III/IV: M.Eng., B.Eng. and ACGI

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Tuesday, 1 May 10:00 am

There are SIX questions on this paper.

Answer FOUR questions.

Time allowed: 3:00 hours

Corrected
L6

Q3, Q4.

Examiners: Toumazou, C. and Papavassiliou, C.

Special instructions for invigilators:

None

Information for candidates:

None

1. *Figure 1* shows two bipolar integrated circuits.

For the bandgap voltage reference circuit of *Figure 1(a)*, show that $dV_o/dT = 0$ (where T is temperature) if $I_1 = I_2 \exp [29 R_3/R_2]$, and for this condition $V_o = 1.283$ V.

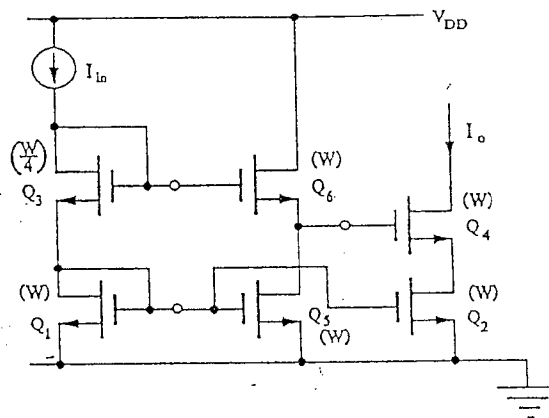
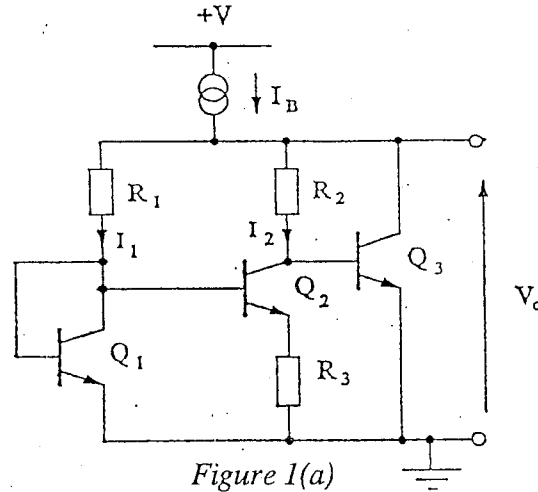
Assume the temperature coefficient of V_{BE} to be -2.5 mV/ $^{\circ}$ C, the collector current of transistor Q_3 is 100 μ A and the device saturation current $I_s = 1.2 \times 10^{-13}$ A.

Boltzmanns Constant $k = 1.38 \times 10^{-23}$ J/K and electron charge $q = 1.6 \times 10^{-19}$ C. [10]

For the circuit of *Figure 1(a)*, design a suitable current source I_B of value 300 μ A, which is virtually independent of power supply voltage and directly proportional to absolute temperature. Sketch the circuit and ignore any automatic start-up circuitry. [7]

Figure 1(b) shows a high swing low voltage cascode current-mirror. Estimate the minimum output voltage swing $V(\min)$ which ensures that all devices remain in saturation. Given the following data, calculate $V(\min)$: $I_o = 100$ μ A, $K = 40$ μ A/ V^2 , and $(W/L) = 1$ for all [8] devices.

What is the new value of $V(\min)$ if (W/L) is increased to 10?



2. Briefly explain the operation of each of the biasing circuits in *Figure 2*. [10]

For the circuits of *Figure 2(a)* and *Figure 2(b)* calculate a value for resistor R to yield an output current I_0 of $10\ \mu\text{A}$ and use this example to show that the circuit of *Figure 2(b)* has a lower fractional temperature coefficient. You may assume that the circuits are operating at room temperature. The forward saturation current of the transistor $I_s = 10^{-14}\ \text{A}$, the temperature coefficient of $V_{BE} = -2\ \text{mV}/^\circ\text{C}$ and R is a polysilicon resistor with a temperature coefficient of $1500\ \text{ppm}/^\circ\text{C}$. [6]

It is likely that on power-up the output currents of *Figure 2(a)* and *Figure 2(b)* will fall into a zero current state. Sketch a suitable start-up circuit for one of these two circuits to ensure this condition will not occur. [3]

Finally, using reasonable engineering approximations, give an expression for the output resistance of the circuit of *Figure 2(c)*. You only need consider transistors Q_1 , Q_2 , Q_3 and Q_7 since the remaining transistors are purely for biasing purposes. [6]

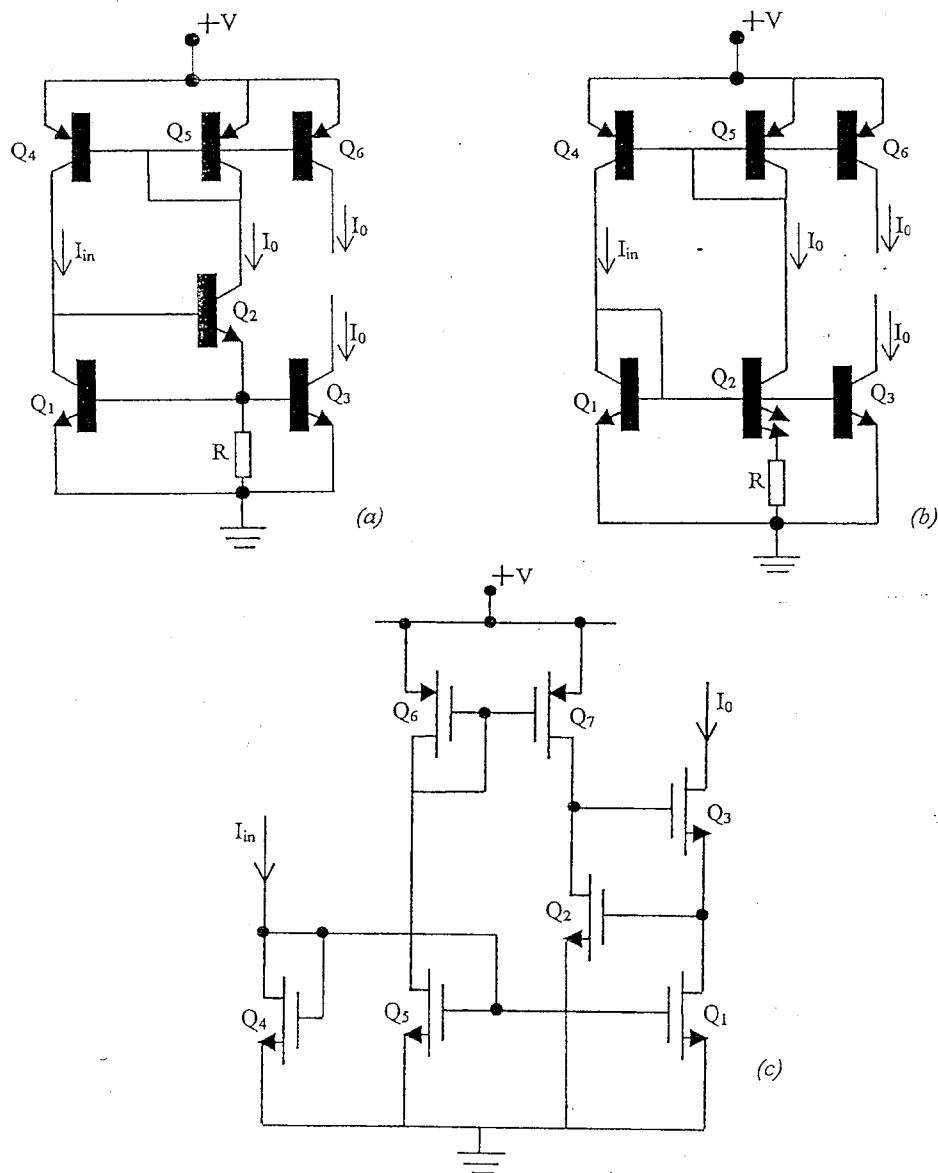


Figure 2

3. Figure 3 shows a partially-designed two-stage CMOS op-amp required to give a voltage gain of approximately 80 dB, a slew-rate of 5 V/ μ s and a gain-bandwidth product of 3 MHz. Given that the technology is a fixed 5 μ m length double metal CMOS process, design the channel widths of transistors Q1, Q2 and Q6 for the op-amp to meet the above performance specifications. Aspect ratios of all other devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below. [16]

After simulation you find that the phase margin of your op-amp is below specification. *Qualitatively*, discuss a sequence of parameter changes that would lead to improvement in phase margin; you are willing to sacrifice amplifier gain-bandwidth product. [5]

Finally, give a reason why the introduction of a single integrated resistor in series with the compensation capacitor should significantly improve the amplifier's phase margin. [4]

CMOS TRANSISTOR MODEL PARAMETERS

MODEL PARAMETERS	K_P (μ A/V ²)	λ (V ⁻¹)	V_{T0} (V)
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

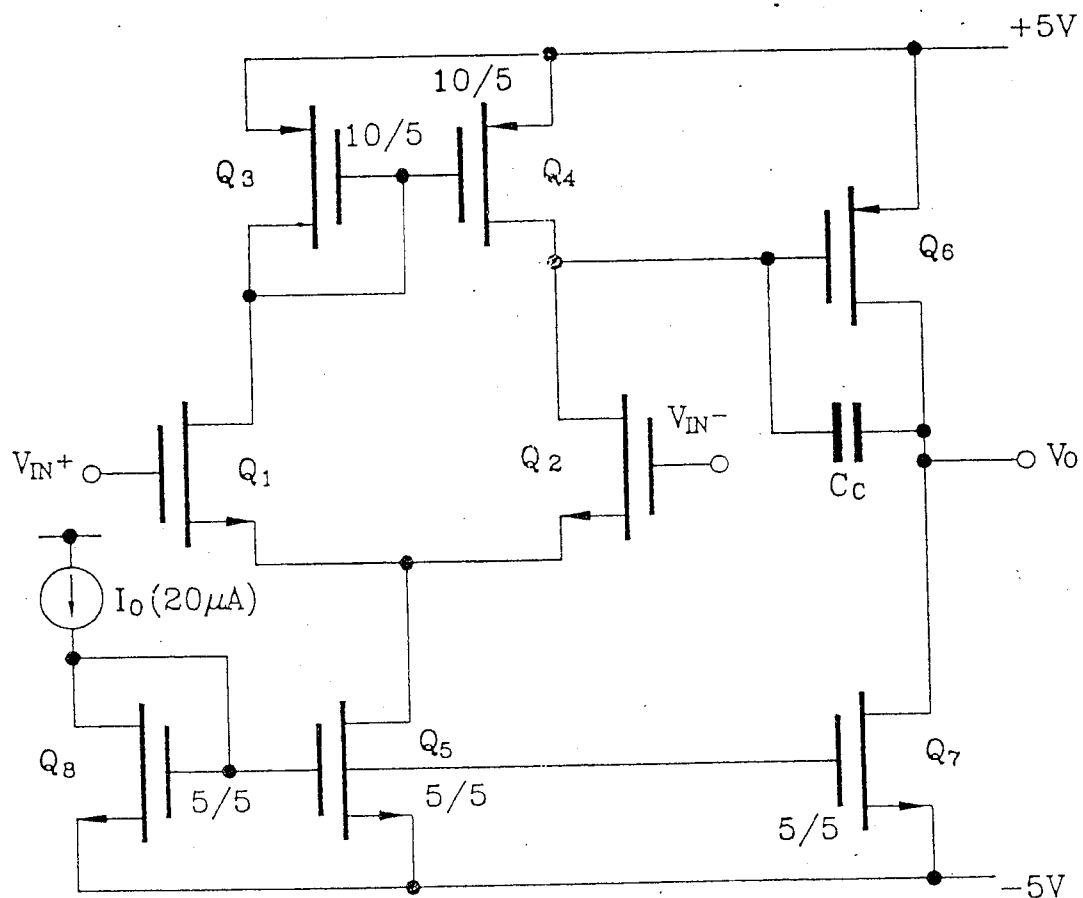


Figure 3

4. Using two switches and a capacitor, sketch a circuit that will synthesise an active resistor. Given that the switches are driven by a pair of non-overlapping clocks running at a frequency of 100 kHz, estimate the value of a capacitor to give a resistance of 10 MΩ. [8]

A fundamental limitation imposed on the Dynamic Range (DR) of any high performance A/D converter will ultimately be switch noise. Prove that the fundamental limit is given by,

$$DR = \frac{V_{ref}}{\sqrt{(10kTRf_c)}} \quad [7] \quad 10.47$$

where V_{ref} is the reference voltage, k is Boltzmann's constant, T is absolute temperature, R is switch resistance and f_c is the maximum clock frequency of the switch. You may assume that the system settles in $10t$ (where t = time constant), over one period of the clock frequency.

Finally, *Figure 4* shows one section of a switched capacitor ladder filter. Based on this filter structure, design a 3rd-order Chebyshev low-pass filter with a cut-off frequency of 5 kHz and a 1.0 dB pass band ripple. Assume a clock frequency of 100 kHz. Passive component values for the LC prototype, normalised to 1 rad/s, are $C_1 = C_3 = 2.0236$, $L_2 = 0.994$. In your analysis assume all integrators to be lossless. [10]

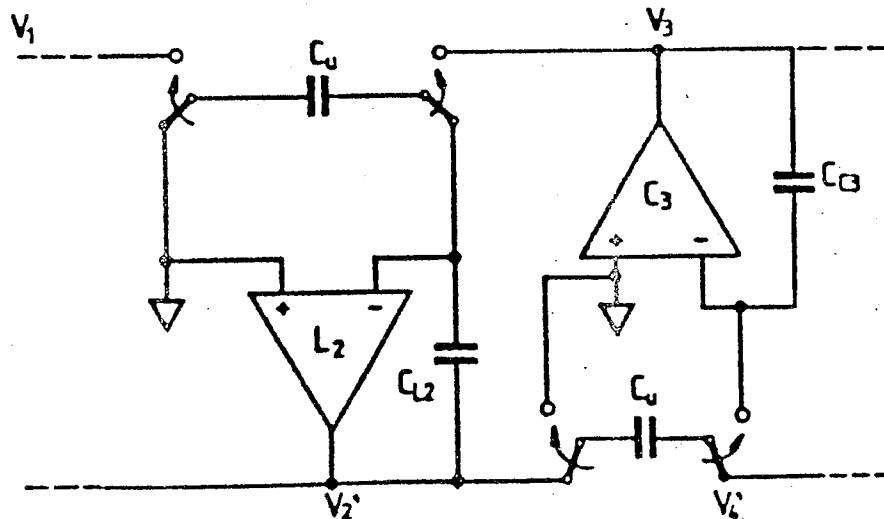


Figure 4

5. Classical CMOS operational amplifiers (op-amps) are either single-stage or two-stage designs. Based on the two stage design of *Figure 3* sketch a typical architecture for a two-stage cascoded output op-amp and a single-stage fully differential folded cascode op-amp. Briefly describe the operation of each of these op-amps and give one performance advantage and disadvantage of each compared to the basic op-amp architecture of *Figure 3*. Ignore common-mode feedback circuitry in the folded cascode op-amp. [18]

Finally, what is the function of the circuit of *Fig. 5(a)*? [7]

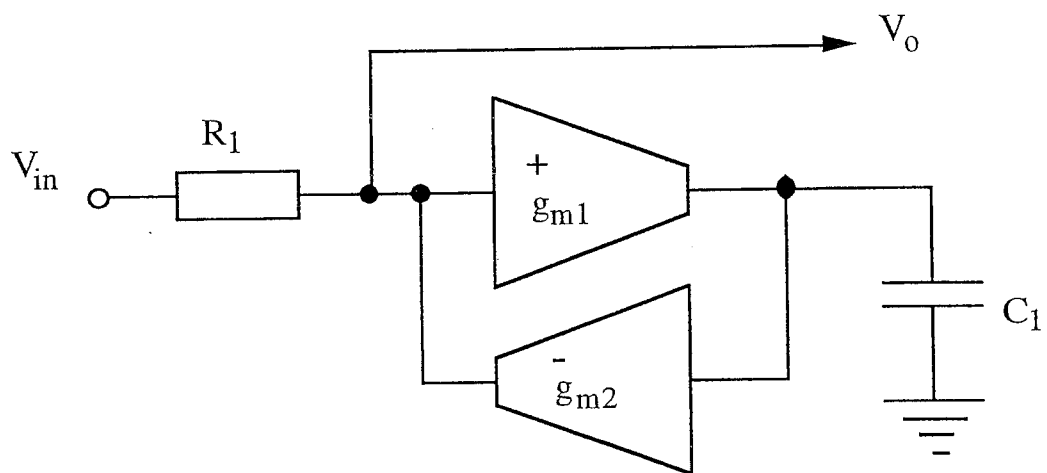


Figure 5(a)

6. In mixed-mode ASIC design, process technology is being optimised for digital performance specifications. Give one example of the constraints this places upon analogue circuit design performance.
Two high-performance analogue-to-digital converters are the current-mode algorithmic converter and the sigma-delta converter. Sketch a typical architecture for one of these converter types and explain its principles of operation. [18]

When prototyping high frequency amplifiers, why is a good ground plane important? [4]

Why is a x10 scope probe used for measuring high frequency signals on the oscilloscope? [3]

ANALOGUE INTEGRATED CIRCUITS & SYSTEMS

E3.01

ACI

Q1 For the bandgap voltage reference

$$V_{BE1} = V_{BE2} + I_2 R_3 \quad (\beta \gg 1)$$

Since $V_{BE1} - V_{BE2} = V_T \ln(I_1/I_2)$
 Then $V_0 = V_{BE3} + (R_2/R_3) V_T \ln(I_1/I_2)$

For $dv_0/dT = 0 \rightarrow$ assumes V_{BE} has -ve temp coefficient

Then $dV_{BE3}/dT = V_T/T (R_2/R_3) \ln(I_1/I_2)$

Since $dV_{BE3}/dT = -2.5 \text{ mV}/^\circ\text{C}$

$$\text{and } \frac{V_T}{T} = k/Q = 1.38 \times 10^{-23} / 1.6 \times 10^{-19}$$

$$= 8.625 \times 10^{-5}$$

$$\therefore (R_2/R_3) \ln(I_1/I_2) = 28.98 \pm 29$$

- [5]

rearranged gives

$$I_1 = I_2 \exp[29 R_3/R_2]$$

To calculate $V_0 \rightarrow$ require V_{BE} of Q_3

and $V_T = 300 \times 8.625 \times 10^{-5} = 25.9 \text{ mV}$

$$V_{BE} = V_T \ln\left[\frac{I_{C3}}{I_S}\right] = 25.9 \times 10^{-3} \ln\left[\frac{100 \times 10^{-6}}{1.2 \times 10^{-13}}\right]$$

$$= 0.532$$

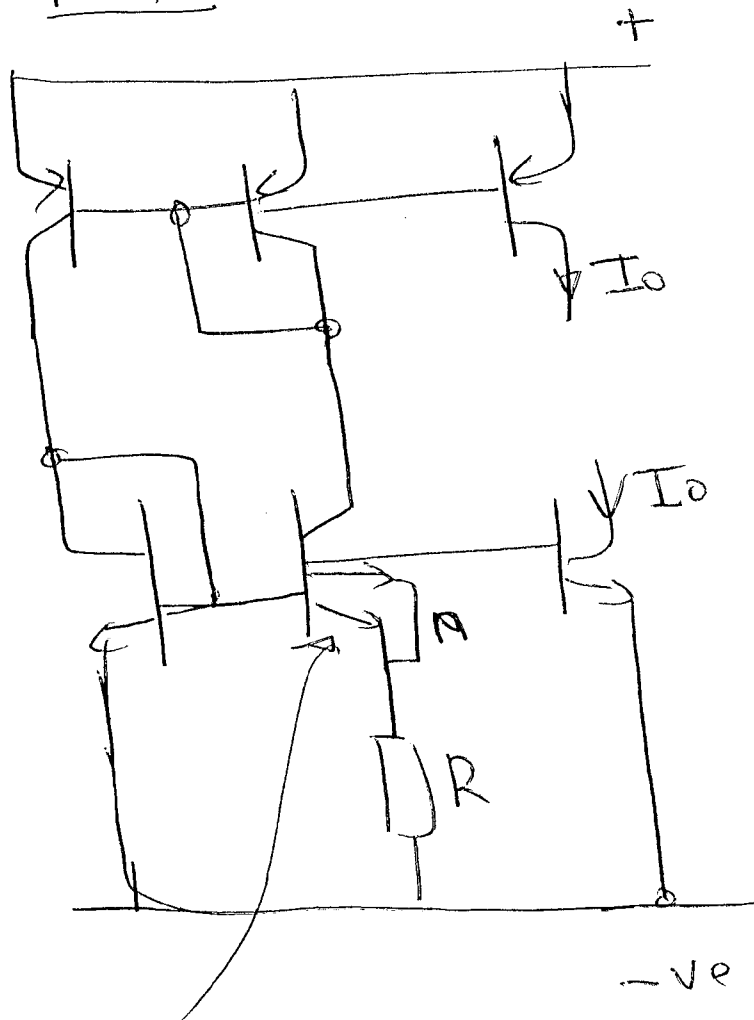
$$\therefore V_0 = 0.532 + [28.98](25.9 \times 10^{-3})$$

$$\approx \underline{\underline{1.283 \text{ volts}}}$$

— [5]

Q1 cont

PTAT



[7]

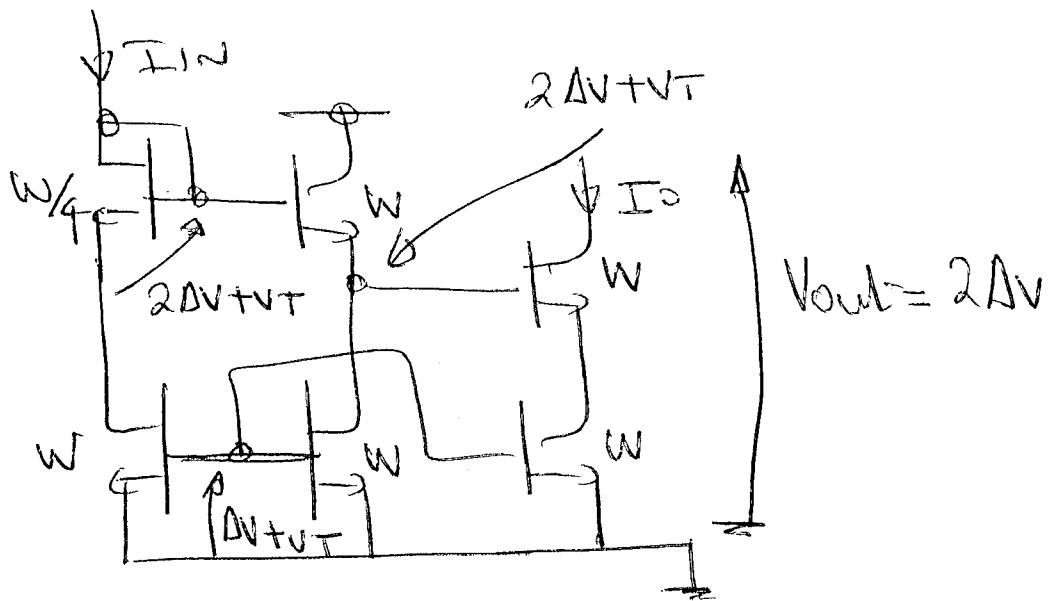
n-emitter - self biasing scheme
requires start-up current.

$$I_0 = V_T \ln [n/R] = 300 \mu A$$

for $n=2$

$$\therefore R = 60 \Omega.$$

Q1 cont



Assume equal L_s

$$I_O = I_{IN}, \beta_1 = \beta_2 = \beta_4 = \beta_5 = \beta_6 = \beta$$

$$\beta_3 = \beta/4$$

$$V_{sct3} = 2(V_{SS} - V_T)$$

$$\text{where } \Delta V = (V_{SS} - V_T)$$

$$\text{since } I_O = \beta (V_{SS} - V_T)^2$$

$$\text{then } (V_{SS} - V_T) = \sqrt{I_O / \beta} = \sqrt{\frac{100 \times 10^{-6}}{40 \times 10^{-6} / 2}}$$

$$\Delta V = 1.414 \text{ V}$$

[8]

Total 25/25.

Q2

Fig 2a is a self biased V_{BE} referenced current source and sink. Output current is virtually power supply independent since $I_O = V_{BE1}/R = V_{BE2}/R = \frac{V_T \ln(I_{IN}/I_{S1})}{R}$. Since I_{IN}

appears in the log and I_O sets I_{IN} then I_O is almost insensitive to power supply. However 2 stable states exist. $I_O \propto \ln(I_{IN})$ and $I_O = I_{IN}$.

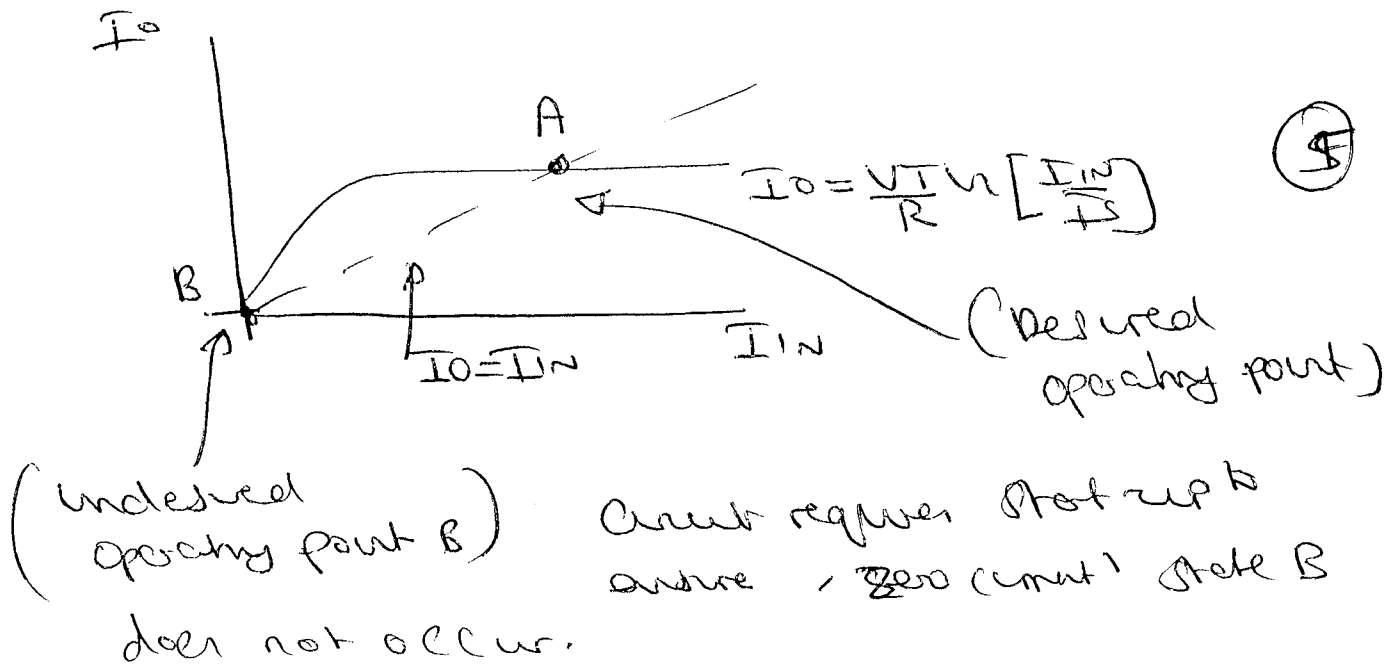


Figure 2(b), has the same fraction of supply independent biasing as Figure 2(a), and is known as a PTAT (proportional to Absolute Temp) constant current source/sink. The output current is now given by the difference between V_{BE1} and V_{BE2} , i.e. $I_O = \frac{V_{BE1} - V_{BE2}}{R}$

$$= \frac{V_T}{R} \ln \left[\frac{I_{IN}}{I_O} \times \frac{I_{S2}}{I_{S1}} \right]$$

Qn 2 cont

Since Q_2 has twice the emitter area of Q_1 then $I_{S2} = 2I_{S1}$, $I_0 = \frac{V_T}{R} \ln 2$

$I_0 = I_{in}$ from current mirror Q_4, Q_5 .

Some disadvantages in figure 2(a), requires automatic start-up circuit.

Note output current is now much less dependent upon I_{in} . Also PNTT results in lower temperature coefficient than

V_{BE} reference source because of positive temperature coefficient of V_T .

Fig 2(a) $\Rightarrow V_{BE1} = V_T \ln \left[\frac{10 \times 10^{-6}}{10^{-14}} \right] = 0.539V$

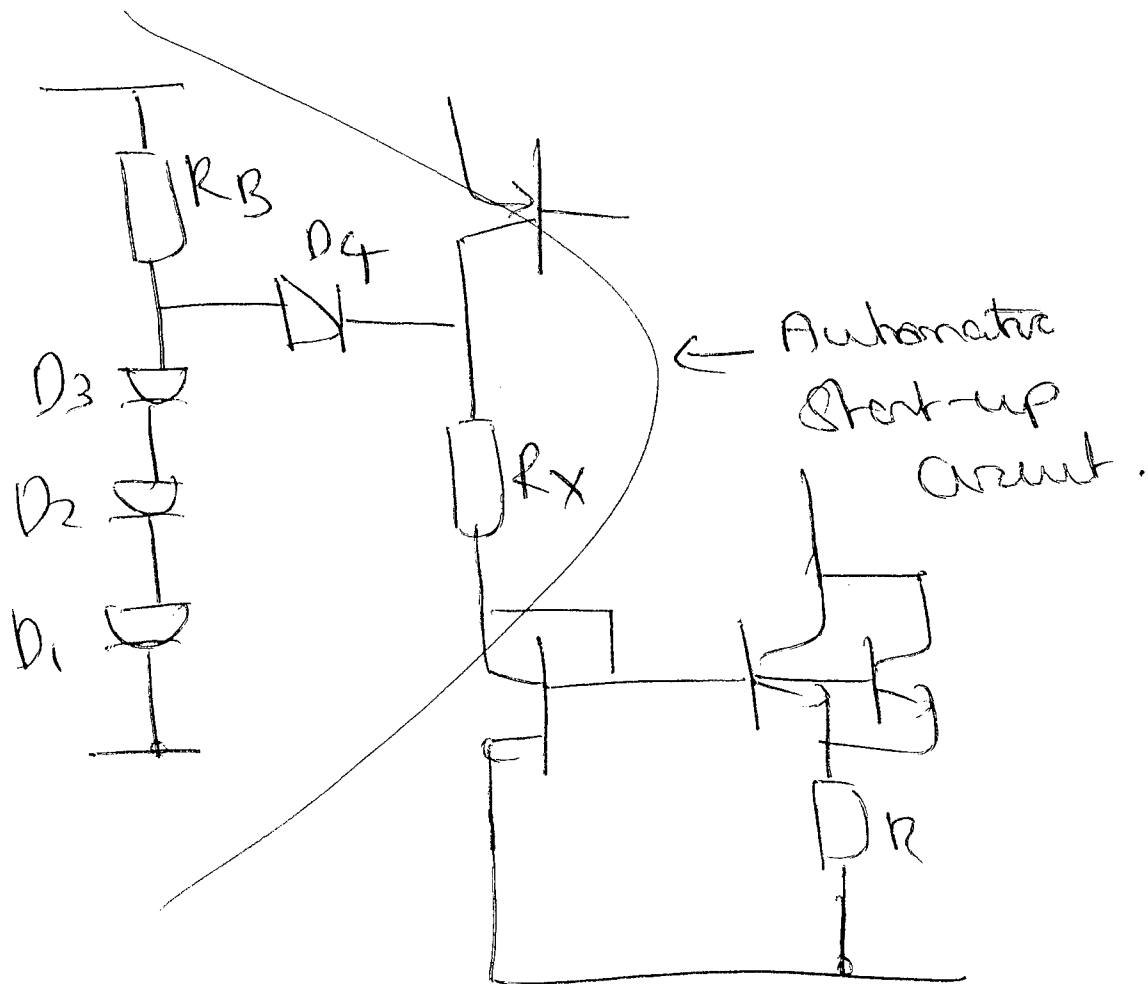
Since $I_0 = V_{BE}/R \Rightarrow R = 53.9k\Omega$

$$\begin{aligned} T_{ef} &= \frac{1}{V_{BE1}} \frac{\partial V_{BE1}}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T} \\ &= \frac{1}{0.539} \times (-2mV) - 1500 \times 10^{-6} = -0.52\%/^{\circ}C \\ &= \text{OR } -5200ppm/^{\circ}C \end{aligned} \quad (3)$$

Fig 2(b) $I_0 = \frac{V_T \ln 2}{R} \Rightarrow R = 1.8k\Omega$

$$\begin{aligned} T_{ef} &= \frac{1}{V_T} \frac{\partial V_T}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T} \\ &= \frac{1}{T} - \frac{1}{R} \frac{\partial R}{\partial T} = \frac{1}{300} - 1500 \times 10^{-6} = 0.18\%/^{\circ}C \\ &= \text{OR } 1833ppm/^{\circ}C \Rightarrow \text{lower} \end{aligned} \quad (3)$$

Qn 2 cont



(3)

last part of 2c

Transistor \$Q_3\$ cascodes \$Q_1\$

then $r_{o3} = r_{ds1} \parallel g_{m3} r_{ds3}$

\$Q_2\$ provides negative feedback current \$Q_1\$
to further increase the output resistance
of current to $r_{out} = \frac{g_{m2} (r_{ds2} \parallel r_{ds7})}{g_{m3} r_{ds3}}$

assuming equal \$g_m\$ and \$r_{ds}\$

then $r_{out} = \frac{g_m^2 r_{ds}^2}{2}$

(6)

7/23/23

Question 3

Specs $A = 80 \text{ dB}$, $S.R. = 5 \text{ V/MS}$, $G.B. = 3 \text{ MHz}$.

$$A_1 = g_{m2} / (g_{o2} + g_{o4})$$

$$(g_{o2} + g_{o4}) = I_{D2} [\lambda_N + \lambda_P] = 10 \times 10^{-6} [0.05] = 5 \times 10^{-7} \text{ S}^{-1}$$

$$g_{m2} = \sqrt{\beta_2 I_{D2}} \Rightarrow \text{but } G.B. = \frac{g_{m2}}{2\pi C_c}$$

Hence to calculate g_{m2} require C_c . Since

$$S.R. = I_0 / C_c \text{ then } C_c = 4 \text{ pF.} \Rightarrow g_{m2} = 7.5 \times 10^{-5} \text{ A/V}$$

$$\therefore A_1 = 150.8 \text{ From } g_{m2} \Rightarrow \beta_2 = 42 \times 10^{-4} = \left(\frac{K W}{2 L} \right)$$

$$\therefore (W/L)_2 = 9.47 \text{ OR } \approx (47/5)$$

$$(W/L)_1 = (W/L)_2 = 47/5$$

(8)

$$\text{Since } A_1 = 150.8, A_2 = (3981/80) \approx 66.3$$

$$\text{Now } A_2 = g_{m6} / (g_{o7} + g_{o6})$$

$$(g_{o7} + g_{o6}) = I_{D7} (\lambda_N + \lambda_P) = 20 \times 10^{-6} (0.05) = 1 \times 10^{-6} \text{ S}^{-1}$$

$$\text{giving } g_{m6} = 6.63 \times 10^{-5} \Rightarrow \beta_6 = \left(\frac{g_{m6}}{2} \right)^2 \frac{2}{I_{D6}} = 5.5 \times 10^{-5}$$

$$\therefore (W/L)_6 = \frac{2 \beta_6}{K} = 5.5 \text{ OR } (27.5/5)$$

(8)

Failed Phase Margin

Possible sequences.

$\left. \begin{array}{l} \text{Reduce } W_1 = W_2 \\ \text{Increase } W_6 \end{array} \right\}$

- ① Increase C_c [reduce $G.B$ and $S.R$]
- ② Increase I_0 to increase $S.R.$ [traded A_1]
- ③ Increase (W_2) hence g_{m2} to increase A_2 .

2-step solution

(5)

- ① Reduce $W_1 = W_2$ [reduces g_{m2} hence $G.B$ and A_1]

- ② Reduce I_0 [increased A_1 , but reduced $S.R$]

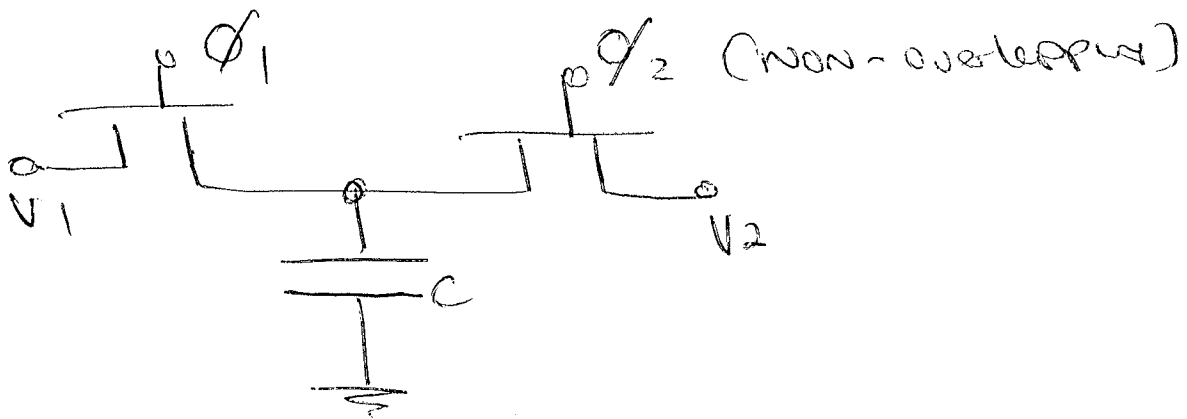
- ③ Can afford to increase $G.B$, increase C_c to increase $S.R.$ [Further reduced $G.B$]

PTO

Introduction of a series R with C introduces a tunable R.H.P zero which can either be adjusted ($1/\omega_{MG}$) into a L.H.P zero added phase lead compensation or used to cancel the amplifiers non-dominant pole.

④

Qn 4



Excess charge $\Delta Q = C[V_1 - V_2]$

$$I_{av} = \frac{\Delta Q}{T} = \frac{C[V_1 - V_2]}{T}$$

$$R_{eq} = \frac{(V_1 - V_2)}{I_{av}} = T/C$$

Assuming $f_{clock} \gg f_{signal}$

(5/3)

then $R_{eq} \approx \frac{1}{f_c C} \approx 10 \text{ M}\Omega$

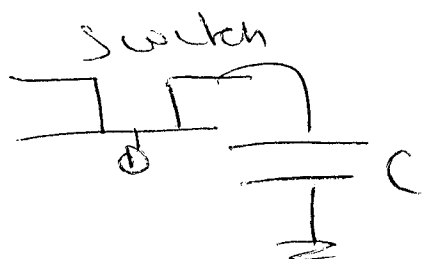
$f_c = 100 \text{ kHz}$, $C = 1 \text{ pF}$

(3/3)



$DR = V_{ref}/\text{Noise} = 2^N$

switch



Noise

$$\sqrt{\frac{KT}{C}}$$

(3/3)

Q24 4 cont

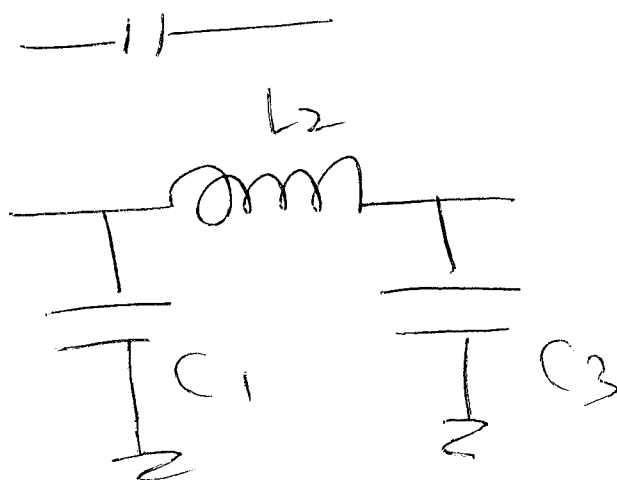
Assume $f_c = \frac{1}{10 \cdot R \cdot C}$

(2/2)

then solving for C gives

$$DR = 2^N = V_{\text{ref}} / \sqrt{K_T 10 R f_c}$$

(2/2)



Solution for
LCR prototype.

Inductive transformation $(L_2 / R_s) f_s$
 $= C_{L2} / C_u$

(3/3)

Capacitive transformation
 $= C_{C3} / C_u = f_c R_s C_3$

(3/3)

where R_s is normalized driving scaling

resistor,
 Assuming $R_s = 1$, $\left. \begin{aligned} C_{C1} / C_u &= f_c C_1 \\ C_{C3} / C_u &= f_c C_3 \\ C_{L2} / C_u &= f_c L_2 \end{aligned} \right\} \text{general transformation.}$

Qn 4 cont

Table values of C_1, L_2 and C_3 are normalized to $1 \text{ rad/s} \div 2\pi f_p$ ($f_p = 5 \text{ kHz}$)

$$C_1 = C_3 = 2.0236 / (2\pi \cdot 5 \times 10^3) = 6.44 \times 10^{-5} \text{ F}$$

$$L_2 = 0.994 / (2\pi \cdot 5 \times 10^3) = 3.164 \times 10^{-5} \text{ H}$$

For termination resistors (ie loss in input and output integrator.)

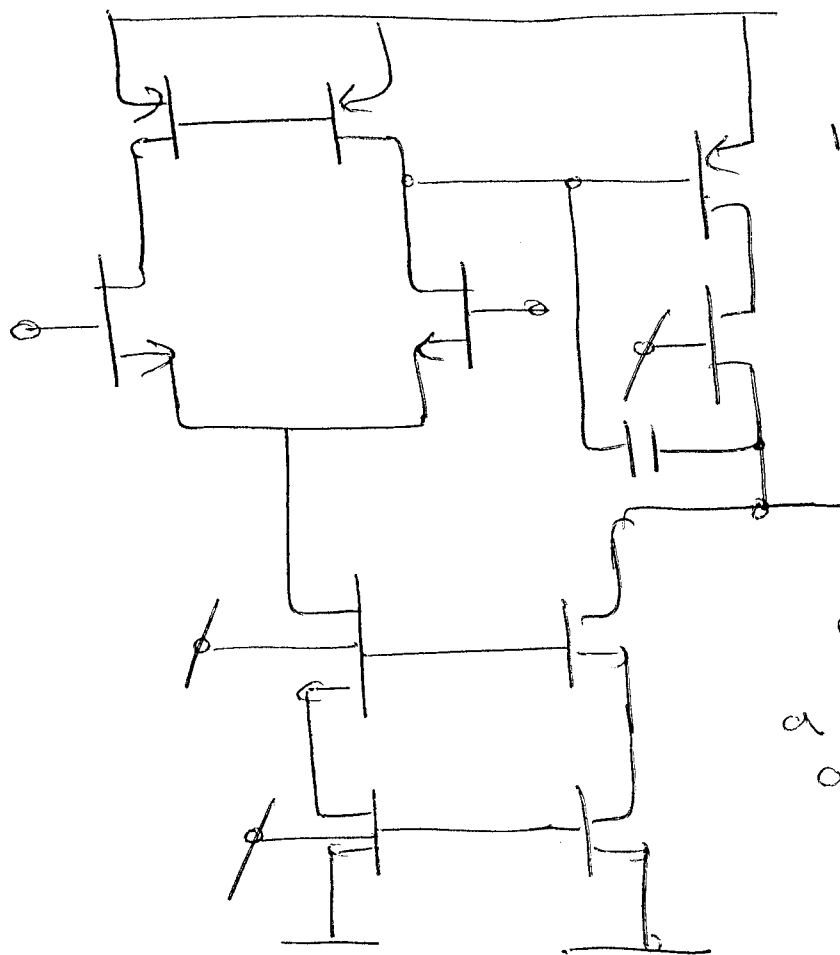
assume $C_u = C R_i = C R_o = 1 \text{ pF}$

Then $C_1 = C_3 = \underline{6.44 \text{ pF}}$

$$C_{L2} = \underline{3.164 \text{ pF.}} \quad (2/2)$$

BM $(25/25)$

Qn 5



INPUT - Diff pair with CM active load provides voltage gain of the order of $gm/2g_{o1}$.
Diff to single ended conversion

2nd gain stage is a single cascode amplifier with a voltage gain of the order of $(gm/2g_{o2})^2 \times 1/2$.

Main advantage

- Increase in overall voltage gain. [5]

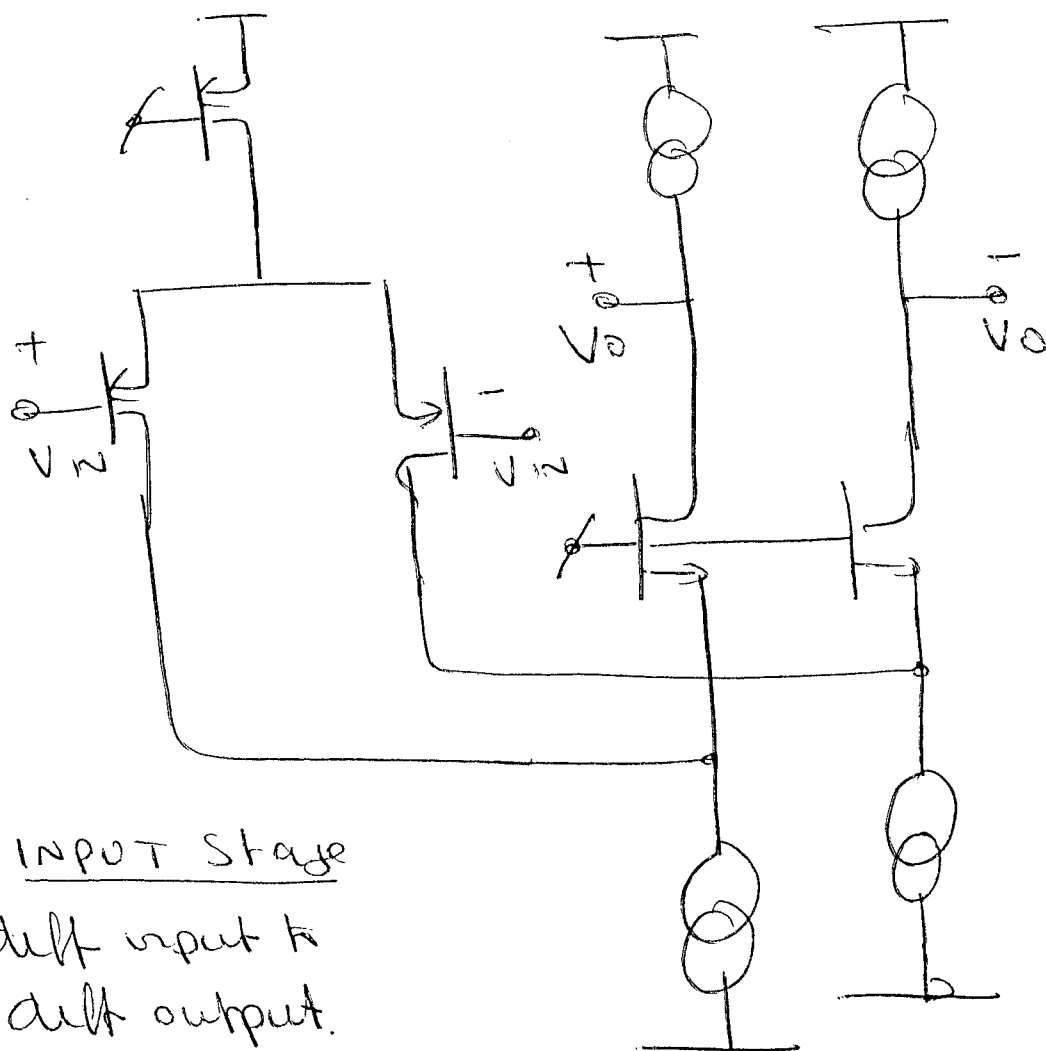
Disadvantages

- Phase margin reduced due to reduction in output pole frequencies
- Output voltage swing reduced due to cascode
- Input noise due to lower gain at input stage.

[4]

Qn 5 cont

Folded cascode amplifier.



INPUT Stage

diff input to
diff output.

Single path folded to output

Gain of the order of $gm^2/2go^2$

Main disadvantage

Output swing limited

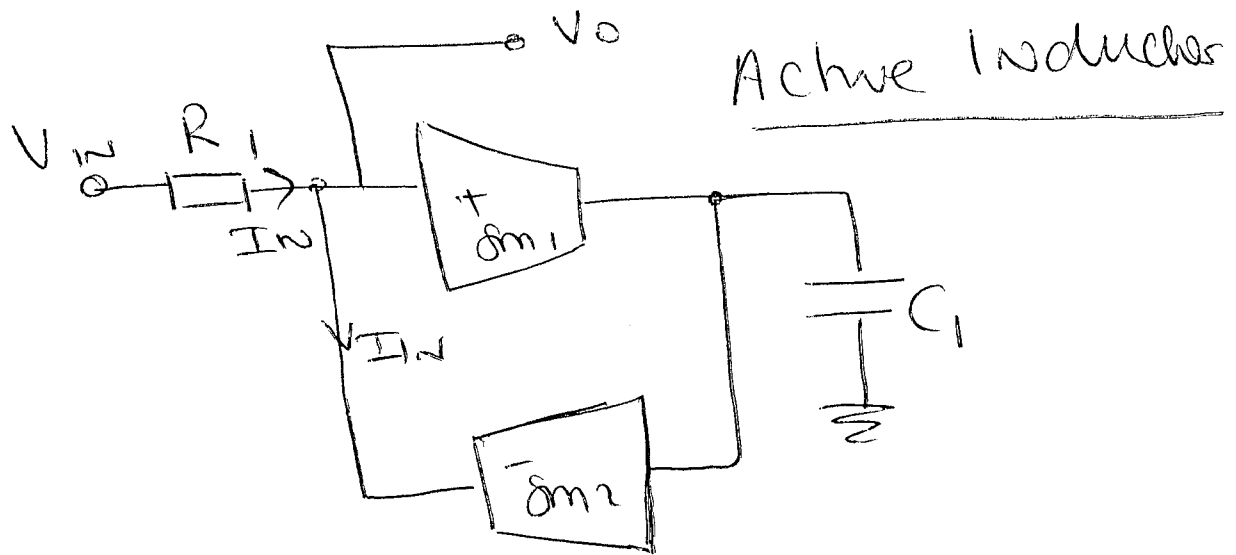
Main advantages

- Single high impedance at node of output (high speed)
- Good PSRR performance
- High CMVR
- Low noise - wideband
- Fully differential

[5]

[4]

Q5 cont



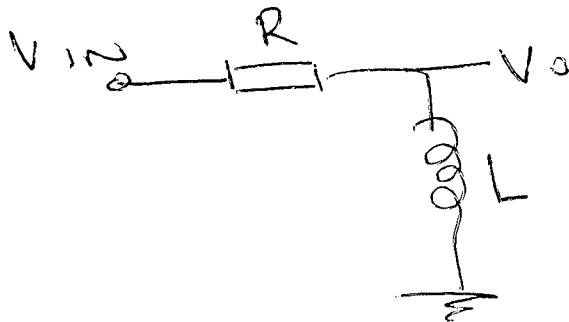
$$I_{IN} = g_{m2} V_O$$

$$V_O = \frac{g_{m1} V_{IN}}{sC}$$

$$\therefore I_{IN} = \frac{g_{m1} g_{m2} V_{IN}}{sC}$$

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} = s \frac{C}{g_{m1} g_{m2}} \quad [5]$$

$$Z_{IN} = sL = sC / g_{m1} g_{m2} \Rightarrow L = \frac{C}{g_{m1} g_{m2}}$$



High pass filter
of

$$f = \frac{1}{2\pi R \left[\frac{g_{m1} g_{m2}}{C} \right]}$$

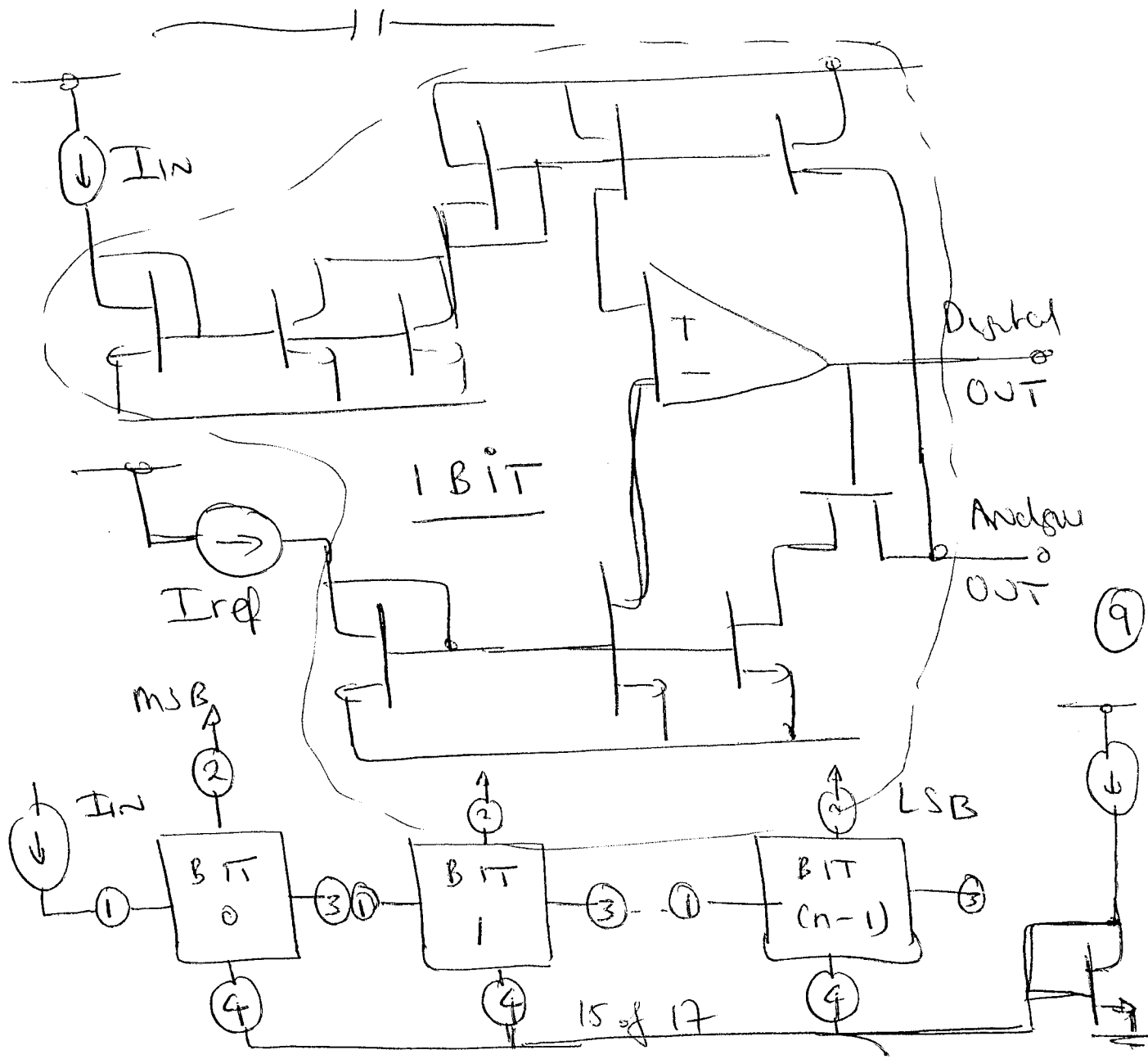
[2]

TOM 25/25

Q. 6/.

Examples : - Feature sizes will constantly shrink while threshold voltage will be lowered limiting performance of analogue switches (ii) Logic gate leakage will prevent optimum switched-capacitor filter performance (iii) As power supply voltages reduce, dynamic range of analogue parts will be limited

(4)



(9)

Qn 6 cont

Basic Architecture

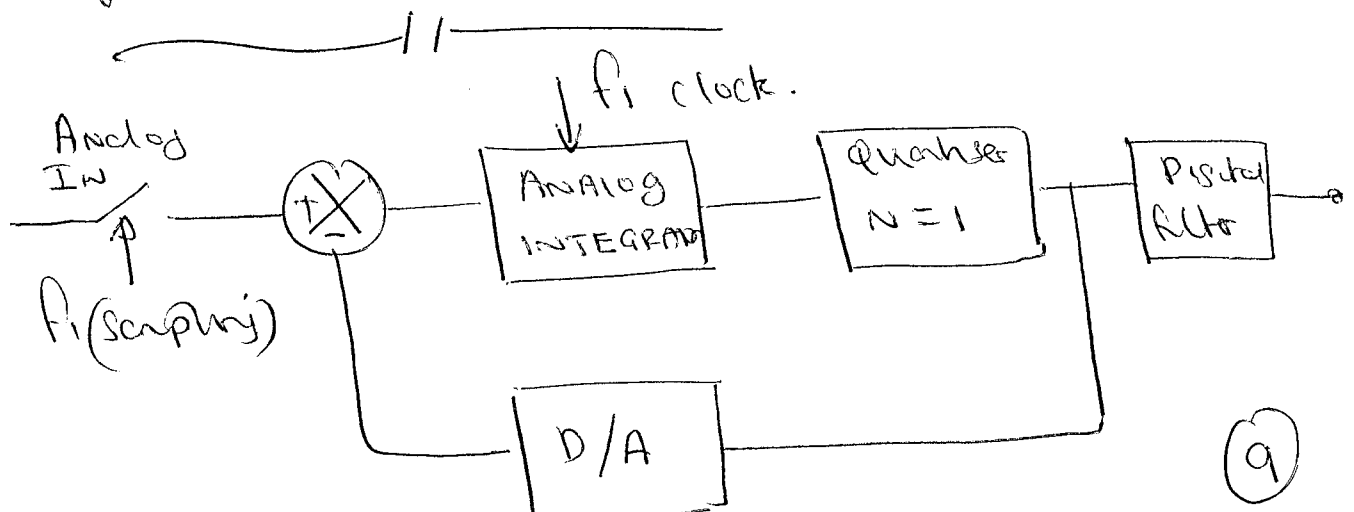
operation

$2I_{IN}$ on +ve terminal of comparator
Compares with I_{ref} (-ve) terminal.

if $2I_{IN} < I_{ref}$, comp output goes low, digital output = 0 and Analogue output $2I_{IN}$. if $2I_{IN} > I_{ref}$, comp output goes high, digital output = 1, analogue out $2I_{IN} - I_{ref}$.

Analogue output continuously feeds into following bit 'cell' which performs exactly the same function

The process is continued as many times as possible to achieve the required resolution.



Qn 6/cont

In the $\Sigma \Delta$ modulator, coarse quantization at high sampling rate is combined with -ve feedback and digital filtering to achieve increased resolution at low sampling rates. This reduces requirements upon component accuracy. The architecture includes a negative feedback loop producing a coarse estimate that oscillates about the true value of input, the digital filter averages this coarse estimate to produce a linear approximation. The feedback A/D and integrator force the quantization error to have a frequency spectrum. The output of the digital filter is down sampled and gives a multibit digital representation. All high frequency quantization noise is simply reduced.

(9)