E3.11
AO8

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2010

MSc and EEE PART III/IV: MEng, BEng.and ACGI

Corrected Copy

ADVANCED ELECTRONIC DEVICES

Thursday, 6 May 10:00 am

Q5 clarification.

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer Question One and FOUR other questions.

All questions carry equal marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : K. Fobelets, K. Fobelets
Second Marker(s) : W.T. Pike, W.T. Pike

Special instructions for invigilators

Q1 is compulsory

Special instructions for students

Q1 is compulsory

Constants and Formulae

permittivity of free space:	$\varepsilon_o = 8.85 \times 10^{-12}$ F/m
permeability of free space:	$\mu_o = 4\pi \times 10^{-7}$ H/m
intrinsic carrier concentration in Si:	$n_{i\,Si} = 1.45 \times 10^{10}$ cm^{-3} at T = 300K
intrinsic carrier concentration in GaAs:	$n_{i\,GaAs} = 1.79 \times 10^{6}$ cm^{-3} at T = 300K
dielectric constant of SiO_2:	$\varepsilon_{ox} = 4$
dielectric constant of Si:	$\varepsilon_{Si} = 11.8$
dielectric constant of GaAs:	$\varepsilon_{GaAs} = 12.9$
electron affinity of Si	$\chi_{Si} = 4.05$ eV
electron affinity of GaAs	$\chi_{GaAs} = 4.07$ eV
effective density of states of Si:	$N_{C\,Si} = 2.8 \times 10^{19}$ cm^{-3}
	$N_{V\,Si} = 1.04 \times 10^{19}$ cm^{-3}
effective density of states of GaAs:	$N_{C\,GaAs} = 4.7 \times 10^{17}$ cm^{-3}
	$N_{V\,GaAs} = 9.0 \times 10^{18}$ cm^{-3}
bandgap of Si	$E_{g\,Si} = 1.12$ eV
bandgap GaAs:	$E_{g\,GaAs} = 1.42$ eV
thermal voltage:	kT/e = 0.026V at T = 300K
charge of an electron:	$e = 1.6 \times 10^{-19}$ C (1 eV)

$$p = N_v e^{(E_v - E_F)/kT} \text{ and } p_i = N_v e^{(E_v - E_i)/kT}$$
$$n = N_c e^{(E_F - E_c)/kT} \text{ and } n_i = N_c e^{(E_i - E_c)/kT}$$

Carrier density

$$I_{DS} = \frac{\mu C_{ox} W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right)$$

MOSFET current

$$V_{th} = \phi_m - \phi_s + 2\times\phi_F + \gamma \times \sqrt{2\times\phi_F}$$

Threshold voltage

$$\phi_F = \frac{kT}{e}\ln\left(\frac{N_A}{n_i}\right)$$

Fermi potential (difference between intrinsic and Fermi level)

$$\gamma = \frac{\sqrt{2e\varepsilon_s N_A}}{C_{ox}}$$

Body effect coefficient

$$J = \frac{eD_n n_p}{L_n}\left(e^{\frac{eV}{kT}} - 1\right) + \frac{eD_p p_n}{L_p}\left(e^{\frac{eV}{kT}} - 1\right)$$

Diode diffusion current density

$$V_0 = \frac{kT}{e}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Built-in voltage

$$W_{depl}(V) = \left[\frac{2\varepsilon(V_0 - V)}{e}\frac{N_A + N_D}{N_A N_D}\right]^{1/2}$$

Depletion width in pn diode

The Questions

1. Compulsory question.

a) When the gate length of a MOSFET is reduced to a value well below 500 nm without changing any other parameter, short channel effects occur.

i) Give two changes to the MOSFET characteristics that are caused by these short channel effects.

[2]

ii) Propose two methods that reduce short channel effects in MOSFETs.

[2]

iii) Give the two geometrical/material parameters that determine the value of the threshold voltage in a long channel MOSFET.

[2]

iv) Give a physics based reason (brief) why each of these parameters in iii) is increasing/decreasing the threshold voltage.

[2]

b) Sketch the energy band diagram (E_c, E_v, E_F, E_G) of an Ohmic contact on an n-type semiconductor and show that increasing the doping density improves the quality of the contact.

[4]

c) The sub-threshold slope is given by $S = \frac{kT}{e} \times \ln(10) \times \left(1 + \frac{C_B}{C_{ox}}\right)$. Why does S approach its theoretical minimum in a finFET with a narrow, thin channel? C_B is the bulk capacitance and C_{ox} is the oxide capacitance.

[4]

d) Give the two reasons for the increase of the mobility in an oxide-gated buried channel modulation doped Si field effect transistor (MODFET).

[4]

2. MEDICI TCAD of a semiconductor device.

line	Input file
1	TITLE A semiconductor device
2	
3	MESH
4	x.mesh x.max=0.90 h1=0.010
5	y.mesh y.max=0.010 h1=0.0025
6	y.mesh y.max=0.016 h1=0.0020
7	y.mesh y.max=0.050 h1=0.0010
8	y.mesh y.max=0.100 h1=0.0020
9	y.mesh y.max=0.300 h1=0.0050
10	y.mesh y.max=0.500 h1=0.0100
11	y.mesh y.max=1.500 h1=0.0150
12	
13	region num=1 x.min=0.3 x.max=0.6 y.min=0.0 y.max=0.01 polysilicon
14	region num=2 x.min=0.0 x.max=0.9 y.min=0.016 y.max=0.120 silicon
15	region num=3 x.min=0.0 x.max=0.9 y.min=0.12 y.max=0.220 silicon
16	region num=4 x.min=0.0 x.max=0.9 y.min=0.22 y.max=0.320 silicon
17	region num=5 x.min=0.0 x.max=0.9 y.min=0.32 y.max=1.500 silicon
18	region num=6 x.min=0.3 x.max=0.6 y.min=0.01 y.max=0.016 s.oxide
19	region num=7 x.min=0.0 x.max=0.3 y.min=0.00 y.max=0.016 s.oxide
20	region num=8 x.min=0.6 x.max=0.9 y.min=0.00 y.max=0.016 s.oxide
21	
22	electr name=C1 x.min=0.65 x.max=0.90 y.min=0.0 y.max=0.0
23	electr name=C2 x.min=0.00 x.max=0.25 y.min=0.0 y.max=0.0
24	electr name=C3 x.min=0.30 x.max=0.60 y.min=0.0 y.max=0.01
25	electr name=C4 bot
26	
27	profile y.min=0.016 y.max=1.500 impurity=B n.peak=1.e17 uniform
28	profile x.min=0.0 x.max=0.25 y.min=0.016 y.max=0.3 impurity=As n.peak=4.e19 uniform
29	profile x.min=0.65 x.max=0.9 y.min=0.016 y.max=0.3 impurity=As n.peak=4.e19 uniform
30	profile x.min=0.25 x.max=0.3 y.min=0.016 y.max=0.12 impurity=As n.peak=1.e19 uniform
31	profile x.min=0.6 x.max=0.65 y.min=0.016 y.max=0.12 impurity=As n.peak=1.e19 uniform
32	
33	contact name=C3 print n.polysili
34	
35	models analytic e.effect temperat=300. print
36	symbolic gummel carriers=2 electron holes
37	method itlimit=80
38	solve v(C1)=0.000 v(C2)=0.00 v(C3)=0.000 v(C4)=0.00
39	solve elec=C1 vstep=0.050 nstep=2 project
40	solve elec=C3 vstep=-0.10 nstep=5 project
41	
42	log IVFILE=ivdc
43	loop steps=30
44	solve elec=C3 vstep=+0.05 nstep=1 project
45	l.end

On p.4 the MEDICI input file of a MOSFET is given. Read it carefully to answer the following questions.

a)

i) Give the gate length.

[2]

ii) Give the oxide thickness.

[2]

iii) Define contacts C1, C2, C3, C4 in MOSFET terms (gate, source, bulk, drain).

[4]

iv) Sketch the complete source contact region on an x-y graph and indicate the doping density and dimension of the different regions.

[4]

v) Sketch the data that occurs in the file ivdc, labelling your axes and indicating the minimum and maximum values on the x-axis as defined in the input file.

[4]

b) There are two errors in the input file.

i) Give the line numbers on which these errors occur.

[2]

ii) Give the corrected version of these two lines.

[2]

3. MEDICI TCAD of a semiconductor device.

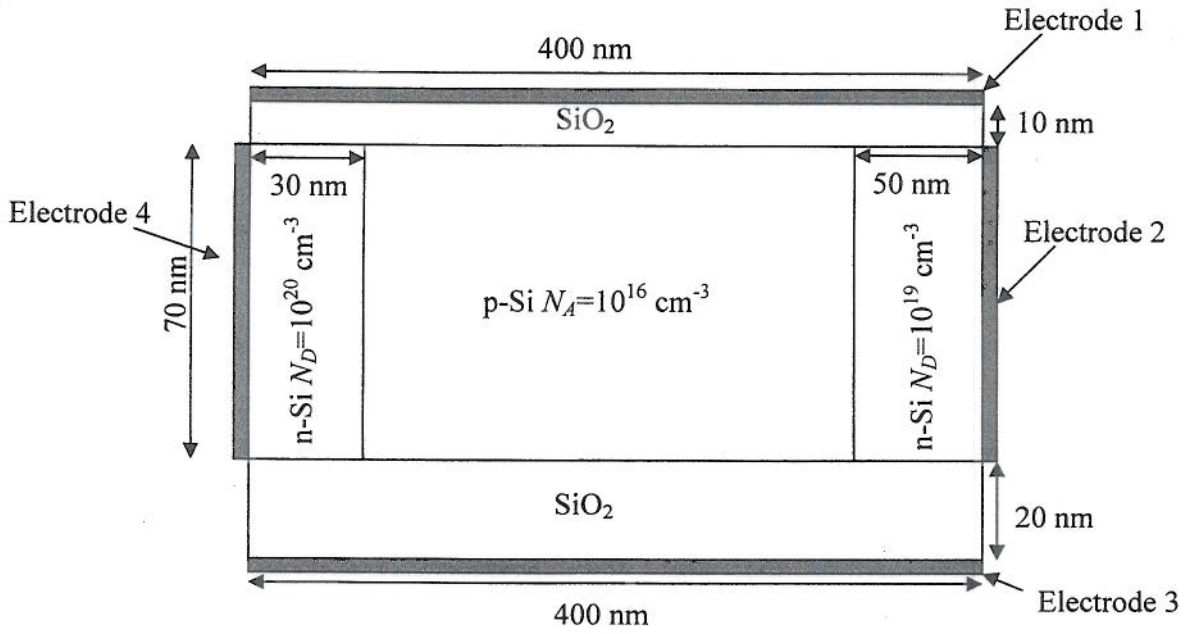

Figure 3.1 Geometry of an oxide gated Field Effect Transistor. All electrodes are 1 dimensional.

a) Write the MEDICI input file for this device that defines the structure. Your input files should include the functions:
1. TITLE
2. MESH
3. REGION
4. ELECTRODE
5. PROFILE

[10]

b)

i) Which device does this input file describe?

[2]

ii) Give the number of the contact(s) that can act as a gate and briefly explain your answer.

[5]

iii) Of the gate contacts you have identified in 3 b)ii) which has the largest influence on the carriers underneath it? Briefly explain your answer.

[3]

4. Long channel silicon MOSFET

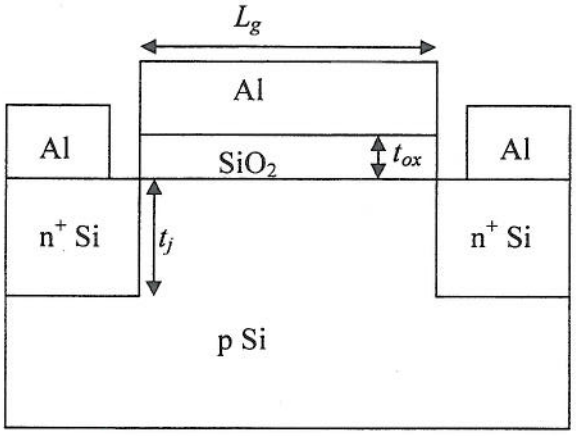

Figure 4.1 Cross section of a MOSFET.

The parameters of the silicon MOSFET given in fig. 4.1 are: gate length $L_g = 2$ μm, gate width $W_g = 100$ μm, oxide thickness $t_{ox} = 100$ nm, junction depth $t_j = 500$ nm, doping in substrate $N_A = 10^{16}$ cm^{-3}, doping in ohmic contact regions $N_D = 10^{19}$ cm^{-3}. The work function of aluminium is $\phi_m = 4.8$eV. The operation temperature is 300K.

a) Sketch the energy band diagram (E_c, E_v, E_F) from the gate to the substrate midway between the source and drain of the long channel MOSFET when no bias is applied. Ensure that all relative distances between the energy levels in the band diagram are correct. Also indicate work functions and electron affinities where appropriate. Note $\phi_m \neq \phi_{Si}$.

[8]

b) Calculate the flat band voltage V_{FB} for the gate-oxide-semiconductor junction.

[5]

c)

i) Give the expression of the voltage dropped across the oxide V_{ox} as a function of the applied gate voltage V_{GS} and the voltage drop across the semiconductor V_s.

[2]

ii) Give the expression of V_s at threshold.

[2]

ii) If we change the work function of the metal on the gate to be $\phi_m = \phi_{Si}$, would the threshold voltage increase or decrease? Give a brief reason for your answer.

[3]

5. n-type GaAs-based MESFET.

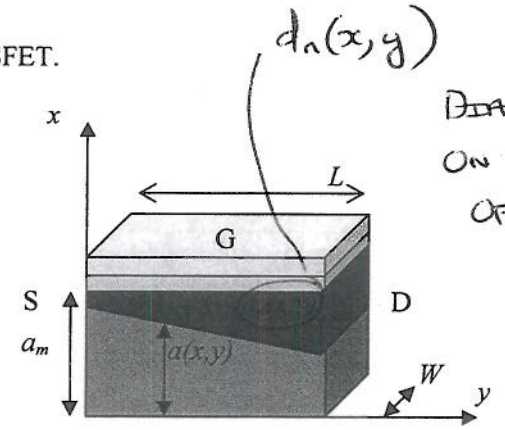

DIAGRAM MADE CLEAR ON BOARD AT START OF EXAM (10.00AM)

Figure 5.1 Schematic diagram of a biased n-MESFET. a_m is the metallurgic depth of the GaAs channel, $d_n(x,y)$ is the depletion width, L is gate length, W is gate width. S, D, G are respectively source, drain and gate contact position.

a)

i) What type of contact forms the gate of a MESFET?

[3]

ii) Is a MESFET an enhancement or depletion mode device? Explain briefly.

[3]

iii) Why do you expect the leakage currents in a Si MESFET to be higher than in a GaAs MESFET?

[4]

b) Sketch the energy band diagram (E_c, E_v, E_F, E_G) from the gate to substrate midway between source and drain of the MESFET when no bias is applied. Indicate the build-in potential V_{bi} and gate barrier height ϕ_B on the diagram.

[5]

c) Give the expression of the active channel depth $a(x,y)$ as a function of x, y, material parameters and applied drain and gate voltage (V_{DS} and V_{GS} resp.). You can assume that the variation of the longitudinal potential $V(y)$ between source and drain is linear.

[5]

6. Si/SiGe modulation doped field effect transistor.

a)

i) Which layer is strained when a thin layer of Si is epitaxially grown on a thick $Si_{0.7}Ge_{0.3}$ virtual substrate?

[2]

ii) What type of strain can be found in this layer (tensile or compressive)?

[2]

ii) What is modulation doping and explain briefly why it is used?

[4]

b) Look carefully at fig. 6.1 to answer the following question.

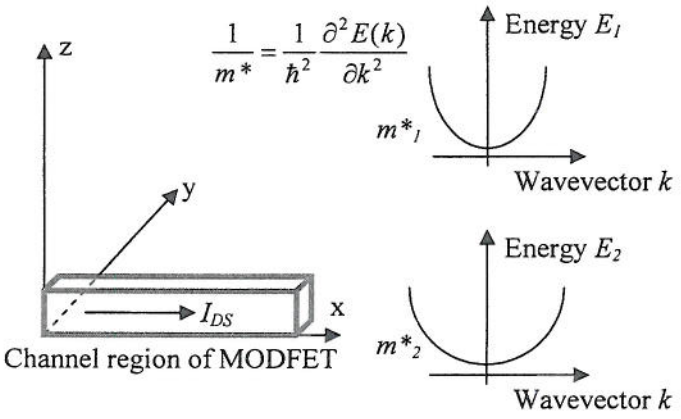

Figure 6.1 Left: current through the channel of a MODFET, right: dispersion relations for the different conduction bands in the strained layer. The equation defines the effective mass, m^*_1 and m^*_2 are the effective mass of the carriers in the respective valleys E_1 and E_2.

i) In an unstrained MOSFET channel, carriers move in 6 equivalent conduction band valleys, 4 of them are given by the $E_2(k)$ dispersion relation and 2 of them are given by the $E_1(k)$ dispersion relation. Derive the expression for the average effective mass of carriers moving through the unstrained channel.

[4]

ii) In the strained MODFET channel carriers move only in the $E_1(k)$ band. Derive the expression for the average effective mass of carriers moving through the strained channel.

[4]

iii) Give two benefits for the introduction of this type of strain in the channel of the field effect transistor.

[4]

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The Answers 2010

1. Compulsory question.

a) i) 2 out of the following list:
Threshold voltage changes, DIBL (drain induced barrier lowering), increase in sub-threshold slope S, current increases faster than with 1/L, higher output conductance

[2]

ii) 2 out of the following list:
Decrease of oxide thickness, increase the doping density in the channel reduce the junction depth, apply different specialist doping techniques in the channel

[2]

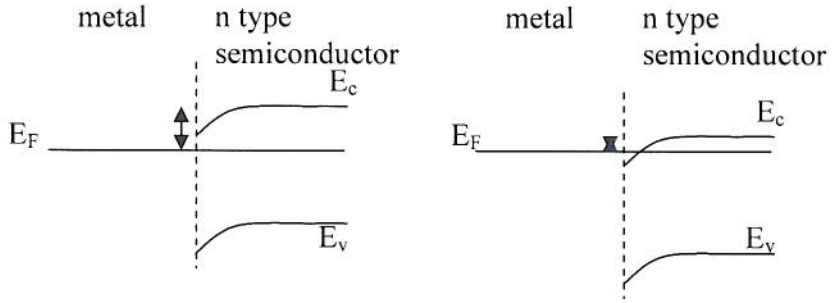
iii) oxide thickness, doping in channel.

[2]

iv) The thinner the oxide the less voltage drop across the oxide and thus more across the semiconductor thus threshold is reach at lower gate voltages (in absolute value)
Increasing the doping density in the channel will increase the threshold voltage because more majority carriers need to be depleted and more minority carriers attracted underneath the gate to create inversion.

[2]

b) ohmic contact is obtained when there is no high potential barrier against current flow. Thus the work function difference between metal and semiconductor increases the density of majority carriers at the interface. Below left is the solution for an n-doped semiconductor (E_c closer to E_F than E_v). In order to improve the ohmic contact the doping in the semiconductor needs to be increased (see the right figure below), this causes a lowering of the barrier for lower energetic electrons as indicated by the arrows on the diagrams.



[4]

c) In a finFET two or more gates exists thus the value of C_{ox} increases. Since the channel is thin and narrow the volume of depletion charges is restricted thus C_B reduces. Thus $\frac{C_B}{C_{ox}} < 1 \rightarrow S = \frac{kT}{e}\log_{10}(1)$

[4]

d) The buried channel removes the carriers from the SiO2-Si interface and thus interface roughness scattering decreases.
Modulation doping separates the doping atoms from the channel and thus impurity scattering decreases.

[4]

2. MEDICI TCAD of a semiconductor device.

a) .

i) 300 nm

[2]

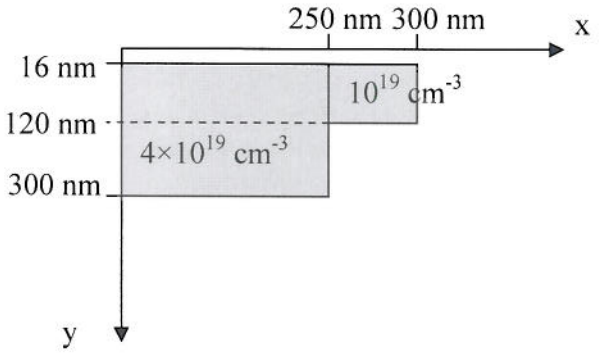
ii) 6 nm

[2]

iii) C1 drain (positive bias is applied on C2)
C2 source
C3 gate
C4 bulk

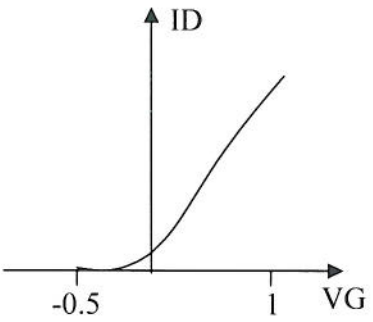
[4]

iv)



[4]

v) [4]



b) There are two errors in the input file.

i) 22 & 23

[2]

ii)

22	electr name=C1 x.min=0.65 x.max=0.90 y.min=0.016 y.max=0.016
23	electr name=C2 x.min=0.00 x.max=0.25 y.min=0.016 y.max=0.016

[2]

3. MEDICI TCAD of a semiconductor device.

a)

```
TITLE    A finFET

MESH
x.mesh  x.max=0.40  h1=0.005
y.mesh  y.max=0.10  h1=0.010

region num=1 x.min=0.0 x.max=0.4 y.min=0.0  y.max=0.01 s.oxide
region num=2 x.min=0.0 x.max=0.4 y.min=0.01  y.max=0.08 silicon
region num=3 x.min=0.0 x.max=0.4 y.min=0.08  y.max=0.10 s.oxide

electr  name=source  x.min=0.0 x.max=0.0 y.min=0.01 y.max=0.08
electr  name=drain   x.min=0.4 x.max=0.4 y.min=0.01 y.max=0.08
electr  name=gate1   x.min=0.0 x.max=0.4 y.min=0.0 y.max=0.0
electr  name=gate2   x.min=0.0 x.max=0.4 y.min=0.1 y.max=0.1

profile  x.min=0.0  x.max=0.4 y.min=0.01  y.max=0.8  impurity=B n.peak=1.e16  uniform
profile  x.min=0.0  x.max=0.03 y.min=0.01  y.max=0.3  impurity=As n.peak=1.e20  uniform
profile  x.min=0.35  x.max=0.4 y.min=0.01  y.max=0.3  impurity=As n.peak=1.e20  uniform
```

NOTE: other solutions are possible [10]

b)

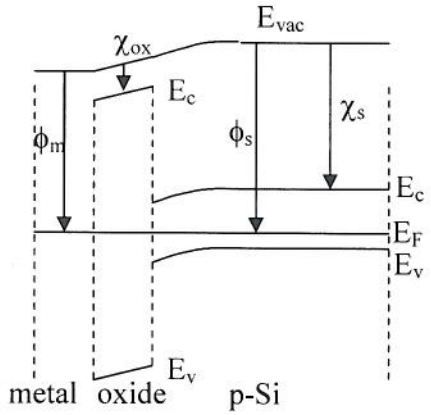
i) finFET or double gated MOSFET [2]

ii) Electrode 1 and electrode 2 as they are both defined on oxide. [5]

iii) Electrode 1 because it is separated from the channel with the thinnest oxide layer thus represents the largest capacitance. [3]

4. Long channel silicon MOSFET

a) $\phi_s=\chi_s+(E_c - E_F)$.
$\phi_s = 4.955$ eV (see calculations done in b)
Thus $\phi_m<\phi_s$ and therefore band bending will exist without a voltage applied.



[8]

b) $V_{FB} =\phi_m-\phi_s$
$\phi_s=\chi_s+(E_c - E_F)$

$$n = N_c e^{(E_F-E_c)/kT} = \frac{n_i^2}{N_A} \rightarrow E_F - E_c = kT \ln \frac{n_i^2}{N_A N_c} \text{ or } E_c - E_F = kT \ln \frac{N_A N_c}{n_i^2}$$

$$V_{FB} = \phi_m - \left(\chi_s + kT \ln \frac{N_A N_c}{n_i^2} \right) = 4.8 - \left(4.05 + 0.026 \ln \frac{10^{16} \times 2.8 \times 10^{19}}{(1.45 \times 10^{10})^2} \right)$$

$$V_{FB} = 4.8 - (4.05 + 0.905) = -0.155V$$

$\phi_s = 4.955$ eV

[5]

c)

i) $V_{ox} = V_{GS} - V_s$.

[2]

ii) $V_s = 2\phi_F$ (see formulae list for fF).

[2]

iii) The threshold voltage would be higher because (with reference to the energy band diagram above) we see that if there is a work function difference as given, the conduction band is already bending down (inverting), thus less gate voltage must be applied for full inversion. If the work function difference does not exist then we start from flat band and a higher voltage needs to be supplied. Note that is there is sufficient band bending that we go into depletion mode operation.

[3]

5. n-type GaAs-based MESFET.

a)

i) Schottky contact

[3]

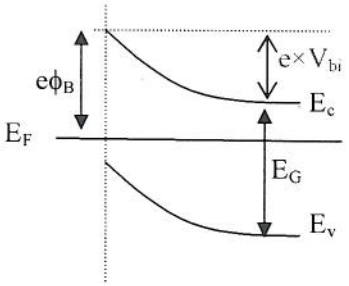
ii) Depletion mode because if we forward bias the gate (enhancement) then there will be a large gate leakage current flowing.

[3]

iii) Because the intrinsic carrier concentration in Si is higher than in GaAs, thus a Si undoped substrate will be more conductive than a GaAs substrate. As a consequence there will be a higher substrate leakage current.

[4]

b)



[5]

c)

i) From the formulae list we find the depletion region for a pn diode:

$$W_{depl}(V)=\left[\frac{2\varepsilon(V_0-V)}{e}\frac{N_A+N_D}{N_AN_D}\right]^{1/2}$$

In the case of a MESFET we have a one-sided junction that means that we can approximate the depletion width in the MESFET as for $N_A>>N_D$ and thus the equation becomes:

$$W_{depl}(V)=\left[\frac{2\varepsilon(V_0-V)}{e}\frac{1}{N_D}\right]^{1/2}$$

V_0 is the built-in voltage, V is the voltage as each point y in the channel. This voltage is determined by the difference between the lateral (V_{DS}) and horizontal voltage (V_{GS}): $V=V_{GS}-V(y)$.

V(y) can be assumed to vary linearly between source and drain thus:

$V(y)=ay+b$ (a and b constants to be determined by boundary conditions)

@source y=0 and $V(0)=0 \rightarrow b=0$

@drain y=L and $V(L)=V_{DS} \rightarrow a=V_{DS}/L$

Thus $V(y)= V_{DS}\times y/L$

$$d_n(y)=W_{depl}(V(y))=\sqrt{\frac{2\varepsilon(V_0-V_{GS}+V(y))}{eN_D}}=\sqrt{\frac{2\varepsilon\left(V_0-V_{GS}+\frac{V_{DS}\times y}{L}\right)}{eN_D}}$$

[5]

$$a(y)=a_m-\sqrt{\frac{2\varepsilon\left(\phi_m-\phi_s-V_{GS}+\frac{V_{DS}\times y}{L}\right)}{eN_D}}$$

6. Si/SiGe modulation doped field effect transistor.

a)

i) the thin Si layer

[2]

ii) tensile

[2]

ii) Modulation doping is a technique to separate the doping atoms from the channel of the FET. It is used to remove impurity scattering and thus increase mobility.

[4]

b)

i) $$\frac{1}{m^*} = \frac{1}{6}\left(\frac{4}{m_2} + \frac{2}{m_1}\right) = \frac{1}{3}\left(\frac{2}{m_2} + \frac{1}{m_1}\right)$$

[4]

ii) $$\frac{1}{m^*} = \frac{1}{2}\left(\frac{2}{m_1}\right) = \frac{1}{m_1}$$

[4]

iii) The effective mass is smaller, from previous $m_1 < m_2$
phonon scattering processes are reduced because 4 of the valleys moved to higher energies and no scattering exist with those.
Both of these increase the mobility.

[4]