1. a) State two advantages and two disadvantages of using a purely analogue approach to conduct signal processing.

[Bookwork]
Advantages:
1. You can use the physical primitives of the devices to perform computation. [1]
2. One wire can represent many bits of information, there is no quantisation error. [1]

Disadvantages:
1. It is not easily programmable. [1]
2. It is prone to offset and noise. [1]

[Total 4 points]

b) i) Derive the transconductance efficiency for transistors operating in weak and strong inversion and show using a graph which one is more efficient terms of bias current.

Application of taught theory
Weak Inversion:

$$I_{DS(wi)} = I_0 \exp\left(\frac{V_{GS}}{nU_t}\right)$$

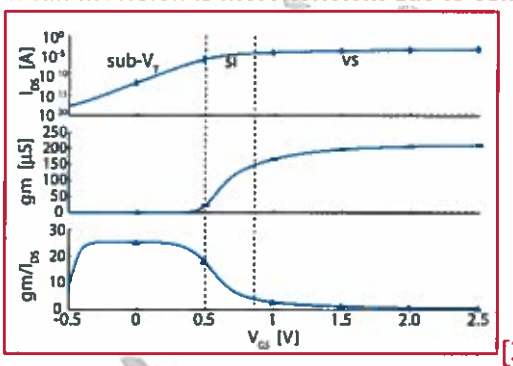
Transconductance efficiency: $\boxed{\frac{g_m}{I_{DS(wi)}} = \frac{1}{nU_t}}$ [1]

Strong inversion:

$$I_{DS(si)} = \beta(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Transconductance efficiency: $\boxed{\frac{g_{m(si)}}{I_D} = 2\sqrt{\frac{\beta}{I_D}}}$ [1]

Weak inversion is more efficient due to constant maximum transconductance efficiency.



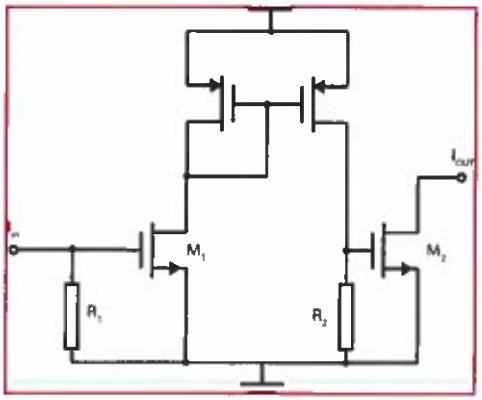
[2]

[Total 4 points]

ii) Using two or more transistors operating in these two modes plus two resistors, draw a circuit which implements the following function stating assumptions for the choice of resistors R_1 and R_2:

$$I_{out} = \beta\left(I_o R_2 exp\left(\frac{I_{in}R_1}{nU_t}\right) - V_{TH}\right)^2$$

New circuit derivation. The student should realise he can compute I_{out} using the simple physical primitives of the MOS transistor. R_1 needs to be selected to guarantee $V_{GS1} < V_{TH}$ such that transistor M1 is in Weak inversion and R_2 needs to be selected such than $V_{GS2} > V_{TH}$ such that transistor M2 is in Strong inversion.



[Total 4 points]

c) The total noise of a MOS transistor is defined as follows:

$$v_n^2 = \frac{K_w}{I_D^p} \cdot \Delta f + \frac{K_f}{A} \cdot \ln\left(\frac{f_h}{f_l}\right)$$

(i) Using this equation, derive for M=2 stages and n devices of Figure 1.1 the equation for total output noise.

New application of taught theory:

Total output noise: $v_{no}^2 = \sum_{i=1}^{i=M} v_m^2 G_i^2$

Distributed gain: $G_i = \prod_{k=i}^{k=M} g_k$ using M=2 we get:

$$v_{no}^2 = n_1 \frac{K_w}{(I_1/n_1)} \cdot \Delta f + n_1 \frac{K_f}{(A_1/n_1)} \cdot \ln\left(\frac{f_h}{f_l}\right)(Av_1.Av_2)^2 + n_2 \frac{K_w}{(I_2/n_2)} \cdot \Delta f + n_2 \frac{K_f}{(A_2/n_2)} \cdot \ln\left(\frac{f_h}{f_l}\right)(Av_2)^2$$

[Total 4 points]

(ii) Explain why computing with 32 bit precision in analogue is challenging and discuss what the optimum precision for analogue computation is.

Computing with a precision of more than 10 bits in analogue is inefficient because for the same or more precision digital consumes less power and area. There is a fundamental limit as to how much area and power we can spend to reduce the noise due to flicker noise and this sets a hard limit on output SNR at about 80 dB. This makes 32 bit precision in computation virtually impossible.

[Total 4 points]

2.

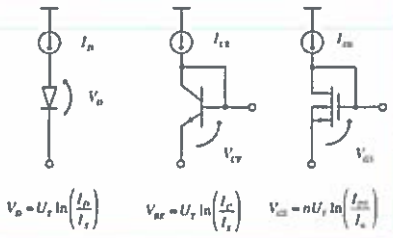
a) This question concerns translinear circuits.

(i) What is a translinear element ?

A translinear element is one in which is transcondctance is linearly proportional to the current flowing through the device. [1]

(ii) Draw three devices which could be used as translinear elements justifying your choices with equations describing their operation.

- The Diode
- The Bipolar Transistor
- The MOS transistor in weak inversion (NB: body effect)



[1 point for each]

[Total 4 points]

b) List the three factors which contribute to non-ideal behaviour in translinear circuits.

1) Area mismatch [1]
2) Finite output resistance [1]
3) Body effect. [1]

[Total 3 points]

c) Figure 2.1 shows a translinear circuit made up of NMOS transistors biased in weak inversion.

(i) Derive I_Z as a function of I_X and I_Y by applying the translinear principle. Show all necessary steps.

Derivation from taught theory

- First loop (M2, M3 Current mirror)

$$I_2 = I_3$$

- Second loop (M2,M1 M4, M5)

$$I_1 \cdot I_2 = \left(\frac{I_4}{2}\right)\cdot\left(\frac{I_5}{2}\right)$$

$$I_1 = (I_Z - I_3) = (I_Z - I_2)$$

$$I_2 = (I_1 + I_Y) = (I_Z - I_2) + I_Y$$

$$I_2 = \frac{(I_Z - I_Y)}{2} \qquad I_1 = \frac{(I_Z + I_Y)}{2}$$

- Final result:

$$\frac{(I_Z - I_Y)}{2}\cdot\frac{(I_Z + I_Y)}{2} = \frac{I_X^2}{4}$$

$$I_Z = \sqrt{I_X^2 + I_Y^2}$$

[4]

(ii) What is the function of the circuit shown in Figure 2.1 ?

Vector sum circuit. [1]

[Total 5 points]

d) Figure 2.2 shows a translinear circuit capable of computing the trigonometric function sin(πy) through the approximation $\frac{y-y^3}{1+y^2}$.

(i) Express the currents I_3 and I_4 in terms of I and I_X.

New Derivation

$$\left[\frac{I-I_X}{2}\right]^2 II_4 = I_3\left[\frac{I+I_X}{2}\right]^2$$

$$\frac{I_4}{I_3} = \left[\frac{I+I_X}{I-I_X}\right]^2 \text{ and } I_3+I_4=I$$

$$I_4 = \frac{I(I+I_X)^2}{(I-I_X)^2+(I+I_X)^2}$$

$$I_3 = \frac{I(I-I_X)^2}{(I-I_X)^2+(I+I_X)^2}$$

[4]

(ii) Express the differntial output current I_2-I_1 and show that when I_X=yI then I_2-$I_1 = I\frac{y\cdot y^3}{1+y^2}$

$$I_2 = \frac{I-I_X}{2} + \frac{I(I+I_X)^2}{(I-I_X)^2+(I+I_X)^2}$$

$$I_1 = \frac{I+I_X}{2} + \frac{I(I-I_X)^2}{(I-I_X)^2+(I+I_X)^2}$$

$$I_2 - I_1 = \frac{I^2I_X - I_X^3}{I^2+I_X^2}$$

$$I_2 - I_1 = I\frac{y-y^3}{1+y^2}$$

[4]

[Total 8 points]

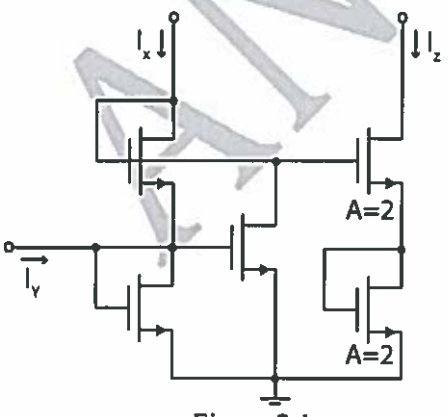


Figure 2.1

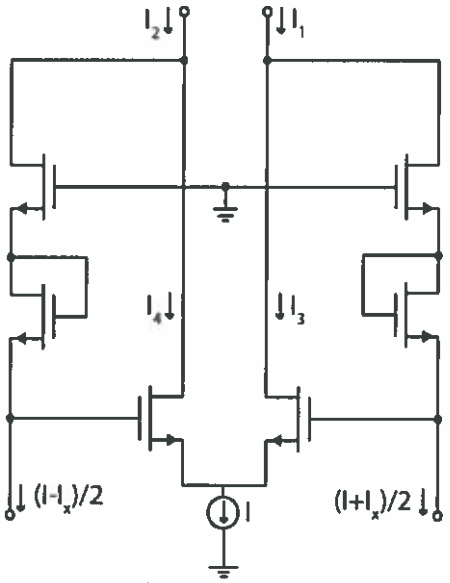


Figure 2.2

3. a) Figure 3.1 shows a block diagram of a current-mode companding integrator, with an input X and an output Y. f() and g() represent non-linear functions which compress and expand the signal such that the input-output relationship of the integrator is linear and given by:

$$Y = \tau \int X \cdot dt$$

Given that the expansive function is defined as $I_{out} = g(V_c) = I_T \tanh(V_c/nU_t)$, derive the function f(x) such that linear integration is achieved. All constants should be grouped to represent a current I_1, with the function f(x) composed of just I_{in}, I_1 and I_T. Hint: use the relationship $tanh\left(\frac{V_c}{nU_t}\right) = I_{out}/I_T$.

New derivation

Requirement for linear integration: $Y = \tau \int X \cdot dt$ i.e $\frac{dY}{dt} = \tau X$

$$\frac{dY}{dt} = \frac{d(g(V_c))}{dV_c} \cdot \frac{dV_c}{dt} = \frac{d(g(V_c))}{dV_c} \cdot \frac{I_c}{C} = \frac{d(g(V_c))}{dV_c} \cdot \frac{f(X)}{C}$$

$\frac{dY}{dt} = \tau X$ thus $\frac{d(g(V_c))}{dV_c} \cdot \frac{f(X)}{C} = \tau X$ so for linear integration: $f(X) = \tau X C \left(\frac{d(g(V_c))}{dV_c}\right)^{-1}$

$$\frac{d(g(V_c)}{dV_c} = \frac{I_T}{nU_t}\sec^2\left(\frac{V_c}{nU_t}\right) = \frac{I_T}{nU_t}\left(1 - \tan^2\left(\frac{V_c}{nU_t}\right)\right)$$

$$tanh\left(\frac{V_c}{nU_t}\right) = I_{out}/I_T$$

$$\frac{d(g(V_c)}{dV_c} = \frac{I_T}{nU_t}\left(1 - \left(\frac{I_{out}}{I_T}\right)^2\right)$$

$$f(x) = \frac{I_{in}\tau C n U_t}{I_T - I_{out}^2/I_T} = I_{in}\frac{I_1 I_T}{I_T^2 - I_{out}^2}$$

[Total 6 points]

b) The transfer function of an oscillator may be defined in state space representation by the following equations:

$$\dot{X}_1 = -\omega_0 X_1 + \omega_0 X_2$$

$$\dot{X}_2 = -2\omega_0 X_1 + \omega_0 X_2 + \omega_0 U$$

$$Y = X_1$$

whereby Y is the output and U is the input and X_1 and X_2 are the states.

(i) By using the mappings below show how these linear equations can be mapped to non-linear log-domain design equations. You may use the following mapping for constant currents, $I_1 = I_2 = I_\omega$ and $I_U = I_O$.

$$X_1 = I_1 \exp\left(\frac{V_1}{nU_t}\right) \qquad X_2 = I_2 \exp\left(\frac{V_2}{nU_t}\right) \qquad U = I_U \exp\left(\frac{V_U}{nU_t}\right)$$

Appliction of taught methodology.
Should apply state space mapping and derive the following KCL equations:

$$C\dot{V}_1 = -I_\omega - I_\omega \exp\left(\frac{V_2 - V_1}{nU_t}\right)$$

$$C\dot{V}_2 = -2I_\omega \exp\left(\frac{V_1 - V_2}{nU_t}\right) + I_\omega + I_0 \exp\left(\frac{V_U - V_2}{nU_t}\right)$$

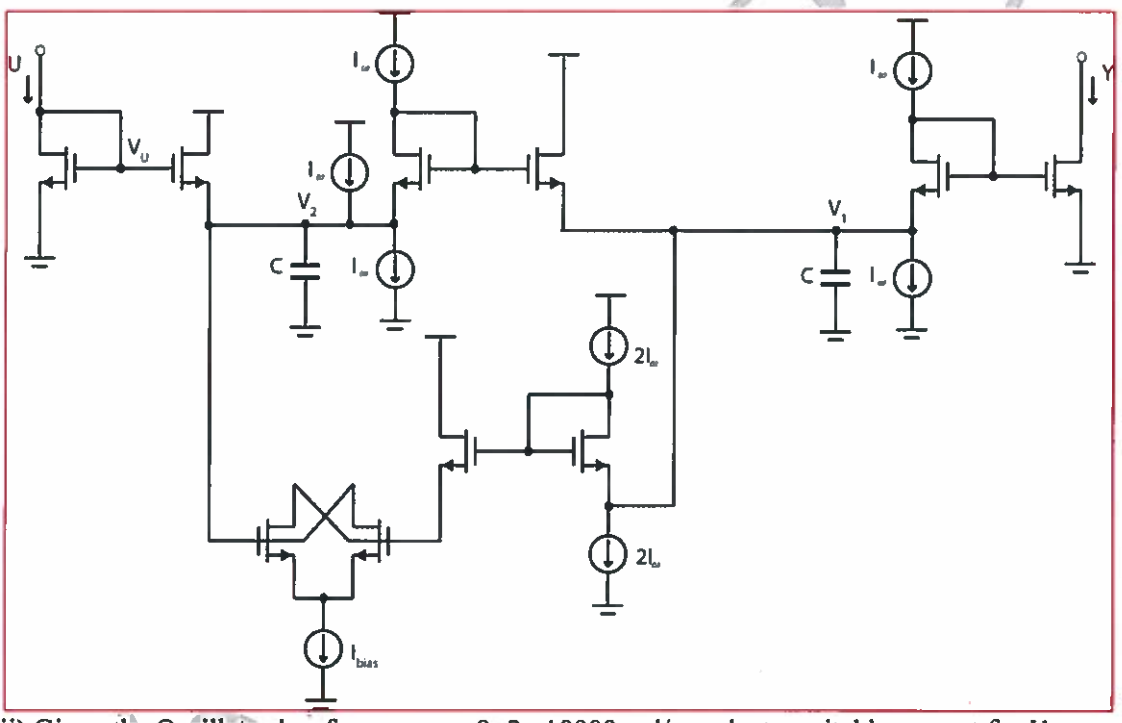
$$Y = I_\omega \exp\left(\frac{V_1}{nU_t}\right)$$

[Total 6 points]

(ii) With these log-domain design equations, sketch a schematic of the final log domain filter using weak inversion MOS transistors.

[Total 6 points]

Drawing of log domain circuit.



ii) Given the Oscillator has frequency, ω0=2π.10000 rad/s , select a suitable current for I1 given that the filter capacitor is C=10pf , n=1.23 and Ut=25mV.

$$I_\omega = C\omega_0 nU_t$$

I1=10px2π.10000x1.23x25m=19.3nA.

[Total 2 points]

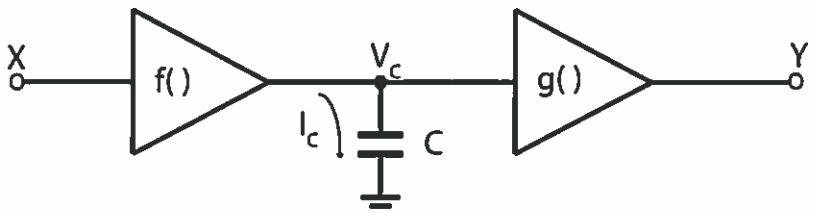


Figure 3.1

4 a) Figure 4.1 shows a conventional second-generation positive current conveyor, CCII+.

i) Explain it's operation principle and describe how impedances at each of its three ports, X, Y, Z, differ from a standard operational amplifier.

[bookwork]

- Current-voltage characteristics
  $V_X=V_Y$, $I_Z=\pm I_X$, $I_Y=0$
  $Z_Y \rightarrow \infty$, $Z_X \rightarrow 0$, $Z_Z \rightarrow \infty$ [2]
- Voltage-follower between Y-input and X-output
- Current-follower between X-input and Z-output [2]

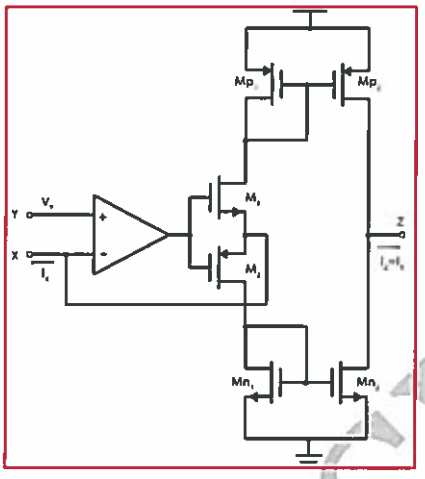
Plus a comparison with Op-amp terminals

[Total 4 points]

ii) Draw the circuit of a CMOS implementation of a bi-directional CCII+.

Application of taught circuits

Schematic:

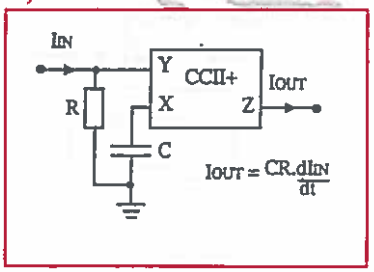


[Total 3 points]

Using current conveyors design circuits which implement:

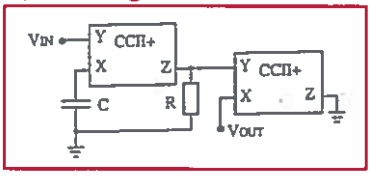
Application of taught circuits

iii) A current mode differentiator



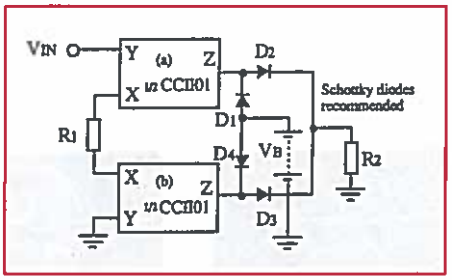
[2]

iv) A voltage mode differentiator



[2]

v) A full wave voltage mode rectifier



[2]

[Total 6 points]

b) Derive the generalized equation which describes output currents from the circuit in Figure 4.2 and explain the function of this circuit.

Derivation from Theory:

This is a current normalizer. [1]

Derivation [4]:

$$I_{ini} = I_0 \exp\frac{V_{di}}{nU_t}$$

$$I_{outi} = I_0 \exp\frac{V_{di} - V_c}{nU_t} = I_{ini} \exp\frac{-V_C}{nU_t}$$

$$\sum_{i=1}^{N} I_{outi} = I_b$$

$$\exp\frac{-V_C}{nU_t} = \frac{I_b}{\sum_{i=1}^{N} I_{ini}}$$

$$I_{outi} = I_b \frac{I_{ini}}{\sum_{i=1}^{N} I_{ini}}$$

[Total 4 points]

c) Draw a circuit than can calculate the correlation of two signals and explain its operation.

[bookwork]

Two transistor current correlator circuit [2]

Equation of operation with description [1]

[Total 3 points]

5.

a) Explain the principle of autozeroing with the aid of diagrams.

[bookwork]

Basic Principle:

- Sample the unwanted quantity (noise and offset)
- Subtract this from the instantaneous value of the contaminated signal.
- The cancellation can occur at the input , or at an intermediate node between the input and output.
- Constant noise (i.e offset) will get subtracted.

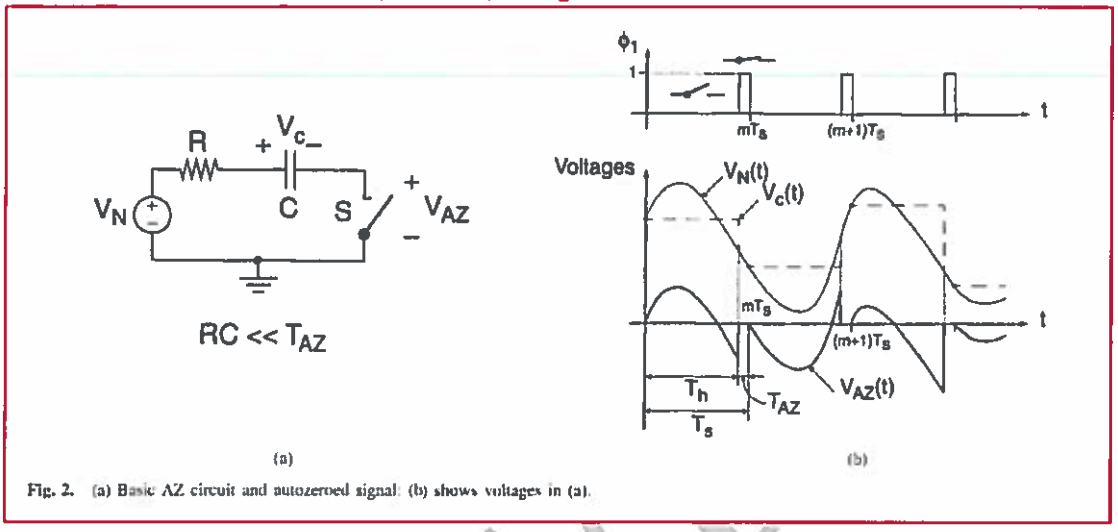


Fig. 2. (a) Basic AZ circuit and autozeroed signal: (b) shows voltages in (a).

[3]

b) Explain how autozeroing affects the noise spectrum of the signal.

Low-frequency random noise (i.e 1/f noise) will be high pass filtered and thus reduced at low frequencies at the expense of increased wide-band noise due to aliasing.

[2]

[Total 5 points]

c) Figure 5.1 shows a switched capacitor amplifier corrlated double sampling amplifier.

(i) Derive the output voltage of this amplifier Vout for both phases Φ1 and Φ2 showing how this removes any offset in the amplifier. You may ignore feedback capacitor C_{dg}.

Derivation from theory:

Φ1: C_1 charges to V_{in}-V_{os}, C_2 charges to V_{os}, V_{out}=V_{os}

Φ2: C_1 charges to -V_{os}, C_2 charges to V_{os}-V_{out}

Charge conservation on node A: Q'_1-Q_1=Q'_2-Q_2

$C_1(V_{in}-V_{os})-C_1(-V_{os})=C_2V_{os}-C_2(V_{os}-V_{out})$

$V_{out}=V_{in}C_1/C_2$ independent of V_{os} !

[Total 4 points]

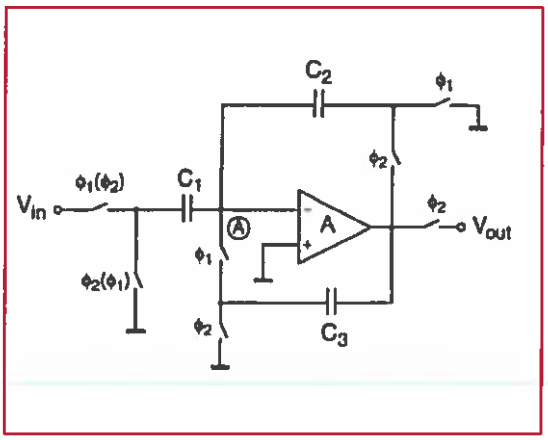
(ii) Explain why this configuration requires an opamp with a high slew rate ?

Output switches from V_{os} to V_{out} requiring the opamp to have high slew rate. [1 point]

(iii) Show how this circuit can be modified reduce the high slew rate requirements deriving the change in output voltage required.

Application of taught Theory:

Circuit with feedback capacitor C3.



[3]

Final change in output voltage, $\Delta V=V_{out}(\Phi 1)-V_{out}(\Phi 2)= (Q_3(\Phi 1)-Q_3(\Phi 2))/C_3=V_A=V_{os}-V_{out}/A$ [1]

[Total 5 points]

d) Derive the output current for the switch current algorithmic cell shown in Figure 5.2 showing how this eliminates any error caused due to the switches.

Derivation from Theory:

Operation

Assuming a charge injection δ

- Period 1: $I_{ds1}-J=\delta 1$
- Period 2: $I_{ds2}-J=-\delta 1+\delta 2$
- Period 3: $I_{ds3}-J=I_{in}+\delta 1-\delta 2+\delta 3$
- Period 4: $I_{ds1}-J=I_{in}+\delta 1-I_{ds3}=+\delta 2-\delta 3$
- Period 5: $I_{ds2}-J=\delta 2-\delta 2+\delta 3=\delta 3$
- Period 6: $I_{ds3}=I_{in}+\delta 3-\delta 3=I_{in}$
- Period 7: $I_{out}=I_{in}$!

[Total 5 points]

6. Figure 6.1 shows a trignonometric circuit whereby all transistors are operating in the weak inversion region of operation with the output currents given by:

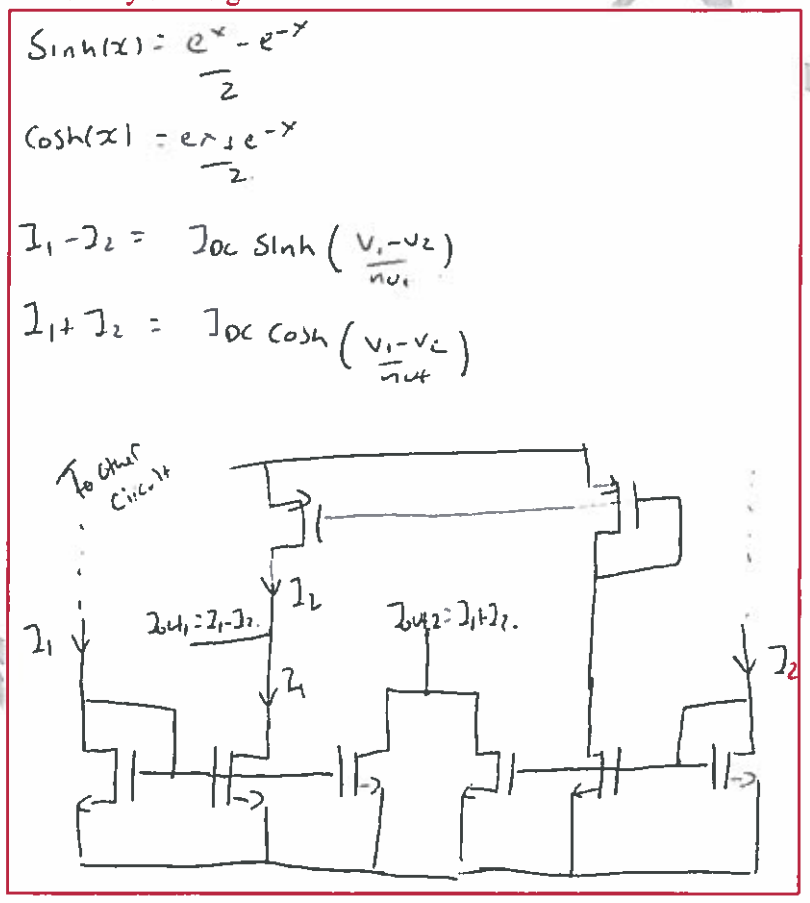
$$I_1 = \frac{I_{DC}}{2} e^{\left(\frac{V_+ - V_-}{nU_t}\right)} \qquad I_2 = \frac{I_{DC}}{2} e^{\left(\frac{-(V_+ - V_-)}{nU_t}\right)}$$

a) Show how the circuit can be transformed to give the following trigonometric functions:

$$I_{out1} = I_{DC} \sinh\left(\frac{V_1 - V_2}{nU_t}\right)$$

$$I_{out2} = I_{DC} \cosh\left(\frac{V_1 - V_2}{nU_t}\right)$$

Application of theory to design new schematic:



[Total 6 points]

b) Figure 4.2 shows a differential pair whereby both transistors M1 and M2 are biased in the weak inversion region of operation. Derive the function for the output current showing how it is trigonometrically related to the input voltage.

$$I_{out} = I_{tail} \tanh\left(\frac{V_{GS1} - V_{GS2}}{2nU_t}\right) \qquad (1)$$

Mathematical derivation:

$$I_1 = I_0 \exp\left(\frac{V_{GS1}}{nU_t}\right)$$

$$I_2 = I_0 \exp\left(\frac{V_{GS2}}{nU_t}\right)$$

$$I_{tail} = I_1 + I_2 = I_0(e^{V_{GS1}/nU_t} + e^{V_{GS2}/nU_t})$$

$$I_{out} = I_1 - I_2 = I_0(e^{V_{GS1}/nU_t} - e^{V_{GS2}/nU_t})$$

$$V_{inD} = V_{GS1} - V_{GS2}$$

$$\frac{I_{out}}{I_{tail}} = \frac{e^{V_{GS1}/nU_t} - e^{V_{GS2}/nU_t}}{e^{V_{GS1}/nU_t} + e^{V_{GS2}/nU_t}} = \frac{e^{V_{inD}/nU_t} - 1}{e^{V_{inD}/nU_t} + 1} = \tanh\left(\frac{V_{inD}}{2nU_t}\right)$$

[Total 6 points]

c) Using the two circuits from parts a and b or otherwise design a circuit which implements the following trigonometric function:

$$I_{out} = I_{bias}\,\mathrm{sech}\frac{V_1 - V_2}{nU_t}$$

whereby I_{bias} is an individually tuned current.

Application of theory to design new schematic:

c) Combine two circuits.

$I_{out1} = I_{0c}\sinh\left(\frac{V_1 - V_2}{nU_t}\right)$

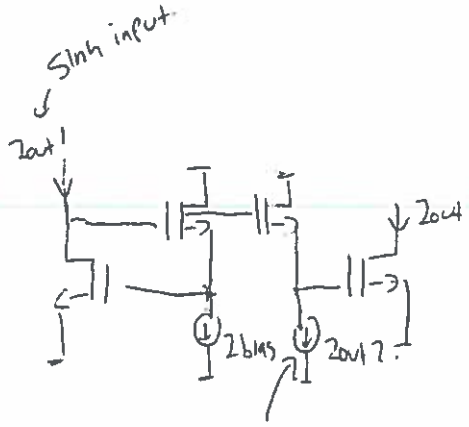
$I_{out2} = I_{0}\tanh\left(\frac{V_1 - V_2}{nU_t}\right) = I_{0}\frac{\sinh(V_1 - V_2/nU_t)}{\cosh(V_1 - V_2/nU_t)}$

$\frac{I_{out1}}{I_{out2}} = \frac{1}{\cosh\left(\frac{V_1 - V_2}{nU_t}\right)} = \mathrm{Sech}\left(\frac{V_1 - V_2}{nU_t}\right)$

multiply by I_{bias}:

translinear cell → $I_{bias}\frac{I_{out1}}{I_{out2}} = I_{bias}\,\mathrm{Sech}\left(\frac{V_1 - V_2}{nU_t}\right)$

$$I_{OUT} = I_{bias}\,\frac{I_{out1}}{I_{out2}} = I_{bias}\,\tanh\left(\frac{v_1 - v_2}{nV_T}\right)$$



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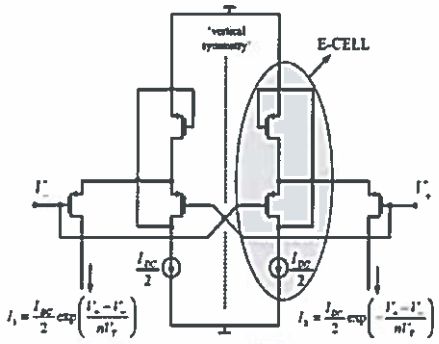

Figure 6.1

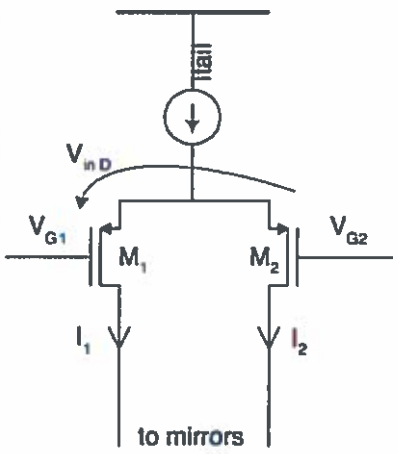

Figure 6.2