E1.4 SOLUTIONS

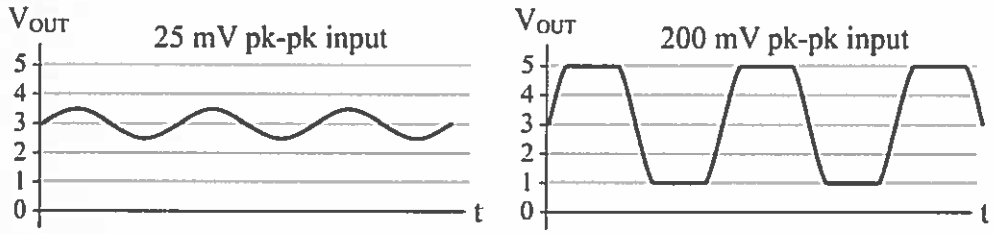
Question 1

a) Assume active mode initially (easier calculation). Assuming zero gate current, $V_{GS} = 0$ and drain current is $I_D = K(-V_t)^2 = 0.5m \times (1.5)^2 = 1.125$ mA. But this would imply $V_{DS} = 3 - 1.125 \times 1.5 = 1.31$ V $< (V_{GS} - V_t) = 1.5$ V, so active assumption was wrong and device is in **TRIODE mode.**

In triode mode we need to solve $(3 - V)/1.5k = 0.5m \times [2V(1.5) - V^2]$, or $3V^2 - 13V + 12 = 0$. Roots are V = 3 or 4/3. Larger root can be rejected, so **V = 4/3 V.** [6]

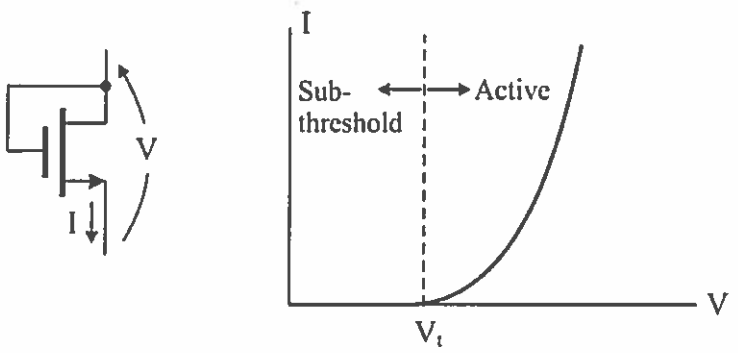
b) The small-signal voltage gain required is the single-ended differential gain of a differential pair, which may be quoted as derivation not requested. The sign is positive since the input and output are on opposite sides, so we have $A_v = v_{out}/v_{in} = +g_m R_C/2$. The collector bias current is 0.2 mA, so $g_m = 0.2m/25m = 8$ mS, and $R_C = 10$ kΩ, so $\mathbf{A_v = +40}$. [4]

The quiescent output voltage is $5 - 0.2m \times 10k = 3$ V, and the output voltage range is from +1 V (when RH transistor carries all the tail current) to +5 V (when LH transistor carries all the tail current). A 25 mV pk-pk input will produce an output amplitude of ~1 V pk-pk, which is well within the output voltage range. However, with a 200 mV pk-pk input the output will be clipped because $200 \text{ mV} \times 40 = 8 \text{ V} > (5 - 1) = 4$ V. [2]



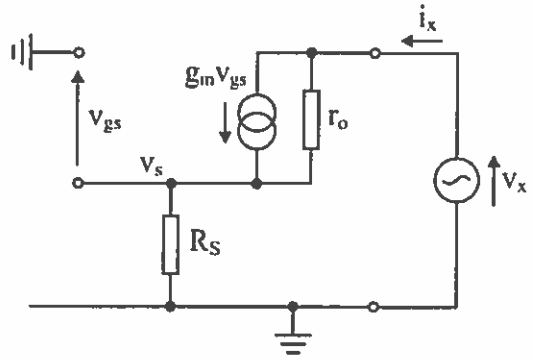
[4]

c) Assuming V and I are as in diagram below, the MOSFET has $V_{DS} = V_{GS} = V$ and consequently is active provide $V > V_t$ (because $V_{DS} = V_{GS}$ implies $V_{DS} > V_{GS} - V_t$). Also, I is just the drain current (since $I_G = 0$), so we have $I = 0$ for $V \le V_t$ and $I = K(V - V_t)^2$ for $V > V_t$.



[6]

d) SSEC:



KCL at output node gives:

$$i_x = g_m v_{gs} + (v_x - v_s)/r_o$$

Also we have $v_{gs} = -v_s$ and $v_s = i_x R_S$

Eliminating v_{gs} and v_s from the first equation, and collecting terms in i_x, gives:

$$i_x[1 + R_S/r_o + g_m R_S] = v_x/r_o$$

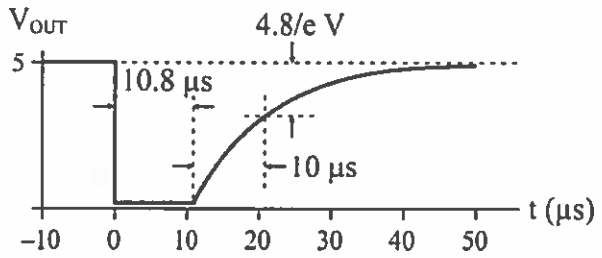
The output resistance is then obtained as: $R_o = v_x/i_x = r_o + R_S + g_m R_S r_o$ [6]

e) For $t < 0$, with zero input voltage, the transistor is off, and the RL network will have reached steady state with $V_L = 0$ and $I_L = 0$. The output voltage will be $V_{OUT} = +5$ V.

When the input goes high, the transistor turns on with $I_B = 4.3/43k = 100$ µA. Since I_L is continuous, we know $I_L = 0$ at t=0+. The max collector current is ~5V/1k = 5 mA, and this is less than $\beta I_B = 10$ mA, so the transistor is saturated with $V_{OUT} \sim 0.2$ V.

While the transistor remains saturated, $V_L = 4.8$ V and the inductor current increases according to $dI_L/dt = 4.8/10m = 480$ V/sec. This will continue until the collector current reaches 10 mA, at which point the transistor will come out of saturation. The current in the 1k resistor is 4.8 mA, so the transistor will come out of saturation when $I_L = 5.2$ mA. This will occur at $t = \mathbf{T = 5.2m/480 = 10.8}$ µs. [4]

With the transistor active, the RL network is fed by a DC current source of 10 mA. The steady state has $V_L = 0$ and $I_L = 10$ mA. Also, the initial inductor current at $t = T$ is $I_L = 5.2$ mA. The trajectory for I_L is therefore $I_L = 10 + (5.2 - 10)\exp(-t'/\tau)$ mA, where $t' = t - T$ and $\tau = L/R = 10$ µs.



The output voltage is

$V_{OUT} = 5 - L dI_L/dt = 5 - 4.8\exp(-t'/\tau)$ V

which is as plotted to the left.

[4]

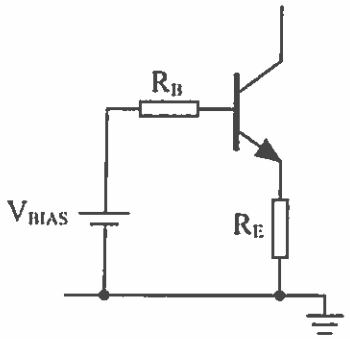
f) For steady oscillation we require a solution to the characteristic equation with $s = j\omega$ where ω is the oscillation frequency. Substituting this form of s into the given equation we obtain:

$$-j(1 + K)\omega^3 R^3 C^3 - 6\omega^2 R^2 C^2 + j5\omega RC + 1 = 0$$

Considering just the real part of this equation, we can see that $\omega = \dfrac{1}{\sqrt{6}RC}$. [4]

Question 2

a) Replacing input resistor network by Thévenin equivalent, bias circuit reduces to:



$V_{BIAS} = 10\times39/(39 + 220) = 1.506$ V

$R_B = 39k//220k = 33.13k$

KVL then gives: $I_ER_E + V_{BE} + I_BR_B = V_{BIAS}$

$\Rightarrow I_E = (V_{BIAS} - V_{BE})/[R_E + R_B/(1 + b)]$

Assuming $V_{BE} = 0.7$ V,

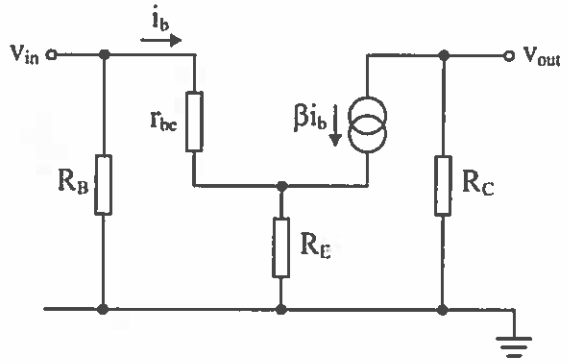
$I_E = (1.506 - 0.7)/(1.2k + 33.1k/201) = 0.591$ mA

$I_C = aI_E = 200\times0.591/201 = \mathbf{0.588\ mA}$

$V_{OUT} = 10 - 0.588\times10 = \mathbf{4.12\ V}$

[6 + 2]

b) SSEC:



KVL on input side:

$$i_br_{be} + (1+\beta)i_bR_E = v_{in}$$

KVL on output side:

$$-\beta i_bR_C = v_{out}$$

$\Rightarrow A_v = v_{out}/v_{in} = -\beta R_C/[r_{be} + (1 + \beta)R_E]$

Using $r_e = r_{be}/(1 + \beta)$ this reduces to

$$A_v = -\alpha R_C/(r_e + R_E)$$

$r_e = V_T/I_E = 42.3\ \Omega$, $r_{be} = V_T/I_B = 8503\ \Omega$

For SSEC : [6]

$A_v = -(200/201)\times10k/(42.3 + 1.2k) = \mathbf{-8.01}$

$R_i = R_B//(v_{in}/i_b) = R_B//[r_{be} + (1 + \beta)R_E] = 33.13k//249.7k = \mathbf{29.25\ k\Omega}$

Ro = **10 kΩ** (by inspection) [6]

c) The in-circuit gain will be reduced by the potential dividers at the input and output. It will therefore be given by:

$$\frac{v_L}{v_S} = \frac{29.25}{29.25+5}\times(-8.01)\times\frac{10}{10+10} = \mathbf{-3.42}$$ [6]

d) The cut-off frequencies are given by $f_c = 1/(2\pi RC)$ where R is the total resistance in the network and C is the capacitance. Rearranging we obtain $C = 1/(2\pi Rf_c)$.

At the input: R = 5k + 29.25k = 34.25k, so for $f_c = 100$ Hz we require **C = 46.5 nF.**

At the output: R = 10k + 10k = 20k, so for $f_c = 100$ Hz we require **C = 79.6 nF.** [4]

Question 3

a) The (active mode) drain current of the upper MOSFET (Q2) is:

$$I_{D2} = K_2[(V_{BIAS} - V_{DD} - V_{t2}]^2 \quad \Rightarrow \quad V_{BIAS} = V_{DD} + V_{t2} \pm \sqrt{(I_{D2}/K_2)}$$

Q2 is p-channel so we need to take the –ve sign which gives $\mathbf{V_{BIAS} = 10 - 1.5 - 1 = 7.5\ V.}$ [4]

The drain current of the lower MOSFET (Q1) is:

$$I_{D1} = K_1(V_{G1} - V_{t1})^2 \quad \Rightarrow \quad V_{G1} = V_{t1} \pm \sqrt{(I_{D1}/K_1)}$$

and this time we take the +ve sign which gives $\mathbf{V_{G1} = 1 + 0.5 = 1.5\ V.}$ [4]

Q1 will remain active provided $V_{DS1} = V_{OUT} \geq V_{GS1} - V_{t1} = 0.5$ V.

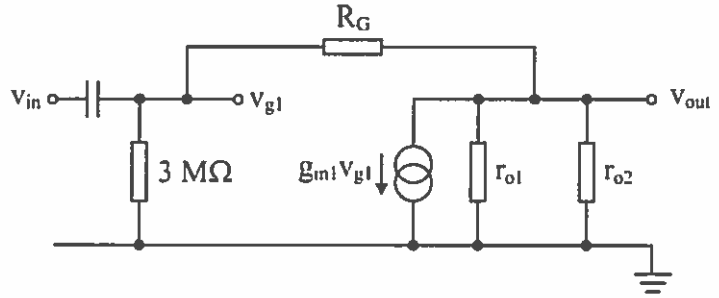
Q2 will remain active provided $V_{DS2} \leq V_{GS2} - V_{t2}$ or $V_{OUT} \leq V_{BIAS} - V_{t2} = 9$ V.

The output voltage range for both active is therefore $\mathbf{0.5\ V \leq V_{OUT} \leq 9\ V.}$

The midpoint of the range is $V_{OUT} = 4.75$ V. For $V_{G1} = 1.5$ V when $V_{OUT} = 4.75$ V we require and R_G such that $[3M/(3M+R_G)] = 1.5/4.75$, or $\mathbf{R_G = [(4.75/1.5) - 1] \times 3M = 6.5\ M\Omega.}$ [6]

NB: we have neglected the small discrepancy between the drain currents due to the current flowing in the bias network.

b) SSEC:



[6]

KCL at the output gives:

$$g_{m1}v_{g1} + v_{out}/r_{o1} + v_{out}/r_{o2} + (v_{out} - v_{g1})/R_G = 0.$$

In the mid-band the input capacitor is effectively short-circuit, so $v_{g1} = v_{in}$ and we can rearrange the above equation to obtain the voltage gain:

$$A_v = -(g_{m1} - 1/R_G)\cdot(r_{o1}//r_{o2}//R_G)$$

With $g_{m1} = 2\sqrt{(K_1 I_D)} = 0.8$ mA/V, $r_{o1} = r_{o2} = V_A/I_D = 250$ kΩ, $R_G = 6.5$ MΩ, $\mathbf{Av = -98.}$

The input resistance due to R_G is $R_G/(1 - A_v) = 6.5M/99 = 65.7$ kΩ. The overall input resistance is therefore $\mathbf{R_i = 3M//65.7k = 64.2\ k\Omega.}$ [6]

c) To obtain the same operating point for Q1, the load resistor value needs to be:

$$(V_{DD} - V_{OUT})/I_D = (10 - 4.75)/0.2m = \mathbf{26.25\ k\Omega}$$

With this value replacing r_{o2} in the gain expression, we obtain $\mathbf{A_v = -18.9.}$ [4]