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IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2006

MSc and EEE PART IV: MEng and ACGI

RADIO FREQUENCY ELECTRONICS

Monday, 8 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Corrected Copy

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : S. Lucyszyn
Second Marker(s) : E. Rodriguez-Villegas

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The Questions

1. An RF signal of 1 mW is input to a power amplifier with an output of 1 W. Design a suitable power amplifier to give the best overall performance using the following transistor stages.

	$P_{OUT\|MAXLIN}$ [dBm]	P_{DC} [mW]	IP_3 [dBm]
Stage 1	25	600	40
Stage 2	30	2000	40
Stage 3	15	60	40

Table 1.1 Transistor Stage Specifications.
(Note that all the transistors have a perfect impedance matching)

[2]

a) From the design, calculate the following at each stage and the overall values for:

i) Power gain [1]

ii) Output power [2]

iii) Basic efficiency [2]

iv) PAE [2]

v) IP_3 [2]

vi) IMD_3 for two-tone power level given in (ii) [2]

vii) Dissipated power [2]

b) From first principles, prove that the 3rd order intermodulation log-power gain slope is three times that of the desired output log-power slope. [2]

c) In linear operation, if the overall input power drops by 3 dB, what happens to the following:

i) Output power [1]

ii) I_3 power [1]

iii) IMD_3 [1]

2.

a) Draw the basic schematic of a 2-stage corporate (also called a binary) power amplifier and illustrate how the couplers can be implemented with:

i) Only 0° power couplers. Name such a coupler. [2]

ii) Only 90° power couplers. Name such a coupler. [2]

iii) Only 180° power couplers. Name such a coupler. [2]

b) Draw a 4-stage corporate power amplifier employing four identical 2 W single-ended amplifiers, each having 6 dB of power gain and 30% PAE. All the power couplers are identical and have an insertion loss of 0.5 dB. Determine the following [2]

i) Output power [1]

ii) Power gain [1]

iii) Total power dissipated in the input couplers [2]

iv) Total power dissipated in the output couplers [2]

v) Output power dissipated [2]

vi) Overall PAE [2]

c) What conclusions can be drawn from the overall PAE calculated in b)(vi), when compared to the PAE for each single-ended amplifier. What practical way can be adopted to improve the overall PAE? [2]

3. For a given filter order n, the element values of the Butterworth lowpass prototype can be calculated using equation (3.1):

$$go = 1.0$$

$$g_i = 2\sin\left(\frac{(2i-1)\pi}{2n}\right) \quad for\ i = 1\ to\ n \qquad (3.1)$$

$$g_{n+1} = 1.0$$

a) Design a 3-pole lowpass *L-C* filter with a cut-off frequency of 2 GHz and terminating impedances of 50 Ω.

[5]

b) Design a 3-pole bandpass *L-C* filter with a passband from 1 to 2 GHz and terminating impedances of 50 Ω.

[5]

c) Show, from first principles, how a shunt connected parallel *R-L-C* tuned circuit can be "synthesized" using a series connected series *R-L-C* tuned circuit having two impedance inverters.

[5]

d) Modify the design in 3b) so that the parallel *L-C* tuned circuit is replaced by a series *L-C* tuned circuit and inductive impedance inverters.

[5]

4.

a) Draw the basic circuit diagram for a 4-stage distributed amplifier (also know as the travelling-wave amplifier). Describe the basic principle of operation and from this state its main advantage over traditional amplifiers.

[5]

b) Given four identical FETs, represented by a simple equivalent circuit model having intrinsic values of C_{gs} = 2 pF, C_{ds} = 1 pF and g_m = 70 mS, calculate the inductance values, cut-off frequencies and theoretical power gain for 50 Ω input and output transmission lines.

[5]

c) Explain how the gain-bandwidth product can be increased. Also, explain why more stages do not necessarily give more power gain.

[5]

d) Explain the practical problem of biasing the transistors when the distributed amplifier is employed in optoelectronics applications.

[5]

5.

a) Draw the block diagram of a simple 2-channel I-Q vector modulator and explain the basic principle of operation. Also, give two examples of applications for this circuit.

[3]

b) Using simple S-parameter analysis, derive equations for all the S-parameters for the simple I-Q vector modulator in 5a). HINT: assume that power couplers are lossless and reciprocal. Also, treat the bi-phase amplitude modulators as simple S-parameter blocks.

[5]

c) Draw the block diagram for a simple bi-phase reflection-type amplitude modulator.

[3]

d) Using simple S-parameter analysis, derive equations for all the S-parameters for the simple bi-phase amplitude modulator in 5c). HINT: assume that power couplers are lossless and reciprocal.

[5]

e) Calculate the power insertion loss for the complete 2-channel I-Q vector modulator having the following conditions:

i) All reflection terminations are short circuits

[2]

ii) The in-phase reflection terminations are short circuits and the quadrature-phase reflection terminations are impedance matched to the coupler

[2]

6.

a) Compare and contrast lumped-element impedance matching over the use of distributed-elements, in terms of frequency performance. How does this affect their role in DC biasing networks?

[4]

b) With lumped-element impedance matching, what terminating impedance conditions are best suited for L-match, π-match and T-match networks.

[4]

c) A 2 GHz narrow-band amplifier has an output impedance of $(5 - j7)\ \Omega$ and must be matched to a system impedance of 50 Ω. Design simple matching circuits to achieve maximum power transfer:

i) With the use of one lumped-element component and one distributed-element component

[4]

ii) With the use of two lumped-element components

[4]

d) With monolithic technology, discuss the difficulties implementing lumped-element and distributed-element components. How can micromachining technologies help to overcome some of the problems with monolithic implementations? How does this affect their role in filter networks?

[4]

RADIO FREQUENCY ELECTRONICS

The Solutions 2006

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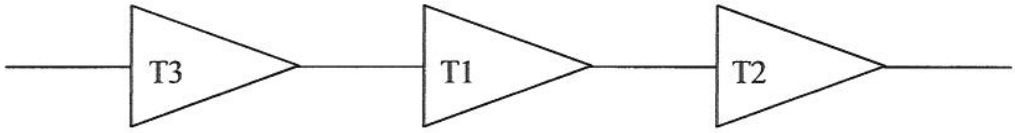
Model answer to Q 1(a): Computed Example



i) Power Gain [dB] 15 10 5

Overall Power Gain = G1+G2+G3 = 30 dB

[2]

ii) $P_{OUT}|_{MAXLIN}$ [dBm] +15 = 31.6 mW +25 = 316 mW +30 = 1000 mW

Final Stage $P_{OUT}|_{MAXLIN}$ = +30 dBm

[2]

iii) Basic Efficiency [%] 52.7 52.7 50
Overall Basic Efficiency = Final Stage $P_{OUT}|_{MAXLIN}$/ Sum(P_{DC}) = 1 W / 2.66 W = 37.59 %

[2]

iv) PAE [%] 51.0 47.4 34
Overall PAE = Overall Basic Efficiency *(1 – 1/(Overall Power Gain)) = 37.56

[2]

v) IP_3 [dBm] 40 39.59 38.7
Final Stage IP_3 = 38.7 dBm

[2]

vi) IMD_3 [dBc] 50 29 17.4
Final Stage IMD_3 = 2*(Final Stage IP_3 - Final Stage $P_{OUT}|_{MAXLIN}$) = 17.4 dBc

[2]

vii) P_{DISS} [mW] 29.4 315.6 1316
Overall P_{DISS} = 1.661 W = 32.2 dBm

[2]

Model answer to Q b(a): Textbook Derivation

$$IMD_3 = \frac{C}{I_3} \quad and \quad IMD_3[dBc] \approx 2 \cdot (IP_3 - C)$$

$$\therefore I_3 \sim \frac{C^3}{IP_3^{\,2}} \quad \therefore \frac{\partial I_3[dBm]}{\partial Pin[dBm]} = 3\frac{\partial C[dBm]}{\partial Pin[dBm]} - 2\frac{\partial IP_3[dBm]}{\partial Pin[dBm]} \quad where, \frac{\partial IP_3[dBm]}{\partial Pin[dBm]} = 0$$

In other words, the third – order intermodulation log power gain slope is three times that of the desired output log power gain slope. Therefore, IMD_3 improves rapidly as input power decreases.

[3]

Model answer to Q 1(c): Computed Example

If the input power drops by 3 dB:

i) P_{OUT} drops by 3 dB

[1]

ii) I_3 drops by 9 dB

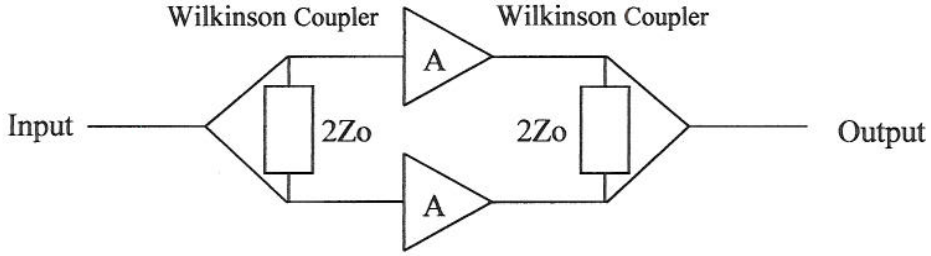
[1]

iii) IMD_3 increases by 6 dB

[1]

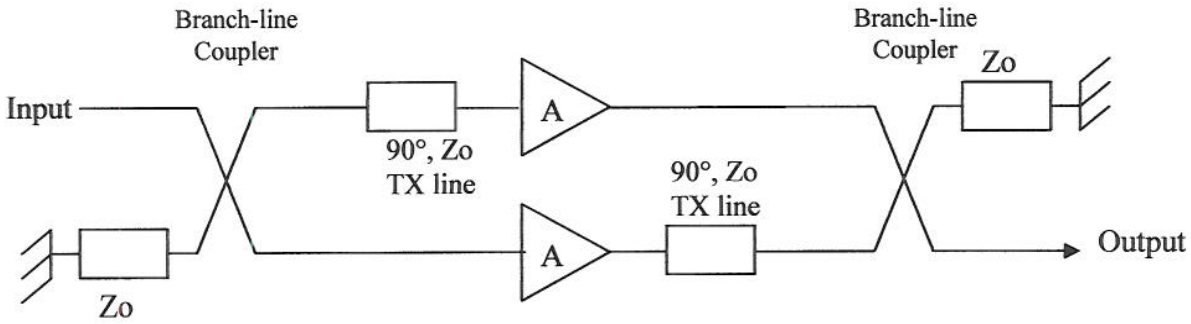
Model answer to Q 2(a): Extension of Bookwork

i) Only 0° power couplers. This can be implemented with a Wilkinson coupler.



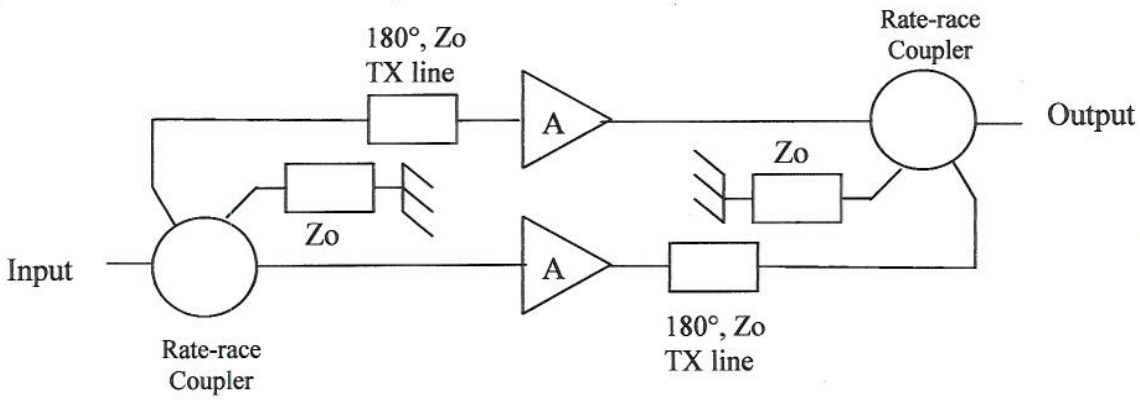
[2]

ii) Only 90° power couplers. This can be implemented with a branch-line coupler having an addition 90° length of transmission line on its direct port.



[2]

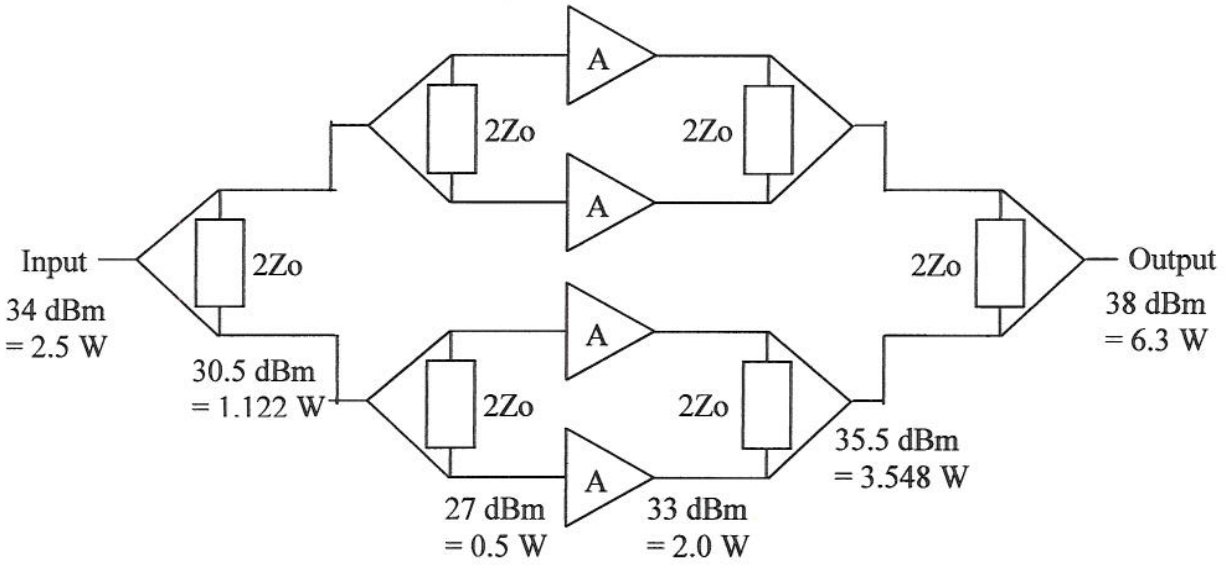
iii) Only 180° power couplers. This can be implemented with a rat-race coupler having an addition 180° length of transmission line on its sum port.



[2]

Model answer to Q 2(b): Computed Example

The 4-stage corporate power amplifier is shown below.



[2]

i) Output power = 6.3 W = 38 dBm [1]

ii) Power gain = 6.3/2.5 = 2.52 = 4 dB [1]

iii) Total power dissipated in the input couplers = (0.256 + 2*0.122) = 0.5 W [2]

iv) Total power dissipated in the output couplers = (2*0.452 + 0.796) = 1.7 W [2]

v) Output power dissipated = 0.5 + 4*(5 + 0.5 – 2) + 1.7 = 16.2 W [2]

vi) Overall PAE = (6.3 – 2.5)/20 = 19 % [2]

Model answer to Q 2(c): Extension of Bookwork

The drop in PAE from 30 % for the individual single-ended amplifiers to down to 19% for the overall PAE shows that the losses in the power couplers play an important role. The output couplers dissipate most heat and so the loss of the output couplers has to be reduced more than for the input couplers.

[2]

Model answer to Q 3(a): Computed example

For a 3-pole Butterworth lowpass prototype the normalised elements are:

$g_0 = 1;\ g_1 = L_{n1} = 1;\ g_2 = C_{n2} = 2;\ g_3 = L_{n3} = 1;\ g_4 = 1$

Low-pass de-normalising:

Series inductor:	Shunt Capacitor:
$Ls = \frac{LnR_L}{\omega_c}$	$C_P = \frac{Cn}{\omega_c R_L}$

with fc = 2 GHz and R_L = 50 Ω:
Zs = 50 Ω; L_1 = 3.979 nH; C_2 = 3.183 pF; L_3 = 3.979 nH; Z_L = 50 Ω

[5]

Model answer to Q 3(b): Computed example
For a 3-pole Butterworth lowpass prototype the normalised elements are:

$g_0 = 1; g_1 = L_{n1} = 1; g_2 = C_{n2} = 2; g_3 = L_{n3} = 1; g_4 = 1$

Band-pass de-normalising:

Series-connected series-tuned circuit:		Shunt-connected parallel-tuned circuit:	
$Ls = \frac{Ln\, R_L}{\omega_p}$	$Cs = \frac{\omega_p}{\omega_o^2 Ln\, R_L}$	$C_P = \frac{Cn}{\omega_p R_L}$	$L_P = \frac{\omega_p R_L}{\omega_o^2 Cn}$

with f_1 = 1 GHz, f_2 = 2 GHz , and R_L = 50 Ω:

$\omega_p = 2*\pi*(f_2 - f_1) = 6.283 \times 10^9$ rad/s
$\omega_o = 2*\pi*\sqrt{(f_2 * f_1)} = 8.886 \times 10^9$ rad/s

Zs = 50 Ω;
L_{s1} = 7.958 nH; C_{s1} = 1.592 pF;
C_{p2} = 6.366 pF; L_{p2} = 1.958 nH
L_{s3} = 7.958 nH; C_{s3} = 1.592 pF
Z_L = 50 Ω

[5]

Model answer to Q 3(c): Extension of Bookwork

A shunt *R-L-C* circuit has the following admittance:

$$Y_S = G_p + j\omega C_p + \frac{1}{j\omega L_p}$$

This can be converted into a series *R-L-C* tuned circuit by using K-inverters. The corresponding impedance will be:

$$Z_S = R_S + j\omega L_S + \frac{1}{j\omega C_S} \equiv K^2 Y_P$$

Using discrete inductance values to realise an impedance inverter with a –L/+L/–L π-network:

$$K = \omega L$$

$$Z_S = G_P(\omega L)^2 + j\omega C_P(\omega L)^2 + \frac{(\omega L)^2}{j\omega L_P}$$

$$\therefore R_S = G_P(\omega L)^2 \quad ; \quad L_S = C_P(\omega L)^2 \quad ; \quad C_S = \frac{L_P}{(\omega L)^2}$$

For convenience, we can choose to set $(\omega L)^2 = 1x10^{+3}$ and, therefore, it can be easily seen that the series inductance value in *nH* will be equal to the parallel capacitance value in *pF*. Likewise, the series capacitance value in *pF* will be equal to the parallel inductance value in *nH*. Alternatively, with $\omega_p L = R_L$, $L_{s1} = L_{s2} = L_{s3}$ and $C_{s1} = C_{s2} = C_{s3}$.

[5]

Model answer to Q 3(d): Computed example

For convenience, we can choose to set $(\omega L)^2 = 1x10^{+3}$. Therefore:

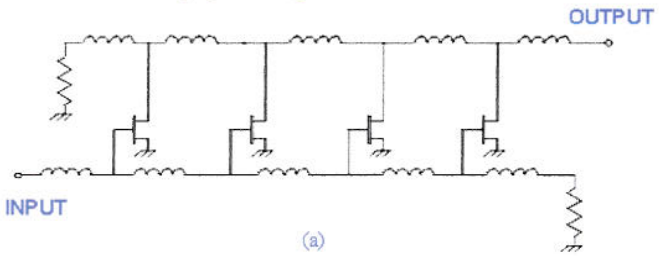
The inductive impedance inverter has $(\omega_o L)^2 = 1x10^{+3}$ *and* $\therefore L = 3.559\ nH$

Z_s = 50 Ω;
L_{s1} = 7.958 nH → (7.958 nH – 3.559 nH) = 4.399 nH;
C_{s1} = 1.592 pF;
$L_{p\_K\text{-}inverter}$ = 3.559 nH
C_{p2} = 6.366 pF → L_{s2} = (6.366 nH – 3.559 nH) = 2.807 nH;
L_{p2} = 1.958 nH → C_{s2} = 1.958 pF
$L_{p\_K\text{-}inverter}$ = 3.559 nH
L_{s3} = 7.958 nH → (7.958 nH – 3.559 nH) = 4.399 nH;
C_{s3} = 1.592 pF
Z_L = 50 Ω

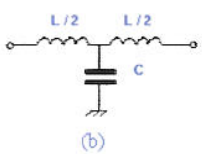
[5]

Model answer to Q 4(a): Bookwork

The distributed amplifier: (a) circuit diagram and (b) a single section of constant-K ladder



$$Z_o = \sqrt{\frac{L}{C}} \qquad f_c = \frac{1}{\pi\sqrt{LC}} \qquad G = \frac{n^2 g_m{}^2 Z_0{}^2}{4}$$



The artificial gate transmission line absorbs Cgs, while the drain line absorbs Cds. As a result, there should be no resonances and, therefore, this is ideal for ultra-wideband applications.

[5]

Model answer to Q 4(b): Computed example

$$Zo = \sqrt{\frac{Lg}{Cgs}} \quad \therefore Lg = 5nH \quad \therefore fcg = \frac{1}{\pi\sqrt{LgCgs}} = 3.183GHz$$

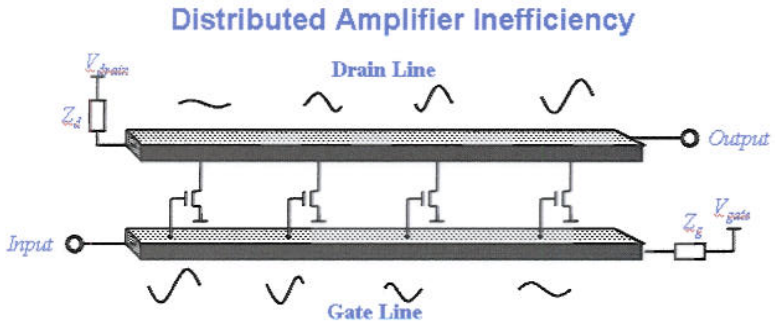
$$Zo = \sqrt{\frac{Ld}{Cds}} \quad \therefore Ld = 2.5nH \quad \therefore fcd = \frac{1}{\pi\sqrt{LdCds}} = 6.366GHz$$

$$Power\ Gain = \left(\frac{4x70x10^{-3}x50}{2}\right)^2 = 7^2 = 49 = 16.9dB$$

[5]

Model answer to Q 4(c): Bookwork

The bandwidth can be increased by employing physically smaller transistors. As a result, the values of Cgs and Lg will be reduced and so the associated gate-line cut-off frequency will increase. However, reducing the size of the transistor will reduce the transconductance and, thus, the power gain. Therefore, the power gain can be increased, in principle, by introducing more transistor stages.



- Power flow in both directions
- Unequal voltages along the drain line
- Imperfect termination
- Losses in gate and drain line

When you have more stages the losses in the gate line attenuate the signal so much as it passes down the line that the associated amplifiers have difficulty amplifying it. As a result, there is little to be gained. Therefore, after about 4 stages, there if diminishing returns on having more stages.

[5]

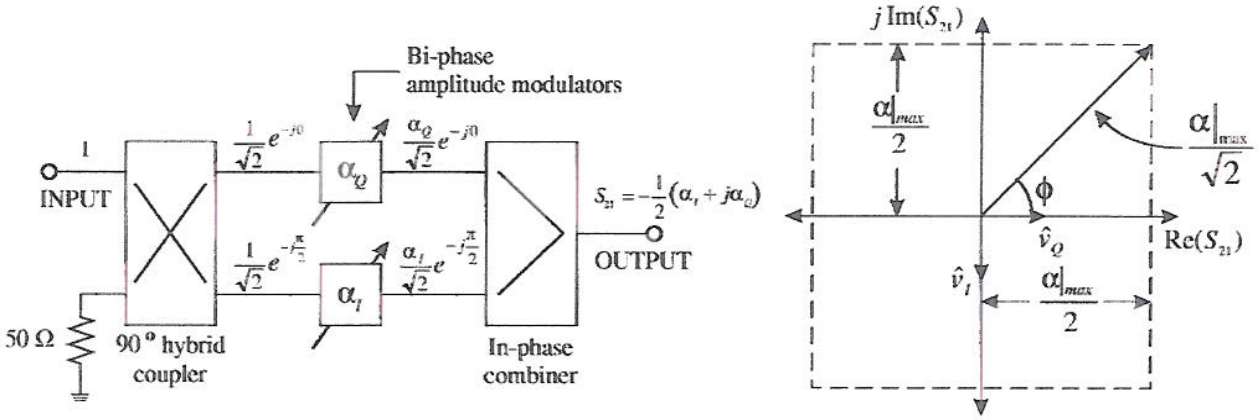
Model answer to Q 4(d): Bookwork

Optoelectronic applications require amplifiers to operate from DC up to the cut-off frequency. However, practical biasing circuits may suffer from the effects of parasitic components. These will cause resonances and, as a result, gain ripples in the amplifiers frequency response.

[5]

Model answer to Q 5(a): Presented in Lecture

The basic 2-channel I-Q vector modulator is shown below. The input signal is split into 2 quadrature channels, using a quadrature power coupler. Each signals in each channel than then be modulated by independent bi-phase amplitude modulators. The two resulting signals are then power combined using an in-phase power combiner.



This circuit can be used as direct-carrier digital modulators and also found in phase array antenna applications, where each radiating element has its own vector control.

[3]

Model answer to Q 5(b): Extension of lecture presentation

The following superscript notations L, I, Q, W represent the quadrature power coupler, In-phase modulator, quadrature phase modulator and in-phase power coupler, respectively.

$$S_{21} = S_{21}^{L} S_{21}^{I} S_{12}^{W} + S_{41}^{L} S_{21}^{Q} S_{13}^{W}$$

$$S_{21}^{L} = S_{12}^{L} = \frac{1}{\sqrt{2}} \quad and \quad S_{12}^{W} = S_{41}^{L} = S_{14}^{L} = S_{13}^{W} = \frac{-j}{\sqrt{2}}$$

$$\therefore S_{21} = \frac{-1}{2}\left(S_{21}^{Q} + jS_{21}^{I}\right) = S_{12}$$

$$S_{11} = S_{21}^{L} S_{11}^{I} S_{12}^{L} + S_{41}^{L} S_{11}^{Q} S_{14}^{L}$$

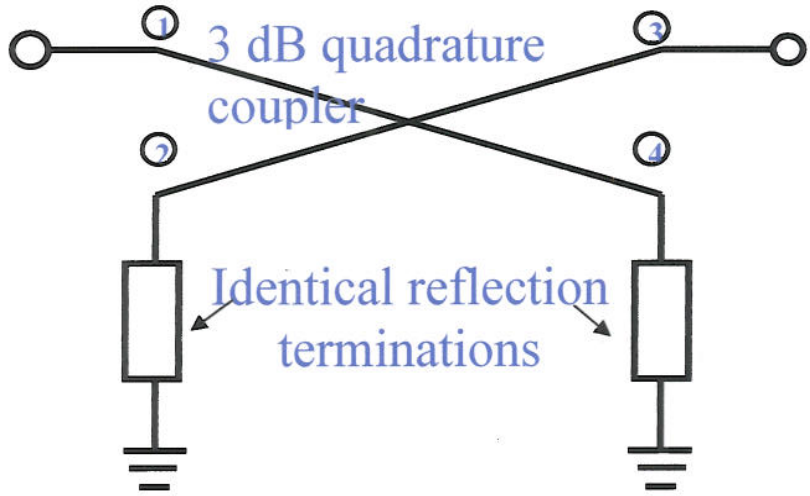
$$\therefore S_{11} = \frac{1}{2}\left(S_{11}^{I} - S_{11}^{Q}\right)$$

$$S_{22} = S_{21}^{W} S_{22}^{I} S_{12}^{W} + S_{31}^{W} S_{22}^{Q} S_{13}^{W}$$

$$\therefore S_{11} = \frac{-1}{2}\left(S_{22}^{I} + S_{22}^{Q}\right)$$

[5]

Model answer to Q 5(c): Extension of lecture presentation



[3]

Model answer to Q 5(d): Extension of lecture presentation

The following superscript notations C represent the quadrature power coupler and the subscript T represents the reflection termination.

$$S_{21} = S_{21}^{C}\rho_T S_{32}^{C} + S_{41}^{C}\rho_T S_{34}^{C}$$

$$S_{21}^{C} = S_{12}^{C} = S_{34}^{C} = \frac{1}{\sqrt{2}} \quad and \quad S_{32}^{C} = S_{41}^{C} = S_{14}^{C} = \frac{-j}{\sqrt{2}}$$

$$\therefore S_{21} = -j\rho_T = S_{12}$$

$$S_{11} = S_{21}^{C}\rho_T S_{12}^{C} + S_{41}^{C}\rho_T S_{14}^{C}$$

$$\therefore S_{11} = 0 = S_{22}$$

[5]

Model answer to Q 5(e): Computed example

i) All reflection terminations are short circuits

$$\rho_T^{I} = \rho_T^{Q} = -1$$

$$\therefore S_{21}^{I} = S_{21}^{Q} = +j$$

$$S_{21} = \frac{-j}{2}(+j-1) \quad \therefore |S_{21}|^2 = \frac{1}{2}$$

$$\therefore Power\ Insertion\ Loss = -3dB$$

[2]

ii) The in-phase reflection terminations are a short circuit and the quadrature-phase reflection terminations are impedance matched to the coupler.

$$\rho_T^I = -1 \quad \rho_T^Q = 0$$
$$\therefore S_{21}^I = +j \quad S_{21}^Q = 0$$

$$S_{21} = \frac{1}{2} \quad \therefore |S_{21}|^2 = \frac{1}{4}$$
$$\therefore \textit{Power Insertion Loss} = -6dB$$

[2]

Model answer to Q 6(a): Bookwork

Lumped-element components are attractive because of their small size and their smooth frequency characteristic in their normal operating frequency range. For this reason they are used extensively in the RF electronics industry. However, as frequency increases they exhibit resonances, which make them unusable as frequency approaches the first self-resonant frequency. In contrast, distributed-element transmission lines can be used at high frequencies, but are not desirable at low frequencies. This is because their role depends on their electrical length, which results in a physical length that is inversely proportional to frequency. Therefore, as frequency decreases they can become prohibitively long.

Lumped-element components are used to implement a low-pass filter for DC biasing networks. Unfortunately, due to undesirable resonances within the components, it is important to make sure that there is sufficient out-of-band isolation above the filter's cut-off frequency, to avoid the RF signal path "seeing" the power supply. At higher frequencies, quarter-wave transformers are employed in biasing networks, with the use of distributed-element lines.

[4]

Model answer to Q 6(b): Bookwork

L-Match – Most useful with one low impedance and one high impedance terminations,
$R_{MIN} < R_{INTERMEDIATE} < R_{MAX}$

π-Match – Most useful with both high impedance terminations (e.g. low frequency valves)
$R_{INTERMEDIATE} < R_{MIN}$

T-Match – Most useful with both low impedance terminations (e.g. transistors)
$R_{MAX} < R_{INTERMEDIATE}$

[4]

Model answer to Q 6(c): Computed example

(i) An inductor is connected in series with the output of the transistor. If it has an inductance of L = +7/(2πfo) = 0.557 nH then it will resonate-out the reactive component of the transistor's output impedance. All that is needed now is a quarter-wavelength impedance transformer, with a characteristic impedance of √(5*50) = 15.81 Ω, to be inserted in series with the inductor.

[4]

(ii) An inductor is connected in series with the output of the transistor. If it has an inductance of L = +7/(2πfo) = 0.557 nH then it will resonate-out the reactive component of the transistor's output impedance. Now an L-network is cascaded with the inductor.

$$Loaded\ Q-factor, Q_L = \sqrt{\frac{Zo}{R_{OUT}} - 1} = 3$$

$$Q_S = \frac{|X_S|}{R_{OUT}} \equiv Q_L \quad \therefore L_S = \frac{3x5}{2x\pi x2x10^9} = 1.194nH$$

$$Q_P = \frac{R_G}{|X_P|} \equiv Q_L \quad \therefore C_P = \frac{3}{50x2x\pi x2x10^9} = 4.775pF$$

In order to reduce the component count, L_S is combined with L to give a combined inductance of 1.751 nH.

[4]

Model answer to Q 6(d): Bookwork

With both lumped-element and distributed-element components, monolithic technology has problems with the conductor dimensions being very small. As a result of the limited cross-sectional areas, these components exhibit high current densities and poor unloaded Q-factors. Therefore, they are not suitable for implementing low loss or high selectivity filters. In addition, with lumped-element components, their values are limited because of unwanted shunt capacitive parasitics that result in low self-resonant frequencies. Also, their physical structures begin to exhibit distributed-element characteristics at higher frequencies.

Micromachining technology allows lumped-element and distributed-element components to be realised without the use of dielectrics. As a result, they will not suffer from dielectric losses. Moreover, without a dielectric, their size increases and, thus, it may be possible to reduce the current densities within the conductors. This can significantly increase the Q-factors of the components and, thus, make them more attractive for realising low loss and high selectivity filters.

[4]