EE4-17
EE9-AO4

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2015

MSc and EEE PART IV: MEng and ACGI

Corrected Copy

# HIGH PERFORMANCE ANALOGUE ELECTRONICS

Tuesday, 12 May 10:00 am

Time allowed: 3:00 hours

correction 11:05
Q2 (f).

**There are FOUR questions on this paper.**

**Answer ALL questions.**

*All questions carry equal marks*

**Any special instructions for invigilators and information for candidates are on page 1.**

Examiners responsible First Marker(s) : E. Rodriguez-Villegas
Second Marker(s) : P. Georgiou

## The Questions

1. (a) Explain the function of the mixer in the superheterodyne receiver.

[6]

(b) Explain the reason to downconvert the RF signal to an intermediate frequency band instead of directly using just an antenna and a bandpass filter.

[6]

(c) What would be the advantages and disadvantages of mixing your RF signal with a square wave instead of a purely sinusoidal signal? If you were to use a square wave signal what circuit would you place after the mixer to improve the performance? Very briefly explain why.

[4]

(d) Give the name of the circuit in Figure 1 if the capacitor and inductor were not present. Explain the functionality of the inductor and capacitor.

[4]

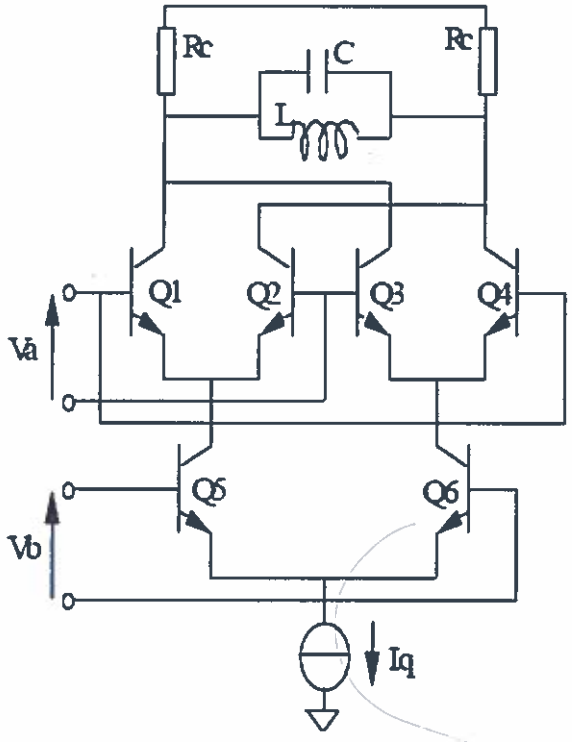


**Figure 1**

2. (a) For the MOS transistor in Figure 2(a) what is the maximum $V_{out}$ voltage that would keep the device operating in the strong inversion triode region considering a minimum input signal $V_{in}(min)$? (Note: Give an equation as a function of the threshold voltage. It is assumed the input signal always remains higher than the threshold voltage).

[3]

(b) For the circuit in Figure 2(b), in which region would you operate the different transistors if you wanted to use it as a transconductor? Briefly explain why.

[3]

(c) Briefly explain an advantage and a disadvantage of the circuit in Figure 2(c), with respect to the circuit in Figure 2(b), if they were to be used as transconductors.

[3]

(d) Find an expression for the output current $I_{out}$ in Figure 2(c) (assuming the transistors are biased in the region you choose in (c)). What is the function of the amplifier N2?

[5]

(e) What is the advantage of using configuration (c) instead of (d)?

[2]

(f) Indicate where the positive and negative inputs of the amplifier are in Figure 2(c). Briefly explain why.

[2]

(g) How would the circuit in Figure 2(c) need to be modified in order to still work as a linear transconductor if both transistors were n-type? Draw a schematic.

[2]

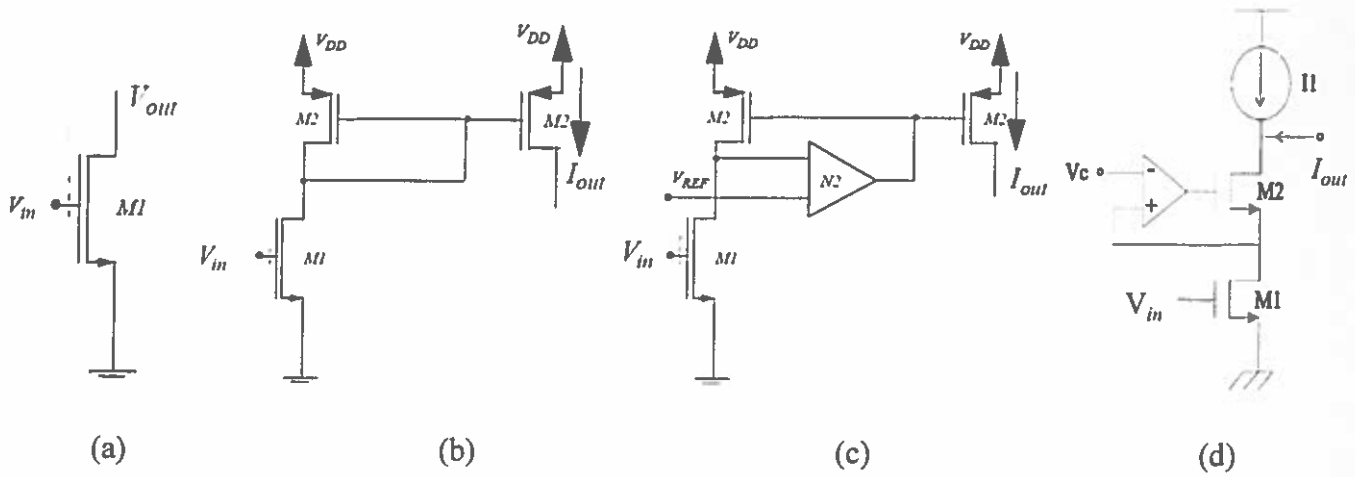


**Figure 2**

3. (a) Draw the schematic of a differential pair transconductor with n-channel MOS transistors.

[4]

(b) The current for an n-channel MOS transistor biased in the weak inversion saturation region with its source and bulk grounded and its drain voltage $V_{DS}>4U_T$ is approximately given by:

$$I_D = I_s \exp\left(\frac{V_{GS}}{\eta U_T}\right)$$

Find an expression for the output current in a differential pair designed with MOS devices in the weak inversion saturation region as a function of the differential input voltage, $\eta$, $U_T$ and the bias current. Find also an expression for the same block implemented with bipolar transistors instead. What is the difference between the two equations? Why would you opt for weak inverted MOS devices instead of bipolar to design the differential pair?

[5]

(c) If noise is an issue, but not area, how would you improve the previous design?
(Hint: You can use more transistors. Just explain the concept. No need to derive equations).

[4]

(d) After simulating the previous circuit you notice that something is not working as expected. When checking the two input transistor's (M1 and M2) operating points, you see the following (Note: the threshold voltage is 0.5V):

M1: $V_{GS}$=0.7V, $V_{DS}$=0V, $V_{BS}$=0V
M2: $V_{GS}$=0.45V, $V_{DS}$=1V, $V_{BS}$=0V

Are those data giving you any hint of something that could be causing the circuit not to work as expected?

[2]

(e) How would you create a mixer just using differential pairs? Draw the schematic.

[5]

4. (a) Name and give expressions for all the noise sources in a MOS transistor.

[4]

(b) Draw the small signal equivalent noise model for a MOS transistor.

[4]

(c) Derive the expression for the equivalent noise at the gate of a MOS transistor.

[4]

(d) For the circuit in Figure 4 draw a low frequency small signal equivalent model including all the noise sources and giving expressions for them.

[2]

(e) For the circuit in Figure 4 calculate the input-referred Flicker noise and also the input referred thermal noise. (Note: You can express your results in terms of power spectral density).

[2]

(f) For the circuit in Figure 4 calculate the total output noise in terms of power spectral density.

[2]

(g) As a designer briefly describe which strategy you would follow to improve the noise performance of the circuit in Figure 4.

[2]

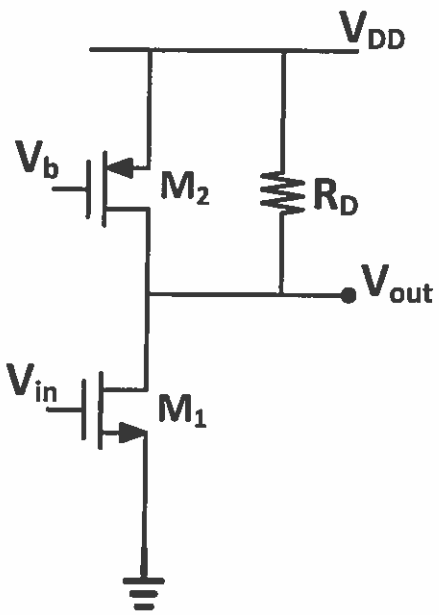


**Figure 4**