UNIVERSITY OF LONDON
IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2003

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

*This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute*

# PAPER C112

# HARDWARE

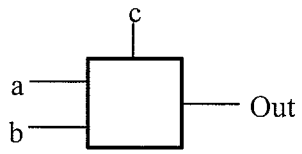
Tuesday 29 April 2003, 16:00
Duration: 90 minutes
(Reading time 5 minutes)

*Answer THREE questions*

Paper contains 4 questions
Calculators required

1. Multiplexers

a. Use AND, OR and INVERTOR gates to design a two input multiplexer labelled as shown in the block diagram below, with the functionality described by the table.




| c | Out |
|---|---|
| 0 | a |
| 1 | b |

b. Draw the complete truth table for the circuit of part a.

c. Using only three multiplexers of the type defined in part a, design a four input multiplexer with four data inputs a,b,c,d and two control inputs c0 and c1 with the functionality defined in the following table:

| C1 | C0 | Out |
|---|---|---|
| 0 | 0 | a |
| 0 | 1 | b |
| 1 | 0 | c |
| 1 | 1 | d |

d. Briefly describe how some four-to-one multiplexers, as defined in part c, could be used to build a shifter for a simple 8 bit central processor. The functionality of the shifter is as defined by the table below.

| C1 | C0 | Action |
|---|---|---|
| 0 | 0 | No Shift |
| 0 | 1 | Shift right with carry |
| 1 | 0 | Shift left (arithmetic) (bn <- bn-1, b0 <- 0) |
| 1 | 1 | Rotate right (bn-1 <- bn, b7 <- b0) |

e. Show how one multiplexer, as defined in part a, could be connected up to act as an AND gate.

*The five parts carry, respectively, 20%, 15%, 15%, 30%, 20% of the marks.*

2. Sequential Circuit Design

A counter is to work in two modes determined by a single bit input as follows:
When the input is 1 the counter outputs 0, 3, 4, 0, 3, 4, 0, 3, 4 etc.
When the input is 0 the counter outputs 0, 2, 1, 3, 0, 2, 1, 3, 0, etc.

a. Draw the transition diagram of a finite state machine that corresponds to the specification.

b. Compile a state transition table in the following format for an implementation of this circuit using three flip flops:

| | This State | | | | Next State | | | |
|---|---|---|---|---|---|---|---|---|
| Input | Name | Q2 | Q1 | Q0 | Name | D2 | D1 | D0 |
| 0 | 0 | | | | | | | |
| 0 | 1 | | | | | | | |
| 0 | 2 | | | | | | | |
| 0 | 3 | | | | | | | |
| 0 | 4 | | | | | | | |
| 0 | | | | | | | | |
| 0 | | | | | | | | |
| 0 | | | | | | | | |
| 1 | | | | | | | | |
| 1 | | | | | | | | |
| 1 | | | | | | | | |
| 1 | | | | | | | | |
| 1 | | | | | | | | |
| 1 | | | | | | | | |
| 1 | | | | | | | | |
| 1 | | | | | | | | |

c. Draw Karnaugh maps for D0 D1 and D2, determine the minimum form of the equations for D0 D1 and D2.

d. The output will be displayed on a seven segment display. The middle segment will be illuminated when the digits 2,3 and 4 are displayed. Write down the canonical minterm equation for the output O that will provide a logic 1 when this segment is to be illuminated. Use a Karnaugh map to find a minimum form of this equation.

*The four parts carry equal marks.*

3. Binary Coded Decimal Arithmetic

Binary coded decimal digits are commonly used in calculators. Four bits are used to define a digit in the following manner:

| Digit | b3 | b2 | b1 | b0 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |

The rest of the bit combinations (1010, 1011, 1100, 1101, 1110, 1111) are not used and are invalid BCD digit combinations.

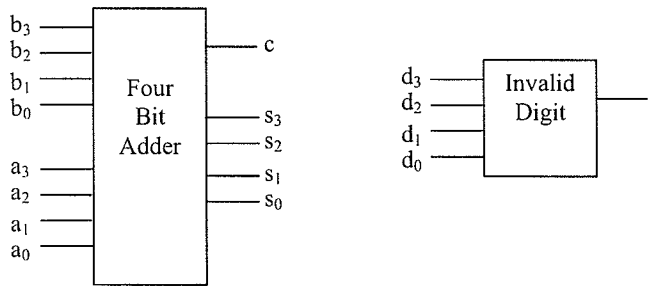
A circuit for adding BCD digits with carry is to be designed.

a. Draw a Karnaugh map of a circuit which has four inputs (b3,b2,b1,b0) and one output which is 1 only if the four bit number input is not a valid BCD digit. Write down the Boolean equation of the minimum form of the circuit.

b. Suppose a full adder is used to add two BCD digits as if they were four bit binary numbers. If the result is a valid BCD digit and the carry is zero then the result is correct. However if the carry is 1 and the result is a valid BCD digit, it is not the correct digit. Write down all the possible combination in which this will happen, and suggest how the result could be corrected by adding a four bit number to the result.

c. If the result is not a valid BCD digit we again must make a correction. Find two examples where this would happen, and determine what number you need to add to the result to make it correct.

d. Draw the complete BCD adder using two four bit binary adders, the circuit you designed in Part a (drawn as a block diagram as shown below), and any other individual gates you require. You can assume that only valid BCD digits are used as input.




*The four parts carry equal marks.*

4. Flip-Flops

a. The Set-Reset (R-S) flip flop

(i) Draw the circuit of a Set-Reset flip-flop using two nand gates.

(ii) If the input to your circuit of part a(i) changes from (1,0) to (1,1) explain what will happen to the output.

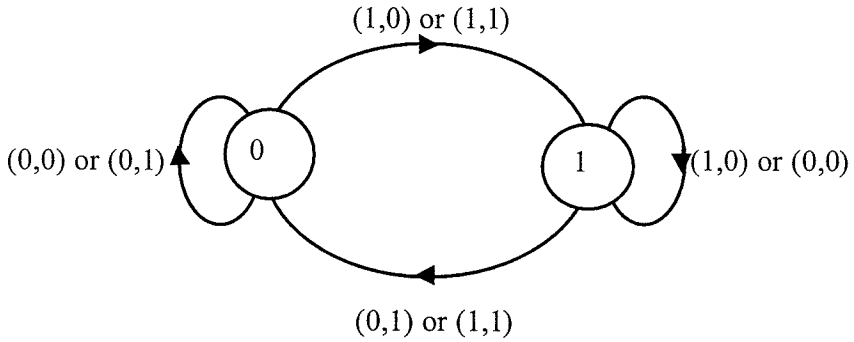
(iii) If the input to your circuit of part a(i) changes from (0,0) to (1,1) explain what will happen to the output.

b. The D-Type latch and flip-flop

(i) Design a D-type latch using the Set-Reset flip flop of part a(i), two AND gates and an inverter.

(ii) Design a master slave D-type flip flop, triggered on the falling clock edge, using two of the D type latches that you designed in part b(i) and one inverter.

c. The J-K flip flop, commonly used in hardware design, is a circuit with two inputs labelled J and K, and complementary Q and Q' outputs. It is defined by the following finite state machine, where the inputs are shown as tuples (J,K).




Design a circuit for the J-K flip flop using one D-Type flip flop and whatever other gates you require.

*The three parts carry, respectively, 30%, 30%, 40% of the marks.*