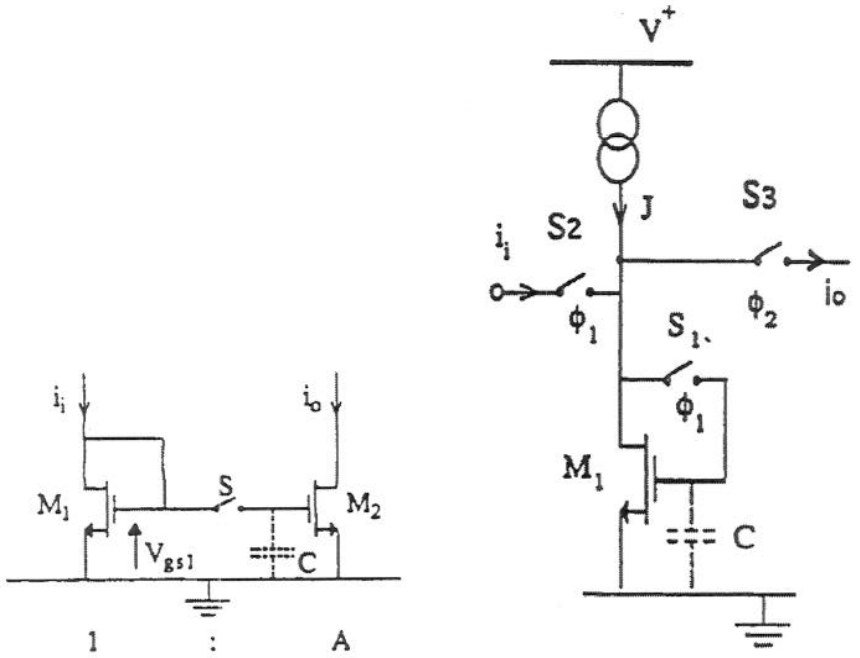
The Answers

1.

(a) [Bookwork]



First generation cell on the left. Single phase clock on S, it is a track and hold circuit. Major limitation is transistor mismatch (gain, size, temperature due to different power dissipation)

Second generation on the right. Two phase clock, during ϕ_1 it acts like a track circuit, during ϕ_2 it acts like a hold circuit.

[5]

(b) [Interpretation] The step response is derived from the continuous time response of the current mirror. This is a single pole system with a pole at $\omega_0 = g_m / 2C_{gs} = \omega_T / 2$, so that the step response is $y(t) = 1 - e^{-\omega_0 t} = 1 - e^{-\omega_T t/2}$

[5]

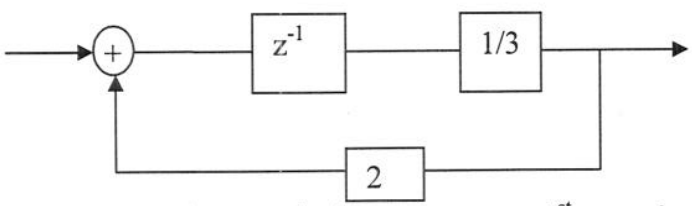
(c) [Numerical example] Settling to 0.01% requires 9.2 time constants, so that the maximum sampling frequency is $f_S < f_T / 19 \simeq 52MHz$. Finally, the sampling theorem dictates that $f_B < f_S / 2$. It follows that the signal frequency must be less than $\max f_B = 26MHz$.

[5]

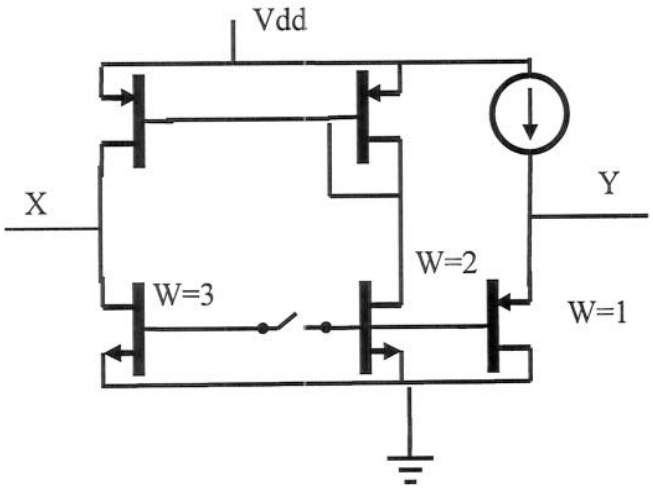
(d) [Synthesis example] We can factor this as

$$Y_N = \frac{1}{3}\left(\left(2Y_{N-1} + X_{N-1}\right) + X_N\right) \Rightarrow y = \frac{1}{3}\left(z^{-1}\left(2y + x\right) + x\right)$$

A diagram for this is



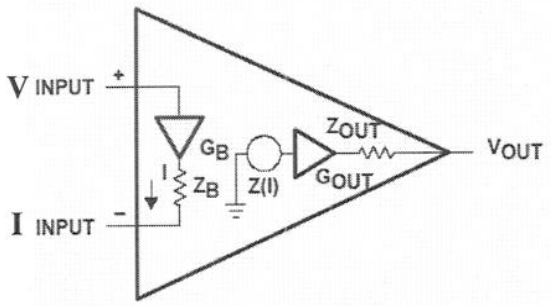
This can be implemented with a two output 1st gen.mirror with W(Q1)=2, and the y output W=1, the feedback output =2.



[5]

2.

(a) [bookwork] A CFOA comprises a voltage follower from the non-inverting to the inverting input, and a high gain transimpedance amplifier from the inverting input to the (voltage) output. A block diagram follows:



The slew rate is unlimited since it is proportional to the input current, which is only limited by the power handling of the device. In a conventional, voltage mode, op-amp, the slew rate is limited by the integrating node current supply.

[5]

(b) [Interpretation] There are two transfer functions: The voltage buffer which has a response:

$H(s)=\dfrac{1}{1+s\tau_B}$, and the transimpedance amplifier which consists of a current mirror, an impedance and a voltage buffer, so:

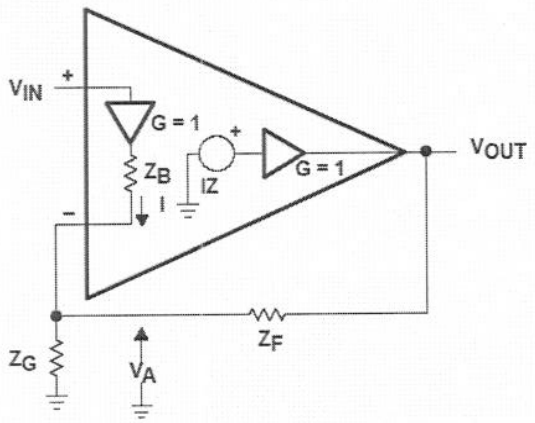
$T(s)=\dfrac{Z(s)}{(1+s\tau_M)(1+s\tau_B)}$. Usually the transimpedance $Z(s)$ is a shunt RC network, so

$$T(s)=\frac{Z_0}{(1+s\tau_M)(1+s\tau_B)(1+sZ_0C_0)}\simeq\frac{1}{sC_0(1+s\tau_M)(1+s\tau_B)}$$

At low frequencies this is an integrator. (or a dominant pole transimpedance amplifier)

[5]

(c) [Extension of bookwork] The non-inverting amplifier can be analysed as



$$V_{out} = -Z(s) I_-$$

$$I_- = \frac{1}{Z_B}(V_- - V_{in}) = \frac{1}{Z_B}\left(V_{in}\left(\frac{Z_G // Z_F}{Z_B + Z_G // Z_F} - 1 \right) + V_{out} \frac{Z_B // Z_G}{Z_B // Z_G + Z_F} \right) =$$

$$= \frac{1}{Z_B}\left(\frac{-V_{in}(Z_B Z_G + Z_F Z_B)}{Z_B Z_G + Z_F Z_B + Z_F Z_G} + V_{out} \frac{Z_B Z_G}{Z_B Z_G + Z_F Z_B + Z_F Z_G} \right) \Rightarrow$$

$$V_{out} = \frac{-Z(s)}{Z_B}\left(\frac{-V_{in}(Z_B Z_G + Z_F Z_B)}{Z_B Z_G + Z_F Z_B + Z_F Z_G} + V_{out} \frac{Z_B Z_G}{Z_B Z_G + Z_F Z_B + Z_F Z_G} \right) \Rightarrow$$

$$\frac{V_{out}}{V_{in}} = \frac{Z(s)(Z_G + Z_F)}{Z_B Z_G + Z_F Z_B + Z_F Z_G + Z(s) Z_G}$$

[5]

Assuming a dominant pole $Z(s) = \frac{Z_0}{1 + s\tau}$ we get

$$\frac{V_{out}}{V_{in}} = \frac{Z_0(Z_G + Z_F)}{(1 + s\tau)(Z_B Z_G + Z_F Z_B + Z_F Z_G) + Z_0 Z_G} =$$

$$= \frac{Z_0(Z_G + Z_F)}{Z_B Z_G + Z_F Z_B + Z_F Z_G + Z_0 Z_G} \frac{1}{1 + \frac{s\tau(Z_B Z_G + Z_F Z_B + Z_F Z_G)}{Z_B Z_G + Z_F Z_B + Z_F Z_G + Z_0 Z_G}}$$

If $Z_0 >> Z_B, Z_G, Z_F$ and $Z_B << Z_G, Z_F$

$\frac{V_{out}}{V_{in}} \simeq \left(1 + \frac{Z_F}{Z_G}\right) \frac{1}{1 + \frac{s\tau(Z_B + Z_F)}{Z_0}}$ so that the gain depends on both Z_G and Z_F while the bandwidth $\omega_B = \frac{Z_0}{\tau(Z_B + Z_F)}$ only depends on Z_F, Z_B and Z_0

[5]

3.

(a) [bookwork]

i. a CCII is a voltage and current controlled current source. It can be described as:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

ii. The 1st generation conveyor mirrors ix to iy. iy=0 in the 2nd generation conveyor.

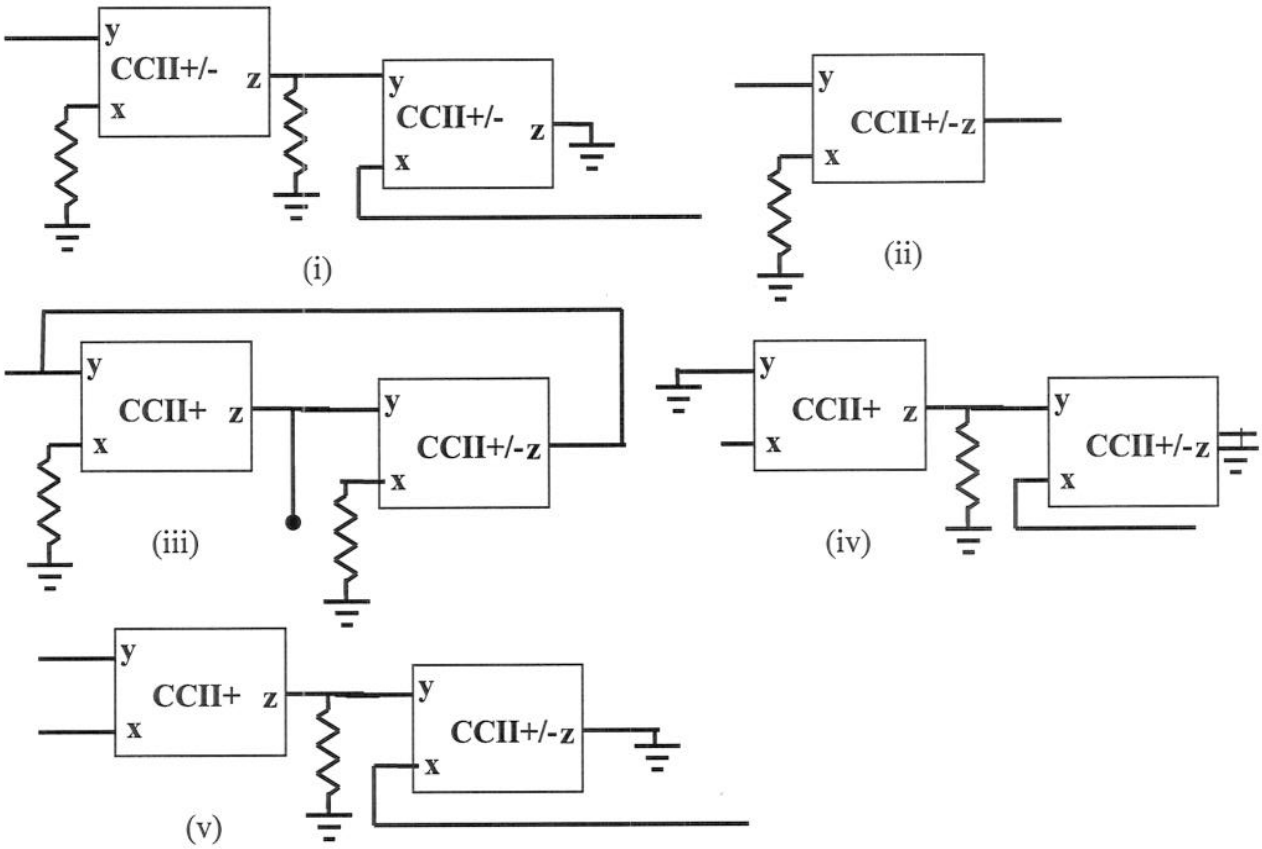
iii. an op-amp has 2 voltage inputs and a voltage output. A cc has a voltage input, a current input and a current output.

iv. A CFOA has a voltage output

v. A FET.

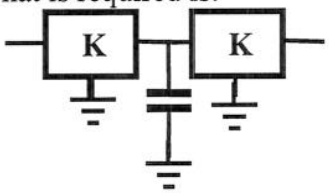
[5]

(b) [Mostly bookwork, some interpretation]



[10]

(c) [Synthesis Example] A grounded inductor between two gyrators is equivalent to a floating inductor. So What is required is:



Where each of the gyrators is the answer to biii

[5]

4.

a) [bookwork] On a closed loop of p-n junctions $\prod_{CW} J_C = \prod_{CCW} J_C$ (J are collector current densities)

For this to be true we need:

- number of CW junctions= number of CCW junctions
- number of CW npn= number of CCW npn
- number of CW pnp= number of CCW pnp
- all junctions at the same temperature

[5]

b) [interpretation] Valid at subthreshold, same expressions and conditions as bipolar principle.

Advantages: low power, drain or source current can be used indiscriminantly

Disadvantage: Threshold voltage comes into play.

[5]

c) [computed example]

$$I_2 = I_{out} + I_6$$

$$I_1 I_2 I_3 I_4 I_5 = I_6 I_7 I_8 I_9 I_{10} \Rightarrow z^2 I_1 I_{out}^2 = z^2 I_3 I_4^2 \Rightarrow I_{out} = I_4 \sqrt{\frac{I_3}{I_1}}$$

$$\text{if } |I_3| = \left|\frac{d}{dt} I_{in}\right| = \omega |I_{in}| \text{ and } |I_1| = \left|\int I_{in} dt\right| = \frac{1}{\omega} |I_{in}| \Rightarrow I_{out} \propto \omega I_{in}$$

[10]

5.

a) [bookwork]

$$\left.\begin{aligned} &I_{in} = I_s e^{\beta V_i} \Rightarrow V_i = V_T \ln\left(I_{in} / I_s\right) \\ &I_C + I_0 = C\frac{dV_C}{dt} + I_0 = I_s e^{\beta(V_i - V_C)} = I_{in} e^{-\beta V_C} \\ &I_{out} = I_S e^{\beta V_1} = I_S e^{\beta V_C + \ln(I_0/I_S)} = I_S e^{\beta V_C} I_0 / I_S = I_0 e^{\beta V_C} = I_0 x \end{aligned}\right\} \text{with } \beta = q/kT = 1/V_T$$

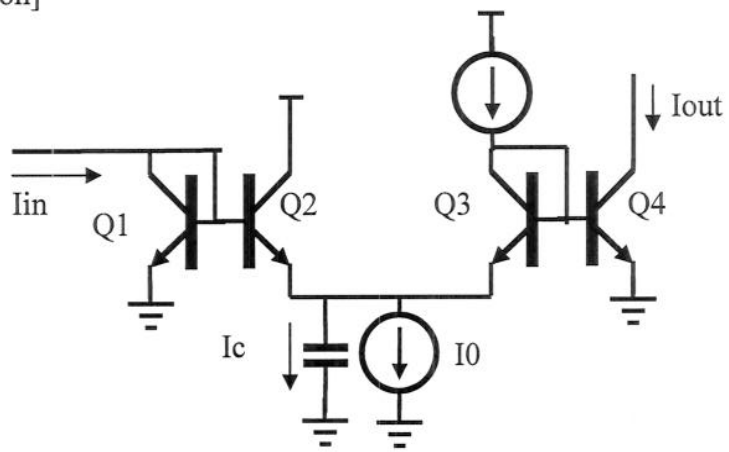
$$x = e^{\beta V_C}$$

$$\frac{dx}{dt} = \beta \frac{dV_C}{dt} x$$

$$C\frac{dV_C}{dt} + I_0 - I_{in} e^{-\beta V_C} = 0 \Rightarrow \frac{C}{\beta x}\frac{dx}{dt} + I_0 - \frac{I_{in}}{x} = 0 \Rightarrow \frac{C}{\beta}\frac{dx}{dt} + I_0 x = I_{in}$$

[5]

b) [interpretation]



$$I_{C2} = I_C - I_U = I_s e^{\beta V_{in}} / e^{\beta V_C} \Rightarrow I_{C2}' = \beta I_{C2}\left[V_{in}' - V_C'\right]$$

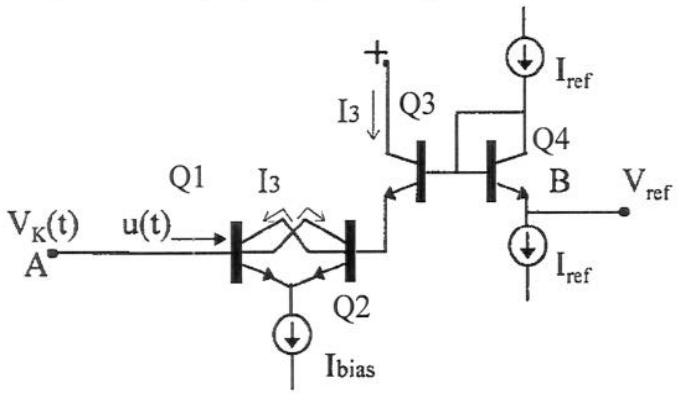
$$V_C' = \frac{1}{C} I_C = \frac{1}{C}\left[I_{C2} - I_U\right]$$

$$I_{C2}' = \beta I_{C2}\left[V_{in}' - V_C'\right] = \beta I_{C2}\left[V_{in}' - \frac{1}{C}\left[I_{C2} - I_U\right]\right] \Rightarrow$$

$$I_{C2}' - \frac{\beta}{C}\left(CV_{in}' + I_U\right) I_{C2} + \frac{\beta}{C} I_{C2}^2 = 0 \Rightarrow I_{C2}' - \frac{\beta}{C}\left(CV_{in}' + I_U\right) I_{C2} + \frac{\beta}{C} I_{C2}^2 = 0$$

[5]

c) [computed example, interpretation]



$$\left.\begin{aligned} &I_3 = I_s e^{\beta V_{BE3}} \\ &V_{B3} = V_{B4} = V_{ref} + \frac{1}{\beta}\ln\left(I_{ref}/I_s\right) \\ &V_{E3} = V_K \end{aligned}\right\} \Rightarrow I_3 = u = I_S \exp\beta\left(V_{ref} + \frac{1}{\beta}\ln\left(I_{ref}/I_s\right) - V_K\right) \Rightarrow$$

$$u = I_S \exp\beta\left(V_{ref} - V_K\right)\exp\left(\ln\left(I_{ref}/I_s\right)\right) = I_{ref}\exp\beta\left(V_{ref} - V_K\right)$$

This is useful for 2 reasons:

- it implements the exponential mapping $x = e^{\beta V_C}$ i.e. generates a current signal proportional to the exponential f a voltage somewhere else in the circuit.
- It implements the $z = 1/x$ function required to linearise the ODE describing the log domain cell.

[5]

d) [computed example] Normalised notation:

$$t \to \omega_0 t$$

$$\frac{d^2y}{dt^2} + \omega_0^2 y = \omega_0^2 U \Rightarrow \ddot{y} + y = x$$

$$\left.\begin{aligned} &\dot{y} = z \\ &\dot{z} + y = x \end{aligned}\right\} \Rightarrow \frac{d}{d\tau}\begin{bmatrix} y \\ z \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}\begin{bmatrix} y \\ z \end{bmatrix} + \begin{bmatrix} 0 \\ x \end{bmatrix}$$

[5]