IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2016

EEE PART I: MEng, BEng and ACGI

**ANALOGUE ELECTRONICS 1**

Corrected Copy

Monday, 6 June 10:00 am

Time allowed: 2:00 hours

**There are THREE questions on this paper.**

**Answer ALL questions.**
**Q1 carries 40% of the marks. Questions 2 and 3 carry equal marks (30% each).**

**Any special instructions for invigilators and information for candidates are on page 1.**

Examiners responsible
First Marker(s) : A.S. Holmes
Second Marker(s) : C. Papavassiliou

## The Questions

1. For each part of this question, state clearly any assumptions made in your calculations.

   a) For the circuit in Figure 1.1, choose values for $R_S$ and $R_D$ such that the drain current is 0.5 mA and the MOSFET is at the point of pinch-off.

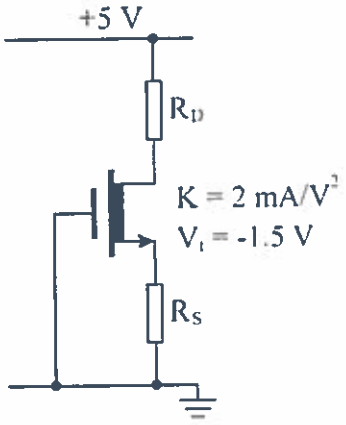


*Figure 1.1* [6]

   b) Using the resistance reflection rule, or otherwise, determine the small-signal output resistance of the circuit in Figure 1.2.

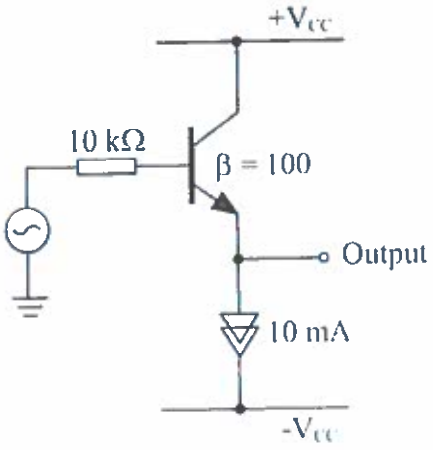


*Figure 1.2* [6]

   c) Sketch the circuit for a Class B push-pull output stage and explain why such a circuit exhibits cross-over distortion. To aid your explanation sketch the output waveform produced when the input signal is a sinusoid with amplitude 10 V peak-to-peak. [8]

**Question 1 continues on the next page...**

**Question 1 continued**

d) Determine the differential output voltage V for the circuit in Figure 1.3, assuming the MOSFETs are matched and have $K = 0.5\ mA/V^2$. You may quote the standard result for the small-signal differential gain of a differential pair.

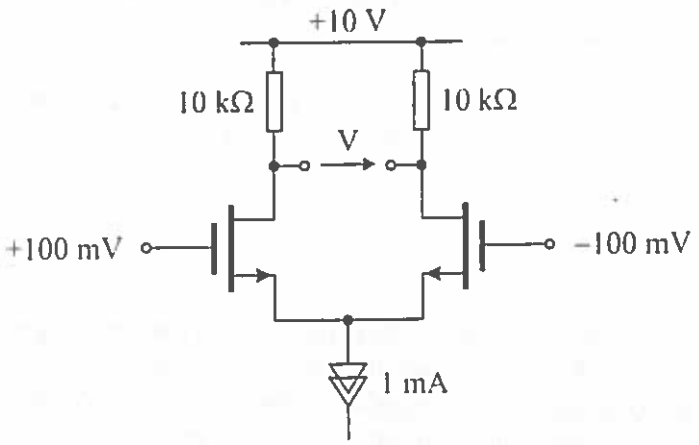


*Figure 1.3*

[6]

e) A depletion type active load is a 2-terminal device formed by connecting together the gate and source of a depletion mode MOSFET. Sketch the I-V characteristic for this kind of device, showing clearly on your graph the active and linear regions of operation. State which polarity of device your graph refers to. [6]

f) The rise time of a digital signal is normally defined as the time taken for the voltage to rise from 10% to 90% of its final value. Similarly the fall time is the time taken for the voltage to fall from 90% to 10% of its initial value. Using these definitions determine the rise and fall times of the output voltage in the circuit of Figure 1.4, assuming the input waveform switches instantaneously between zero and +5 V.

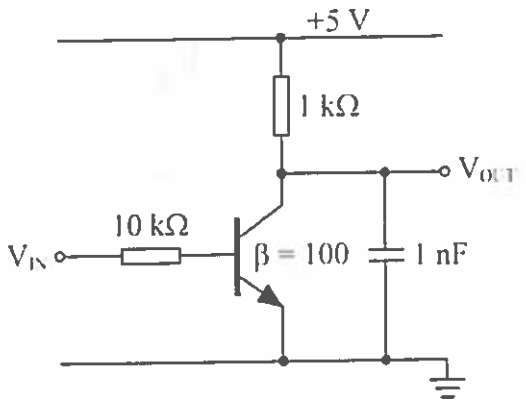


*Figure 1.4*

[8]

2. Figure 2.1 shows a common-emitter amplifier, connected between an AC-coupled signal source and a capacitive load. You should assume that the AC-coupling capacitor, C, is effectively a short circuit at all signal frequencies of interest.

a) Determine the collector bias current and quiescent output voltage of the amplifier, stating clearly any assumptions you make. Your calculation should take into account the base current of the transistor. [8]

b) Draw a small-signal equivalent circuit for the amplifier, replacing the RC network in the emitter by an equivalent impedance $Z_E$, and show that the small-signal voltage gain may be written as:

$$A_V = \frac{-\alpha R_C}{r_e + Z_E}$$

where $R_C$ is the load resistance in the collector, $r_e$ is the small-signal emitter resistance of the transistor and $\alpha$ is its common-base current gain. You may neglect the small-signal output resistance of the transistor. Hence evaluate $A_V$ both in the mid-band, where $C_E$ is effectively a short circuit, and at low frequency where $C_E$ is effectively an open circuit. [12]

c) Choose the value of $C_E$ so that the 3-dB point at the low-frequency end of the mid-band occurs at 1 kHz. Also determine the cut-off frequency associated with the load capacitor, and hence sketch a Bode plot showing the variation of the in-circuit gain $v_L/v_S$ with frequency over the frequency range 1 Hz to 1 MHz. [10]

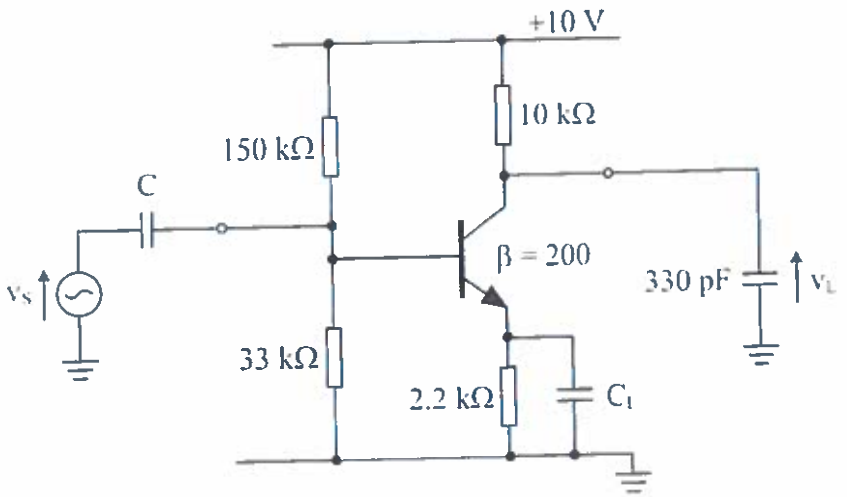


*Figure 2.1*

3. Figure 3.1 shows an NMOS amplifier employing two enhancement mode MOSFETs.

a) Explain the role of the 10 MΩ resistor and show that, if the current in the 1 MΩ resistors is neglected, the quiescent output voltage may be expressed as:

$$V_{OUT} = \frac{V_{DD} - 2V_{t2} + 2V_{t1}\sqrt{K_1/K_2}}{1 + 2\sqrt{K_1/K_2}}$$

where the symbols K and $V_t$ denote the usual MOSFET parameters, and the subscripts 1 and 2 refer to Q1 and Q2 respectively.

Evaluate $V_{OUT}$ and determine the quiescent drain current in each MOSFET. [12]

b) Draw a small-signal equivalent circuit of the amplifier, and hence determine the small-signal voltage gain at frequencies for which the input capacitor is effectively a short circuit. Also calculate the small-signal input resistance of the circuit. You should assume the MOSFETs have infinite small-signal output resistance. [12]

c) If a sinusoidal input signal is applied to the amplifier, over what range of input amplitudes will both transistors remain active? Assume that the input capacitor has negligible impedance at the signal frequency. [6]

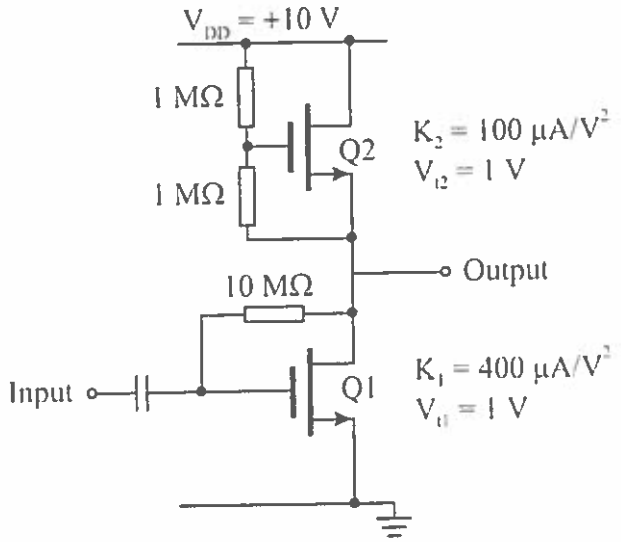


*Figure 3.1*