E4.16
AO5

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2007

MSc and EEE PART IV: MEng and ACGI

CURRENT-MODE ANALOGUE SIGNAL PROCESSING

Friday, 4 May 10:00 am

Time allowed: 3:00 hours

Corrected Copy

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : C. Papavassiliou
Second Marker(s) : E. Rodriguez-Villegas

E4.16 Current Mode Analogue Signal Processing

1. a) State the translinear principle for a circuit containing loops consisting entirely of base-emitter junctions of bipolar transistors. Assume that each transistor has a different area. Comment on how the effects of collector voltage variation and finite β errors can be accounted for. [5]

   b) Identify input and output currents in figure 1.1(a) Write equations relating the currents in figure 1.1(a) assuming that current gain and collector voltage errors are negligible. [5]

   c) Show that the currents in figure 1.1(b) satisfy the following equation:

$$\frac{I_{o2}-I_{o1}}{I_2-I_1}=\left(1+\frac{I_5}{I_1+I_2}\right) \tag{1.1}$$

   [5]

   d) Suggest how the circuit in figure 1.1(b) can be used as a mixer which can multiply a small differential RF signal with a bigger local oscillator signal. [5]

[Total: 20]

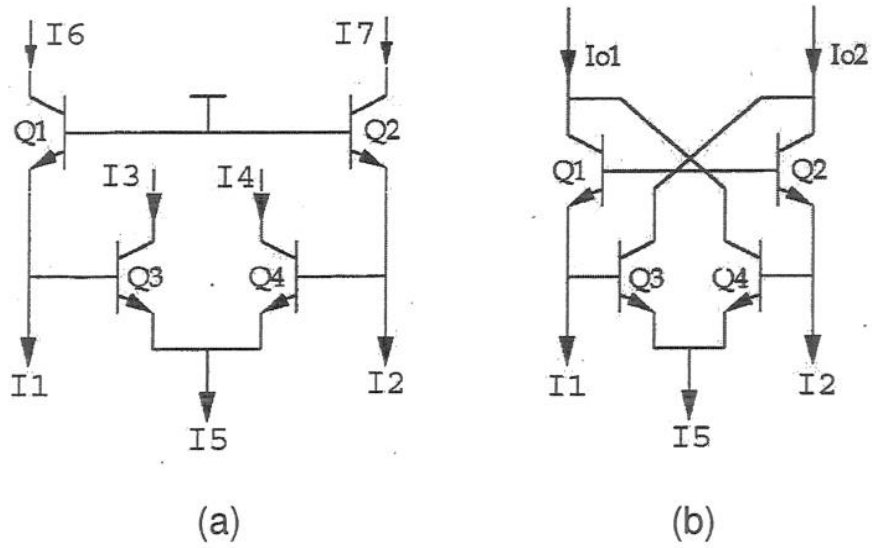


Figure 1.1 Translinear circuits for question 1.

2. a) State the definition of the adjoint of a network [5]

b) State the transformation rules by which we can derive the adjoint of a voltage mode circuit. [3]

c) Derive the current mode equivalent of the band reject filter of figure 2.1. Assume the voltage amplifier has a gain K and ideal terminal characteristics.

[7]

d) Modify the circuit of question 2.c) so that it has ideal current mode terminal characteristics. [2]

e) How can the circuit of question 2.c) be used as a **Voltage Mode** circuit? [3]

[Total: 20]

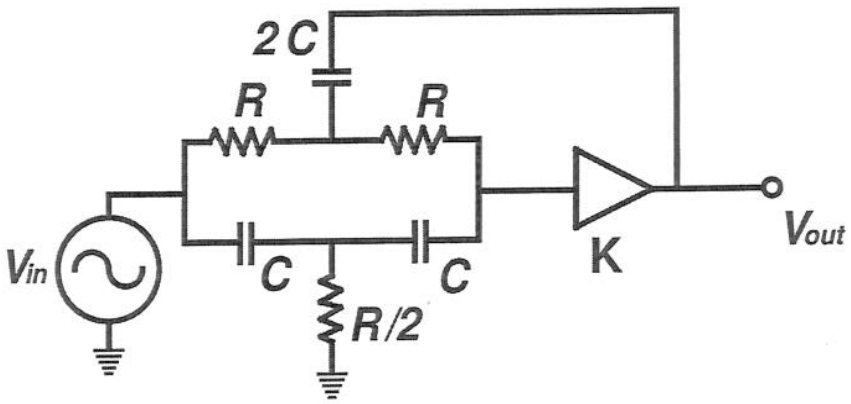


Figure 2.1 Schematic of filter for question 2.c)

3. a) Define the two types of second generation current conveyor (CCII) in terms of their voltage - current characteristics. [4]

b) Which common device is an approximate small signal realisation of one of the CCII types? How does the small signal behaviour of this device deviate from the behaviour of an ideal CCII at DC and as frequency increases? [2]

c) Draw schematic diagrams for the following circuits implemented with second generation current conveyors:

i) Finite gain current amplifier [3]

ii) Ideal current integrator [2]

iii) Lossy current integrator [2]

iv) Summing current amplifier [2]

d) Use the subcircuits of question 3.c), and any other subcircuits you may need, to derive a block diagram for a CCII implementation of a current mode version of the filter of figure 3.1. [5]

[Total: 20]

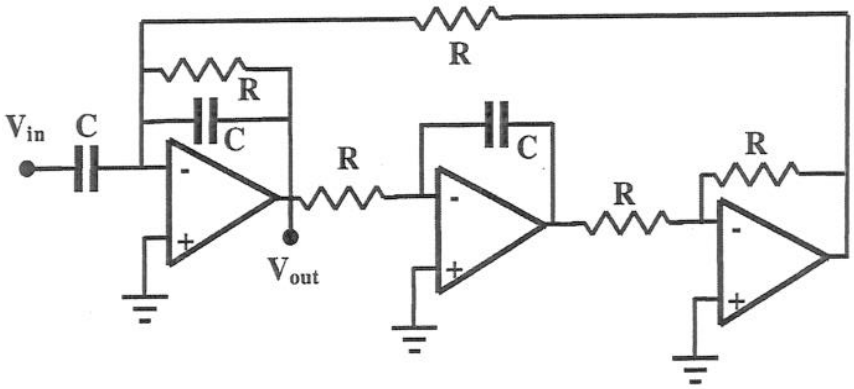


Figure 3.1 Voltage mode filter for question 3.

4. Consider the circuit in figure 4.1.

In this question $\beta = q/kT = 1/V_{th}$ with $V_{th} = 26mV$ the thermal voltage at room temperature. Other symbols have the meaning shown in figure 4.1.

a) Use the translinear principle to derive an expression relating the collector currents of the 4 transistors. Express I_c in terms of I_{in}, I_{out}, I_0 and U. Assume the transistors are all identical and have infinite current gain. [2]

b) Prove that

$$I_{out} = I_0 \exp(\beta V_c) \Rightarrow \frac{dIout}{dt} = \frac{\beta I_{out} I_c}{C} \tag{4.1}$$

[3]

c) Prove that the output current satisfies a differential equation of the form:

$$\frac{dIout}{dt} + \alpha I_{out} = \beta I_{in} \tag{4.2}$$

Express the constants α and β in terms of the thermal voltage, bias currents and the node capacitance. [4]

d) Derive a state space model for a second order high-pass filter of equation 4.3 using ideal integrators. [5]

$$H(s) = \frac{y(s)}{x(s)} = \frac{s^2}{s^2 + 2\zeta s\omega_0 + \omega_0^2} \tag{4.3}$$

e) Draw a block diagram to show how the filter in question 4.d) can be implemented using two log-domain cells like the one in figure 4.1. Specify I_0, U and C for each cell so that $\omega_0 = 100MHz$ and $\zeta = 1$. Specify any "'black box" circuits you need to implement feedback connections. The filter you design should have voltage mode terminal characteristics. [6]

[Total: 20]

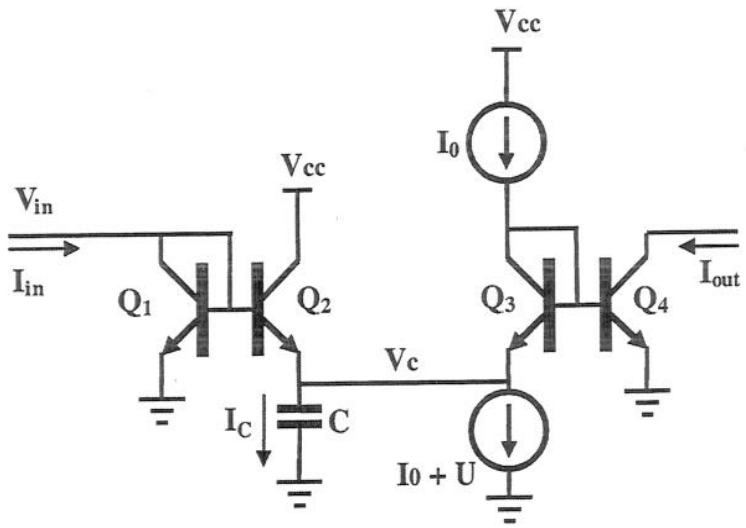


Figure 4.1 A filter unit cell for question 4.

5. a) Draw a block diagram for the current feedback op-amp (CFOA), using voltage buffers, current mirrors and passive components. [3]

b) Write an equation for the frequency response of the open loop gain of the CFOA. Explain why, in many applications, the CFOA does not exhibit a constant gain-bandwidth product. [3]

c) Derive an equation for the DC voltage gain of the circuit in figure 5.1. What roles do the two resistors play in determining the gain and bandwidth of the amplifier? [3]

d) Why is the slew rate of the CFOA large? [3]

e) Draw schematic diagrams to show how the following building blocks may be made out of current feedback op-amps and passive components:

i) Unity gain voltage buffer. [2]

ii) Differentiator. [2]

iii) Integrator. [4]

[Total: 20]

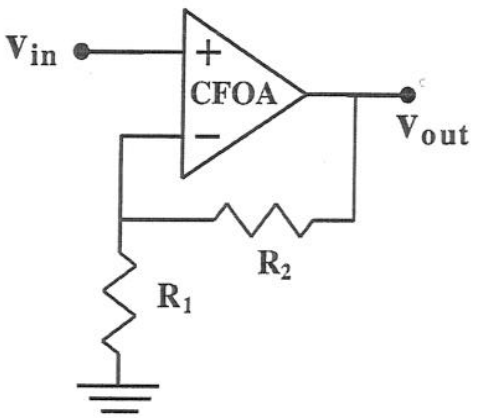


Figure 5.1 A current feedback op-amp circuit for question 5.

6. a) Draw a schematic diagram for a first generation current copier. Describe its operation and comment on its limitations. [3]

b) Draw a schematic diagram for a second generation current copier (SI cell); explain its operation. What is its main advantage relative to the first generation copier? [3]

c) Explain 3 limitations of the second generation SI cell and describe, using appropriate circuit diagrams, methods used to reduce the effects of these limitations. [3 each]

d) Comment on how the considerations listed in question 6.c) will limit the maximum signal frequency in an application where filter coefficients need to be realised with a high relative accuracy. [5]

[Total: 20]

2007

A05 E416: Current Mode ASP - SOLUTIONS

Q1:

a) [bookwork] In a closed loop containing :
- an equal number CW and CCW pnp BE junctions
- an equal number CW and CCW npn BE junctions
- all transistors at same temperature

the collector current densities satisfy:

$$\prod_{n\in CW}\frac{I_{c,n}}{A_{n,eff}}=\prod_{n\in CCW}\frac{I_{c,n}}{A_{n,eff}}$$

The effective areas can be used to account for drain voltage:

$$A_{eff}=A\left(1+V_{CE}/V_A\right)$$

If the emitter current appears in a circuit then, clearly, $I_E=I_C\left(\beta+1\right)/\beta$

[5]

b) [computed example, taught] Inputs: I_1 , I_2 , I_5 . The rest are outputs.

$$I_3+I_4=I_5=2I_{52}\Rightarrow I_4=I_{52}\left(1+y\right),I_3=I_{52}\left(1-y\right)$$

$$I_6=I_1$$

$$I_7=I_2$$

$$I_1I_3=I_4I_2\Rightarrow\frac{I_1}{I_2}=\frac{I_4}{I_3}=\frac{1+y}{1-y}$$

Let the average of I_1 , I_2 be I_0 we can write:

$$I_1=I_0\left(1+y\right)$$

$$I_2=I_0\left(1-y\right)$$

[5]

c) [computed example, taught]

$$I_{01}=I_1+I_4=\left(I_0+I_{52}\right)\left(1+y\right)$$

$$I_{02}=I_2+I_3=\left(I_0+I_{52}\right)\left(1-y\right)$$

$$\left.\begin{aligned}I_{02}-I_{01}&=\left(I_0+I_{52}\right)\left(1-y\right)-\left(I_0+I_{52}\right)\left(1+y\right)=\left(-\left(I_1+I_2\right)-I_5\right)y\\I_2-I_1&=-\left(I_1+I_2\right)y\end{aligned}\right\}\Rightarrow$$

$$\frac{I_{02}-I_{01}}{I_2-I_1}=1+\frac{I_5}{I_1+I_2}$$

[5]

d) [exercise]

Apply the LO on I_5 and the RF on I_1 and I_2 . Then,

$$I_{IF}=\left(I_{02}-I_{01}\right)=\left(1+\frac{I_5}{I_1+I_2}\right)\left(I_2-I_1\right)=I_{RF}+\frac{I_{LO}I_{RF}}{\left\langle I_{RF}\right\rangle}$$

The lower the common mode RF signal the higher the gain.

[5]

Q2: a) [bookwork] Two networks A, B are called adjoint if: $\sum_n \left(V_n^A I_n^B - I_n^A V_n^B \right) = 0$.

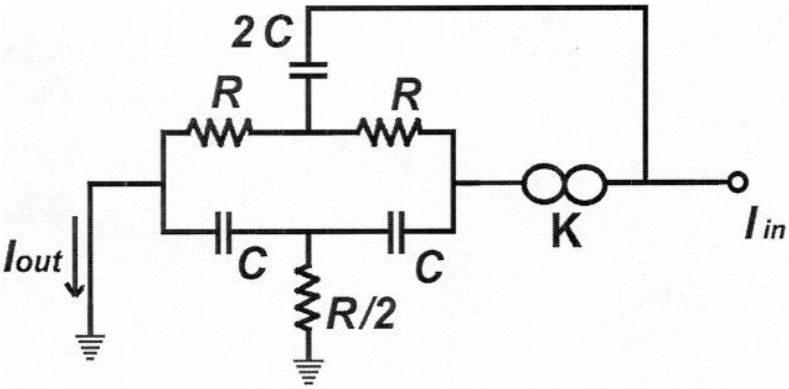
(will accept for partial credit verbose descriptions)

[5]

b) [bookwork] Keep passives the same, Replace voltage amps by reverse current amps of equal gain and vice versa, replace voltage sources by current meters and current sources by voltage meters.

c) [computed example]

[3]



[7]

d) If the voltage amplifier is ideal then this has already an ideal current input. To also have an ideal current output we need a transconductor at the output (left)

[2]

e) To use this in voltage mode we need a transconductor at the input (right) and a transimpedance at the output (left)

[3]

Q3. a) [bookwork] CCII are inverting and non inverting

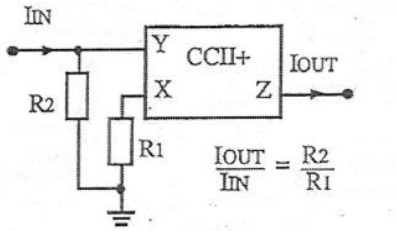
$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}$$

[4]

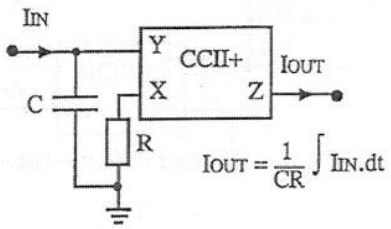
b) [bookwork] The MOSFET is similar to a CCII- . At higher frequencies Iy is significant.

[2]

c) [bookwork] i) Current amp



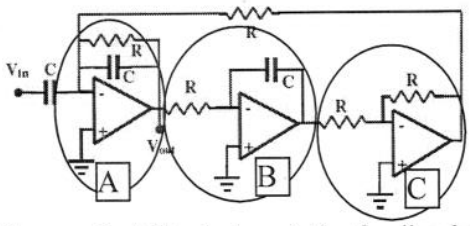
ii) current integrator:



Precede these with a current buffer (ground y, input at x, output at z) for better behaviour.
iii) lossy current integrator: use shunt RC in place of C
iv) x is a summing junction , connect currents to it via mirrors

[9]

d) [computed example]



Observe that block A and the feedback resistor form a lossy voltage integrator, block B an ideal voltage integrator, block c a voltage gain cell. By superposition, V_{in} contibutes to v_{out} $\frac{sRCV_{in}}{1+RsC}$ so that a current differentiator is needed as well. This would be same as integrator with interchanged R and C.

[5]

4. a) [extension of taught theory]

$$I_1 I_3 = I_2 I_4 \Rightarrow I_{in} I_0 = (I_c + U) I_{out} \Rightarrow I_c = I_{in} I_0 / I_{out} - U$$

[2]

b) $$I_{out} = I_s \exp\beta\left(V_c + \frac{1}{\beta}\ln\left(\frac{I_0}{I_s}\right)\right) = I_0 \exp\beta V_c \Rightarrow \frac{dI_{out}}{dt} = I_{out}\beta\frac{dV_c}{dt} = \frac{\beta I_{out} I_c}{C}$$

[3]

c) substitute in a) $$\frac{dI_{out}}{dt} = \frac{\beta I_{out} I_c}{C} = \frac{\beta I_{out}}{C}(I_{in} I_0 / I_{out} - U) \Rightarrow$$

$$\frac{dI_{out}}{dt} + \frac{\beta U}{C} I_{out} = \frac{\beta I_{in} I_0}{C}$$

[4]

d) [application] state space model:

$$H(s) = \frac{s^2}{s^2 + 2\zeta s\omega_0 + \omega_0^2} \Rightarrow$$

$$y\left(s^2 + 2\zeta s\omega_0 + \omega_0^2\right) = s^2 x$$

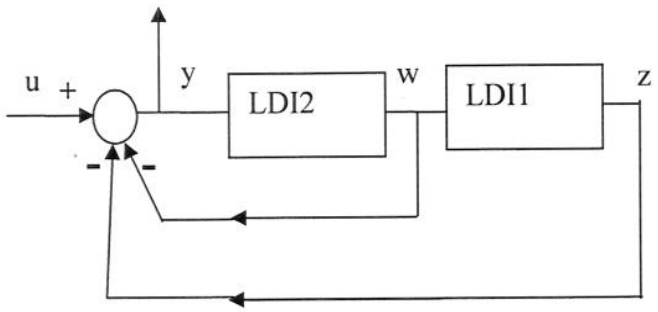
if z is the solution of $z\left(s^2 + 2\zeta s\omega_0 + \omega_0^2\right) = u$ then y is the 2nd derivative of z.

The state space decomposition of the unit response is:

$$\left.\begin{aligned} \dot{z} &= w \\ \dot{w} = \ddot{z} = y &= u - 2\zeta\omega_0 w + \omega_0^2 z \end{aligned}\right\} \Rightarrow \frac{d}{dt}\begin{bmatrix} z \\ w \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -\omega_0^2 & -2\zeta\omega_0 \end{bmatrix}\begin{bmatrix} z \\ w \end{bmatrix} + \begin{bmatrix} 0 \\ u \end{bmatrix}$$

[5]

e)



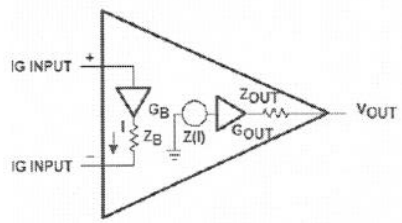
For both integrators U=0. Then, assuming we have unity gain inverters,

$$\left.\begin{aligned} \frac{\beta I_{01}}{C_1}\frac{\beta I_{02}}{C_2} &= \omega_0^2 \\ \frac{\beta I_{02}}{C_2} &= 2\zeta\omega_0 \end{aligned}\right\} \Rightarrow \frac{\beta I_{01}}{C_1} = \frac{\omega_0}{2\zeta}$$ Assuming equal capacitors, $I_{02} = 4I_{01}$

For the circuit to have voltage mode characteristics we need a transconductor at the input and a transimpedance at the output.

[6]

5) a) [bookwork]



Z(I) is usually a mirror feeding into a high impedance node, typically a capacitor.

[3]

b) [extension of theory]

From V+ to V- : $\frac{V_-}{V_+} = \frac{1}{1+s\tau_1}$

From V- to the high impedance junction: $\frac{i_z}{i_-} = \frac{1}{1+s\tau_2}$

The transimpedance is typically a capacitor. Finally there is another buffer, presumably similar to the one at the input. To lowest order,

$$Z_T = \frac{v_{out}}{i_-} = \frac{Z_0}{1+s\tau_2}\frac{1}{1+s\tau_1}$$

This is NOT a dominant pole amplifier and cannot be expected to manifest a constant GBW product.

[3]

c) [bookwork]

$$\left(\frac{V_{out}-v_{in}}{R_2}-\frac{v_{in}}{R_1}\right)Z = V_{out} \Rightarrow V_{out}\left(1-\frac{Z}{R_2}\right) = -v_{in}Z\frac{R_1+R_2}{R_1R_2}$$

In the limit $Z \to \infty$

$\frac{V_{out}}{v_{in}} \to 1+\frac{R_2}{R_1}$. R2 sets the bandwidth, R1 the gain.

[3]

d) [bookwork] The slew rate of an amplifier is determined by the maximum current available at the high impedance capacitive node. In the CFOA this current is the input current mirrored, unlike the op-amp where it is limited by an internal supply.

[3]

e) [design, extension of theory]

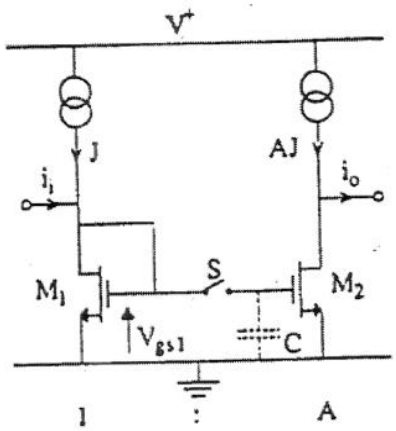
i) Voltage buffer: The previous circuit with R2=0

ii) Differentiator: Use an inductor in the feedback path, or an HPF at the v-input.

iii) Integrator. Cannot use a feedback capacitor, since it would lead leads to an increasing feedback current with frequency. Given that there are 3+ poles in the forward (transimpedance) path it follows that the oscillation condition can be satisfied with C in the feedback.

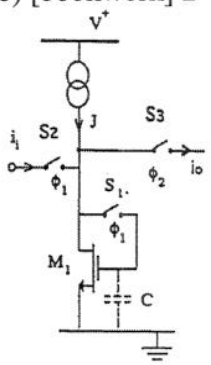
To make an integrator one can use a passive LPF at the voltage input terminal of a CFOA.

6. [mostly bookwork – I do not expect the semi-quantitative analysis for full credit]
a) 1st generation copier: M1 memorises, M2 copies.
Transistor match important



[3]

b) [bookwork] 2nd generation SI cell:



It is a sample and hold, does not matter what the memory device is. Complexity: 2 clock phases.

[3]

c[bookwork, interpretation]
i) Drain voltage variation: Gain error due to channel length modulation. In memory cycle input admitance is

$$Y_{in} = g_m$$

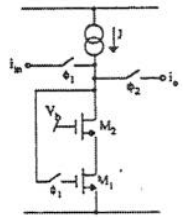
in the output cycle output admittance is

$$Y_{out} = \lambda I_d$$

A cycle reading from a source of Z_s and writing to a load Z_l would lead to a current gain correction

$$H = \frac{i_{out}}{i_{in}} = \frac{g_m Z_s}{Z_s g_m + 1} \frac{1}{1 + Z_L \lambda I_D}$$

A level difference between input and output can also lead to a gain error.
Cascoding is one way to reduce this effect.



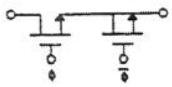
$R_o = g_{m2} r_{ds1} r_{ds2}$

[3]

ii) Charge injection

Switches are not ideal relays, but transistor circuits. This means that the gate currents of the switches add onto the signal currents so that $\delta i \simeq \omega C_{gs} v_{\text{supply}}$. So the charge injection current error is proportional to the switching frequency. Charge injection errors are reduced by use of dummy switches operated in antiphase with the main switch:

Dummy switch compensation

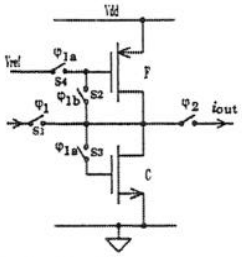


[3]

iii) Settling time

Both at input and at output mode there will be an single pole low pass response for signal to settle. Typically the input settling will be

$\tau_i = \dfrac{1}{2\pi f_T}$ but there is only half a period available for the signal to settle. Can be partially corrected by measuring the discrepancy between signal and memorised version, as in the S^2I cell:



4 clock phases are now required, and the signal frequency is effectively constrained to ¼ the master clock frequency.

[3]

d) [interpretation of theory] I look for interpretation here. To correct channel length modulation error, we will assume a chain of identical cells so, in each cycle the gain is:

$$H = \frac{i_{out}}{i_{in}} = \frac{g_m Z_s}{Z_s g_m + 1} \frac{1}{1 + Z_L \lambda I_D} = \frac{g_m / \lambda I_D + 1}{g_m / \lambda I_D} \frac{1}{1 + \lambda I_D / g_m} = \left(\frac{x}{1+x}\right)^2 \simeq 1 - \frac{1}{2x}$$

x being the FET intrinsic voltage gain. $x \simeq \dfrac{f_T}{f}$. cascoding increases the max voltage gain to $x_{cascode} \simeq x^2$ With a cascode cell we still need $f_{\text{signal}} \leq f_T / 100$

The settling time introduces a gain of $H \simeq \text{sinc}\left(\frac{\pi f_{\text{signal}}}{f_{sw}}\right) \simeq 1-\frac{1}{3}\left(\frac{\pi f_{\text{signal}}}{f_{sw}}\right)^3$ so that approximately $\frac{f_{\text{signal}}}{f_{sw}} \leq \frac{1}{20}$. Algorithmic corrections make the error smaller but introduce a factor of 2 reduction on the signal frequency relative to the switching frequency.

Finally, charge injection adds a constant error term. We can estimate:

$$\left.\begin{aligned} \delta I_{inj} &\propto \omega_{sw} C_{gs} V_{DD} \\ \delta I_{sig} &\propto \frac{\omega_{sig}}{\omega_{sw}} g_m V_{DD} \end{aligned}\right\} \Rightarrow \frac{\delta I_{inj}}{\delta I_{sig}} \propto \frac{\omega_{sw}^2}{\omega_{sig}\omega_T} \Rightarrow f_{sig} \gg \frac{f_{sw}^2}{f_T}$$

meaning that the charge injection error gets worse the higher the ratio of the switching to signal frequency.

[5]