IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2017

EEE PART II: MEng, BEng and ACGI

Corrected copy

ANALOGUE ELECTRONICS 2

Thursday, 15 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : T. Constandinou
Second Marker(s) : C. Toumazou

1. This question consists of 5 sub-questions. Each item can be answered in a few words or a short paragraph with use of a diagram and/or expression where helpful. Please answer all sub-questions and simplify expressions where possible stating any assumptions made.

a) Which of the topologies shown below in Fig. 1.1 would have better performance? Explain why. [5]

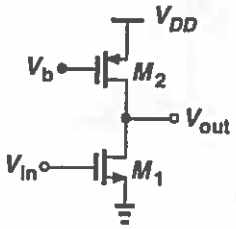

Fig. 1.1(a)

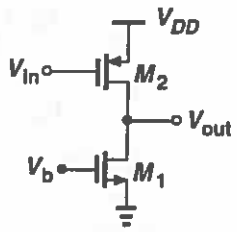

Fig. 1.1(b)

b) Propose a *circuit topology* (e.g. common source amplifier with resistive load), for each of the following applications, in each case justifying your selection, and sketching the circuit schematic.

(i) A pre-amplifier to interface to a capacitive microphone. [5]

(ii) A circuit to increase the DC level of a signal by 1V. [5]

(iii) A high frequency amplifier providing relatively high isolation between the input and output. [5]

c) An inverting amplifier must provide a nominal gain of 20 with a gain error of 0.5%. Determine the minimum required op-amp gain. [5]

d) Determine the closed loop gain of the circuit shown below in Fig. 1.2. Assume $\lambda = 0$. [5]

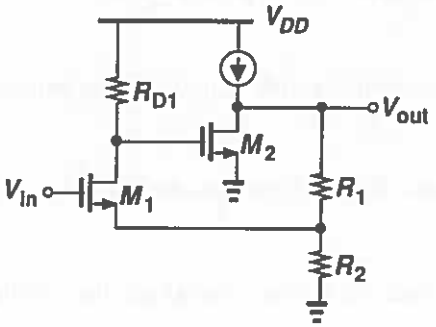

Fig. 1.2

e) Derive expressions (by inspection) for the *output resistance* of the amplifier circuits shown below in Fig. 1.3 (including r_0). [10]

(i)

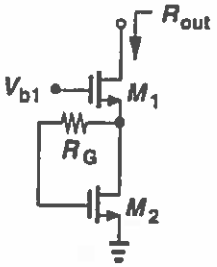

Fig. 1.3(a)

(ii)

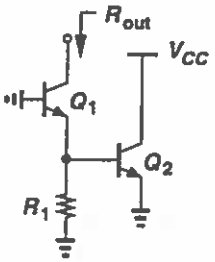

Fig. 1.3(b)

2. The circuit shown below in Fig. 2.1 is a single-stage fully differential amplifier with corresponding transistor dimensions shown in Table 2.1.

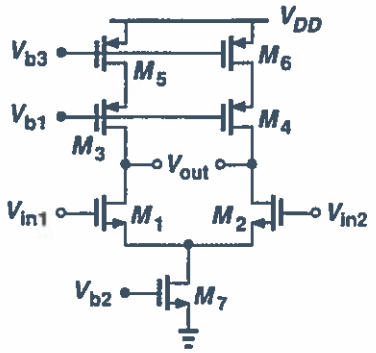

Fig. 2.1

Table 2.1. Transistor sizes

M_1	M_2	M_3	M_4	M_5	M_6	M_7
200/0.5	200/0.5	9/0.18	9/0.18	50/1	50/1	50/1

Assume all devices are in saturation and assume $\lambda \neq 0$. Use the following expression for the large signal drain current of a MOSFET (in saturation) with corresponding transistor parameters:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$\mu_n C_{ox} = 200\mu A/V^2$ $\quad V_{THN} = 0.4V$ $\quad \lambda_N = 0.1V^{-1}$
$\mu_p C_{ox} = 100\mu A/V^2$ $\quad V_{THP} = -0.5V$ $\quad \lambda_P = 0.2V^{-1}$

a) Design a voltage reference circuit to generate V_{b2} from a 1.8V supply such that $I_{D7} = 2mA$.
[5]

b) Determine an expression for the differential voltage gain of the amplifier.
[5]

c) Determine an expression for the common-mode voltage gain of the amplifier.
[5]

d) Use your answers to parts (b) and (c) to evaluate the common-mode rejection ratio.
[10]

e) State the function of transistors $M_1 - M_2$, $M_3 - M_4$, $M_5 - M_6$, and M_7 and comment on the specified device sizes.
[5]

3. The circuit below in Fig. 3.1 illustrates a cascade of two identical common source stages.

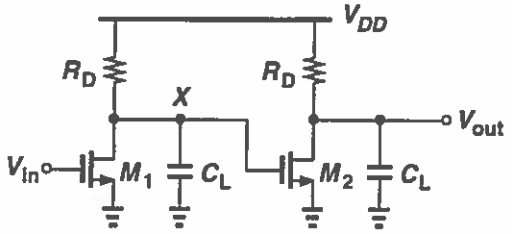

Fig. 3.1

a) Neglecting channel-length modulation and other capacitances, construct the Bode plot of V_{out}/V_{in} including both the magnitude and phase responses.

[8]

b) Annotate your plot with the following: (i) *Bandwidth*; (ii) *Phase margin*; (iii) *Gain Margin*.

[5]

c) Derive the transfer function of the circuit, substitute $s = j\omega$, and obtain an expression for $|V_{out}/V_{in}|$. Determine the -3dB bandwidth of the circuit.

[10]

d) Using your answers to parts (b) and (c), design the two-stage amplifier for a total voltage gain of 15 and $-3dB$ bandwidth of 1.8GHz. Assume each stage carries a bias current of 1mA, CL=40fF, and $\mu_n C_{ox} = 200\mu A/V^2$.

[7]