UNIVERSITY OF LONDON

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 1998

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER 1.6

HARDWARE

Tuesday, April 28th 1998, 2.00 - 3.30

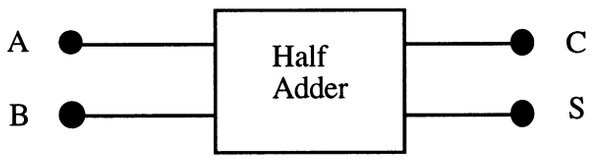
Answer THREE questions

For admin. only: paper contains 4 questions

1. Computer Arithmetic

a A half adder is defined by the following truth table

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1



Design a combinatorial logic circuit with inputs A and B and outputs S and C.

b A full adder has additionally a carry in. Show how two half adders and one OR gate can be connected to make a full adder.

c Using four AND gates and two half adders design a two bit multiplier with inputs A1 A0 and B1 B0 and outputs O3 O2 O1 and O0.

d Show how to connect up four of your two bit multipliers designed in part c to make a four bit multiplier.

The four parts carry, respectively, 20%, 25%, 25% and 30%, of the marks.

2. Sequential Recognition Circuit

A non-repeating sequence recogniser has a single input and a single output. It s output is to be zero normally, but should go to 1 whenever the input sequence 101 has been recognised. For example:

Input	0	1	0	1	1	1	0	1	0	1	0
Output	0	0	0	1	0	0	0	1	0	0	0

a Draw a the finite state machine that corresponds to the specification using the Moore machine convention that outputs are associated with states.

b Compile a state sequencing table in the following format:

Input	St	St+1	Q1	Q0	D1	D0
0						
0						
0						
0						
1						
1						
1						
1						

c Draw Karnaugh maps D0 and D1 and determine the minimum form of the state sequencing logic.

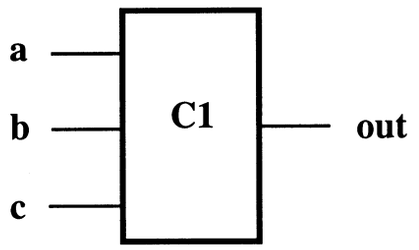
d Design a circuit that will give produce the correct output.

The four parts carry, respectively, 25%, 25%, 30% and 20%, of the marks.

Turn Over

3. Combinational Circuits

a A three-input one-output combinational circuit called C1 has the following Karnaugh map:



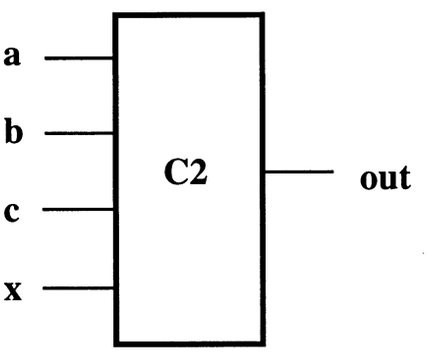
a \ bc	00	01	11	10
0	0	0	0	1
1	1	0	0	1

i) What is its truth table?

ii) Determine the simplest circuit that can be used for *C1* which may contain invertors, two-input AND, OR, NAND or NOR gates.

iii) Find the simplest circuit for *C1* which is built from two-input NAND gates only.

b A four-input one output combinational circuit, *C2* is built with inputs *x, a, b*, and *c*.



When x=0, the output of this new circuit, is exactly the same as the output of circuit C1 in terms of inputs *a,b,* and *c*. When x=1 the output is equal to c'.

i) Draw the Karnaugh map for this circuit.

ii) Determine the simplest circuit (fewest gates) that can be used for *C2* which may contain invertors, two three or four-input AND, OR, NAND or NOR gates.

iii) We find out that the input combinations 000 and 001 for inputs *a,b,c* are never used for circuit *C2*, and therefore, these can be considered "don't care" inputs. What is the simplest circuit for *C2* now?

c Build a two-to-one multiplexer from invertors, two-input AND, OR, NAND and/or NOR gates . Use this multiplexer and your circuit of part *a.ii* to design a circuit for *C2* using the functional design approach. Compare this circuit to the circuit of part b.ii. Comment on advantages and disadvantages of using the direct and the functional design approach for this example and in general.

The three parts carry, respectively, 30%, 40%, 30% of the marks.

4. Register Transfers

a Outline briefly the steps that are required to transfer a byte of data from one eight bit register to another. Indicate how the register data lines are connected and how the clock signals are applied.

b The figure overleaf shows part of a simple eight bit processor. Some of the instructions can be executed in one cycle, for example

AND B,A

in which the contents of register A is replaced by the logical bitwise AND of the contents of A and B. For this particular instruction determine the values that the controller should use for the multiplexer control inputs S0 S1 S2 S3, and the function selectors F0, F1, F2, F3, F4, and indicate which register clocks out of C0 C1 C2 will receive a pulse.

c Some of the instructions will require several clock cycles to execute. For example, the instruction:

MOV A,B

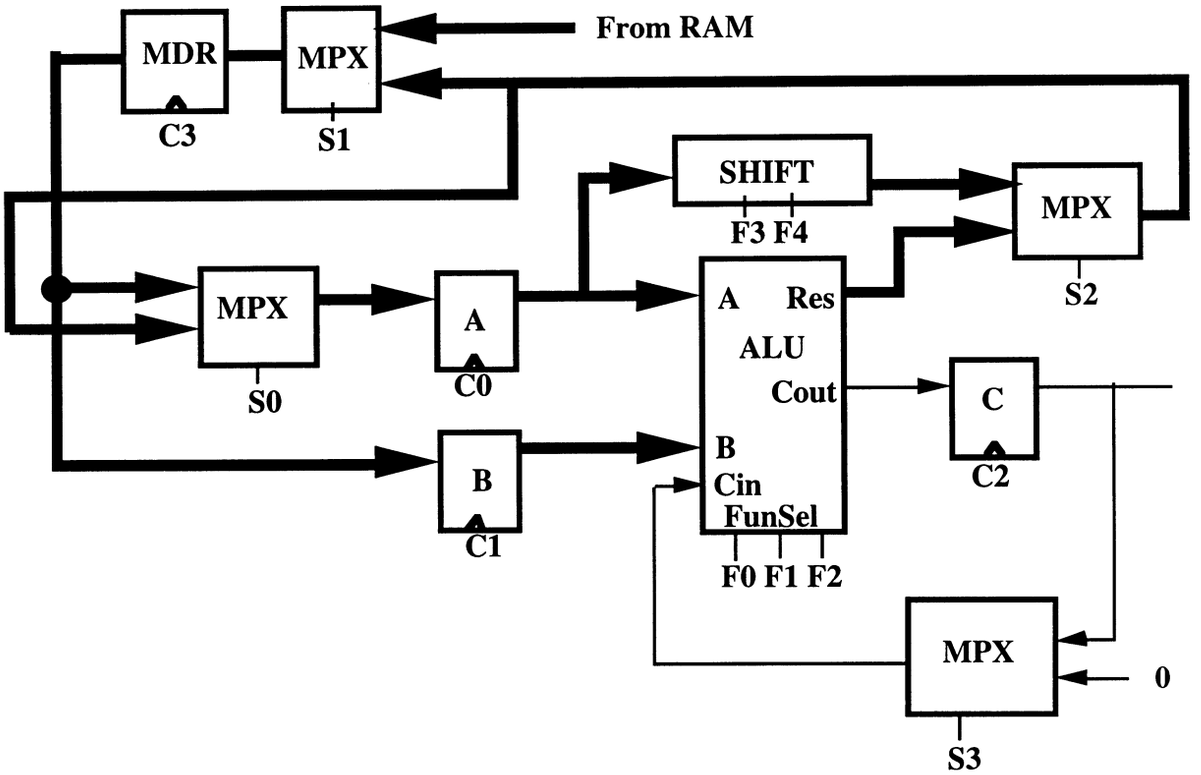
Moves the contents of register A to B, overwriting what was previously in Bbut preserving the contents of the MDR. Write down the required register transfers to implement this instruction, and determine the values of S0 to S3, F0 to F5 and C0 to C2 for all the necessary cycles.

d If there is the possibility of adding one more multiplexer where would you place it and why?

e Explain why register C has been included.

The five parts carry, respectively, 20%, 20%, 30%, 15%,15% of the marks.

Turn Over



Definitions

Clock gates:

C0 Controls Register A
C1 Controls Register B
C2 Controls the carry store
C4 Controls the Memory Data Register

Multiplexer Selection

S0 Selects the input to register A (0=MDR, 1=Result)
S1 Selects the input to the Memory Data Register (0=RAM,1=ALU/Shifter)
S2 Selects the source of the result (0=Function Generator, 1=Shifter)
S3 Selects the ALU Carry In (0=0, 1=C)

ALU Carry in selector

0 0
1 C

Function Selection

F0 ALU Function Select, bottom bit
F1 ALU Function Select, middle bit
F2 ALU Function Select, top bit
F3 Shifter function select, bottom bit
F4 Shifter function delect, top bit

ALU function:

000 0
001 B-A
010 A-B
011 AplusB
100 AeorB
101 A+B
110 A•B
111 -1

Shifter function

00 No Action
01 Shift Left
10 Logical Shift Right
11 Arithmetic Shift Right

End of Paper