Information for Candidates:

The following notation is used in this paper:

1. Unless explicitly indicated otherwise, digital circuits are drawn with their inputs on the left and their outputs on the right.
2. Within a circuit, signals with the same name are connected together even if no connection is shown explicitly.
3. The notation X2:0 denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0.
4. Signed binary numbers use 2's complement notation.

1. (a) *Figure 1.1* shows a decoder circuit `hex_to_BCD` that decodes a 4-bit binary number `d[3:0]` into two binary coded decimal (BCD) digits: `disp_1[6:0]` and `disp_0[6:0]`, which drive two 7-segment displays. The leftmost display (disp_1) should either be blank or shows the digit 1. For example, if `d[3:0] = 4'b0101`, the value 5 is displayed; if d[3:0] = 4'b1100, the value 12 is displayed.

The mapping of the 7-segment display inputs `seg[6:0]` to the segments is also shown in *Figure 1.1*.

(i) Design the decoder circuit in the form of a Verilog module with the following interface declarations:

```
Module  hex_to_BCD (dgt _1, dgt _0, in);
  Output [6:0]     dgt_1, dgt _0;
  Input  [3:0]     in;
```

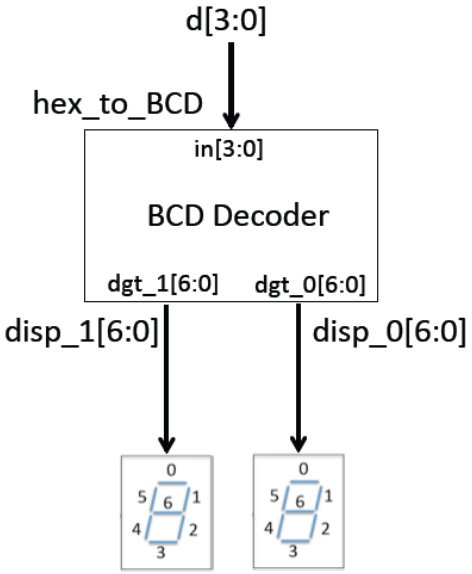
[6]

(ii) The decoder circuit is to be implemented on an Altera Cyclone III FPGA that consists of Logic Elements (LEs), each having a 4-input lookup table (LUT) and a D flip-flop.

Estimate and justify the number of LEs required to implement your decoder design.

[2]

Marks may be deducted for an unnecessarily complicated design.



seg[6:0]	digit
1000000	0
1111001	1
0100100	2
0110000	3
0011001	4
0010010	5
0000010	6
1111000	7
0000000	8
0010000	9
1111111	blank

Figure 1.1

(b) Consider the circuit shown in *Figure 1.2*. The propagation delay t_d of the inverters G1 to G3, and the clock-to-Q delay t_{cq} of the flip-flops FF1 and FF2, are in the range of 0.5ns to 1.0ns. The setup and hold times of the flip-flops FF1 and FF2 are 1.3ns and 1.1ns respectively. The clock to FF2 is driven through a delay element DLY with a delay of t_{dly}.

(i) Assuming that t_{dly} = 0ns and using only the setup time constraint, calculate the maximum operating frequency of the clock signal CLK.

[3]

(ii) Assuming that t_{dly} = 0ns, show that there is a hold time violation for FF1.

[3]

(iii) Delaying the clock to FF2 can eliminate the hold time violation. Show that the hold time violation is eliminated if the delay t_{dly} > 0.1 ns.

[2]

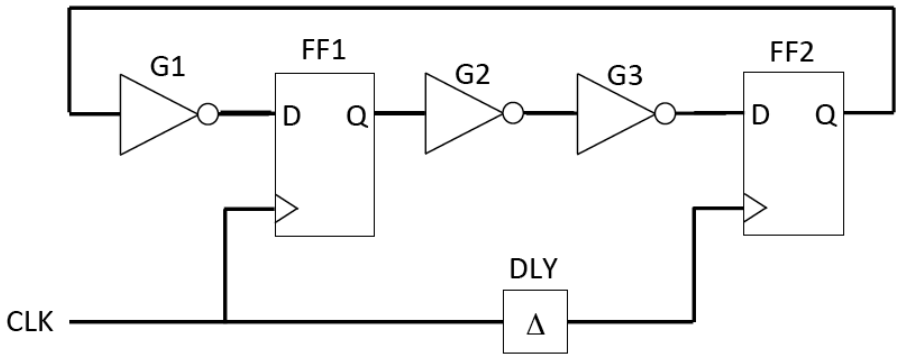


Figure 1.2

(c) *Figure 1.3* shows a 4k x 4 RAM chip with address bus ADR, data bus DATA, a write enable signal WR, a chip select signal CS and a synchronising clock CLK.

(i) Specify the size of the address and data buses for the RAM chip.

[2]

(ii) An 8k x 8 bit RAM module is required in a microprocessor system with a 16-bit address bus and an 8-bit data bus. The starting address of the RAM module is 16'h8000.

a) Design, in the form of a schematic diagram, a circuit using four 4k x 4 RAM chips shown in Figure 1.3 to implement the 8k x 8 RAM module.

[4]

b) Derive the Boolean expression for the chip select signals required for each of the 4k x 4 RAM chip.

[2]

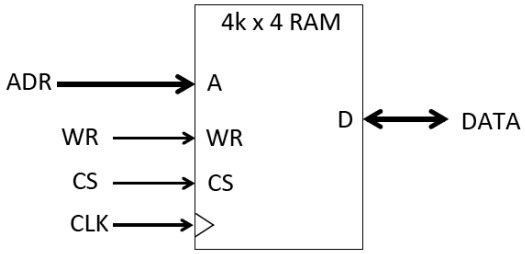


Figure 1.3

(d) *Figure 1.4* shows the state diagram of a finite state machine (FSM) with two input signals X and Y, and one output signal Z, driven with a clock signal CLK. Changes in X and Y are synchronised on the falling edges of CLK; changes in state and Z are synchronised on the rising edges of CLK.

(i) Complete the timing diagram shown in *Figure 1.5* given that the FSM is initially in state A.

[4]

(ii) Specify in Verilog HDL a design of this FSM using one-hot state encoding. In order to reduce the time you need to answer this question, you are only required to show the Verilog code for the module interface, declarations, state definitions, and for the part of the state machine specification relevant to transitions from state A to other states.

[4]

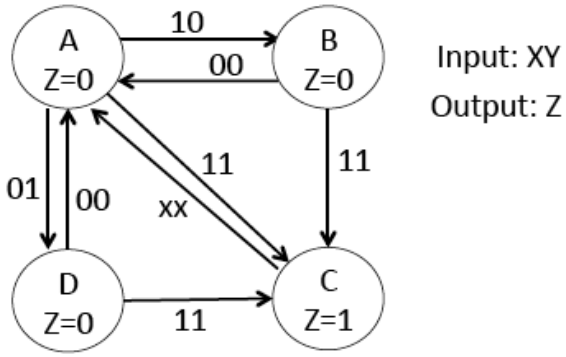


Figure 1.4

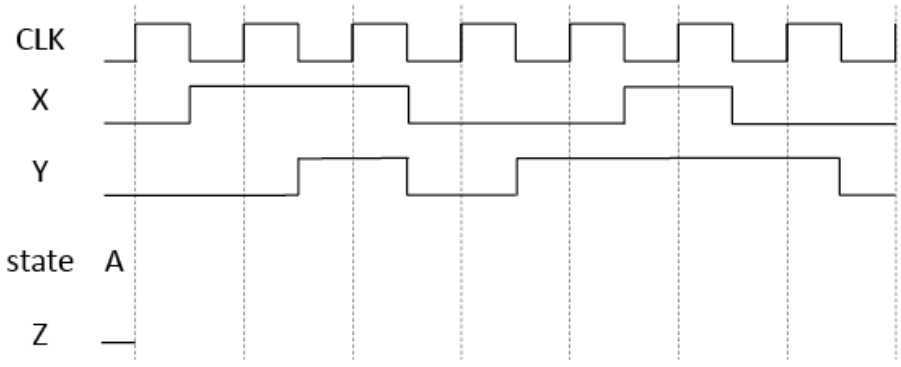


Figure 1.5

(e) *Figure 1.6* shows the schematic diagram of a resistor network DAC consisting of 1025 identical resistors R_0 to R_{1024}, 1024 analogue switches SW_0 to SW_{1023}, an operational amplifier and a digital decoder circuit. The input to the DAC is IN[9:0] and the output is V_{out}.

(i) Describe the principle of operation of this DAC and explain the function of the decoder circuit. (You are not required to provide a design for the decoder circuit.)

[2]

(ii) Derive a mathematical relationship between Vout and IN[9:0].

[2]

(iii) What is the range and resolution of the DAC?

[2]

(iv) Assuming that IN[9:0] = 10'b0100011010, which switch will be closed? What is expected voltage at Vout?

[2]

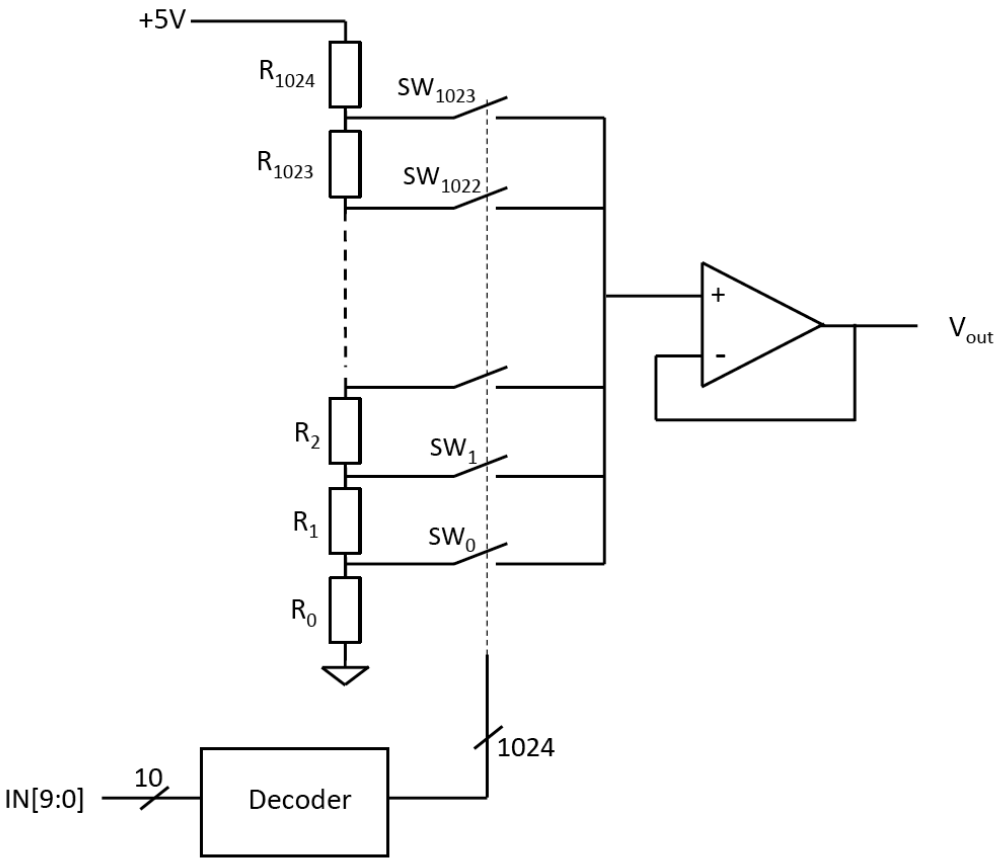


Figure 1.6

2. *Figure 2.1* shows a clock divider circuit consisting of a 3-bit adder M1, a 4-bit register M2 and a 4-bit counter M3. The counter M3 increments on the rising edge of the clock CLK if Q3 is high. The clock frequency is 50MHz.

   (a) Assuming that the binary number N[2:0] has the value 3'b011 and that the register M2 initially has the value of 4'b0100, complete the timing diagram shown in *Figure 2.2*, demonstrating the operation of the circuit spanning 10 clock cycles.

   [10]

   (b) Explain what happens if the initial value of the register is not 4'b0100?

   [5]

   (c) What is the average frequency of Q3 and X3 given that N[2:0] = 3'b011?

   [5]

   (d) This circuit is implemented on an Altera Cyclone III FPGA, which consists of Logic Elements (LEs), each with a 4-input lookup table (LUT) and a D-type flip-flop. Estimate with justifications the number of LEs required to implement this circuit.

   [5]

   (e) Assume that the LUT has a worst-case delay of 250ps and the D flip-flop has a clock-to-output delay of 100ps, and a setup and hold time of 80ps and 45ps respectively. Estimate the maximum frequency of CLK for which the circuit will operate correctly.

   [5]

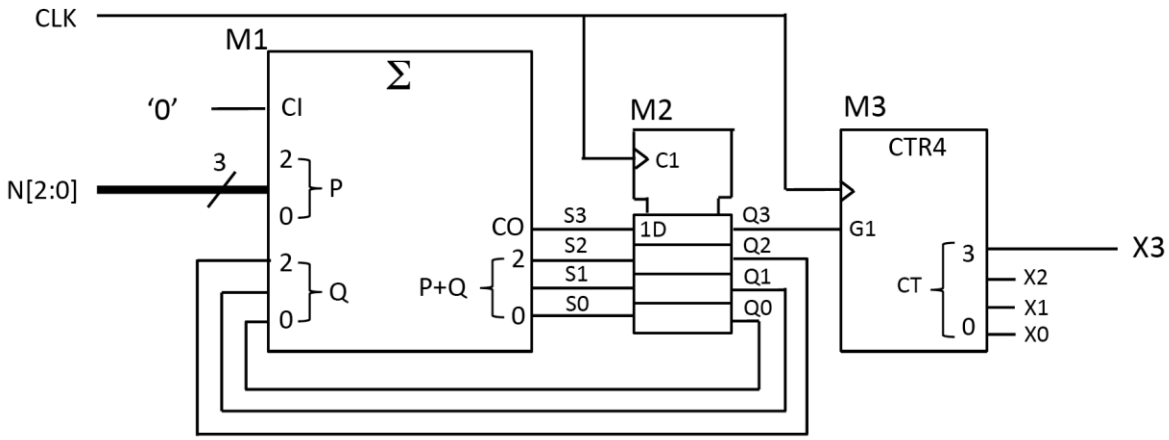


Figure 2.1

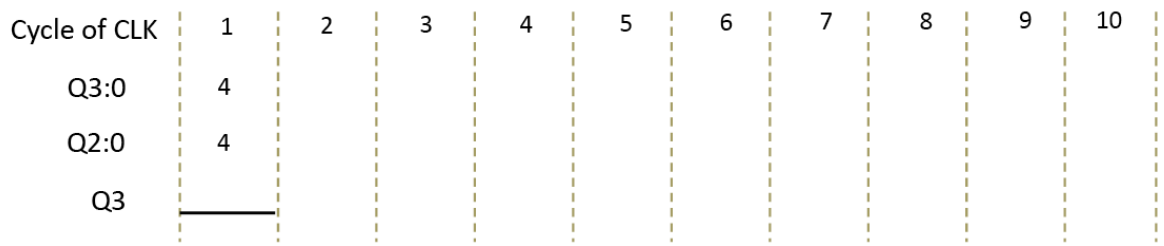


Figure 2.2

3. *Figure 3.1* shows an interface circuit to control the transfer data from System A to System B. The circuit consists of a register R1 and a finite state machine M1 whose state diagram is as shown.

The transfer protocol from A to R1 is as follows: (i) when Data_A is valid and A asserts REQ_A (i.e. sets to 1); (ii) M1 asserts GNT_A when R1 is able to accept new data; (iii) A de-asserts REQ_A; (iv) M1 de-asserts GNT_A to indicate that data is successfully stored in R1. M1 will not assert GNT_A until B has read previous data in R1.

The transfer of data from R1 to B happens in a similar manner: (i) when Data_B is valid M1 asserts REQ_B; (ii) B asserts GNT_B when it is ready to read new data; (iii) M1 de-asserts REQ_B; (iv) B de-asserts GNT_B to indicate that the new data is read.

The signal LD goes high to enable loading of the register R1 on the following rising edge of the clock signal CLK. Systems A and B are synchronised to the falling edge of the clock CLK, while the interface circuit is synchronised to the rising edge of CLK.

(a) Complete the timing diagram of *Figure 3.2* by showing the sequence of states that the state machine follows and the waveform of the signals LD, GNT_A, REQ_B and Data_B. The vertical lines in the figure denote the rising edges of CLK and the state machine is initially at state 0.

[15]

(b) Draw the timing diagram for the case where the transfer of data from A to B is at the maximum rate. State any assumption used.

[15]

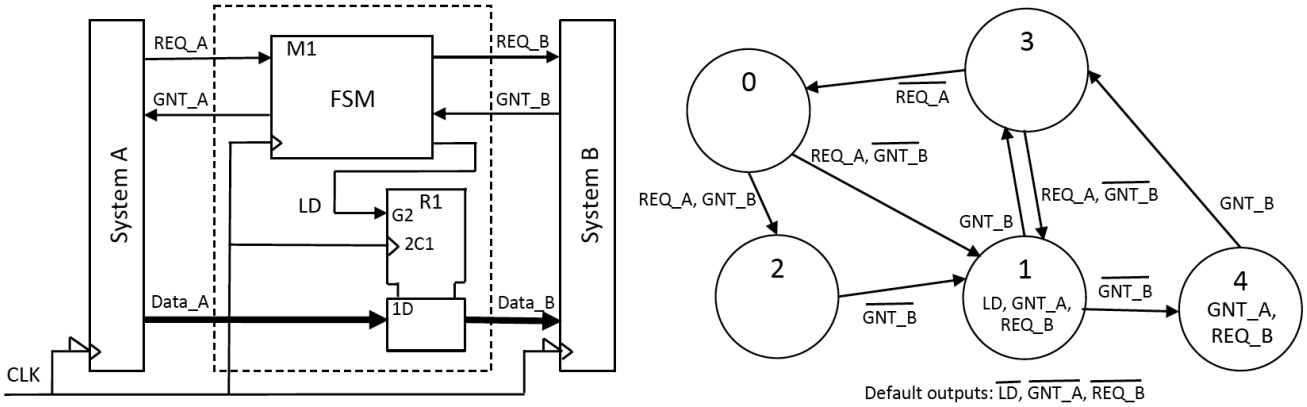


Figure 3.1

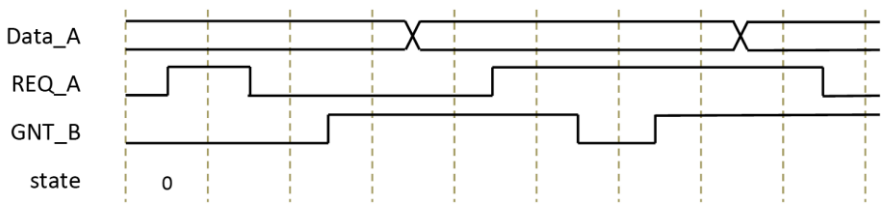


Figure 3.2