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IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2011

MSc and EEE PART III/IV: MEng, BEng.and ACGI

POWER ELECTRONICS

Tuesday, 3 May 2:30 pm

Time allowed: 2:00 hours

There are FOUR questions on this paper.

Answer THREE questions.

All questions carry equal marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : T.C. Green, P.D. Mitcheson
Second Marker(s) : P.D. Mitcheson, T.C. Green

1.

a) Figure 1.1 shows closed-loop controlled switch mode power supply (SMPS).

i) Describe the purpose of the items labelled A and B. [3]

ii) Describe the key design considerations in choosing the inductor, capacitor and switching frequency. [5]

iii) Describe the key consideration in choosing the control loop compensator transfer function, C. [2]

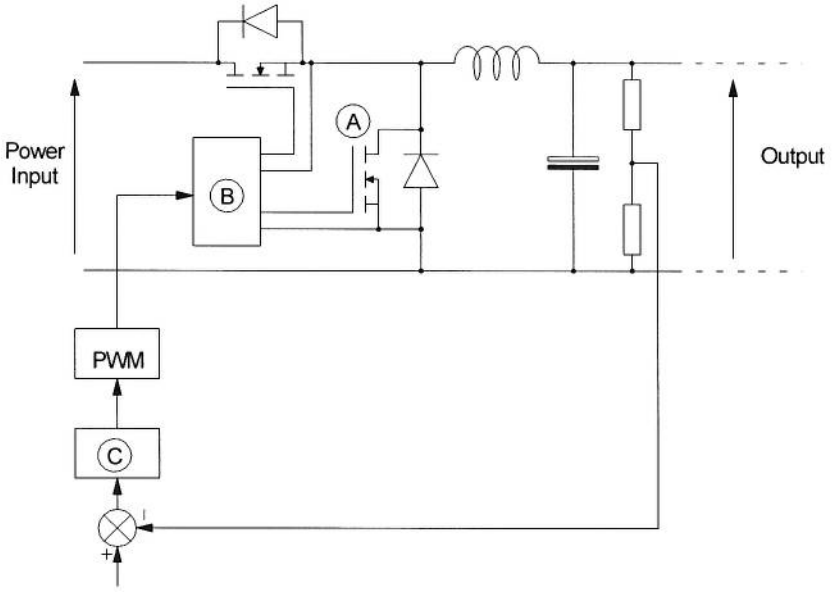


Figure 1.1 A double-switched buck SMPS

b) A transformer isolated flyback SMPS is to be designed for use in discontinuous mode. It will operate from 400 V input and is required to provide 100 W at a 48 V output. The switching frequency has been selected as 40 kHz.

i) Explain why 0.4 is a good choice of nominal duty-cycle for discontinuous operation of flyback SMPS. [2]

ii) Choose a value of L_1 assuming the nominal duty cycle is 0.4. [4]

iii) Choose a suitable value of L_2. [2]

iv) Specify the effective series resistance of the output capacitor to achieve an output voltage ripple of 100 mV or less. [2]

2.

a) Distinguish between the terms (i) power factor; (ii) displacement factor and (iii) distortion factor. [5]

b) A rectifier has been tested on 235 V(RMS) input. The power meter recorded that it drew 900 W with an RMS current of 8 A. The meter also record the fundamental component of current as 5 A(RMS).

Calculate the

i) apparent power; [1]

ii) power factor; [1]

iii) distortion factor and [1]

iv) displacement factor. [1]

c) Sketch the circuit of a single-phase rectifier circuit capable of exercising control over the input current wave-shape. Explain how the circuit is controlled. [6]

d) Explain the difference in instantaneous power exchange with the DC-link capacitor for single-phase and three-phase rectifiers. For a wave shape controlled rectifier, explain why this feature requires the bandwidth of the voltage control loop to be set to a low value for the single-phase case. [5]

3.

a) i) Sketch a 3-phase inverter. [2]

ii) State the relationship between DC-link voltage and the maximum phase and line voltages that an inverter can create. [2]

iii) Discuss the spectrum and the role of an output-side filter of an inverter. [3]

iv) The DC-link of an inverter is to be provided by rectifying a standard 3-phase 50Hz supply. Discuss why the rectifier may need to be bi-directional and what circuit would be used for the bi-directional case. [3]

b) The nameplate of a 1-pole-pair induction machine gives the following basic information for its operation on a fixed frequency supply. This information is taken to represent its maximum or rated operation for the conditions given.

Phase Voltage 230 V

Frequency 50 Hz

Rated Speed 2,900 rpm

Rated Power 7.5 kW

Determine the following.

i) The rated torque and the slip-speed limit (in rad/s) at which that occurs. [4]

ii) The air-gap flux linkage present under rated conditions (an approximate answer is sufficient). [2]

iii) The frequency (corrected for slip) and approximate stator voltage required to operate at rated torque at 5,400 rpm. [4]

4. Figure Q4.1 shows a cross section through a double-diffused power MOSFET, Figure 4.2 shows a MOSFET switching a diode clamped inductive load.

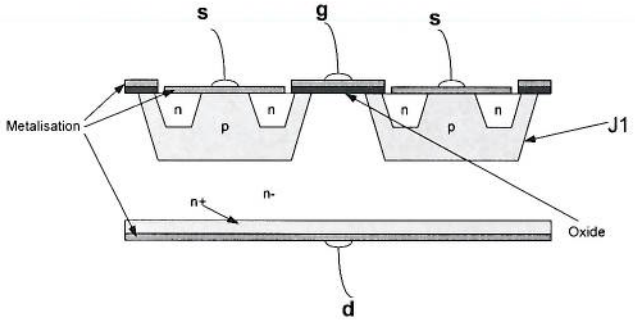


Figure 4.1 Cross section through power MOSFET

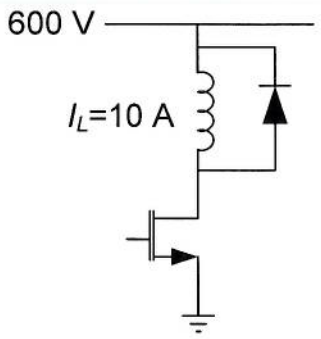


Figure 4.2 Diode clamped inductive load circuit

a) Explain why power semiconductors are manufactured using many tessellated individual cell structures rather than one single large device and why power devices tend to be manufactured so that conduction occurs between top and bottom of the wafer rather than across the surface (as in an integrated circuit). [4]

b) With reference to Figure 4.1 and using an equivalent circuit diagram of a power MOSFET, explain why the rate of rise of the drain-source voltage is limited when the device turns off. [5]

c) The MOSFET used in the circuit of Figure 4.2 has an intrinsic *dv/dt* limit at turn-off of 20 V/ns due to the device internal structure. However, in order to comply with EMC requirements, it is necessary to reduce the value of dv/dt to 10 V/ns. Design a suitable turn-off snubber circuit applied to Figure 4.2 in order to limit *dv/dt* to 10 V/ns. [5]

d) A designer is considering changing the MOSFET used in the circuit of Figure 4.2. In the proposed replacement device, the per-cell capacitance of junction J1 (Figure 4.1) is 10 pF and the equivalent resistance of the *p* diffusion between the source metallisation and J1 is 10 Ω. In order to comply with the maximum *dv/dt* limit of 10 V/ns set by EMC requirements, does this device require a snubber? [6]

Answers 2011

1.

a) Figure 1.1 shows closed-loop controlled switch mode power supply (SMPS).

i) Describe the purpose of the items labelled A and B. [3]

ii) Describe the key design considerations in choosing the inductor, capacitor and switching frequency. [5]

iii) Describe the key consideration in choosing the control loop compensator transfer function, C. [2]

[Interpretation of material in notes]

i) [3 marks for basic descriptions]
A – Rectifier Mosfet: in low voltage design cases, the diode voltage drop can be a significant adverse factor in efficiency. Using a Mosfet path has a much lower voltage drop and lower power loss. This requires the rectifier Mosfet to be switched in anti-phase with the main Mosfet.
B – Gate driver: Two tasks (1) Under-lap delay time: the main and rectifier Mosfet would, if on or partially on together, form a short circuit across the input. To ensure one is safely off before the other turns on, a short delay is inserted in the turn-on edge of he anti-phase signals. (2) Main Mosfet has a source that is not ground referenced. This requires level shift of the gate drive signal and a floating power supply (via boost-strap capacitor perhaps).

ii) [3 marks for basic description; 2 marks for trade-offs and compromises in choosing control compensator and switching frequency]

Inductor chosen to be large enough to keep current ripple small (and subsequent voltage ripple) but value also dictates size/cost
Capacitor chosen to achieve low voltage ripple with ESR normally being dominant concern.
PWM with frequency chosen as trade-off between switching power loss and passive component size.

iii) [2 marks]
D – Control loop compensator: chosen to achieve well damped poles from the LC plant; a good steady-state error and a roll-off of closed loop gain beneath the operating frequency of the modulator.

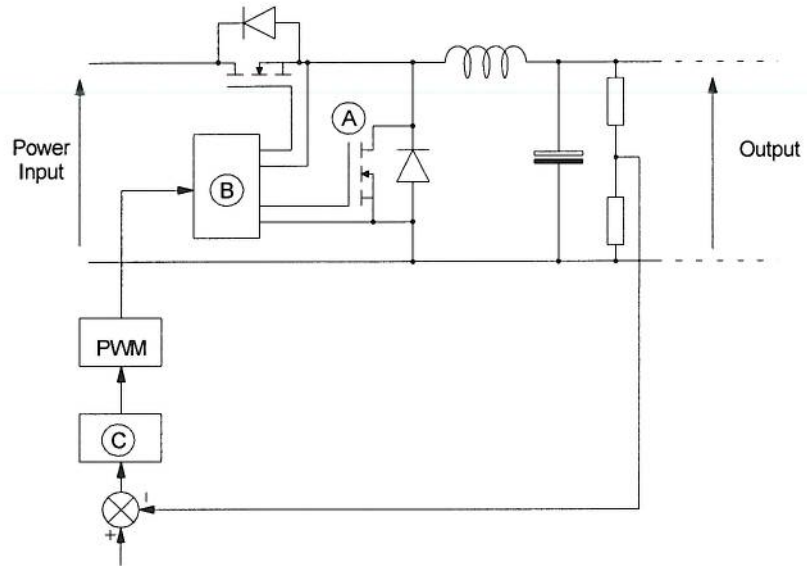


Figure 1.1 A double-switched buck SMPS

b) A transformer isolated flyback SMPS is to be designed for use in discontinuous mode. It will operate from 400 V input and is required to provide 100 W at a 48 V output. The switching frequency has been selected as 40 kHz.

i) Explain why 0.4 is a good choice of nominal duty-cycle for discontinuous operation of flyback SMPS. [2]

ii) Choose a value of L_1 assuming the nominal duty cycle is 0.4. [4]

iii) Choose a suitable value of L_2. [2]

iv) Specify the effective series resistance of the output capacitor to achieve an output voltage ripple of 100 mV or less. [2]

[Interpretation of notes]
i) A nominal duty cycle of 0.5 is a good choice for continuous or discontinuous mode because high nominal duty-cycles give rise to a lower value of N2 and hence a higher reflected voltage on the primary and higher voltage blocking capability needed in the switch. Lower duty cycles mean that the peak current in the primary and switch have to be increased to carry the same power. So, 0.5 is a good compromise between current and voltage rating of the switch. The nominal duty-cycle for a flyback converter in discontinuous operation should be somewhat less than 0.5 to ensure a period of non-conduction so 0.4 is a good choice.

[Calculation based on manipulation of known equations]
ii) [1 mark of sensible duty-cycle; 3 marks for corresponding inductor value]
At 40 kHz, the energy per cycle is

$$E_C = \frac{P_O}{f_{Sw}}$$

The energy stored and released from the core each cycle is

$$E_C = \tfrac{1}{2} L_1 \hat{i}_1^2 = \tfrac{1}{2} L_1 \left(\frac{V_1}{L_1} \frac{\delta}{f_{Sw}} \right)^2 = \tfrac{1}{2} \frac{1}{L_1} \left(\frac{V_1 \delta}{f_{Sw}} \right)^2$$

So, L_1 can be found.

$$L_1 = \tfrac{1}{2} \frac{V_1^2 \delta^2}{f_{Sw} P_O} = \frac{400^2 \times 0.4^2}{2 \times 40 \times 10^3 \times 100} = 3.2mH$$

iii)

L2 is found from the turns-ratio based on voltage ratio. Could also calculate from need to remain discontinuous.

$$L_2 = L_1 \left(\frac{N_2}{N_1} \right)^2 = L_1 \left(\frac{V_2}{V_1} \frac{\delta}{\delta_{diode}} \right)^2 = 3.2m \times \left(\frac{48}{400} \frac{0.4}{0.4} \right)^2 = 0.046mH$$

iv)

Calculate I2 peak when carrying full power and then choose ESR

$$\hat{i}_1 = \frac{V_1}{L_1} \frac{\delta}{f_{Sw}} = \frac{400}{3.2m} \times \frac{0.4}{40k} = 1.25A$$

$$or \quad \hat{i}_1 = \frac{P}{V_1} \frac{2}{\delta} = \frac{100}{400} \times \frac{2}{0.4} = 1.25A$$

$$\hat{i}_2 = \hat{i}_1 \frac{N_1}{N_2} = 1.25 \times \frac{400}{48} = 10.42A$$

$$R_{ESR} = \frac{\Delta v_O}{\hat{i}_2} = \frac{100m}{10.42} = 9.6m\Omega$$

2.

a) Distinguish between the terms (i) power factor; (ii) displacement factor and (iii) distortion factor. [5]

[Book work]

(i) Power factor is the ratio of real power (average of instantaneous power) to apparent power (product of RMS voltage and RMS current. In the case of a sinusoidal voltage and a distorted current it can be expressed as the product of the displacement factor and the current distortion factor.

(ii) Displacement factor is the cosine of the angle difference between the fundamental component of current and the voltage.

(iii) Distortion Factor is the ration of the fundamental current (expressed in RMS terms) to the RMS current.

b) A rectifier has been tested on 235 V(rms) input. The power meter recorded that it drew 900 W with an RMS current of 8 A. The meter also record the fundamental component of current as 5 A(rms).

Calculate the

i) apparent power; [1]
ii) power factor; [1]
iii) distortion factor and [1]
iv) displacement factor. [1]

[Manipulation of standard expressions]

(i)

$$S = V_{RMS} I_{RMS} = 235 \times 8 = 1,880 VA$$

(ii)

$$PF = \frac{P}{S} = \frac{900}{1880} = 0.479$$

(iii)

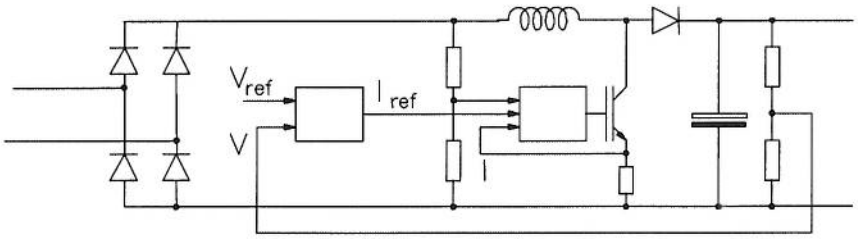
$$\mu = \frac{I_{1RMS}}{I_{RMS}} = \frac{5}{8} = 0.625$$

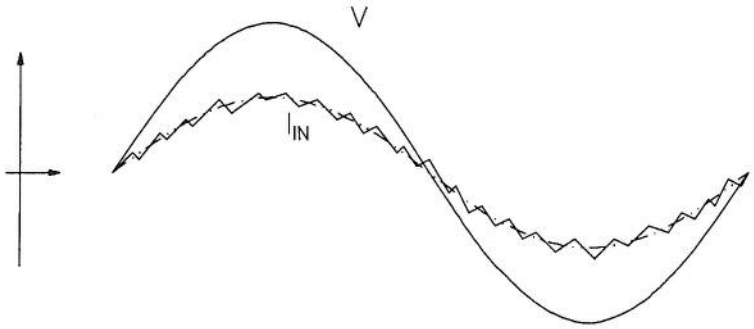
(iv)

$$\cos(\phi_1) = \frac{PF}{\mu} = \frac{0.479}{0.625} = 0.766$$

c) Sketch the circuit of a single-phase rectifier circuit capable of exercising control over the input current wave-shape. Explain how the circuit is controlled. [6]

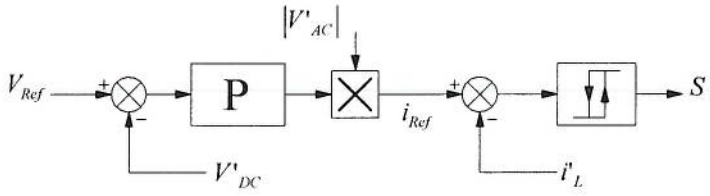
[Book work]
A boost type SMPS can be arranged to draw a controlled current from a varying voltage. A diode bridge is used to rectify the AC voltage and a control loop set to force the current to be a full wave rectified sinewave also (a simple sinewave will be drawn from the AC supply). The magnitude of the sinewave is set by a second controller according to the error between the DC output voltage and its reference value.

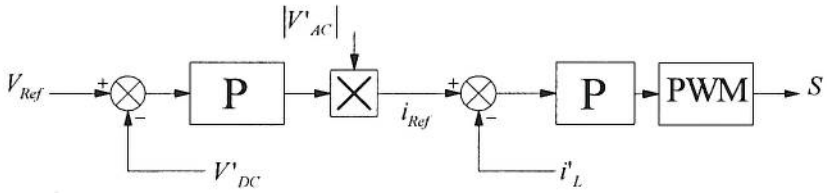




Two variants of control exist. The first uses a hysteresis controller for the current loop and results in fast response but a varying switching frequency. The second uses fixed-frequency pwm. The spread spectrum resulting from a varying switching frequency can make filter design difficult but it does have the advantage of spreading emissions thinly over a range rather than producing high level emissions concentrated at particular frequencies.

The control loop for the output voltage must be designed with a limited bandwidth typically around 5 Hz. The energy drawn from a single-phase supply will vary at twice line frequency even if sinusoidal current wave-shape is achieved. Thus, there will be an unavoidable output voltage ripple at twice line frequency which the control loop should not attempt to reject.


$|V'_{AC}|$
V_{Ref}
P
i_{Ref}
S
V'_{DC}
i'_L


$|V'_{AC}|$
V_{Ref}
P
i_{Ref}
P
PWM
S
V'_{DC}
i'_L

d) Explain the difference in instantaneous power exchange with the DC-link capacitor for single-phase and three-phase rectifiers. For a wave shape controlled rectifier explain why this feature requires the bandwidth of the voltage control loop to be set to a low value for the single-phase case. [5]

[Bookwork and interpretation]
The DC output of a rectifier supplies a constant instantaneous power (constant voltage and constant current). A single phase AC input supplies an instantaneous power that is the product of a sinusoidal voltage and a sinusoidal current. The result is a constant term plus a double frequency term. The constant term is passed to the output and the double frequency term is exchanged with the DC-link capacitor which must be rated for this duty and large enough to avoid a large double frequency voltage ripple.

In the three-phase case, the double frequency terms of the three phases sum to zero such that the instantaneous power of the three phase set is constant and there is not significant power exchange with the DC-link capacitor.

When closing a control loop on the DC-link capacitor voltage of a single-phase rectifier it is important not to have the controller respond to the double frequency term and attempt to correct it since it can not be corrected and attempting to do so will distort the input AC waveform. For that reason a filter is added to the control loop to include a dominant pole well blow this frequency.

3.

a) i) Sketch a 3-phase inverter. [2]

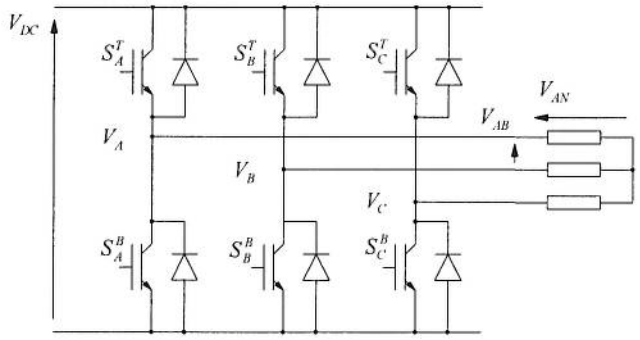
ii) State the relationship between DC-link voltage and the maximum phase and line voltages that an inverter can create. [2]

iii) Discuss the spectrum and the role of an output-side filter of an inverter. [3]

iv) The DC-link of the inverter is to be provided by rectifying a standard 3-phase 50Hz supply. Discuss why the rectifier may need to be bi-directional and what circuit would be used for the bi-directional case. [3]

[Book work]

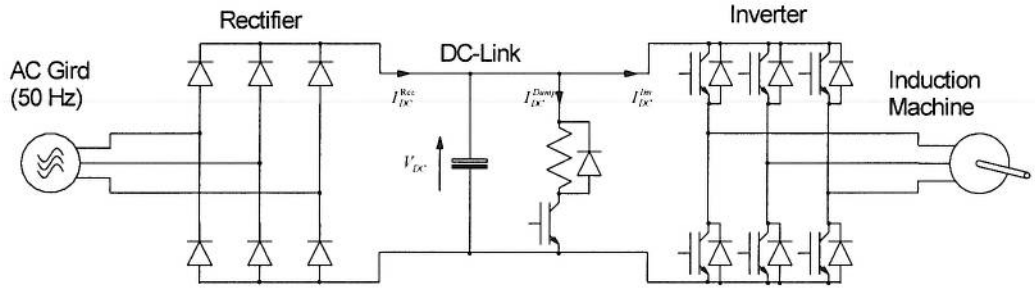
i)



ii) $\hat{V}_{ph} = \frac{1}{2}V_{DC}$ $V_{ph}(rms) = \frac{1}{2\sqrt{2}}V_{DC}$ $V_{line}(rms) = \frac{\sqrt{3}}{2\sqrt{2}}V_{DC}$

iii) *The phase voltage created by one limb of an inverter contains the desired fundamental frequency term plus a DC offset of half the DC link voltage plus sideband and carrier terms for each integer multiple of the switching frequency. The DC offset and carrier of the odd switching multiples are common-mode and are not of concern in three-phase three-wire systems. The sidebands around the switching frequency multiples may be of no consequence if the load is inductive and the frequency high because of the natural filtering of the load. If this is not true then a passive LC filter will need to be added to attenuate these terms.*

iv) *Some classes of load can regenerate: the common example is variable speed AC motor which is sometimes decelerated by applying reverse torque. With reverse torque and forward rotation, power is transformed from mechanical to electrical form and returned through the inverter to the DC-link where it will tend to increase the voltage on the DC link capacitor. If the energy return is significant then it must be removed to avoid excessive voltage rise. If the rectifier supplying the DC-link is bi-directional then power can be passed to the AC supply. An active rectifier is needed which is in practice another inverter bridge that forms a back-to-back pair. (Diagram not needed but could be used).*



(b) The nameplate of a 1-pole-pair induction machine gives the following basic information for its operation on a fixed frequency supply. This information is taken to represent its maximum or rated operation for the conditions given.

Phase Voltage 230 V
Frequency 50 Hz
Rated Speed 2,900 rpm
Rated Power 7.5 kW

Determine the following.

(i) The rated torque and the slip-speed limit (in rad/s) at which that occurs. [4]

Both quantities can be assessed at the nameplate data point and are then more generally true. For a 2-pole-pair machine supplied at 50Hz the sync speed is 3,000 rpm.

$$\omega_{Slip}^{Max} = \omega_S - \omega_R = \frac{2\pi 50}{1} - 2900 \times \frac{2\pi}{60} = 10.47\ rad/s$$

$$T^{Max} = \frac{P}{\omega_R} = \frac{7500}{2900 \times \frac{2\pi}{60}} = 24.70\ Nm$$

(ii) The air-gap flux linkage present under rated conditions (an approximate answer is sufficient). [2]

Approximate by ignoring stator voltage drop.

$$\psi_{AG}^{Max} \approx \frac{|V_S|}{\omega_E} = \frac{230}{2\pi 50} = 0.732\ Wb$$

(iii) The frequency (corrected for slip) and approximate stator voltage required to operate at rated torque at 5,400 rpm. [4]

With the correction for slip

$$f_E = \frac{P\omega_S}{2\pi} = \frac{P(\omega_R + \omega_{Slip})}{2\pi} = \frac{1\times(5400\times\frac{2\pi}{60}+10.47)}{2\pi} = 90 + 1.66 = 91.66\ Hz$$

Approximate voltage by ignoring stator voltage drop.

$$|V_S| = \omega_E \psi_{AG}^{Max} = 2\pi \times 91.66 \times 0.732 = 421.6\ V$$

4. Figure 4.1 shows a cross section through a double-diffused power MOSFET (left) and a MOSFET switching a diode clamped inductive load (right).

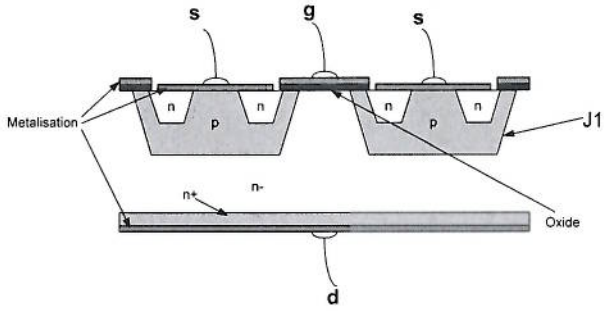


Figure 4.1 Cross section through power MOSFET

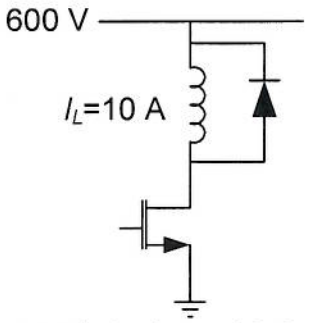


Figure 4.2 Diode clamped inductive load circuit

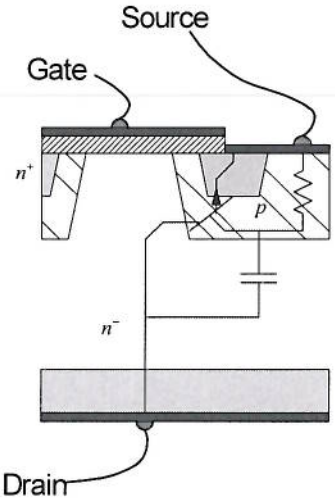
a) Explain why power semiconductors are manufactured using many tessellated individual cell structures rather than one single large device and why power devices tend to be manufactured so that conduction occurs between top and bottom of the wafer rather than across the surface (as in an integrated circuit. [4]

[bookwork]

- *Power devices must block high voltage and conduct high current*
- *Voltage blocking requires significant length and high currents requires significant area – which leads to large volume*
- *Therefore allowing conduction through the bulk rather than just on the surface is a more efficient use of Silicon as the depletion layer can extend into the thickness of the wafer*
- *The cells are arranged so maximise the individual gate area because the channel resistance is a significant limiting factor to on state resistance. Thus we must maximise gate width. The choice is between a very wide device (along a 1D extrusion) or making the device up of tessellated cells to make it more square*

b) With reference to Figure 4.1 and using an equivalent circuit diagram of a power MOSFET, explain why the rate of rise of the drain-source voltage is limited when the device turns off. [5]

The power MOSFET has a parasitic MOSFET structure built in as shown in the diagram below:

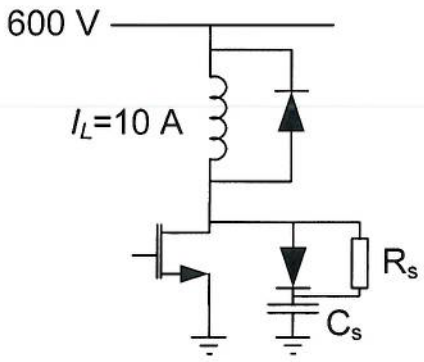


The combined resistance of the n- drift region and the p region form an RC circuit with the depletion capacitance of the pn- junction. If the device is quickly turned off, the drain voltage rapidly increases with respect to the source and thus current flows into p region through the charging capacitance and increases the potential of that region. This is equivalent to increasing the voltage on the base of the parasitic BJT, allowing current to flow through the BJT and limiting the rate of rise of voltage of the MOSFET.

c) The MOSFET used in the circuit of Figure 4.2 has an intrinsic dv/dt limit at turn-off of 20 V/ns due to the device internal structure. However, in order to comply with EMC requirements, it is necessary to reduce the value of dv/dt to 10 V/ns. Design a suitable turn-off snubber circuit applied to Figure 4.2 in order to limit dv/dt to 10 V/ns. [5]

[This is a standard question on snubbers although the students normally think of snubbers as a loss reduction mechanism, rather than a dv/dt limiter.]

The standard turn-off snubber (required for limiting a rate of rise of voltage across the device) is shown below and the value of R and C must now be chosen



The fastest rate of rise of voltage across the MOSFET occurs when the MOSFET has turned off fully (i.e. is not conducting current anymore) and the entire load current flows into the snubber capacitor. Thus, we have:

$$C_s \frac{dV_s}{dt} = I_L$$

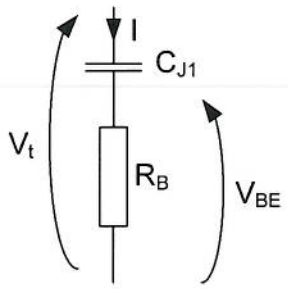
Thus, Cs = 10/1e9 = 10nF

The choice of R_s cannot be calculated exactly as not enough information about the circuit operation is given - but the students should state that R can be chosen by allowing a 5 time constants of the RC to occur in the period when the MOSFET is turned on to allow the snubber to reset

d) A designer is considering changing the MOSFET used in the circuit of Figure 4.2. In the proposed replacement device, the per-cell capacitance of junction J1 (Figure 4.1) is 10 pF and the equivalent resistance of the *p* diffusion between the source metallisation and J1 is 10 Ω. In order to comply with the maximum dv/dt limit of 10 V/ns, does this device require a snubber? [6]

This question is simple but is not something that the students have seen before. The maximum dv/dt is set by the voltage across the resistance of the p-region, i.e. the base-emitter voltage of the BJT.

Thus, we require that the voltage across this resistor stays below approximately 0.7 in order not to turn the BJT on. The simple equivalent RC circuit is:



And thus:

$$I = C_{J1}\frac{dV_{CJ1}}{dt} = \frac{V_{BE}}{R_B}$$

If we are to keep V_{BE} constant at the worst case value of at 0.7, then $dVC_{J1}/dt = dV_t/dt$

And thus:

$$\frac{dV_t}{dt} = \frac{0.7}{R_B C_{J1}}$$

Therefore, dv/dt max for this device (as limited internally) is approximately 7 V/ns, meaning that this device does not require a snubber to meet the 10 V/ns maximum switching speed..