IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2011

EEE PART II: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 2

Thursday, 2 June 2:00 pm

Time allowed: 2.00 hours

There are THREE questions on this paper.

ALL questions are compulsory.
Question 1 carries 40% of the marks and Questions 2 and 3 carry 30% each.

Any special instructions for invigilators and information for candidates are on page 1.

Basic expressions for voltage gain, input and output resistance for single stage amplifiers are given on the last page.

Examiners responsible
First Marker(s): T.G. Constandinou, T.G. Constandinou
Second Marker(s): K. Harris, K. Harris

1. This question consists of 10 brief items. Each item can be answered in a few words or a short paragraph with use of a diagram and/or expression where helpful. Please answer all sub-questions, which carry equal marks.

a) List four types of *non-ideal behaviour* in a real (as oppose to ideal) operational amplifier. [4]

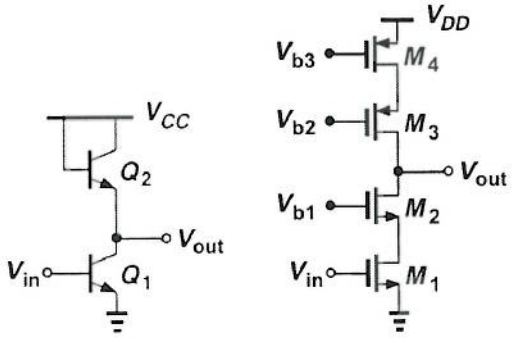
b) List four benefits of applying *negative feedback* to analogue circuits. [4]

c) Explain why *device mismatch* poses a challenge in analogue design. Give two techniques in analogue layout design to improve device matching. [4]

d) Describe what is meant by the *body effect* and explain how circuits can be designed to eliminate/reduce this. [4]

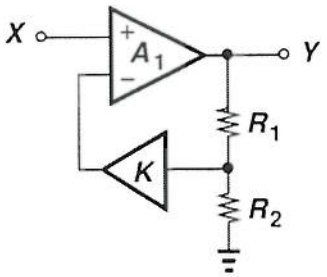
e) With the aid of a diagram describe *Miller's Theorem* and explain where this is useful. [4]

f) Derive expressions (by inspection) for the *voltage gain* of the circuits shown below (assuming $\lambda \neq 0$, i.e. $r_O < \infty$). State any assumptions made if simplifying the expressions. [4]



(i) (ii)

g) Calculate the *loop gain* and *closed-loop gain* of the circuit shown below. Assume the op-amp exhibits an open-loop gain of A_1, but is otherwise ideal. [4]

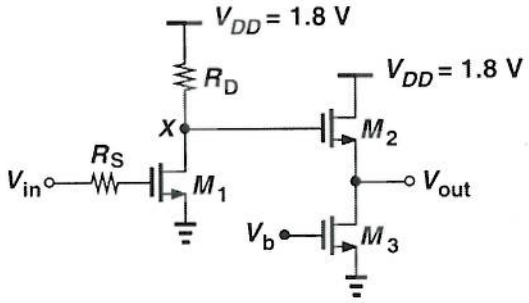


h) Explain what is meant by a *cascode* and how this technique can be applied to improve amplifier performance. [4]

i) Explain which amplifier topology (single stage) you would use as a *voltage buffer*. Justify your reasoning. [4]

j) Design a 5KΩ *integrated* polysilicon resistor (i.e. calculate W and L) assuming a maximum current of 0.5mA (given $R_{poly}=8\Omega/\square$ and $J_{max}=0.1\text{mA}/\mu\text{m}$). [4]

2. The circuit shown below is a two stage amplifier, specifically a common source stage followed by a source follower stage. Assume $\lambda>0$ (i.e. $R_{out}<\infty$) for all devices.



a) Redraw the circuit above to: (i) identify the 3 nodes that are associated with poles and (ii) include all the parasitic device capacitances (within M_{1-3}).

[10]

b) Determine an expression for the low frequency voltage gain of the first stage (V_x/V_{in})

[2]

c) Determine an expression for the resistance seen looking into node X.

[2]

d) Determine an expression for the DC (i.e. low frequency) voltage gain of the 2nd stage (V_{out}/V_x).

[2]

e) Determine an expression for the output resistance.

[2]

f) Determine expressions for the capacitances (to ground) at each of the nodes identified above by lumping together the parasitic capacitances appearing at each node. Use Miller's theorem to resolve any floating (i.e. ungrounded) capacitances.

[6]

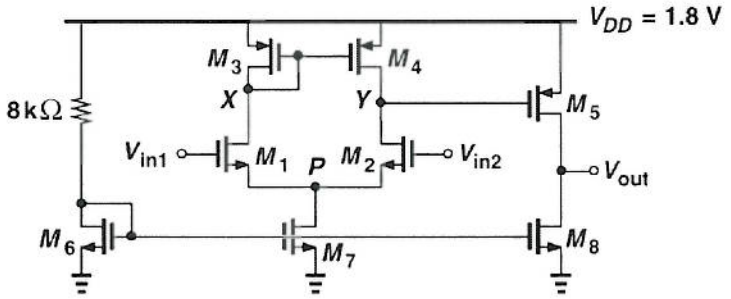
g) Determine expressions for the three pole frequencies (ω_{p1}, ω_{p2} and ω_{p3}).

[6]

3. A basic two stage operational amplifier is shown below.

This circuit consists of the differential pair (M_1 and M_2), an active current mirror (M_3 and M_4) to convert a differential to single-ended output, a second stage common source amplifier (M_5), and biasing circuit (8kΩ resistor and passive current mirror $M_{6\text{-}8}$).

Assume all devices are in saturation and $\lambda>0$ (i.e. $R_{out}<\infty$). Where required, use the following values: $\mu_n C_{ox}=200\mu A/V^2$, $\mu_p C_{ox}=100\mu A/V^2$, $V_{TH,n}=0.4V$, $V_{TH,p}=-0.5V$, $\lambda_n=0.1V^{-1}$, $\lambda_p=0.2V^{-1}$.



Use the following expression for the drain current of a MOSFET:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS}-V_{TH}\right)^2$$

a) Calculate the current through device M_6 (I_6), given that $(W/L)_6=6.4/0.18$. [7]

b) Given that $I_7=1.5mA$ and $I_8=3mA$, calculate $(W/L)_7$ and $(W/L)_8$. [2]

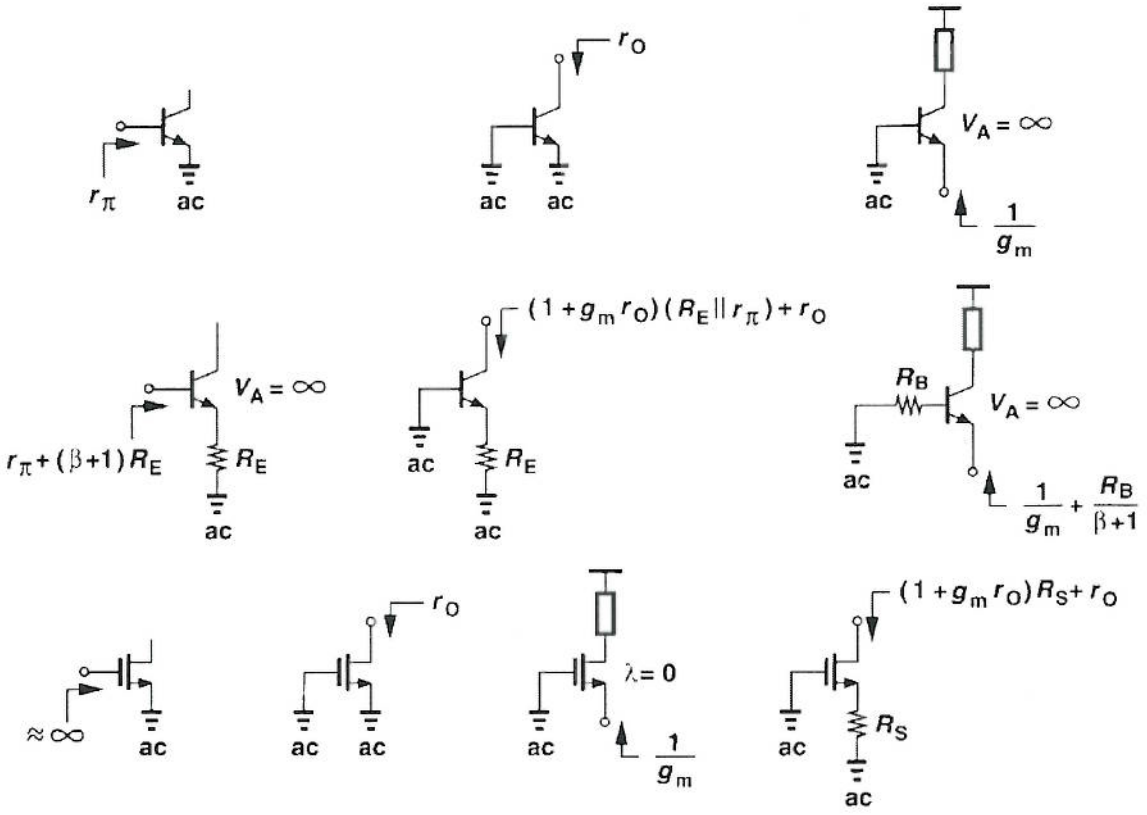
c) Derive an expression for the differential voltage gain of the first stage ($A_{v1}=V_y/V_{in1}-V_{in2}$). [5]

d) Derive the expressions for the voltage gain of the second stage ($A_{v2}=V_{out}/V_y$) and therefore the total voltage gain ($A_v=A_{v1}A_{v2}=V_{out}/V_{in1}-V_{in2}$). [3]

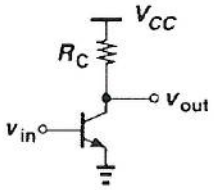
e) Given that: $(W/L)_1=(W/L)_2=250/1$
$(W/L)_3=(W/L)_4=4/4$
$(W/L)_5=40/4$
Calculate the voltage gain (in dB). [10]

f) Give three drawbacks of the bias generator circuit used in this design. [3]

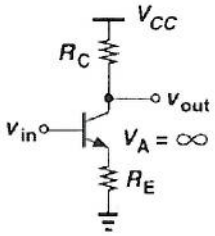
Input and Output Impedances



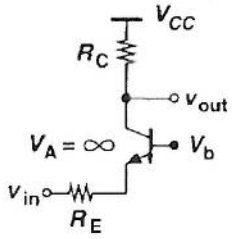
Voltage Gain Equations



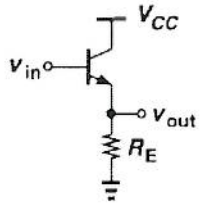
$$A_v = -g_m(R_C \| r_O)$$



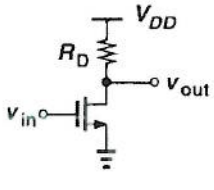
$$A_v = -\frac{R_C}{\frac{1}{g_m} + R_E}$$



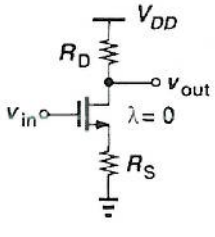
$$A_v = \frac{R_C}{\frac{1}{g_m} + R_E}$$



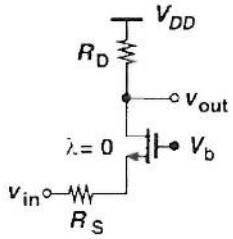
$$A_v = \frac{R_E \| r_O}{\frac{1}{g_m} + R_E \| r_O}$$



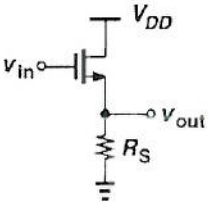
$$A_v = -g_m(R_D \| r_O)$$



$$A_v = -\frac{R_D}{\frac{1}{g_m} + R_S}$$



$$A_v = \frac{R_D}{\frac{1}{g_m} + R_S}$$



$$A_v = \frac{R_S \| r_O}{\frac{1}{g_m} + R_S \| r_O}$$

ANSWERS E2.2 – 2010/11

(1) (a) (i) offset voltage due to input stage mismatch and finite gain
(ii) input bias current (in BJT) – non-zero
(iii) finite gain – not infinite
(iv) non-zero o/p impedance
(v) bandwidth/slew-rate
(vi) limited input/output range

} any 4 of the following (4)

(b) (i) gain desensitisation
(ii) bandwidth enhancement
(iii) modification of input/output impendances
(iv) improved linearisation (4)

(c) ~~Lecture 5pt~~: Device mismatch poses a challenge in analogue design because although devices may be designed to be identical (or scaled), in reality due to processing tolerances there will always be mismatch ∴ performance will be different to the designed. (2)

Methods to improve: (i) larger device area
(ii) close proximity
(iii) same orientation
(iv) use common centroid geometry
(v) use dummy devices

} any 2 of the following (2)

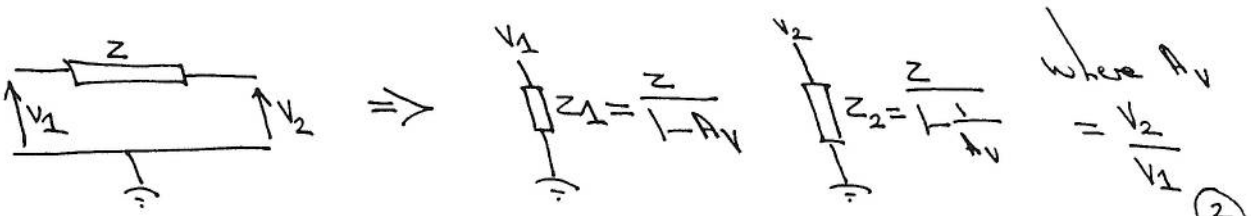
(d) The body effect manifests itself as a variation in MOSFET (CMOS tech) threshold voltage depending on the source-body bias (V_{SB}). (1)

The full expression is: $V_{TH} = V_{TH\phi} + \gamma\left(\sqrt{2\phi + V_{SB}} - \sqrt{2\phi}\right)$ (1)

where ∴ $V_{TH\phi}$ is the $V_{SB}=\phi$ threshold voltage
γ is the body effect parameter
2ϕ is the surface potential parameter. (1)

The body effect can be reduced eliminated be designing circuits such that all $V_{SB}=\phi$. If any devices have sources that are not connected to the power supply, the circuit should be designed such that these are PMOS devices – since they are in N-wells ∴ have an independent body terminal. (2)

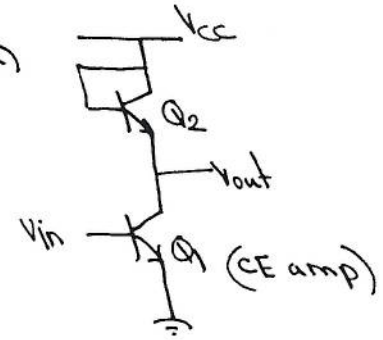
(e) Millers theorem establishes that in a linear circuit, if two nodes are connected by an impedance Z, this impedance can be replaced by two grounded impedances Z_1 and Z_2 as follows: (1)



(2)

This is particularly useful in analogue circuit analysis for resolving floating impedances, for example parasitic transistor capacitances to grounded impedances at each node. (1)

(f) (i)



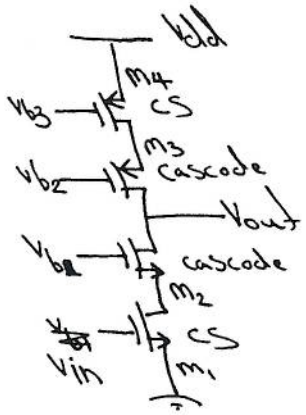
$$A_V = -g_{m1}\left(r_{o1} \| r_{o2} \| \frac{1}{g_{m2}}\right)$$

→ assuming $\frac{1}{g_{m2}} \ll r_{o1}, r_{o2}$

$$A_{v1} \approx \frac{-g_{m1}}{g_{m2}}$$

(2)

(ii)



$$A_V = -g_{m1}\left(\left(g_{m2} r_{o1} r_{o2} + r_{o1} + r_{o2}\right) \| \left(g_{m3} r_{o3} r_{o4} + r_{o3} + r_{o4}\right)\right)$$

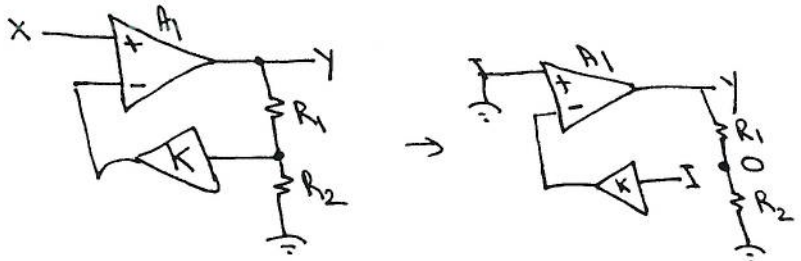
→ assuming $g_{m2} r_{o1} r_{o2} \gg r_{o1}, r_{o2}$

and $g_{m3} r_{o3} r_{o4} \gg r_{o3}, r_{o4}$

$$A_V \approx -g_{m1}\left(g_{m2} r_{o1} r_{o2} \| g_{m3} r_{o3} r_{o4}\right)$$

(2)

(g)



$$0 = I(-A_1) K \frac{R_2}{R_1 + R_2}$$

$$-\frac{0}{I} = K A_1 \cdot \frac{R_2}{R_1 + R_2}$$

(2)

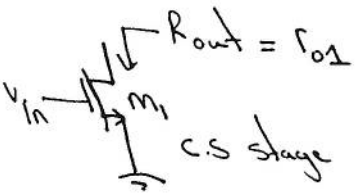
loop gain =

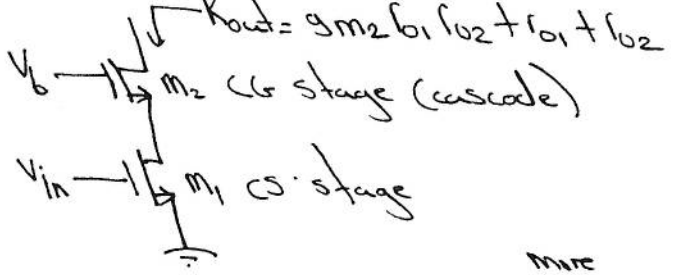
open-loop gain $= A_{OL} = A_1$

$$\therefore \text{closed-loop gain} = \frac{A_1}{1 + LG} = \frac{A_1}{1 + K A_1 \frac{R_2}{R_1 + R_2}}$$

(2)

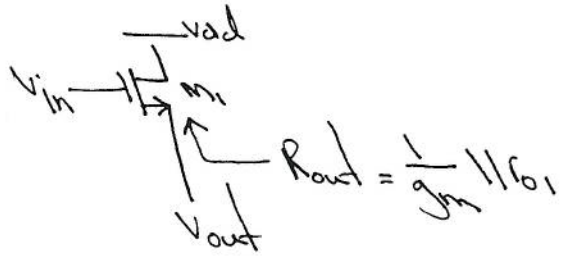
(h) A cascode stage is a common-base (or common-gate) amplifier connected to the o/p of a common emitter (or common source) amplifier. This can also be viewed as a degenerated common emitter. A cascode stage is often used to boost the output impedance of an amplifier and therefore also the voltage gain.





(4)

(i) The common-collector (or common drain) amplifier, often referred to as emitter (or source)-follower is preferred as a voltage buffer. This is because in this configuration the amplifier has a high input impedance and low output impedance and therefore is ideal as a voltage buffer.



(4)

(j) Given $J_{max} = 0.1\ mA/\mu m$, $I_{max} = 0.5\ mA$
and $R_{poly} = 8\Omega/\square$

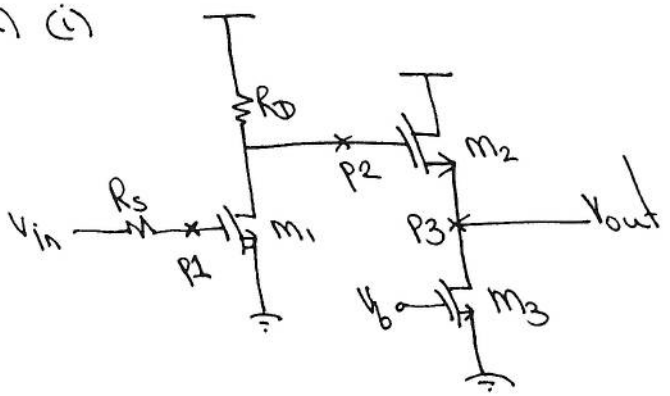
for a 5kΩ resistor: $W = \frac{I_{max}}{J_{max}} = \underline{5\mu m}$

$$\frac{L}{W} = \frac{5000}{8} = 625$$

$$\therefore L = 625 \times 5 = \underline{3125\mu m}$$

(4)

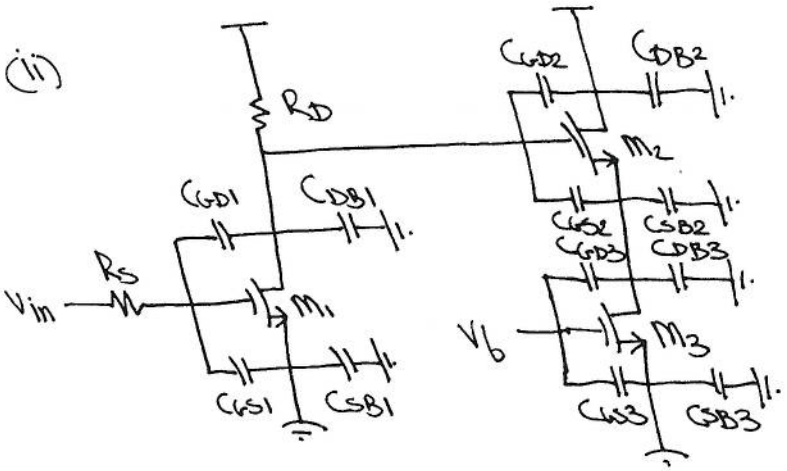
(2) (a) (i)



nodes associated with poles illustrated of left: P1, P2 and P3

(3)

(ii)



(7)

(b) $$\frac{V_x}{V_{in}} = -g_{m1}(R_D \| r_{o1})$$ (2)

(c) $$R_x = R_D \| r_{o1}$$ (2)

(d) $$\frac{V_{out}}{V_x} = \frac{r_{o2} \| r_{o3}}{1/g_{m2} + r_{o2} \| r_{o3}}$$ (2)

(e) $$R_{out} = \frac{1}{g_{m2}} \| r_{o2} \| r_{o3}$$

assuming $\frac{1}{g_{m2}} \ll r_{o2}, r_{o3} \rightarrow R_{out} \approx \frac{1}{g_{m2}}$ (2)

(f) $$C_{P1} = C_{GS1} + C_{GD1}\left(1 + \left|\frac{V_x}{V_{in}}\right|\right) = C_{GS1} + C_{GD1}\left(1 + g_{m1}(R_D \| r_{o1})\right)$$ (2)

$$C_{P2} = C_{DB1} + C_{GD2} + C_{GD1}\left(1 + \frac{1}{g_{m1}(R_D \| r_{o1})}\right) + C_{GS2}\left(1 - \frac{r_{o2} \| r_{o3}}{\frac{1}{g_{m2}} + r_{o2} \| r_{o3}}\right)$$ (2)

$$C_{P3} = C_{SB2} + C_{DB3} + C_{GD3} + C_{GS2}\left(1 - \frac{\frac{1}{g_{m2}} + r_{o2} \| r_{o3}}{r_{o2} \| r_{o3}}\right)$$ (2)

(9) $\omega_{p1} = \dfrac{1}{R_S \cdot C_{p1}} = \dfrac{1}{\left[C_{GS1} + C_{GD1}\left(1 + g_{m1}(R_D \| r_{O1})\right)\right] R_S}$ (2)

$$\omega_{p2} = \frac{1}{R_x \cdot C_{p2}} = \frac{1}{\left[C_{DB1} + C_{GD2} + C_{GD1}\left(1 + \frac{1}{g_{m1}(R_D \| r_{O1})}\right) + C_{GS2}\left(1 - \frac{r_{O2} \| r_{O3}}{\frac{1}{g_{m2}} + r_{O2} \| r_{O3}}\right)\right](R_D \| r_{O1})}$$ (2)

$$\omega_{p3} = \frac{1}{R_{out} \cdot C_{p3}} = \frac{1}{\left[C_{SB2} + C_{DB3} + C_{GD3} + C_{GS2}\left(1 - \frac{\frac{1}{g_{m2}} + r_{O2} \| r_{O3}}{r_{O2} \| r_{O3}}\right)\right]\frac{1}{g_{m2}}}$$ (2)

(3) (a) $V_{GS6} + I_6 \cdot (8K\Omega) = 1.8$

$$V_{GS6} + \tfrac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS6} - V_{TH})^2 (8K) = 1.8$$

$$(8K)\,\frac{200\mu}{2} \cdot \frac{6.4}{0.18}(V_{GS} - 0.4)^2 + V_{GS} = 1.8$$

$$8K\left(3.5 \times 10^{-3}\right)\left(V_{GS}^2 - 0.8V_{GS} + 0.16\right) + V_{GS} - 1.8 = 0$$

$$28.4V_{GS}^2 - 22.75V_{GS} + V_{GS} + 4.54 - 1.8 = 0$$

$$28.4V_{GS}^2 - 21.75V_{GS} + 2.744 = 0$$

$V_{GS} = 0.606$ and ~~0.159~~ below threshold.

$$\therefore I_6 = \tfrac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$= \tfrac{1}{2}(200\mu)\frac{6.4}{0.18}(0.606 - 0.4)^2$$

$$= 150\mu A$$

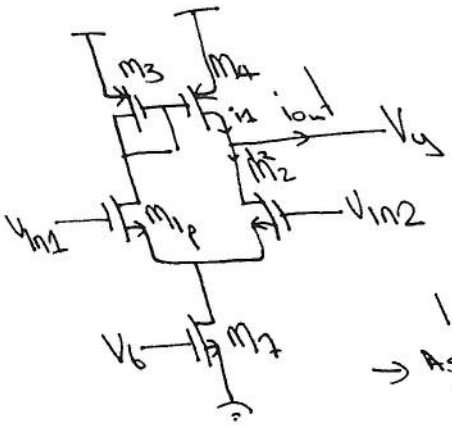
(8)

(b) Given that $I_7 = 1.5mA$, $I_8 = 3mA$

$$\Rightarrow \left(\frac{W}{L}\right)_7 = 10\left(\frac{W}{L}\right)_6 \Rightarrow \frac{64}{0.18} = \left(\frac{W}{L}\right)_7$$

$$\left(\frac{W}{L}\right)_8 = 20\left(\frac{W}{L}\right)_6 \Rightarrow \frac{128}{0.18} = \left(\frac{W}{L}\right)_8$$ (2)

(3) (c)



$I_{out} = i_1 - i_2$

→ Assuming node P is an AC ground

$i_1 = g_{m1} V_{in1}$

$I_2 = g_{m2} V_{in2}$

$\therefore i_{out} = g_{m1}(V_{in1} - V_{in2})$ assuming M_1 and M_2 are identical.

$V_y = i_{out} \cdot R_y$

$R_y = r_{o2} \| r_{o4}$

$\therefore \frac{V_y}{V_{in1} - V_{in2}} = g_{m1}(r_{o2} \| r_{o4})$ (5)

(d) $\frac{V_{out}}{V_y} = -g_{m5}(r_{o5} \| r_{o8})$

$\frac{V_{out}}{V_{in1} - V_{in2}} = \frac{V_{out}}{V_y} \times \frac{V_y}{V_{in1} - V_{in2}}$

$= -g_{m5}(r_{o5} \| r_{o8}) \cdot g_{m1}(r_{o2} \| r_{o4})$

$|A_v| = g_{m1} g_{m5} (r_{o2} \| r_{o4})(r_{o5} \| r_{o8})$ (3)

(e) $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{250}{1}$

$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \frac{4}{4}$

$\left(\frac{W}{L}\right)_5 = \frac{40}{4}$

use $g_m = \sqrt{2 I_D \frac{W}{L} \mu C_{ox}}$

$g_{m1} = \sqrt{1.5m \left(\frac{250}{1}\right) 200\mu} = 8.66mS$

$g_{m5} = \sqrt{6m \left(\frac{40}{4}\right) 100\mu} = 2.45mS$

$r_{o2} = \frac{1}{\lambda_n I_{D2}} = \frac{1}{0.1 \cdot 0.75m} = 13.3K.$

$r_{o4} = \frac{1}{\lambda_p I_{D4}} = \frac{1}{0.2 \cdot 0.75m} = 6.6K$

$\Big\} \; r_{o2} \| r_{o4} = 4.44K$

$r_{o5} = \frac{1}{\lambda_p I_{D5}} = \frac{1}{0.2 \cdot 3m} = 1.6K$

$r_{o8} = \frac{1}{\lambda_n I_{D5}} = \frac{1}{0.1 \times 3m} = 3.3K$

$\Big\} \; r_{o5} \| r_{o8} = 1.1K$

$\therefore A_v = (2.45m)(8.66m)\, 4.4K \cdot 1.1K = 103.6$

$= 40.3dB$ (10)

(f) PVT ⟶ P = Process

V = Voltage (Power Supply)

T = Temperature

} Need to list the following explaining how it is dependant. (3)