IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2018

EEE/EIE PART II: MEng, BEng and ACGI

DIGITAL ELECTRONICS 2

Corrected copy

Friday, 8 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 carry equal marks (30% each).

Exam paper should NOT be taken out of the exam room

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung
Second Marker(s) : W. Dai

Information for Candidates:

The following notation is used in this paper:

1. Unless explicitly indicated otherwise, digital circuits are drawn with their inputs on the left and their outputs on the right.
2. Within a circuit, signals with the same name are connected together even if no connection is shown explicitly.
3. The notation X2:0 denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0.
4. Signed binary numbers use 2's complement notation.

1. (a) *Figure 1.1* shows a circuit with two D flip-flops FF1 and FF2 with setup and hold times of 2 ns and 1 ns respectively, and a clock-to-Q output delay of 2 ns. The clock signal CLK has a 1:1 mark-space ratio. The signal path has two combinational circuits, LUT_1 and LUT_2, each having a propagation delay between 1 ns and 5 ns. The clock path is driven by non-inverting clock buffer, which has a propagation delay between 2 ns and 10 ns.

(i) Derive the inequalities for the setup time constraints for this circuit.

[4]

(ii) Hence derive the maximum frequency of the signal CLK for reliable operation of this circuit.

[2]

(iii) How would you modify the circuit to increase the maximum operating clock frequency? What is the new maximum frequency?

[2]

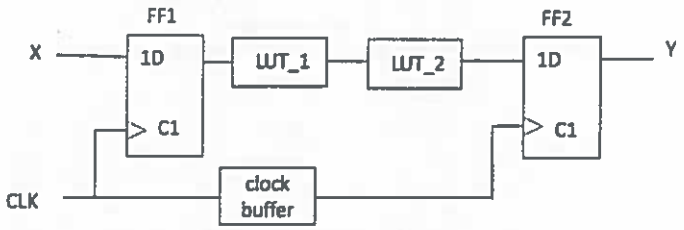


Figure 1.1

(b) *Figure 1.2* depicts a circuit with four D-type flip-flops FF1-FF4 connected in series with an XOR gate.

(i) If FF1, FF2 and FF4 are initially reset, and FF3 is initially set, determine the output Q4:1 over 10 clock cycles.

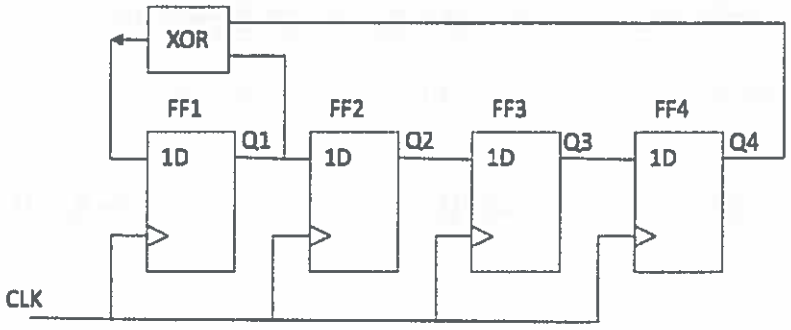
[2]

(ii) Implement this circuit in Verilog HDL with an interface defined in *Figure 1.2*.

[4]

(iii) Given that $1 + x^3 + x^5$ is a primitive polynomial, design in the form of a schematic circuit diagram a linear-feedback shift register that produces a 5-bit pseudo-random binary number.

[2]




```
module sr4 (
   clk,
   q);

   input clk;
   output [4:1]  q;
```

Figure 1.2

(c) *Figure 1.3(a)* shows the state diagram of a four-states Finite State Machine (FSM) with one input A and one output X.

(i) Draw the state transition table for this FSM.

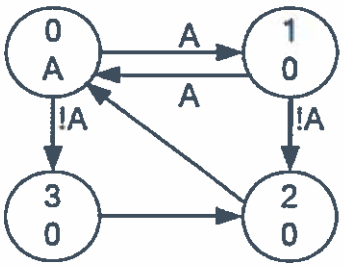
[2]

(ii) Complete the timing diagram shown in *Figure 1.3(b)*.

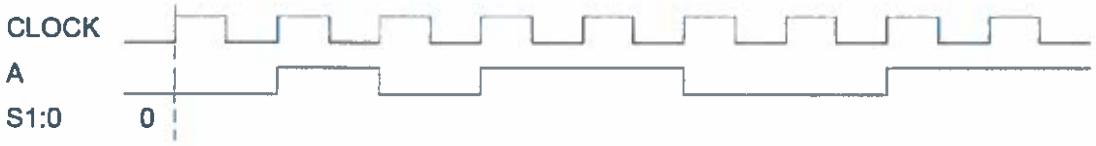
[2]

(iii) Using one-hot encoding, specify this FSM in Verilog HDL.

[4]



(a)



(b)

Figure 1.3

(d) A microprocessor system with an address bus A17:0 contains an address decoder module that produces four chip select signals: ROM_CS, NVRAM_CS, RAM_CS and IO_CS. The Boolean equations for these four signals are:

$$\text{ROM\_CS} = \overline{A17} \,\&\, \overline{A16} \,\&\, \overline{A15}$$
$$\text{NVRAM\_CS} = \overline{A17} \,\&\, \overline{A16} \,\&\, \text{A15} \,\&\, \overline{A14}$$
$$\text{RAM\_CS} = \overline{A17} \,\&\, A16$$
$$\text{IO\_CS} = \text{A17} \,\&\, \text{A16} \,\&\, \text{A15} \,\&\, \text{A14} \,\&\, \text{A13} \,\&\, \text{A12} \,\&\, \text{A11} \,\&\, \text{A9} \,\&\, \overline{A8}$$

(i) Determine the address ranges associated with each chip select signal.

[4]

(ii) Implement the decoder circuit in Verilog HDL with the module interface defined in *Figure 1.4*.

[4]

```
module decoder (
   addr,  rom_cs, nvram_cs, ram_cs, io_cs);
```

Figure 1.4

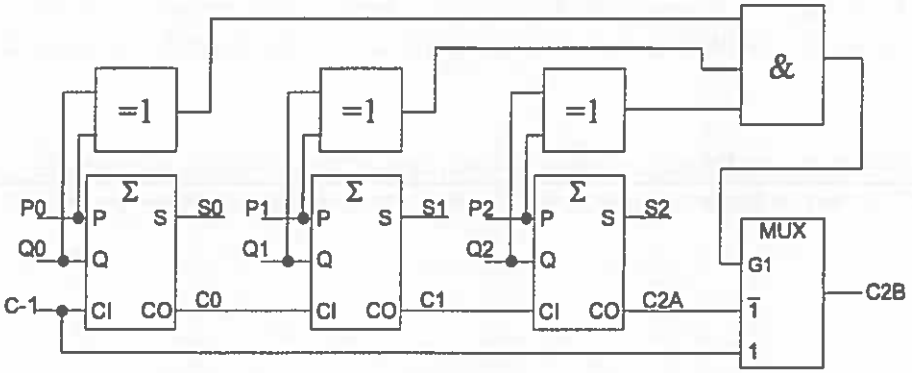
(e) *Figure 1.5(a)* shows the circuit of a 3-bit carry-skip binary adder. The worst-case propagation delays of the circuit elements are given in *Figure 1.5(b)* (in nanoseconds).

(i) Determine the worst-case propagation delays from P0 and from C–1 to C2A and C2B.

[4]

(ii) What is the worst-case delay from C–1 to the output carry of a 6-bit binary adder implemented with two such 3-bit adders as shown in *Figure 1.5(a)*?

[4]



(a)

Device	Path	Delay
Adder	any input → S any input → CO	3 2
Multiplexer	SEL → output data input → output	3 2
XOR gate	any input → output	2
AND gate	any input → output	1

(b)

Figure 1.5

2. *Figure 2.1*(a) shows a flash analogue-to-digital converter comprising three identical resistors, four comparators and a logic block. The output of a comparator is high whenever the voltage at the "+" input is greater than that at the "–" input. VIN is the analogue input to be converter. A, B, C and D are the outputs of the four comparators. X2:0 is the converted digital values for VIN.

(a) What are the range of voltage values of VIN for signals A, B, C and D to be high?

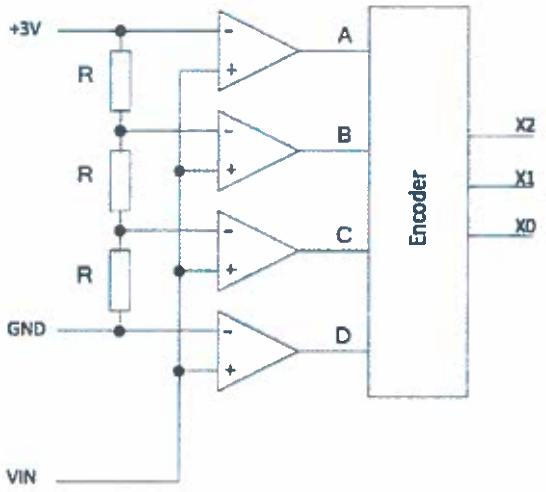
[10]

(b) The truth table in *Figure 2.1(b)* defines the relationship between X2:0 to A, B, C and D. Design the encode module in Verilog HDL with the module interface shown.

[10]

(c) Given that the resistors are accurate to within ±20%, what is the accuracy of the flash ADC in unit of least significant bit (LSB)? State any assumption used.

[10]



(a)

ABCD	X2:0
0000	0
0001	1
0011	2
0111	3
1111	4

```
module encoder (
    A, B, C, D, X);

    input A, B, C, D;
    output [2:0] X;
```

(b)

Figure 2.1

3. The circuit of *Figure 3.1(a)* contains: a 64-byte random access memory (RAM), an 8-bit binary counter (CTR8), a 6-bit adder (Σ), a 6-bit multiplexer (MUX), a flip-flop and two 8-bit registers REG8W and REG8R. The registers store a new value on the rising edge of the clock, C, but only when the enable input, EN is high just before the rising edge. Tristate outputs are marked with ▽ and enabled by the OE input. Data is written into the RAM when WE is low and read out when OE is high.

   Only the six most significant output bits of the counter, Q7:2 are taken to the adder and the multiplexer; the two least significant bits are used to generate the signals F=Q1+Q0 and L=Q1•Q0. All signals transitions occur just after the rising edge of C.

   (a) Assuming that N5:0 = 0 and that the counter initially contains the value Q7:0 = 18, complete the timing diagram shown in Figure 3.1(b) covering eleven clock cycles and showing the values of Q7:0, A5:0 and the waveforms of Q1, Q0, F, L and WE . You should indicate only the rising edges of C rather than its full waveform.

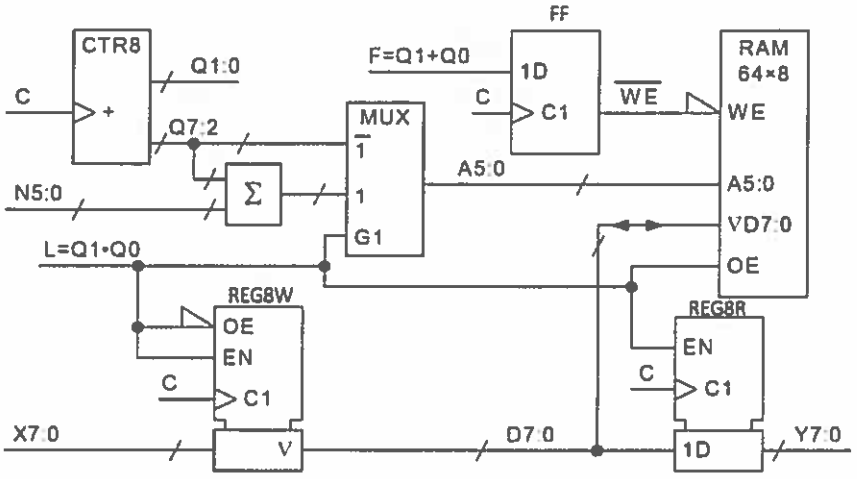
   [15]

   (b) Indicate on your diagram the times when (i) the value X7:0 is stored, (ii) D7:0 it is written into RAM, (iii) D7:0 it is read back from RAM and (iv) Y7:0 changes to a new value.

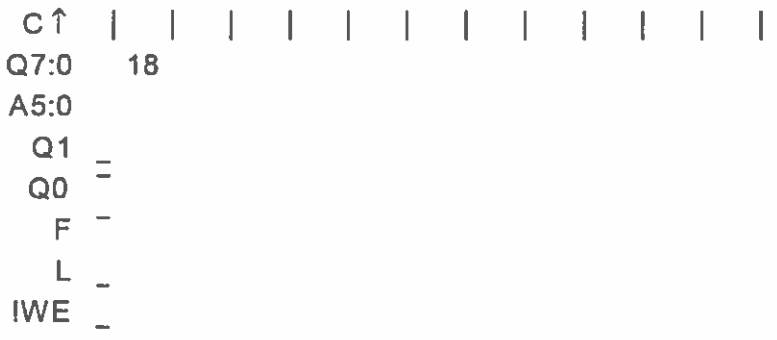
   [5]

   (c) If X7:0 changes only on the rising edge of Q1, determine the number of clock cycles delay between X7:0 and Y7:0 when N5:0 is equal to (i) 0, (ii) 63, (iii) 1.

   [10]



(a)



(b)

Figure 3.1