EE4-16
EE9-AC6

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2015

MSc and EEE PART IV: MEng and ACGI

**ANALOGUE SIGNAL PROCESSING**

Thursday, 21 May 10:00 am

Time allowed: 3:00 hours

Corrected Copy

**There are SIX questions on this paper.**

**Answer FOUR questions.**

*All questions carry equal marks*

**Any special instructions for invigilators and information for candidates are on page 1.**

Examiners responsible First Marker(s) : P. Georgiou
Second Marker(s) : K. Fobelets

**Special instructions for students**

*Unless otherwise stated the following parameters have the following definitions:*

$V_{DS}$ *: Drain Source Voltage.*

$V_{GS}$ *: Gate Source Voltage.*

$V_{TH}$ *: Threshold Voltage.*

$U_t$ *: Thermal Voltage.*

$n$ *: Weak Inversion Slope factor.*

$g_m$*: Transconductance.*

*Useful identities:*

$$cos^2 A + sin^2 A = 1$$

$$cos^2 A - sin^2 A = cos(2A)$$

$$sec^2 A - tanh^2 A = 1$$

1. a) State two advantages and two disadvantages of using a purely analogue approach to conduct signal processing.

[4]

b)

(i) Derive the transconductance efficiency for transistors operating in weak and strong inversion and show using a graph which one is more efficient terms of bias current.

[4]

(ii) Using two or more transistors operating in these two modes plus two resistors, draw a circuit which implements the following function stating assumptions for the choice of resistors $R_1$ and $R_2$:

$$I_{out} = \beta\left(I_o R_2 exp\left(\frac{I_{in}R_1}{nU_t}\right) - V_{TH}\right)^2$$

[4]

c) The total noise of a MOS transistor is defined as follows:

$$v_n^2 = \frac{K_w}{I_D^p}\cdot\Delta f + \frac{K_f}{A}\cdot\ln\left(\frac{f_h}{f_l}\right)$$

(i) Explain what all the terms of this equation mean and using this equation, derive for M=2 stages and $n$ devices per stage of Figure 1.1 the equation for total output noise.

[4]

(ii) Explain why computing with 32 bit precision in analogue is challenging and discuss what the optimum precision for analogue computation is.

[4]

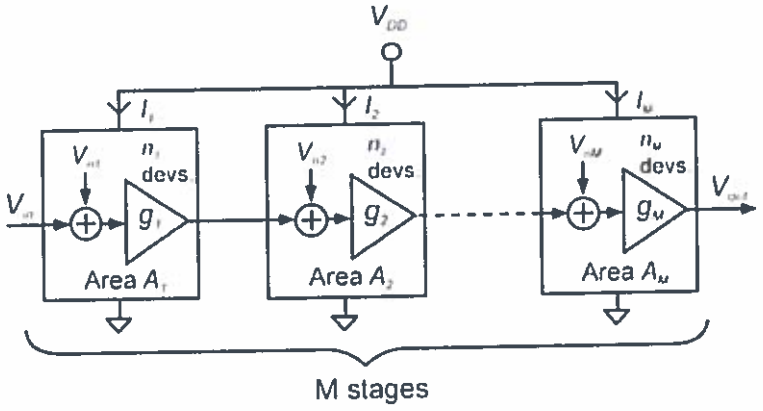


Figure 1.1

2.

a) This question concerns translinear circuits.

(i) What is a translinear element ?

(ii) Draw three devices which could be used as translinear elements justifying your choices with equations describing their operation.

[4]

b) List the three factors which contribute to non-ideal behaviour in translinear circuits.

[3]

c) Figure 2.1 shows a translinear circuit made up of NMOS transistors biased in weak inversion.

(i) Derive $I_Z$ as a function of $I_X$ and $I_Y$ by applying the translinear principle. Show all necessary steps.

(ii) What is the function of the circuit shown in Figure 2.1 ?

[5]

d) Figure 2.2 shows a translinear circuit capable of computing the trigonometric function $\sin(\pi y)$ through the approximation $\frac{y-y^3}{1+y^2}$ .

(i) Express the currents $I_3$ and $I_4$ in terms of I and $I_X$.

(ii) Express the differntial output current $I_2$-$I_1$ and show that when $I_X = yI$ then $I_2$-$I_1$ = $I\frac{y \cdot y^3}{1+y^2}$

[8]

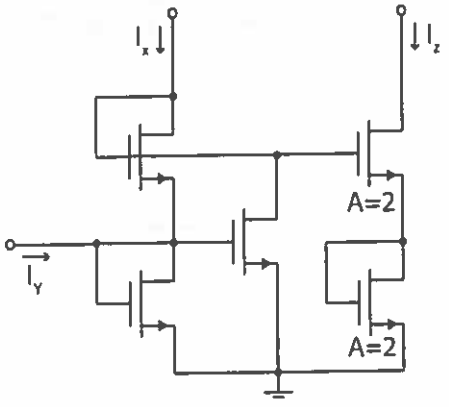


Figure 2.1

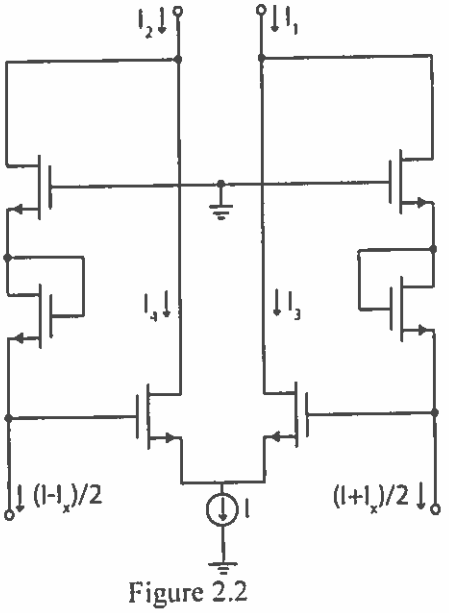


Figure 2.2

3. a) Figure 3.1 shows a block diagram of a current-mode companding integrator, with an input X and an output Y. f() and g() represent non-linear functions which compress and expand the signal such that the input-output relationship of the integrator is linear and given by:

$$Y = \tau \int X \cdot dt$$

Given that the expansive function is defined as $I_{out} = g(V_c) = I_T \tanh(V_c / nU_t)$, derive the function f(x) such that linear integration is achieved. All constants should be grouped to represent a current $I_1$, with the function f() composed of just $I_\omega$, $I_1$ and $I_T$.

[6]

b) The transfer function of an oscillator may be defined in state space representation by the following equations:

$$\dot{X}_1 = -\omega_0 X_1 + \omega_0 X_2$$

$$\dot{X}_2 = -2\omega_0 X_1 + \omega_0 X_2 + \omega_0 U$$

$$Y = X_1$$

where Y is the output, U is the input and $X_1$ and $X_2$ are the states.

(i) By using the mappings below, show how these linear equations can be mapped to non-linear log-domain design equations. You may use the following mapping for constant currents, $I_1 = I_2 = I_\omega$ and $I_U = I_O$.

$$X_1 = I_1 \exp\left(\frac{V_1}{nU_t}\right) \qquad X_2 = I_2 \exp\left(\frac{V_2}{nU_t}\right) \qquad U = I_U \exp\left(\frac{V_U}{nU_t}\right)$$

[6]

(ii) With these log-domain design equations, sketch a schematic of the final log domain filter using weak inversion MOS transistors.

[6]

(iii) Given the oscillation frequency is set to be $\omega_0 = 2\ \pi\ 10000$ rad/s, select a suitable current for $I_1$ given that the filter capacitor is C = 10 pf , n = 1.23 and $U_t = 25$ mV.

[2]

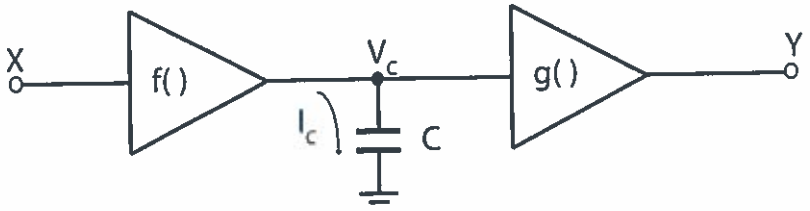


Figure 3.1

4.

a) Figure 4.1 shows a conventional second-generation positive current conveyor, CCII+.

(i) Explain it's operation principle and describe how impedances at each of its three ports, X, Y, Z, differ from a standard operational amplifier. [4]

(ii) Draw the circuit of a CMOS implementation of a bi-directional CCII+. [3]

Using current conveyors design circuits which implement:

(iii) A current mode differentiator.

(iv) A voltage mode differentiator.

(v) A full wave voltage mode rectifier. [6]

b) Derive the generalized equation for the output currents, $I_{out}$ of the circuit in Figure 4.2 and explain the function of this circuit. [4]

c) Draw a circuit than can calculate the correlation between two signals and explain its operation. [3]

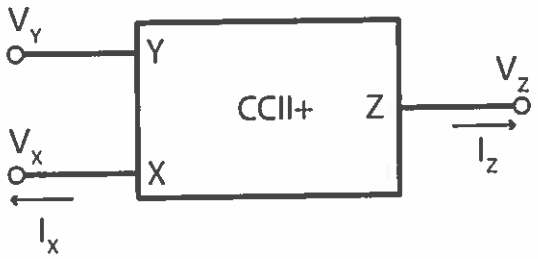


Figure 4.1

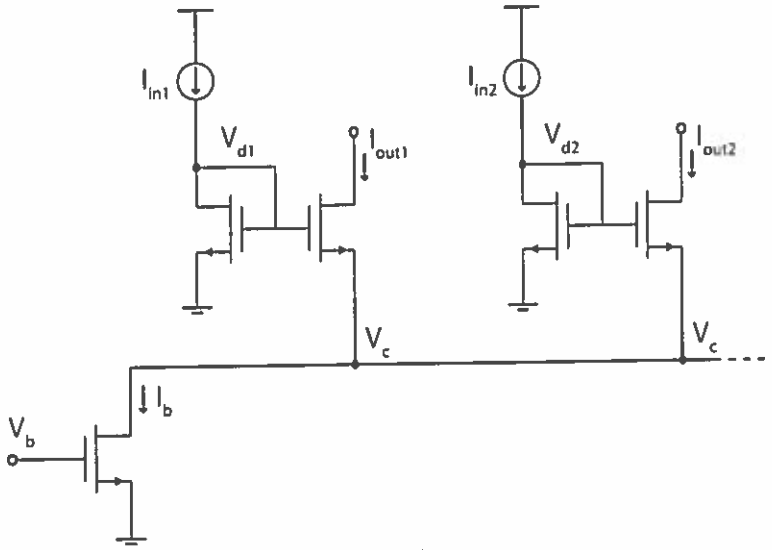


Figure 4.2

5.

a) Explain the principle of autozeroing with the aid of diagrams. [3]

b) Explain how autozeroing affects the noise spectrum of the signal. [2]

c) Figure 5.1 shows a switched capacitor amplifier correlated double sampling amplifier.

(i) Derive the output voltage of this amplifier $V_{out}$ for both phases $\Phi_1$ and $\Phi_2$ showing how this removes any offset in the amplifier. You may ignore feedback capacitor $C_{dg}$. [4]

(ii) Explain why this configuration requires an opamp with a high slew rate ? [1]

(iii) Show how the circuit of Figure 5.1 can be modified to reduce the high slew rate requirements, and derive the change in output voltage after this modification. [5]

d) Derive the output current, $I_{out}$ for the switch current algorithmic cell given in Figure 5.2 showing how this eliminates any error caused due to the switches. [5]

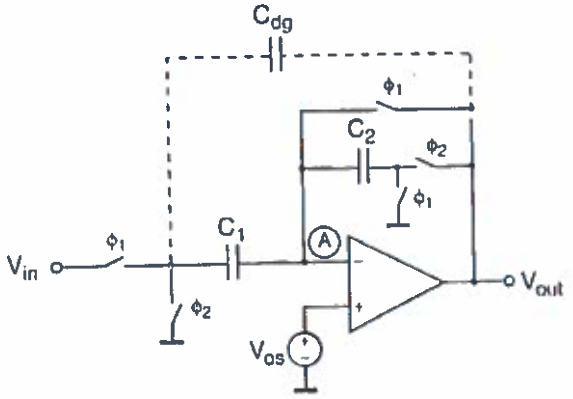


Figure 5.1

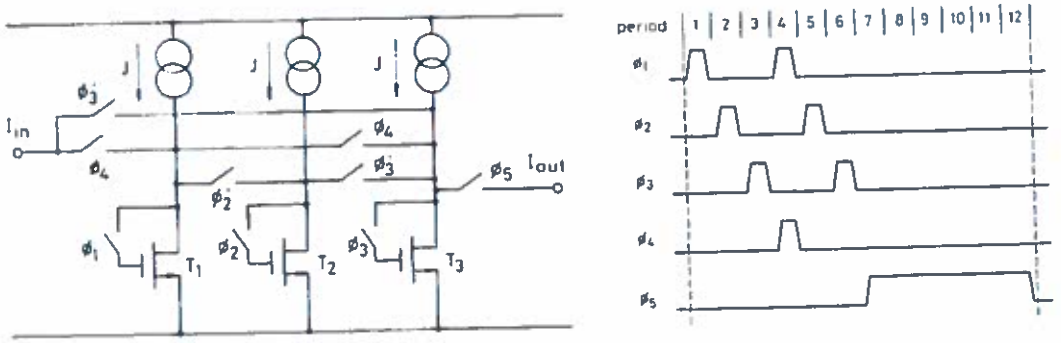


Figure 5.2

6. Figure 6.1 shows a trignonometric circuit where all transistors operate in the weak inversion region with the output currents given by:

$$I_1 = \frac{I_{DC}}{2} e^{\left(\frac{V_+ - V_-}{nU_t}\right)} \qquad I_2 = \frac{I_{DC}}{2} e^{\left(\frac{-(V_+ - V_-)}{nU_t}\right)}$$

a) Show how the circuit can be transformed to give the following trigonometric functions:

$$I_{out1} = I_{DC} \sinh\left(\frac{V_1 - V_2}{nU_t}\right)$$

$$I_{out2} = I_{DC} \cosh\left(\frac{V_1 - V_2}{nU_t}\right)$$

[6]

b) Figure 6.2 shows a differential pair where both transistors M1 and M2 are biased in the weak inversion region. Derive the function for the output current showing how it is trigonometrically related to the input voltage.

[6]

c) Using the two circuits from parts a) and b) or otherwise, design a circuit which implements the following trigonometric function:

$$I_{out} = I_{bias} \operatorname{sech} \frac{V_1 - V_2}{nU_t}$$

whereby $I_{bias}$ is an individually tuned current.

[8]

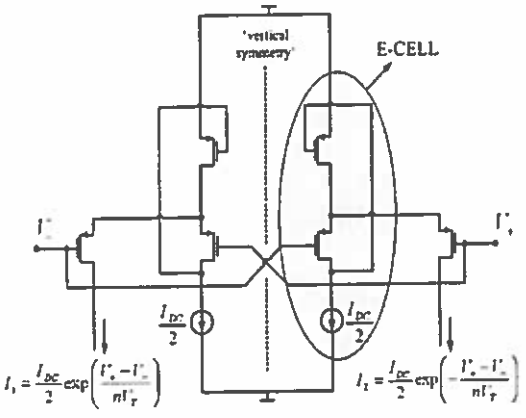


Figure 6.1

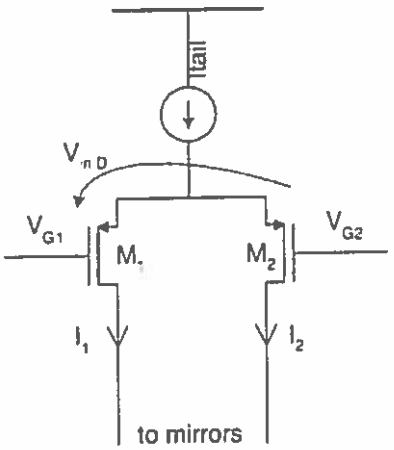


Figure 6.2