Digital Electronics I [EE1-02]

Question 1

1. a) (i)

$$\overline{\overline{A}+\left(\overline{A\overline{B}}\right)\overline{C}}$$
$$=A\left(\overline{\left(\overline{A\overline{B}}\right)\overline{C}}\right)$$
$$=A\left(A\overline{B}+C\right)$$
$$=A\overline{B}+AC$$

[4]

ii)

$$ABC+B\left(A\oplus B\right)$$
$$=ABC+B\left(\overline{A}B+A\overline{B}\right)$$
$$=ABC+\overline{A}B$$
$$=B\left(AC+\overline{A}\right)$$
$$=B\left(C+\overline{A}\right)$$
$$=BC+\overline{A}B$$

[4]

b)

$$f=\overline{A}\overline{B}\left(\overline{C\oplus D}\right)+A\overline{B}\overline{C}\overline{D}+ACD+ABD$$
$$=\overline{A}\overline{B}CD+\overline{A}\overline{B}\overline{C}\overline{D}+A\overline{B}\overline{C}\overline{D}+ACD+ABD$$

f

AB \ CD	00	01	11	10
00	1	0	1	0
01	0	0	0	0
11	0	1	1	0
10	1	0	1	0

$$f=\overline{B}\overline{C}\overline{D}+ABD+\overline{B}CD$$

Here, 1 mark for drawing the Karnaugh map, 1 for filling it out correctly, 1 for the correct grouping, and 1 for the final expression.

[4]

c)

f AB \ CD	00	01	11	10
00	0	0	0	1
01	1	0	0	1
11	0	1	0	1
10	1	0	0	1

$$f=\left(A+\bar{D}\right)\left(B+\bar{D}\right)\left(A+B+C\right)\left(\bar{A}+\bar{B}+C+D\right)\left(B+\bar{C}+\bar{D}\right)$$

Here, 1 mark for drawing the Karnaugh map, 1 for filling it out correctly, 1 for the correct grouping, and 1 for the final expression.

[4]

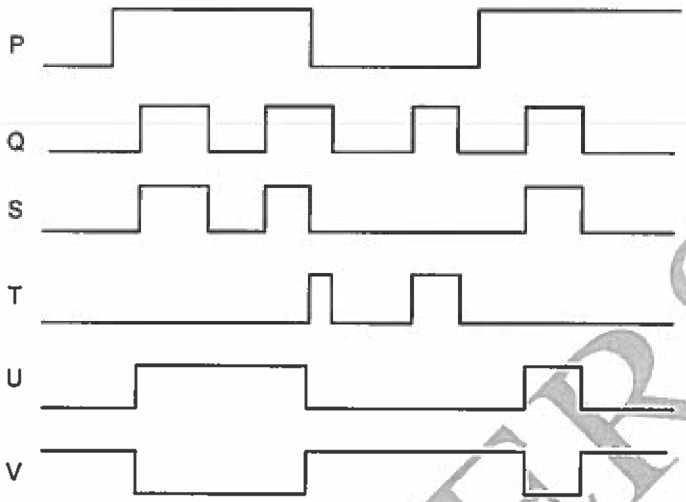
d)

Decimal	Hexadecimal	Binary	BCD
5153	1421		
		0011 0111 1001 1000	(1) 0100 0010 0011 0010
	1CF	0000 0001 1100 1111	
-1101		1111 1011 1011 0011	

Give 2 marks per answer.

[8]

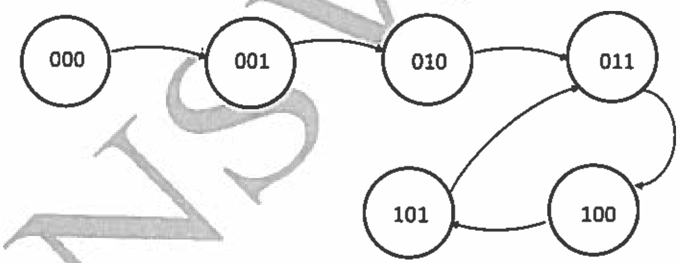
e)



Marks: 2 marks per waveform

[8]

f)



Give 2 marks correct states and 2 marks for correct interconnections.

[4]

g)

A	B	C	Y	Z
0	0	0	0	1
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

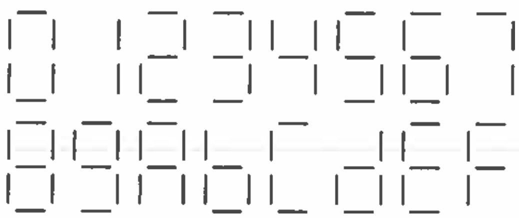
Give 0.5 marks per row of the table.

[4]

Question 2

2.

(a) (i) The hexadecimal pattern is as follows:



[4]

(ii) We first draw the K-map for the top horizontal segment, with the hexadecimal number corresponding to the variables X[3:0]:

		X1, X0			
	f	00	01	11	10
X3, X2	00	1	0	1	1
	01	0	1	1	1
	11	1	0	1	1
	10	1	1	0	1

This gives the Boolean expression:

$$f = \overline{X0}X3 + X1X2 + X1\overline{X3} + \overline{X0}\,\overline{X2} + \overline{X1}\,\overline{X2}X3 + X0X2\overline{X3}$$

The expression may be converted directly to NAND gates only by applying De Morgan's theorem:

$$f = \overline{\overline{\overline{X0}X3 + X1X2 + X1\overline{X3} + \overline{X0}\,\overline{X2} + \overline{X1}\,\overline{X2}X3 + X0X2\overline{X3}}}$$

$$= \overline{\left(\overline{\overline{X0}X3}\right)\left(\overline{X1X2}\right)\left(\overline{X1\overline{X3}}\right)\left(\overline{\overline{X0}\,\overline{X2}}\right)\left(\overline{\overline{X1}\,\overline{X2}X3}\right)\left(\overline{X0X2\overline{X3}}\right)}$$

The circuit then uses 4 two-input NAND gates, 2 three-input NAND gates, 1 six-input NAND gate, and 7 inverters.

Marks: 1 marks for K-map, 1 marks for initial expression from this, 2 marks for NAND expression.

[4]

(iii)

f	X1, X0: 00	01	11	10
X3, X2: 00	1	0	1	1
01	0	X	1	1
11	1	0	1	1
10	1	X	0	1

For a NOR implementation, we can solve in POS form:

$$\overline{f} = \overline{X1 + \overline{X0}} + \overline{X3 + \overline{X2} + X1} + \overline{\overline{X3} + X2 + \overline{X0}}$$

$$\Rightarrow f = \overline{\left(\overline{X1 + \overline{X0}}\right) + \left(\overline{X3 + \overline{X2} + X1}\right) + \left(\overline{\overline{X3} + X2 + \overline{X0}}\right)}$$

Marks: 1 marks for K-map, 1 mark for the grouping and/or an initial expression, and 2 marks for the final NOR expression.

[4]

b) To determine if A = B requires a bit-by-bit comparison using an XNOR gate will determine equality. To determine A > B again requires a bit-by-bit comparison. Starting from the most significant bit, if $A_3 > B_3$ then A > B. However, if this is not true, and $A_3 = B_3$, then we need to check the next set of bits and so on. This gives the following Boolean expressions for H, E and L:

$$H = A_3\overline{B}_3 + \left(\overline{A_3 \oplus B_3}\right)A_2\overline{B}_2 + \left(\overline{A_3 \oplus B_3}\right)\left(\overline{A_2 \oplus B_2}\right)A_1\overline{B}_1 + \left(\overline{A_3 \oplus B_3}\right)\left(\overline{A_2 \oplus B_2}\right)\left(\overline{A_1 \oplus B_1}\right)A_0\overline{B}_0$$

$$E = \left(\overline{A_3 \oplus B_3}\right)\left(\overline{A_2 \oplus B_2}\right)\left(\overline{A_1 \oplus B_1}\right)\left(\overline{A_0 \oplus B_0}\right)$$

$$L = \overline{A}_3B_3 + \left(\overline{A_3 \oplus B_3}\right)\overline{A}_2B_2 + \left(\overline{A_3 \oplus B_3}\right)\left(\overline{A_2 \oplus B_2}\right)\overline{A}_1B_1 + \left(\overline{A_3 \oplus B_3}\right)\left(\overline{A_2 \oplus B_2}\right)\left(\overline{A_1 \oplus B_1}\right)\overline{A}_0B_0$$

Alternatively, given H and E as above, we have: $L = \overline{H}.\overline{E}$

Give 2 marks for identifying logic, and 2 marks each for the three Boolean expressions.

[8]

c) The 8 bit numbers A[7:0] and B[7:0] can each be broken up into two halves containing the upper four and lower four bits. We can then use COMP modules to compare A[7:4] with B[7:4], and A[3:0] with B[3:0].

[2]

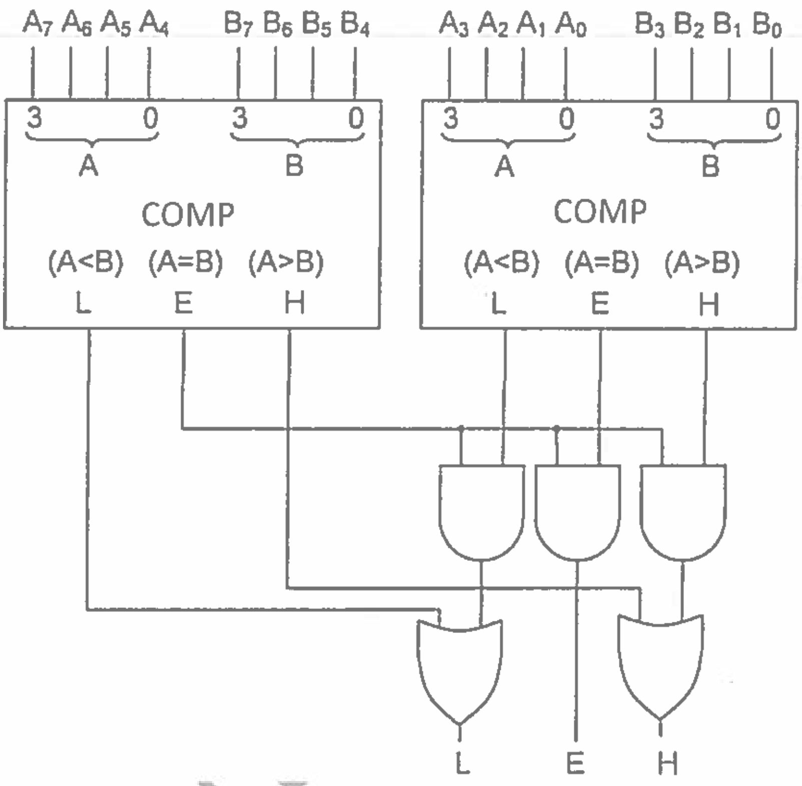
Additional combinational logic is necessary to allow the H, E and L outputs of each COMP module to be compared and obtain the comparison between A[7:0] and B[7:0]. The following logic will produce H, E and L:

H = 1 if A[7:4] > B[7:4], OR: A[7:4] = B[7:4] AND A[3:0] > B[3:0].
L = 1 if A[7:4] < B[7:4], OR: A[7:4] = B[7:4] AND A[3:0] < B[3:0].

E = 1 if A[7:4] = B[7:4] AND A[3:0] = B[3:0].

[4]

This gives the following circuit diagram:



[4]

Question 3

3. a) With A, B as the present state of the FSM, A^+, B^+ as the next state, X input and Y output, we have the following state transition table:

A	B	X	A^+	B^+	Y^+
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	0	0	0

Give 2 marks for basic table format and 0.5 marks for each correct row of the table.

[6]

b) For an FSM implemented using D-flip-flops, the next state of the flip-flop is simply the present input to the flip-flop. This gives the following Karnaugh maps and Boolean equations:

For A^+:

X \ AB	00	01	11	10
0	0	1	1	0
1	0	0	0	1

$$\Rightarrow \qquad A^+ = \overline{X}B + XA\overline{B}$$

For B^+:

X \ AB	00	01	11	10
0	0	0	1	0
1	1	0	0	1

$\Rightarrow \qquad B^+ = X\overline{B} + \overline{X}AB$

For Y

X \ AB	00	01	11	10
0	0	0	0	0
1	1	0	0	1

$\Rightarrow \qquad Y = X\overline{B}$

Give 1 mark for each K-map and 1 mark for each Boolean expression.

[6]

c) Using the result of (b) it can be seen that 2 OR gates and 4 AND gates are necessary. Note that the Y term does not need an additional AND gate as it is available within the expression for B^+.

[4]

d) The state transition table may be redrawn with one-hot encoding as follows:

S3S2S1S0	X	$S3^+ S2^+ S1^+ S0^+$	Y^+
0001	0	0001	0
0001	1	0010	1
0010	0	0100	0
0010	0	0001	0
0100	0	0001	0
0100	1	1000	1
1000	0	1000	0
1000	1	0001	0

Give 4 marks for understanding this and for drawing the table.

By inspection of the table:

$$S_3^+ = S_2X + S_3\overline{X}$$

$$S_2^+ = S_1\overline{X}$$

$$S_1^+ = S_0X$$

$$S_0^+ = S_0\overline{X} + S_1X + S_2\overline{X} + S_3X$$

$$Y = S_0X + S_2X$$

Give 2 marks for each expression.

[14]