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EE3-01  
EE9AC1

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING  
EXAMINATIONS 2011

MSc and EEE PART III/IV: MEng, BEng. and ACGI

**ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS**

Tuesday, 10 May 2:30 pm

Time allowed: 3:00 hours

**There are SIX questions on this paper.**

**Answer FOUR questions.**

*All questions carry equal marks*

**Any special instructions for invigilators and information for candidates are on page 1.**

Examiners responsible      First Marker(s) :      C. Toumazou  
Second Marker(s) :      P. Georgiou

1. (a) Figures 1.1 and 1.2 show two popular biasing schemes typically used in analogue integrated systems. Briefly outline the main feature of each of these circuits.

[4]

For the bandgap voltage reference circuit of Figure 1.1, show that  $\delta V_0 / \delta T = 0$  (where  $T$  is temperature) if  $(R_2/R_3) \ln [I_1/I_2] = 29$  for  $V_0 = 1.283$  V. Assume the temperature coefficient of  $V_{BE}$  to be  $-2.5\text{mV}/^\circ\text{C}$ , the collector current of transistor  $Q_3$  is  $100\mu\text{A}$  and the device saturation current is  $I_S = 1.2 \times 10^{-13}$  A. Boltzmann's constant  $k = 1.38 \times 10^{-23}$  J/K and the electron charge is  $q = 1.6 \times 10^{-19}$  C.

[7]

- (b) Show that the circuit of Figure 1.2 can be developed into a current source with output current directly proportional to absolute temperature and virtually independent of supply voltage. Since it is likely that on power-up the output current will fall into a zero current state, sketch a suitable start-up circuit that ensures that this condition will not occur and explain the operation of the circuit.

[9]

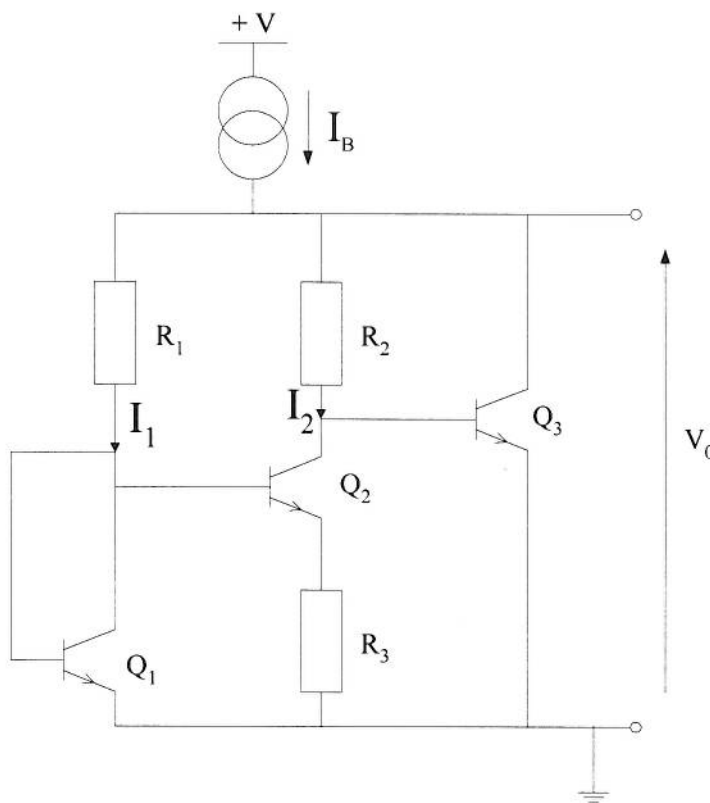


Figure 1.1

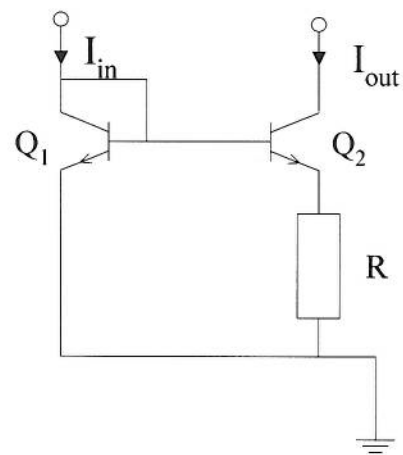


Figure 1.2

2. (a) Sketch a typical circuit diagram for a single-stage fully differential folded cascode CMOS op-amp. Briefly explain the concept of common-mode feedback with reference to your folded cascode op-amp and sketch a common-mode feedback circuit.

[8]

- (b) Estimate the low-frequency differential voltage gain, slew rate and gain-bandwidth product of the two-stage CMOS op-amp shown in Figure 2. Aspect ratios of all devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below.

[10]

- (c) Explain qualitatively why the addition of a resistor in series with compensation capacitor  $C_c$  improves amplifier stability.

[2]

#### CMOS TRANSISTOR PARAMETERS

MODEL PARAMETERS	$K_p$ ( $\mu\text{A/V}^2$ )	$\lambda$ ( $\text{V}^{-1}$ )	$V_{T0}$ (V)
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

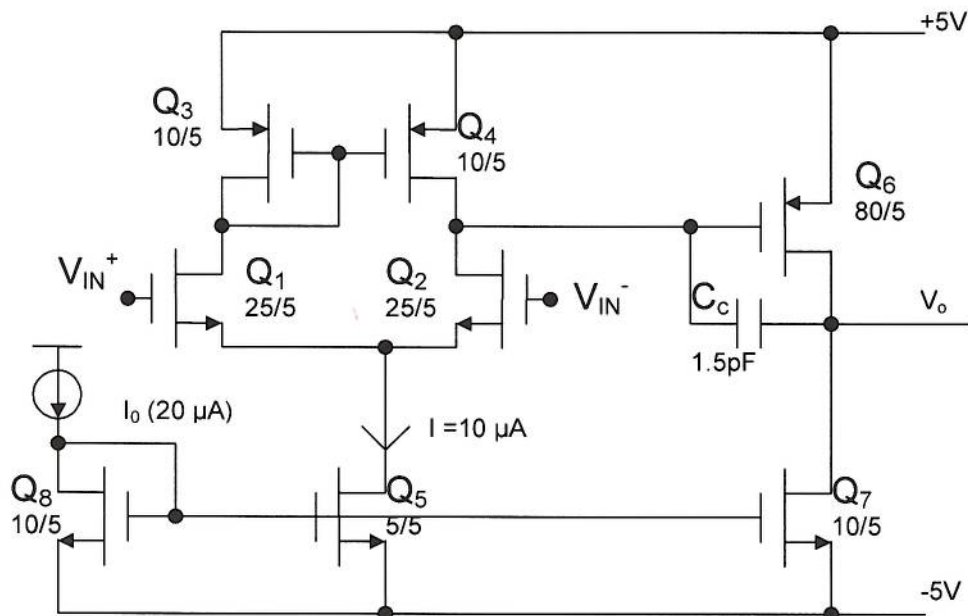


Figure 2

3. (a) Derive an expression for the fundamental limitation imposed on the Dynamic Range (DR) of any high performance A/D converter using the following parameters:  $V_{ref}$  is the reference voltage,  $k$  is the Boltzmann's constant,  $T$  is absolute temperature,  $R$  is switch resistance and  $f_c$  is the clock frequency of the switch. You may assume that the system settles in  $10\tau$  (where  $\tau$  is the time constant), over one period of the clock frequency.

[8]

- (b) A very high resolution analogue-to-digital converter is the oversampling converter sometimes referred to as the sigma-delta modulator. Explain its principles of operation using a diagram where necessary.

[12]

4. (a) Under what operating conditions does the MOSFET of Figure 4.1 realise a linear floating resistor between terminals *A* and *B*? Explain why the bulk is not connected to the source.
- [6]
- (b) Discuss three sources of non-linearity in the single MOSFET resistor realisation of Figure 4.1 and suggest one suitable circuit design to help eliminate one or more of these non-linear terms. Show all necessary circuit analysis to confirm your design.
- [6]
- (c) Figure 4.2 shows a fully differential continuous time integrator using a balanced double differential linear active transresistor. Derive an expression for the time constant of the integrator. You may ignore all bulk effects, and assume all MOSFETs are operating in the triode region.
- [8]

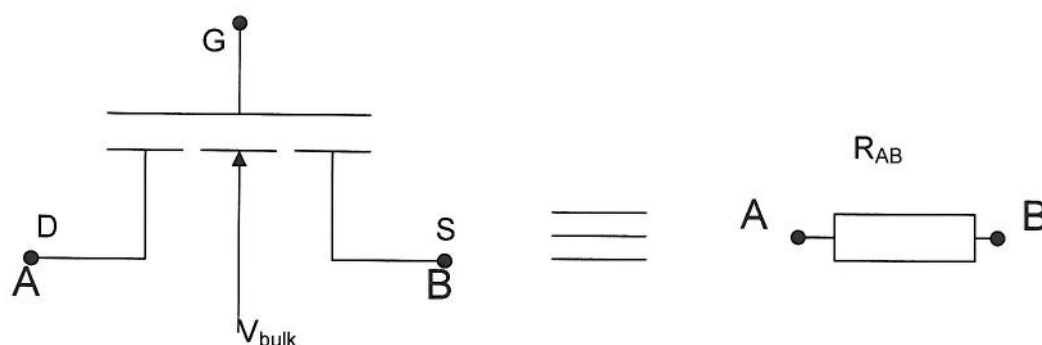


Figure 4.1

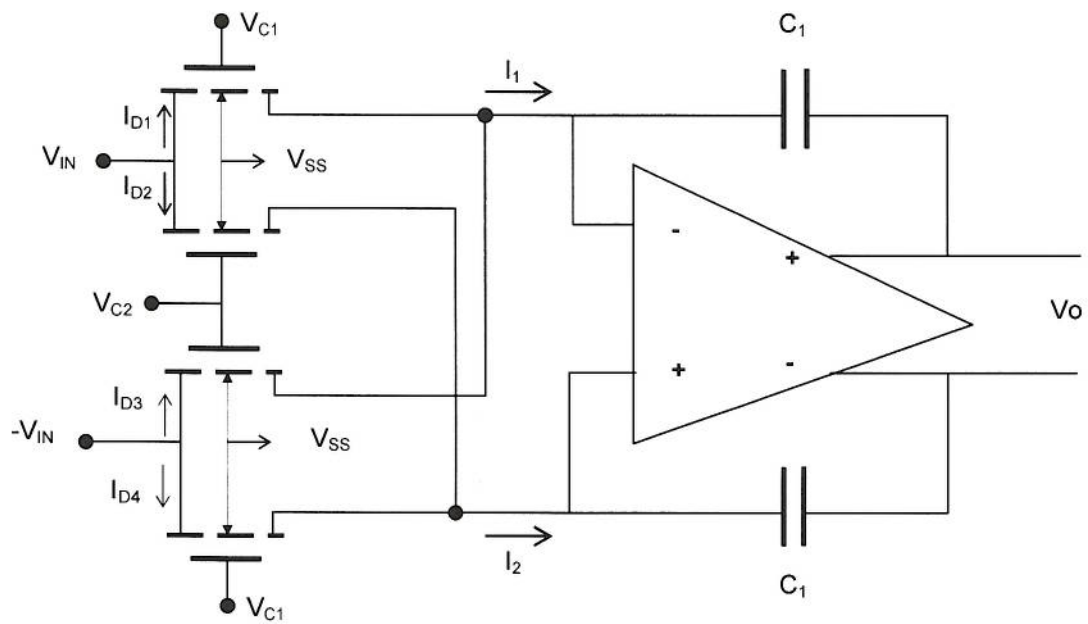


Figure 4.2

5. (a) With the aid of a suitable macromodel, explain the theoretical concept of current feedback and how it results in constant bandwidth amplification. Using a current-feedback op-amp, design a closed-loop non-inverting gain stage with a bandwidth of 10 MHz for a fixed voltage gain of 100. Assume an internal compensation capacitance of 4pF and that the open-loop transresistance gain of the amplifier is very much larger than the amplifier feedback resistor.

[15]

- (b) The circuit shown in Figure 5 is a single bit cell of a current-mode algorithmic analogue to digital converter. Briefly describe the operation of the cell and give reasons why this converter is particularly suitable for mixed-analogue and digital VLSI.

[5]

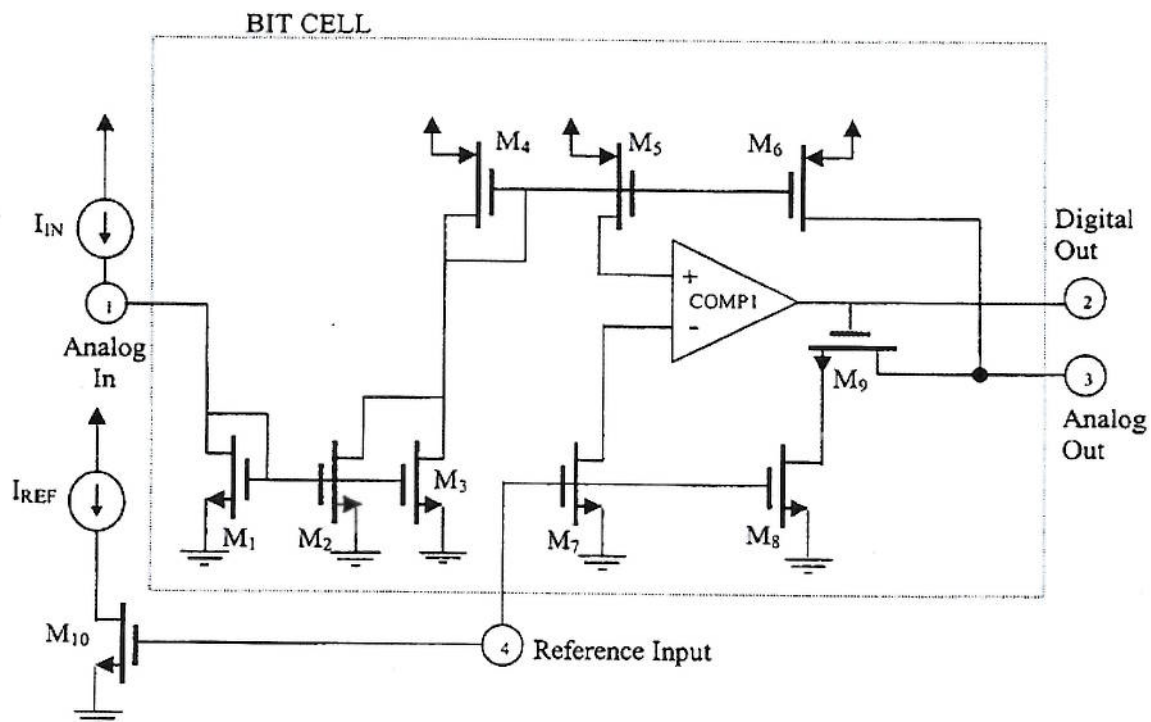


Figure 5



6. (a) Sketch circuits for both a Lossy and differential switched-capacitor integrator. Derive an expression for the transfer function of the differential integrator. Assume clock frequency much higher than the maximum input signal frequency. Also assume the switches are ideal. [10]
- (b) Figure 6 shows one section of a switched capacitor ladder filter. Based on this filter structure, design a 3<sup>rd</sup>-order Chebyshev low-pass filter with a cut-off frequency of 5 kHz and a 1.0 dB pass band ripple. Assume a clock frequency of 100 kHz. Passive component values for the LC prototype, normalised to 1 rad/s, are  $C_1 = C_3 = 2.0236$ ,  $L_2 = 0.994$ . In your analysis assume all integrators to be lossless. [10]

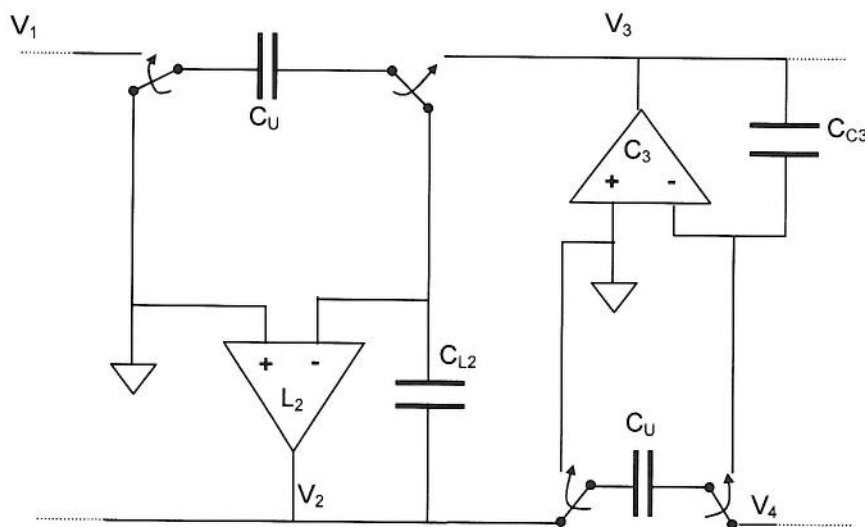


Figure 6

# ANALOG - SOLUTIONS

EXAM 2011

EE3-01  
EE9AC1

1  
18

Q1/ Bandgap voltage reference circuit has almost zero temperature coefficient. Used mainly as stable voltage reference in ICs.

2

PTAT (Proportional to absolute temperature) current generator. Output current usually insensitive to power supply voltage. Used as a biasing circuit in most precision ICs.

2

For BG reference:  $V_{BE1} = V_{BE2} + I_2 R_3$  ( $\beta \gg 1$ )

Since

$$V_{BE1} - V_{BE2} = V_T \ln(I_1/I_2)$$

$$\text{Then } V_0 = V_{BE3} + (R_2/R_3) V_T \ln(I_1/I_2)$$

$V_T \ln(I_1/I_2) \rightarrow$  assume room temp.

$$\text{For } dV_0/dT = 0, \text{ then } dV_{BE3}/dT = \frac{V_T R_2}{T R_3} \ln \frac{I_1}{I_2}$$

$$\text{Since } \frac{dV_{BE}}{dT} = -2.5 \text{ mV}/^\circ\text{C}, \quad \frac{V_T}{T} = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}}$$

$$\text{Then } \left(\frac{R_2}{R_3}\right) \ln\left(\frac{I_1}{I_2}\right) = 29 \text{ and so}$$

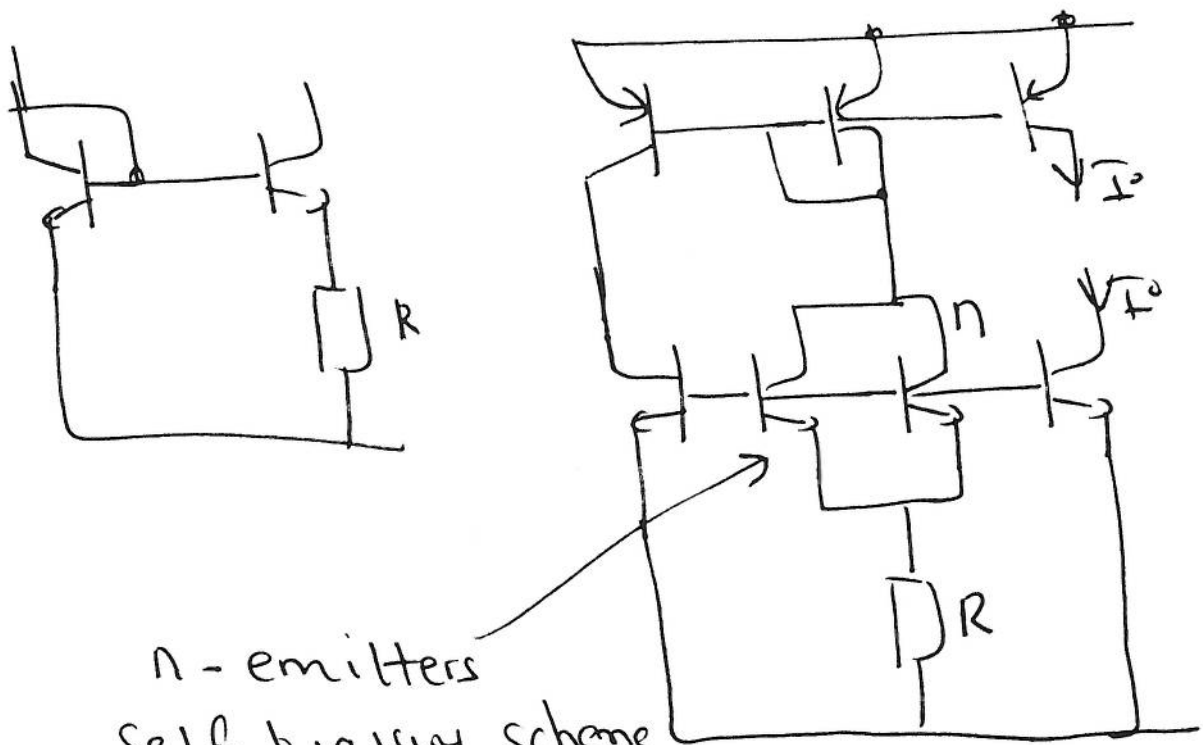
$$V_0 = 1.283 \text{ V}$$

8

(T

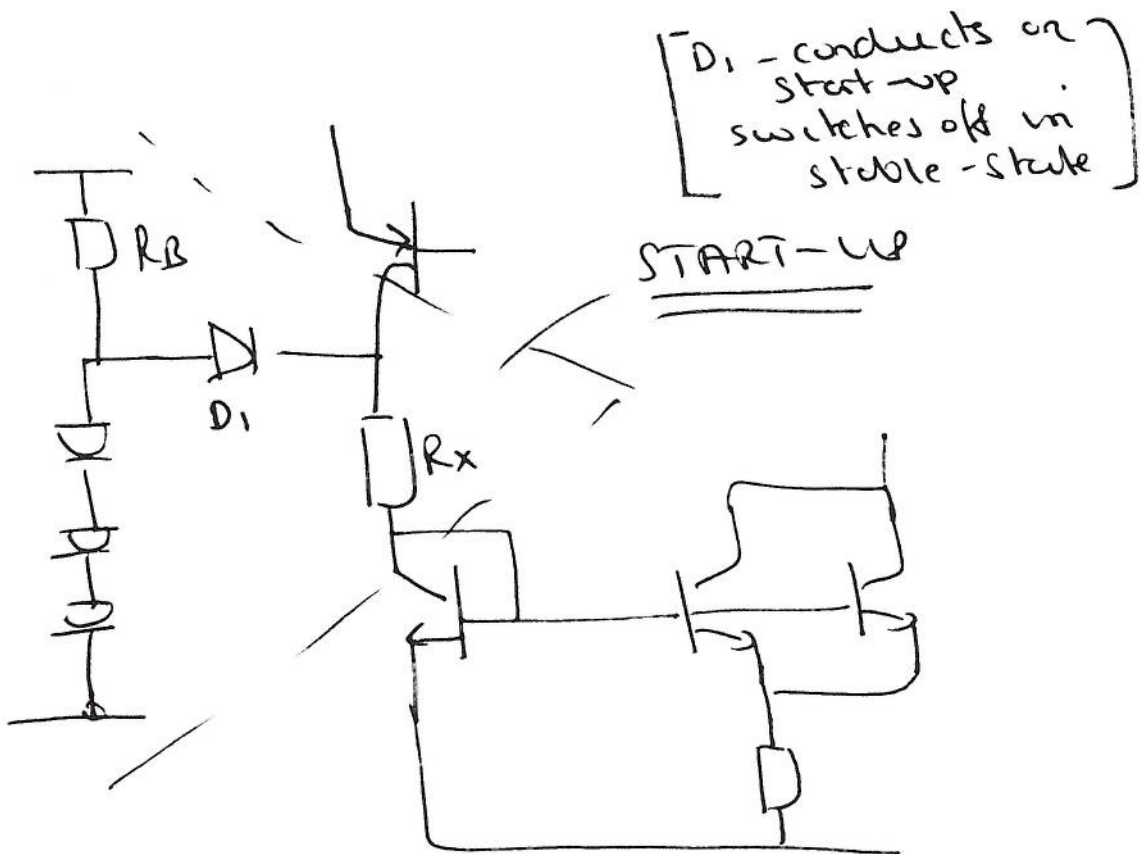
Question 1 continued.

2



n-emitters  
self biasing scheme  
requires start up.

$$I_0 = \frac{V_T}{R} \ln [n]$$



5

4

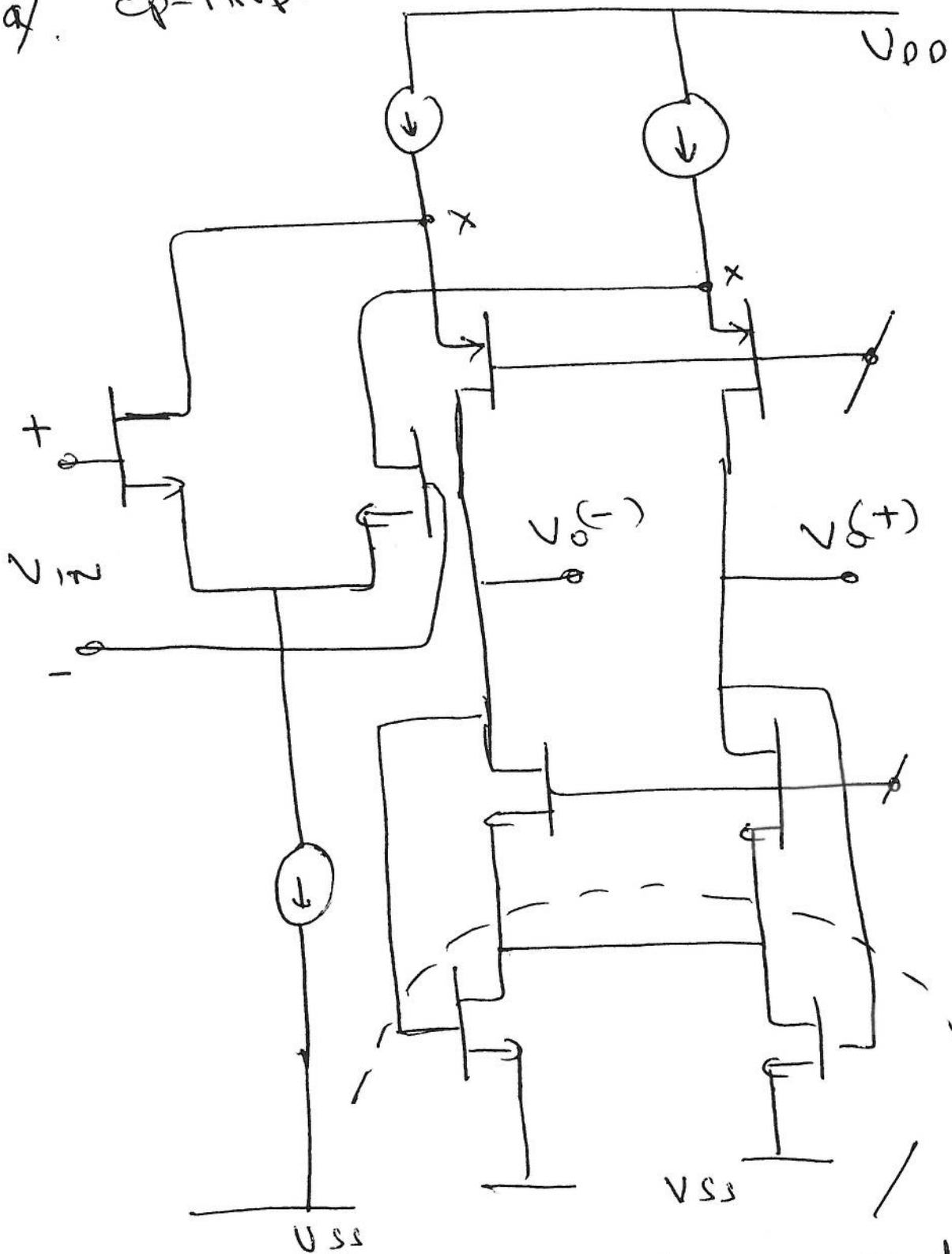
CT

Qu. 2

3

Architecture of folded-cascode

a/ op-amp.



$$A \approx \left(\frac{1}{2}\right) \left(\frac{g_m}{g_{o1}}\right)^2$$

Common-mode feedback.

(T

## Qn2 (cont.)

Single-stage because one current path from input to output.

Node X is low impedance and so very small voltage swing is generated. Only high impedance

node is at the output. (2)  
Not necessary to pole split since dominant pole at output not two stages.

Diff output op-amps with high gain have no way of stabilisation since outputs are undefined (voltage that is).

Common-mode feedback - senses common-mode output and via negative feedback controls the current through the output stage to ensure stable quiescent operating point. Circuit shown in the figure. (2)



an 2 cont

b/. OP-Amp

$$\textcircled{2/2} \quad A_{v1} = -g_{m2} / (g_{o2} + g_{o4})$$

$$(g_{o2} + g_{o4}) = I_{D2} (\lambda_n + \lambda_p)$$

$$= 5 \times 10^{-6} \times 0.05 = 2.5 \times 10^{-7} \Omega^{-1}$$

$$g_{m2} = 2 \sqrt{\beta_2 I_D} \Rightarrow \beta_2 = \frac{k_n}{2} \left( \frac{W}{L} \right)_2$$

$$\beta_2 = 7.5 \times 10^{-5} \text{ A/V}$$

$$\therefore g_{m2} = 3.87 \times 10^{-5} \text{ S}$$

$$\textcircled{2/2} \quad A_1 = \underline{\underline{-154.9}}$$

$$A_n = \boxed{-g_{m6} / (g_{o7} + g_{o6})}$$

$$(g_{o6} + g_{o7}) = I_{D6} (\lambda_{np} + \lambda_n)$$

$$= 20 \times 10^{-6} \times 0.05$$

$$= 10 \times 10^{-7} \Omega^{-1}$$

$\textcircled{2/1}$

$$g_{m6} = 1.13 \times 10^{-4}, \quad A_2 = -113.$$

$$A_T = A_1 A_2 = 17503$$

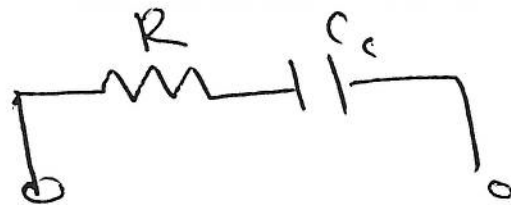
Q2 cont.

$$C.B.P = \frac{g_{m2}}{2\pi C_c} = 4.1 \text{ MHz} \quad - (2)$$

$$S.R = I_0 / C_c = \left( \frac{10}{1.5} \right) \text{ V}/\mu\text{s} \quad - (2)$$

— TOTAL 10/10

Introduce  $R$  in series with  $C_c$



provides feedforward compensation and eliminates RHP Zero in the op-amp's transfer function.

Zero is given by  $Z = -g_{m6}/C_c$  with  $R$

$$Z = -\frac{1}{(1/g_{m6} - R)C_c} \quad \text{Improves } \phi$$

by setting  $Z = P_2 = \text{2nd pole}$  with  $R$ .

(2/2)

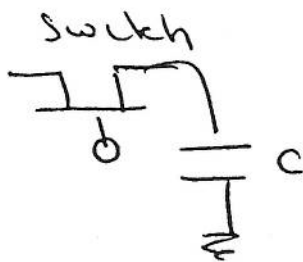
B1

# Constraints

Qn 3

7.

a.) Dynamic Range  $\Delta V_{ref}/noise = 2^N$



Rms noise of switch  
driving Capacitor  
 $= \sqrt{\frac{kT}{C}}$

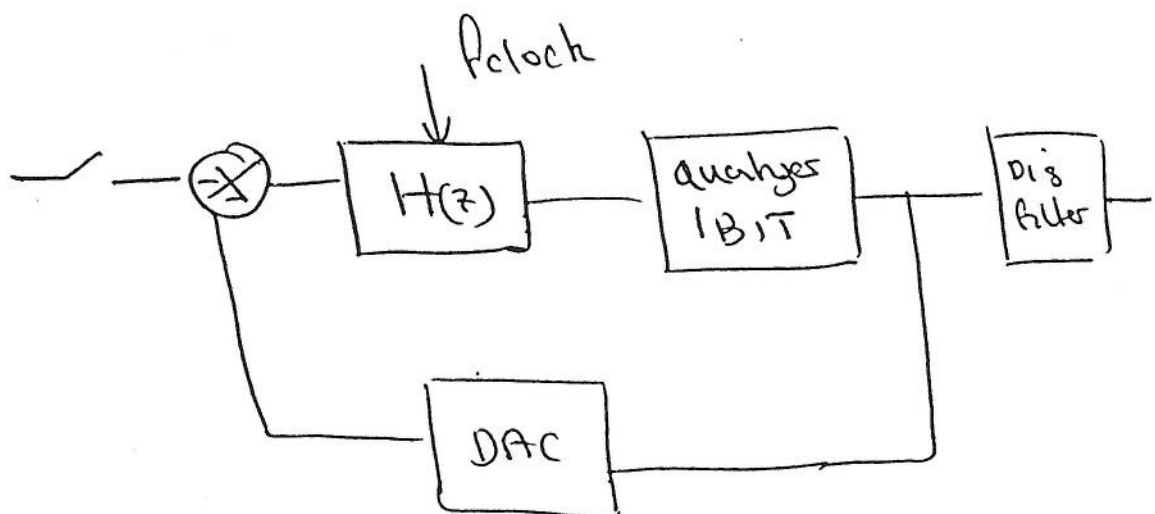
$$\therefore DR = \frac{V_{ref}}{\sqrt{\frac{kT}{C}}} = 2^N$$

Assume  $f_c = 1/(10RC)$

then solving for C gives

$$DR = 2^N = V_{ref} / \sqrt{kT \cdot 10RC}$$

b.)



Basic idea is that coarse quantization noise gets shaped by  $1/(Hz)$  via feedback

8/8

Ct



Generally  $H(z)$  is an Integrator so noise is shaped differentially. This reduces requirements upon component accuracy.

The architecture includes a negative feedback loop producing the coarse estimate that oscillates about the true value of input, the digital filter averages this coarse estimate to produce a finer approximation. The feedback DFE and forward integrator force the quantization error to have a high frequency spectrum. The output of the digital filter is downsampled and given a multi-bit digital representation. High frequency quantization noise is reduced. Noise shaped away very high  $(S/N)$  at low frequency.

# QUESTION 4

Q4

- a) Assumption is that if  $(V_{DS} \geq 0)$  or  $(V_{DS} < V_{GS} - V_T)$  device acts in linear region. From

$$I_D = \frac{\kappa W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] (1 + \lambda V_{DS})$$

for  $V_{DS} < (V_{GS} - V_T)$ , then  $\lambda V_{DS} \ll 1$

$$\text{So } I_D = \frac{\kappa W}{L} (V_{GS} - V_T) V_{DS}$$

6/6

$$\text{OR } R_{AB} = V_{DS} / I_D = L / (\kappa W (V_{GS} - V_T))$$

- b) Three sources of non-linearity
- (i) limited due to  $V_{BS}$  changing  $V_T$  for negative  $V_{DS}$  due to body effect.  
i.e.  $V_T = V_{T0} + \gamma \left[ \sqrt{-V_{BS} + 2\phi_F} - \sqrt{2\phi_F} \right]$   
 $\gamma$  = bulk threshold parameter  
 $\phi_F$  = Fermi-level potential

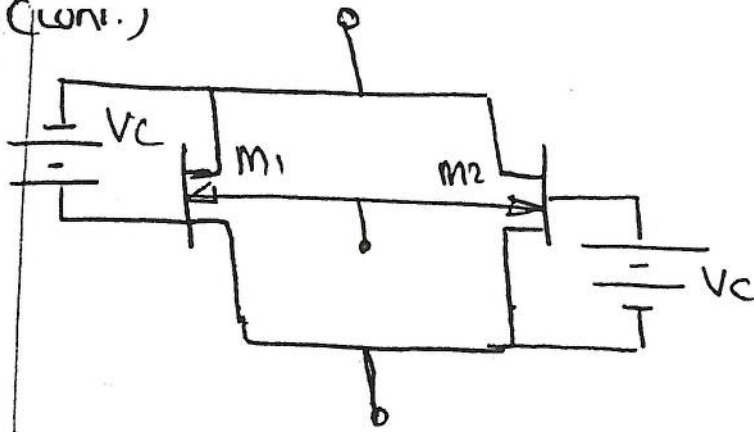
- (ii) limited due to  $V_{DS}$  approaching  $(V_{GS} - V_T)$  hence saturation region for large positive  $V_{DS}$ .

- (iii) For large values of  $V_{DS}$  the  $V_{DS}^2/2$  term comes in making the resistor quite non-linear.

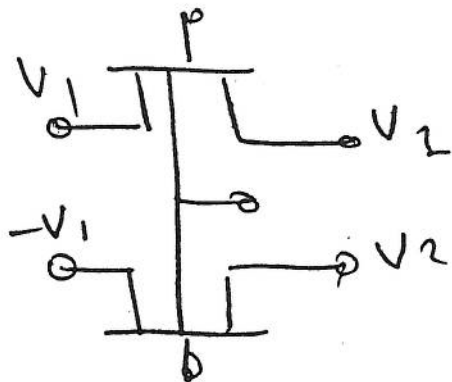
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Q4 (cont.)

10

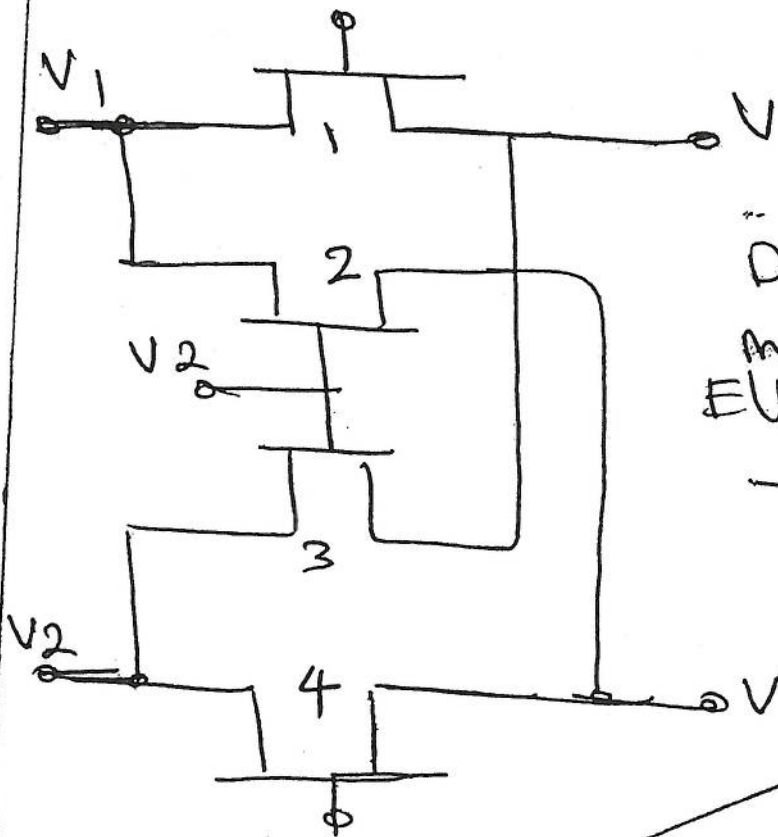


Parallel current - eliminates  $V_{ds}^2/2$  term.



Differential scheme

Effects of  $V_{ds}$  cancelled.



Double differential MOS.  
Eliminates  
-  $V_{ds}$  and  $V_T$  term.

Any one  
of these  
will do!

2/2

Q4 cont,

Double differential integrals

$$I_{D1} = 2\beta [(V_{C1} - V - V_T)(V_1 - V) - \frac{1}{2}(V_1 - V)^2]$$

$$I_{D2} = 2\beta [(V_{C2} - V - V_T)(V_1 - V) - \frac{1}{2}(V_1 - V)^2]$$

$$I_{D3} = 2\beta [(V_{C2} - V - V_T)(V_2 - V) - \frac{1}{2}(V_2 - V)^2]$$

$$I_{D4} = 2\beta [(V_{C1} - V - V_T)(V_2 - V) - \frac{1}{2}(V_2 - V)^2]$$

Expanding it can be shown that:-

$$(V_1 - V_2)/(I_1 - I_4) = 1/2\beta(V_{C1} - V_{C2}) = R$$

Independent of both  $V_T$  and  $V_{DS}$  terms

$$\text{Hence } N = \frac{2CR}{1} = \left[ \frac{C}{\beta(V_{C1} - V_{C2})} \right]$$

8/8

—————//—————



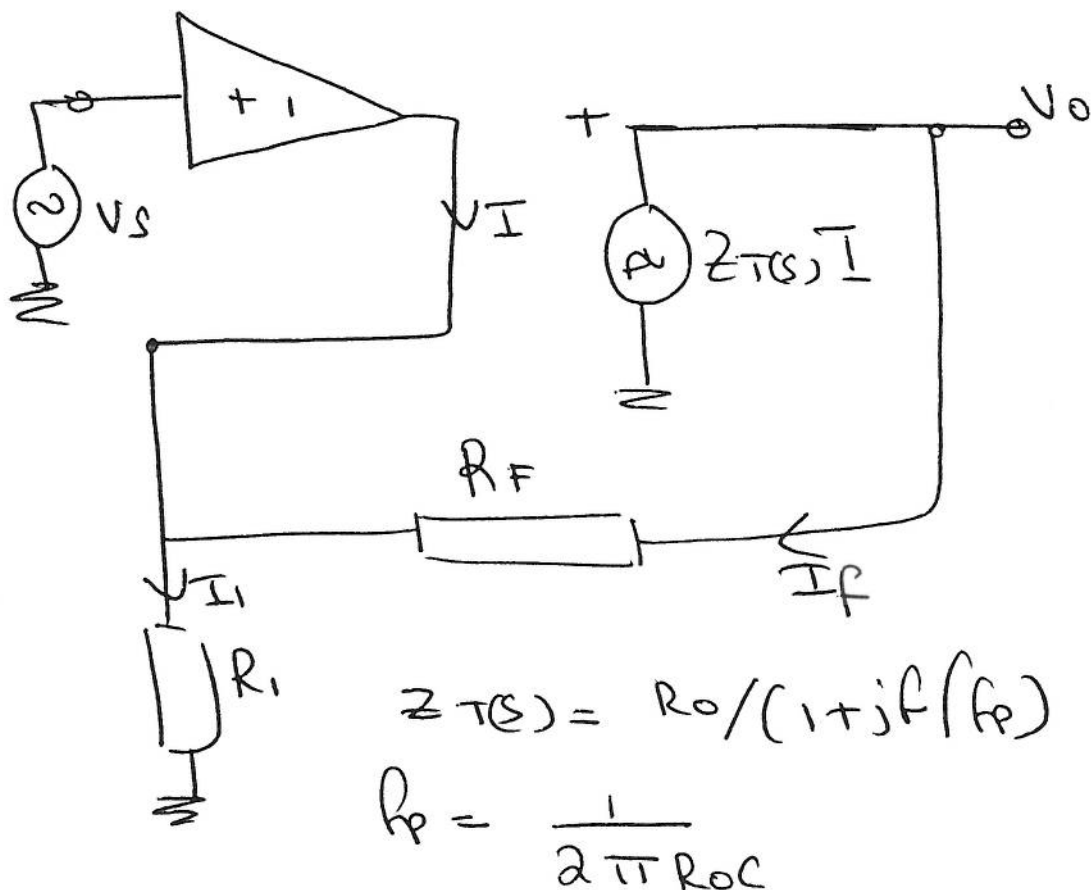
Q5

Advantages of Current-mode

1) High frequency performance, wide dynamic range

low power supply voltages

2



C = compensation capacitor

3 equations

$$I_f = (V_o - V_s) / R_F \quad \text{--- (1)}$$

$$I_1 = V_s / R_1 \quad \text{--- (2)}$$

$$V_o = Z_T(s) I = Z_T(s) [I_1 - I_f] \quad \text{--- (3)}$$

8

15

Q 5 cont/d...

13

Subs ① and ② into ③ gives,

$$(V_o/V_s) = (1 + R_F/R_i) Z^{-1}(s) / (R_F + Z(s))$$

Subs for  $Z^{-1}(s)$

gain

$$(V_o/V_s)_{sw} = (1 + R_F/R_i) \left[ \frac{R_o}{R_o + R_F} \right]$$

$$\times \frac{1}{\left( 1 + jf / \underbrace{f_p \left[ \frac{R_o + R_F}{R_F} \right]} \right)}$$

Assuming  $R_o \gg R_F$  BW

Then

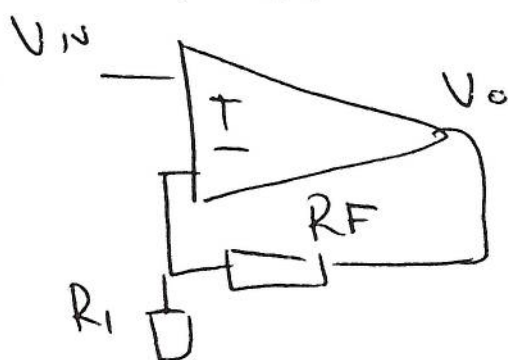
Closed loop gain  $\approx (1 + R_F/R_i) - *$

$$\text{Closed loop Bandwidth} \approx \frac{f_p R_o}{R_F} = \frac{1}{2\pi R_F C}$$

Hence  $R_F$  sets the amplifier  
constant BW

and  $R_i$  chosen to set the gain

Lx.



$$BW = \frac{1}{2\pi R_F C} = 10 \text{ MHz}$$

$\therefore$  Given  $C = 4 \text{ pF}$

$$R_F = 3.98 \text{ k}\Omega$$

$$\text{Since } A = (1 + R_F/R_i) = 100$$

$R_i = 39.8 \text{ k}\Omega$

5

Q 5 cont/d...

### Analytic Converter

$2I_{in}$  on +ve terminal of comparator  
compared to  $I_{ref}$  (-ve) terminal

If  $2I_{in} < I_{ref}$ , comp output goes low

digital output = 0 and analogue  
output =  $2I_{in}$

If  $2I_{in} > I_{ref}$ , comp output goes high

digital output = 1, analogue output  
 $2I_{in} - I_{ref}$

Analogue output consequently feeds  
into following 'bit' which  
performs exactly the same function.

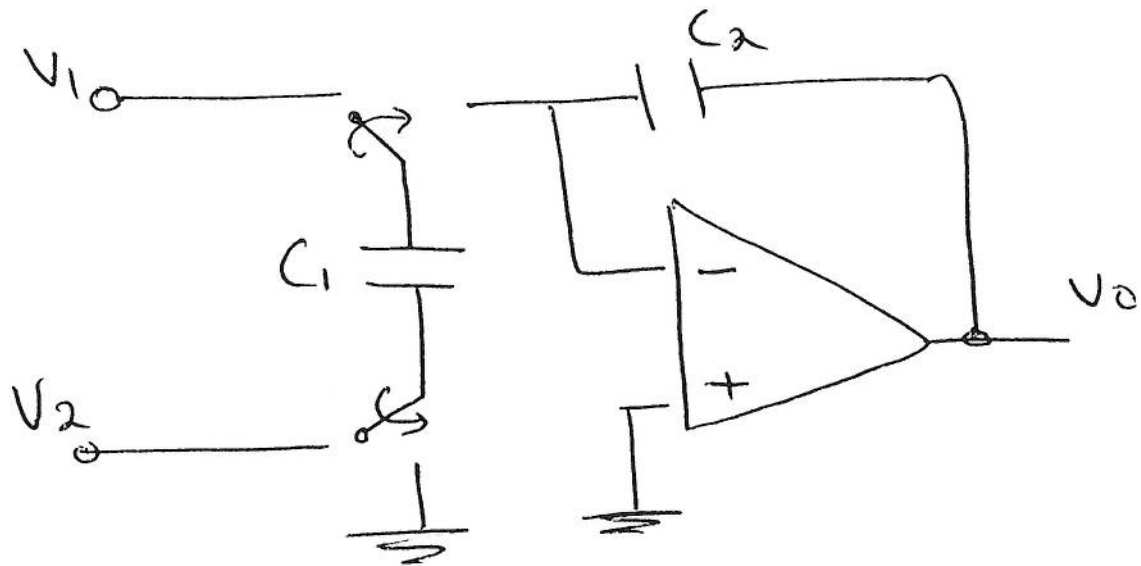
The process is repeated as many times  
as necessary to achieve desired  
resolution.

Digital VLSI — small size,  
low-power  
supply voltages  
less stringent  
upon analogue accuracy

Qu 6/

15

a) Differential Integrator



During  $\phi_1$   $Q = C_1 [V_1 - V_2]$

$$I_{av} = f_c C_1 [V_1 - V_2]$$

$f_c$  = clock frequency

$$\text{During } \phi_2 \Rightarrow I_{av} = -f_c (V_1 - V_2) C_1$$

$$\therefore V_0 = \frac{-1}{j\omega C_2} f_c C_1 [V_1 - V_2]$$

$$\therefore \frac{V_0}{(V_1 - V_2)} = -\frac{f_c}{j\omega} \frac{C_1}{C_2} \approx T = \frac{C_2}{C_1} f_c$$

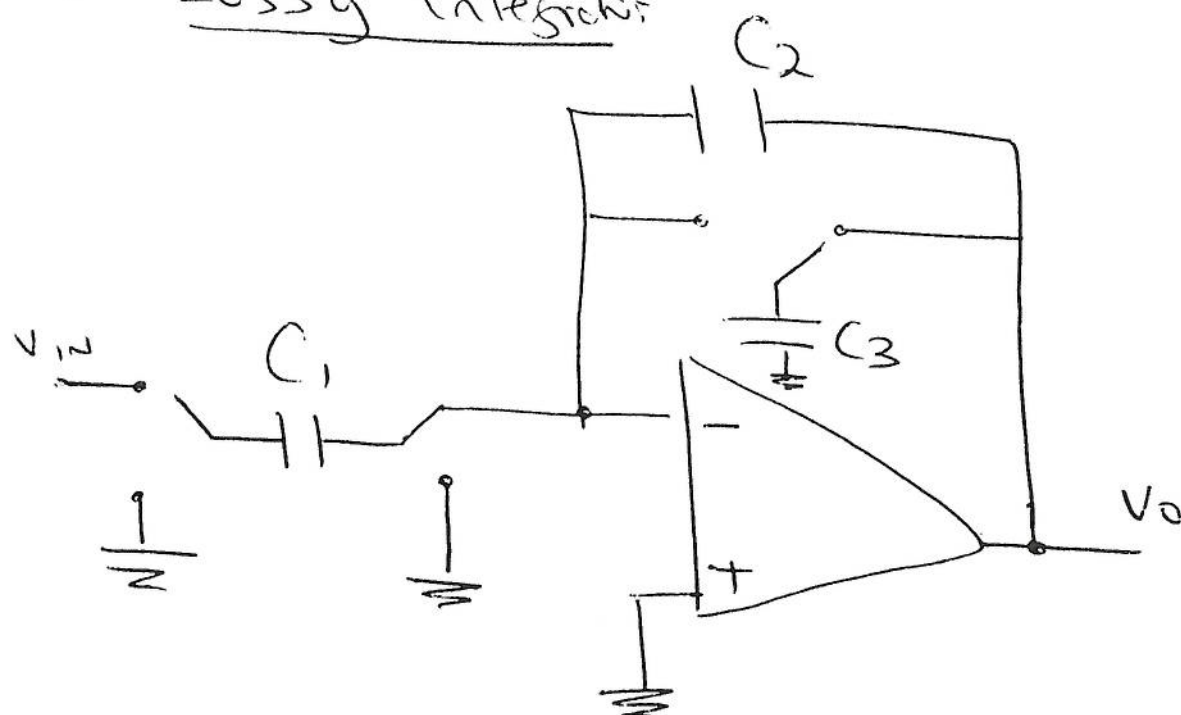
(5/5)

LT



# Q6 Lossy Integrator

16



During  $\phi_1$   $Q = C_1 V_{in} \Rightarrow I_{avg} = f_c C_1 V_{in}$

During  $\phi_2$

$$I_{avg} = -[f_c C_3 V_o + j\omega C_2 V_o]$$

$$\therefore f_c C_1 V_{in} = -[f_c C_3 V_o + j\omega C_2 V_o]$$

$$V_{in} = -\left[\frac{C_3}{C_1} V_o + \frac{j\omega C_2 V_o}{C_1 f_c}\right]$$

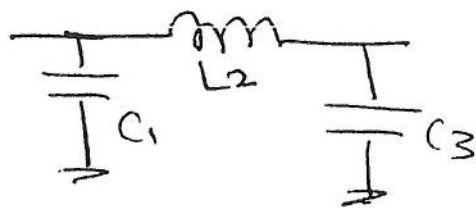
$\therefore \frac{V_o}{V_{in}} = -\frac{C_1}{C_3} \left( \frac{1}{1 + \frac{C_2 j\omega}{C_3 f_c}} \right)$

$\therefore T = \left( \frac{C_2}{C_3} \right) \frac{1}{f_c}$

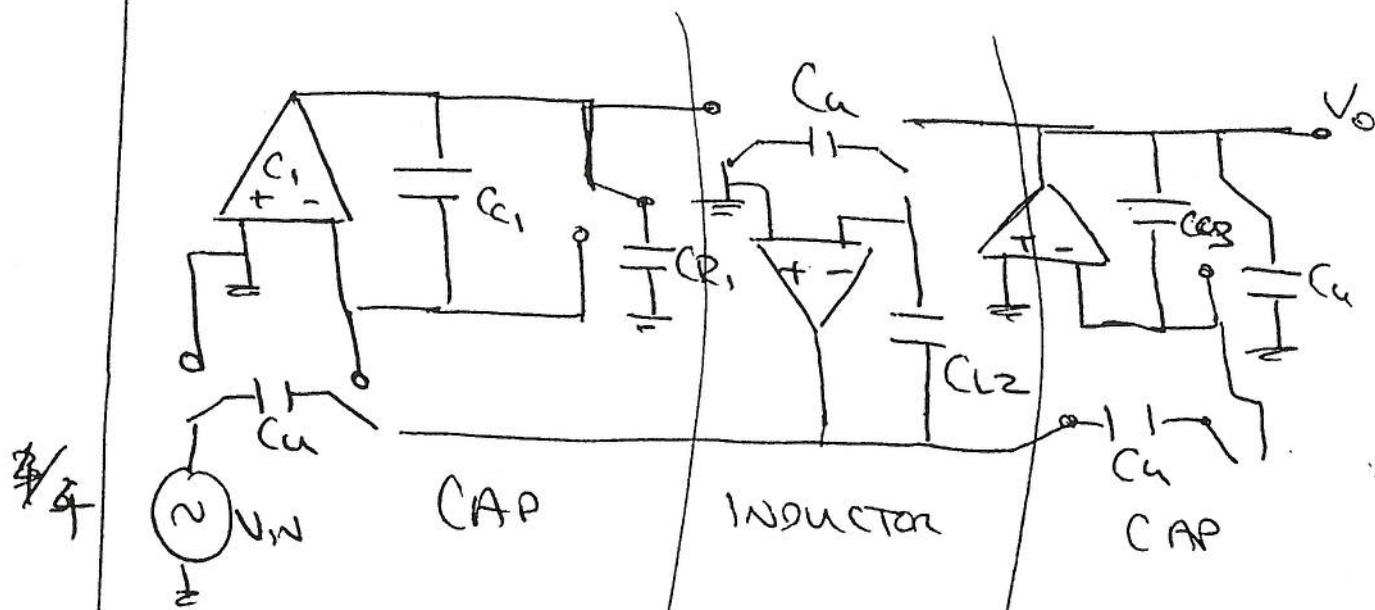
Q6

Q6

Section of LCR prototype.



General transformation Rules (not really required but the bright students may include)



Conversion into differential integrals.

Inductor transformation

$$(L_2/R_s) f_c = C_{12}/C_u$$

Capacitor transformation.

$$C_3/C_u = f_c R_s C_3$$

where  $R_s$  is normalising during scaling resistor. Assuming  $R_s = 1$

$$C_1/C_u = f_c C_1$$

$$C_3/C_u = f_c C_3$$

$$C_{12}/C_u = f_c L_2$$

general transformation

and ...

Table values of  $C_1$ ,  $L_2$  and  $C_3$   
are normalized to  $1 \text{ rad/s} \div 2\pi f_p$

$$f_p = 5 \text{ kHz}$$

$$C_1 = C_3 = 2.0236 / (2\pi 5 \times 10^3) \\ = 6.44 \times 10^{-5} \text{ F}$$

$$C_{L2} = 0.994 / (2\pi 5 \times 10^3) \\ = 3.164 \times 10^{-5} \text{ F}$$

For termination  $R_s$

assume  $C_{u1} = C_{r1} = C_{r0} = 1 \text{ pF}$

Then

$$\left[ \begin{array}{l} C_{L1} = C_{L3} = 6.44 \text{ pF} \\ C_{L2} = 3.164 \text{ pF} \end{array} \right]$$

6/6

to get 20/20