IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2011

EEE/ISE PART I: MEng, BEng and ACGI

Corrected Copy

ANALOGUE ELECTRONICS 1

Monday, 13 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : A.S. Holmes
Second Marker(s) : G.A. Constantinides

The Questions

1. For each part of this question, state clearly any assumptions made in your calculations.

   a) For the circuit in Figure 1.1, determine the voltage at the collector of the transistor.

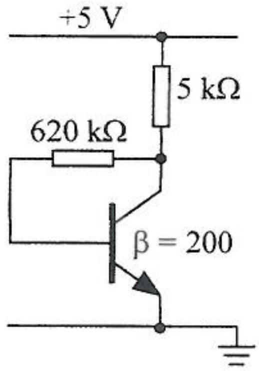


Figure 1.1 [6]

   b) For the circuit in Figure 1.2, determine the operating modes of both MOSFETs and the value of the voltage V.

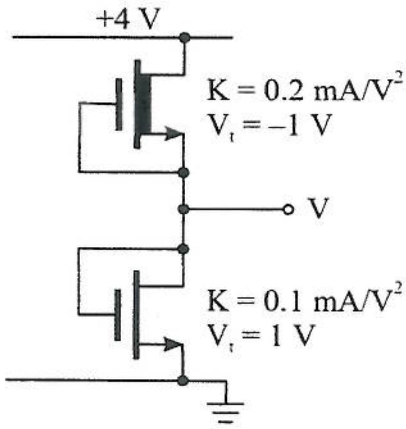
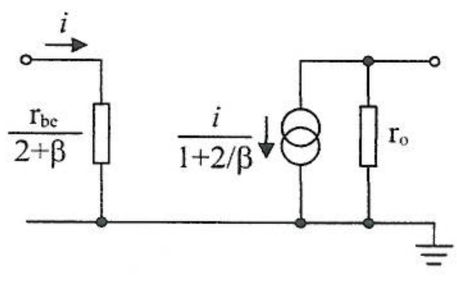


Figure 1.2 [6]

   c) Sketch the circuit for a simple BJT current mirror. Also draw the small-signal equivalent circuit and show that, if the transistors are matched, it can be reduced to the following approximate form:



[8]

Question 1 continues on the next page...

Question 1 continued

d) Using the resistance reflection rule, or otherwise, determine the small-signal output resistance of the circuit in Figure 1.3.

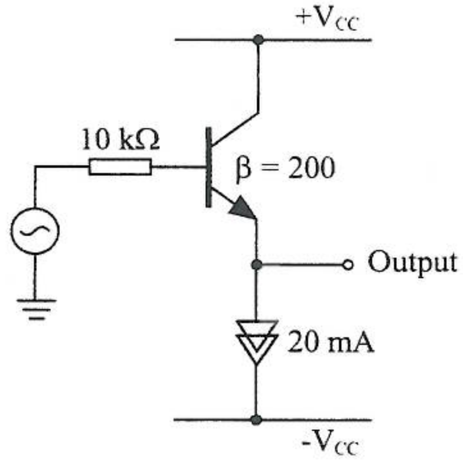


Figure 1.3

[6]

e) For the Darlington pair shown in Figure 1.4, determine the operating modes of the two transistors and the value of the current I.

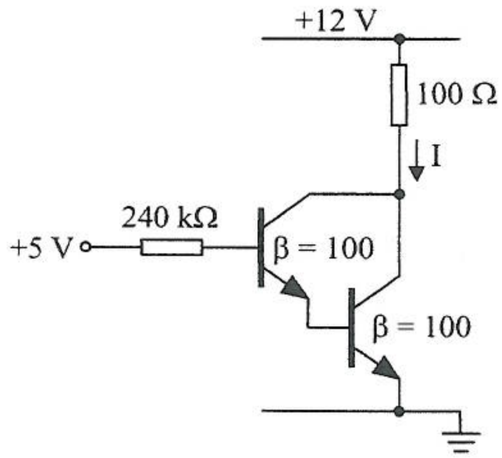


Figure 1.4

[8]

f) The characteristic equation for a Wien Bridge oscillator is of the form:

$$(1 - K)sR_2C_1 + (1 + sR_1C_1)(1 + sR_2C_2) = 0$$

where R_1, R_2, C_1 and C_2 are the components in the frequency-selective network, K is the amplifier gain, and s is complex frequency. Derive expressions for the value of K required for stable oscillation, and for the oscillation frequency. [6]

2. Figure 2.1 shows a common-emitter amplifier, connected between an AC-coupled signal source and a capacitive load. The transistor has a β value of 200.

   a) Determine the collector bias current and quiescent output voltage of the amplifier, stating clearly any assumptions you make. Your calculation should take into account the base current of the transistor. [8]

   b) Draw a small-signal equivalent circuit for the amplifier, replacing the RC network in the emitter by an equivalent impedance Z_E, and show that the small-signal voltage gain may be written as:

$$A_V = \frac{-\alpha R_C}{r_e + Z_E}$$

   where R_C is the load resistance in the collector and r_e is the small-signal emitter resistance of the transistor. You may neglect the small-signal output resistance of the transistors. Hence evaluate A_V both in the mid-band, where C_E is effectively short-circuit, and at low frequency where C_E is effectively open-circuit. [12]

   c) Choose the value of C_E so that the 3-dB point at the low-frequency end of the mid-band occurs at 1 kHz. Also determine the cut-off frequency associated with the load capacitor, and hence sketch a Bode plot showing the variation of the in-circuit gain v_L/v_S with frequency over the frequency range 1 Hz to 1 MHz. You should ignore the effect of the AC-coupling capacitor at the input. [10]

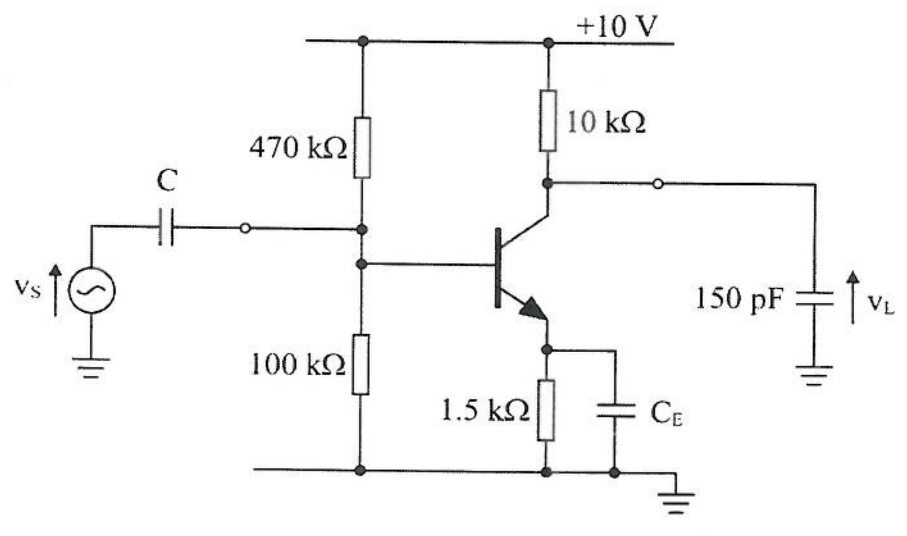


Figure 2.1

3. Figure 3.1 shows an NMOS amplifier employing two enhancement mode MOSFETs.

a) Neglecting the current in the bias resistors, and assuming both transistors are active, show that the output voltage V_{OUT} may be expressed as:

$$V_{OUT} = V_{DD} - V_{t2} - \sqrt{\frac{K_1}{K_2}} \cdot (V_{G1} - V_{t1})$$

where K and V_t denote the usual MOSFET parameters, V_G denotes gate voltage, and subscripts 1 and 2 refer to Q1 and Q2 respectively. [10]

b) By considering the constraint imposed on V_{OUT} and V_{G1} by the bias network, calculate the quiescent output voltage and the quiescent drain current in each MOSFET. Also confirm that both MOSFETs are indeed active under quiescent conditions. What is the minimum supply voltage at which the amplifier could be operated? [12]

c) Using the equation in part a), or otherwise, calculate the voltage gain of the amplifier in the mid-band where the input capacitor is effectively short-circuit. Also determine the range of output voltages over which this voltage gain will be achieved. [8]

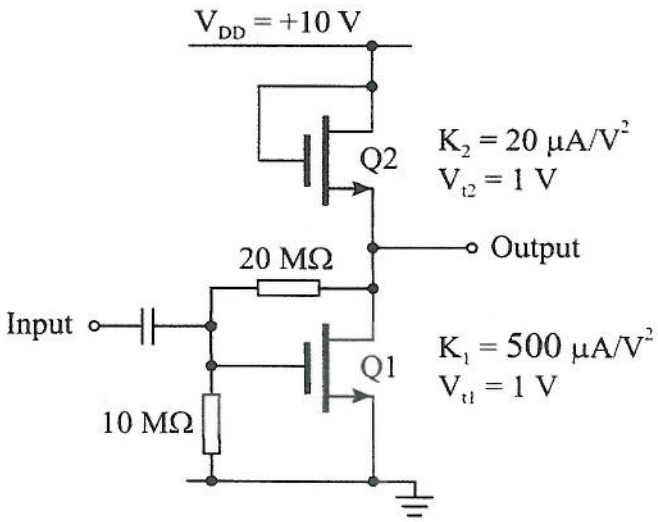


Figure 3.1

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1. a) Transistor is active, so $I_B = (V_C - V_{BE})/R_B = I_E/(1+\beta)$; also $I_E = (V_{CC} - V_C)/R_C$.

Eliminating I_E:
$$(V_C - V_{BE})\, R_C = (V_{CC} - V_C)\, R_B/(1+\beta)$$
$$\Rightarrow V_C\,[R_C + R_B/(1+\beta)] = V_{CC}R_B/(1+\beta) + V_{BE}R_C$$

Assuming $V_{BE} = 0.7$ V, $V_C = [5\times620\text{k}/201 + 0.7\times5\text{k}]/[5\text{k} + 620\text{k}/201] = \mathbf{2.34\ V}$ [6]

b) Both devices are above threshold and conducting. To see this note that: (1) the upper device Q2 has $V_{GS} = 0 > V_t$ and will carry current for any $V_{DS} > 0$, (2) the lower device Q1 will carry current for any $V_{DS} > 1$ V, and (3) the sum of the two V_{DS} values is fixed at 4 V.

Also, lower device Q1 is enhancement mode and D-G connected $\Rightarrow$ **Q1 ACTIVE**

Mode of upper device depends on V, but let's assume initially it is active (easier calculation). In this case we have:
$$I_D = K_2V_{t2}^2 = 0.2\text{m} \times (-1)^2 = 0.2\text{ mA}$$

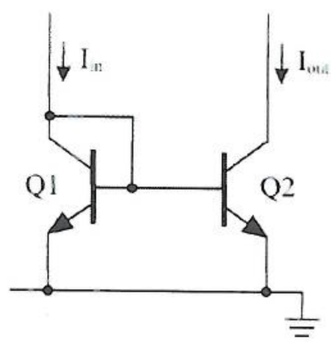
and, since Q1 carries same current:
$$I_D = K_1(V - V_{t1})^2$$

Rearranging and taking +ve √ (to ensure Q1 above threshold):
$$V = V_{t1} + \sqrt{(I_D/K_1)} = 1 + \sqrt{(0.2\text{m}/0.1\text{m})} = 1 + \sqrt{2} = 2.42\text{ V}$$

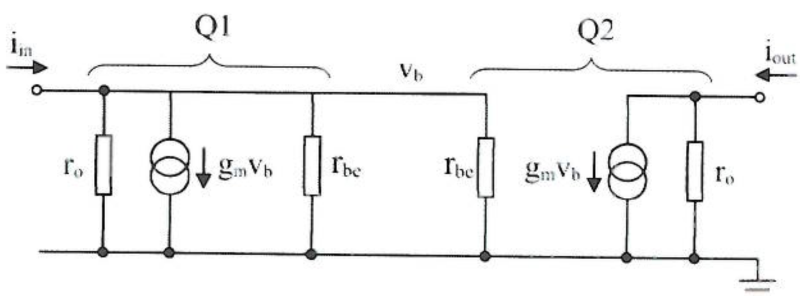
Check mode of Q2: $V_{DS} = 4 - 2.42 = 1.58\text{ V} > (V_{GS} - V_t) = 1\text{ V} \Rightarrow$ **Q2 ACTIVE**

Since active mode assumption was correct, V value stands i.e. $\mathbf{V = 2.42\ V}$ [6]

c) Simple BJT current mirror:



SSEC:



KCL at the input gives:

$$i_{in} = v_b/r_o + g_m v_b + v_b/r_{be} + v_b/r_{be}$$

Since $r_o >> r_{be} >> 1/g_m$, the first term will be relatively small, and we can write:

$$i_{in} \approx g_m v_b + 2v_b/r_{be} = (\beta + 2)v_b/r_{be}$$

where we have used the relation $g_m = \beta/r_{be}$. So, the input side of the current mirror appears as a resistor of value:

$$R_{in} = v_b/i_{in} \approx r_{be} /(\beta + 2)$$

Also, the output side current source can be expressed as:

$$g_m v_b = g_m R_{in} i_{in} \approx i_{in} (\beta/r_{be})\cdot r_{be} /(\beta + 2) = i_{in} /(1 + 2/\beta)$$

The SSEC can therefore be reduced to the approximate form shown. [8]

d) Resistance reflection rule says: $R_o = R_S/(1 + \beta) + r_e$

With $R_S = 10\ k\Omega$, $r_e = V_T/I_E = 25\ mV/20\ mA = 1.25\ \Omega$, and $\beta = 200$, we get $\mathbf{R_o = 51.0\ \Omega}$ [6]

(NB this is very easy if student knows reflection rule; otherwise it is more work)

e) Assuming $V_{BE} = 0.7$, the base current of the LH transistor Q1 will be:

$$I_{B1} = (5 - 1.4)/240k = 15\ \mu A$$

If both transistors are active, the total output current will be:

$$I = I_{C1} + I_{C2} = \beta I_{B1} + \beta(\beta + 1)I_{B1} = \beta(\beta + 2)I_{B1} = 100\times 102\times 15e\text{-}6 = 153\ mA$$

But this would imply a collector voltage of $12 - 0.153\times 100 = -3.3$ V which is not possible.
⇒ LH transistor is SATURATED, and RH transistor is ACTIVE

Assuming $V_{CEsat} = 0.2$ V, the collector voltage is 0.9 V, and $I = (12 - 0.9)/100 =$ **111 mA** [8]

f) For stable oscillation, the characteristic equation needs to be satisfied for $s = j\omega$ where ω is the oscillation frequency. Substituting $s = j\omega$ into the given equation we obtain:

$$j\omega(1 - K)R_2C_1 + (1 + j\omega R_1C_1)(1 + j\omega R_2C_2) = 0$$

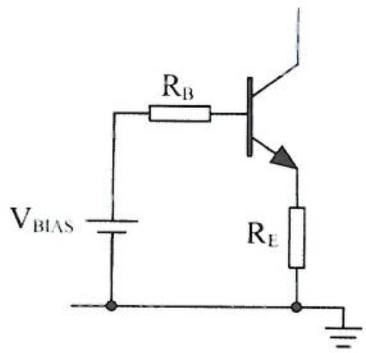
Multiplying out and collecting together real and imaginary terms:

$$1 - \omega^2 R_1C_1R_2C_2 + j\omega[(1 - K)R_2C_1 + R_1C_1 + R_2C_2] = 0$$

Re{LHS} = 0 $\Rightarrow \boldsymbol{\omega = 1/\sqrt{(R_1C_1R_2C_2)}}$ oscillation freq

Im{LHS} = 0 $\Rightarrow \mathbf{K = 1 + R_1/R_2 + C_2/C_1}$ required K value [6]

2. a) Replacing input resistor network by Thévenin equivalent, bias circuit reduces to:



$V_{BIAS} = 10\times100/(100 + 470) = 1.754$ V

$R_B = 100k//470k = 82.5k$

KVL then gives: $I_ER_E + V_{BE} + I_BR_B = V_{BIAS}$

$\Rightarrow\ I_E = (V_{BIAS} - V_{BE})/[R_E + R_B/(1 + \beta)]$

Assuming $V_{BE} = 0.7$ V,

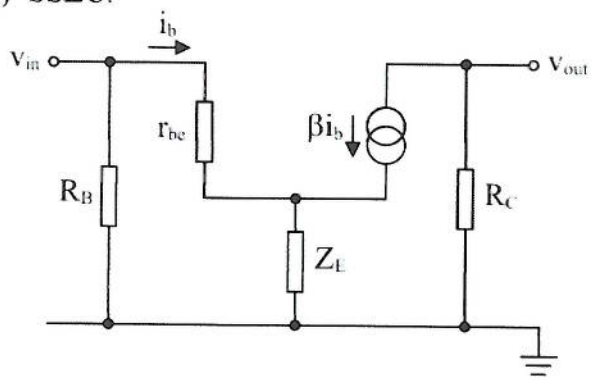
$I_E = (1.754 - 0.7)/(1.5k + 82.5k/201) = 0.552$ mA

$I_C = \alpha I_E = 200\times552/201 = \mathbf{0.549\ mA}$

$V_{OUT} = 10 - 0.549\times10 = \mathbf{4.51\ V}$

[8]

b) SSEC:



KVL on input side:

$$i_br_{be} + (1+\beta)i_bZ_E = v_{in}$$

KVL on output side:

$$-\beta i_bR_C = v_{out}$$

$\Rightarrow A_v = v_{out}/v_{in} = -\beta R_C/[r_{be} + (1 + \beta)Z_E]$

Using $r_e = r_{be}/(1 + \beta)$ this reduces to

$$A_v = -\alpha R_C/(r_e + Z_E)$$

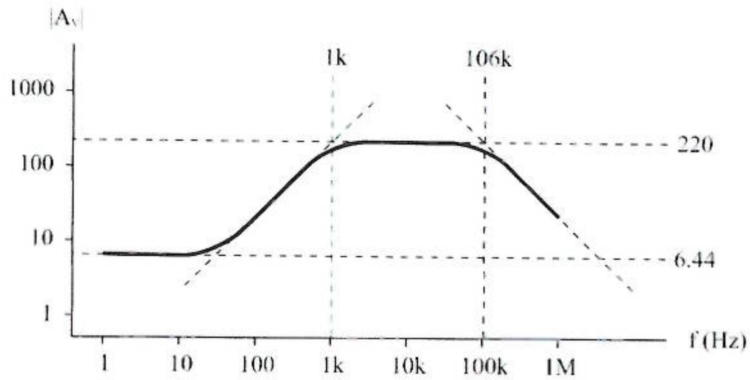
$r_e = V_T/I_E = 25m/0.552m = 45.3\ \Omega$

In mid-band, where $Z_E \rightarrow 0$, $A_v = -\alpha R_C/r_e = \mathbf{-220}$

At low frequency, where $Z_E \rightarrow 1.5\ k\Omega$, $A_v = -\alpha R_C/(r_e + Z_E) = \mathbf{-6.44}$ [12]

c) At low end of mid-band, $Z_E \approx 1/j\omega C_E$ and a HP filter is formed with r_e. The cut-off frequency is therefore given by $\omega_cr_eC_E = 1$ or $f_c = 1/(2\pi r_eC_E)$. With $r_e = 45.3\ \Omega$, for a cut-off at 1 kHz we require $C_E = 1/(2\pi r_ef_c) = 1/(2\pi\times45.3\times1k) = \mathbf{3.5\ \mu F}$

Load capacitor C_L and output resistor R_C form a LP filter with cut-off frequency $f_c = 1/(2\pi R_CC_L) = 1/(2\pi\times10k\times150p) = \mathbf{106\ kHz}$



[10]

3. a) If both MOSFETs are active, then drain currents will be given by:

$$I_{D1} = K_1(V_{G1} - V_{t1})^2 \quad ; \quad I_{D2} = K_2(V_{DD} - V_{OUT} - V_{t2})^2$$

Neglecting current in bias network, drain currents must be equal:

$$K_1(V_{G1} - V_{t1})^2 = K_2(V_{DD} - V_{OUT} - V_{t2})^2$$

Taking +ve √ of both sides (both devices above threshold):

$$\sqrt{K_1}\cdot(V_{G1} - V_{t1}) = \sqrt{K_2}\cdot(V_{DD} - V_{OUT} - V_{t2})$$

Rearranging: $V_{OUT} = V_{DD} - V_{t2} - \sqrt{(K_1/K_2)}\cdot(V_{G1} - V_{t1})$ as required. [10]

b) At DC, the bias network imposes the condition $V_{OUT} = 3V_{G1}$. Using this relation we can eliminate V_{G1} from the equation given in a), giving:

$$V_{OUT} = [V_{DD} - V_{t2} + \sqrt{(K_1/K_2)}\cdot V_{t1}]/[1 + \sqrt{(K_1/K_2)}/3]$$

With $V_{DD} = 10$ V, $V_{t2} = V_{t1} = 1$ V and $\sqrt{(K_1/K_2)} = 5$, this gives $\mathbf{V_{OUT} = 5.25\ V}$

Drain current obtained by substituting $V_{OUT} = 5.25$ V or $V_{G1} = 5.25/3 = 1.75$ V into relevant drain current equation. Using Q2 equation, $I_D = 20\mu\times(10 - 5.25 - 1)^2 = 281\ \mu A$

Mode checks:

Q1: $V_{DS1} = 3V_{GS1} > (V_{GS1} - V_{t1})$ **ACTIVE**

Q2: $V_{DS2} = V_{GS2} > (V_{GS2} - V_{t2})$ **ACTIVE**

NB could just argue that both must be active since enhancement mode with $V_{DS} \geq V_{GS}$.

At minimum supply voltage, both devices will be at threshold. Under these conditions, supply voltage will be:

$$V_{DDmin} = 3V_{t1} + V_{t2} = \mathbf{4\ V}$$ [12]

c) The voltage gain can be obtained most easily by differentiating the equation given in a):

$$A_v = \partial V_{OUT}/\partial V_{G1} = -\sqrt{(K_1/K_2)} = \mathbf{-5}$$

Output voltage range:

Upper limit is where Q2 reaches threshold i.e. when $V_{OUT} = V_{DD} - V_{t2} = 9$ V

Lower limit is where Q1 reaches pinch-off point i.e. when $V_{OUT} = (V_{G1} - V_{t1})$. Substituting this condition into equation given in a) the lower limit is obtained as:

$$V_{OUT} = (V_{DD} - V_{t2})/\ [1 + \sqrt{(K_1/K_2)}] = 9/6 = 1.5\ V$$

Output voltage range is therefore $\mathbf{1.5\ V \leq V_{OUT} \leq 9\ V}$ [8]