E3.01
AC1

IMPERIAL COLLEGE LONDON

Exam cps –
but 1-sided

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2007

MSc and EEE PART III/IV: MEng, BEng.and ACGI

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Wednesday, 2 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s) :	C. Toumazou
	Second Marker(s) :	D.G. Haigh

1. (a) The circuit shown in Figure 1.1 is a single-stage inverting voltage amplifier using two CMOS FETs. Write a simple SPICE programme which will compute a small signal gain and phase frequency response analysis of the circuit over the frequency range 10 kHz to 10 MHz. The .OPTIONS card and the transistor model process parameters *QP* and *QN* are already built into the SPICE Library.

[6]

(b) Sketch and label typical phase and gain characteristics of the amplifier. What effect does cascoding have on amplifier performance in particular amplifier phase margin.

[6]

(c) What is the function of the passive components C_1, R_1 and R_2 shown on the circuit?

[4]

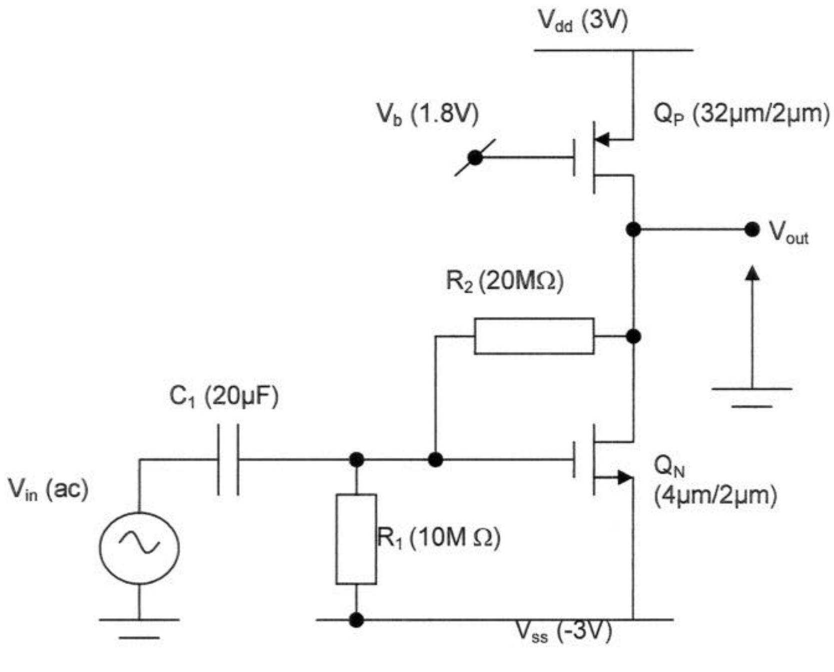

Figure 1.1

d) In practice voltage reference Vb is provided by an on-chip voltage reference circuit similar to the one shown in Figure 1.2. Explain qualitatively why such a four transistor reference circuit can have smaller chip area than an equivalent two transistor circuit with the same power consumption

[4]

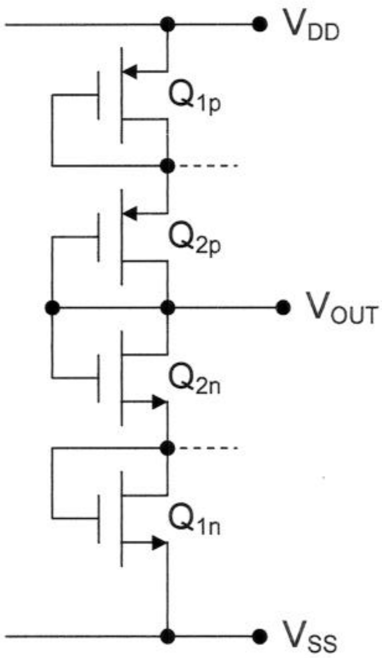

Figure 1.2

2. (a) Voltage and current-sources are key components in analogue circuit design. Sketch a typical band-gap voltage reference circuit and prove that the temperature coefficient of the output voltage V_0 is zero if $V_0 = 1.283\ V$. Assume the temperature coefficient of V_{BE} to be $-2.5mV/°C$, Boltzmann's constant $k = 1.38 \times 10^{-23}\ J/K$ and electron charge $q = 1.6 \times 10^{-19}\ C$.

[11]

(b) Calculate the fractional temperature coefficient for the constant current generator of Figure 2 at room temperature, given that R is a polysilicon resistor with a temperature coefficient of 1500 ppm/°C. What is the function of the four diodes ?

[5]

(c) Explain why transistor Q_2 in figure 2 has two emitters and also why the output current I_0 is directly proportional to absolute temperature.

[4]

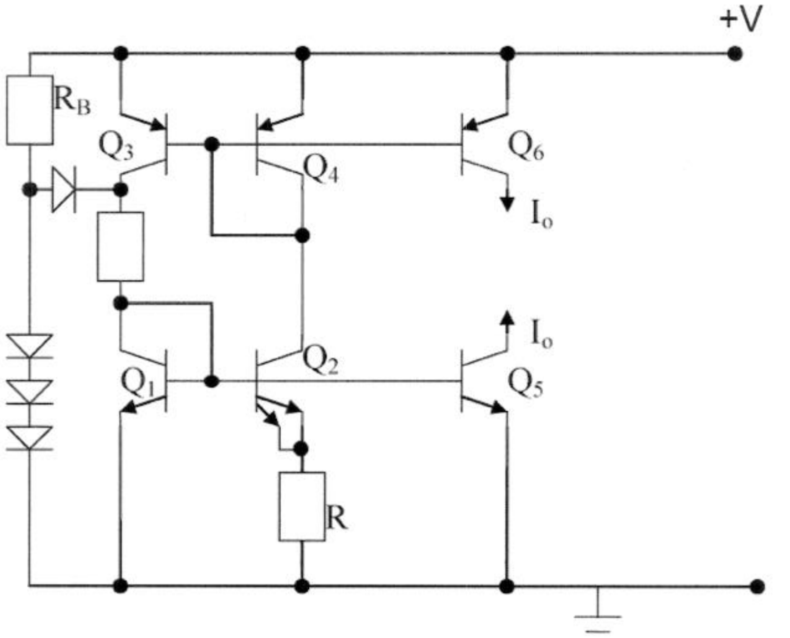

Figure 2

3. (a) Sketch a typical circuit diagram for a single-stage fully differential folded cascode CMOS op-amp. Why is the folded cascode op-amp regarded as a single stage design? Finally briefly explain the concept of common-mode feedback with reference to your folded cascode op-amp.

[8]

(b) Estimate the low-frequency differential voltage gain, slew rate and gain-bandwidth product of the two-stage CMOS op-amp shown in Figure 3.1. Aspect ratios of all devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below.

[10]

(c) Explain qualitatively why the addition of a resistor in series with compensation capacitor Cc improves amplifier stability.

[2]

CMOS TRANSISTOR PARAMETERS

MODEL PARAMETERS	*Kp (μA/V2)*	*λ(V^{-1})*	*V_{TO} (V)*
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

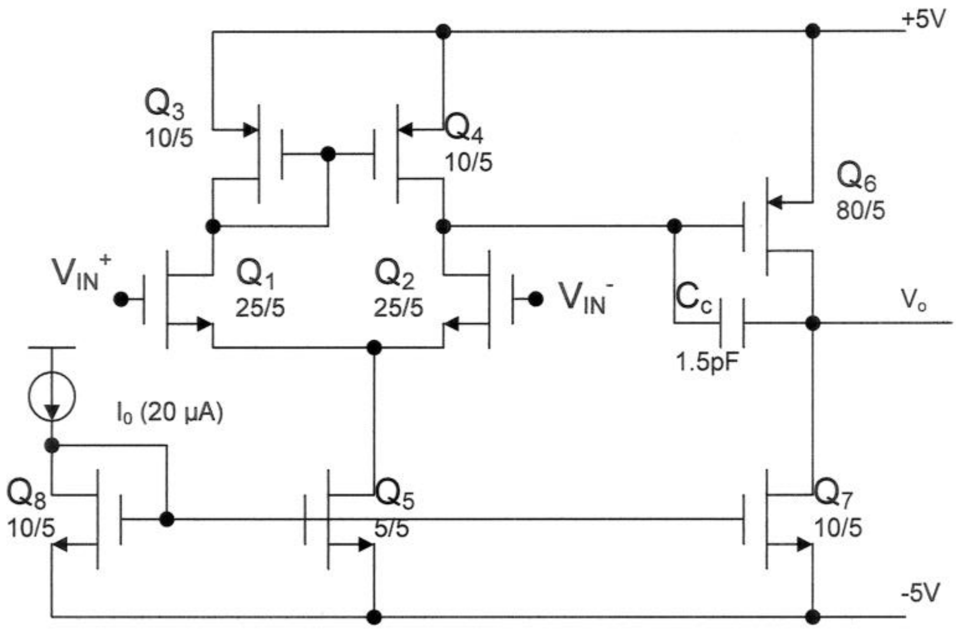

Figure 3.1

4. (a) Under what operating conditions does the MOSFET of Figure 4.1 realise a linear floating resistor between terminals *A* and *B*? Show that under these conditions the equivalent resistance R_{AB} can be approximated by

$$R_{AB} = \frac{L}{KW(V_{GS} - V_T)}$$

stating any assumptions. All symbols have their usual meaning.

[6]

(b) Discuss three sources of non-linearity in the single MOSFET resistor realisation of Figure 4.1 and suggest one suitable circuit design to help eliminate one or more of these non-linear terms. Show all necessary circuit analysis to confirm your design.

[6]

(c) Figure 4.2 shows a fully differential continuous time integrator using a balanced double differential linear active transresistor. Derive an expression for the time constant of the integrator. You may ignore all bulk effects, and assume all MOSFETs are operating in the triode region.

[8]

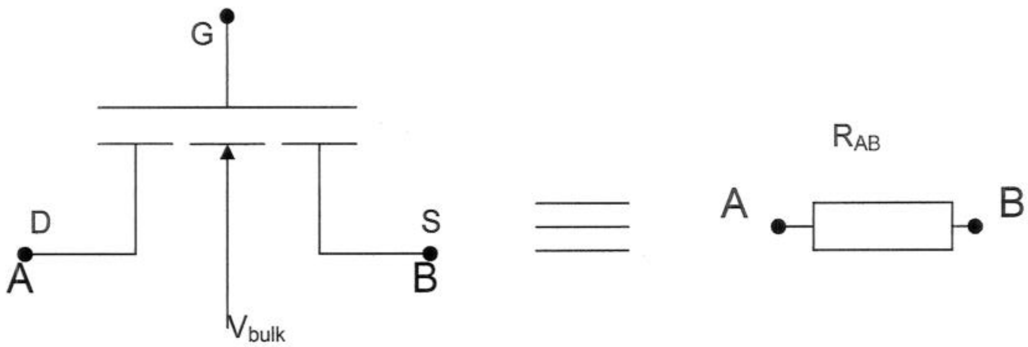

Figure 4.1

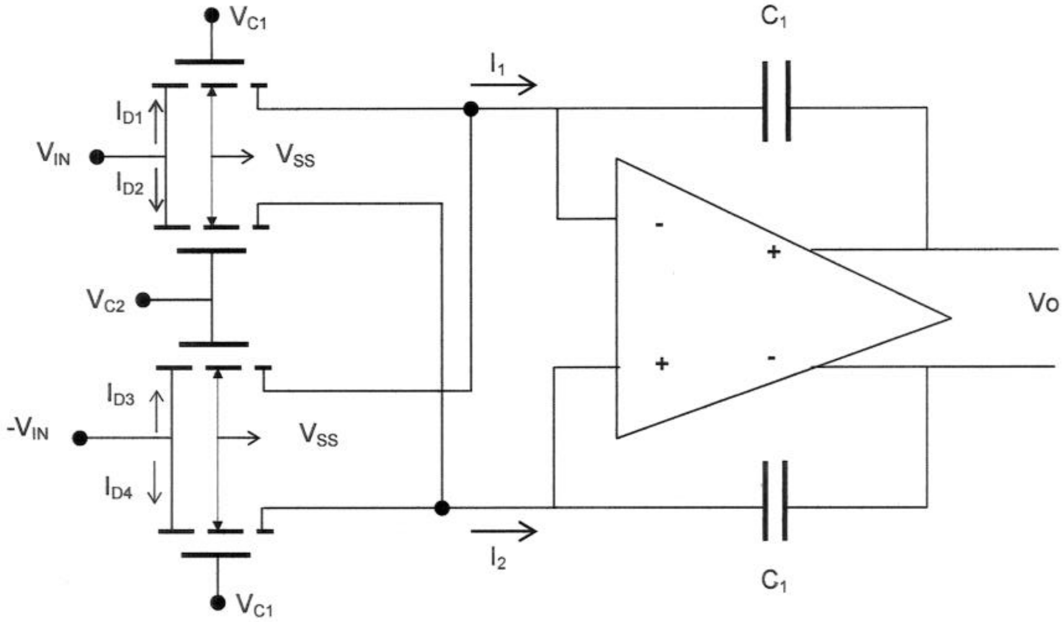

Figure 4.2

5. (a) Sketch circuits for both a Lossy and differential switched-capacitor integrator and derive an expression for the transfer function of each implementing switches by MOSFETs of equal size and assuming that the integrators are driven by non-overlapping clocks with a clock frequency much higher than the maximum input signal frequency. Also assume the switches are ideal.

[10]

(b) Figure 5.1 shows one section of a switched capacitor ladder filter. Based on this filter structure, design a 3rd-order Chebyshev low-pass filter with a cut-off frequency of 5 kHz and a 1.0 dB pass band ripple. Assume a clock frequency of 100 kHz. Passive component values for the LC prototype, normalised to 1 rad/s, are $C_1 = C_3 = 2.0236$, $L_2 = 0.994$. In your analysis assume all integrators to be lossless.

[10]

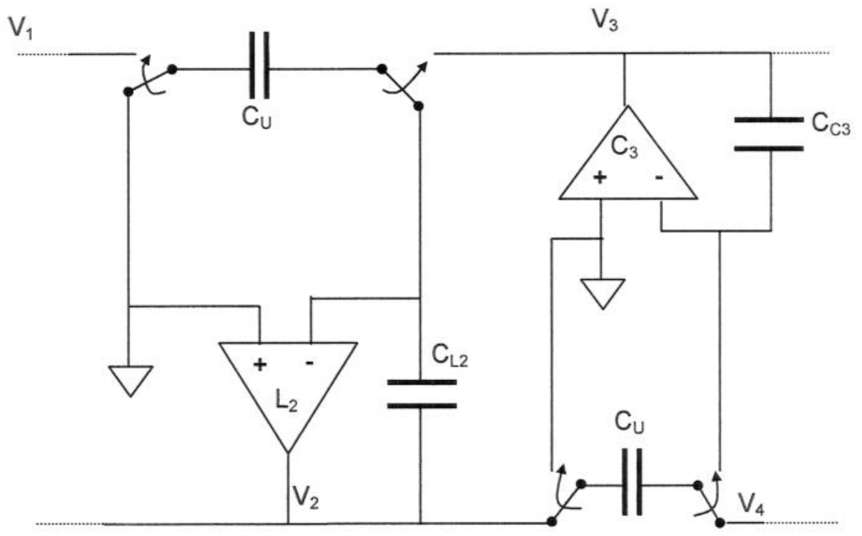

Figure 5.1

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6. (a) Give one advantage and one disadvantage of each of the three CMOS current mirror circuits shown in Figures 6.1, 6.2 and 6.3.
[6]

(b) For the current mirror of Figure 6.2 derive the voltage swing in terms of device threshold voltage V_T, clearly stating any assumptions you make.
[7]

(c) With the aid of a macromodel, explain the theoretical concept of current feedback and how it results in constant bandwidth application.
[7]

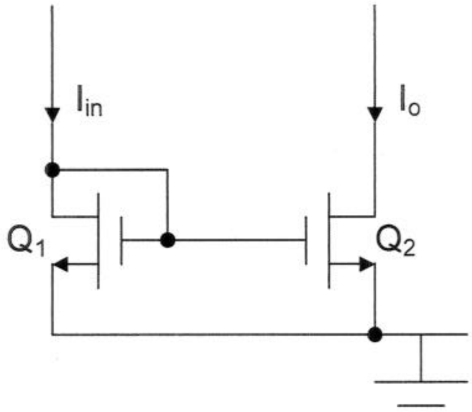


Figure 6.1

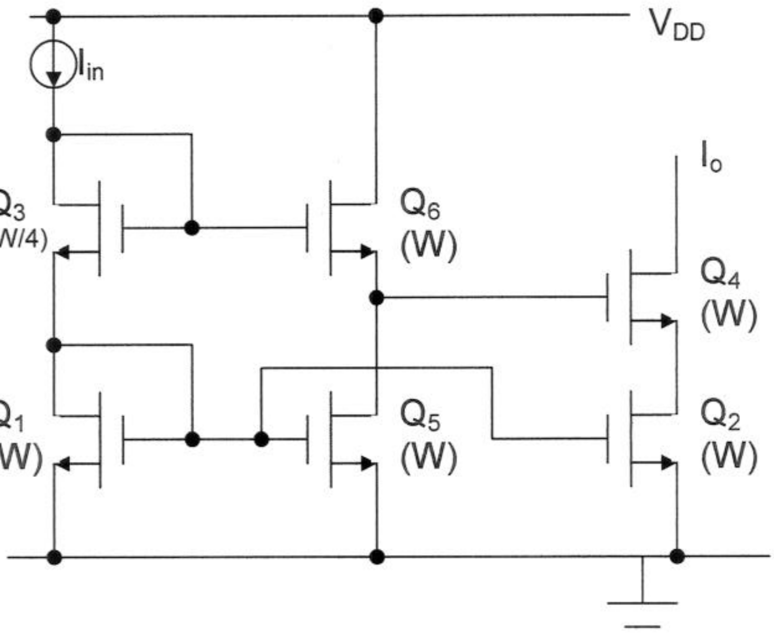


Figure 6.2

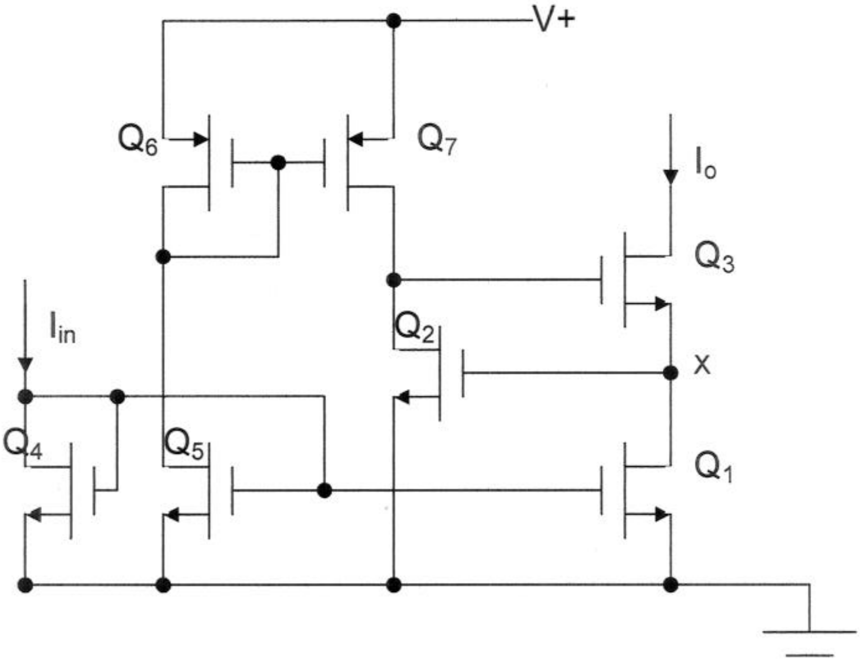


Figure 6.3

E3.01/ACI

2007 Exam. original.

3rd Year/MSc

Analogue Integrated Circuits and Systems

E3.01/ACI

SOLUTIONS

1st Marker C. TOUMAZOU

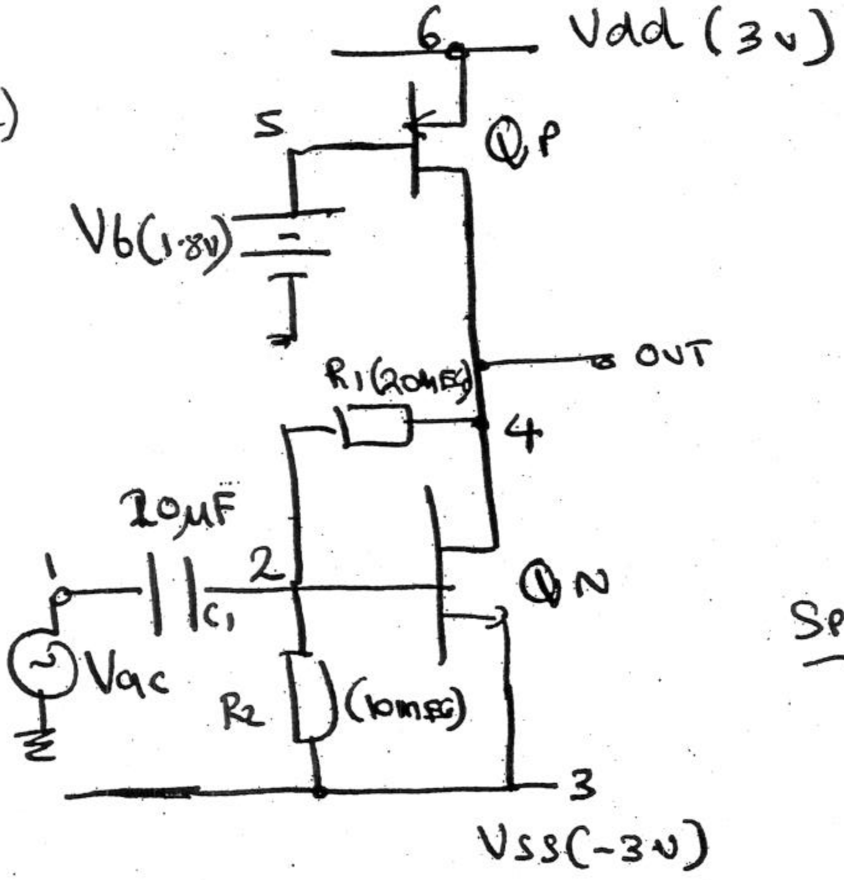
2nd Marker D. Haigh

CT

Q1

$\frac{1}{21}$

a)



SPICE NETLIST

.Title inverting cmos Amplifier.

Component Netlist

```
C1   1  2   20 E-6
R1   2  4   20 MEG
R2   2  3   10 MEG
M1   4  2  3  QN  W=4u  L=2u
M2   4  5  6  QP  W=32u  L=2u
Vdd  6  0   3V
Vss  3  0   -3V
Vb   5  0   1.8V
Vac  1  0   ac 1
```

sources

```
.Model QN, Qp
.op all
.option post
.ac dec 10 10K 10MEG
.PRINT ac VdB(4)
.PRINT ac Vp (4)
.END.
```

Analysis Print

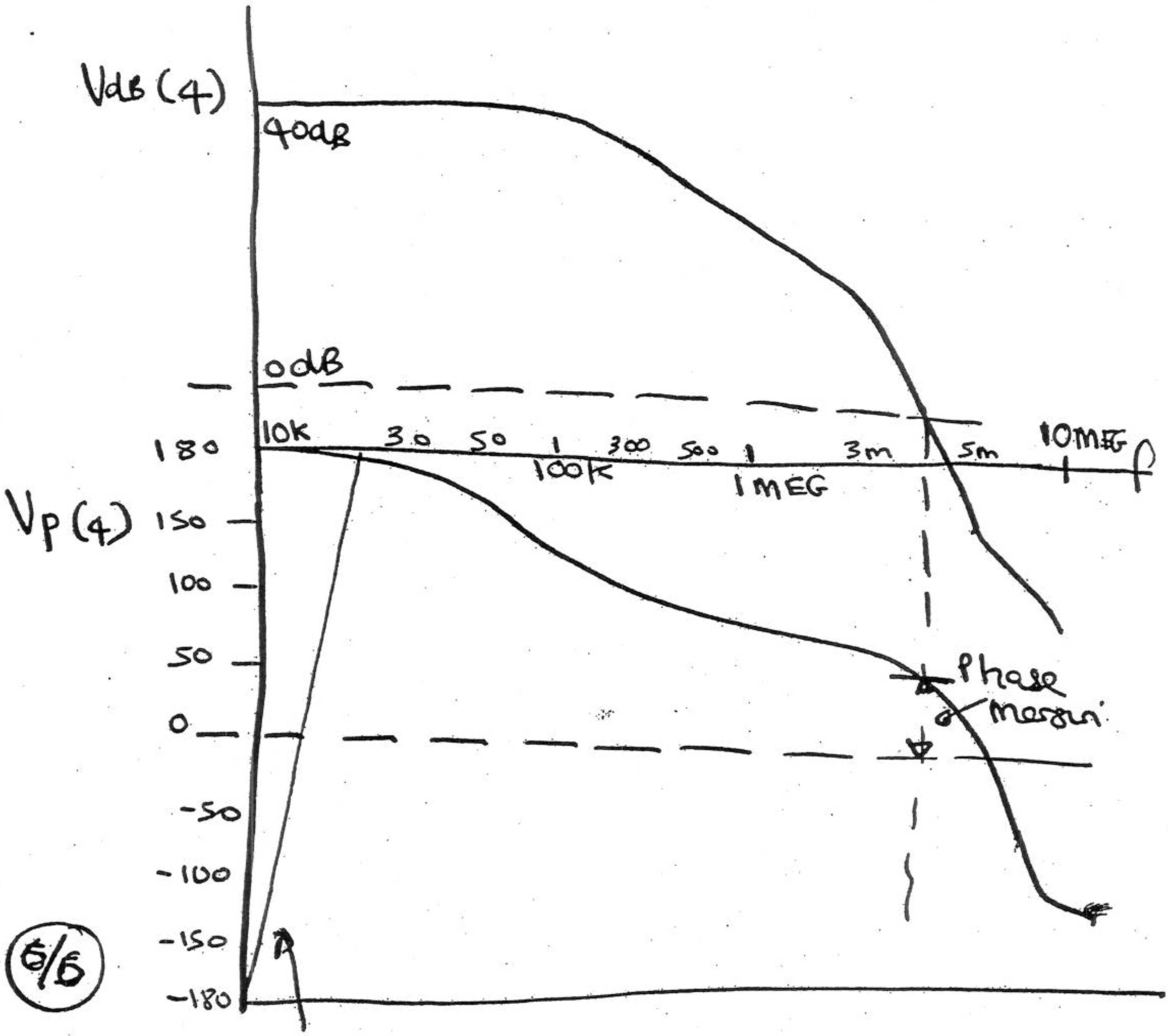
6/6

CT

Q1 (cont)

Typical SPICE output Plot.

(2)



Autoscaling in SPICE

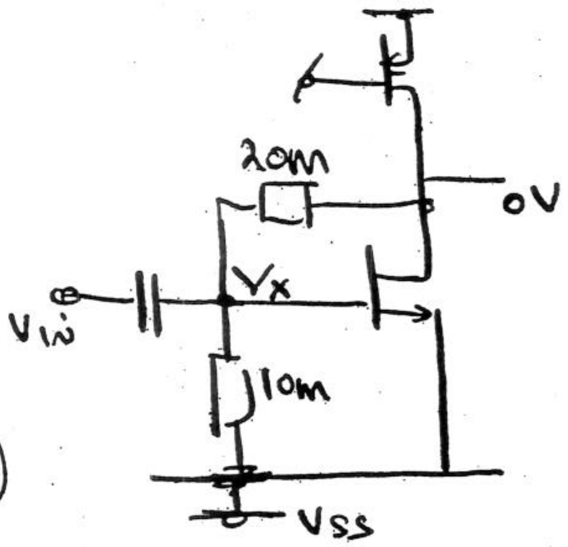
6/6

Likely that theory and Simulated will differ because of approximations generally assumed in theory. Models for transistors in SPICE have inaccuracy. Also inaccuracy in parameter extraction for SPICE models.

Cascoding will increase amplifier gain but will compromise phase margin due to added capacitance at output.

CT

Large passive components used for DC biassing. Sets high impedance output of amplifier at dc bias close to 0V. Large values of R used so that input and output impedance levels are not loaded. 20μF capacitor used to ac couple input. Typically



$$V_x = V_{ss} + \left(\frac{-V_{ss}}{3}\right)2$$

$$= \left[\frac{V_{ss}}{3}\right]$$

4/4

CT

Figure Q1 d)

Since $I \simeq \frac{kW}{2L}(V_{gs}-V_T)^2$

then if V_{gs} is small $\simeq V_T$

then (W/L) large.

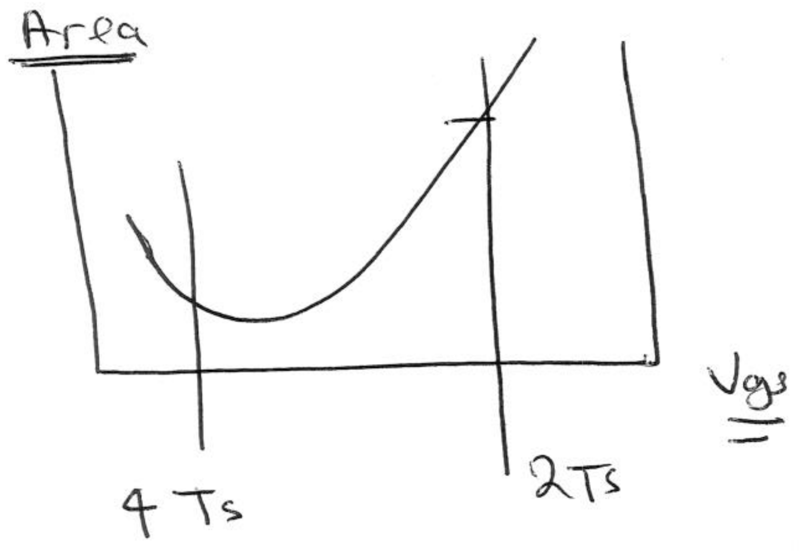
If $V_{gs} \gg V_T$, then (W/L) small

small (W/L) gives large chip area

$\therefore$ Two transistor PD has

larger V_{gs}/transistor than

four transistors PD for same supply

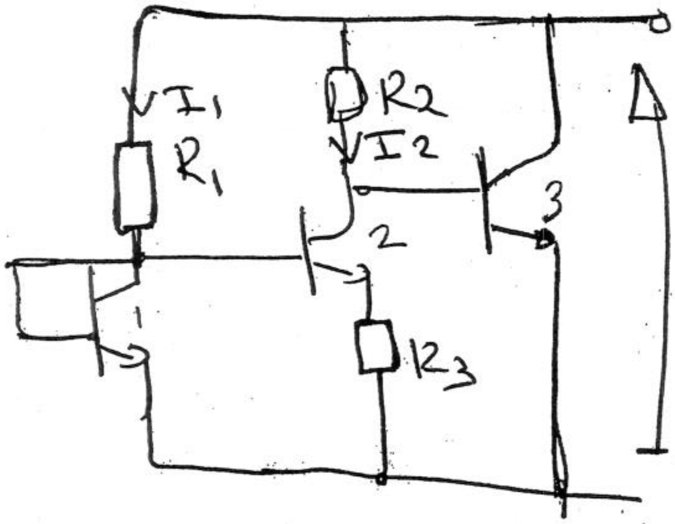


4/4

Ans 2

(5)

Q2



Bandgap.

(5/5)

$V_{BE1} = V_{BE2} + I_2 R_3$

$\beta >> 1$

Since $V_{BE1} - V_{BE2} = V_T \ln(I_1/I_2)$

then $V_0 = V_{BE3} + R_2/R_3 \, V_T \ln(I_1/I_2)$

$V_T \ln(I_3/I_s) \rightarrow$ assume Non-temp

For $dV_0/dt = 0$, then dV_{BE3}/dT

$= \frac{V_T}{T} \frac{R_2}{R_3} \ln\left(\frac{I_1}{I_2}\right)$

Since $\frac{dV_{BE}}{dt} = -2.5\,mV/°C$, $\frac{V_T}{T} = \frac{1.38\times10^{-23}}{1.6\times10^{-19}}$

then $\left(\frac{R_2}{R_3}\right) \ln\left(\frac{I_1}{I_2}\right) = 29$ and so

(6/6) $V_0 = 1.283V$

b) For PTAT temperature coefficient of V_T cancels with negative temp coefficient of Resistor

C+

Qu 2 cont

$$TcF = \frac{1}{V_T} \partial V_T / \partial T - 1/R \, \partial R / \partial T$$

$$= \frac{1}{T} - 1500 \times 10^{-6} \text{ @ Room T}$$

$$= 1833 \text{ ppm}/^\circ C$$

3/3

The diodes are part of a start-up circuit which will conduct when the PTAT is in its 'zero' operating state

TOTAL 20/20

An injection of current is provided by R_B which starts-up the circuit switching off the diode connected to the collector of Q3.

2/2

4/4

c). since $I_o = \frac{(V_{be1} - V_{be2})}{R}$

Prop to temperature

$$\simeq \frac{V_T}{R} \ln\left[\frac{I_1}{I_o} \frac{I_{s2}}{I_{s1}}\right] \simeq \frac{V_T \ln 2}{R}$$

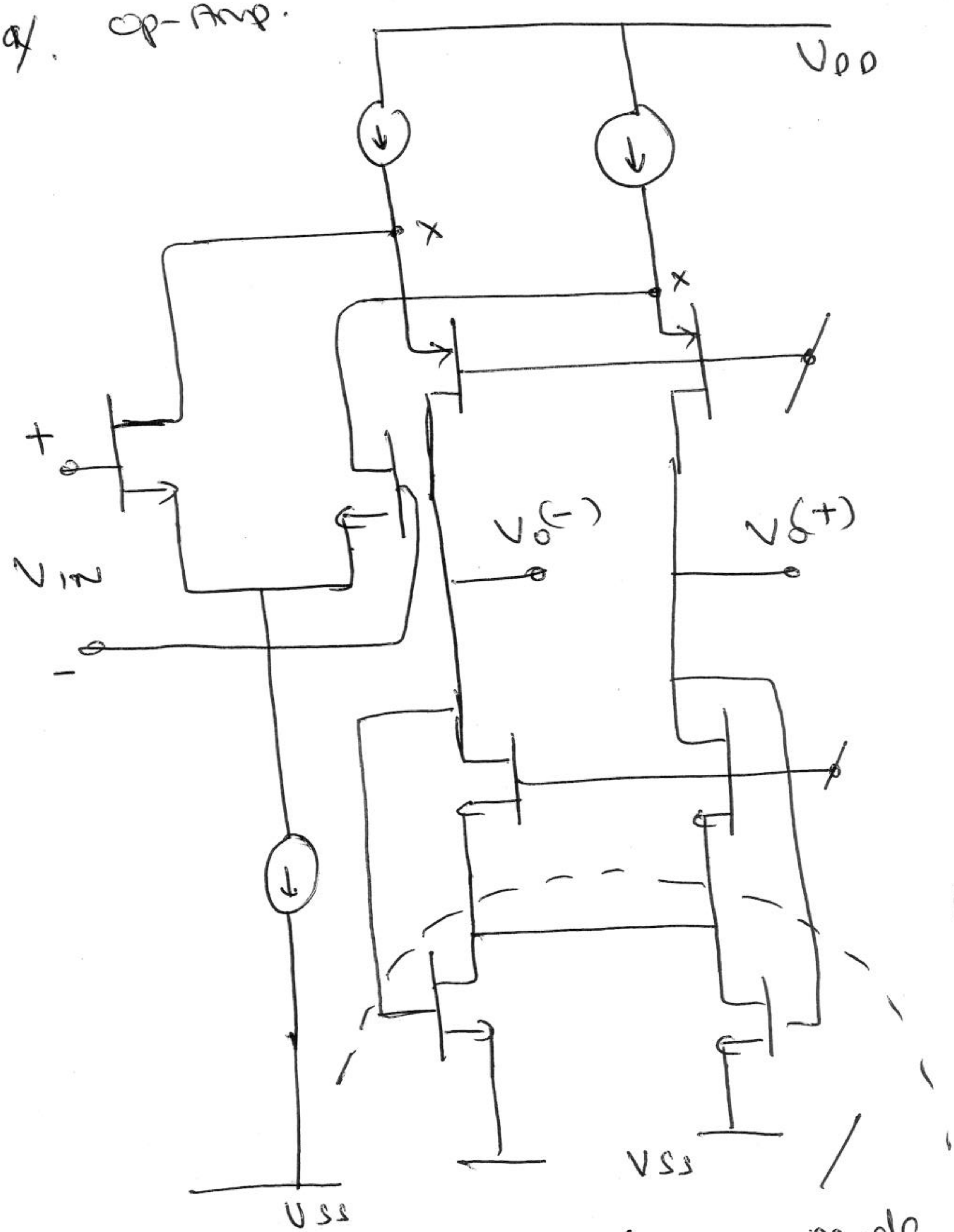
If $I_{s2} = I_{s1}$ and $I_o = I_1$ then $I_o \simeq 0$

important for $I_{s2}/I_{s1} = n = 2$ in this case.

CT

Qu 3

a/. Architecture of folded-cascode op-Amp.



4

$$A \approx \left(1/2\right)\left(g_m/g_o\right)^2$$

CT

Qu 3 cont

Single-stage because one current path from input to output.

Node X is low impedance and so very small voltage swing is generated. Only high impedance node is at the output. 2

Not necessary to pole split since dominant pole at output not two stages.

Diff output op-amps with high gain have no way of stabilisation since outputs are undefined (voltage that is).

Common-mode feedback - senses common-mode output and via negative feedback controls the current through the output stage to ensure stable quiescent operating point. Circuit shown in the figure. 2

b/. <u>OP-Amp</u>

(2/2) $\boxed{A_{v1} = -g_{m2}/(g_{o2}+g_{o4})}$

$(g_{o2}+g_{o4}) = I_{D2}(\lambda_N+\lambda_P)$

$= 5\times10^{-6}\times0.05 = 2.5\times10^{-7}\,\Omega^{-1}$

$g_{m2} = 2\sqrt{\beta_2 I_D} \Rightarrow \beta_2 = \frac{k_N}{2}\left(\frac{W}{L}\right)_2$

$\beta_2 = 7.5\times10^{-5}\,A/V$

$\therefore\ g_{m2} = 3.87\times10^{-5}\,S$

(2/2) $A_1 = -154.9$

$A_2 = \boxed{-g_{m6}/(g_{o7}+g_{o6})}$

$(g_{o6}+g_{o7}) = I_{D6}(\lambda_{NP}+\lambda_N)$

$= 20\times10^{-6}\times0.05$

$= 10\times10^{-7}\,\Omega^{-1}$

(2/1)

$g_{m6} = 1.13\times10^{-4}$, $A_2 = -113$.

$A_T = A_1A_2 = 17503$

CT

Qu 3 cont (10)

$$G.B_p = \frac{g_{m2}}{2\pi C_c} = 4.1\,MHz \quad -(2)$$

$$S.R = I_o/C_c = \left(\frac{10}{1.5}\right) V/\mu s \quad -(2)$$

— TOTAL 10/10

c. Introduce R in series with C_c ✗

provides feedforward compensation and eliminates RHP zero in the op-amps transfer function.

Zero is given by $Z = -\,g_{m6}/C_c$

with R

$$Z = -\frac{1}{\left(1/g_{m6} - R\right) C_c}$$. Improves ϕ

by setting $Z = P_2$ = 2nd pole. with R.

(2/2)

(T

Q4 Assumption is that if ($V_{DS} \simeq 0$) or
a ($V_{DS} << (V_{GS} - V_T)$) device acts in linear region. From

$$I_D = \frac{KW}{L}\left[(V_{GS}-V_T)V_{DS} - V_{DS}^2/2\right](1+\lambda V_{DS})$$

for $V_{DS} << (V_{GS}-V_T)$, then $\lambda V_{DS} << 1$

So $I_D = \frac{KW}{L}(V_{GS}-V_T)V_{DS}$

6/6 OR $R_{AB} = V_{DS}/I_D = L/(KW(V_{GS}-V_T))$

b) Three sources of Non-linearity

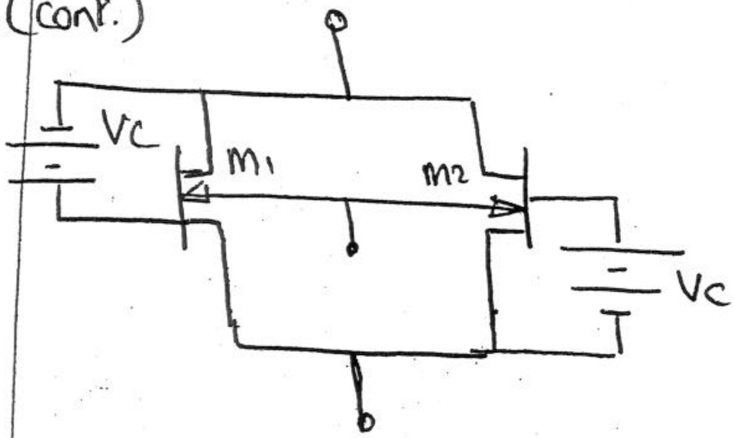
(i) limited due to V_{BS} changing V_T for negative V_{DS} due to body effect.
ie. $V_T = V_{T0} + \gamma\left[\sqrt{-V_{BS}+2\phi_F} - \sqrt{2\phi_F}\right]$
γ = bulk threshold parameter
ϕ_F = Fermi-level potential

(ii) limited due to V_{DS} approaching ($V_{GS} - V_T$) hence saturation region for large positive V_{DS}.

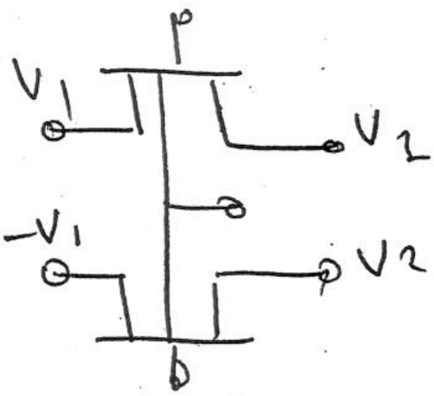
(iii) For large values of V_{DS} the $V_{DS}^2/2$ term comes in making the resistor quite non-linear.

4/4

Q4 (cont.)

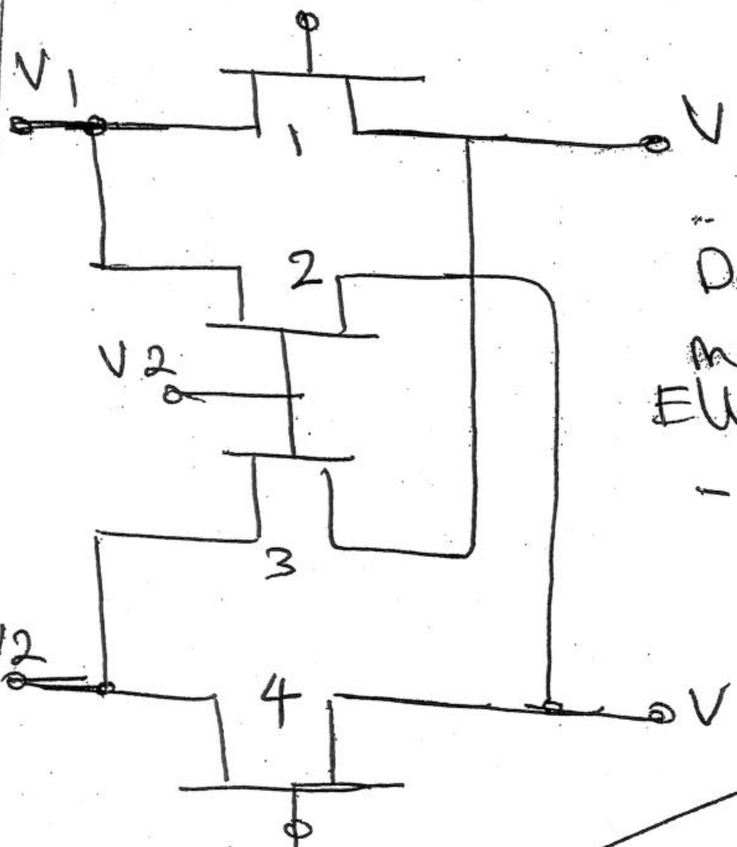


Parallel circuit - eliminates $V_{ds}^2/2$ term.



Differential scheme

Effects of V_{DS} cancelled.



Double differential mos.
Eliminates
- V_{DS} and V_T term.

ANY one of these will do!

2/2

CT

Q4 (cont)

Double differential integrator

$$I_{D1} = 2\beta\left[(V_{C1} - V - V_T)(V_1 - V) - \tfrac{1}{2}(V_1 - V)^2\right]$$

$$I_{D2} = 2\beta\left[(V_{C2} - V - V_T)(V_1 - V) - \tfrac{1}{2}(V_1 - V)^2\right]$$

$$I_{D3} = 2\beta\left[(V_{C2} - V - V_T)(V_2 - V) - \tfrac{1}{2}(V_2 - V)^2\right]$$

$$I_{D4} = 2\beta\left[(V_{C1} - V - V_T)(V_2 - V) - \tfrac{1}{2}(V_2 - V)^2\right]$$

Expanding it can be shown that :-

$$(V_1 - V_2)/(I_1 - I_2) = 1/2\beta(V_{C1} - V_{C2}) = R$$

Independent of both V_T and V_{DS} terms

Hence $\tau = 2CR = \left[\dfrac{C}{\beta(V_{C1} - V_{C2})}\right]$

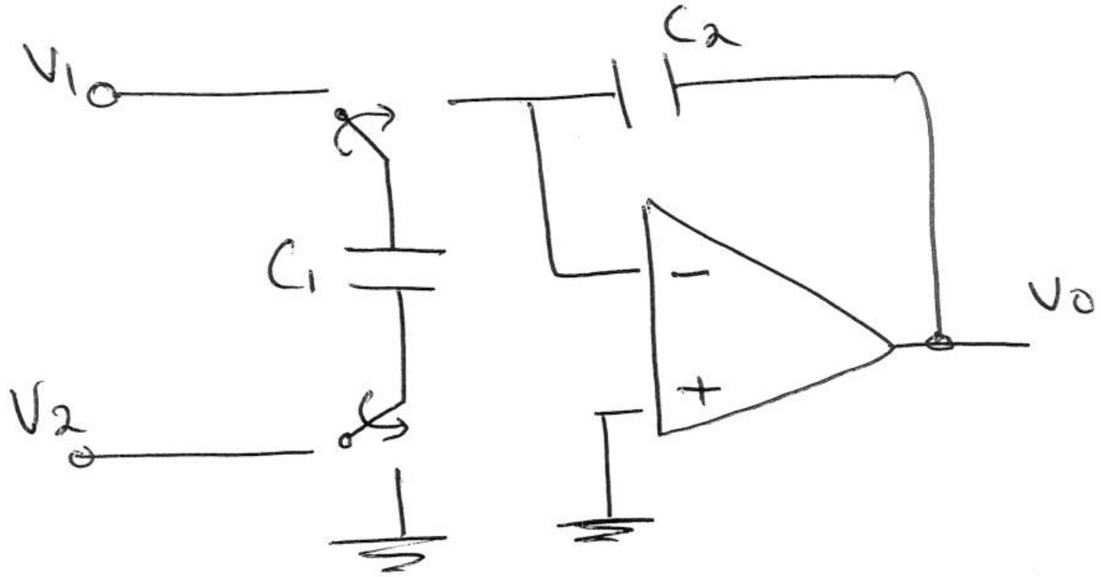
8/8

———————//———————

CT

Qu5/.

a) Differential integrator



During ϕ_1 $Q = C_1[V_1 - V_2]$

$I_{av} = f_c C_1 [V_1 - V_2]$

f_c = clock frequency

During $\phi_2 \Rightarrow$ $I_{av} = -f_c(V_1 - V_2)C_1$

$\therefore V_o = \frac{-1}{j\omega C_2} f_c C_1 [V_1 - V_2]$

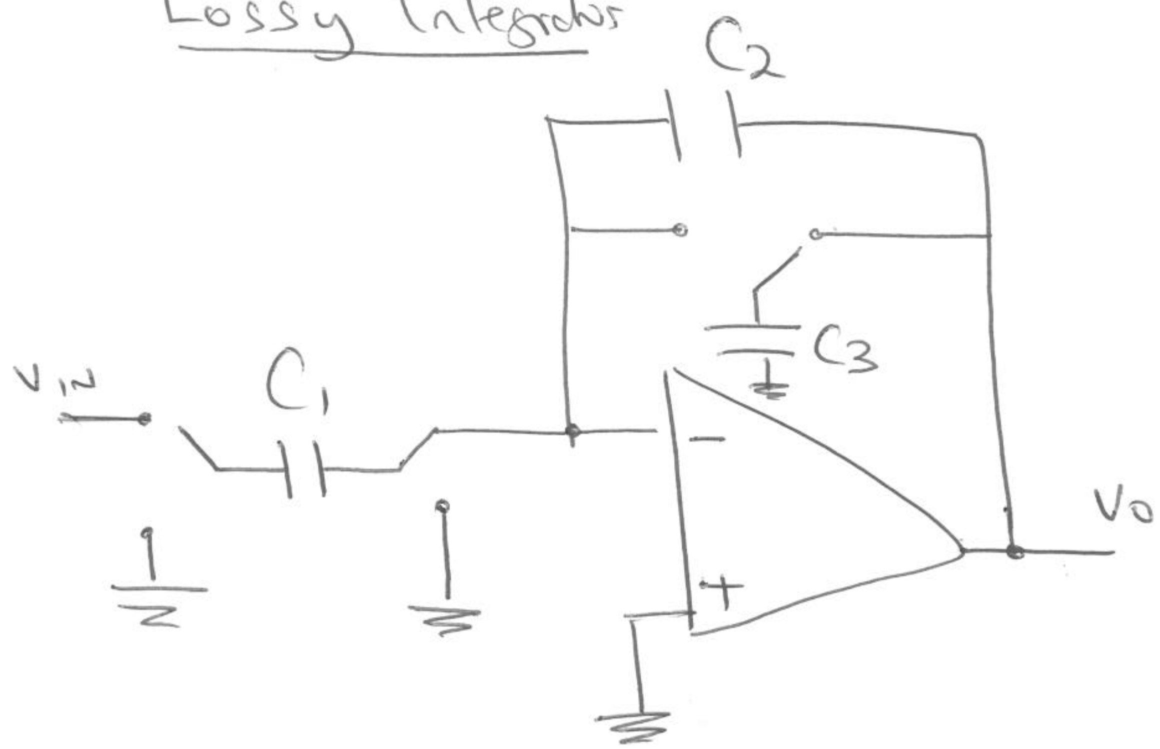
$\therefore \frac{V_o}{(V_1 - V_2)} = -\frac{f_c}{j\omega}\frac{C_1}{C_2} \approx \tau = \frac{C_2}{C_1 f_c}$

5/5

CT

Q45 cont

Lossy Integrator



During ϕ_1 $\quad Q = C_1 V_{IN} \Rightarrow I_{av} = f_c C_1 V_{IN}$

During ϕ_2

$$I_{av} = -\left[f_c C_3 V_O + j\omega C_2 V_O\right]$$

$$\therefore f_c C_1 V_{IN} = -\left[f_c C_3 V_O + j\omega C_2 V_O\right]$$

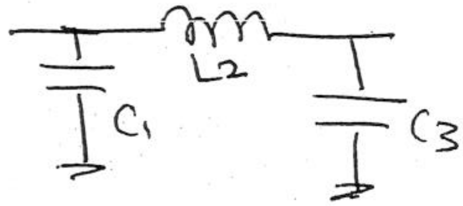
$$V_{IN} = -\left[\frac{C_3}{C_1} V_O + \frac{j\omega C_2 V_O}{C_1 f_c}\right]$$

$$\therefore \frac{V_O}{V_{IN}} = -\frac{C_1}{C_3}\left(\frac{1}{1 + \frac{C_2}{C_3} j\omega / f_c}\right)$$

5/5

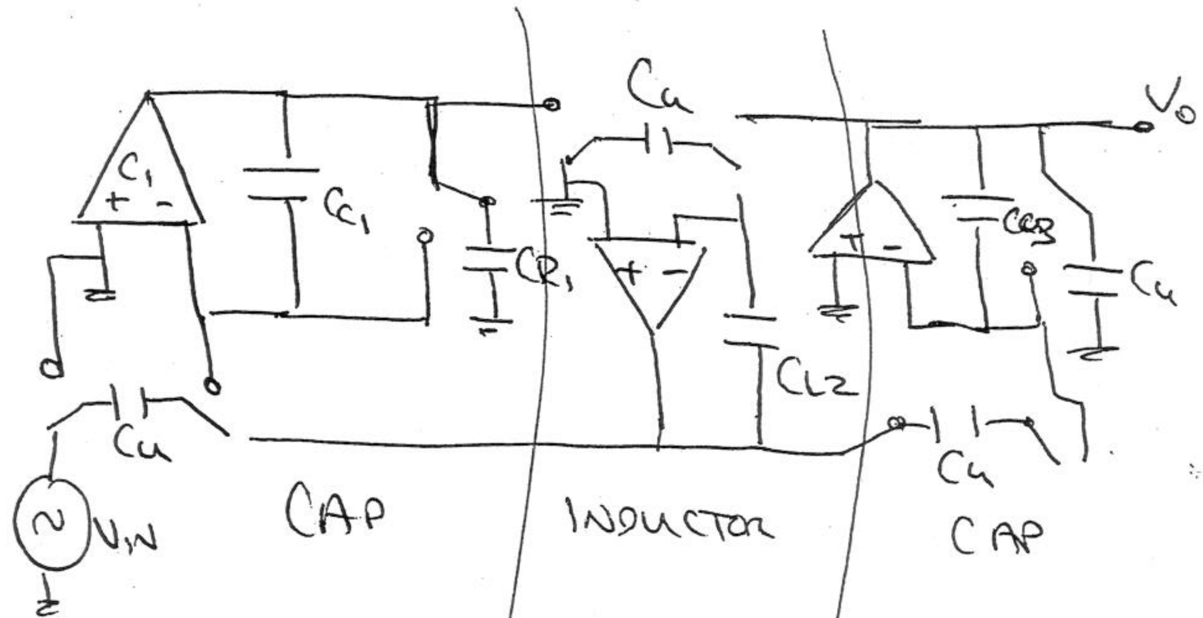
$$\approx T = \left(C_2/C_3\right)\frac{1}{f_c}$$

section of LCR prototype.



General transformation Rules (Not really required but the bright students may include)

3/4



Conversion into differential integrators.

Inductor transformations

$(L_2/R_S)f_c = C_{L2}/C_U$

Capacitor Transformations.

$C_3/C_U = f_c R_S C_3$

where RS is normalising dummy scaling resistor; Assuming $R_S = 1$

$$\left.\begin{aligned} C_{C1}/C_U &= f_c C_1 \\ C_{C3}/C_U &= f_c C_3 \\ C_{L2}/C_U &= f_c L_2 \end{aligned}\right\} \text{general transformation}$$

Qu 5 cont

Table values of C_1, L_2 and C_3 are normalised to 1 rad/s $\div 2\pi f_p$

$f_p = 5\,kHz$

$$C_1 = C_3 = 2.0236/(2\pi\, 5\times10^3)$$
$$= 6.44\times10^{-5}\,F$$

$$C_{L2} = 0.994/(2\pi\, 5\times10^3)$$
$$= 3.164\times10^{-5}\,F$$

For termination R_s

assume $C_{u} = C_{R_1} = C_{R_0} = 1\,pF$

Then $\begin{bmatrix} C_{R_1} = C_{R_3} = 6.44\,pF \\ C_{L2} = 3.164\,pF \end{bmatrix}$

6/6

Total 20/20

CT

(18)

Qu 6/.

a)

Fig 6.1 - Simple mirror

Advantages - High frequency
- High output swing

(2) Disadvantage - very inaccurate

Fig 6.2 - High swing cascode

Advantage - Higher output swing than cascode

Disadvantage - complex, poor frequency performance.

(2)

Figure 6.3 - Regulated cascode

Advantage - Highest output swing
Highest output resistance

Disadvantage - inaccuracy of simple current-mirror
(2)
- feedback leading to potential instability.

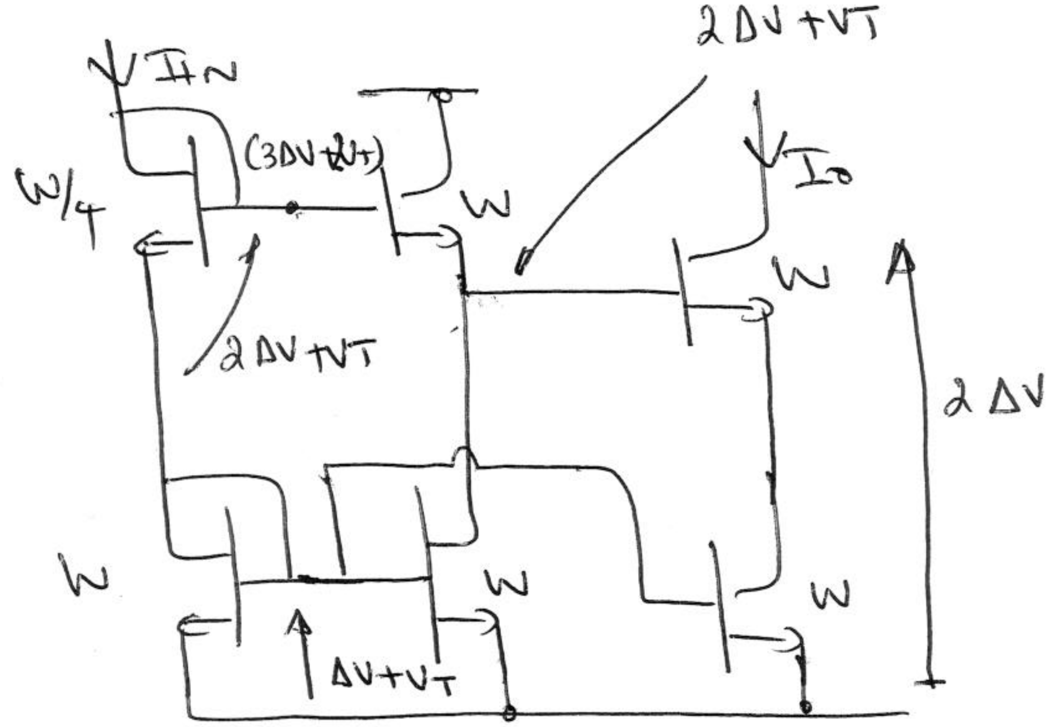
(6/6)

CT

Qu 6 cont

output swing

Circuit includes all saturation Voltages



Assuming equal L's

$I_O = I_{IN}$

$\beta_1 = \beta_2 = \beta_4 \quad \beta_5 = \beta_6 = \beta$

$\beta_3 = \beta/4$

7/7

$\therefore V_{sat(3)} = 2(V_{GS} - V_T)$

NOTE $\Delta V = (V_{GS} - V_T)$

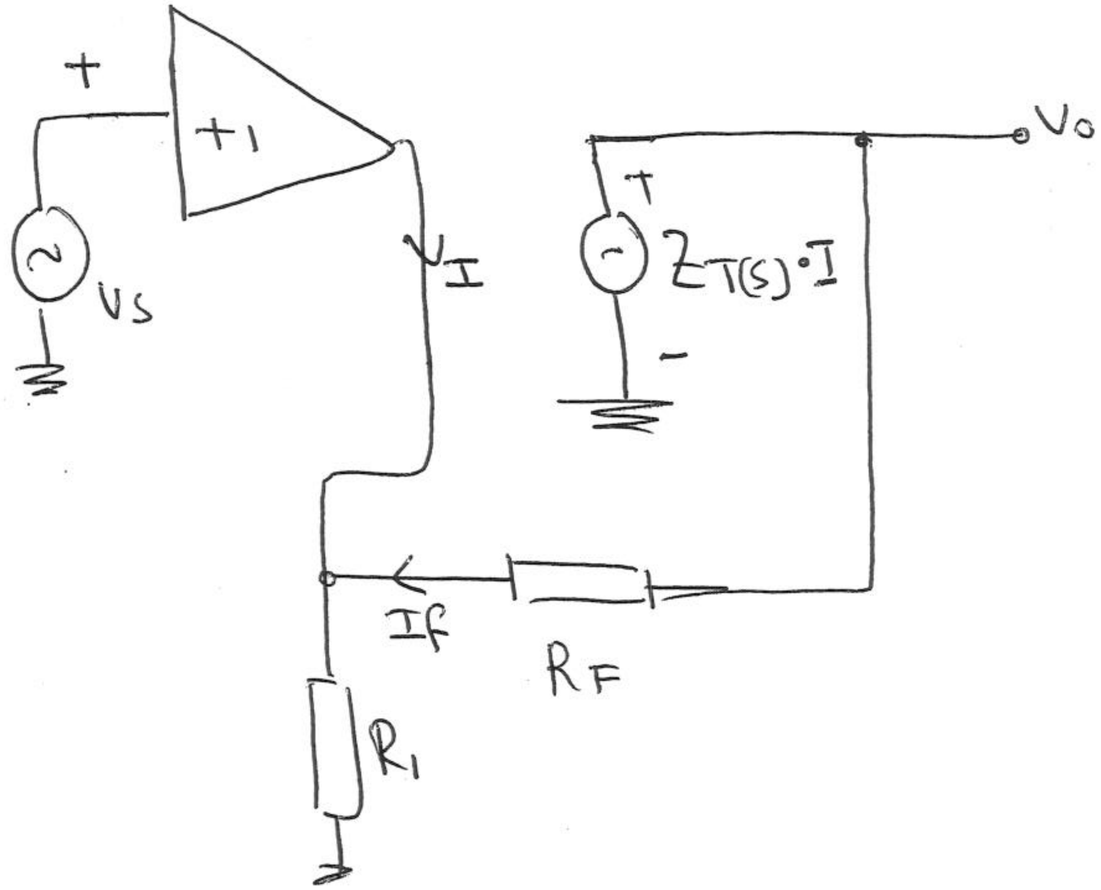
Swing $\underline{\underline{2\Delta V}}$.

LT

Qu 6 cont

macromodel of Current-feedback op-amp.

c).



$Z_{T(s)} = Z_{T0} / (1 + jf / f_p) \Rightarrow f_p$ dominant Pole

From model

$I_f = (V_o - V_s)/R_F$

$I_1 = V_s/R_1$

$V_o = Z_{T(s)} I = Z_{(T)}(I_1 - I_f)$

From above

$$(V_o/V_s) = (1 + R_F/R_1) \left[\frac{Z_{T(s)}}{R_F + Z_{T(s)}} \right]$$

Qu 6 cont (21)

substitute $Z(T)$s, and assume $Z_{TO} \gg R_F$

$$\left(V_O/V_S\right)_{j\omega} = \left(1 + \frac{R_F}{R_1}\right)\left[\frac{Z_{TO}}{Z_{TO}+R_F}\right]\left(\frac{1}{\left(1+jf/f_p\left(\frac{Z_{TO}+R_F}{R_F}\right)\right)}\right)$$

Assuming $Z_{TO} \gg R_F$

$$\left(\frac{V_O}{V_S}\right)_{j\omega} = \left(1+\frac{R_F}{R_1}\right)\frac{1}{\left(1+jf/\frac{GB}{R_F}\right)}$$

where $G.B = f_p Z_{TO}$

f_p closed $= \underline{\underline{G.B/R_F}} \Rightarrow$ determined by R_F

Gain determined by R_1

$$A_C = \underline{\underline{\left(1+\frac{R_F}{R_1}\right)}}$$

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