UNIVERSITY OF LONDON

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 1999

BEng Honours Degree in Computing Part III
MEng Honours Degrees in Computing Part IV
MSc Degree in Advanced Computing
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the
Diploma of Membership of Imperial College
Associateship of the City and Guilds of London Institute

PAPER 3.34

MICROCONTROLLERS AND COMPUTER INTERFACING

Monday, April 26th 1999, 10.00 – 12.00

Answer THREE questions

For admin. only:
paper contains 4 questions

1a Derive the formula for the closed loop gain of an idealised negative feedback Operational Amplifier. You should clearly show your working and include an appropriate diagram.

b State the two basic assumptions made during the analysis and use of an idealised Operational Amplifier.

c The negative feedback Operational Amplifier presents a load to the source of the signal. The positive feedback variation does not. Draw the circuit diagram for a positive feedback operational amplifier and derive the closed loop gain of your circuit.

The three parts carry, respectively, 40%, 20%, 40% of the marks.

2 a If a sine wave of frequency f and amplitude V is sampled with an aperture time τ what is the maximum possible error in one sample value?

b Shannon showed that when a signal, $f(t) = A\sin(2\pi f_s t)$, is to be sampled, the minimum sampling frequency must be twice the signal frequency. What frequencies will be derived if this minimum criteria is not met for a typical sinusoidal waveform? What is the maximum frequency that can be converted by an Analog to Digital Converter with a conversion time of 25μs?

c In the context of an Analog to Digital convertor, what is meant by *full scale*, *resolution* and *accuracy*? If an 8 bit A/D has a *full scale* range of 5V, what is its resolution and with what accuracy can it convert a signal of 50mV?

d With the aid of a diagram, describe the operation of a 4-bit binary-weighted Digital to Analog converter. Why is it impractical to build such converters with more than 8 bits?

The four parts carry, respectively, 20%, 20%, 30%, 30% of the marks.

3 a Two important groups of motors are *stepper* and *DC* motors. By giving a brief description of each show why *DC* motors are not appropriate for precise positioning of actuators and why stepper motors are not appropriate for battery powered systems.

b *DC* motors are ideally driven by analog DC signals that vary over the full range of the motor's rating. However, Pulse Width Modulation (PWM) can be an equally effective way of controlling such motors. Outline the principles of PWM and explain the importance of the frequency and duty cycle of a PWM signal.

c Speed and straight line control is a significant problem in robots that have two DC motors as their locomotion systems. When presented with an extra load (a hill for example) they will slow down unless the PWM signal is altered; this means that the desired speed of the motor is not achieved. Worst still, despite being presented with identical PWM signals under identical external conditions, the motors will run at slightly different speeds.

i How does a simple proportional controller attempt to compensate for the first of these problems: the desired vs actual speed of an individual motor?

ii How does the inclusion of an integral feedback path help ensure that straight line motion is obtained?

The three parts carry, respectively, 30%, 20%, 50% of the marks.

4 There are a variety of reasons why we might want to interrupt the normal processing of instructions by a processor. I/O devices (interfaces) and unexpected errors in hardware and software are examples of events that may need to be handled by exceptional sequences of instructions.

a Outline the use of vectored interrupts to establish which of a number of potential devices has caused the interrupt. What advantage do polled interrupts have over vectored interrupts within this context?

b In a safety-critical application the speed with which interrupts are responded to may be critical.

i What factors will affect interrupt latency?

ii In what ways is a power-on reset interrupt different to any other type of reset or interrupt?

c A common goal of a real-time control system is robustness in the face of software errors. It is particularly important that the micro-processor does not halt in an ill-defined state but can cope with unexpected software errors and handle them securely. What hardware would you need to add to a typical microprocessor that will help ensure reliable and safe handling of software faults?

The three parts carry, respectively, 25%, 25%, 50% of the marks.

Paper Ends