Question 1

1. a) (i)

$$\overline{A\bar{B}\bar{C}+AC}+A\bar{B}C = \overline{A\bar{B}\bar{C}}.\overline{AC}+A\bar{B}C$$
$$= (\bar{A}+B+C)(\bar{A}+\bar{C})+A\bar{B}C$$
$$= \bar{A}+\bar{A}B+\bar{A}C+\bar{A}\bar{C}+B\bar{C}+A\bar{B}C$$
$$= \bar{A}(1+\bar{B}+C+\bar{C})+B\bar{C}+A\bar{B}C$$
$$= \bar{A}+B\bar{C}+A\bar{B}C = \bar{A}+\bar{B}C+B\bar{C}$$
$$= \bar{A}+\bar{B}(C+\bar{C}) = \bar{A}+\bar{B}$$

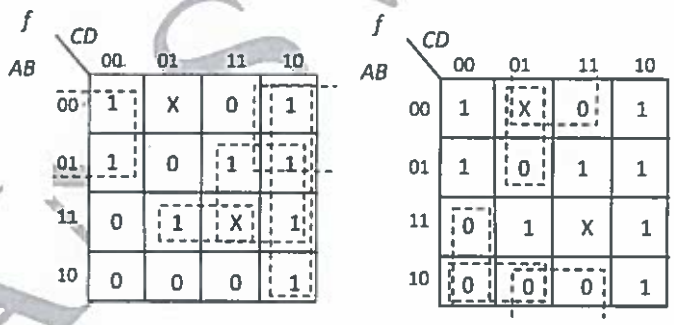
[4]

(ii)

$$\overline{\overline{A+\bar{B}}+C} = (A+B)\bar{C}$$
$$= A\bar{C}+B\bar{C} = A\bar{C}(B+\bar{B})+B\bar{C}(A+\bar{A})$$
$$= AB\bar{C}+A\bar{B}\bar{C}+\bar{A}B\bar{C}$$

[4]

b)



$$f = \bar{A}\bar{D}+ABD+BC+C\bar{D}$$
$$f = (\bar{A}+C+D)(\bar{A}+B+C)(A+C+\bar{D})(B+\bar{D})$$

Here, 1 mark each for the Karnaugh maps, 1 for the correct grouping in each map, and 1 for each of the final expressions.

[6]

c) (i) 36FDC008 (ii) F6FDC008
This question requires sign extension. Give two marks for each part.

[4]

d)

Decimal	Hexadecimal	Signed binary (8 bits wide)	Unsigned binary
4.6875			1101.1011
-39		1101 1001	
	DA2F		1101 1010 0010 1111

Give 2 marks per answer.

[6]

e)

A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Here, 2 marks each for S and C_o

[4]

f) $g = \overline{A}\overline{B} + A\overline{B}\left(A\overline{E} + \overline{A}\overline{E}\right) = \overline{A}\overline{B} + A\overline{B}\overline{E} = \overline{B}\left(\overline{A} + A\overline{E}\right) = \overline{B}\left(\overline{A} + \overline{E}\right)$

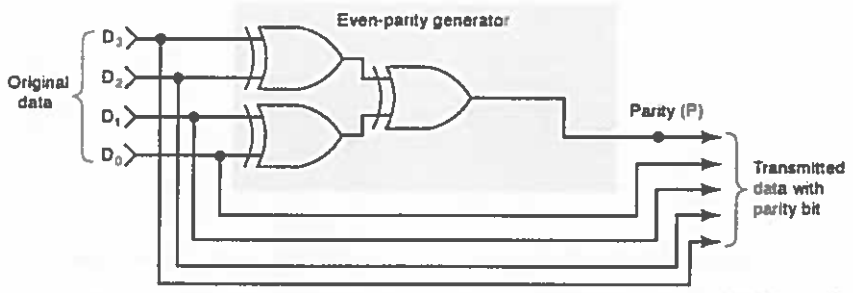
$f = \overline{C}\,\overline{D} + \overline{C}Dp + C\overline{D} = \overline{D} + \overline{C}Dp = \overline{D} + \overline{C}p$

$= \overline{D} + B\overline{C}\left(\overline{A} + \overline{E}\right) = \overline{D} + \overline{ABC} + \overline{BCE}$

Give 2 marks for understanding multiplexer and XOR gate operation, 2 marks for Boolean simplification, and 2 each for the correct final expressions.

[8]

g)

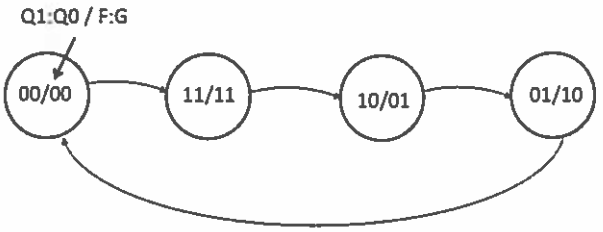


Give 2 marks for showing an understanding of parity and the use of XOR gates, and 2 for the connections.

[4]

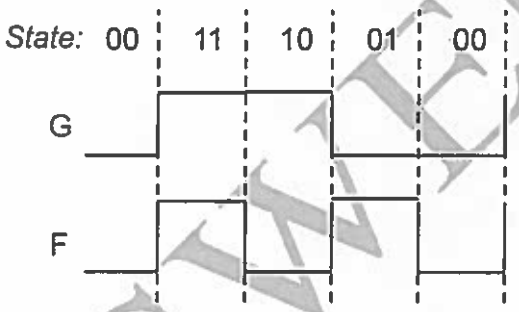
Question 2

(a)
(i)



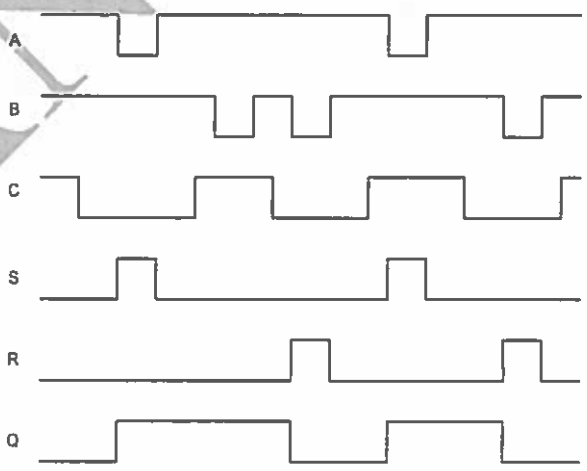
Give 4 marks for correct states and labels, and 2 for connections. [6]

(ii)



Give three marks per waveform. [6]

b)



Give 2 marks per waveform for S, R and Q. [6]

c)
(i) The transmission gate is not explicitly covered in the lectures, however all components of this have been covered. It can be seen from the circuit that the FETs are either both 'on' (B = high, logic 1) or both 'off' (B = low, logic 0). When the FETs are 'on', Q = A and when the FETs are 'off', the output terminal Q is floating or disconnected from input A. If we assume no charge is lost from the output (ideal FET switches), the previous state will be retained. This gives the following truth table:

A	B	Q
0	0	Q (or floating)
0	1	0
1	0	Q (or floating)
1	1	1

Give 2 marks for assumptions regarding Q, and 4 marks for the truth table.

[6]

(ii)

X	Y	Z
0	0	Z
0	1	0=A
1	0	Z
1	1	1=A

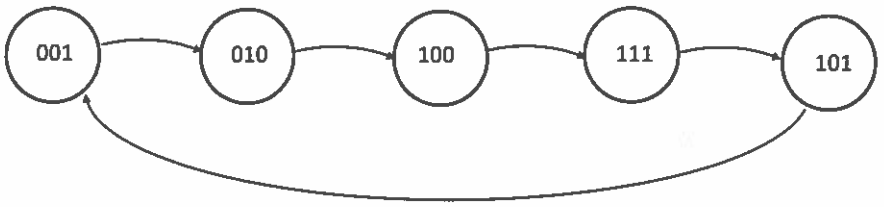
The above truth table is similar to a D latch.

Give 4 marks for truth table and 2 for seeing this is a D latch.

[6]

Question 3

3. a) i) Using states Q2Q1Q0 to define the FSM:



Give 1 mark for five states, 2 for labelling and 2 for correct interconnections. [5]

b) Using Q2Q1Q0 as the present state of the FSM, and $Q2^{+}Q1^{+}Q0^{+}$ as the next state:

Q2	Q1	Q0	$Q2^{+}$	$Q1^{+}$	$Q0^{+}$
0	0	1	0	1	0
0	1	0	1	0	0
1	0	0	1	1	1
1	1	1	1	0	1
1	0	1	0	0	1

Give 1 mark for each correct row of the table.

[5]

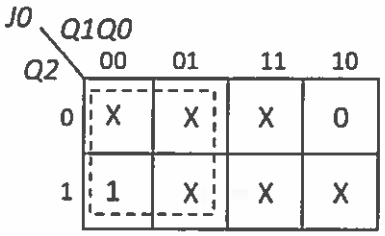
c) The FSM can be implemented using three J-K flip-flops, one each to store Q2, Q1 and Q0.

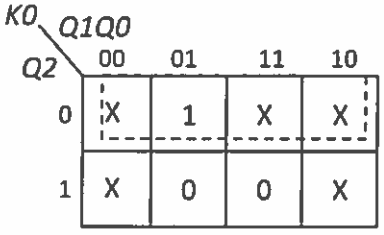
We first require the output transition table for the J-K flip-flop:

Output transition	J	K
0 → 0	0	X
0 → 1	1	X
1 → 0	X	1
1 → 1	X	0

Using this table, it is possible to fill out the J-K inputs needed for each output, where we assume undefined states are don't cares:

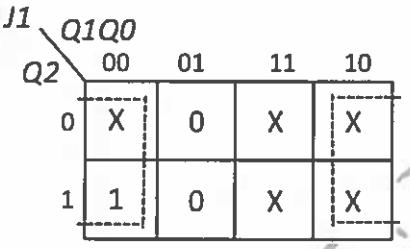
For $Q0^+$:

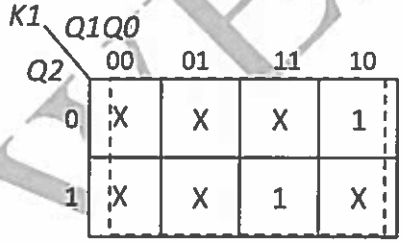




$\Rightarrow \quad J0 = \overline{Q1} \qquad K0 = \overline{Q2}$

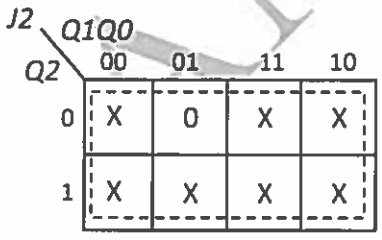
For $Q1^+$:

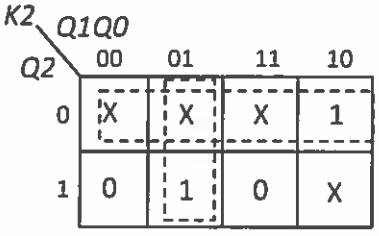




$\Rightarrow \quad J1 = \overline{Q0} \qquad K1 = 1$

For $Q2^+$



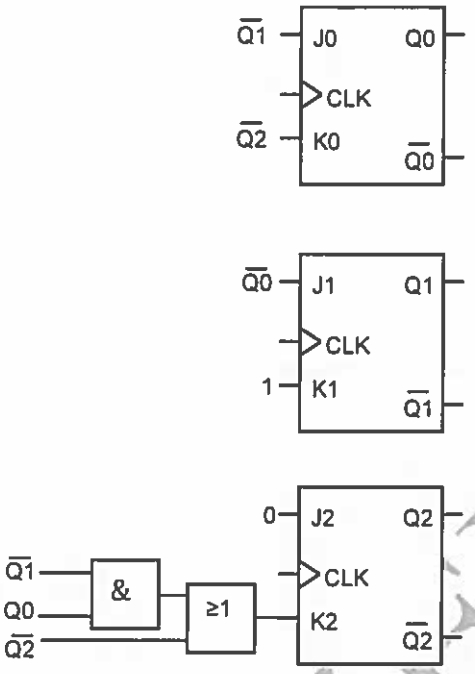


$\Rightarrow \quad J2 = 0 \qquad K2 = \overline{Q2} + \overline{Q1}Q0$

Give 3 marks for the output transition table, 1 mark for each of the six Karnaugh maps, and 1 mark for each of the six J, K expressions.

[15]

d)



Give 1 mark for showing three J-K flip-flops, and 4 marks for the correct inputs and gates at the flip-flops. Note that the diagram above does not show interconnects from output to input terminals for clarity, however inputs are labelled to show connections.

[5]