IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2013

EEE PART I: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 1

Friday, 7 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : A.S. Holmes
Second Marker(s) : C. Papavassiliou

The Questions

1. For each part of this question, state clearly any assumptions made in your calculations.

a) For the circuit in Figure 1.1, determine the operating mode of the MOSFET and the value of the voltage V.

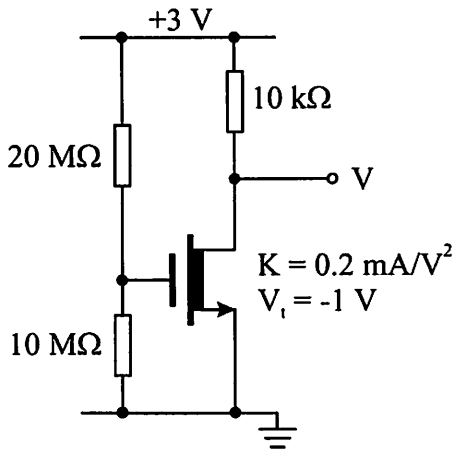


Figure 1.1

[6]

b) For the circuit in Figure 1.2, determine the operating modes of both transistors and the value of the current I.

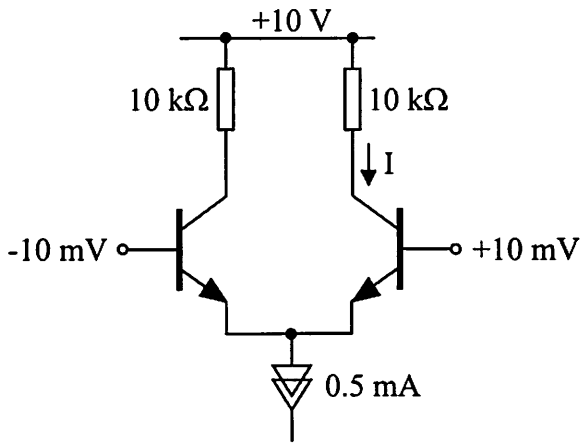


Figure 1.2

[6]

c) A grounded common emitter amplifier is constructed using a BJT with an Early voltage of 110 V. If the load resistance in the collector circuit is 5 kΩ, and the transistor is biased at a collector current of 1.0 mA, what is the small-signal voltage gain of the circuit? Assuming the same bias current, by what ratio could the gain of the amplifier be increased if the load resistor were replaced by an active load based on the same type of transistor. [6]

Question 1 continues on the next page...

Question 1 continued

d) Figure 1.3 shows an enhancement mode MOSFET connected as a 2-terminal component. Sketch the I-V characteristic of this device for $V \geq 0$, marking on your graph any boundaries between different operating modes.

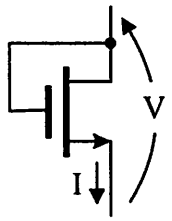


Figure 1.3 [6]

e) A 5V input pulse of duration 10 μs is applied to the circuit in Figure 1.4 by a CMOS logic gate. Assuming the circuit had reached steady state before the pulse was applied, calculate the time interval over which the output voltage is below 5 V. Also sketch the variation of V_{OUT} over a period of 20 μs starting at the rising edge of the pulse.

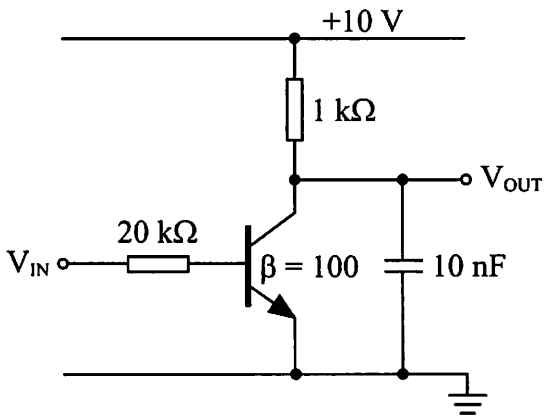


Figure 1.4 [10]

f) The characteristic equation for a Colpitts oscillator is of the form:

$$s^3LC_1C_2 + \frac{s^2LC_2}{R} + s(C_1 + C_2) + \left(g_m + \frac{1}{R}\right) = 0$$

where L, C_1 and C_2 are the reactive components, R represents the circuit losses, and g_m is the usual transistor parameter. By assuming an appropriate form for the complex frequency, s, derive an expression for the oscillation frequency. Also determine the minimum transconductance required for oscillation to occur. [6]

2. a) Determine the collector bias current and quiescent output voltage for the amplifier in Figure 2.1, stating clearly any assumptions you make. Your calculation should take into account the base current of the transistor. [8]

b) Draw a small-signal equivalent circuit for the amplifier, assuming the bypass capacitor is effectively short-circuit, and hence determine the small-signal macromodel parameters (input resistance, output resistance and voltage gain) in the mid-band. [12]

c) Two amplifiers similar to that in Figure 2.1 are cascaded between a signal source and a load, as shown in Figure 2.2. Draw a small-signal circuit for the overall set-up, representing the amplifiers by their macromodels. Hence determine the overall voltage gain v_L/v_S for this arrangement at frequencies for which all the coupling capacitors are effectively short-circuit. [10]

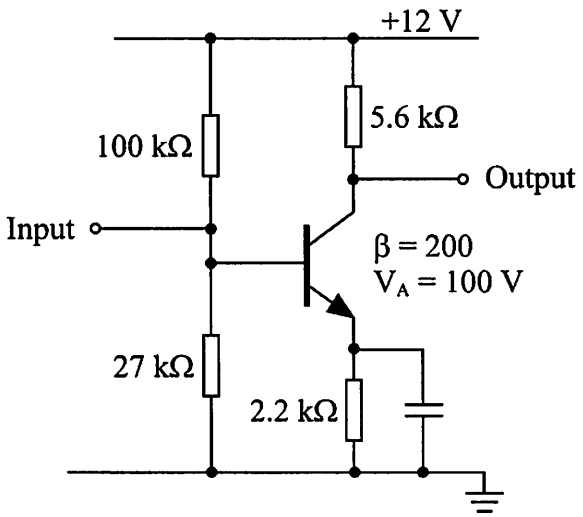


Figure 2.1

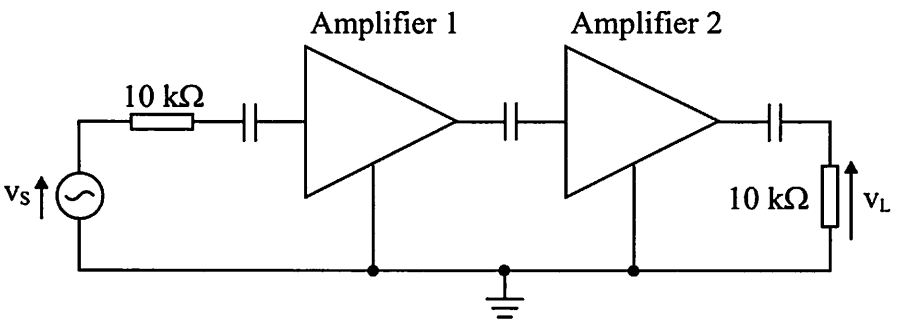


Figure 2.2

3. Figure 3.1 shows a single-stage CMOS amplifier in which both MOSFETs contribute to the small-signal gain.

a) Explain the role of the resistor R_G, and show that the quiescent output voltage V_{OUT} is given by:

$$V_{OUT} = \frac{V_{DD} + V_{t2} + V_{t1}\sqrt{(K_1/K_2)}}{1 + \sqrt{(K_1/K_2)}}$$

where the symbols K and V_t denote the usual MOSFET parameters, and the subscripts 1 and 2 refer to Q1 and Q2 respectively.

Hence determine the value of V_{OUT}, and the quiescent drain current in each MOSFET. [12]

b) Draw a small-signal equivalent circuit of the amplifier, including R_G, and calculate the small-signal voltage gain at frequencies for which the input capacitor is effectively short-circuit. Also determine the small-signal input resistance. [12]

c) If a sinusoidal input signal is applied to the amplifier, over what range of input signal amplitudes will both transistors remain active? You may assume that the input capacitor has negligible impedance at the signal frequency. [6]

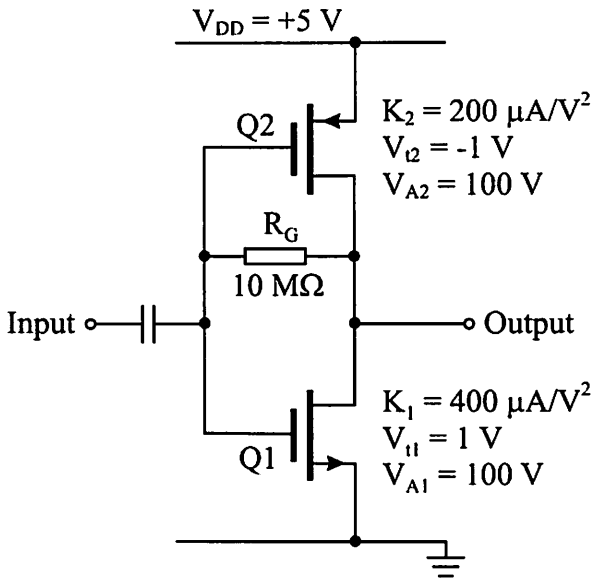


Figure 3.1

Analogue Electronics 1 – SOLUTIONS 2013

Question 1

a) The MOSFET has V_{GS} = 1 V and so is conducting ($V_{GS} > V_t$ = -1 V). If it were in the active mode, the drain current would be $I_D = K(V_{GS} - V_t)^2 = 0.2m\times(1 - -1)^2 = 0.8$ mA. However, this would imply $V_D = 3 - 0.8m\times10k = -5$ V which is not possible. It follows that the MOSFET must be in the **triode mode.**

In triode mode, we have $I_D = K[2(V_{GS} - V_t)V - V^2] = (3 - V)/10k$. Putting V_{GS} = 1 V, Vt = -1 V and K = 0.2 mA/V^2, this becomes $2[4V - V^2] = 3 - V$, or $2V^2 - 9V + 3 = 0$. The roots of this quadratic are 4.14 V and 0.363 V, and the first of these can be rejected as it is $>V_{DD}$. So **V = 0.363 V.** [6]

b) The differential input voltage is small (-20 mV) so this question can be answered using either small-signal analysis or large signal equations. Both methods are shown below, and in both cases base currents are assumed to be negligible.

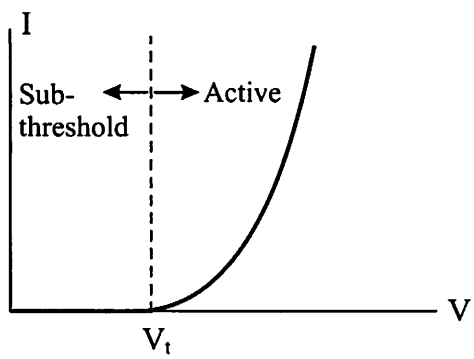
Small-signal method: single-ended gain to RH output is $A_d = g_mR_C/2$ = (0.25mA/25mV) × 10k/2 = 50, so signal voltage at RH output is -20m x 50 = -1 V. Quiescent voltage across RH collector resistor is 0.25m × 10k = 2.5 V, so total voltage across resistor including effect of input voltage is 2.5 + 1 = 3.5 V, and current is **I = 3.5/10k = 0.35 mA.**

Large signal method: RH collector current is $I = I_0/[1 + \exp(V_D/V_T)]$ where I_0 is the tail current. With I_0 = 0.5 mA, V_D = -20 mV and V_T = 25 mV this gives **I = 0.345 mA.** [6]

c) The small-signal voltage gain for a grounded C.E. amplifier is $A_v = -g_m(R_C//r_o)$. (This can be quoted as a standard result.) In this case we have $g_m = I_C/V_T$ = 1.0m/25m = 40 mS, RC = 5 kΩ and $r_o = V_A/I_C$ = 110/1m = 110 kΩ, so $R_C//r_o$ = 4.78 kΩ and **A_v = -191.**

With an active load, the gain would become $A_v = -g_m(r_o//r_o) = -g_mr_o/2$ = -2200, so the ratio of gains is **2200/191 = 11.5.** [6]

d) The (enhancement mode) MOSFET has $V_{DS} = V_{GS} = V$ and consequently is active provide $V > V_t$ (because $V_{DS} = V_{GS}$ implies $V_{DS} > V_{GS} - V_t$). Also, I is just the drain current (since I_G = 0), so we have $I = 0$ for $V \le V_t$ and $I = K(V - V_t)^2$ for $V > V_t$.



[6]

Question 1 continued

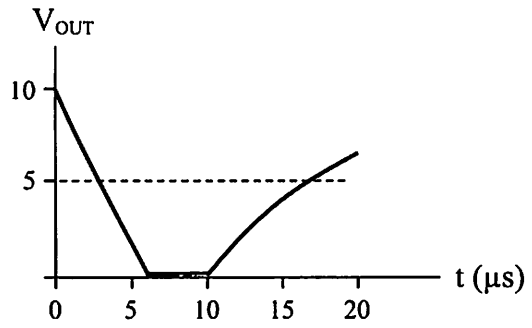
e) Initially the circuit will be in steady state with the transistor off. The capacitor will have charged up to the supply voltage, so the output voltage will be +10 V.

Immediately following the rising edge of the pulse (assumed to occur at t = 0), the transistor will be active. Assuming V_{BE} = 0.7 V, the base current will be $I_B = (5 - 0.7)/20k = 215\ \mu A$ and the collector current will be $I_C = \beta I_B = 21.5$ mA. If the transistor remained active, the new steady-state output voltage would be $10 - 0.0215 \times 1k = -11.5$ V. The initial trajectory of the output voltage is therefore $V_{OUT} = -11.5 + (10 + 11.5)\exp(-t/\tau)$ with $\tau = 1k \times 10n = 10\ \mu s$.

The time taken for the output voltage to fall to 5 V is obtained by substituting $V_{OUT} = 5$ into the above equation. This gives $t = \tau\ln(21.5/16.5) = 2.65\ \mu s$.

To see whether the transistor saturates we substitute V_{OUT} = 0.2 V into the output voltage equation, which after rearrangement gives $t = \tau\ln(21.5/11.7) = 6.08\ \mu s$. So, the transistor does saturate during the input pulse.

At t = 10 μs the input goes low, and the transistor turns off. The capacitor then charges back up to the supply voltage. The initial output voltage is 0.2 V, and the steady state value is 10 V, so the equation for the output voltage trajectory is $V_{OUT} = 10 + (0.2 - 10)\exp(-t'/\tau)$ where $t' = t - 10\ \mu s$. The output voltage reaches 5 V at $t' = \tau\ln(9.8/5) = 6.73\ \mu s$ or $t = 16.73\ \mu s$. So the time spent below 5 V is **16.73 – 2.65 = 14.08 μs.** [6]



[4]

f) To find the frequency of stable oscillation, we look for roots of the characteristic equation for which s is purely imaginary, i.e. roots with s = jω, ω being the frequency of oscillation. Substituting this form of s into the c.e. we obtain:

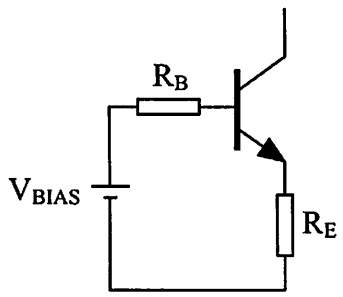
$$-j\omega^3 LC_1C_2 - \omega^2 LC_2/R + j\omega(C_1 + C_2) + (g_m + 1/R) = 0$$

The imaginary part of this equation gives $\omega^2 = (C_1 + C_2)/(LC_1C_2)$ so the resonant frequency in Hz is $\mathbf{f = \frac{1}{2\pi}\sqrt{(C_1 + C_2)/(LC_1C_2)}}$.

The real part gives $\frac{C_1 + C_2}{LC_1C_2} \cdot \frac{LC_2}{R} = g_m + \frac{1}{R}$, which simplifies to $\mathbf{g_m = \frac{C_2}{C_1 R}}$. This is the minimum transconductance for oscillation. [6]

Question 2

a) The bias cct is:



where $V_{BIAS} = 12 \times 27/(27 + 100) = 2.551$ V

and $R_B = 100k//27k = 21.26$ kΩ

KVL gives: $I_E R_E + V_{BE} + I_B R_B = V_{BIAS}$

$\Rightarrow I_E = (V_{BIAS} - V_{BE})/[R_E + R_B/(1 + \beta)]$

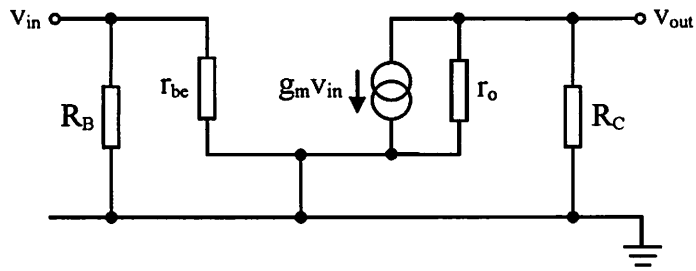
Assuming $V_{BE} = 0.7$ V, this gives $I_E = 0.8028$ mA

Assuming transistor active, $\mathbf{I_C = \alpha I_E = 0.799\ mA.}$

With this I_C value, $\mathbf{V_{OUT} = 12 - 0.799m \times 5.6k = 7.53\ V.}$

Mode check: $V_{OUT} > V_B$, so active assumption was correct. [8]

b) SSEC:



$g_m = I_C/V_T = 0.799m/25m = 32$ mS

$r_{be} = \beta/g_m = 200/0.032 = 6.25$ kΩ

$r_o = V_A/I_C = 100/0.799m = 125$ kΩ

[6]

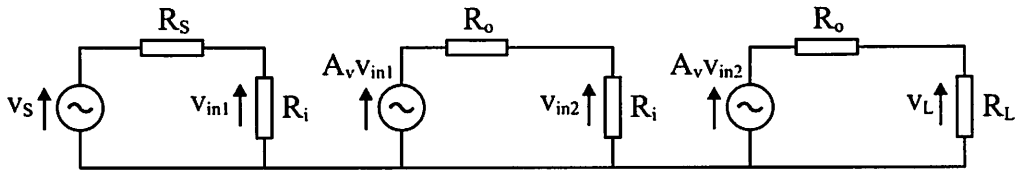
Macromodel parameters, by inspection of SSEC:

$\mathbf{R_i = R_B//r_{be}} = 21.26k//6.25k = \mathbf{4.83\ k\Omega}$

$\mathbf{R_o = R_C//r_o} = 5.6k//125k = \mathbf{5.36\ k\Omega}$

$\mathbf{A_v = -g_m R_o} = -0.032 \times 5.36k = \mathbf{-172}$ [6]

c) Overall SSEC in mid-band is:



[5]

and, by inspection: $$v_L = \frac{R_L}{R_L + R_o} \cdot A_v \cdot \frac{R_i}{R_i + R_o} \cdot A_v \cdot \frac{R_i}{R_i + R_S} v_S$$

Evaluating: $$\frac{\mathbf{v_L}}{\mathbf{v_S}} = (-172)^2 \frac{10}{10 + 5.36} \cdot \frac{4.83}{4.83 + 5.36} \cdot \frac{4.83}{4.83 + 10} = \mathbf{+2973}$$ [5]

Question 3

a) R_G sets the operating point by imposing the condition $V_{GD} = 0$ on both FETs (when there is no input signal current).

[2]

Both FETs are active, and $I_{D1} = I_{D2} = I_D$ (since $I_G = 0$)

$\Rightarrow$ $I_D = K_1(V_{OUT} - V_{t1})^2 = K_2(V_{OUT} - V_{DD} - V_{t2})^2$

And, taking $\sqrt{}$ $\sqrt{(K_1/K_2)}(V_{OUT} - V_{t1}) = \pm (V_{OUT} - V_{DD} - V_{t2})$

Both FETs must be above threshold, so take –ve sign

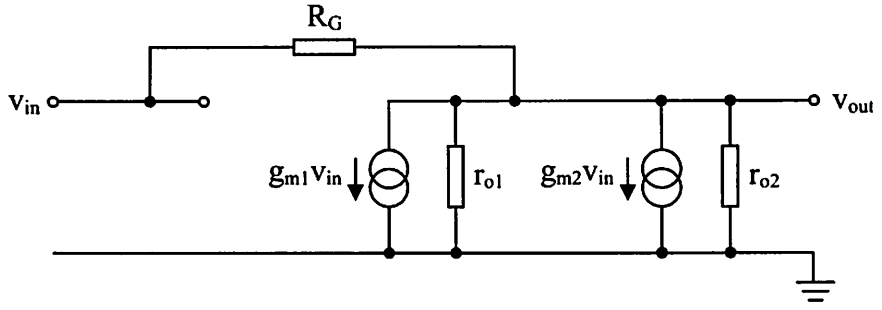
$\Rightarrow$ $V_{OUT}[1 + \sqrt{(K_1/K_2)}] = V_{DD} + V_{t2} + \sqrt{(K_1/K_2)}V_{t1}$

$\Rightarrow$ $V_{OUT} = [V_{DD} + V_{t2} + \sqrt{(K_1/K_2)}V_{t1}]/ [1 + \sqrt{(K_1/K_2)}]$ as required [6]

Putting $V_{DD} = 5$, $V_{t1} = 1$, $V_{t2} = -1$, $\sqrt{(K_1/K_2)} = \sqrt{2}$ gives $\mathbf{V_{OUT}} = (4 + \sqrt{2})/(1 + \sqrt{2}) = \mathbf{2.243\ V}$

$\mathbf{I_D} = K_1(V_{OUT} - V_{t1})^2 = 0.4m(2.243 - 1)^2 = \mathbf{0.618\ mA}$ [4]

b) SSEC:



[6]

KCL at the output node gives: $g_{m1}v_{in} + v_{out}/r_{o1} + g_{m1}v_{in} + v_{out}/r_{o2} + (v_{out} - v_{in})/R_G = 0$.
Rearranging, the voltage gain is obtained as:

$$\mathbf{A_v} = v_{out}/v_{in} = -(g_{m1} + g_{m1} - 1/R_G)(r_{o1}//r_{o2}//R_G)$$

$g_{m1} = 2\sqrt{(K_1 I_D)} = 0.994$ mA/V, $g_{m1} = 2\sqrt{(K_2 I_D)} = 0.703$ mA/V, $r_{o1} = r_{o2} = V_A/I_D = 162$ kΩ

$\Rightarrow \mathbf{A_v} = -1.697m \times 80.3k = \mathbf{-136}$ [3]

$i_{in} = (v_{in} - v_{out})/R_G = v_{in}(1 - A_v)/R_G \Rightarrow \mathbf{R_{in}} = R_G/(1 - A_v) = 10M/137 = \mathbf{73\ k\Omega}$ [3]

c) Q1 will remain active provided $V_{OUT} \geq V_G - V_{t1}$ where V_G is the gate voltage common to both FETs. Similarly, Q2 will remain active provided $V_{OUT} \leq V_G - V_{t2}$. If we ignore changes in V_G due to the input signal, which is reasonable since the gain is relatively high, we can use quiescent value of V_G which is equal to the quiescent output voltage (2.243V). The output voltage range is then 1.243 to 3.243, and the maximum output signal amplitude is 2 V pk-pk. The corresponding input amplitude is 2/136 = 14.7 mV pk-pk.

If the input signal is taken into account then the limit for Q1 corresponds to the situation $(2.243 + A_v v_{in}) = (2.243 + v_{in}) - V_{t1}$ or $v_{in} = V_{t1}/(1 - A_V)$. A similar relation is obtained for Q2, and the maximum input amplitude becomes 2/137 = 14.6 mV pk-pk. [6]