IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2018

EEE PART I: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 1

Corrected copy

Tuesday, 5 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : A.S. Holmes
Second Marker(s) : C. Papavassiliou

The Questions

1. For each part of this question, state clearly any assumptions made in your calculations.

   a) For the circuit in Figure 1.1, determine the minimum supply voltage V_{DD} for which the MOSFET will be in the active mode.

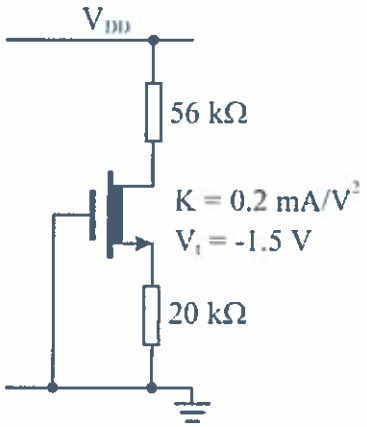

Figure 1.1 [6]

   b) For the circuit in Figure 1.2, derive a relationship between the input and output currents when both transistors are active. You should neglect base currents and assume the transistors are matched. Hence determine the value of R required to give I_{OUT} = 10 μA when I_{IN} = 100 μA.

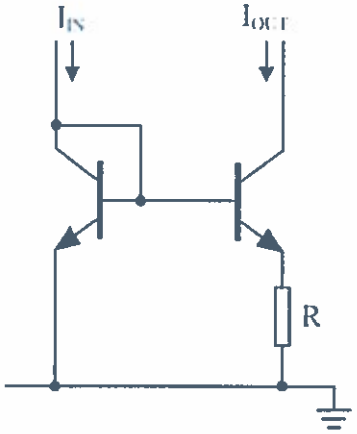

Figure 1.2 [6]

   c) Using small-signal analysis, and neglecting output resistance, show that a signal voltage applied between the B and E terminals of a Darlington pair is shared equally by the two base-emitter junctions. Hence show that the transconductance of such a device is expected to be 0.5× that of a BJT biased at the same collector current. [8]

Question 1 continues on the next page...

Question 1 continued

d) For the circuit in Figure 1.3, determine the operating modes of both MOSFETs and the value of the voltage V_G.

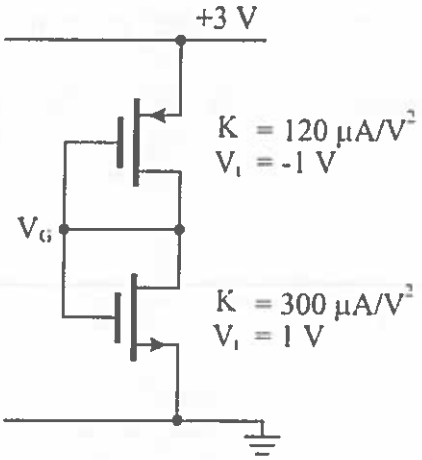

Figure 1.3

[6]

e) Briefly describe and explain the differences between Class A, Class AB, and Class B output stages, referring to signal integrity, conduction angle, and power consumption. [6]

f) The voltage V_{IN} applied to the circuit in Figure 1.4 is switched from +5 V to zero at time t = 0, having previously been held at +5 V for a long time. It remains at zero for 20 μs before switching back to +5 V. The resulting output voltage transient is as shown in the graph to the right. Calculate the voltages V_A, V_B, V_C.

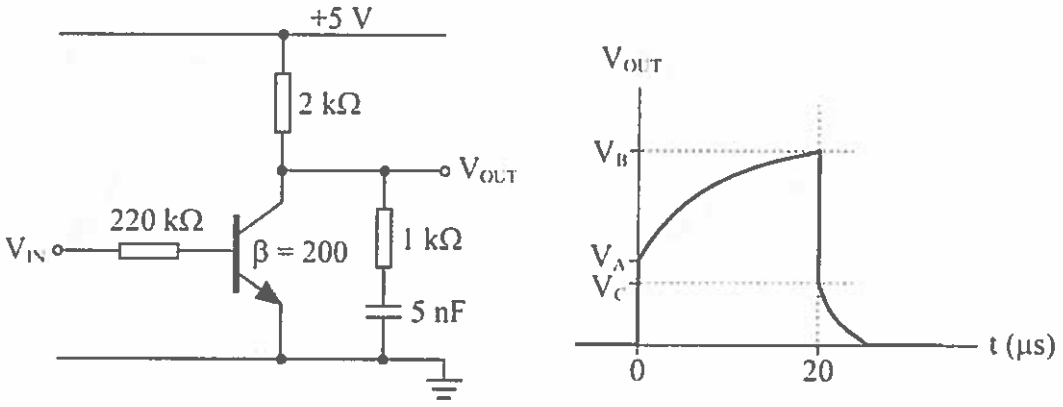

Figure 1.4

[8]

2. Figure 2.1 shows a common-emitter amplifier in which the amplifying transistor is biased using a 1 mA current source. The current source is non-ideal and has an output resistance of r_e = 120 kΩ. According to the datasheet for the amplifying transistor, the β value is typically 200 but can lie anywhere in the range 100 to 300. The Early voltage is 100 V.

a) Assuming β = 200, determine the value of R_F that will give a quiescent output voltage of +4 V. You may neglect the current source output resistance. Also calculate, for the same value of R_F, the quiescent output voltages corresponding to the maximum and minimum β values. How could the biasing arrangement be modified to reduce the dependence of the quiescent output voltage on the β value? [8]

b) Draw a small-signal equivalent circuit for the amplifier, and hence evaluate its small-signal voltage gain. Also calculate the small-signal input resistance. Your analysis should include all resistances in the circuit and assume β = 200. [12]

c) To increase the input resistance of the amplifier, the bias resistor R_F is replaced by the RC network shown in Figure 2.2. Assuming the capacitor has negligible impedance at signal frequencies, calculate the voltage gain and input resistance for the modified circuit, and hence verify that the input resistance is indeed increased. [6]

d) Suggest a further modification to the circuit that could yield even higher input resistance while retaining high voltage gain. Your modification can include adding one or more components. [4]

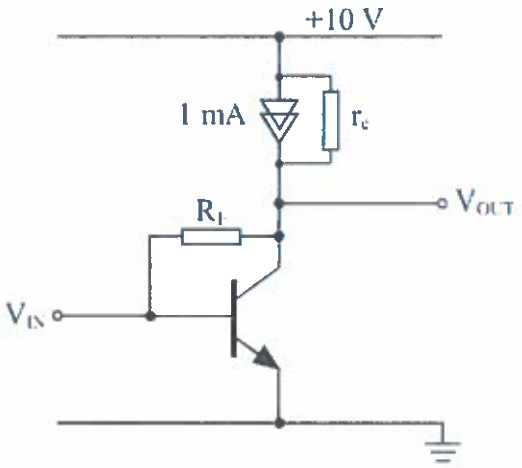

Figure 2.1

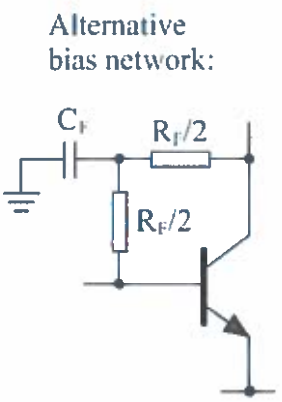

Figure 2.2

3. Figure 3.1 shows a MOS differential amplifier in which all four transistors are matched, with parameters $K = 0.5$ mA/V^2, $V_t = 1$ V and $V_A = 100$ V. You may neglect the effect of the finite output resistance when answering parts a) and b).

   a) Choose the values of R_{BIAS} and R_D to give a bias current of $I = 0.25$ mA and a quiescent output voltage of $V_{OUT} = +5$ V when all transistors are active. Also determine the voltage at the drain of Q4 when $V_{IN1} = V_{IN2} = 0$ V. [8]

   b) Determine the upper and lower limits of the common mode input voltage range of the amplifier. [6]

   c) Draw a small-signal equivalent circuit of the amplifier and, by considering the response to a purely differential input signal $v_d = (v_{in1} - v_{in2})$, derive an expression for the single-ended differential voltage gain, A_d. Also calculate the numerical value of A_d. [12]

   d) It is proposed that the passive load resistors be replaced by a current mirror active load to achieve higher voltage gain. Assuming no other changes are made, what is the maximum single-ended differential voltage gain that can be achieved with this modification if the current mirror transistors also have $V_A = 100$ V? [4]

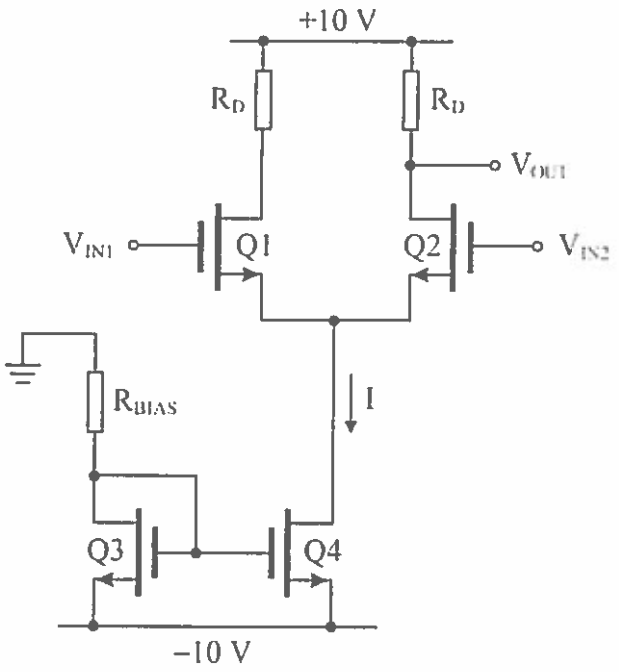

Figure 3.1