E4.20
AC3
ISE4.19

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2003

INTRODUCTION TO DIGITAL INTEGRATED CIRCUIT DESIGN

Monday, 28 April 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

Corrected Copy

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung
Second Marker(s) : T.J.W. Clarke

Information for Invigilators:

Students may bring any written or printed aids into the examination.

Information for Candidates:

Students may need red, green, blue, yellow and black coloured pens.

The Questions

1. a) Figure 1.1 (See the colour supplementary sheet) shows the layout of a CMOS cell with four inputs `A`, `B` and `C`, and two outputs `OUT1` and `OUT2`. Extract and draw the transistor-level schematic diagram.

[10]

b) What function does this circuit perform?

[2]

c) Draw the vertical cross sections through the chip along the lines `PP'` and `QQ'`. Label your diagram and indicate the different types and levels of doping (e.g. p^-, n^+ etc).

[8]

2. a) Using your own group design project as a reference, describe the proper procedure for designing a full-custom integrated circuit.

[4]

b) Draw a diagram showing the hierarchy of cells used in the chip that your group designed. Comment on the partitioning of your design in light of the cell hierarchy.

[4]

c) Outline your own personal contributions and justify any design decisions made. If you and your group were to design the same chip again, what if anything would you have done differently?

[8]

d) Explain and assess the strategy you adopted for verifying and testing your chip.

[4]

3. a) Assume that you are a project leader in a company designing an ASIC for a new product for the telecommunication market. You are told that the expected demand can be as high as 1 million units in the first year. The complexity of the circuit that your team is designing is around 50,000 gates. You are required to decide which technology you should implement this ASIC, i.e. full custom, standard cell, gate array or FPGA. State what additional information you must acquire before you can make your decision. After stating clearly any additional assumptions that you have made, explain and justify your decision.

[5]

b) Figure 3.1 shows the transistor level schematic of a standard cell design. It is known that T6 is a minimum sized transistor and all other transistors are appropriately sized. Given that the timing diagram for the input signals `CLK`, `A` and `B` is as shown in Figure 3.2, draw the timing diagram for the signals at `P`, `Q`, `R` and `OUT`. Label your timing diagram with the following four possible signal states: *driven low* (**DL**), *driven high* (**DH**), *charged low* (**CL**), *charged high* (**CH**) and *don't know* (**XX**).

[12]

c) Hence, or otherwise, explain the function of this cell.

[3]

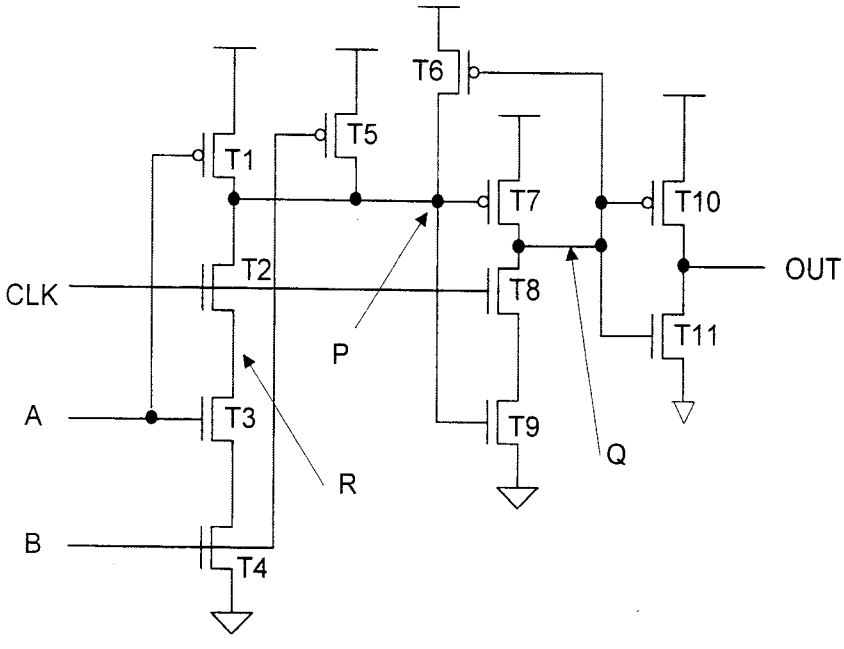

Figure 3.1

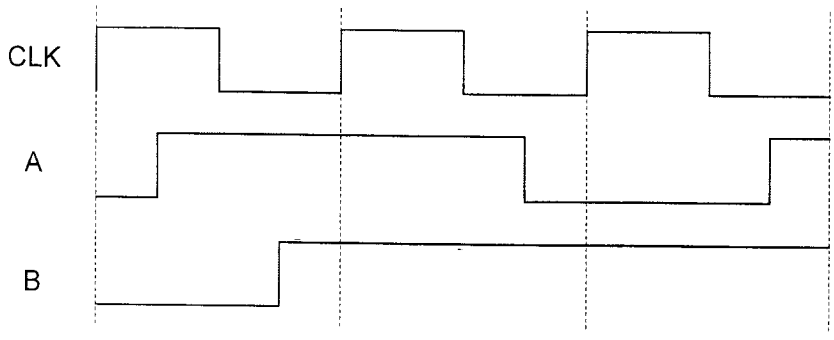

Figure 3.2

4. a) Implement the following Boolean function as a single compound (or complex) CMOS static gate.

$$y = \overline{(a \bullet b + c \bullet d) \bullet e}$$

[4]

b) Assuming that all the n-channel transistors have minimum width and length for the given technology, and that the mobility of an n-channel transistor is twice that of a p-channel transistor, size your circuit correctly so that the worst case rise and fall times are approximately equal.

[3]

c) Use symbolic layout representation (for example, a stick diagram), design the layout of your circuit.

[5]

d) Figure 4.1 shows a tristate bus driver with transistor sizes shown relative to unit size. By applying the Theory of Logic Effort, design an inverter chain to drive the enable input e of 128 such tristate bus drivers. You may assume that the first stage of your inverter chain may present an input capacitance of 6 unit-sized transistors. State any assumptions made.

[8]

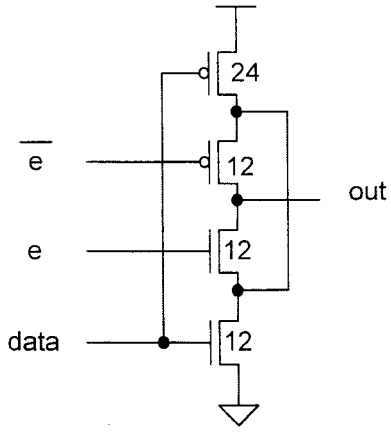

Figure 4.1

5. Figure 5.1 shows a synchronous bit-serial comparator cell where A and B inputs receive two 8-bit unsigned binary numbers with MSB first. The cell can be in one of three states representing S0, S1 and S2 as shown in Figure 5.2. A logic '1' on the R input resets the internal state of the cell to S0. The cell produces H and L outputs after one clock cycle delay which are respectively the higher and lower value of the input sequence in bit-serial form.

Design a transistor level implementation of this bit-serial comparator cell using a single phase clocking method.

[20]

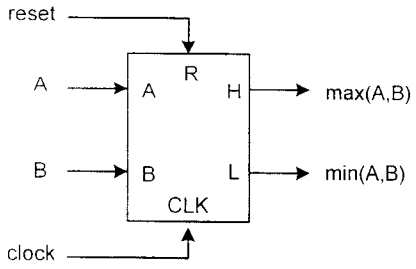

Figure 5.1

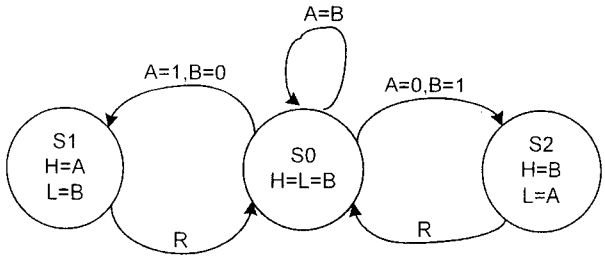

Figure 5.2

6. a) Discuss the advantages and disadvantages of:

(i) Pass-transistor logic

[3]

(ii) Dynamic logic

[3]

b) Figures 6.1 and 6.2 show two pass-transistor logic gates. Derive the truth tables for the two logic gates.

[12]

c) Hence or otherwise, deduce the function of these circuits.

[2]

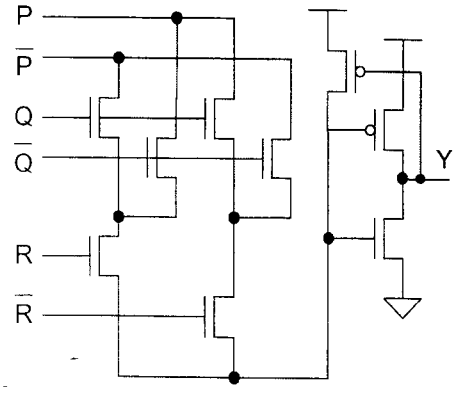

Figure 6.1

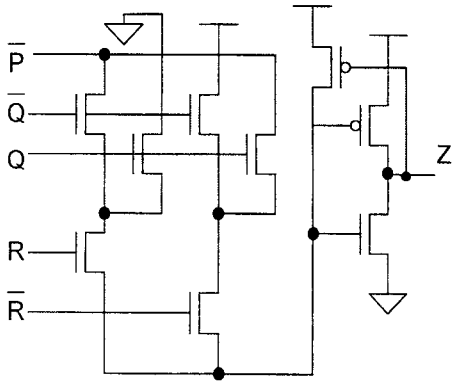

Figure 6.2

Colour Supplementary Sheet

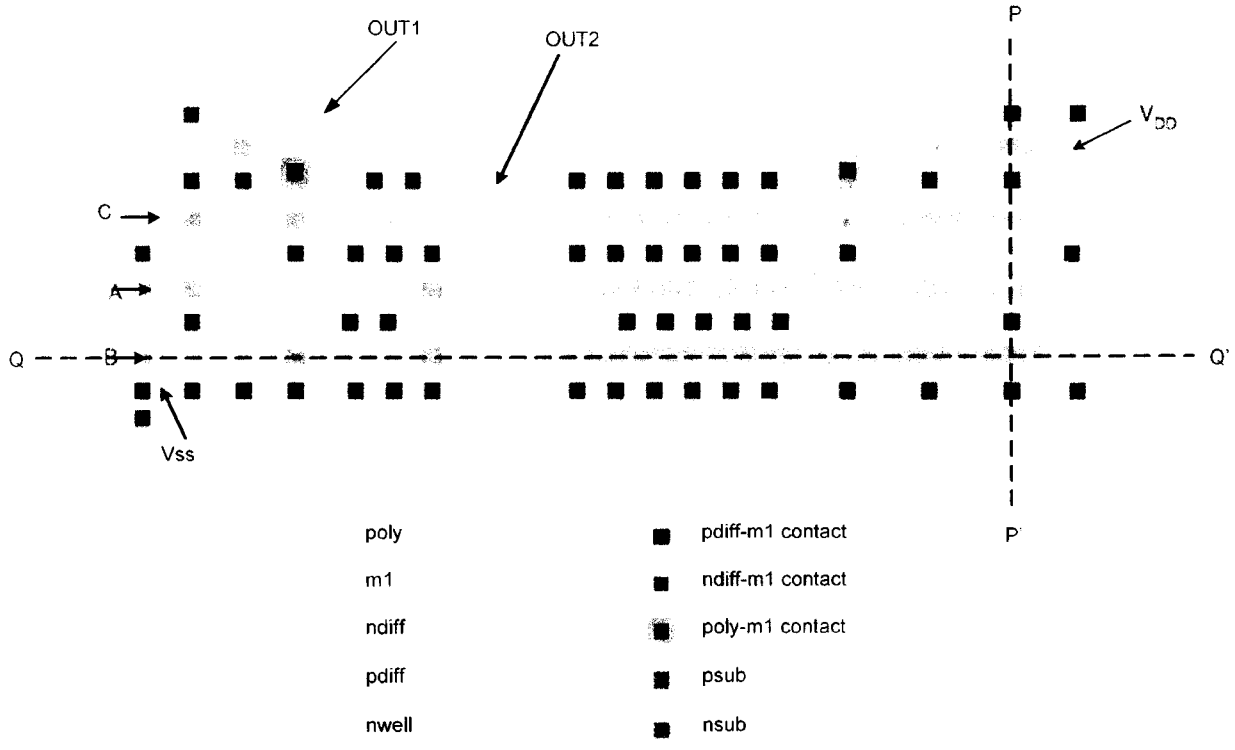

Figure 1.1 Layout of a full-custom cell for Question 1

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