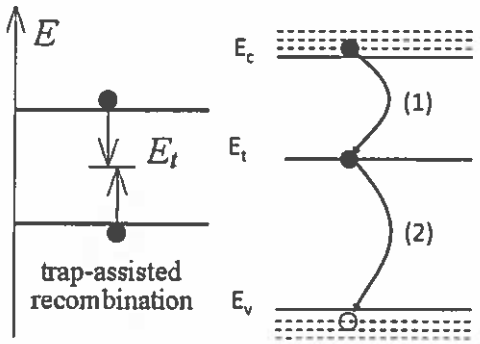
ANSWERS –2016

1. Devices EE2-10A

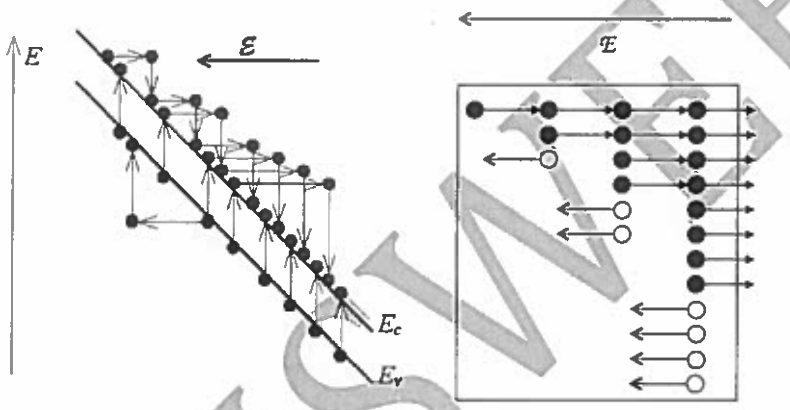
a) Trap assisted recombination (also called Shockley-Read-Hall or SRH recombination). [5]



electrons and holes recombine via a trap level which is an energy level within the bandgap associated to impurities and defects in the semiconductor. They can recombine within the trap or via the trap.

b) Impact ionisation

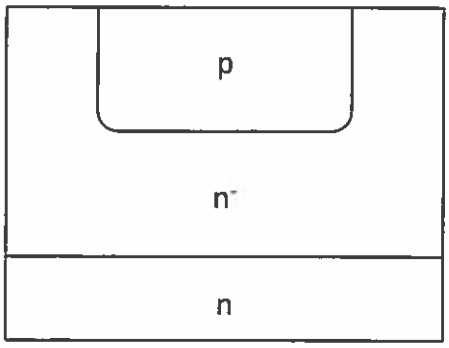
i) [5]



The diagram left illustrates impact ionisation on an energy band diagram, the one of the right within a material cross section.

Impact ionisation occurs under high electric field (high voltage per length). The carrier, electron or hole is accelerated by the high electric field, until it has high kinetic energy. Then it will collide, scatter, interact with a lattice atom, transfer its energy that then releases an electron-hole pair. The initial carrier together with the newly released pair will be accelerated by the field until their kinetic energy is sufficiently high that when interaction with an atom occurs, each can generate electron-hole pairs. Multiplier the initial number of e.g. electrons by 2^N electrons after N impact ionisation events.

ii) [5]



In order to reduce the probability for impact ionisation, the electric field must be kept small. This can be done by widening the drift region across which the reverse bias voltage occurs because the electric field = voltage/length. Therefore the devices are fabricated vertically to allow large lengths without consuming too much Si real estate.

The other aspect is to reduce the doping density such that the depletion region extends (widens) thus also reducing the electric field.

c) for lifetime = based on exercise done in class & completely worked out in coursenotes [10]

Note: the following is a copy and paste from the note, however for the exam answer all subscript p must be changed into n.

Solving the switching problem: $\frac{dQ_p(t)}{dt} = i_p(t) - \frac{Q_p(t)}{\tau_p}$

For $0 < t < t_{sd}$ we know that i_p remains constant at $-I_r$, thus:

$$\frac{dQ_p(t)}{dt} = -I_r - \frac{Q_p(t)}{\tau_p}$$

Separation of variables:

$$\frac{dQ_p(t)}{Q_p(t) + \tau_p I_r} = -\frac{dt}{\tau_p}$$

Integrate:

$$\int_{Q_p(0)}^{Q_p(t)} \frac{dQ_p(t)}{Q_p(t) + \tau_p I_r} = -\int_0^t \frac{dt}{\tau_p}$$

$$\ln\left(Q_p(t) + \tau_p I_r\right)\Big|_{\tau_p I_f}^{Q_p(t)} = -\frac{t}{\tau_p}$$

$$\ln\left(Q_p(t) + \tau_p I_r\right) - \ln\left(\tau_p I_F + \tau_p I_r\right) = -\frac{t}{\tau_p}$$

$$\ln\frac{\left(Q_p(t) + \tau_p I_r\right)}{\left(\tau_p I_F + \tau_p I_r\right)} = -\frac{t}{\tau_p}$$

$$Q_p(t) = -\tau_p I_r + \left(\tau_p I_F + \tau_p I_r\right)\exp\left(-\frac{t}{\tau_p}\right)$$

$$Q_p(t) = \tau_p\left[-I_r + \left(I_f + I_r\right)\exp\left(\frac{-t}{\tau_p}\right)\right]$$ (30)

The storage delay time t_{sd} can then be extracted by stating that at $t=t_{sd}$, $Q_p(t_{sd})=0$. Thus:

$$0 = \tau_p\left[-I_r + \left(I_f + I_r\right)\exp\left(\frac{-t_{sd}}{\tau_p}\right)\right]$$

The storage delay time is then (under the assumption of quasi steady state) :

$$t_{sd} \cong \tau_p \ln\left[1 + \frac{I_f}{I_r}\right]$$

t_{sd} is given in Fig. 1.1(b): $t_{sd} = 55.5\ 10^{-6}$ s. Since in the experiment (Fig. 1.1(a)) $I_F = I_R$ the derived expression for t_{sd} becomes: $t_{sd} = \tau_n \ln(2)$ thus $\tau_n = 8\ 10^{-5}$ s. [3]

The forward bias current is given in Fig. 1.1(b) to be i = 6.98 mA. This is the current that is effectively flowing through the diode. Since it is an n^+p diode, the diode current is mainly determined by the electrons minority carrier diffusion current through the p-type region. The expression of the diode current destiny can be found from the formulae sheet.

$J_n = \frac{eD_n n_p}{L_n}\left(e^{\frac{eV}{kT}} - 1\right)$ assuming $V = V_d >> V_T$ and using $L_n = \sqrt{D_n \tau_n}$ gives:

$I \approx I_n = \frac{eAn_i^2 L_n}{\tau_n N_A} exp\left(\frac{V_d}{V_T}\right)$ [3]

the diffusion length can be found from this expression

$L_n = \frac{I_n \tau_n N_A}{eAn_i^2 exp\left(\frac{V_d}{V_T}\right)}$

Note that the voltage in this expression is the diode voltage, not the applied voltage. The diode voltage can be found from: $V_{applied} = V_d + R\ I_d$ [1st year circuit analysis knowledge].

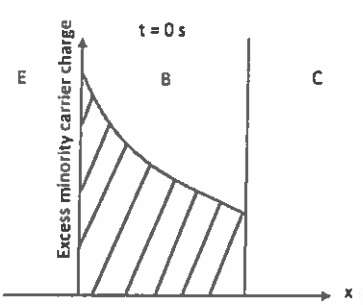
$V_d = 7.55\ V - 1000\ \Omega\ 6.98\ 10^{-3}\ A = 0.57\ V$ [3]

Note that V_d is indeed >> V_T.

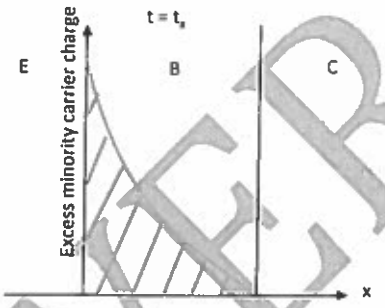
$$L_n = \frac{6.98\times10^{-3}\times8\times10^{-5}\times10^{16}}{1.6\times10^{-19}\times1\times(1.45\times10^{10})^2\times exp\left(\frac{0.57}{0.026}\right)} = 5\times10^{-2}cm$$ [1]

d) [5]

This is because the BJT was in oversaturation. This means that the base current was high such that the transistor goes into oversaturation because the output current is clamped by the load. In that case, the base current builds up a large stored charge in the base supplied by the 2 forward biased junctions (EB and BC). See figure. When the base voltage goes into reverse bias, first the additional base charge needs to be removed before the forward bias on the BC junction can get to zero and then turn reverse. It is at that moment ($V_{BC} = 0$) that we reach $t=t_a$ and i_c can drop together with i_b.



region (A) in fig. 1.2

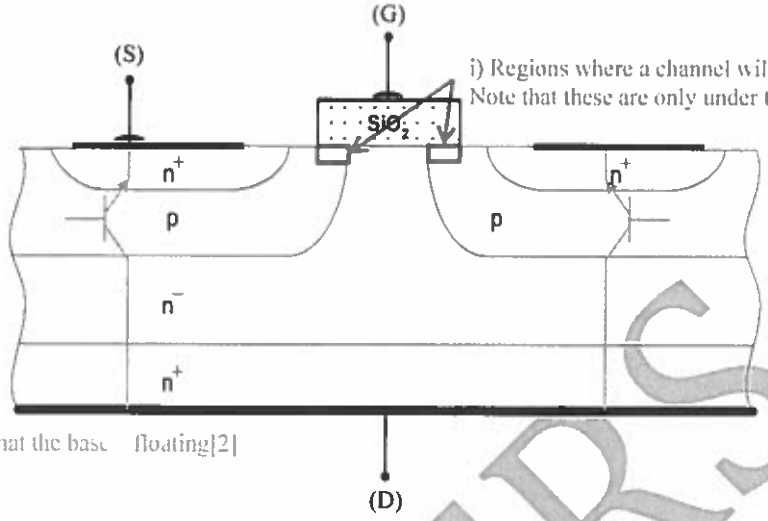


onset of region (B) in fig. 1.2

The charge difference between the blue plot and the orange plot needs to be removed before the BC voltage can go to reverse bias and $i_c = \beta\ i_b$ is followed again.

2.

a)



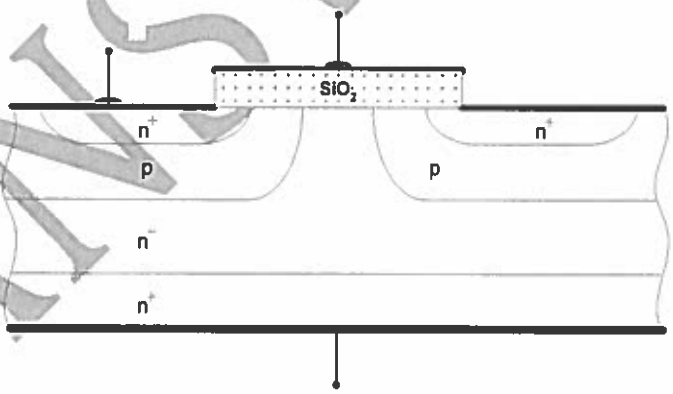
i) Regions where a channel will be formed when VGS > Vth
Note that these are only under the gate.[2]

ii) npn BJTs. Note that the base floating[2]

iii) (1) The gate overlap with the p-type region is not sufficient the invert a channel that connects the source via the channel to the drain. Thus the transistor is will be difficult or even impossible to switch on.

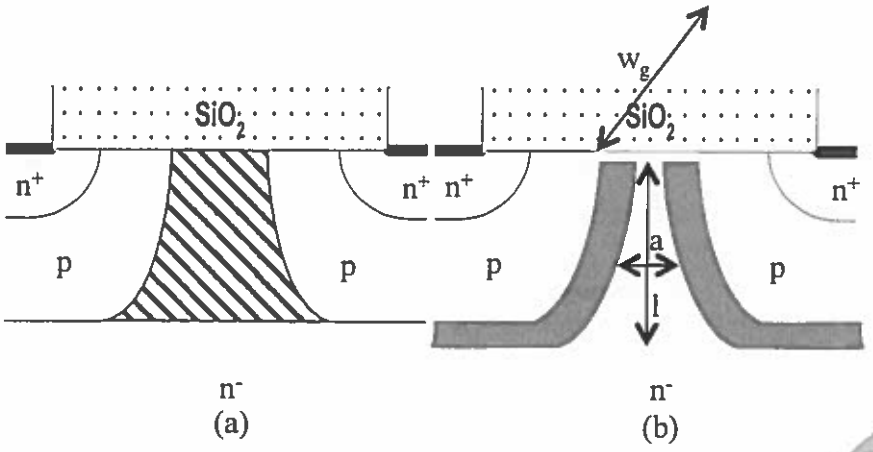
(2) The source contacts must overlap the p-type region in order to avoid the base of the parasitic BJTs to float and thus have any possible voltage depending on electrical noise that might switch it on. Connecting the p-region to the source connects it to the emitter, making $I_B = 0$. [4]

iv) . [2]



b)

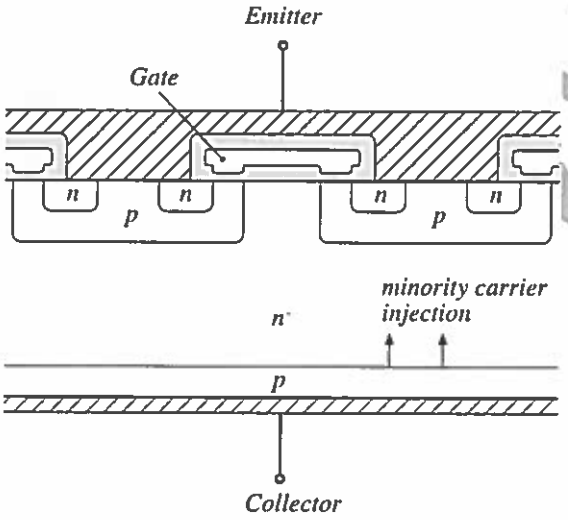
i) [5]



(a) (b)

Figure (a) indicates the region that is called the JFET region. The resistance of that region is determined by the width of the n^- region between the p-doped region and this is controlled by the depletion width around the pn^- junction. When the drain voltage is positive, then this junction is reverse biased and the depletion region will extend in the lowest doped area. See figure (b). Thus the remaining undepleted width between the two depletion regions is becoming narrower. The resistance is: $R = \frac{\rho \times l}{a \times w_g}$ with w_g the gate width. The more depletion V_{DS} increases, the smaller a the higher the resistance R.

ii) [5]



The IGBT differs from the DMOS in that the bottom contact is p-type. When the BJT is on the pn^- junction near the collector contact is forward biased (remember that the naming of the contacts in this structure is misleading and is only base on historical arguments). The forward bias will inject minority carriers in a lowly doped region, thus very soon this can be seen as high injection condition. In high injection condition the majority carrier concentration has to increase to compensate the large minority carrier concentration effectively reducing the resistance of the n^- layer. This is called conductivity modulation.