E3.11
AO8

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2005

MSc and EEE PART III/IV: MEng, BEng.and ACGI

ADVANCED ELECTRONIC DEVICES

Friday, 29 April 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer Question ONE and THREE other questions.

All questions carry equal marks.

Corrected Copy

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : K. Fobelets
Second Marker(s) : K.D. Leaver

1 **Compulsory.**

a) Given a heterojunction with materials M_1 and M_2 use the electron affinity rule to calculate the conduction and valence band offset at the junction. The electron affinities are: χ_{M1}=0.14eV and χ_{M2}= 0.5eV and energy band gaps: E_{gM1}=1.4eV and E_{gM2}=2eV. [2]

b) In GaAs the drift velocity of electrons decreases with increasing electric field beyond a certain field strength. Explain briefly, without calculations, how the energy bands in GaAs causes this. [2]

c) Regarding the value of the transconductance g_m, give one advantage and one disadvantage of using a buried channel in a FET (e.g. MODFET). [2]

d) Explain briefly why it is better to use a SIMOX or Bonded-Etch-Back substrate to fabricate a circuit based on fully depleted SOI MOSFETs. [2]

e) Explain briefly why decreasing the thickness of the gate oxide below 2nm, increases the gate leakage currents. [2]

f) Describe the influence, on the valence band, of compressive strain in SiGe on un-strained Si. Use a sketch of the valence band dispersion relation to support your argument. [2]

g) What difference is there between the materials used in a heterojunction bipolar transistor and a bipolar transistor? [2]

h) Explain why elevated source-drain technology is used? [2]

i) What are the advantages of a double gate MOSFET? Sketch the energy band diagram normal to the gates, midway between source and drain, to illustrate your answer. [2]

j) The term Drain Induced Barrier Lowering (DIBL) refers to which potential barrier in the MOSFET? [2]

2.

a) Which of the band alignments, shown in Figure 2.1, is needed to confine both electrons and holes in the same material? [2]

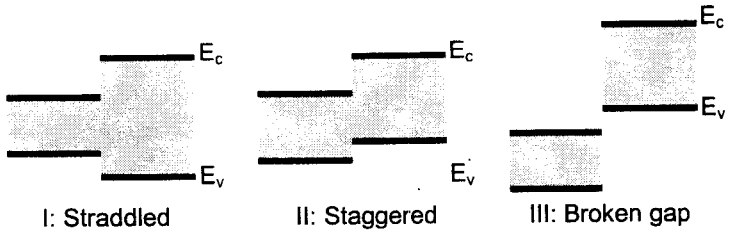


Figure 2.1: Heterojunction energy band diagram alignments

b) Name the scattering process that is severely reduced by the use of modulation doping in HEMTs. [2]

c) Schottky gating [8]

i) Draw the energy band diagrams of an un-biased GaAs MESFET and a GaAs/AlGaAs HEMT, both n-channel depletion-mode, from gate through the substrate. Label all energy bands and offsets.

ii) Give the condition, in terms of work function differences, for which the built-in voltage of the MESFET is approximately equal to that of the HEMT. Define the parameters in your answer to i) above.

d) Complementary GaAs/AlGaAs HEMT. [8]

i) Draw the labelled diagram of the layer structure of a p-channel HEMT.

ii) Draw the energy band diagram from gate into substrate of a p-HEMT when no bias is applied.

iii) Do you have a realistic suggestion of how to make a complementary-HEMT (C-HEMT) pair on a single GaAs substrate?

3

a) Give three implications for MOSFET performance of an increase in gate leakage. [3]

b) The subthreshold slope, S, of a MOSFET is given by the expression: [3]

$$S = \frac{kT}{q}\ln(10)\left(1+\frac{C_{depl}}{C_{ox}}\right)$$

How will the subthreshold slope change, if any change is to be expected, when the oxide thickness remains constant and the doping density in the substrate increases? Justify your answer.

c) Many short channel effects are a result of the high electric fields occurring at the drain end of the channel. Describe, with the help of a sketch, a processing method that reduces short channel effects associated with this feature. [4]

d) In long channel devices, the bulk depletion charge Q_B controlled by the gate is proportional to the gate length L. In short channel devices however the depletion widths due to the ohmic contacts give an important reduction of the remaining charge Q_B that is controlled by the gate. Using the trapezoid approximation, calculate the threshold voltage shift due to this charge sharing.

The gate length $L = 1\mu m$.
The encroached gate length is $L_B = 0.5\mu m$.
The p-type substrate doping density is 5×10^{16} cm^{-3}.
The oxide thickness is 10nm.
The expression for the one-side depletion width is: [10]

$$w_{depl} = \sqrt{\frac{4\varepsilon_0\varepsilon_r V_{bi}}{qN_A}}$$

$$V_{bi} = 0.026\ln\left(\frac{N_A}{n_i}\right)$$

Remember that the shift in threshold voltage is equal to the ratio of the loss of bulk charge over the oxide capacitance.
Constants:
$n_i=1.5\times10^{10}$ cm^{-3}.
$q=1.6\times10^{-16}$ C
$\varepsilon_0=8.85\times10^{-14}$ F/cm
$\varepsilon_{Si}=11.7$
$\varepsilon_{SiO2}=3.9$

4

a) Assume that the solutions to the Schrödinger equation in a heterojunction are given by the following equations.

$$\psi(x)=\begin{cases} E_{f_1}\exp(ik_1x)+E_{b_1}\exp(-ik_1x) & x\le x_1 \\ \alpha_1\exp(k_2x)+\beta_1\exp(-k_2x) & x_1\le x\le x_2 \\ E_{f_2}\exp(ik_1x)+E_{b_2}\exp(-ik_1x) & x_2\le x\le x_3 \\ \alpha_2\exp(k_2x)+\beta_2\exp(-k_2x) & x_3\le x\le x_4 \\ E_{f_3}\exp(ik_1x) & x_4\le x \end{cases}$$

With $k_1=\sqrt{\frac{2m_1E}{\hbar^2}}$ *and* $k_2=\sqrt{\frac{2m_2(V_0-E)}{\hbar^2}}$

i) Sketch the possible energy band diagram of the heterojunction that leads to the above wave equations in the different regions. Ensure that all materials in this structure are characterised by their effective mass. [3]

ii) Explain how the amplitudes of the forward and backward propagating waves can be calculated? (Do not do the calculations!) [3]

b) The three questions below concern the current-voltage relation in tunnel diodes

i) Give an expression, in terms of energy band parameters, for the bias voltage that gives the maximum current in an Esaki diode (this is a tunnel diode or a $p^{++}n^{++}$ junction). [3]

ii) Give an expression, in terms of energy band parameters, for the bias voltage that gives the maximum current in a resonant tunnelling diode (RTD). [3]

iii) Why does the current increase exponentially (at room temperature) at voltages higher than the valley voltage V_v (is the voltage at which the valley current appears) for both tunnelling diodes? [2]

c) The transfer matrix, T_{single}, of a single barrier heterostructure with a barrier width of 2nm and a barrier height of 0.3 eV for an electron with energy of 0.2 eV impinging on the barrier.

$$T_{\text{single}}=\begin{pmatrix} 0.63-j1.79 & -j1.6 \\ j1.6 & 0.63+j1.79 \end{pmatrix} \text{ where } j=\sqrt{-1}.$$

i) Calculate the amplitude of the transmitted wave under the assumption that the amplitude of the incoming wave is 1. [4]

ii) What is the amplitude of the transmitted wave for an incoming electron with an energy of 0.35eV? [2]

5

a) State which two leakage current paths in the MOSFET become more pronounced when scaling the MOSFET below 100nm, and explain briefly why. [4]

b) Describe the fabrication steps to produce a strained-Si layer on top of oxide (s-Si on SOI or s-SOI). Use sketches to clarify your explanation. [6]

c) Sketch the energy band diagram of the double gated FET, with cross section from gate to gate, midway between source and drain given in Figure 5.1, when no external bias is applied. The thickness of the undoped Si layer is W_{Si}=100nm, the thickness of the oxide layers is both t_{ox}=2nm. The workfunctions of the used materials are: ϕ_{Al}=4.4eV, ϕ_{Au}=5.1eV and ϕ_{Si}=4.9eV. The bandgap of Si is 1.12 eV. Make sure the relative energy differences in the band diagram are approximately correct. [6]

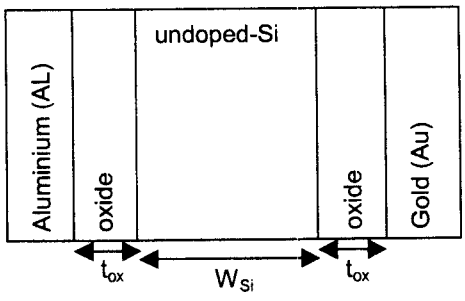


Figure 5.1: Cross section from gate to gate of a double gated FET midway between the source and the drain contact.

d) Is the double gated FET in Figure 5.1 a symmetric or asymmetric gating configuration? [2]

e) How many conducting channels will exist when a negative voltage is applied on the Al gate contact and no voltage on the gold gate contact with respect to the grounded source contact. [2]

6. Essay based on coursework research.

Describe, using diagrams as appropriate, the **finFET**. Make sure that the essay illustrates what a finFET is, why it is introduced and what its advantages and disadvantages are compared to bulk Si MOSFETs. Ensure your answer is concise (expected word count 150 – 200 words). [20]

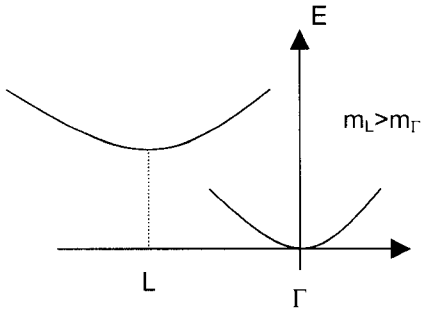
Solutions - 2005

Advanced Electronic Devices [E3.11]
A08

1. **Compulsary.**

a) $\Delta E_c = \chi_{M2} - \chi_{M2} = 0.5 - 0.14 = 0.36eV$
$\Delta E_v = \Delta E_g - \Delta E_c = 0.6 - 0.36 = 0.24eV$ [2]

b) The conduction band of GaAs shows two minima closely spaced (in energy),



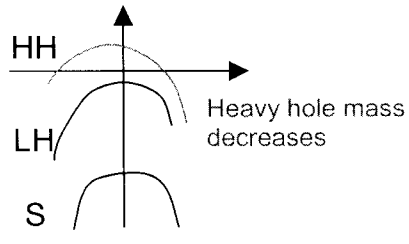
therefore when sufficient energy is available (at certain electric field) there is a transfer of electrons from the Γ minimum to the L minimum. As the effective mass in the L minimum is larger than in the Γ minimum, the average carrier velocity decreases with increasing field (with increasing relative amount of L electrons). [2]

c) Advantage: increases mobility as a result of decreased scattering. Disadvantage: channel is further removed from the gate electrode which reduces the control of the gate on the channel. [2]

d) SIMOX because FDSOI requires thin Si top layers with a well controlled thickness in order to ensure depletion of the Si without gate bias and constant threshold voltage across the wafer. [2]

e) The probability of tunnelling of charged carriers increases with thinning of potential barrier due to the oxide. [2]

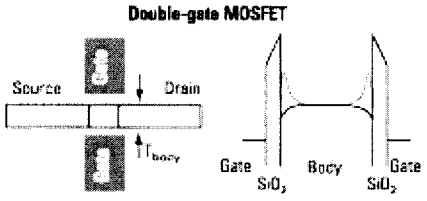
f) Compressive strain splits the degeneracy of the valence bands and pushes the heavy hole valence band to higher energies (this results in an increase in valence band offset). Compressive strain also changes the shape of the HH valence band and thus decreases the effective mass of the heavy holes. [2]



g) The HBT uses a wide bandgap material in the emitter. [2]

h) To reduce the source resistance. [2]

i) Dual gate MOSFETs are capable of driving higher currents with lower leakage when applied to SOI. Gating from both sides gives better control of the channel charges because the second gate electrostatically shields the influence of the drain on the source potential.. [2]



j) Source-channel potential at the source end of the channel. [2]

2. Heterojunctions - FET

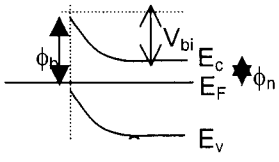
a) I: straddled. [2]

b) Impurity scattering. [2]

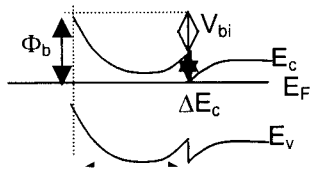
c) Schottky gating [8]

i)

MESFET



HEMT



ii)

$$V_{bi}^{MESFET} = \frac{1}{e}(\phi_b - \phi_n)$$

$$V_{bi}^{HEMT} = \frac{1}{e}(\Phi_b - \Delta E_c)$$

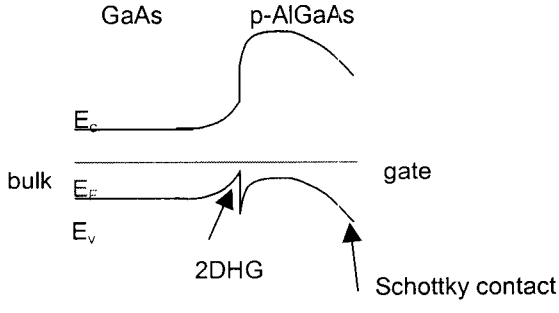
If the schottky barrier height is the same in both devices, the condition for equality of built-in voltage is: $\phi_n = \Delta E_c$

d) Complementary GaAs/AlGaAs HEMT. [8]

i)

p++ GaAs
p AlGaAs
undoped AlGaAs
undoped GaAs

ii)



iii) For instance, grow an undoped epitaxial layer as given below:

GaAs
AlGaAs
undoped AlGaAs
undoped GaAs

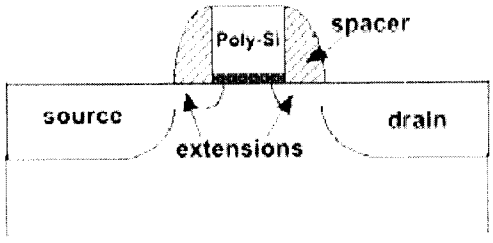
During processing the GaAs and the AlGaAs are doped (2 step doping: first doping into the AlGaAs then extra processing step with gate region covered to dope GaAs heavily for ohmic contacts). Regions for n-HEMT get n-type doping while regions for p-HEMT get p-type doping. Insulation between the two HEMTs is via mesa etch and oxide deposition.

3. Short channel Effects

a) Loss of channel control due to direct injection of carriers.
Increased power consumption
Increased heat dissipation [3]

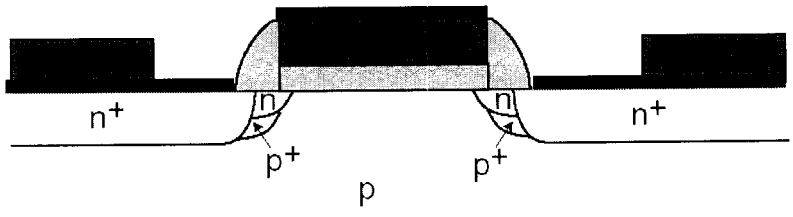
b) S will increase. When the doping density in the substrate increases, the depletion width into the bulk will decrease. The depletion capacitance is inversely proportional to the depletion width and thus C_{depl} increases. The ratio $\frac{C_{depl}}{C_{ox}}$ increases and thus S increases. [3]

c) All possible solutions are based on ion implantation at the drain-gate interface.
Possible solutions include:
LDD doping

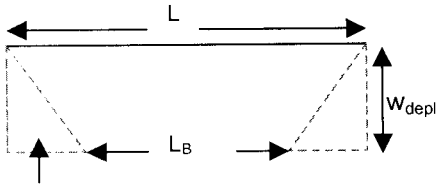


Extension implants

Pocket or halo implants



d)



Depleted bulk charges via the ohmic contacts rather than via the gate.

Trapezoid approximation of the reduction of the bulk charges available for control by the gate. The charge influenced by the source and drain contacts is given by the shaded triangle. The area of the trapezoid is:

The gate length L=1μm and the encroached gate length L_B=0.5μm. The p-type substrate doping is $5x10^{16}$ cm^{-3}. The oxide thickness is 10 nm.
The expression for the one-sided depletion width is:

$$A_{Trap.} = Lw_{depl} - 2\frac{\left(\frac{L-L_B}{2}w_{depl}\right)}{2} = \frac{L+L_B}{2}w_{depl}$$

The amount of charge in the long channel device can be approximated by:

$$Q_B^{long} = eN_A w_{depl} L$$

and in the short channel device:

$$Q_B^{short} = eN_A w_{depl}\frac{L+L_B}{2}$$

The loss of charge controlled by the gate due to the depletion by the contacts is:

$$\Delta Q_B = Q_B^{long} - Q_B^{short} = eN_A w_{depl}\frac{L-L_B}{2}$$

Calculation of depletion width:
Built-in voltage:

$$V_{bi} = 0.026\ln\left(\frac{N_A}{n_i}\right) = 0.026\ln\left(\frac{5x10^{16}}{1.5x10^{10}}\right) = 0.39V$$

Depletion width:

$$w_{depl} = \sqrt{\frac{4\varepsilon V_{bo}}{qN_A}} = \sqrt{\frac{4x11.7x8.85x10^{-14}x0.39}{1.6x10^{-19}x5x10^{14}}} = 0.000014cm = 0.14\mu m$$

Loss of charge:

$$\Delta Q_B = 1.6x10^{-19}x510^{16}x0.000014x\frac{0.5x10^{-4}}{2} = 2.84x10^{-12}C/cm^2$$

The threshold voltage shift is:

$$\Delta V_T = \frac{\Delta Q_B}{C_{ox}}$$

The oxide capacitance:

$$C_{ox} = \frac{\varepsilon_0\varepsilon_{ox}}{t_{ox}} = \frac{3.9x8.85x10^{-14}}{10x10^{-7}} = 3.45x10^{-7}F/cm^2$$

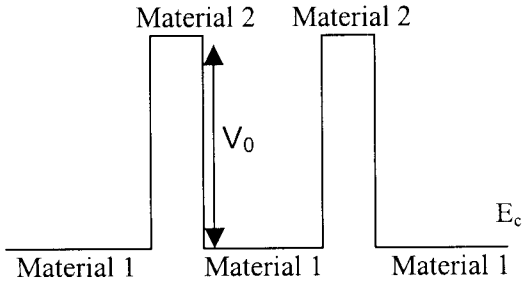
Thus

$$\Delta V_T = \frac{2.84x10^{-12}}{3.45x10^{-7}} = 8.23x10^{-6}V$$

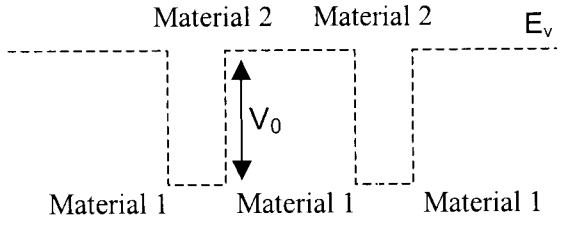
4. Tunnelling devices

a)

i) [3]



Note: material type and amplitude of the potential barrier can be derived from the expressions of the wavevector. The difference between potential barriers and otherwise can be derived from the exponentials in the solutions (real or imaginary)
Another acceptable solution is a QW in the valence band:



ii) By imposing the boundary conditions at each interface of the heterojunction. The boundary conditions are the continuity of the wavefunction and its first derivative (including 1/m*) at the interfaces. [3]

b)

i) $V_p=|1/q|\ (E_{cn}\ (V=0) - E_{vp}(V=0))$: the peak voltage is the forward bias voltage applied to align the bottom of the conduction band in the n-type region with the top of the valence band in the p-type region. [3]

ii) $V_p=|1/q|\ 2(V_0 - E_0)$: The peak voltage is the voltage applied to align the bottom of the conduction band in the input region to the first quasi bound energy level in the quantum well E_0. [3]

iii) Thermionic emission across the potential barrier. [2]

c)

i) The relationship between the transmission matrix and the wave amplitudes is:

$$\begin{pmatrix} t \\ 0 \end{pmatrix} = T_{\text{single}} \begin{pmatrix} 1 \\ r \end{pmatrix} = \begin{pmatrix} T^{(1,1)} & T^{(1,2)} \\ T^{(2,1)} & T^{(2,2)} \end{pmatrix} \begin{pmatrix} 1 \\ r \end{pmatrix} = \begin{pmatrix} T^{(1,1)} + rT^{(1,2)} \\ T^{(2,1)} + rT^{(2,2)} \end{pmatrix} \Rightarrow \begin{cases} t = \dfrac{T^{(1,1)}T^{(2,2)} - T^{(2,1)}T^{(1,2)}}{T^{(2,2)}} = \dfrac{1}{T^{(2,2)}} \\ r = -\dfrac{T^{(2,1)}}{T^{(2,2)}} \end{cases}$$

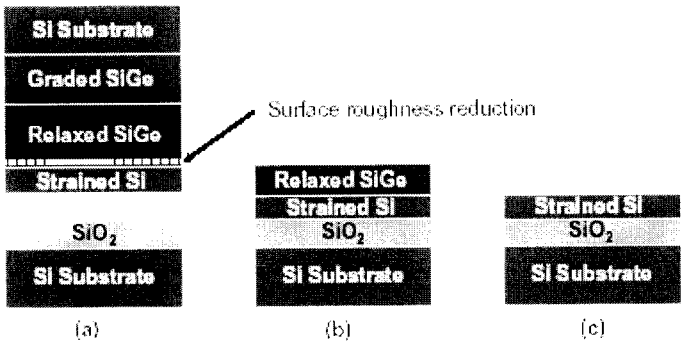
Thus the amplitude of the transmitted wave $t = \dfrac{1}{0.63 + 1.79I} = 0.17 - 0.5I$ [4]

ii) 1 – because it is a free electron as it travels above the barrier. [2]

5. SOI and Double gating

a) The off state leakage current increases because the threshold voltage (V_T) decreases and the sub-threshold current is proportional to the exponential of $-V_T$. V_T has to decrease as V_D has to decrease to keep the appropriate values of the electric field in the device.
The gate leakage currents increase because the thickness of the oxide decreases. For very thin gate oxides the leakage through the gate is determined by tunnelling processes. [4]

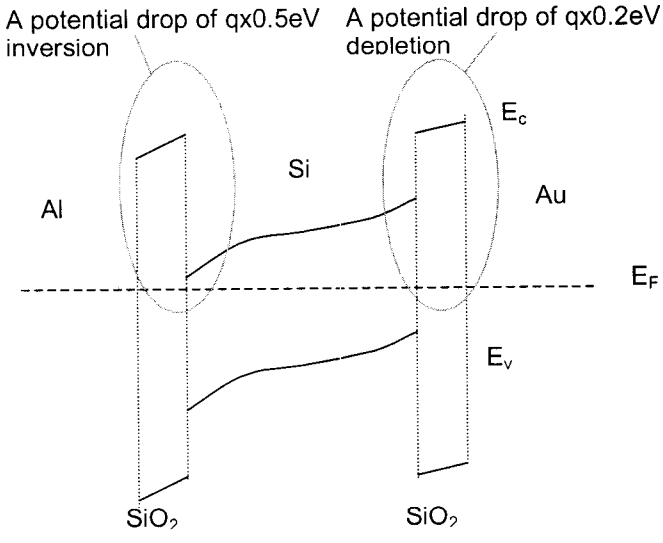
b) E.g. by Smart-cut: [6]



A Si wafer is oxidised creating a thick oxide: fig.(a) lower wafer. A strained-Si layer is grown by epitaxy on relaxed SiGe, grown on a virtual substrate (strain relaxation layer) grown on top of a Si substrate: fig (a) top wafer. The SiGe wafer is implanted with hydrogen with a peak concentration between the s-Si and the relaxed SiGe layer. Wafers are cleaned and then bonded together as in fig. (a). During the bonding process the thermal budget will cause the SiGe wafer to split from the Si/SiO_2 wafer where the peak of the H implant occurs: fig (b). The remaining SiGe layer is then removed by CMP, leaving fig. (c)

This is the best way, the way via the SIMOX on an VS wafer as given in fig. (a) top, is theoretically also possible, but very high thermal processes will need to be done while the s-Si is in place and the implant of oxygen will also go through the s-Si layer. This might cause severe strain relaxation effects in the s-Si device layer which is unwanted.

c) [6]



The potential barrier at the Al-Si interface has to be larger than at the Au-Si interface because the workfunction difference between Al and Si is larger than between Au and Si.

d) asymmetric gating configuration [2]

e) none [2]

6 Essay on finFET

Required is information on geometry, current direction and gating direction with respect to the surface of the SOI. Issues concerning the processing: CMOS compatible, all geometries are defined by lithography and etch. Advantages compared to planar MOSFETs: higher current drive because double channel, reduced DIBL because double gate configuration etc.