Part A: Answer any 2 questions out of 3 from this part

1. a) Explain why is it difficult to use LCC technology for realising a sub-sea DC grid such as the one envisaged in the North-sea.

[4]

- For a LCC HVDC link, voltage polarity reversal is necessary to change the direction power flow through the link. While this is not an issue for a point-to-point HVDC link, it poses a problem for meshed DC grids where voltage polarity reversal affects the power flow in all the DC lines connected to a particular converter station which might not be desirable. Power flow direction is meshed grids should be changeable through current flow direction (like in AC systems) which is not possible with LCC.

- For sub-sea DC grids, use of stronger and lighter polymeric cables offers significant advantages. However, such polymeric cables cannot be used for LCC HVDC due to the need for voltage reversal to change the power flow direction.

[2 marks for each point]

b) The DC circuit breakers are not necessary to protect a LCC HVDC link against DC-side faults. Justify or rectify this statement describing the steps for DC fault current limiting and interruption.

[5]

Following a fault on a LCC HVDC link, the rectifier current increases and the inverter current decreases. Current control at the rectifier restores direct current back to normal. The inverter switches from constant extinction angle control to current control to hold the decreasing current. Rectifier tries to maintain I_{ord} and inverter $I_{ord} - I_m$ resulting in the fault current being limited to only margin current I_m which is typically 10-15% of the rated current.

Such faults on the DC link are detected by collapse of DC voltage and decrease in inverter current. After the fault current is limited to the margin current, the rectifier is driven to inversion keeping the inverter as it is. Current attempts to reverse but it cannot because of valves and is rapidly (10 ms) reduced to zero.

Therefore, DC fault current in a LCC HVDC link can be limited and interrupted using converter control without requiring DC circuit breakers.

[2 marks each for the steps for fault current limiting and interruption and 1 mark for overall argument]

c) A standard six-pulse converter bridge is operating with a commutation overlap angle (μ) less than 60°. Answer the following assuming the thyristor valves to be ideal:

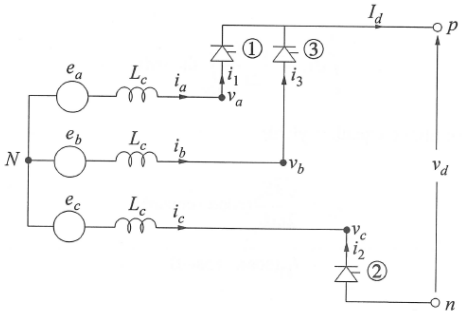
i) Considering commutation of current from phase 'a' (valve 1) to phase 'b' (valve 3), show that the voltage of the positive pole is the average of the voltages of the overlapping phases 'a' and 'b'.

[4]

$$e_b - e_a = L_c \frac{di_3}{dt} - L_c \frac{di_i}{dt}$$

$$i_1 = I_d - i_3 \Rightarrow \frac{di_i}{dt} = 0 - \frac{di_3}{dt}$$

$$e_b - e_a = 2L_c \frac{di_3}{dt} \Rightarrow L_c \frac{di_3}{dt} = \frac{e_b - e_a}{2}$$



Voltage of the positive pole is

$$v_a = v_b = e_b - L_c \frac{di_3}{dt} = \frac{e_b + e_a}{2}$$

[1 mark for each step]

ii) Using the result in part (i) derive an expression for the average reduction in direct voltage due to the commutation overlap in terms of the AC-side voltage, the firing delay (α) and the overlap angle (μ).

[4]

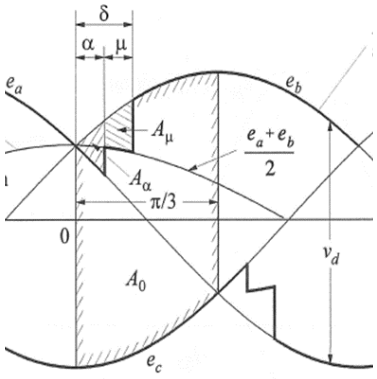
The reduction in voltage due to commutation overlap is indicated by the shaded area A_μ

$$A_\mu = \int_\alpha^{\alpha+\mu} \left[e_b - \frac{e_b + e_a}{2}\right] d\theta$$

$$= \int_\alpha^{\alpha+\mu} \left[\frac{e_b - e_a}{2}\right] d\theta$$

$$= \frac{\sqrt{3}E_m}{2} \int_\alpha^{\alpha+\mu} \sin\theta \, d\theta$$

$$= \frac{\sqrt{3}E_m}{2} [\cos\alpha - \cos(\alpha + \mu)]$$



Average reduction in direct voltage due to commutation overlap is given by:

$$\Delta V_d = \frac{A_\mu}{\pi/3} = \frac{3\sqrt{3}E_m}{2\pi} [\cos\alpha - \cos(\alpha + \mu)]$$

[3 marks for correct derivation of A_μ and 1 mark for average voltage reduction]

d) Explain why a bipole LCC HVDC link can transmit the same amount of power as an equivalent three-phase AC transmission line using identical conductors and insulators.

[3]

Ratio of total power transfer for three-phase AC and bipole DC option is:

$$\frac{P_{AC}}{P_{DC}} = \frac{3\,V_{LN} I_{AC} \cos\phi}{2\,V_{DC} I_{DC}}$$

Identical conductor rating for AC and DC option implies:
$I_{AC} = I_{DC}$

Identical insulator rating for AC and DC option implies:
$\sqrt{2} V_{LN} = V_{DC}$

Hence assuming power factor $\cos\varphi$ = 0.9-0.95

$$\frac{P_{AC}}{P_{DC}} = \frac{3\,V_{LN} I_{AC} \cos\phi}{2\sqrt{2} V_{LN} I_{AC}} \approx 1$$

[1 mark for each step]

2. a) Explain why 'strong' AC systems are necessary at both ends of a LCC HVDC link for reliable operation.

[5]

An AC system at a given location (bus/node) is referred to as 'strong' if the short circuit level at that point is high i.e. the Thevenin equivalent impedance is low. A strong system is therefore, capable of maintaining a stiff (well regulated) line voltage profile which is necessary for commutation of current from one valve to another in a line commutated converter (LCC). For weak systems, voltages could be unacceptably low for satisfactory commutation which could result in frequent commutation failure at the inverter end.

The reactive power consumption of the LCCs increases at high power transfers. If the capacitor/filter banks at the converter station are not capable of meeting the high reactive power demand of the LCC, reactive power has to be transmitted from remote locations which reduces the voltage at the converter station. This in turn reduces the reactive power generation from the capacitor/filter banks leading to a runaway situation unless the power transfer is reduced. For strong systems, the extent of reduction of voltage at the converter station is much less than a weak system where such runaway situations or part loaded operation (disruption) are more likely.

[1 mark for charactersing strong system, 2 marks for relating strength to commutation problems, 2 marks for discussing the runaway situation]

b) A monopole LCC HVDC link with six-pulse converters interconnects two separate 400 kV AC systems. The resistance of the DC transmission line is 1.5 Ω. The rectifier end of the link is set to maintain the direct current at 2 kA until the minimum firing angle limit (α_{min}) of 5° is violated. The inverter end is operating with a fixed extinction angle (γ) of 18°. The commutating resistance at either end is 3.0 Ω. The margin current is 15% of the rated current. Calculate the reactive power drawn by the rectifier under the following conditions. Neglect commutation failure, tap changer action, effect of voltage dependent current order limit (VDCOL) and any upper limit on firing angle (α).

i) when rated AC system voltage is maintained at the converter stations at both ends.

[5]

Inverter end:

$$V_{doi} = \frac{3\sqrt{2}}{\pi} E_{LLi} = 540.19 \text{ kV}$$

$$V_{di} = V_{doi} \cos\gamma - R_c I_d = 507.75 \text{ kV}$$

Rectifier end:

$$V_{dr} = V_{di} + R_L I_d = 510.75 \text{ kV}$$

$$V_{dor} = \frac{3\sqrt{2}}{\pi} E_{LLr} = 540.19 \text{ kV}$$

$$\cos \emptyset_r = \frac{V_{dr}}{V_{dor}} = 0.9455$$

$$Q_r = V_{dr} I_d \tan \emptyset_r = 351.79 \text{ MVAr}$$

[1 mark for each step]

ii) when the rectifier side AC system voltage drops by 20% of the rated value. [6]

$$V'_{dor} = 0.8 \times V_{dor} = 432.15 \text{ kV}$$

$$\cos \alpha' = \frac{V_{dr} + R_{cr} I_d}{V'_{dor}} > 1$$

Hence current control is transferred to inverter while the rectifier goes into constant firing angle (α_{min}) mode.

New current order for the inverter is
$I'_d = I_d - I_m = 1.7 \text{ kA}$

$$V'_{dr} = V'_{dor} \cos \alpha_{min} - R_{cr} I'_d = 425.41 \text{ kV}$$

Power factor at the rectifier end is

$$cos \emptyset_r = \frac{V'_{dr}}{V'_{dor}} = 0.9844$$

Reactive power consumption at the rectifier end is
$Q_r = V'_{dr} I'_d \tan \emptyset_r = 129.29 \text{ MVAr}$

[1 mark for each step]

iii) when the inverter side AC system voltage drops by 10% of the rated value resulting in an increase of extinction angle (γ) to 25° to prevent commutation failure while maintaining the rated direct current flow. [4]

$$V_{doi}'' = 0.9 \times V_{doi} = 486.17 \text{ kV}$$

The rectifier end is able to maintain the DC link current at 2.0 kA

$$V_{di}'' = V_{doi}'' \cos \gamma'' - R_c I_d = 434.62 \text{ kV}$$

$$V_{dr}'' = V_{di}'' + R_L I_d = 437.62 \text{ kV}$$

$$\cos\alpha'' = \frac{V_{dr}'' + R_c I_d}{V_{dor}} \Longrightarrow \alpha'' = 40.3°$$

$$\cos\emptyset_r'' = \frac{V_{dr}''}{V_{dor}} = 0.81$$

$$Q_r'' = V_{dr}'' I_d \tan\emptyset_r'' = 633.38 \text{ MVAr}$$

[1 mark for each step]

3. a) The control characteristics of the rectifier and inverter of a LCC HVDC link is shown in Figure 3.1 in terms of the direct current (I_d) and DC voltage at the rectifier end (V_{dr}). The commutation resistance at each end in R_c. The DC line resistance is R_L. At both ends, a proportional controller with gain K_p is used to maintain the respective current order. Identify the segments of the control characteristics corresponding to the following control modes and derive an expression for the slope of each segment in terms R_c, R_L and K_p. Comment on the nature of the slope in each case considering $K_p >> R_c > R_L$

i) Rectifier in current control mode. [3]

Segment 'BC'

$V_{dor}\cos\alpha = K_p\,(I_{ord} - I_d)$
$V_{dr} = V_{dor}\cos\alpha - R_c I_d = K_p I_{ord} - (K_p + R_c)I_d$

Slope of segment 'BC' is
$m_{\text{BC}} = \left.\frac{\Delta V_{dr}}{I_d}\right|_{BC} = -(K_p + R_c)$
The slope is negative and large.

[0.5 mark for correct segment, 2 marks for expression of slope, 0.5 mark for commenting on the nature of the slope]

ii) Inverter in constant extinction angle control mode. [3]

Segment 'DE'

$V_{dr} = V_{doi}\cos\gamma - (R_c - R_L)I_d$

Slope of segment 'DE' is
$m_{\text{DE}} = \left.\frac{\Delta V_{dr}}{I_d}\right|_{DE} = -(R_c - R_L)$
As $R_c > R_L$ the slope is slightly negative

[0.5 mark for correct segment, 2 marks for expression of slope, 0.5 mark for commenting on the nature of the slope]

iii) Rectifier operating at minimum firing angle (α). [3]

Segment 'AB'
$V_{dr} = V_{dor}\cos\alpha_{\min} - R_c I_d$

Slope of segment 'AB' is

$m_{\text{AB}} = \left.\frac{\Delta V_{dr}}{I_d}\right|_{AB} = -R_c$ i.e. slightly negative

[0.5 mark for correct segment, 2 marks for expression of slope, 0.5 mark for commenting on the nature of the slope]

iv) Inverter in current control mode.

[3]

Segment 'EF'

$V_{doi}\cos\gamma = K_p\,(I_{ord} - I_m - I_d)$

$V_{di} = -K_p(I_{ord} - I_m) + (K_p - R_c + R_L)I_d$

Slope of segment 'EF' is

$m_{\text{EF}} = \left.\frac{\Delta V_{dr}}{I_d}\right|_{EF} == (K_P - R_c + R_L)$

As $K_P \gg R_c > R_L$, the slope is positive and large

[0.5 mark for correct segment, 2 marks for expression of slope, 0.5 mark for commenting on the nature of the slope]

b) What is the role of bridge control and pole control within a converter station of a LCC HVDC link?

[4]

- Bridge control determines the firing instants of the valves within limits for a bridge and takes care of protection (e.g. commutation failure protection).
- Pole control coordinates control of bridges in a pole and provides firing angle orders to individual converters.

[2 marks for each point]

c) Explain why only the inverter end and not the rectifier end of a LCC HVDC link is generally susceptible to commutation failure and spurious turn on of valves due to accidental release of firing pulses.

[4]

- Commutation failure
  Commutation failure is the failure to complete commutation of current from one switch to the next one before reversal of commutating (line) voltage. At high currents and low voltages or low extinction advance angles, the outgoing switch might fail to turn off before the commutating voltage reverses in which case the current in the incoming valve would go down

to zero. This is not a problem at the rectifier end as much longer margin is available for the commutation of current before reversal of the commutating voltage. However, at the inverter, the firing takes place closer to negative zero crossing wherein the margin to complete the commutation process is relatively less making it susceptible to commutation failure.

- Spurious turn-on of valves
  Voltages across the valves are mostly negative (reverse bias) for rectifier operation while those are mostly positive (forward bias) for inverter operation. So the valves in the inverters are more susceptible to spurious turn-on if a firing signal is released accidentally.

[2 marks for each point]

Part B: Answer any 2 questions out of 3 from this part

In all the following questions, use the symbols, current and voltage directions as presented in Figure 1.

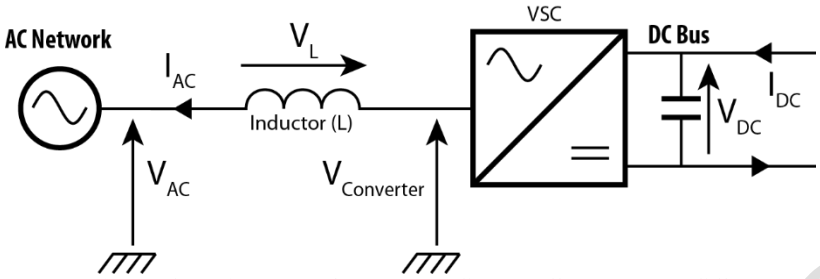


Figure 1 – Diagram of a Voltage Source Converter (VSC)

4. a) What are the properties of VSCs?

[3]

Some of the properties of VSCs are:

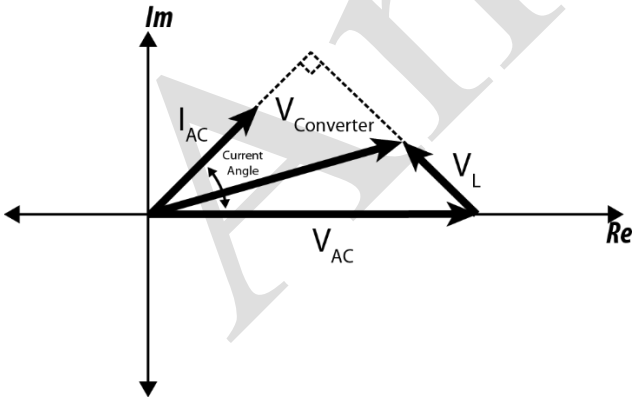
- Uses self-commutated IGBT switches
- Independent control of active and reactive power
- Lower filtering requirement
- Lower footprint compared to LCC
- No dependence on AC system strength
- No DC voltage reversal – stronger and lighter cables, meshing

[KEYWORDS]: IGBT, P-Q control, small filters, smaller footprint, constant DC voltage, can power weak AC grids

[0.5 point per keyword]

b) Use a phasor diagram and equation to explain the relationship between the AC grid and converter voltages?

[2]



$$\bar{V}_{AC} + j\omega L\, \bar{I}_{AC} = \bar{V}_{Converter}$$

[1 point for the correct diagram and 1 point for the equation]

c) What is the purpose of zero-sequence voltage injection in VSCs?

[3]

The basic principles of VSC is to generate an AC voltage waveform on one side of the AC phase reactor. Since the higher its voltage magnitude, the lower the current magnitude, hence lower power losses, there is an incentive to push the AC converter voltage higher. However, the peak voltage is often capped to the DC

terminal voltage (i.e. VDC/2). One way to artificially push the RMS value of the fundamental component of the converter voltage waveform up without pushing its peak voltage involves the injection a zero-sequence voltage (ZSV) in addition to normal sinewave. One basic technique for this ZSV technique consists in using the third harmonic at 1/6 of the fundamental magnitude. Doing so reduces the peak value by √3/2, or inversely to push the fundamental by a factor 2/√3≈1.155, thus 15% above the DC terminal voltage.

[KEYWORDS]: converter voltage constraints, zero-sequence voltage boost voltage, 15% gain
[1 point per keyword]

d) In the case of a VSC with the following characteristics: ±320kV DC bus voltage, 370kV AC voltage at 50Hz, simple sinusoidal modulation (i.e. no zero-phase sequence voltage injection), calculate the following constraints:

i) Maximum capacitive reactive power when the phase reactor is equal to 150mH? [3]

$$\bar{S} = 3\frac{|V_{AC}|^2 - V_{AC}V^*_{converter}}{jL\omega} = 0 + j\,Q$$

$$Q_{Max} = 3\frac{\frac{-|V_{Line}|^2}{3} + \frac{V_{Line}}{\sqrt{3}}|V^{Max}_{Converter}|}{L\omega} = 3\frac{-\frac{370kV^2}{3} + \frac{370kV}{\sqrt{3}}\frac{320kV}{\sqrt{2}}}{150mH\ 2\pi\ 50Hz} = 172\ MVAr$$

[2 for the correct equation, 1 point for the correct answer]

ii) Largest possible phase reactor if 350MVAr of capacitive reactive power is requested? [3]

$$L = 3\frac{\frac{-|V_{Line}|^2}{3} + \frac{V_{Line}}{\sqrt{3}}|V^{Max}_{Converter}|}{Q\omega} = 3\frac{-\frac{370kV^2}{3} + \frac{370kV}{\sqrt{3}}\frac{320kV}{\sqrt{2}}}{400MVAr\ 2\pi\ 50Hz} = 74\ mH$$

[2 for the correct equation, 1 point for the correct answer]

e) For an IGBT with 1.0V initial on-state voltage and 0.6mΩ internal resistance, what are its conduction power losses when conducting the following current waveforms:

i) $I(t) = 1000\,sin\left(2\pi 50\,t + \frac{2\pi}{3}\right) + 600$ [3]

$$P_{conduction} = E_{OS}\,|I|_{average} + R_{IGBT}\,I^2_{RMS}$$

$$|I|_{average} \approx 755A$$

$$I_{RMS} = \sqrt{\frac{1000^2}{2} + 600^2} \approx 927A$$

$$P_{conduction} = 1.0\times 1237 + 0.0006\times 927^2 = 1.271kW$$

[2 for the correct equation, 1 point for the correct answer]

ii) $I(t) = \left|500\, sin\left(2\pi 250\, t - \frac{\pi}{2}\right)\right|$ [3]

$$P_{conduction} = E_{OS}\, |I|_{average} + R_{IGBT}\, I_{RMS}^2$$

$$|I|_{average} = \frac{2}{\pi} 500 \approx 318A$$

$$I_{RMS} = \frac{500}{\sqrt{2}} \approx 354A$$

$$P_{conduction} = 1.0 \times 318 + 0.0006 \times 354^2 = 393W$$

[2 for the correct equation, 1 point for the correct answer]

In all the following question, use the symbols, current and voltage directions as presented in Figure 2. The hybrid MMC has part of its stacks consisting of half-bridge submodules (N_{HB}) and full-bridge submodules (N_{FB}). The total number of submodules per stack is $N_{SM} = N_{HB} + N_{FB}$. Please use the same current convention in your answers.

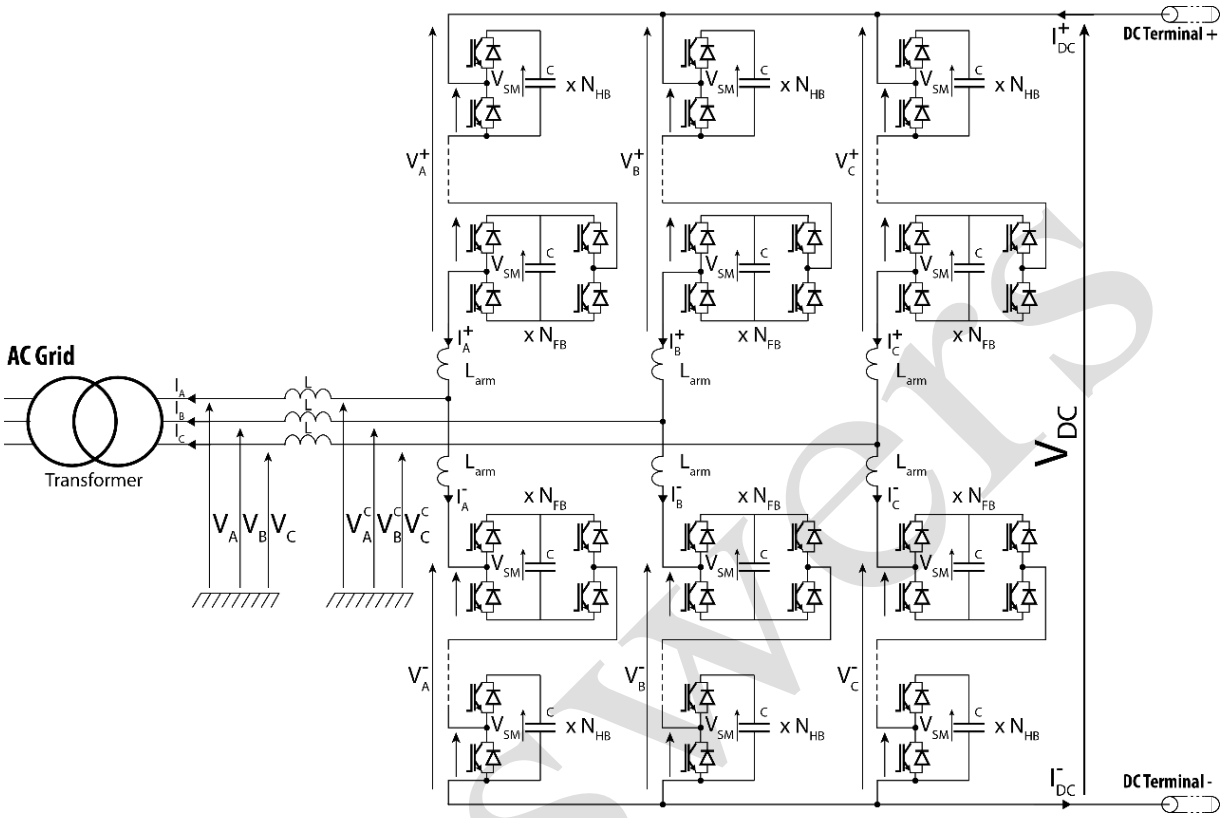


Figure 2 – Electrical diagram of a hybrid MMC

5. a) For a 600 MVA MMC connected to a ±250kV DC bus, calculate the nominal AC line voltage and nominal RMS current magnitudes for the following modulation indexes:

i) 80%?
ii) 100%?
iii) 120%?

[2]

$$\hat{V}_{AC} = m\frac{V_{DC}}{2} \leftrightarrow V_{line} = m\sqrt{\frac{3}{2}}\frac{V_{DC}}{2}$$

$$I_{AC}^{RMS} = \frac{S}{\sqrt{3}V_{line}}$$

m	V_{line}	I_{AC}^{RMS}
80%	245 kV	1.414 kA
100%	306 kV	1.132 kA
120%	367 kV	0.944 kA

[1 point if all voltages right, 1 point if all currents are right, -1 to the total if phase voltage instead of line voltage or peak current instead of RMS]

b) For each of the modulation indexes above, calculate the required number of half-bridge and full-bridge SMs per stack, each rated at 3 kV. Ignore the voltage drops across the inductors and assume constant SM voltage (i.e. infinite SM capacitance). Also include the resulting number of semiconductor devices in the conduction path:

i) Without DC fault blocking?

[5]

During normal operation, the stacks in an MMC must generate voltage levels within this range:

$$V_{Stack}^{Normal} = \frac{V_{DC}}{2} \pm \hat{V}_{AC} \in \frac{V_{DC}}{2}[1-m \quad 1+m]$$

Ignoring SM voltage fluctuations, the ideal mix of HB- and FB-SMs are:

$$N_{FB} = -\frac{V_{DC}}{2}\frac{1-m}{V_{SM}} \; (if\ m > 100\%, otherwise\ 0)$$

$$N_{HB} = \frac{V_{DC}}{2}\frac{1+m}{V_{SM}} - N_{FB}$$

$$N_{Conduction} = 1{\times}N_{HB} + 2{\times}N_{FB}$$

m	N_{FB}	N_{HB}	$N_{Conduction}$ (per stack)
80%	0	150	150
100%	0	167	167
120%	17	167	201

[2 points for the methodology, 1 point per correct answer]

ii) This Time when DC fault blocking is required?

[5]

To offer DC-side fault blocking, the MMC stacks must be able to match the AC grid voltage without the support of the DC bus voltage. This leads to the following voltage generation range under DC-side faults:

$$V_{Stack}^{Fault} = \pm\hat{V}_{AC} \in \frac{V_{DC}}{2}\{-m \quad m\}$$

This must be combined with the normal operation range detailed above, leading to a new voltage level generation requirement for the MMC stacks.

$$V_{Stack}^{Blocking} \in V_{Stack}^{Fault}\ and\ V_{Stack}^{Normal} \in \frac{V_{DC}}{2}\{-m \quad 1+m\}$$

The number of FB and HB SMs is done similarly to the non-fault blocking case.

m	N_{FB}	N_{HB}	$N_{Conduction}$ (per stack)
80%	67	83	217
100%	84	83	251
120%	100	84	284

[2 points for the methodology, 1 point per correct answer]

c) An MMC is inverting power, resulting in 707A RMS AC currents (no reactive power) being pushed to the AC grid and 1500A DC current pulled from the DC grid:

i) Write all the six arm current equations based on these AC and DC grid currents.

[2]

$$I_A^+(t) = \frac{I_A(t)}{2} + \frac{I_{DC}}{3} = 500\cos(\omega t) + 500$$
$$I_A^-(t) = -\frac{I_A(t)}{2} + \frac{I_{DC}}{3} = -500\cos(\omega t) + 500$$
$$I_B^+(t) = \frac{I_B(t)}{2} + \frac{I_{DC}}{3} = 500\cos\left(\omega t - \frac{2\pi}{3}\right) + 500$$
$$I_B^-(t) = -\frac{I_B(t)}{2} + \frac{I_{DC}}{3} = -500\cos\left(\omega t - \frac{2\pi}{3}\right) + 500$$
$$I_C^+(t) = \frac{I_C(t)}{2} + \frac{I_{DC}}{3} = 500\cos\left(\omega t + \frac{2\pi}{3}\right) + 500$$
$$I_C^-(t) = -\frac{I_C(t)}{2} + \frac{I_{DC}}{3} = -500\cos\left(\omega t + \frac{2\pi}{3}\right) + 500$$

[1 point per correct triplet of arm currents]

ii) To balance its submodule capacitors, the energy management of this MMC asks for the following balancing currents:

- Horizontal balancing current in Phase A: 100A
- Horizontal balancing current in Phase B: 200A
- Horizontal balancing current in Phase A: -300A
- Vertical balancing current (RMS) for Phase A only: 354A
- Vertical balancing current (RMS) for Phase B only: 0A
- Vertical balancing current (RMS) for Phase C only: 0A

Calculate the final vertical balancing current equations for each phase to keep the DC current free from any AC components.

[4]

$$I_A^V = I_A^a + I_A^b + I_A^c = 354\sqrt{2}\cos(\omega t) + 0 + 0, \left(354\sqrt{2} \approx 500\right)$$
$$I_B^V = I_B^a + I_B^b + I_B^c = 0 + 354\frac{\sqrt{2}}{\sqrt{3}}\cos\left(\omega t + \frac{5\pi}{6}\right) + 0, \left(354\frac{\sqrt{2}}{\sqrt{3}} \approx 289\right)$$
$$I_C^V = I_C^a + I_C^b + I_C^c = 0 + 0 + 354\frac{\sqrt{2}}{\sqrt{3}}\cos\left(\omega t + \frac{7\pi}{6}\right)$$

[1 point per correct equation]

iii) Write the new equations for all six arm current equations using both the AC, DC and balancing currents.

[2]

$$I_A^+(t) = \frac{I_A(t)}{2} + \frac{I_{DC}}{3} + I_A^H + I_A^V = 1000\cos(\omega t) + 600$$

$$I_A^-(t) = -\frac{I_A(t)}{2} + \frac{I_{DC}}{3} + I_A^H + I_A^V = 0\cos(\omega t) + 600, no\ AC!$$

$$I_B^+(t) = \frac{I_B(t)}{2} + \frac{I_{DC}}{3} + I_B^H + I_B^V = 577\cos\left(\omega t - \frac{5\pi}{6}\right) + 700$$

$$I_B^-(t) = -\frac{I_B(t)}{2} + \frac{I_{DC}}{3} + I_B^H + I_B^V = -577\cos\left(\omega t - \frac{\pi}{2}\right) + 700$$

$$I_C^+(t) = \frac{I_C(t)}{2} + \frac{I_{DC}}{3} + I_C^H + I_C^V = 577\cos\left(\omega t + \frac{5\pi}{6}\right) + 200$$

$$I_C^-(t) = -\frac{I_C(t)}{2} + \frac{I_{DC}}{3} + I_C^H + I_C^V = -577\cos\left(\omega t + \frac{\pi}{2}\right) + 200$$

[1 for the right general equations, 1 for the final equations]

In all the following questions, use the symbols, current and voltage directions as presented in Figure 3.

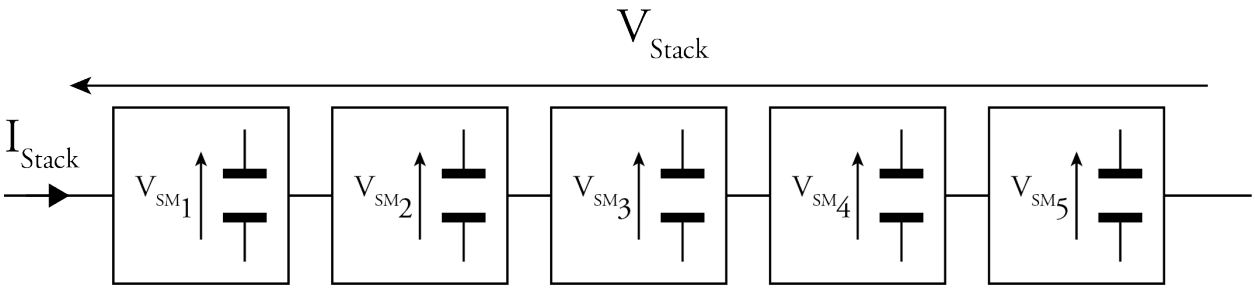


Figure 3 – Stack of submodules with pre-charged capacitors

6. a) Explain the working principles of a stack of submodules, including the operating conditions for stable operation.

[3]

Each submodule can generate a zero, positive or sometimes negative voltage level. When many of these submodules are connected in series, they form a stack which can generate complex voltage waveforms composed of numerous small steps. Since the submodules rely on their charged capacitors to provide the voltage levels, the stack of submodules must operate at a zero-average power condition. Otherwise the capacitor voltages will start drifting, leading to either loss of control or deterioration.

[KEYWORDS]: voltage level generation, zero average power, voltage drift otherwise

[1 point per concept properly explained]

b) A stack of submodules generates a voltage waveform of the following equation:

$$V_{Stack}(t) = 600\sin(\omega t) - 100\sin(3\omega t) + 500$$

For each of the current waveform equations below, state whether the stack will operate stably or not. Provide proof to your answers.

i) $I_{Stack}(t) = 10\sin(\omega t) - 6$

ii) $I_{Stack}(t) = 30\sin(\omega t) - 15$

iii) $I_{Stack}(t) = 30\sin\left(\omega t + \frac{\pi}{2}\right)$

iv) $I_{Stack}(t) = 20\sin(\omega t) + 30\sin(3\omega t) - 9$

v) $I_{Stack}(t) = 5\sin(\omega t) + 10\sin(\omega t) - 2$

[5]

$$P_{AC1} = \frac{\hat{V}_{AC}\hat{I}_{AC}}{2}\cos(\varphi_{AC})$$

$$P_{AC3} = \frac{\hat{V}_3\hat{I}_3}{2}\cos(\varphi_3)$$

$$P_{DC} = V_{DC}I_{DC}$$

$$P_{Stack} = P_{AC1} + P_{AC3} + P_{DC} = 0 \ (to\ ensure\ stable\ operation)$$

	P_{AC}	P_3	P_{DC}	P_{Stack}
i)	3,000 W	0 W	-3,000 W	0 W → Stable
ii)	9,000 W	0 W	-7,500 W	1.5 kW → Unstable
iii)	0 W	0 W	0 W	0 W → Stable
iv)	6,000 W	1,500 W	-4,500 W	0 W → Stable
v)	1,500 W	500 W	-1,000 W	1.0 kW → Unstable

[1 point (or 0.5 if no proof) per correct answer]

c) The operational study of a stack of N_{SM} submodules equipped with a capacitor C_{SM} at the nominal voltage V_{SM} is necessary for the estimation of its maximum ($\widehat{\Delta E}$) and minimum ($\widecheck{\Delta E}$) energy deviations, assuming a maximum submodule voltage deviation of $\pm\Delta V$. Calculate the missing parameters in each case below:

i) Number of submodules,
when $C_{SM} = 1mF, V_{SM} = 3kV, \widehat{\Delta E} = 20kJ, \widecheck{\Delta E} = -5kJ, \Delta V = 10\%$

ii) submodule capacitance,
when $N_{SM} = 20, V_{SM} = 1kV, \widehat{\Delta E} = 15kJ, \widecheck{\Delta E} = -10kJ, \Delta V = 10\%$

iii) Nominal submodule voltage,
when $N_{SM} = 18,\ C_{SM} = 5mF, \widehat{\Delta E} = 5kJ, \widecheck{\Delta E} = -25kJ, \Delta V = 5\%$

iv) Peak-to-peak energy deviation of the stack,
when $N_{SM} = 16,\ C_{SM} = 3.3mF, V_{SM} = 2kV, \Delta V = 5\%$

v) Desired submodule voltage deviation,
when $N_{SM} = 8,\ C_{SM} = 2mF, V_{SM} = 10kV, \widehat{\Delta E} = 50kJ, \widecheck{\Delta E} = -60kJ$

[5]

$$E_{Stack}^{Nominal} = \frac{N_{SM} C_{SM}}{2} V_{SM}^2 = \frac{\widehat{\Delta E} - \widecheck{\Delta E}}{4\,\Delta V} = \frac{\Delta E}{4\,\Delta V}$$

i) $N_{SM} = 14$
ii) $C_{SM} = 6.25mF$
iii) $V_{SM} = 1.825\ kV$
iv) $\Delta E = 21.12\ kJ$
v) $\Delta V = 3.4\%$

[1 point per correct answer]

e) Explain the concept of submodule rotation.

[3]

During the normal operation of a stack of submodules, the conduction of current could displace the charges between the submodule capacitors. To keep an equal voltage distribution between the submodules, a rotation algorithm is used. Its operation consists in controlling the prioritization of the submodule switching instances in order to correct any discrepancies. The prioritization uses the stack voltage command and current signs to determine which submodules should be used first and which to be used last, all depending on their relative level of charge.

[KEYWORDS]: submodule voltage distribution, switching control, use voltage and current signs
[1 point per concept properly explained]

f) Using the representation of a 5-submodule stack in Figure 3 where each submodule is of a full-bridge type, the measured level of charge of the submodule capacitors is:
$V_{SM1} = 1.5kV, V_{SM2} = 1.4kV, V_{SM3} = 1.6kV, V_{SM4} = 1.7kV, V_{SM5} = 1.3kV$.
Indicate the switching state (zero, positive or negative state) of each submodule computed by a rotation algorithm for a certain stack voltage command (choose the solutions which minimize the number of capacitors in the conduction path).

i) The stack voltage command is +4.5kV and the stack current is positive
ii) The stack voltage command is -1.5kV and the stack current is positive

iii) The stack voltage command is +3.0kV and the stack current is negative
iv) The stack voltage command is -6.0kV and the stack current is negative

[4]

For positive stack voltage command and positive current, the lowest submodules are prioritized. This logic is inverted for any changes of voltage or current signs.

Case	***SM 1***	***SM 2***	***SM 3***	***SM 4***	***SM 5***
i)	*Positive*	*Positive*	Zero	Zero	*Positive*
ii)	Zero	Zero	Zero	*Negative*	Zero
iii)	Zero	Zero	*Positive*	*Positive*	Zero
iv)	*Negative*	*Negative*	*Negative*	Zero	*Negative*

[1 point per correct line]