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AC1

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2008

MSc and EEE PART III/IV: MEng, BEng.and ACGI

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Thursday, 8 May 10:00 am

Time allowed: 3:00 hours

Corrected Copy

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : C. Toumazou
Second Marker(s) : D.G. Haigh

1. (a) Figures 1(a) and 1(b) show two popular biasing schemes typically used in analogue integrated systems. Briefly outline the main feature of each of these circuits.

[4]

For the bandgap voltage reference circuit of Figure 1(a), show that $\delta V_0 / \delta T = 0$ (where T is temperature) if $(R_2/R_3)ln\ [\ I_1/I_2\ ] = 29$ for $V_0 = 1.283\ V$. Assume the temperature coefficient of V_{BE} to be -2.5mV/°C, the collector current of transistor Q_3 is 100μA and the device saturation current is $I_S = 1.2 \times 10^{-13} A$. Boltzmann's constant $k = 1.38 \times 10^{-23} J/K$ and the electron charge is $q = 1.6 \times 10^{-19} C$.

[7]

(b) Show that the circuit of Figure 1(b) can be developed into a current source with output current directly proportional to absolute temperature and virtually independent of supply voltage. It is likely that on power-up the output current will fall into a zero current state. Sketch a suitable start-up circuit that ensures that this condition will not occur and explain the operation of the circuit.

[9]

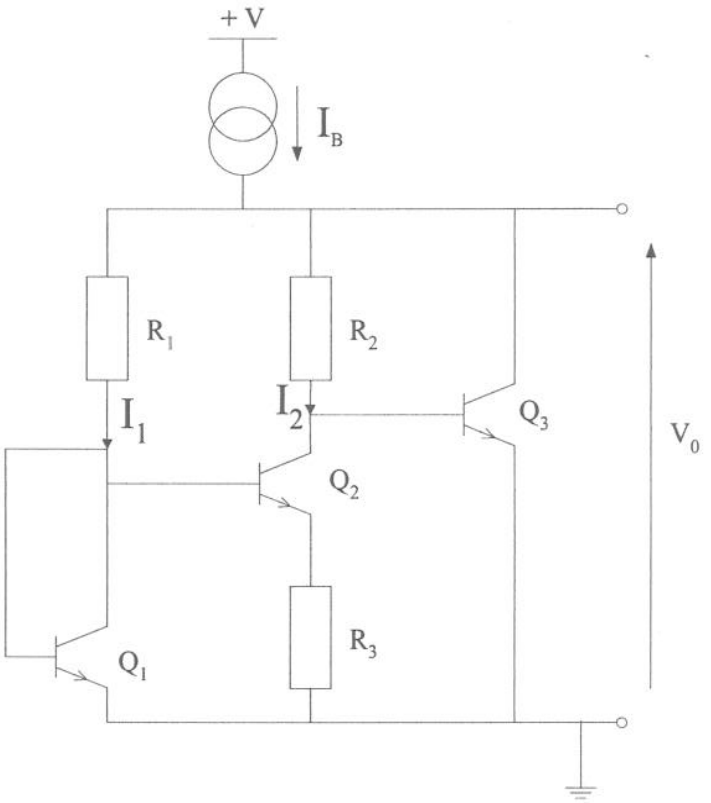

Figure 1(a)

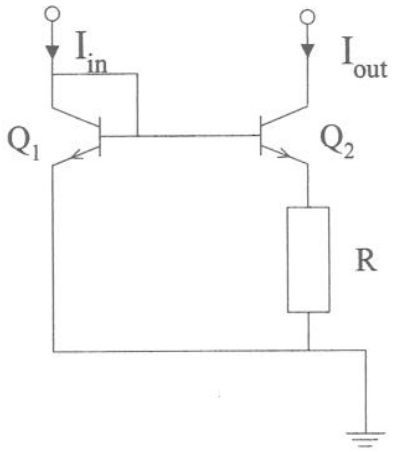

Figure 1(b)

2. (a) Sketch a typical architecture of a current-mode algorithmic analogue to digital converter and explain its principles of operation.

[10]

(b) Assume that the maximum resolution of any sampled-data converter is limited by switch noise (KT/C), calculate the maximum resolution of a stereo-audio system running at a sample rate of 40 kHz. Assume a MOSFET switch aspect ratio $(W/L) = 1/8$, transconductance parameter $Kp = 20\ \mu A/V^2$ and a device threshold voltage $V_T = 1\ V$. The on voltage of the switch is a $5\ V$ reference (i.e. $V_{GS}on = V_{ref} = 5\ V$). You may also assume that the switch settles in $10\ \tau$ (where τ = time constant) over one period of the clock frequency.

Boltzmann's constant $k = 1.38 \times 10^{-23}\ J/K$ and the ambient temperature is $300\ K$.

[10]

3. Figures 3(a) and 3(b) show the basic design of two integrated circuit precision integrators.

   (a) Derive an expression for the time constant of each integrator. Assume that the sampled-data integrator of Figure 3(b) is driven by non-overlapping clocks and that the switches are ideal. Give advantages and disadvantages of continous-time versus sampled data integrators

   [16]

   (b) With the addition of a single switched capacitor to Figure 3(b) show how the integrator can be made lossy?

   [4]

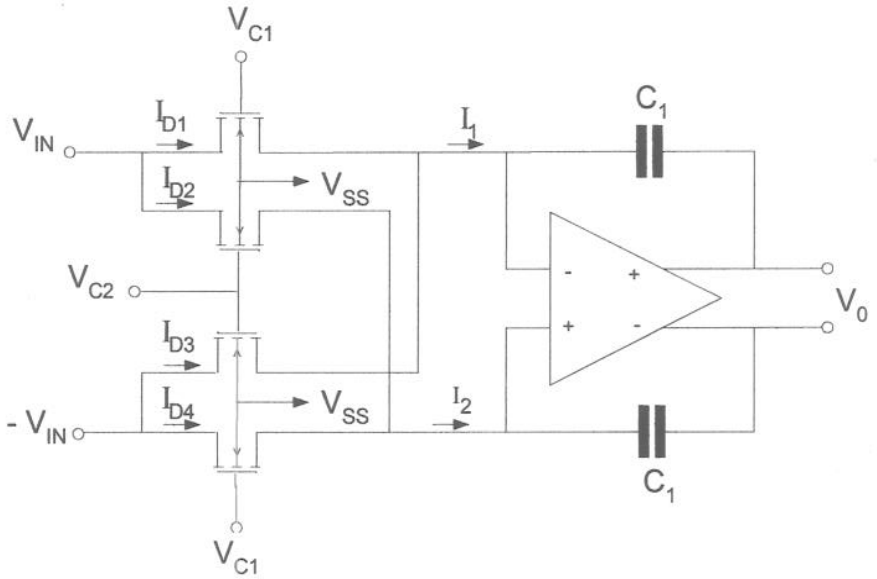

Figure 3(a)

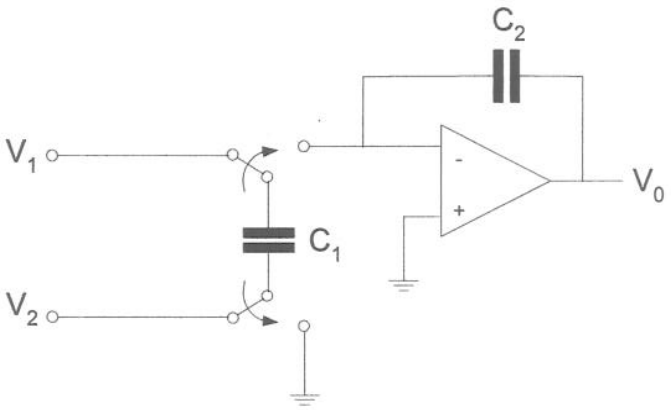

Figure 3(b)

4. Figure 4 (a, b c, and d) show four popular biasing schemes typically used in analogue integrated circuits.

   (a) Briefly explain the function of each of the circuits in Figure 4 (a, b, c and d).

   [8]

   (b) Design the constant current generator of Figure 4(c) to give an output current of 5 μA. Assuming R is a polysilicon resistor with a temperature coefficient of 1500 ppm/°C, calculate the fractional temperature coefficient of the circuit at room temperature.

   [4]

   (c) Derive an expression for the output resistance of the circuit of Figure 4 (d). Explain why this resistance is enhanced over the case when the gate of the transistor Q3 is connected to a fixed d. c. voltage.

   [8]

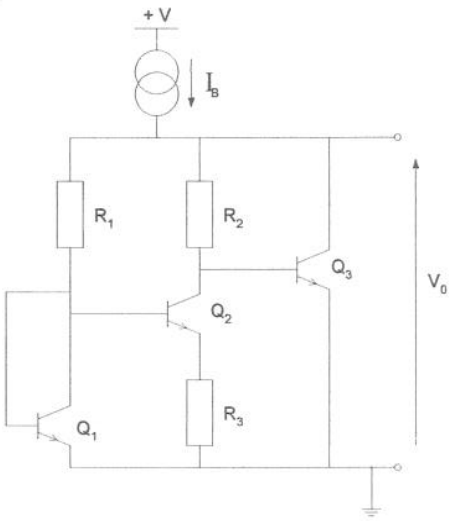

Figure 4(a)

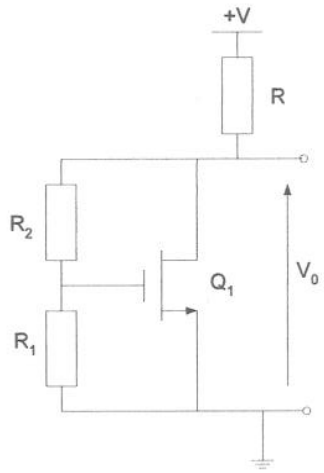

Figure 4(b)

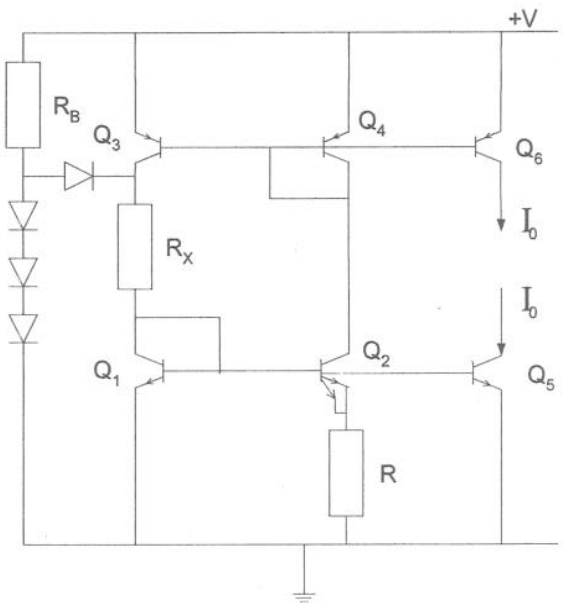

Figure 4(c)

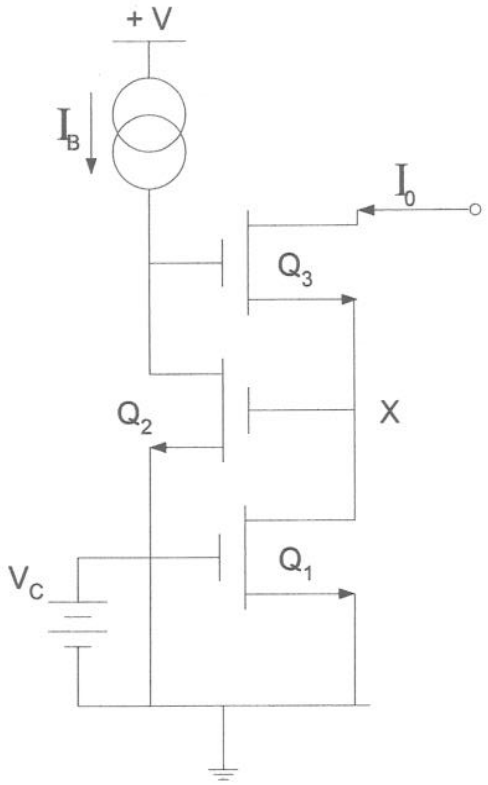

Figure 4(d)

5. (a) Give two advantages of current-mode analogue signal processing compared to traditional voltage-mode processing.

[4]

(b) With the aid of a suitable macromodel, explain the theoretical concept of current feedback and how it results in constant bandwidth amplification. Using a current-feedback op-amp, design a closed-loop non-inverting gain stage with a bandwidth of 10 MHz for a fixed voltage gain of 100. Assume an internal compensation capacitance of 4pF and that the open-loop transresistance gain of the amplifier is very much larger than the amplifier feedback resistor.

[16]

6. (a) Figure 6(a) shows a folded cascode connection. What is the main advantage of this design over the more classical cascode connection? Show via a brief sketch how the architecture of Figure 6(a) can be used to form the basis of a single stage fully differential folded cascode operational amplifier (op-amp) with common-mode feedback included.

[6]

(b) Figure 6(b) shows a two-stage CMOS op-amp. Estimate the low-frequency differential voltage gain and gain-bandwidth product of the amplifier. Aspect ratios of all devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below. What is the main advantage and disadvantage of a single-stage compared to a two-stage op-amp ?

[11]

(c) Explain why a resistor in series with the compensation capacitor C in Figure 6(b) can significantly improve the amplifier's phase margin.

[3]

CMOS TRANSISTOR PARAMETERS

MODEL PARAMETERS	Kp ($\mu A/V^2$)	λ (V^{-1})	V_{T0} (V)
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

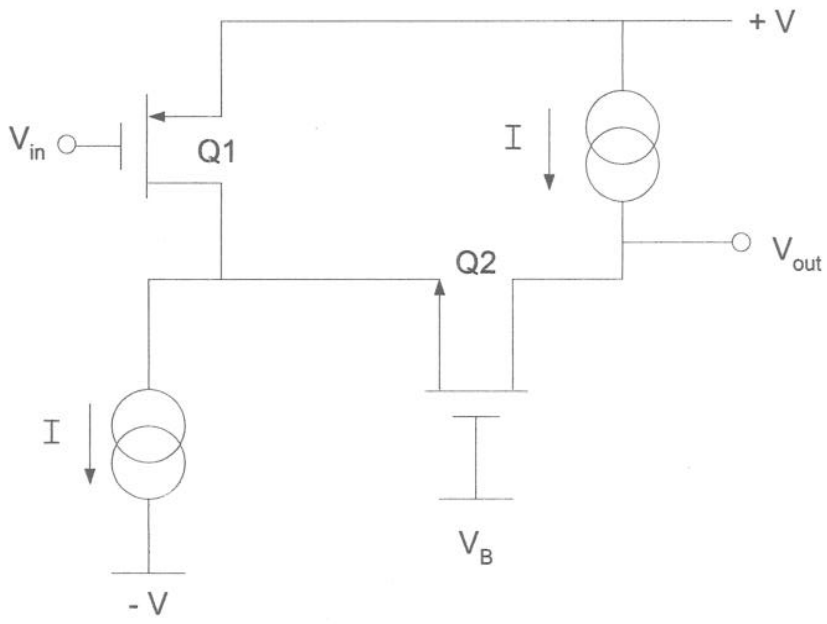

Figure 6(a)

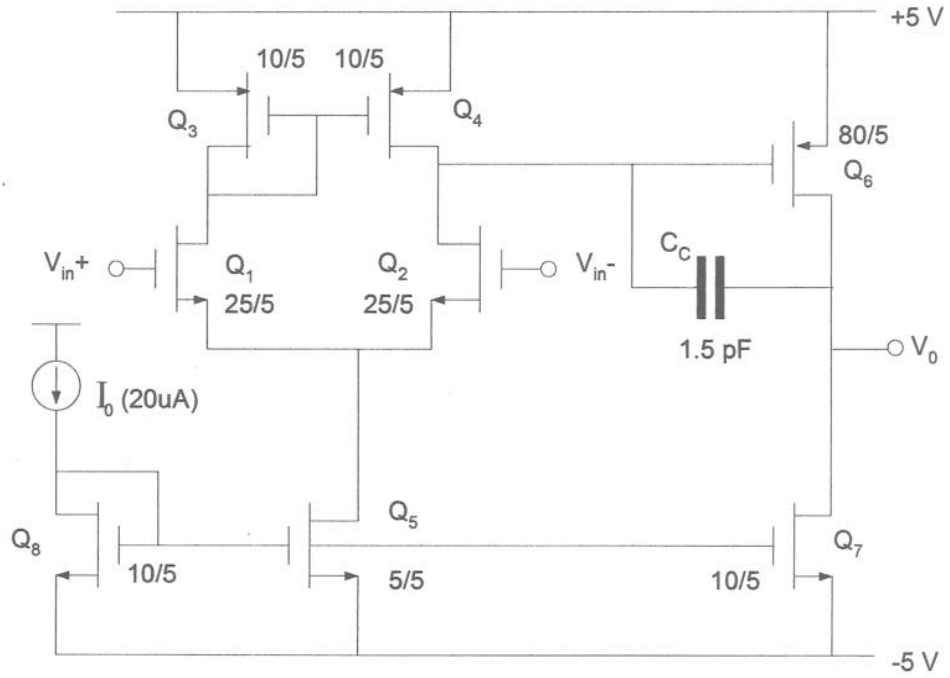
+5 V
10/5
10/5
Q3
Q4
80/5
Q6
Vin+
Q1
25/5
Q2
25/5
Vin-
Cc
1.5 pF
Vo
I0 (20uA)
Q5
Q8
10/5
5/5
10/5
Q7
-5 V

Figure 6(b)