E4.20
AC3
ISE4.19

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2009

MSc and EEE/ISE PART IV: MEng and ACGI

Corrected Copy

Fig 3.2

INTRODUCTION TO DIGITAL INTEGRATED CIRCUIT DESIGN

Tuesday, 5 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung
Second Marker(s) : C. Bouganis

Information for Invigilators:

Students may bring any written or printed aids into the examination.

Information for Candidates:

Students may need red, green, blue, yellow and black coloured pens.

1. a) *Figure 1.1* (see the colour supplementary sheet) shows the layout of an n-well CMOS circuit with five input terminals: `d0, d1, d2, s0 and s1` and one output `y`. Extract and draw the transistor-level schematic diagram of this circuit. Note that the supply signals are labelled as `vdd` and `gnd`.

[10 marks]

b) What function does this circuit perform? Provide a brief description on how this circuit works.

[4 marks]

c) For the layout shown in *Figure 1.1,* draw the vertical cross section along the lines `PP'` and QQ′. Label your diagram indicating the n-well region and the different types and levels of doping (e.g. p^-, n^+ etc).

[6 marks]

2. *Figure 2.1* (see the colour supplementary sheet) shows the layout of a 4 word x 6 bit ROM array without the address decoder and output inverting buffer circuits.

a) Given that the value stored at address 0 bit 0 is 1 and that Out0 is the least significant bit, what are the values stored in all four locations? Explain the operation of this circuit.

[6 marks]

b) Draw the circuit schematic for this layout.

[8 marks]

c) Draw the transistor-level schematic diagram of the rest of the circuit (i.e. address decoder and output buffer) to form a working 4 x 6 ROM. Explain briefly how your circuit works.

[6 marks]

3. *Figure 3.1* shows the schematic of a Complementary Universal Logic Gate (CULG) which can be customised to implement various 3-input functions by connecting the drains of the NMOS transistors (indicated by dark squares) to the appropriate source terminals (indicated by dark circles). This circuit uses complementary inputs, such as `a` and `ax` (`ax` is the complement of `a`), and produces complementary outputs `f` and `fx`.

   a) *Figure 3.2* shows a CULG circuit configured as a 3-input function with three complementary inputs `a, ax, b, bx, c` and `cx`, and outputs `f` and `fx`. Derive the truth table for this gate showing only `a, b, c` and `f`.

   [4 marks]

   b) What are the purposes of the cross-coupled PMOS transistors and the output inverters?

   [2 marks]

   c) Explain why the circuit shown in *Figure 3.3* implements a transparent latch? What are the timing constraints necessary for the input signals Φ1 and Φ2?

   [4 marks]

   d) Using a stick diagram or other symbolic representation, design the layout of the unprogrammed CULG cell (i.e. as shown in *Figure 3.1*), taking into account that the programmable interconnections are best done using vias (or contacts).

   [10 marks]

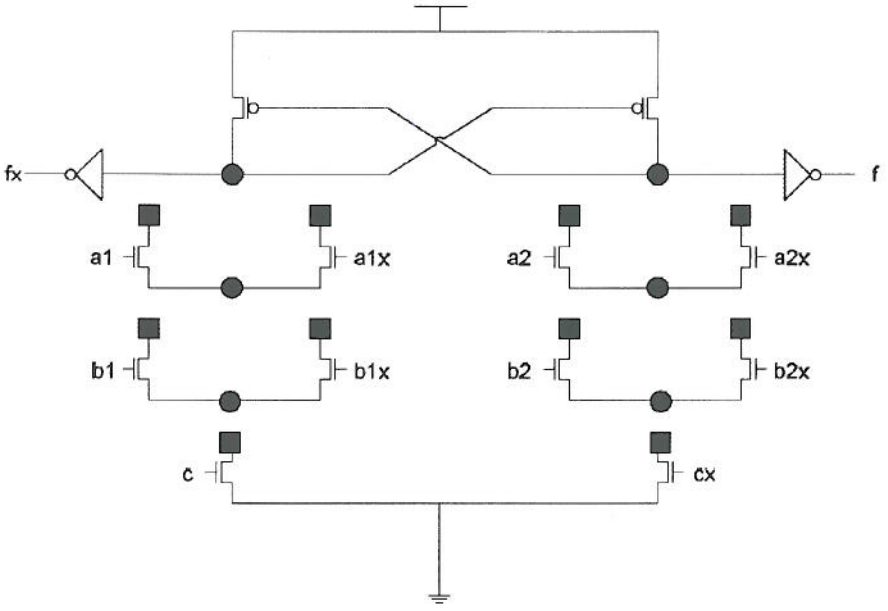

Figure 3.1

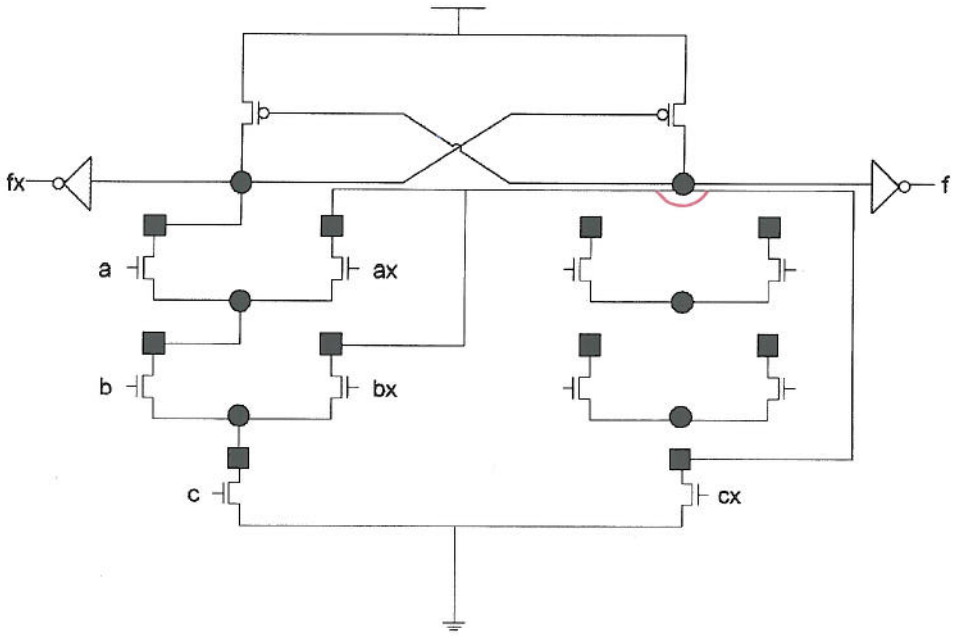

Figure 3.2

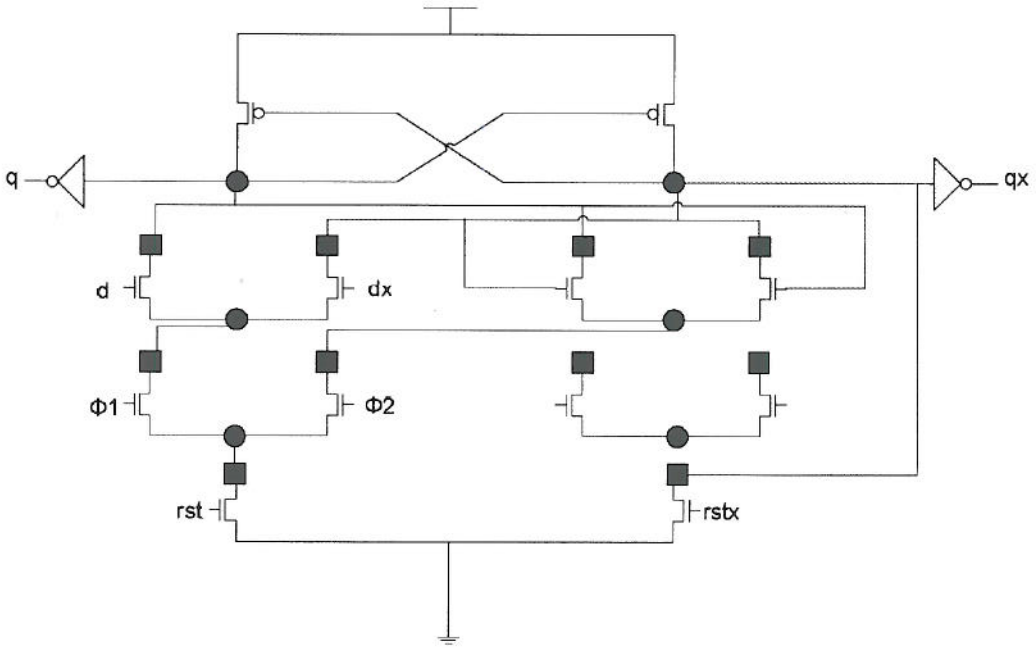

Figure 3.3

4. a) With the help of a diagram, explain the principle of a pulse-triggered register circuit. What are its advantages and disadvantages?

[4 marks]

b) With the help of a diagram, explain the principle of a scan-path register. How may scan-path registers be used to help testing of digital integrated circuits?

[4 marks]

c) *Figure 4.1* shows the clock control circuit for a pulse-triggered scan-path register. Using the timing diagram shown for CLK and TE, explain the function of this circuit and draw the timing diagram for the expected output signals DE, NDE, ST and NST.

[6 marks]

d) *Figure 4.2* shows the register circuit. Explain briefly how this circuit works.

[6 marks]

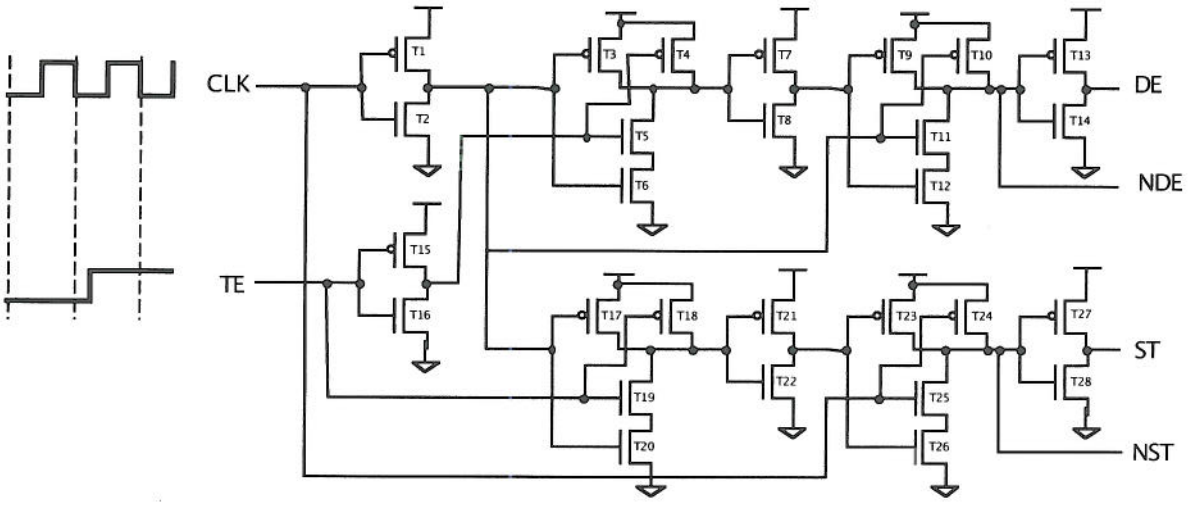

Figure 4.1

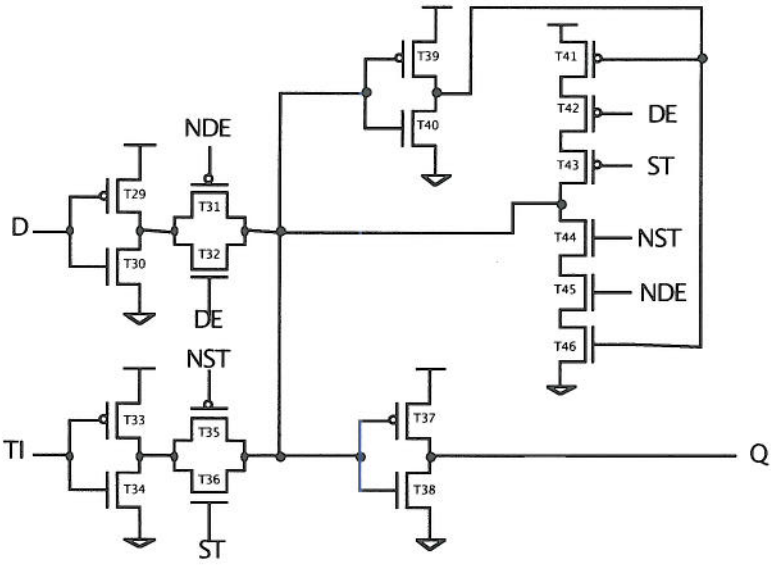

Figure 4.2

5. a) For the circuit in *Figure 5.1*, assume a two unit delay through the register and logic blocks (i.e., $t_R = t_L = 2$). Assume that the registers, which are positive edge-triggered, have a setup time t_S of 1 and zero hold time. The delay through the multiplexer t_M equals t_R.

(i) Assuming that the clock skew is zero, determine the minimum clock period of the circuit assuming that the multiplexer MUX is controlled by a signal synchronous to the clock CLK.

[4 marks]

(ii) What is the minimum clock period of θ if the clock skew is $\delta = t'_\theta - t_\theta = 3$?

[4 marks]

b) In a 180nm CMOS process, the widths of a minimum size inverter p and n transistors are 360nm and 180nm respectively. The unit delay is given to be 20ps. The circuit contains two separate clock paths P1 and P2 as shown in *Figure 5.2*. The total gate widths seen by the two paths are 500μm and 100μm respectively.

(i) Using the method of logical effort, or otherwise, estimate the clock skews between the paths if the inverters shown in *Figure 5.2* are minimum size.

[5 marks]

(ii) Determine the best number of stages of inverters (N_1 and N_2) to use on the two paths in order to minimize the clock skew. For this number of stages, size the inverter buffer circuits for each clock path so that the clock signal delay on each path is minimized.

[7 marks]

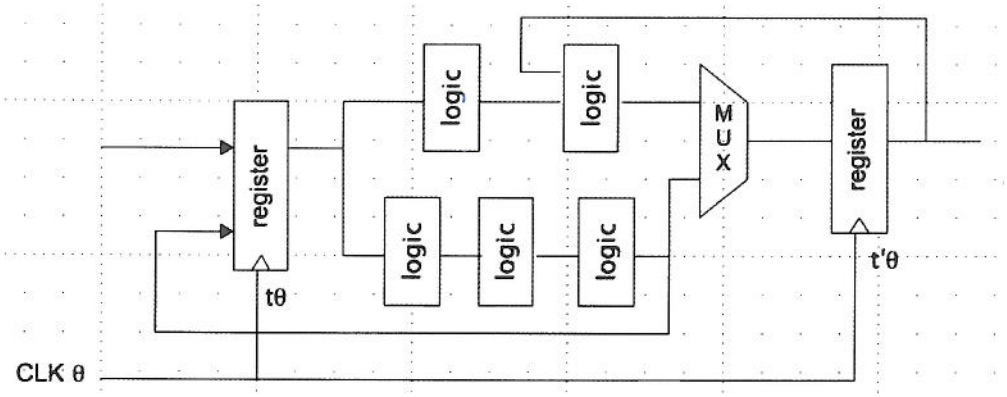

Figure 5.1

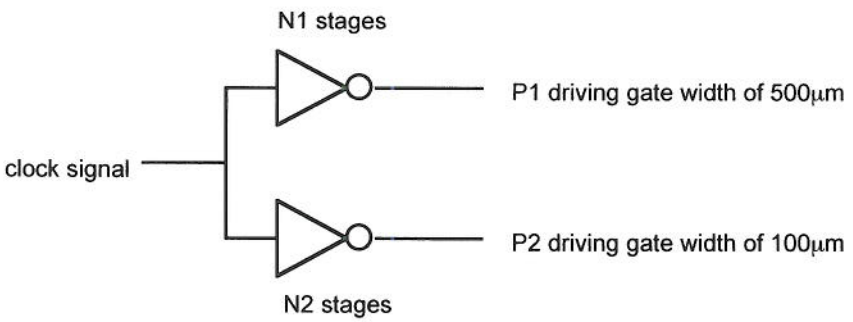

Figure 5.2

6. a) *Figure 6.1* shows the transistor-level schematic diagram of a latch circuit. Given that the timing diagram for the input signals CLK and IN is as shown in *Figure 6.2*, draw the timing diagram for the signals at X, Y, Z and D. Label your timing diagram indicating the various states of the signal nodes as:

driven low (DL) - a path to ground exists,
driven high (DH) - a path to VDD exists,
charged low (CL) - high impedance with no stored charge at ground, and
charged high (CH) - high impedance with stored charge at VDD.

You may assume that initially both Y and Z are charged high.

[8 marks]

b) By considering the high and low phases of the clock signal, explain the function of this circuit.

[6 marks]

c) What is the effect of adding the shaded circuit to the latch as shown in *Figure 6.3*?

[6 marks]

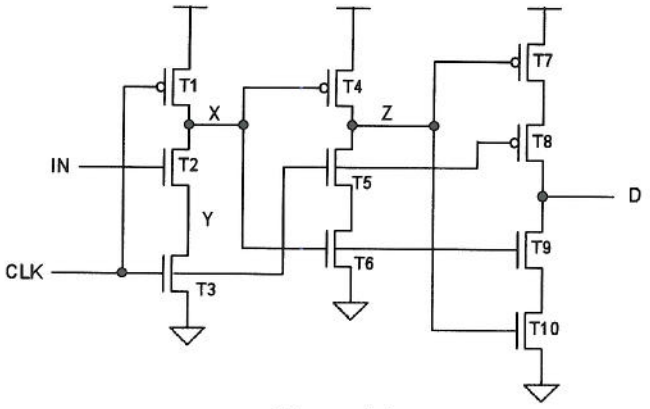

Figure 6.1

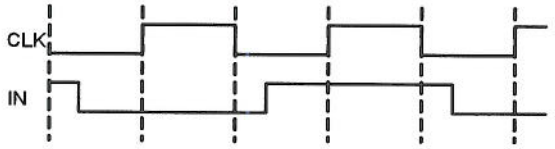

Figure 6.2

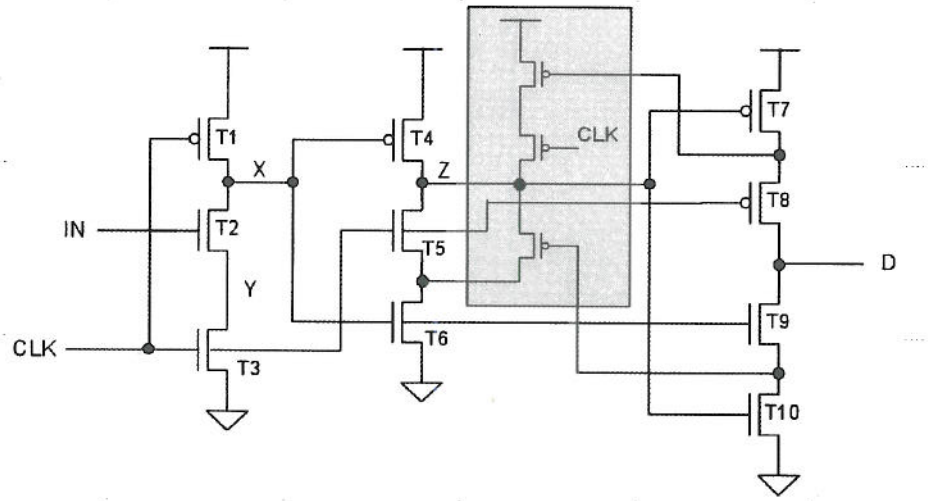

Figure 6.3

Colour Supplementary Sheet

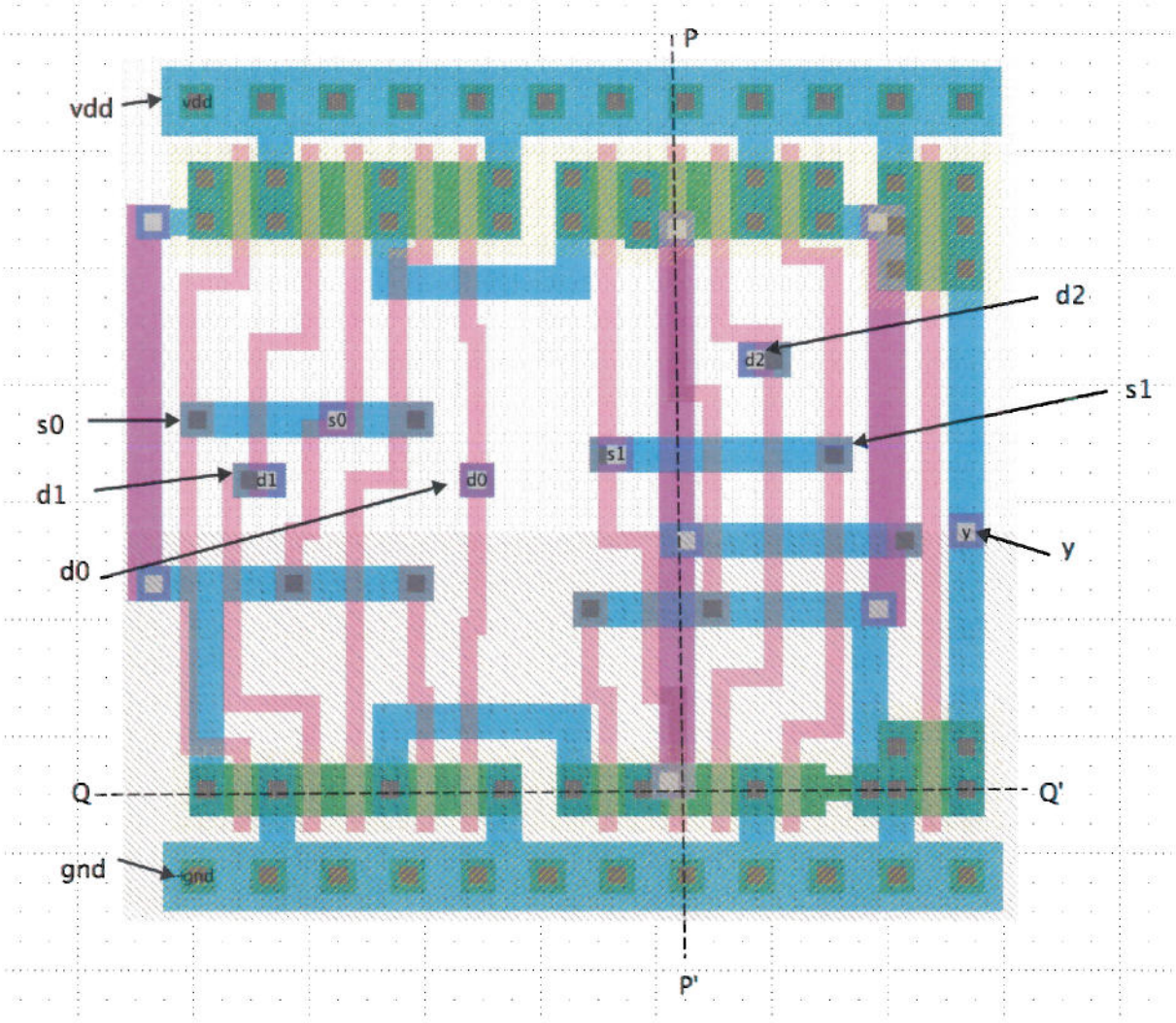

Figure 1.1 Layout of full-custom cell for Question 1

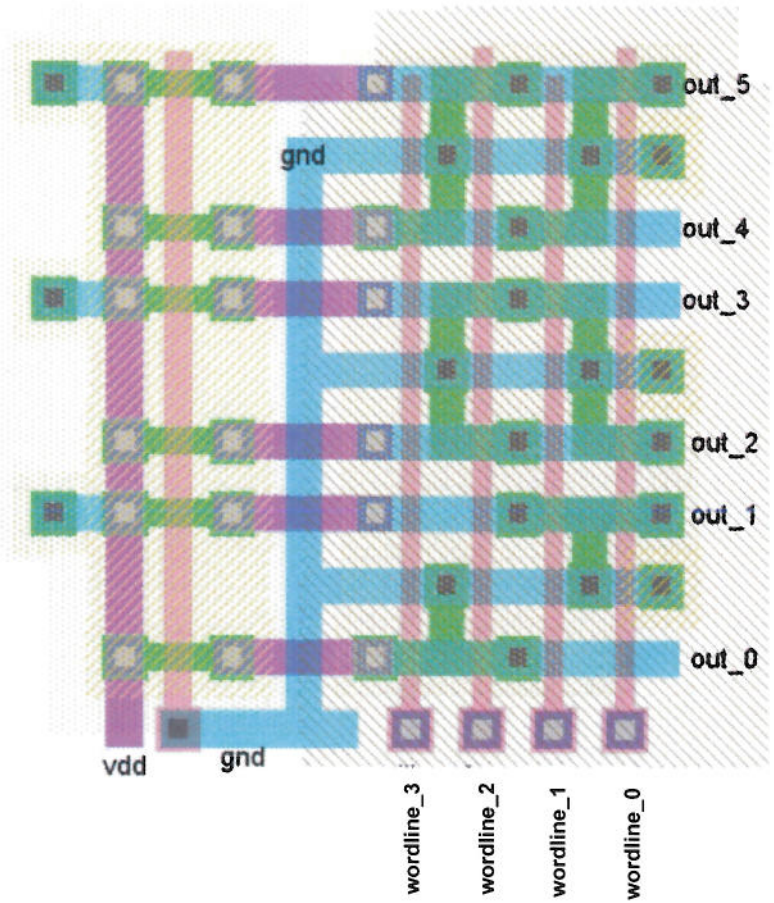

Figure 2.1 Layout of a 4 x 6 ROM for Question 2

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DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
M.Eng. and A.C.G.I. EXAMINATIONS 2009

PART IV

INTRODUCTION TO DIGITAL IC DESIGN

SOLUTIONS

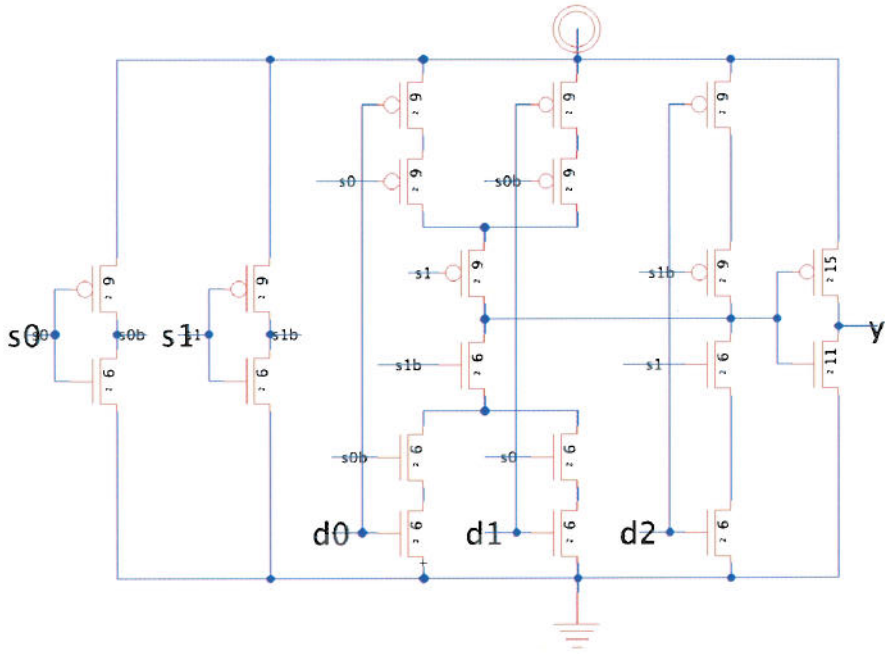
This is an open-book examination.

You may need red, green, blue, yellow and black coloured pens.

First Marker: *Peter Cheung*
Second Marker: *Christos Bouganis*

Solution to Question 1

a) This question tests student's ability to understand a full custom layout. The extracted circuit should be (note that transistor sizes are not required):



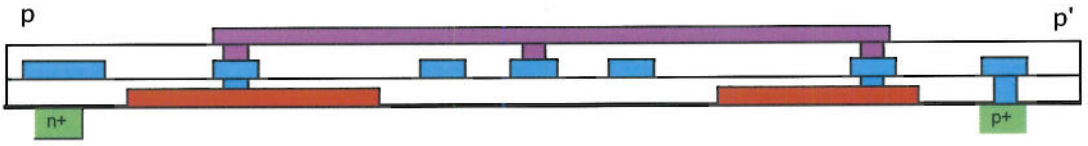
[10 marks]

b) This circuit implements a 3-input MUX.

[4 marks]

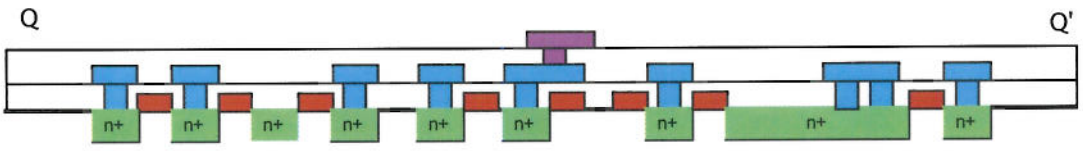
d) This part of the question tests student's ability to relate the layout to the physical process and different layers on the chip.

[6 marks]



Important points to note:

- No diffusion underneath the poly gates
- Poly to M2 needs to go through M1 layer



Solution to Question 2

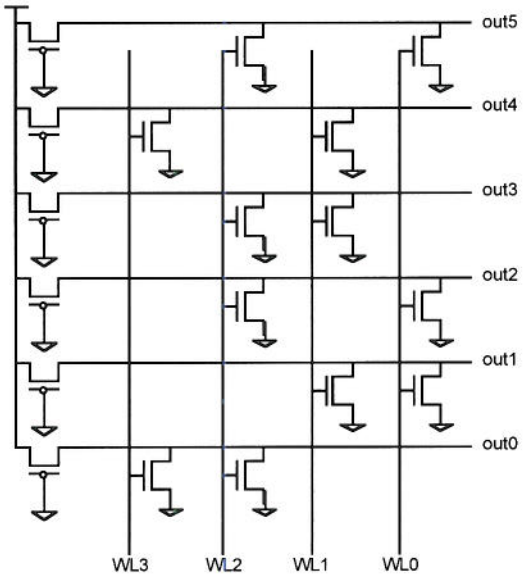
This question tests student's ability to interpret a regular array layout. The layout is generated by the ROM generator of Electric, the CAD tool used on this course.

a)

Address	ROM Content
0	011001
1	100101
2	010010
3	101110

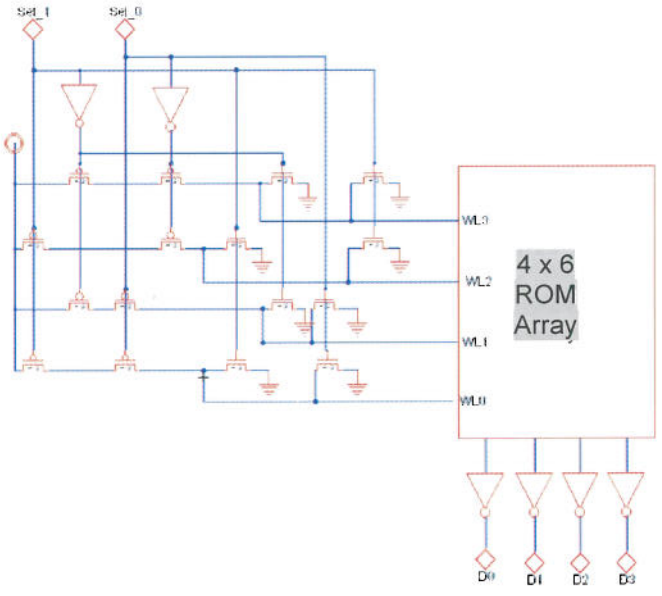
[6 marks]

b)



[8 marks]

c)



[6 marks]

Solution to Question 3

This question is based on the paper "A comparison of via-programmable Gate Array Logic Cell circuits", by Chau etc. in Proccedings of ACM Symposium in FPGA, 2009.

a) This is a 3-input NAND gate (simple truth-table). Students are expected to explain how the circuit actually works.

[4 marks]

b) The purpose of the cross-coupled PMOS transistors is to provide positive feedback so that weak ones are pulled up strongly. This technique is commonly used in complementary pass logic (such as CPL and DPL). The output inverters provide further buffering in order to drive loads.

[2 marks]

c) This is a transparent latch with phi1 and phi2 being the non-overlapping clock. Rst and rstx force the latch to go into reset state.

[4 marks]

d)

This part of the answer depends on student's individual layout. Marks are deduced if the drains of the transistors (indicated by squares) are NOT easily connected to the sources (indicated by the circles), so that via programming becomes difficult.

[10 marks]

Solution to Question 4

This question tests student's understanding of scan-path and pulse-triggered registers. The circuit is based on US Patent 6,911,845, "Pulse Triggered Static Flip-flop having scan test" by Hossain and Cavalli (2005).

(a) Book work. There should be a pulse generator circuit converting the clock signal into a pulse, and a latch driven by the clock pulse. Advantages of pulse triggered registers is that it is clock skew independent and is true single-phased clocking. The disadvantages is that it uses more transistors.

[4 marks]

(b) Book work. Scan-path register is a normal register with an additional test data in port, which can be constructed to form a serial-in serial-out register.

[4 marks]

(c) T3-8, T9-14, T17-22, T23-28 form 4 AND-gates (NAND+inverter). Together, they produce a pulse on DE (data enable) on positive edge of CLK if TE=0. The pulse with is roughly the delay of NAND+inverter. Similar, a pulse is produced on ST (scan test) if TE = 1, on the positive edge of CLK.

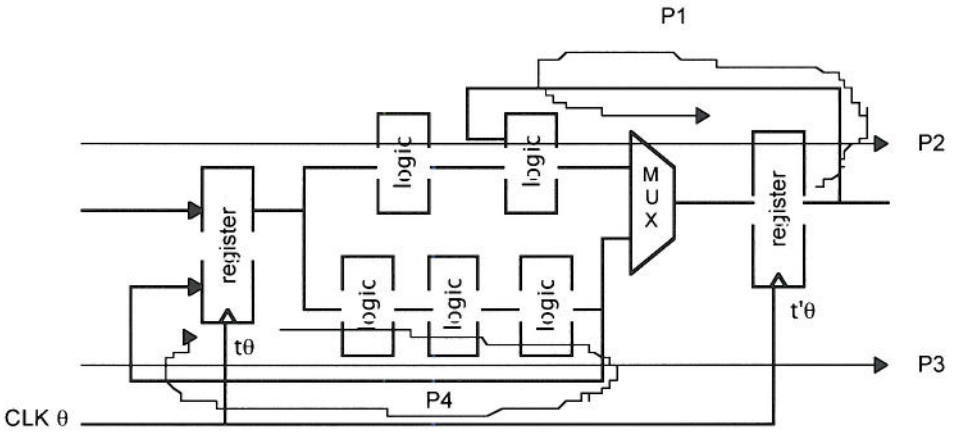
[6 marks]

(d) This is a conventional pass-transistor based latch. T39 – 46 is essentially feedback keeper circuit to ensure that this is a static latch. Since the clocking is pulse triggered, it is acting as a register (instead of a latch). T42 – 45 ensure that the feedback loop is open during pulse sampling so that "fight" does not occur.

[6 marks]

Solution to Question 5

a)



(i) Out of the 4 paths shown in the figure, p3 is the critical one and determines the lower bound on the clock period. Using $T \geq t_{reg} + 4t_{logic} + t_{setup} - \delta$, we get ***Tmin* = 2+8+1 = 11**.

[4 marks]

(ii) As the clock skew increases, the most significant path changes. Repeating the calculations in part (i) we get : Tmin(p1) = 7, Tmin(p2) = 9-3=6, Tmin(p3) = 11-3=8, Tmin(p4) = 9. (Note that the clock skew is 0 for paths p1 and p4). Therefore the minimum clock period is Tmin = 9.

[4 marks]

b) (i) Gate width of minimum size inverter is 0.54 μm. t_d = 20ps. Therefore, the Electrical Effort (and total effort F) for the two paths are:

F_{P1} = 500 /0.54 = 926; F_{P2} = 100 / 0.54 = 185;

Delay estimates of the two paths are: $D_{P1} = 926 * t_d = 18.52$ ns; $D_{P2} = 133 * t_d = 3.7$ ns
P1-P2 skew = $1067 * t_d = 14.82$ ns.

[5 marks]

(ii)

Total effort F for P1 = 926, P2 = 185. Best number of stages (from notes) is given by:
Nbest = log (F)/ log (3.59). $N_{P1} \approx 5.3$, $N_{P2} \approx 4.1$. P1 should be buffered by 6 inverter stages, P2 also by 4 stages. Therefore

For P1, each stage should increase in size by $\sqrt[6]{926} = 3.12$,
for P2, each stage should increase in size by $\sqrt[4]{185} = 3.69$.

Solution – increase sizes of p-trans and n-trans by these factors for each of the stages (round to nearest integer):

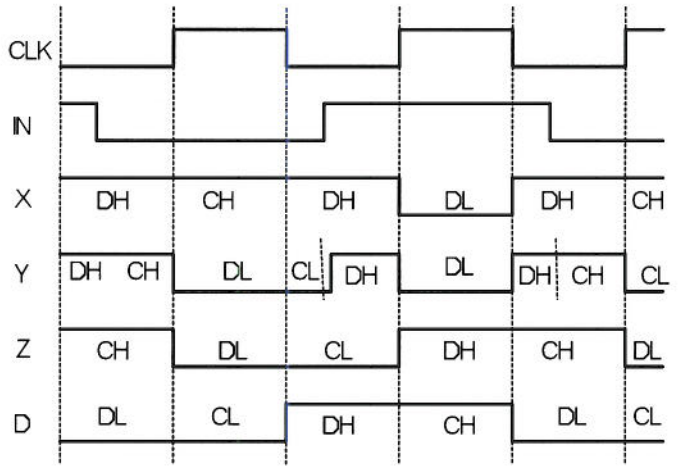
Stage	1	2	3	4	5	6
P1:	x 1	x 3	x 10	x 30	x 95	x 296
P2:	x 1	x 4	x 14	x 50		

P1 delay ≈ $(3/1 + 10/3 + 30/10 + 95/30 + 296/95 + 926/296) * t_d = 18.74\ t_d$
P2 delay ≈ $(4/1 + 14/4 + 50/14 + 185/50) * t_d = 14.77\ t_d$
Clock skew ≈ $3.97* t_d \approx$ 79ps.

[7 marks]

Solution to Question 6

a) This circuit is taken from "New Single-Clock CMOS Latches and Flipflops with Improved Speed and Power Savings" by Yuan and Svensson, IEEE JSSC vol 32, no 1, Jan 97.



[8 marks]

b) The circuit can be viewed as three stages: 1st stage has CLK driving p- and n-transistor (known as PN). This is a precharge circuit. 2nd stage has CLK driving a n-transistor only (known as SN). Together with 1st stage, it evaluates IN to yield Z when CLK goes high. The 3rd stage is a full latch (FL(P)) similar to the C^{2}MOS circuit except that we only use CLK and not CLK_bar. Instead, the precharge node X is used in place of CLK_bar. This is clever because when CLK is low (precharging), X is always high. Therefore during evaluation phase (CLK='1'), the 3rd stage is in storage state. During precharge phase (CLK='0'), the 3rd stage is sampling the data input at Z since it works just like an inverter. Therefore this is working as a single-phase clocking latch.

[6 marks]

c) Z is a dynamic node such that during precharge phase (CLK='0'), it always is a charge node. The circuit in the shade box provide feedback to turn Z into a static node. Note that the output of 3rd stage remains a dynamic node – it becomes tristate when CLK is high. This is actually an advantage when this is driving a bus. (See Yuan's paper.)

[6 marks]