IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2003

MSc and EEE/ISE PART III/IV: M.Eng., B.Eng. and ACGI

DIGITAL SYSTEM DESIGN

Wednesday, 7 May 10:00 am

Time allowed: 3:00 hours

There are SEVEN questions on this paper.

Answer FOUR questions.

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Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible   First Marker(s) :   P.Y.K. Cheung

Second Marker(s) :   D.M. Brookes

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X7:0 is an eight bit bus with X7 being the MSB and X0 the LSB.

Hexadecimal numbers are prefixed with '$'. For example the decimal number 10 is written as $A.

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

1. a) Given that x is an N-bit signed two's complement number, show that

$$x = \sum_{i=0}^{N-1} 2^i (-x_i + x_{i-1})$$

where $x_{-1} = 0$, and for $i \geq 0$, x_i is bit i of x.

Hence, or otherwise, show that

$$x = \sum_{j=0}^{N/2-1} 2^{2j} (-2x_{2j+1} + x_{2j} + x_{2j-1}).$$

State any assumptions used.

[5]

b) Using an 8-bit binary adder, a 13-bit register, a 6-input multiplexer, and any additional gates or multiplexers required, design a circuit that multiplies two 6-bit 2's complement signed numbers in three clock cycles to give a 12-bit 2's complement answer. Draw a timing diagram showing the control signals required for your circuit.

[12]

c) Given that the propagation delays of the various components are as follows: MUX – 5ns; adder – 15ns; register – 5ns; XOR gate – 5ns; any other gates – 2ns; and that the data set-up time for the register is 2ns, derive the maximum possible clock frequency for your circuit. State any further assumptions you make.

[3]

2. a) Briefly explain the operating principle of JTAG boundary scan. Discuss why the JTAG boundary scan test standard is important in testing modern electronic systems. Brief explain how a circuit containing JTAG compliant components can be tested for interconnection faults

[7]

b) Explain what is meant by metastability in a digital system and the circumstances under which it can arise. Explain how a circuit can be protected against the effects of metastability.

[3]

c) Explain the cause of ground bounce found in digital circuits. How may ground bounce be reduced?

[5]

d) With the help of a schematic, explain what is a bus-hold circuit. What is the use of such a circuit?

[5]

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3. Figure 3.1 depicts a 512 x 16 bit synchronous first-in-first-out (FIFO) memory module that is implemented inside an Altera Flex10K FPGA device. All operations are synchronous to a system clock signal *clk*. On the rising edge of *clk*, input data *d_in* is stored in the FIFO if the *put_get* signal is high and output data is read out to *d_out* if *put_get* is low. Data words are read out in the same order that they are stored. If the number of data stored in the FIFO is 510 or higher, the signal *full* goes high. Similarly if the number of data stored is 2 or less, the signal *empty* goes high. The signal *reset* initializes the FIFO to an empty state. The FIFO is enabled by the *strobe* signal which goes high for one cycle when there is either a read or a write operation. You may assume that circuits external to the FIFO ensure that it never overflows or underflows.

a) Using counters as address pointers, static RAM and other circuit components, sketch the functional design of this synchronous FIFO. You may use any functional logic blocks such as adders, subtractors and comparators. Do not show any gate level design of your circuits.

[10]

b) Figure 3.2 depicts a Embedded Array Block (EAB) found in the Flex10K family of FPGA. Each EAB can be configured as 2048 x 1, 1024 x 2, 512 x 4 or 256 x 8 block of RAM. The data output can be registered or unregistered depending on how the EAB is configured as shown in Figure 3.2.

(i) With the aid of a diagram, explain how you would use multiple EABs to implement the memory used in the FIFO.

[4]

(ii) Estimate with justifications the approximate number of logic elements (LEs) required to implement the FIFO. Each LE consists of a 4-inputs-1-output lookup table and an optional 1-bit register.

[4]

(iii) Explain why one may want to register the output data from the EAB memory as shown in Figure 3.2.
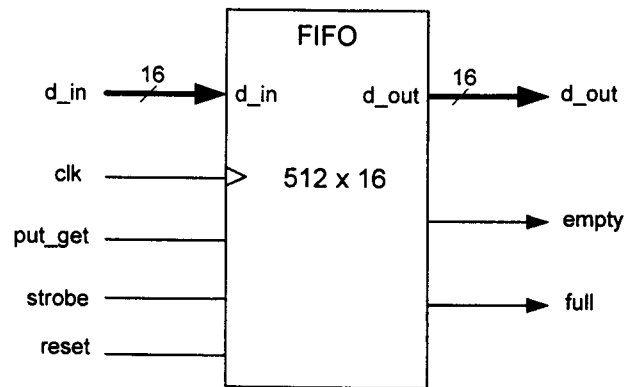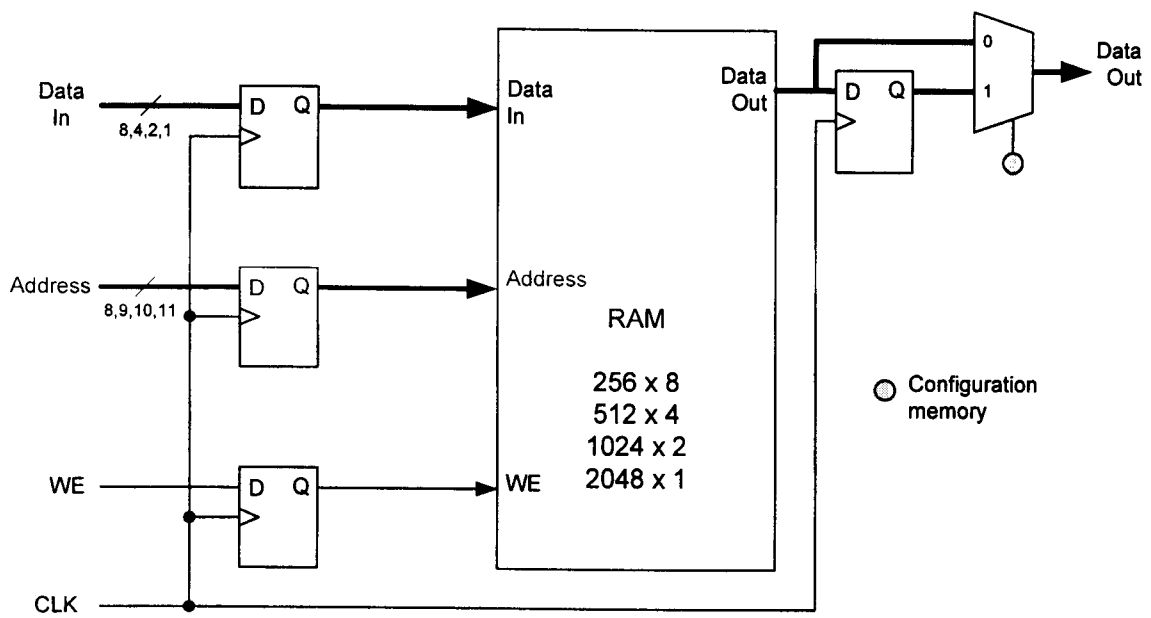
[2]

Figure 3.1

Figure 3.2

4. Figure 4.1 shows a finite state machine (FSM) that recognises some binary serial patterns applied to X and, when any of these serial pattern occurs, Y is driven high. Figure 4.2 shows the state diagram of the FSM.

c) Using the implication chart method, find the minimum state diagram of this FSM.

[10]

d) Draw the fully reduced state diagram.

[3]

e) Implement this state machine using one-hot state encoding. Your implementation should be in the form of Boolean equations.

[4]

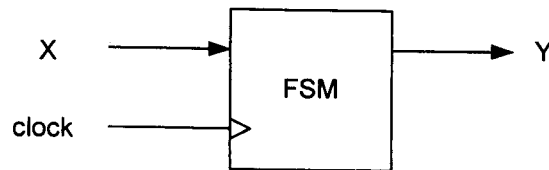f) What binary sequence is recognised by this state machine?
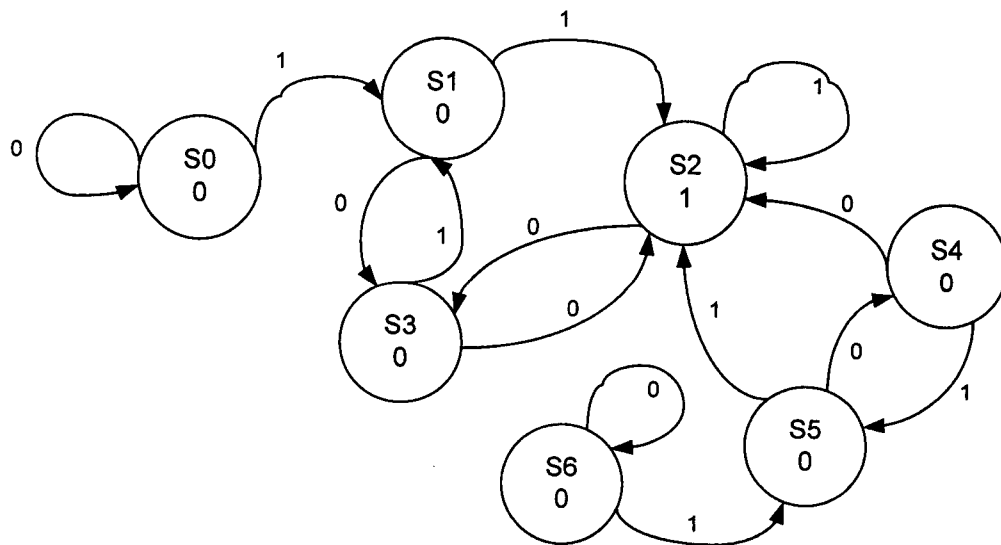
[3]

Figure 4.1

Figure 4.2

5. An asynchronous serial data stream *DIN* is encoded according to the following rules:

1) A '0' bit is represented by a high pulse in *DIN* lasting for a duration T;

2) A '1' bit is represented by a high pulse in *DIN* lasting for a duration 2T.

3) Each '0' or '1' bit is separated by a 'space' consisting of a low level signal lasting for a duration >=T as shown in Fig 5.1;

Any high pulses with a width shorter than 0.5T or longer than 2.5T are ignored. A system clock signal with a period of T/16 is available.

A circuit is required to decode such a data stream and produce two signals *IsZero* and *IsOne* corresponding to a '0' bit and a '1' bit respectively. If a zero is decoded, *IsZero* should go high for one system clock cycle 1.5T after the start of the '0' bit. If a one is decoded, *IsOne* should go high for one system clock cycle 2.5T after the start of the '1' bit. This is demonstrated in Figure 5.1.

Design a FSM connected to a 4-bit binary counter, to produce the *IsZero* and the *IsOne* signals. The design of the FSM should be in the form of an ASM chart or a state transition diagram. Indicate clearly how the FSM is interfaced to the counter.

You may assume that all transitions of *DIN* occur slightly after the rising edge of the system clock.
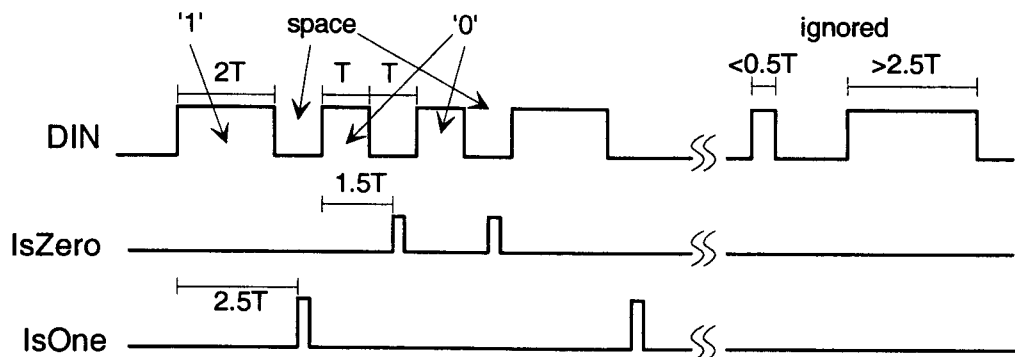
[20]

Figure 5.1

6. *Figure 6.1* shows the memory interface circuit for a 8-bit microprocessor system with a 16-bit address bus and is controlled by a symmetrical clock running at 66 MHz. The system has three memory components with the following address ranges and chip-enable/address to data access times:

	Address Range (hex)	Access Time (EN/Addr to Data)
ROM	0000 - 7FFF	10 ns
RAM	8000 - EFFF	8 ns
FRAM	F000 - FFFF	30 ns

The processor memory read cycle with a single wait cycle inserted is given in *Figure 6.2* with the various timing constraints as shown. The $\overline{WAIT}$ signal is sampled on the falling edge of *CLOCK* during T2 and subsequent wait cycles, and one extra cycle is inserted if $\overline{WAIT}$ is low, otherwise it proceeds to T3.

a) Derive in the form of Boolean equations the address decoder circuit needed to generate the chip-select signals for ROM, RAM and FRAM. (Memory should only be enabled during memory accesses.)

[4]

b) Assuming that the address decoder circuit has a worst-case delay of 5 ns, derive the number of wait states, if any, needed for each type of memory read access.

[6]

c) Design a circuit to produce the signal $\overline{WAIT}$ required to ensure proper memory read access for the memory components.
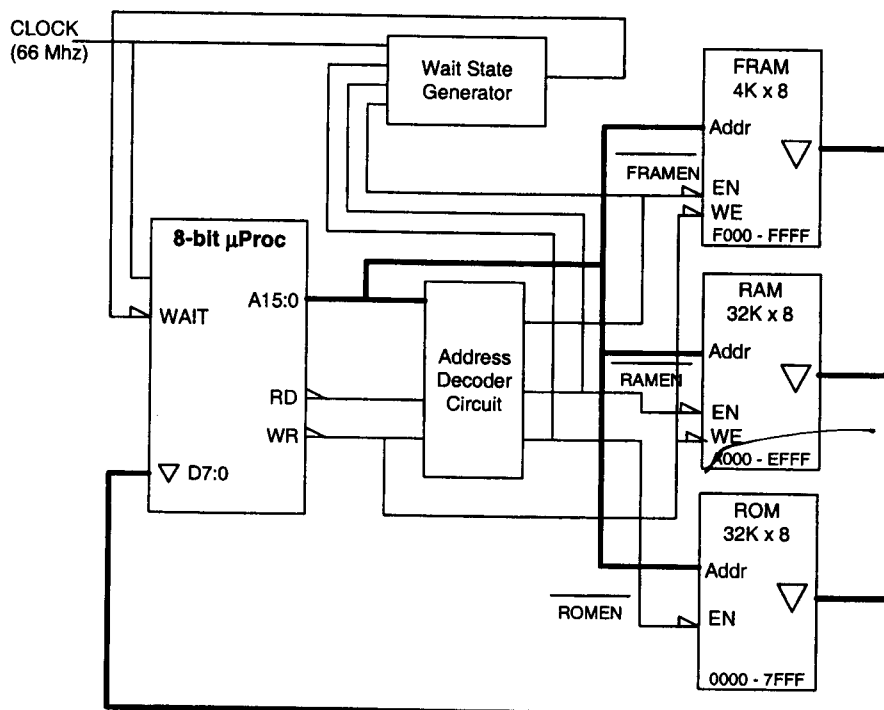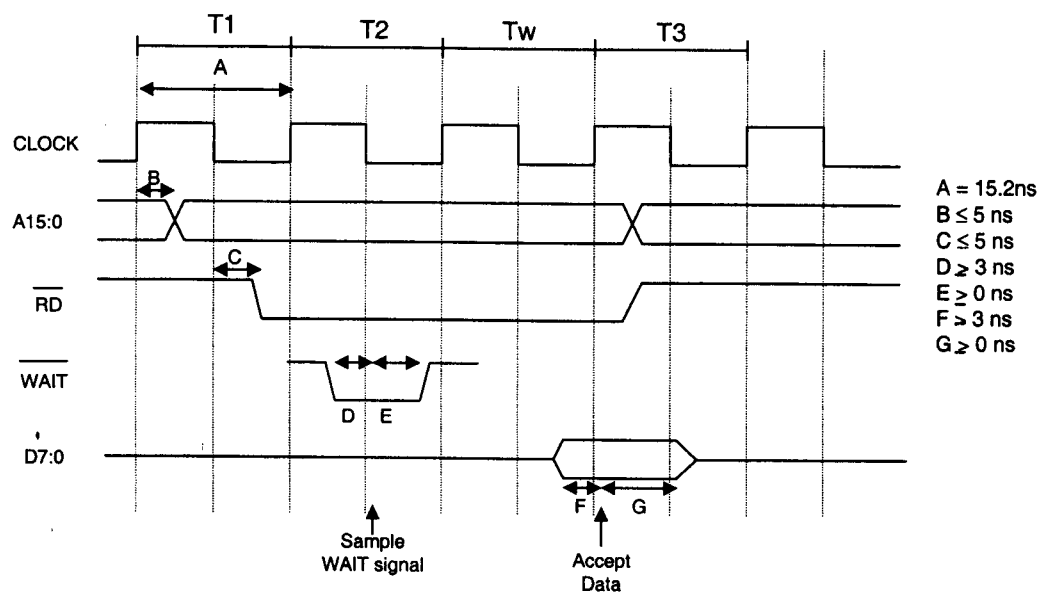
[10]

Figure 6.1

Figure 6.2

7. A digital system accepts three 8-bit unsigned data samples X, Y, Z every clock period, synchronised to the system clock signal clk. The outputs P, Q and R, which are signed 2's complement numbers, are computed according to the matrix equation:

$$\begin{pmatrix} P \\ Q \\ R \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{pmatrix} \begin{pmatrix} X \\ Y \\ Z \end{pmatrix}$$

The coefficients a_{ij} are allowed to take only the values -1, 0 and 1, coded as 2-bit numbers in 2's complement form.

Figure 7.1 shows a circuit that performs the computation. It uses nine identical processing elements (PEs), each consists of a 2-bit register preloaded with the coefficient a_{ij}, one n-bit binary adder and other circuitry.

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P Q R

a) Determine the range of P, Q and R. Hence determine the output wordlength n of the PE in order avoid overflow.

[4]

b) Design the circuit for one such PE. Assume that all a_{ij}'s are preloaded already and do not show the internal circuit of the binary adder. State the values F, G, H for your circuit.

[12]

c) Assuming that the binary adder delay is 5 ns, the delay through any two-input gate or multiplex is 1 ns, the setup and clock-to-output delay of the D flip-flop are both 1 ns, determine the maximum clock frequency for the circuit in Figure 7.1 circuit.
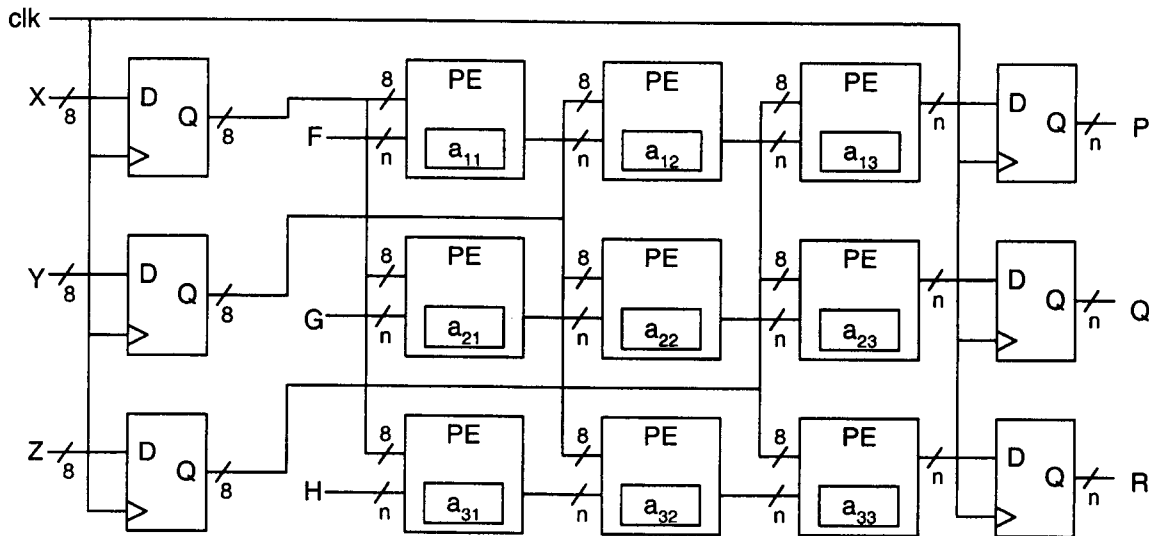
[4]

Figure 7.1

[END]