EE3-11
EE9AO8

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2012

MSc and EEE PART III/IV: MEng, BEng.and ACGI

Corrected Copy
Q3 d iii)

ADVANCED ELECTRONIC DEVICES

Tuesday, 1 May 2:30 pm

Time allowed: 3:00 hours

There are FIVE questions on this paper.

Answer Question One and THREE other questions.

Question One carries 40 marks. All other questions carry 20 marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : K. Fobelets, K. Fobelets
Second Marker(s) : S. Lucyszyn, S. Lucyszyn

Special instructions for invigilators

Q1 is compulsory

Special instructions for students

Q1 is compulsory

Constants and Formulae

permittivity of free space:	$\varepsilon_o = 8.85 \times 10^{-12}$ F/m
permeability of free space:	$\mu_o = 4\pi \times 10^{-7}$ H/m
intrinsic carrier concentration in Si:	$n_{i\,Si} = 1.45 \times 10^{10}$ cm^{-3} at T = 300K
intrinsic carrier concentration in GaAs:	$n_{i\,GaAs} = 1.79 \times 10^{6}$ cm^{-3} at T = 300K
intrinsic carrier concentration in InAs:	$n_{i\,InAs} = 1 \times 10^{15}$ cm^{-3} at T = 300K
dielectric constant of SiO_2:	$\varepsilon_{ox} = 4$
dielectric constant of Si:	$\varepsilon_{Si} = 12$
electron affinity of Si	$\chi_{Si} = 4.05$ eV
electron affinity of GaAs	$\chi_{GaAs} = 4.1$ eV
electron affinity of InAs	$\chi_{InAs} = 4.9$ eV
electron affinity of AlAs	$\chi_{AlAs} = 3.6$ eV
effective density of states of Si:	$N_{C\,Si} = 2.8 \times 10^{19}$ cm^{-3}
	$N_{V\,Si} = 1.04 \times 10^{19}$ cm^{-3}
effective density of states of GaAs:	$N_{C\,GaAs} = 4.7 \times 10^{17}$ cm^{-3}
	$N_{V\,GaAs} = 9.0 \times 10^{18}$ cm^{-3}
effective density of states of InAs:	$N_{C\,InAs} = 8.7 \times 10^{16}$ cm^{-3}
	$N_{V\,InAs} = 6.6 \times 10^{18}$ cm^{-3}
thermal voltage:	kT/e = 0.026V at T = 300K
charge of an electron:	$e = 1.6 \times 10^{-19}$ C (1 eV)

$$p = N_v e^{(E_v - E_F)/kT}$$
$$n = N_c e^{(E_F - E_c)/kT}$$

Carrier density

$$I_{DS} = \frac{\mu C_{ox} W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right)$$

MOSFET current

$$V_{th} = \phi_m - \phi_s + 2\times\phi_F + \gamma \times \sqrt{2\times\phi_F}$$

Threshold voltage

$$\phi_F = \frac{kT}{e}\ln\left(\frac{N_A}{n_i}\right)$$

Fermi potential (difference between intrinsic and Fermi level)

$$\gamma = \frac{\sqrt{2e\varepsilon_s N_A}}{C_{ox}}$$

Body effect coefficient

$$J = \frac{eD_n n_p}{L_n}\left(e^{\frac{eV}{kT}} - 1\right) + \frac{eD_p p_n}{L_p}\left(e^{\frac{eV}{kT}} - 1\right)$$

Diode diffusion current density

$$V_{bi} = \frac{kT}{e}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Built-in voltage pn diode

$$W_{depl}(V) = \left[\frac{2\varepsilon(V_{bi} - V)}{e}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]^{1/2}$$

Depletion width in pn diode

$$S = \frac{dV_{GS}}{dLog(I_{DS})}$$

Sub-threshold swing

Semiconductor material parameters

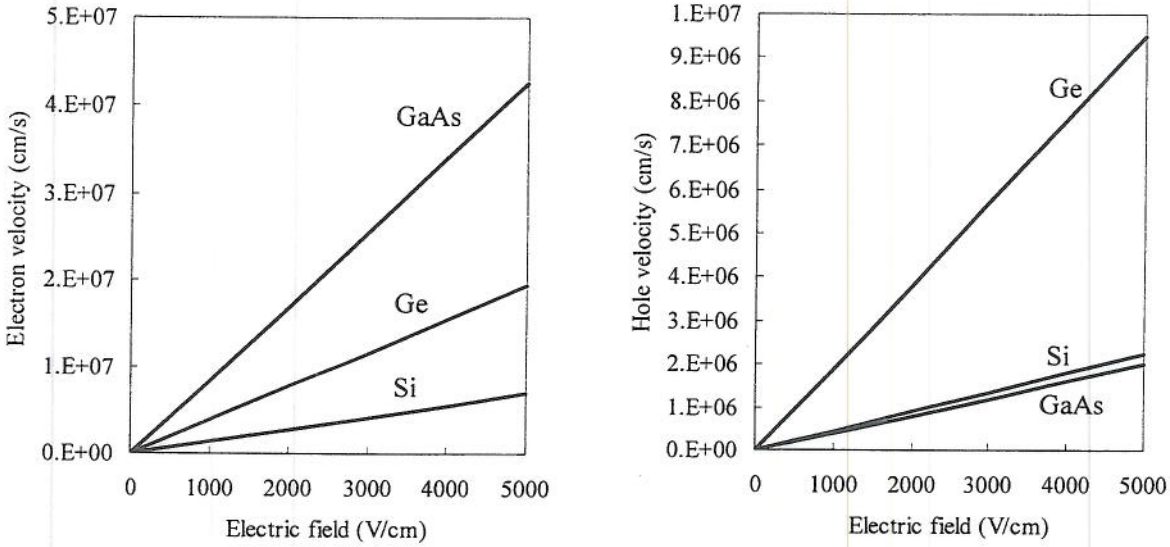

Figure A: Velocity Field curves of GaAs, Ge and Si for electric fields lower than the critical electric field.

1. Compulsory question.

a) Give the names and the mathematical expressions for the majority and minority carrier concentrations in an n-type semiconductor at room temperature. Define all variables used. [4]

b) Sketch the material cross section of a long gate length n-channel enhancement mode MOSFET in saturation. The electric field across the channel is smaller than the critical electric field for velocity saturation. Indicate the different doped regions, inversion and depletion region and ensure that relative widths are correct. [6]

c) Use an energy band diagram (E_c, E_v, E_G, E_F) to explain drain induced barrier lowering (DIBL) in short gate length n-channel MOSFETs. [6]

d) Explain why a weak inversion current flows through an n-channel MOSFET biased with a gate voltage lower than the threshold voltage. Use a material cross section and appropriate energy band diagrams (E_c, E_v, E_G, E_F). [6]

e) The transfer characteristic of an n-channel MOSFET in the triode region is given in Figure 1.1. Explain, using the necessary graphs, how the threshold voltage, V_{th} can be extracted from this characteristic. [6]

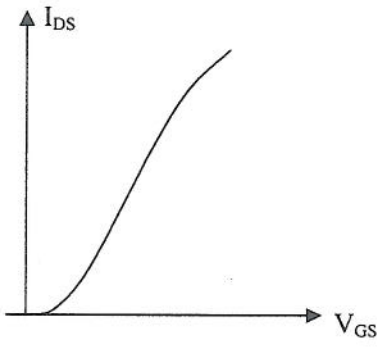

Figure 1.1: The transfer characteristic of a MOSFET in the triode region.

f) Put the following long channel FETs, all with the same gate length and width, in order of their speed performance (fastest to slowest): Si n-channel MOSFET ; Ge n-channel JFET ; GaAs n-channel MESFET ; and AlGaAs/GaAs n-channel HEMT. Use Fig. A on p.3. Which of these FETs do you expect to have the lowest input resistance and why? [6]

QUESTION CONTINUES ON NEXT PAGE!

g) In Figure 1.2 the bandgap energy is given as a function of lattice constant for three different alloys.

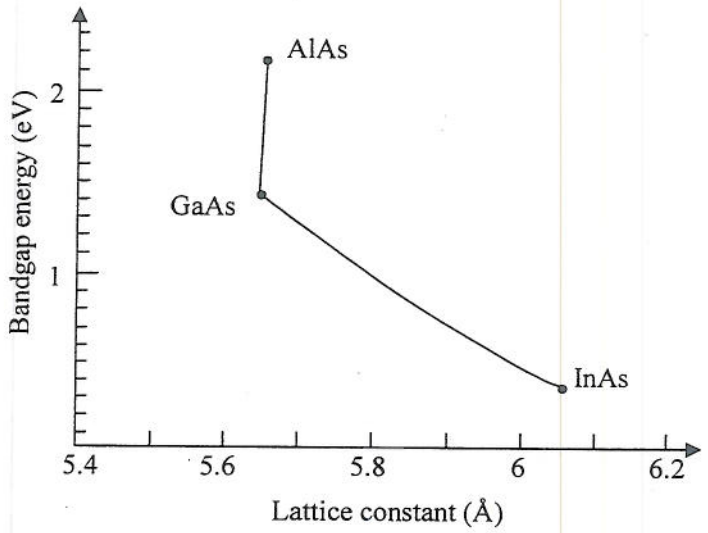

Figure 1.2: Bandgap energy as a function of lattice constant in Ga-containing alloys.

i) Use Figure 1.2 to estimate the lattice constant and bandgap of $In_{0.2}Ga_{0.8}As$ and $Al_{0.5}Ga_{0.5}As$. [2]

ii) Will a thin layer of $In_{0.2}Ga_{0.8}As$, epitaxially grown on a thick layer of $Al_{0.5}Ga_{0.5}As$ be under tensile or compressive strain? Explain briefly why. [2]

iii) Which layer will be best for the quantum well of a HEMT (high electron mobility transistor) if a heterojunction as proposed in ii) is used? Explain briefly why. [2]

2.

a) Sketch the energy band diagram (E_c, E_v, E_G, E_F) from the gate to substrate of an n-channel MOSFET under a small positive gate voltage, V_{GS}. Indicate the following parameters on this graph: the intrinsic level E_i ; the Fermi potential $\phi_F = (E_i - E_F)/e$; the surface potential V_s ; and the voltage drop across the oxide V_{ox}. Ensure that all energy differences in this plot are consistent.

[5]

b) Derive expressions for the electron and hole concentrations, respectively n, p as a function of the intrinsic carrier concentration n_i and the Fermi potential ϕ_F.

[4]

c) Derive the expression for the surface charge n_s at the interface between the gate oxide and the semiconductor as a function of the surface potential V_s, Fermi potential ϕ_F and doping concentration in the substrate N_A.

[5]

d) The surface carrier density n_s, as a function of the surface potential V_s is given in Figure 2.1.

i) Define the regions I, II, III and IV in terms of degree of inversion. [4]

ii) Give the expression for the surface charge in two surface voltage points: $V_s = \phi_F$ and $V_s = 2\phi_F$. [2]

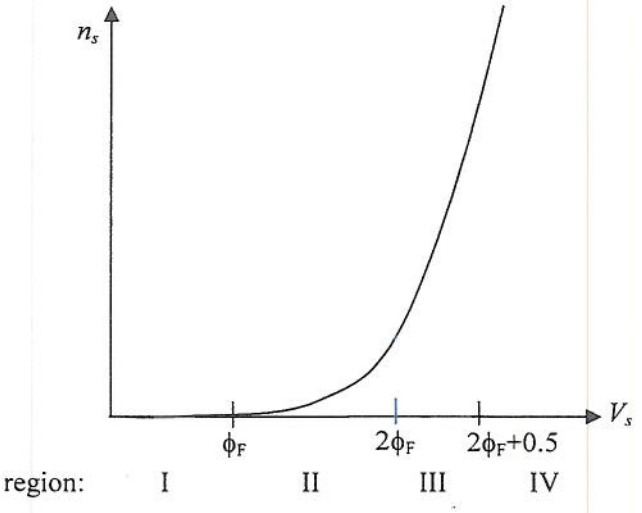

Figure 2.1: The surface carrier density n_s as a function of the surface potential V_s.

3. Figure 3.1 gives the variation of the electron velocity as a function of electric field for carriers travelling in silicon and gallium-arsenide.

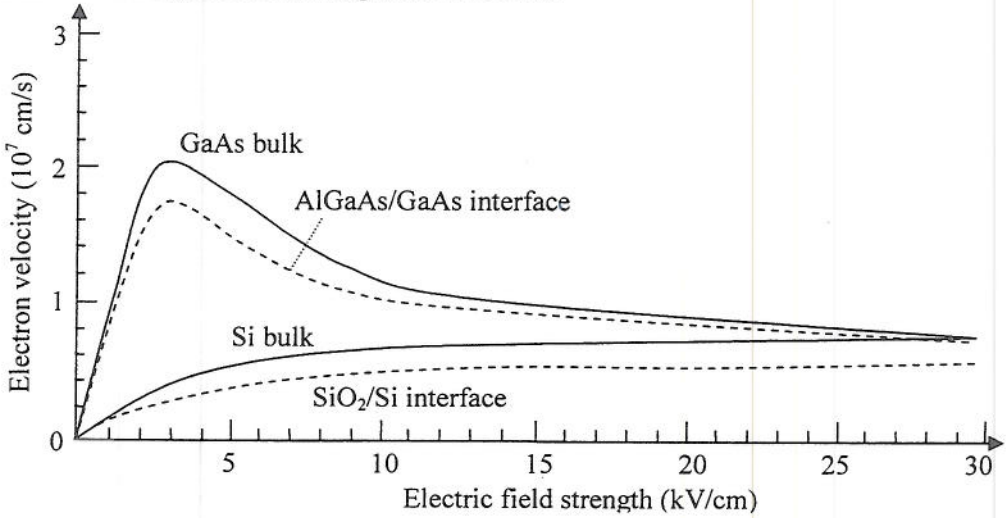

Figure 3.1: The electron velocity as a function of the electric field for different semiconductors (full lines) and different interfaces (dashed lines).

a) Extract an approximate mobility value for the electrons, μ_n in bulk Si and bulk GaAs from the graphs in Figure 3.1. Show your working out. [4]

b) Explain why the mobility of the electrons at the SiO_2/Si interface is different from that in bulk Si. [4]

c) Explain why GaAs has a region of negative differential mobility. [4]

d) An n-channel MOSFET of type 1 reaches the saturation region due to pinch-off. An n-channel MOSFET of type 2 reaches saturation due to velocity saturation. The devices are identical apart from the difference in saturation condition.

i) Sketch the output characteristics I_{DS}-V_{DS} for both MOSFETs, for a source-drain voltage region going from $V_{DS} < 0$ V to $V_{DS} > 0$ V. Explain your answer. [6]

ii) Sketch one transfer characteristic I_{DS}-V_{GS} for each FET at the same drain voltage on the same plot, indicating clearly the difference between both. [2]

4.

a) One of the techniques that can be applied to reduce short channel effects in field effect transistors is increasing the doping concentration in the substrate. Explain, using appropriate sketches and equations, why this is the case. [4]

b) In order to boost the performance of n-channel Si MOSFETs (nMOS), industry has introduced localised strain. Sketch the material cross section of an nMOS in which local strain is applied. Explain what type (tensile or compressive) of strain occurs and why this is beneficial for Si nMOS performance. [4]

c) Calculate the depletion width at the gate-semiconductor interface for a GaAs MESFET with a Ni gate contact when no bias is applied to any of the contacts. Material parameters are given in Table 1 and the list of formulae and constants on p. 2. Assume that the interface state density between Ni and GaAs is zero. [4]

Table 1: Material parameters for the MESFET

	E_G (eV)	χ (eV)	ε_r	N_D (cm^{-3})		ϕ (eV)
GaAs	1.42	4.1	14	10^{17}	Ni	5.01
InAs	0.35	4.9	15	10^{17}		

d) How would the depletion region change when GaAs is replaced by InAs and Fermi level pinning is taken into account? InAs parameters are given in Table 1 and the list of formulae and constants on p.2. Explain your answer briefly using an energy band diagram (E_c, E_v, E_G, E_F). [4]

e) The material cross section of two Schottky-gated heterojunction FETs, based on III-V materials, is given in Figure 4.1. Using the appropriate technical terms, explain why the performance of FET 1 is expected to be better than FET 2. [4]

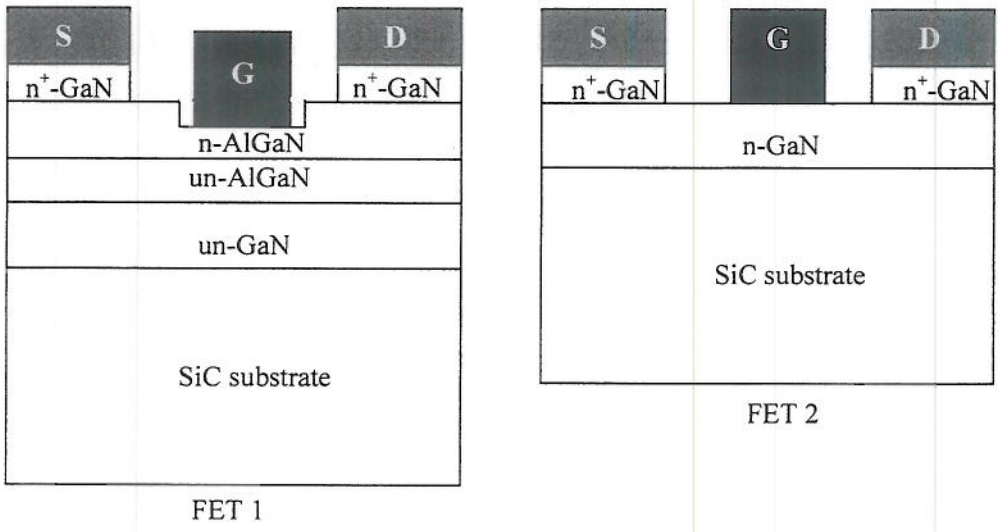

Figure 4.1: Two Schottky-gated heterojunction FETs. Left: FET 1 and right: FET2. The dimensions and doping densities are the same for both FETs.

5.

```
TITLE   A special Field Effect Transistor

MESH

X.MESH x.min=0.00  x.max=0.10  h1=0.010
X.MESH x.min=0.10  x.max=0.30  h1=0.005
X.MESH x.min=0.30  x.max=0.50  h1=0.010

Y.MESH y.min=0.00  y.max=0.10  h1=0.001
Y.MESH y.min=0.10  y.max=0.30  h1=0.005
Y.MESH y.min=0.30  y.max=0.40  h1=0.010

REGION num=1 x.min=0.00 x.max=0.50  y.min=0.00 y.max=0.40 silicon
REGION num=2 x.min=0.14 x.max=0.20  y.min=0.17 y.max=0.23 oxide

ELECTR  name=contactA x.min=0.00  x.max=0.00 y.min=0.00 y.max=0.40
ELECTR  name=contactB x.min=0.50  x.max=0.50 y.min=0.00 y.max=0.40
ELECTR  name=contactC x.min=0.15  x.max=0.19 y.min=0.18 y.max=0.22
+       VOID
COMMENT VOID removes the mesh points from the defined area

PROFILE   x.min=0.00 x.max=0.50 Y.MIN=0.00 Y.MAX=0.40
+         N-TYPE  N.PEAK=1.e16  UNIFORM
PROFILE   x.min=0.00 x.max=0.02 Y.MIN=0.00 Y.MAX=0.40
+         N-TYPE  N.PEAK=1.e20  UNIFORM
PROFILE   x.min=0.36 x.max=0.46 Y.MIN=0.00 Y.MAX=0.40
+         N-TYPE  N.PEAK=5.e17  UNIFORM
PROFILE   x.min=0.46 x.max=0.50 Y.MIN=0.00 Y.MAX=0.40
+         N-TYPE  N.PEAK=1.e20  UNIFORM

REGRID DOPING LOG IGNORE=OXIDE RATIO=2 SMOOTH=1

CONTACT  name=contactC PRINT ALUMINUM

MODELS CONMOB FLDMOB SRFMOB2

METHOD ICCG DAMPED
SOLVE
REGRID POTEN IGNORE=OXIDE RATIO=.2 MAX=1 SMOOTH=1

SYMBOLIC GUMMEL CARRIERS=1  ELECTRON
METHOD ITLIMIT=20
SOLVE  V(contactA)=0.00  V(contactB)=0.00  V(contactC)=0.00

SYMBOLIC NEWTON CARRIERS=1  ELECTRON
SOLVE  V(contactA)=0.00  V(contactB)=0.00  V(contactC)=0.00

SOLVE  V(contactC)=0.20 ELEC=contactC VSTEP=0.20 NSTEP=9

LOG IVFILE=acdc

SOLVE  V(contactB)=0.00 ELEC=contactB VSTEP=0.10  NSTEP=20
```

Go to next page for questions on this input file

a) Sketch the material cross section of the FET defined in the TCAD input file given on p. 9. Include the contacts, material and doping regions and the dimensions of each. [4]

b) The device defined in the TCAD input file is the horizontal cross section through a field effect transistor. Define which contacts act as source, drain and gate. [3]

c) The operation of this device is similar to that of a (choose one of the following):
i) n-channel MOSFET.
ii) p-channel MOSFET.
i) n-channel MESFET.
ii) p-channel MESFET. [1]

d) Sketch the data stored in the file acdc, given that the threshold voltage $V_{th} = 0.2$ V and that no velocity saturation occurs. Label axes and indicate **three** numerical values for the parameter on the x-axis. [4]

e) Compare the depletion region extending from x = 0.02 towards the middle of the device to that extending from x = 0.36 towards the middle of the device when no voltage is applied to the contacts. Use appropriate sketches that visualise the possible differences. [4]

f) Two REGRID commands are given in the input file. Explain briefly what each one does. [4]

AED_ answers 2012 Final (qs)

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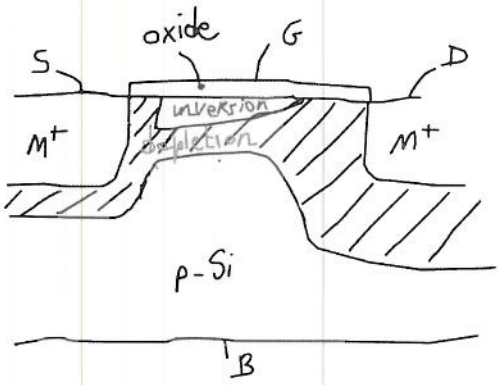
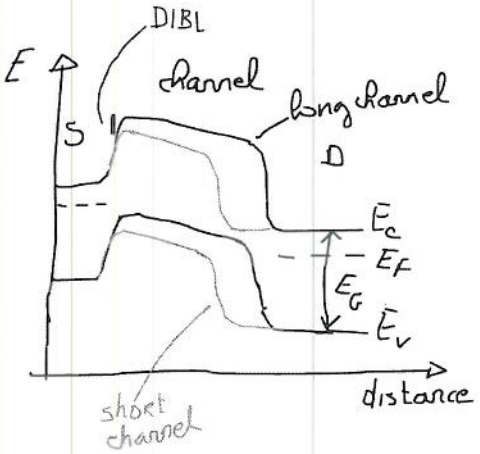
1.

a) majority carrier concentration is electrons: $n = N_D$ with N_D donor doping concentration. [4]

minority carrier concentration is holes: $p = \frac{n_i^2}{N_D}$ with n_i intrinsic carrier concentration

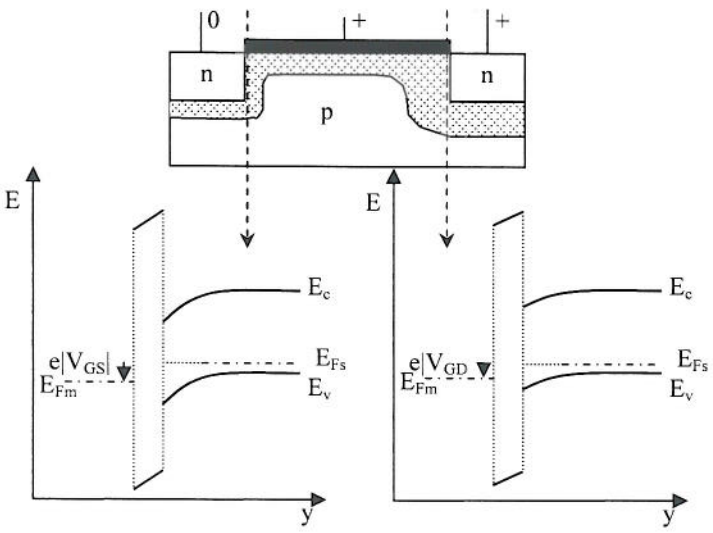


b) Important features in this drawing are: 1. an inversion layer should exist. The inversion layer should be pinched-off near the drain. There should be a depletion layer surrounding the pn junctions (inversion is an n-type material). The inversion layer should be larger at the drain size than at the source side as a positive drain potential is applied with respect to source and bulk. [6]



c) DIBL is a measure for how much the drain voltage reduces the potential barrier between the source and the channel. [6]

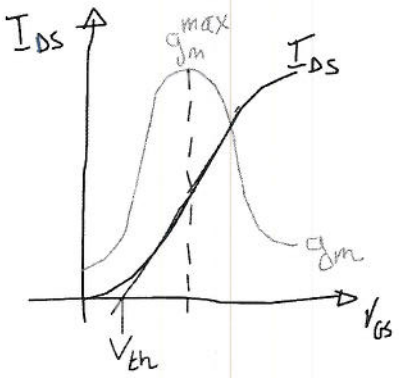
d) Weak inversion current is due to diffusion of electrons from source to drain. The reason is illustrate with the figure.



At the top of the figure, a cross section of an n-channel MOSFET is given. Since the gate voltage is smaller than the threshold voltage, there is no inversion layer. Diffusion is due to carrier concentration gradients. In order to visualise that, we can draw an energy band diagram from gate to substrate close to the source and one close to the drain. The voltage across the oxide at the source side is V_{GS}. The voltage across the oxide at the drain side is $V_{GD}=V_{GS}-V_{DS} < V_{GS}$. Since $V_{GD} < V_{GS}$ the band bending at drain side is smaller than at source side, thus the electron concentration is less at drain side than source side based on the distance between E_c and E_F at the SiO_2/Si interface. [6]

$$n = N_C \exp\left(\frac{E_c - E_F}{kT}\right)$$

e) The IV curve is in the triode region because it is linear in strong inversion. Calculate the transconductance g_m by taking the derivative of I_{DS} to V_{GS}. Drain the tangential through the point on the I_{DS}-V_{GS} characteristic where g_m is maximum. The crossing of this line with $I_{DS}=0$ gives the threshold voltage V_{th}. [6]



f) 1. AlGaAs/GaAs n-channel HEMT
2. GaAs n-channel MESFET
3. Ge n-channel JFET
4. Si n-channel MOSFET

There are two possible answers. Any of the following two are acceptable:

1. GaAs MESFET because the barrier of a Schottky gate on GaAs is lower than that of all the other gating methods.
2. Ge JFET because the intrinsic carrier concentration is high and thus the gate leakage current in the Ge pn junction is high. [6]

g)

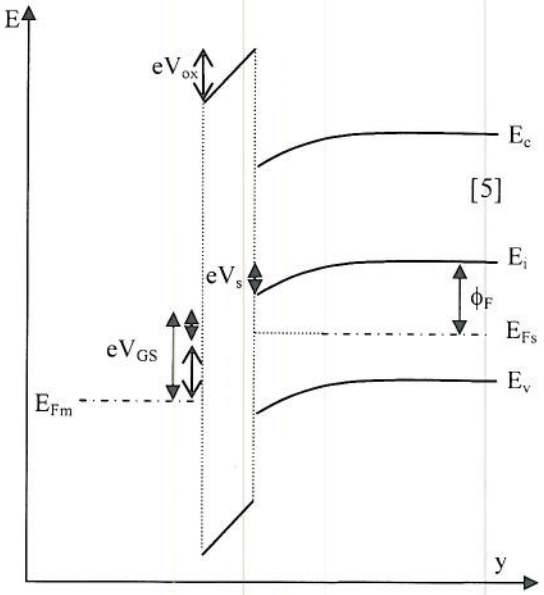
i) $In_{0.2}Ga_{0.8}As$
$E_G \approx 0.2 \times 0.32\ eV + 0.8 \times 1.4\ eV = 1.184\ eV$
$a \approx 0.2 \times 6.6\ Å + 0.8 \times 5.65\ Å = 5.84\ Å$
$Al_{0.5}Ga_{0.5}As$.
$E_G \approx 0.5 \times 2.2\ eV + 0.5 \times 1.4\ eV = 1.8\ eV$
$a \approx 5.65\ Å$ [2]

ii) Compressive strain, because the lattice constant of $In_{0.2}Ga_{0.8}As$ is larger than that of $Al_{0.5}Ga_{0.5}As$. The $In_{0.2}Ga_{0.8}As$ takes the smaller lattice constant and the atoms are therefore compressed, closer together. [2]

iii) The $In_{0.2}Ga_{0.8}As$ because it has the smallest bandgap and thus can form a quantum well in which the carriers can reside. The mobility of the electrons in $In_{0.2}Ga_{0.8}As$ is also higher than in $Al_{0.5}Ga_{0.5}As$, therefore for high speed electronics the $In_{0.2}Ga_{0.8}As$ layer is the better channel. [2]

2.

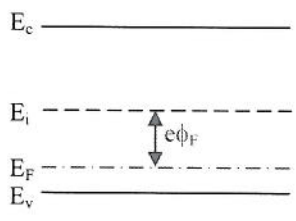
a) Important in this plot is that E_{Fm} is lower than E_{Fs} with a magnitude equal to $V_{ox}+V_s$. The intrinsic level is approximately midway between E_c and E_v. Bends should bend down. [5]



[5]

b)

p-type



$$p = N_v \exp\left(\frac{E_v - E_F}{kT}\right)$$

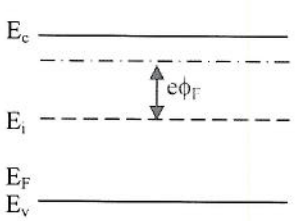
$$p_i = n_i = N_v \exp\left(\frac{E_v - E_i}{kT}\right)$$

$$\frac{p}{n_i} = \exp\left(\frac{E_v - E_F - (E_v - E_i)}{kT}\right)$$

$$\frac{p}{n_i} = \exp\left(\frac{E_i - E_F}{kT}\right)$$

$$p = n_i \exp\left(\frac{e\phi_F}{kT}\right) = n_i \exp\left(\frac{\phi_F}{V_T}\right)$$

n-type



$$n = N_c \exp\left(\frac{E_F - E_c}{kT}\right)$$

$$n_i = N_c \exp\left(\frac{E_i - E_c}{kT}\right)$$

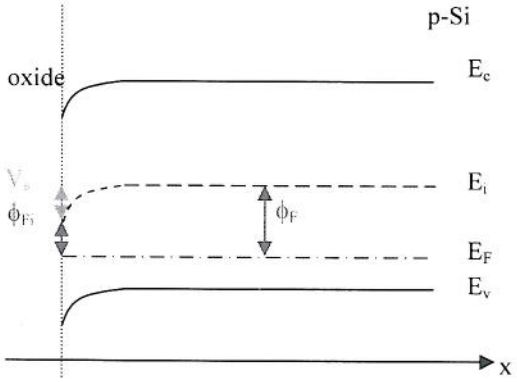
$$\frac{n}{n_i} = \exp\left(\frac{E_F - E_c - (E_i - E_c)}{kT}\right)$$

$$\frac{n}{n_i} = \exp\left(\frac{E_F - E_i}{kT}\right)$$

$$n = n_i \exp\left(\frac{-e\phi_F}{kT}\right) = n_i \exp\left(\frac{-\phi_F}{V_T}\right)$$

[4]

c)



$$n_B = n_i \exp\left(\frac{-\phi_F}{V_T}\right) \quad \& \quad n_s = n_i \exp\left(\frac{\phi_{Fi}}{V_T}\right)$$

$$\phi_{Fi} = \phi_F - V_s$$

$$n_s = n_i \exp\left(\frac{-\phi_F + V_s}{V_T}\right) \qquad n_s = N_A \exp\left(\frac{V_s - 2\phi_F}{V_T}\right)$$

$$p = n_i \exp\left(\frac{\phi_F}{V_T}\right) \quad \& \quad p \approx N_A$$

$$N_A \approx n_i \exp\left(\frac{\phi_F}{V_T}\right) \quad or \quad n_i \approx N_A \exp\left(\frac{-\phi_F}{V_T}\right)$$

[5]

d)

i) I: depletion
II: weak inversion
III: moderate inversion
IV: strong inversion [4]

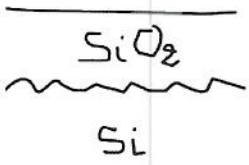
ii) $V_s = \phi_F$ $\quad n_s = N_A \exp\left(\frac{-\phi_F}{V_T}\right) = n_i$

$V_s = 2\phi_F$. $\quad n_s = N_A$ [2]

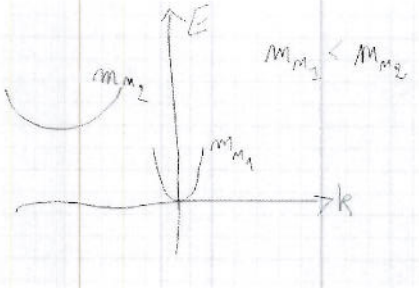
3.

a) Mobility can be extracted from the linear region using $v = \mu E$
GaAs. At $E=10^3$ V cm, $v=10^7$ cm/s: $\mu_n = 10^7/10^3$ cm^2/Vs = 10^4 cm^2/Vs
Si: At $E=1.5\ 10^3$ V cm, $v=0.2\ 10^7$ cm/s: $\mu_n = 0.2\ 10^7/(1.5\ 10^3)$ cm^2/Vs = $1.3\ 10^3$ cm^2/Vs [2]

b) The Si/SiO_2 interface is rough because the SiO_2 layer is amorphous. Electrons travelling through the channel undergo the influence of 2 electric fields, one is due to V_{DS} and accelerates the electrons in the longitudinal direction and the other one is V_{GS} which attracts the electrons to the Si/SiO_2 interface where they undergo surface roughness scattering. Since $\mu \propto \tau$, with τ the average time between scattering events, μ reduces because τ reduces as there are more scattering events. [4]

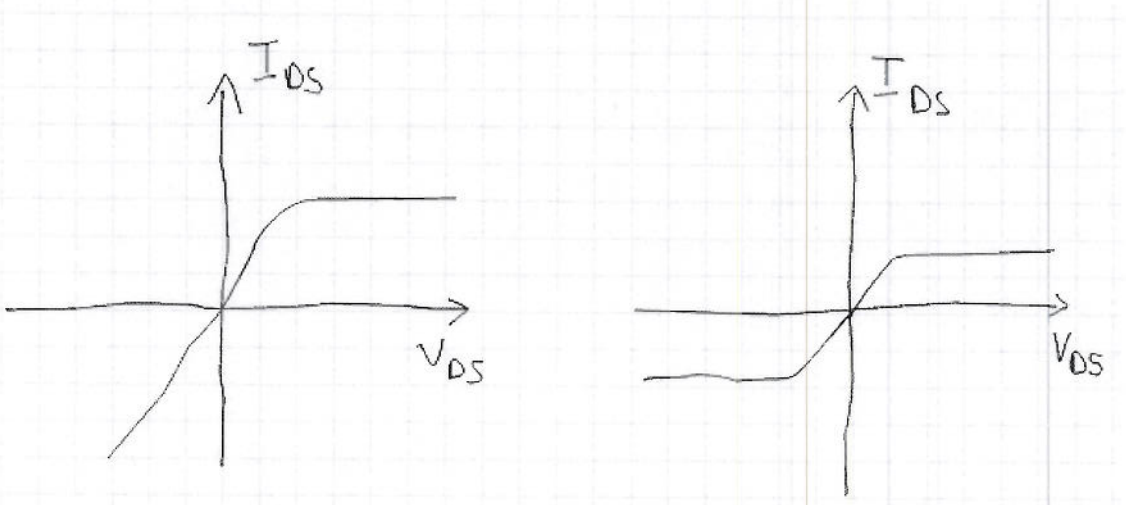


c) This feature is due to the specific conduction band diagram of GaAs. The conduction band diagram consists of two minima that are closely positioned in energy. As a consequence, at higher electric fields the electrons are distributed, with a certain ratio, between the two conduction band minima. The higher lying band has a higher effective mass than the lower lying band. The total effective mass is the weighted sum (based on the fraction of electrons in each band) of the effective masses in each band. When the electron population in the higher lying band increases, its effective mass will gain in importance and, as a result, the overall electron velocity reduces. Note: the velocity of the electrons is inversely proportional to the effective mass. [4]



d) An n-channel MOSFET of type 1 reaches the saturation region due to pinch-off.
An n-channel MOSFET of type 2 reaches saturation due to velocity saturation. The devices are identical apart from the difference in saturation condition.

i) [6]

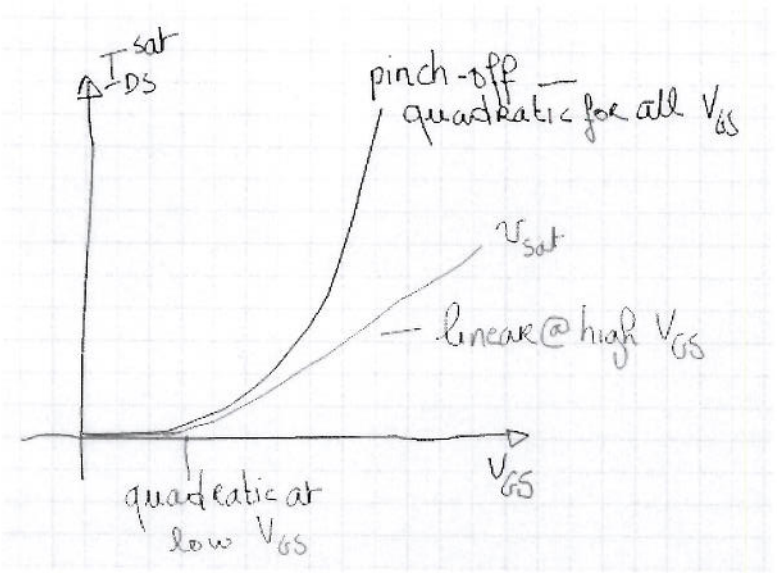


The left graph illustrates the case of pinch-off. Pinch-off occurs when the critical electric field for velocity saturation has not been reached while the pinch-off condition has been reached. In this case there is no saturation in the $V_{DS}<0$ region because the pinch-off condition cannot be achieved. Pinch-off condition: $V_{DS} = V_{GS} - V_{th}$, with $V_{GS}>V_{th}>0$ thus $V_{GS} - V_{th} > 0$ for an enhancement mode nMOS. Thus this can never be negative and therefore $V_{DS}<0$ cannot have pinch-off.

The right graph is for velocity saturation. If it is drawn for the same V_{GS} value as the left one, then the currents should be smaller. Now saturation occurs in both bias directions because the condition

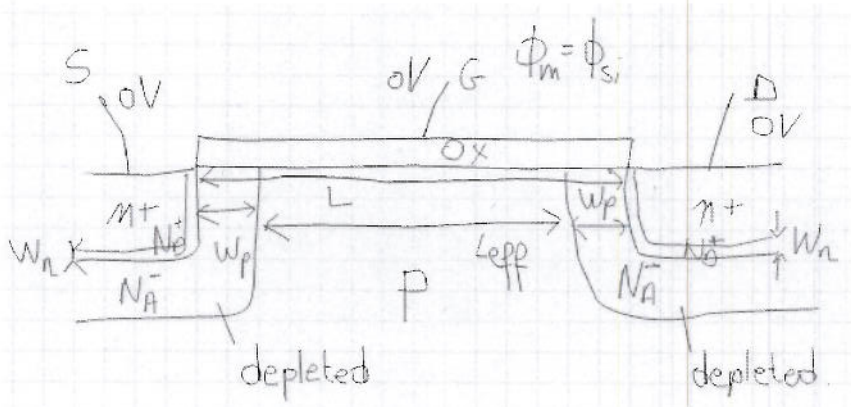
for saturation is the absolute value of the electric field that causes the velocity to saturate. $I_{DS} \propto (V_{GS} - V_{th}) \times v_{sat}$, v_{sat} is the saturation velocity and is constant.

ii) . [4]

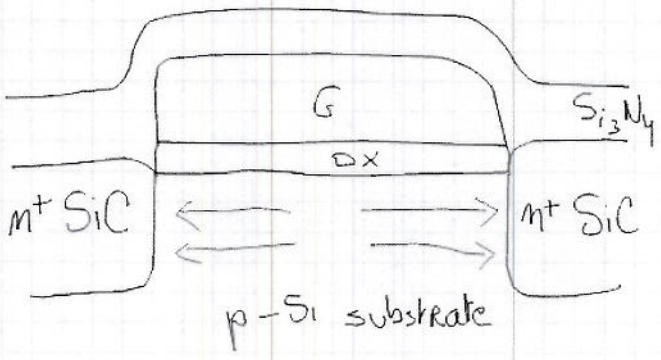


4.

a) SCEs are mainly due to the depletion from the source and the drain towards the channel region. The width of these depletion regions are negligible compared to the total gate length in long gate length devices, but become comparable to the gate length in short gate length devices (effective gate length $L_{eff} < L$ designed gate length). As a consequence, techniques that limit the extend of the depletion width from source and drain into the channel region will limit SCEs. One way to reduce the depletion from the highly doped source and drain region into the channel region is by increasing the doping density in the channel. This can be explained based on charge neutrality. Charge neutrality around the contact-channel n^+p junction gives:
$eAW_nN_D = eAW_pN_A$ or $W_nN_D = W_pN_A$. This equation shows that the depletion width extends into the lowest doped region, thus the p-type channel region. Therefore increasing N_A will reduce the extend of the depletion width W_p into the channel. Parameters are defined on the sketch where all voltages are taken zero. [4]



b) In the local strain approach, the strain is introduced via epitaxially grown stressors in source and drain that have a smaller lattice constant than Si and a silicon nitride top stressor that is under tensile strain. For nMOS, the strain introduced is tensile: the Si channel is under tensile strain. The benefit of tensile strain in the Si channel is an increase of the electron mobility due to a reduction of the effective mass of the electrons in the tensile strained channel (electrons reside in the Δ2 conduction band minima only). There is also a quantum well channel formed between tensile strained Si and unstrained Si underneath. Thus the electrons in the channel sit in a shallow quantum well, this reduces leakage currents through the substrate. [4]



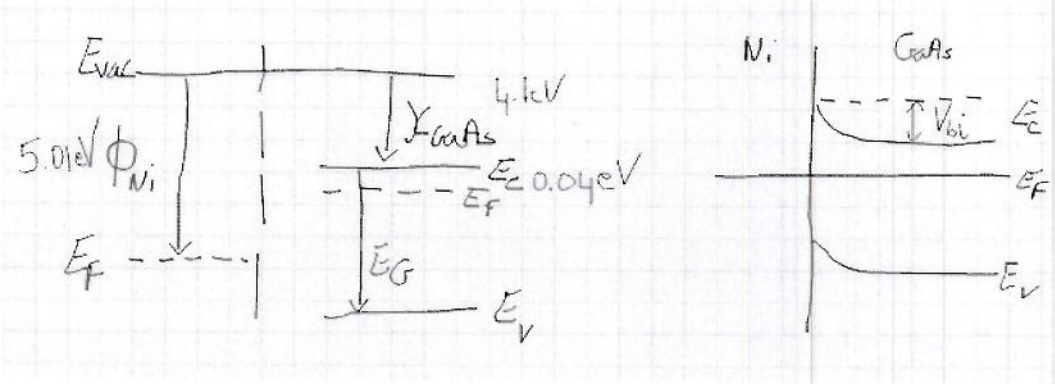
c) The depletion width can be calculated from the one-sided junction calculations in which it is assumed that $N_A >> N_D$. Simplifying the depletion equation found in the formulae list gives:
$W_n = \sqrt{\frac{2\varepsilon(V_{bi}+V_r)}{e}\frac{1}{N_D}} = \sqrt{\frac{2\,\varepsilon_0\,\varepsilon_{GaAs}\,V_{bi}}{e\,N_D}}$ with $V_r = 0$V and V_{bi} can be derived from the sketch of an energy band diagram. Since the work function of GaAs is not given we need to calculate it based on doping density and the knowledge of the electron affinity. Formulae from the list can be used.

$$n = N_C \exp\left(\frac{-(E_c - E_F)}{kT}\right)$$

$$N_D = N_C \exp\left(\frac{-(E_c - E_F)}{kT}\right)$$

$$E_c - E_F = kT \ln\left(\frac{N_C}{N_D}\right) = 0.026 \ln\left(\frac{4.7\,10^{17}}{10^{17}}\right) = 0.04eV$$

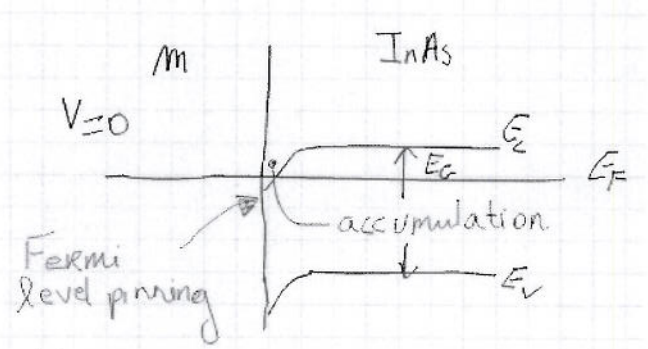
$$\phi_{GaAs} = \chi_{GaAS} + E_c - E_F = 4.14eV$$



$$V_{bi} = \phi_{Ni} - \phi_{GaAs} = 5.01 - 4.14 = 0.87eV$$

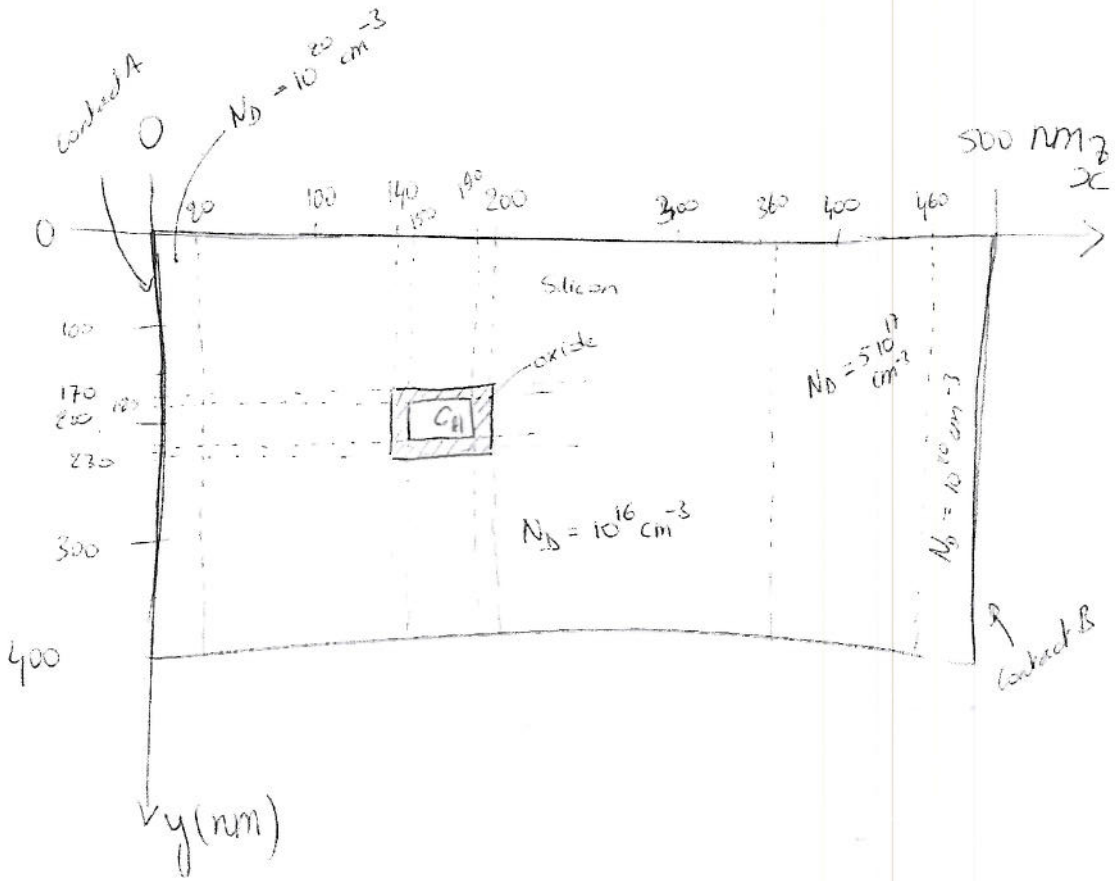
$$W_n = \sqrt{\frac{2 \times 14 \times 8.85 \times 10^{-14}(F/cm) \times 0.87V}{1.6 \times 10^{-19} C \times 10^{17} cm^{-3}}} = 1.16 \times 10^{-5} cm$$ [4]

d) The interface states at the InAs surface causes the Fermi level to pin above the conduction band of InAs. As a consequence the surface is not in depletion but in accumulation (increase of majority carrier electrons). Thus the depletion region at the surface is zero and no Schottky contact can be made. [4]



e) FET1 is a modulation doped field effect transistor. This means that the doping atoms (here sitting in n-AlGaN) are separated from the channel region (in undoped GaN). Due to the larger bandgap of AlGaN than GaN, diffusion of electrons from n-AlGaN happens and populates the quantum well channel in the un-GaN. This reduces impurity scattering, increasing the mobility of the carriers in the un-GaN channel. FET1 also has a buried channel. Thus the un-GaN channel is removed from the surface. This reduces surface scattering effects and removes the problem of Fermi level pinning allowing an improve Schottky barrier height and reduced gate leakage.
FETs is a MESFET with a surface channel and impurity doping in the channel region. Its advantage is the less complex material structure and fabrication.
Thus FET1 is expected to have improved performance because of increased carrier mobility and reduced gate leakage. [4]

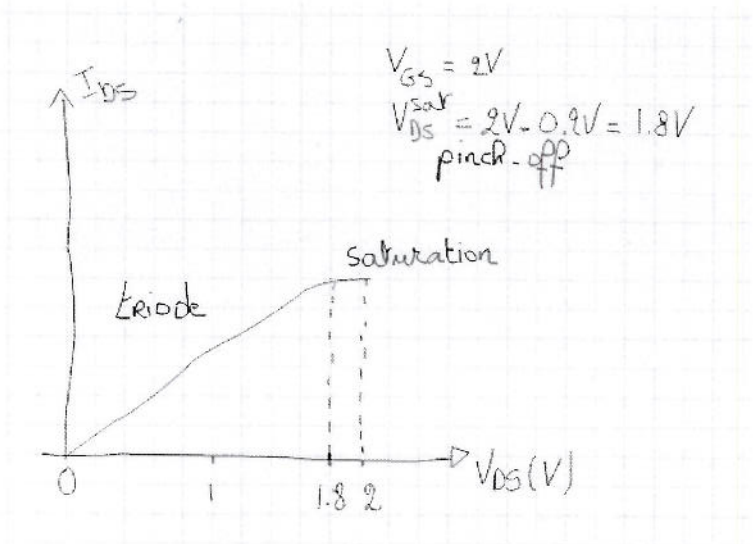
5.a) [4]



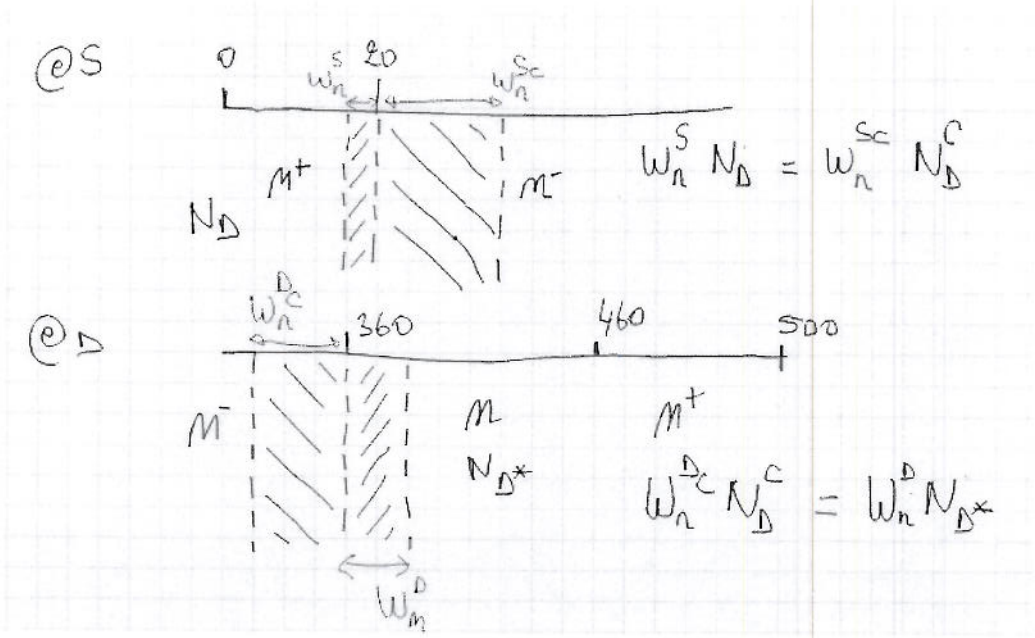
b) Contact A: Source, contact B: drain and contact C: gate [3]

c) i) n-channel MESFET. [1]

d) $V_{GS} = 2V$, V_{DS} (max) = 2V.. [4]



e) Sketch of the depletion regions at the source and at the drain. [4]



Note that $N_D > N_{D^*} > N_D^c$. As a result of charge neutrality (see equations in pictures) we know that the depletion width extends in the lowest doped region and that the extension is proportial to the ratio of doping concentrations. Therefore: $W_n^{Sc} > W_n^{Dc}$ because the ratio of doping concentration across the junction at the source side is larger than that at the drain side.

f) The first REGRID works on doping and increases the number of mesh points where the doping changes in the input file. [4]
The second REGRID works on potential variations, first the Poisson equation is solved which gives the variations of the potential (electric field). Everywhere where there is a strong variation of this parameter the number of mesh points is increased.