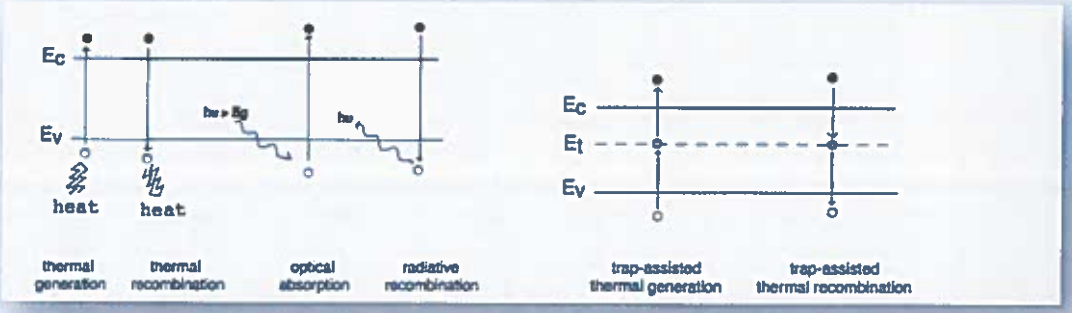
Answers:

1(a)



3 marks for each process and diagram

Trap-assisted/Shockley-Read-Hall is dominant as (i) thermal regeneration is improbable due to the low probability of thermal excitation across the gap (ii) indirect bandgap of silicon means radiative recombination is unlikely.

2 marks

Note: Auger can also be included, though improbable unless high fields are available for intermediate state excitation.

[Bookwork and analysis]

(b)

From diffusion current:

$$I = -DAe\, d\Delta c/dx$$

where Δc is the excess carrier concentration.

1 mark

From formula sheet:

$$c = c_0 \exp\left(\frac{eV}{kT}\right) \text{ with } \begin{cases} c = p_n \text{ or } n_p \\ c_0 \text{ bulk minority carrier concentration} \end{cases}$$ Minority carrier injection under bias

$$\delta c = \Delta c \exp\left(\frac{-x}{L}\right) \text{ with } \begin{cases} \delta c = \delta p_n \text{ or } \delta n_p \\ \Delta c \text{ the excess carrier concentration} \\ \text{at the edge of the depletion region} \end{cases}$$ Excess carrier concentration as a function of distance when recombination occurs – long layer

Hence from diffusion current at the edge of the depletion region gives, for electrons:

$$d\Delta n/dx = -\Delta n/L_n\, e^{-x/L_n}$$

1 mark

which for $x = 0$ is

$$d\Delta n/dx = -\Delta n/L_n.$$

1 mark

Hence from

$$I_n = -D_n A e \, d\Delta n/dx$$
$$= D_n A e \, \Delta n / L_n.$$

1 mark

The excess carrier concentration is caused by injection across the junction:

$$\Delta n = n_{po} e^{-eV/kT} - n_{po}$$
$$= n_{po}(1 - e^{-eV/kT})$$

1 mark

giving

$$I_n = D_n A e \, n_{po}(1 - e^{-eV/kT})/L_n$$

1 mark

and similarly for holes:

$$I_p = D_p A e \, p_{no}(1 - e^{-eV/kT})/L_p$$

1 mark

Hence from

$$I_{tot} = I_s[\exp(eV/kT) - 1].$$

$$I_s = eA\left(\frac{n_{p0}D_n}{L_n} + \frac{p_{n0}D_p}{L_p}\right)$$

2 marks

Assumptions: long-diode approximation, namely the layers are much thicker than the diffusion length

1 mark

[Bookwork and analysis]

(c) Formulae for excess charge:

$$Q_n = -eA\int_{-\infty}^{0} \delta n_p \, dx$$

$$Q_p = eA\int_{0}^{\infty} \delta p_n \, dx$$

1 mark

From formula sheet:

$$i(t) = \frac{Q(t)}{\tau} + \frac{dQ(t)}{dt}$$

Steady state so $dQ/dt = 0$.

1 mark

1 mark

Substitute in previous terms and integrate:

$$I_n = \frac{Q_n}{\tau_n} = \frac{eAL_n\Delta n_p}{\tau_n}$$
$$I_p = \frac{Q_p}{\tau_p} = \frac{eAL_p\Delta p_n}{\tau_p}$$

2 marks

Hence $D_{n,p}/L_{n,p} = L_{n,p} / \tau_{n,p}$

So
$L_{n,p} = \sqrt{(D_{n,p}\ \tau_{n,p})}$

1 mark

Can cross-check with formula sheet:

$$L = \sqrt{D\tau}$$

[Analysis]

2.
a)
a: gate contact
b: drain contact
c: gate oxide
d: source n+
f: substrate p
f1: channel
e: drain n+

h: source contact
i: gate contact
j: gate oxide
k: source n+
l: p-doped,
l1, channel, under gate
m: n-
m1: drift region, under gate
N: n+ doped drain

Lose one mark for each wrong (up to 8 max)

[Bookwork and analysis]

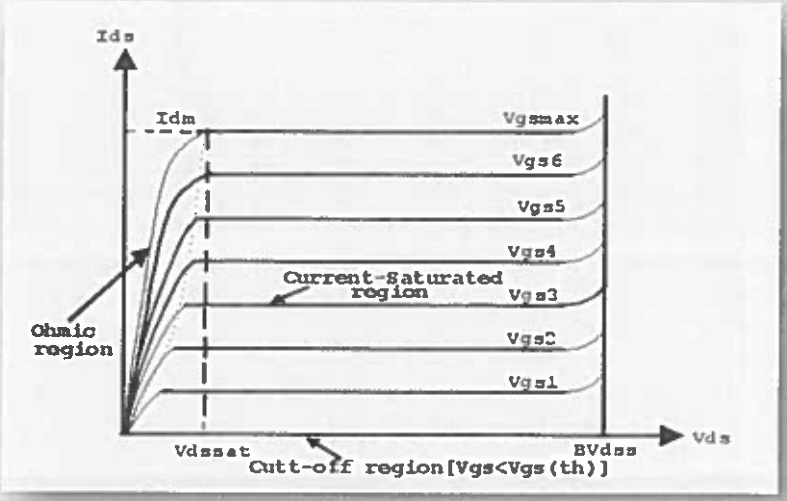
Note, students are not used to the DMOS repeat unit as drawn and so have to adapt their identification of the regions accordingly to the functionality.

b) Ohmic. *1 mark*
To ensure *p* region is grounded and hence parasitic BJT is not active.
2 marks
[Analysis]

c) As the width is decreased, the channel in the lateral MOSFET gets shorter, but is unaffected in the vertical DMOS. Hence in the MOSFET the whole channel can become depleted (punch-through), and high fields will be created when turned off leading to low breakdown voltages. The independence of channel length with lateral width means the DMOS geometry avoids these problems.
3 marks

The oxide is thicker as the voltages are higher
1 mark

[Analysis]
d)



2 marks for curves, 2 marks for labeling

[Bookwork]