IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2014

EEE PART I: MEng, BEng and ACGI

Corrected Copy

ANALOGUE ELECTRONICS 1

Wednesday, 11 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : A.S. Holmes
Second Marker(s) : C. Papavassiliou

The Questions

1. For each part of this question, state clearly any assumptions made in your calculations.

   a) For the circuit in Figure 1.1, choose the value of R_B to give a bias voltage of +2.5 V at the collector of the transistor.

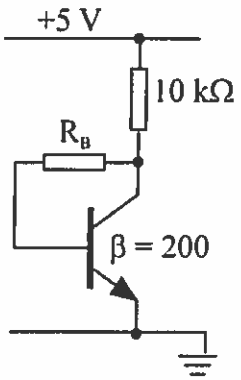

Figure 1.1

[6]

   b) For the amplifier in Figure 1.2, derive an expression for the large-signal relationship between the differential input voltage, $V_D = V_{IN1} - V_{IN2}$, and the differential output voltage V_{OUT} when both transistors are active, and show that it can be expressed in the form $V_{OUT} = 5\tanh(20V_D)$. Hence or otherwise determine the double-ended, small-signal differential gain of the amplifier. You should neglect base currents and assume $r_o \rightarrow \infty$.

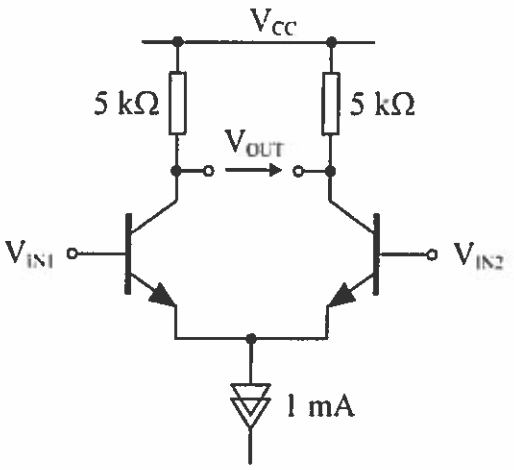

Figure 1.2

[10]

   c) A simple current mirror is formed from a matched pair of BJTs for which β = 100 and V_A = 120 V. Calculate the output voltage at which the input and output currents will be identical.

[6]

Question 1 continues on the next page...

Question 1 continued

d) For the circuit in Figure 1.3, determine the value of the supply voltage V_{DD} if the MOSFET is at the pinch-off point.

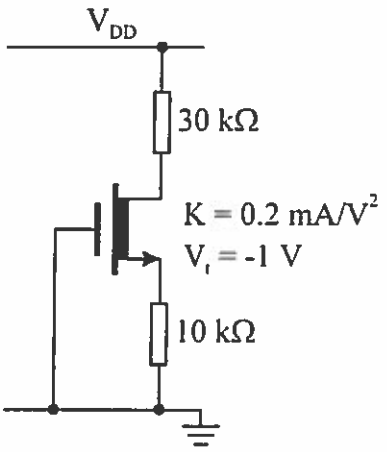

Figure 1.3 [6]

e) A rectangular input pulse of amplitude 5 V and duration 200 μs is applied to the circuit in Figure 1.4. Assuming the input had previously been at 0 V for a long time, draw a dimensioned sketch showing the variation of V_{OUT} over a period of 500 μs starting 100 μs before the rising edge of the pulse.

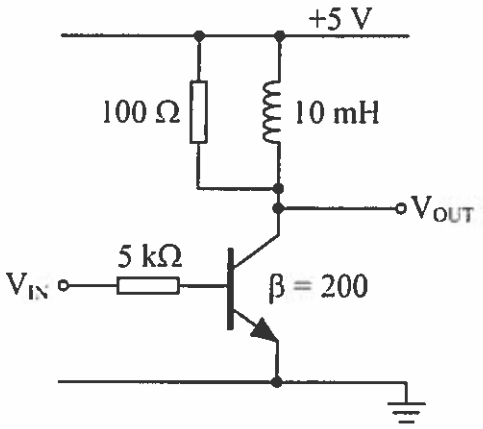

Figure 1.4 [8]

f) Sketch the schematic of a Darlington pair compound transistor, and derive an expression for the overall current gain in terms of the current gains of the individual transistors. [4]

2. Figure 2.1 shows a single-stage amplifier in which a depletion MOSFET provides the active load for an enhancement MOSFET.

a) Determine the quiescent values of the drain current and the output voltage, and verify that both MOSFETs are in the active region under quiescent conditions. Also calculate the minimum supply voltage for which both transistors will remain active in the absence of an input signal. [9]

b) Draw a small-signal equivalent circuit for the amplifier, and hence determine its small-signal voltage gain in the mid-band. Your analysis should take into account the bias resistors. [9]

Also calculate the mid-band small-signal input resistance of the circuit, and hence choose the value of input capacitor C such that the cut-off frequency at the lower end of the mid-band occurs at 100 Hz. [5]

c) The amplifier is used to drive a capacitive load of 150 pF. Sketch a Bode plot showing the frequency dependence of the in-circuit gain in this case. Your plot should cover the frequency range 10 Hz to 100 kHz. [7]

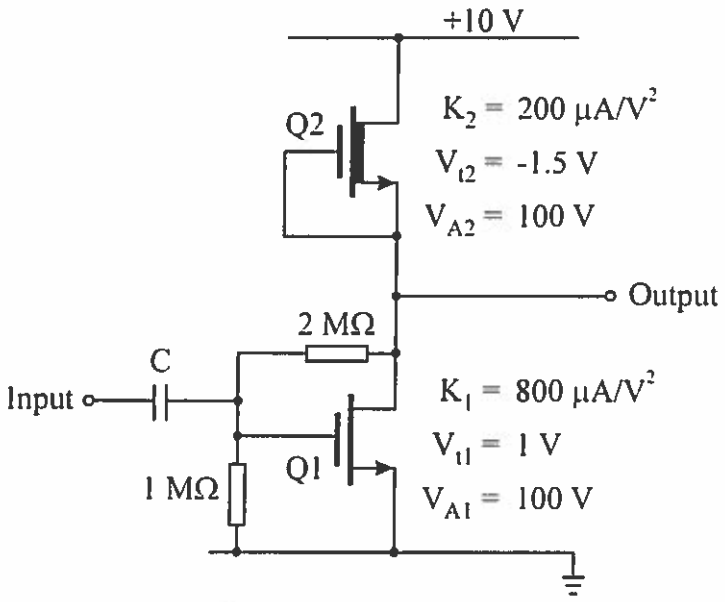

Figure 2.1

3. a) Sketch the circuit diagram for a Class B push-pull output stage. Also sketch the input-output relationship for such a circuit and highlight its key features. [10]

b) Figure 3.1 shows a Class AB output stage in which diode-connected transistors Q1 and Q3 are used to generate bias voltages for the output transistors Q2 and Q4. The transistors Q2 and Q4 are a matched pair, as are the transistors Q1 and Q3. All transistors have $\beta = 100$.

By considering just the upper half of the circuit, and neglecting base currents, show that, when Vout = 0, the currents I_1 and I_2 are related as follows:

$$I_2 \exp(I_2 R / V_T) = N I_1$$

where $N = I_{S2}/I_{S1}$ is the ratio of the saturation currents of Q2 and Q1, and V_T is the thermal voltage. If $I_{S1} = 0.05$ pA and $I_{S2} = 0.5$ pA, what value of R will give a collector bias current of 10 mA in the output transistors? [10]

c) Calculate the base-emitter voltages of Q1 and Q2 when the circuit is delivering an output voltage of 5 V to a 50 Ω load. Hence determine the input voltage in this case, and the voltage gain Vout/Vin, assuming the value of R you calculated in part b). You may assume that Q4 is carrying negligible current. [7]

d) Repeat the gain calculation of part c) for an output voltage of 10 V. Considering the two values you have calculated, comment on the linearity of the output stage. [3]

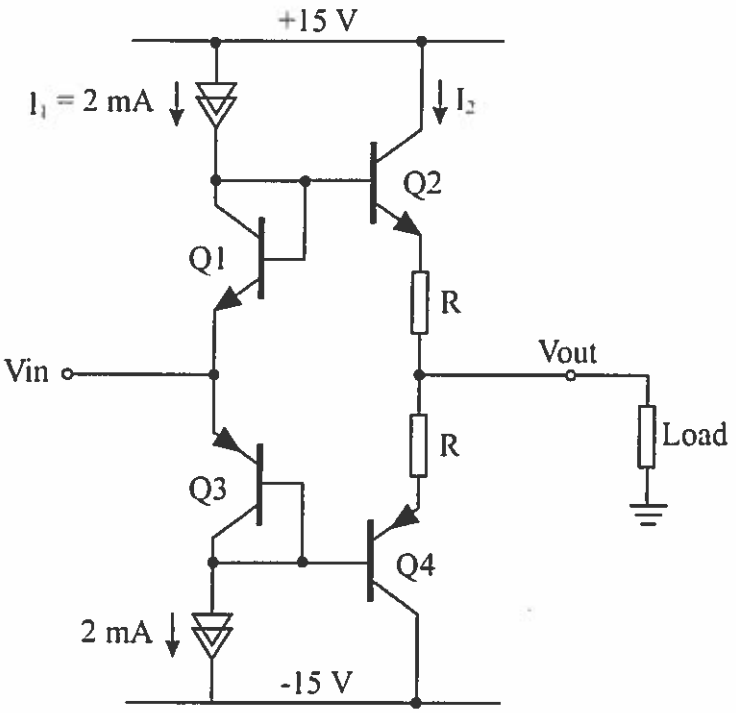

Figure 3.1