# E3-01 Exam Paper 2014 Solutions

## Q1

**1.a)** Self biased PTAT current source with start-up circuit

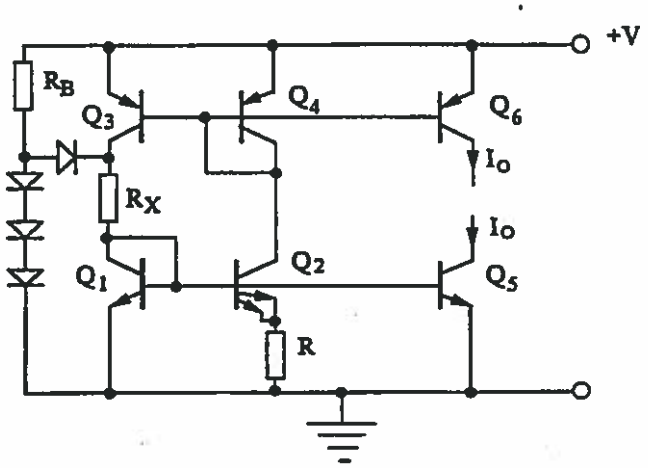


Figure 1. Answer to 1.a), the current source with start up.

Drawing of PTAT [3]

Drawing of startup circuit [3]

**1.b)** Proving the gm is independent of temperature and therefore gain bandwidth.

$$GBW = \frac{g_{m2}}{2\pi C_L}$$

$$g_m = \frac{I_0}{V_t}$$

$$I_0 = \left(V_{be1} - V_{be2}\right)/R = V_T \ln\left[I_{in}/I_0\right]/R$$

$$I_{in}/I_0 = 2$$

$$g_m = \frac{V_T \ln[2]}{2\pi V_T} = \frac{\ln[2]}{2\pi R}$$

$$GBW = \frac{\ln[2]}{2\pi R C_L}$$

Showing the GBW is independent of temperature [5]

**1.c)** Completing the circuit for a two stage amplifier

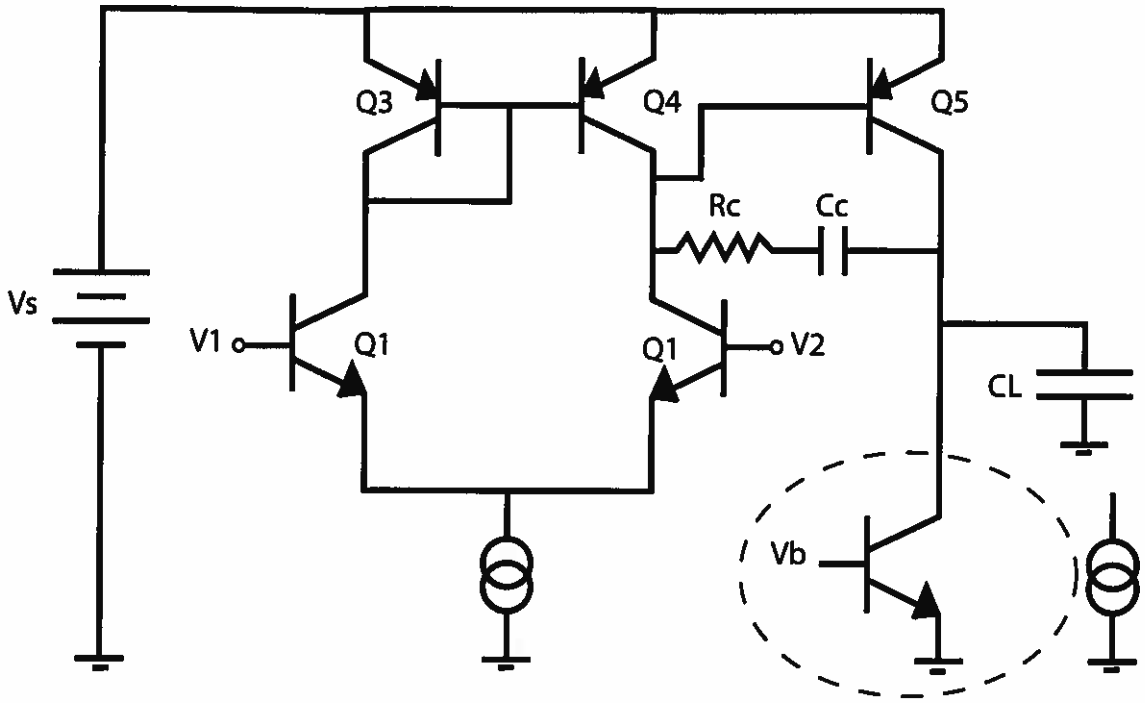


**Figure 2. Answer to 1.c, drawing the second stageof the amplifier.**

**Drawing the second stage of the second stage of the amplifier [3]**

**Adding Compensation [3]**

**1.d)** Adding the compensation capacitance allows splitting the poles helping with the stability of the amplifier so that at the unity gain frequency it has a proper phase margin. Adding a resistive compensation beside the capacitor let us create a zero in transfer function which can be designed to cancel out a pole.

**Explanation on effect of miller capacitance in two stage op-amp [3]**

## Q2

**2.a)** Figure 2.a of question is a bandgap voltage reference circuit which has almost zero temperature coefficient, used mainly as stable voltage reference in ICs. For BG reference,

$$-V_{BE1} = V_{BE2} + I_2 R_3 \quad ; \ \beta \rangle\rangle 1$$

$$V_{BE1} - V_{BE2} = V_T \ln\left(I_1 / I_2\right)$$

$$V_o = V_{BE3} + \left(R_2 / R_3\right) V_T \ln\left(I_1 / I_2\right) \quad ; \ V_{BE3} = V_T \ln\left[I_3 / I_s\right] \ assume\ room\ temp$$

$$For\ \partial V_o/\partial T = 0 \Rightarrow \partial V_{BE3}/\partial T = \frac{V_T}{T}\frac{R_2}{R_3}\ln\left[\frac{I_1}{I_2}\right]$$

$$Since\ \partial V_{BE}/\partial T = -2.5\,mV/^{\circ}C\ \ and\ \ \frac{V_T}{T} = \frac{1.38\times10^{-23}}{1.6\times10^{-19}}$$

$$\Rightarrow\left(\frac{R_2}{R_3}\right)\ln\left(\frac{I_1}{I_2}\right) = 29 \Rightarrow V_o = 1.283$$

**Explaining the bandgap circuit operation [2]**

**Deriving the expression for the output voltage [2]**

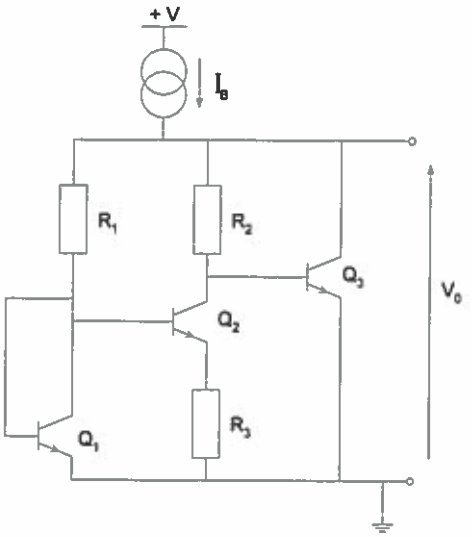


**Figure 3. Question 2 Figure 2.a.**

Circuit of figure 2.b is a Vgs multiplier.

$$V_o \approx V_{GS}\left[1+R_2/R_1\right] = \left(1+R_2/R_1\right)\left[V_T+\sqrt{I_D/\beta}\right]$$

**Circuit work [2]**

**Output voltage [2]**

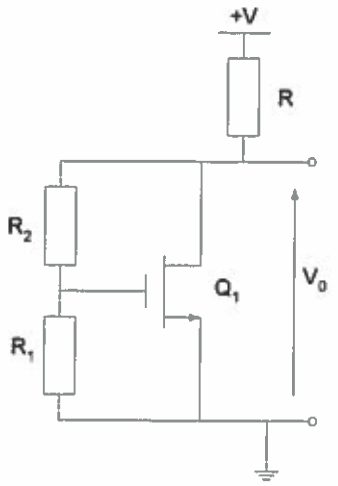


Figure 4. Question 2 Figure 2.b.

Figure 2.c. is a a regulated cascade current sink/source drain-source voltage of Q1 is regulated by the feedback amplifier Q2. It has a very high output impedance equivalent to that of a double cascade

$$I_o = \beta(V_C - V_T)^2$$

**Explanation of the current source/sink [2]**

**Output current equation [2]**

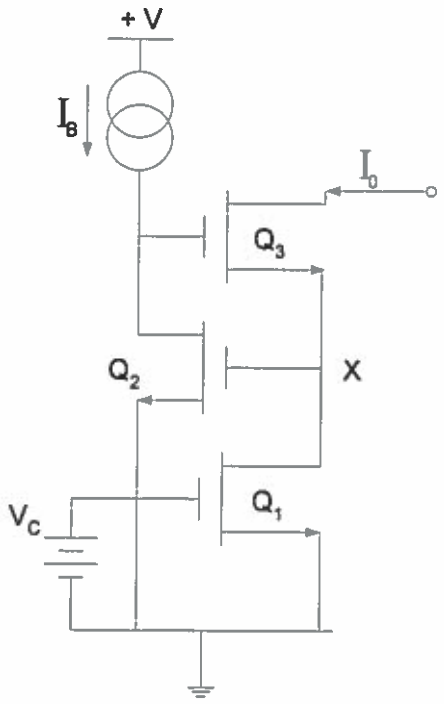


Figure 5. Question 2 Figure 2.c.

2.b The two and four transistor potential dividers depicted in figure below.

$$K_n = 17\mu A/V^2; K_p = 8\mu A/V^2;\ V_{Tn} = V_{Tp} = 1V; V_{DD} = +5V; V_{SS} = -5V; V_{Out} = 0$$

For the two transistor potential divider

$$I_{Qp} = I_{Qn} = \tfrac{1}{2} K_n \frac{W_{Qn}}{L_{Qn}} (V_{out} - V_{ss} - V_{Tn})^2 = \tfrac{1}{2} K_p \frac{W_{Qp}}{L_{Qp}} (V_{out} - V_{dd} - V_{Tp})^2$$

$$\Rightarrow \frac{W_{Qn}}{L_{Qn}} = \frac{10}{136} = 0.073;\ \frac{W_{Qp}}{L_{Qp}} = \frac{10}{64} = 0.156$$

For the four transistor potential divider

$$I_{Qp1} = I_{Qn1} = I_{Qp2} = I_{Qn2} = \tfrac{1}{2} K_n \frac{W_{Qn1}}{L_{Qn1}} (V_{GSn1} - V_{Tn})^2 = \tfrac{1}{2} K_n \frac{W_{Qn2}}{L_{Qn2}} (V_{GSn2} - V_{Tn})^2$$

$$= \tfrac{1}{2} K_p \frac{W_{Qp1}}{L_{Qp1}} (V_{GSp1} - V_{Tp})^2 = \tfrac{1}{2} K_p \frac{W_{Qp2}}{L_{Qp2}} (V_{GSp2} - V_{Tp})^2$$

$$V_{GSn1} = V_{GSn2} = \frac{V_{Out} - V_{SS}}{2} = 2.5V$$

$$V_{GSp1} = V_{GSp2} = \frac{V_{Out} - V_{DD}}{2} = 2.5V$$

$$\frac{W_{n1}}{L_{n1}} = \frac{W_{n2}}{L_{n2}} = \frac{10}{19.125} = 0.523$$

$$\frac{W_{p1}}{L_{p1}} = \frac{W_{p2}}{L_{p2}} = \frac{10}{10} = 1$$

The aspect ratio of the transistors in the four-transistor potential divider is much less than the two-transistor circuit, therefore, its consuming area will be less. For example, assuming common width of 10 units, for the two transistor configuration the active area becomes 10*(64+136)=2000 units while for the four transistor it becomes 10*2*(10+19.125)=582.5 units.

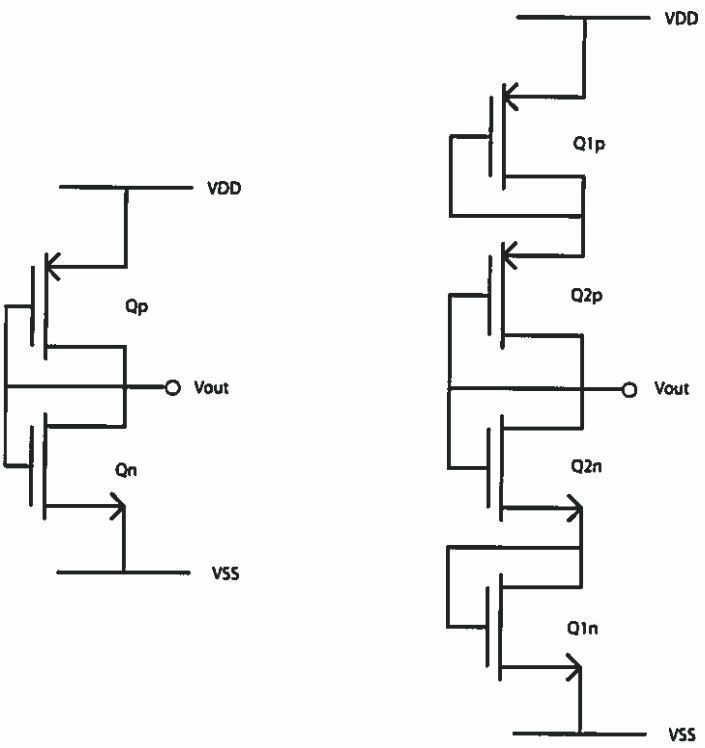


Figure 6. Answer to Question 2.b; potential Divider circuits

**Drawing the potential divider with two transistor [2]**

**Drawing the potential divider with four transistor [2]**

**Calculating the required transistor sizes for each potential divider and comparing their area [4]**

# Q3

## 3.a)

- An algorithmic current mode analogue-to-digital converter

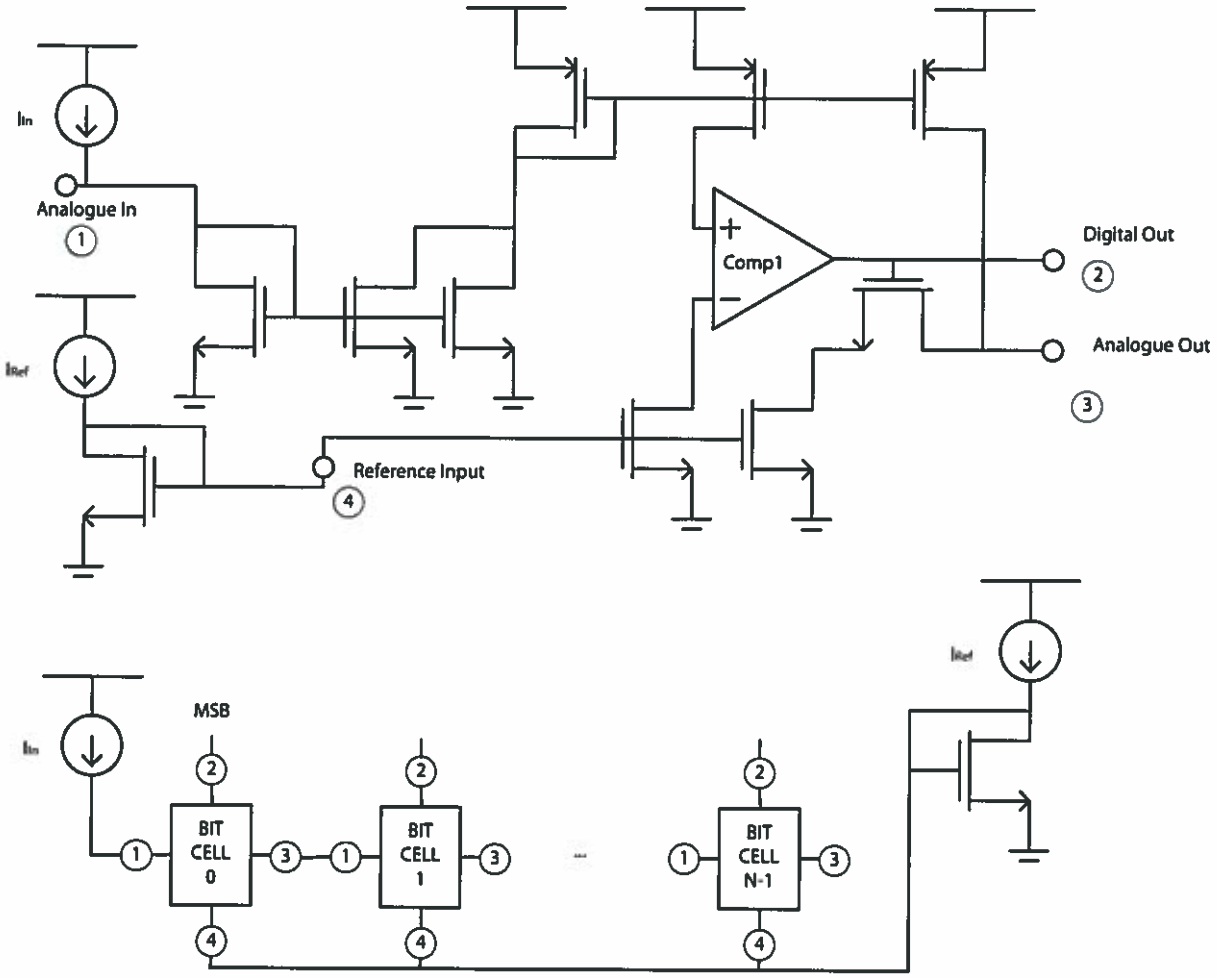


Figure 7. Algorithmic Current Mode Converter.

If 2Iin<IRef, comp goes low, digital output=0;

If 2Iin>IRef, comp output goes high, digital output=1

Analogue output ("In-IRef) feeds into following bit which performs exactly the same function. The process is repeated as many times as necessary in achieve the desired resolution.

- Sigma Delta Modulator

In the sigma-delta modulator, coarse quantization at high sampling rate is combined with negative feedback and digital filtering to achieve increased resolution at lower sampling rates. The architecture comprises a negative feedback loop producing a coarse estimate that oscillates about the true value of input. The feedback A/D and integrator (SC) force the quantizaion error (noise) to have a high frequency spectrum. The output of the modulator is down sampled and gives a multibit digital representation oat lower sampling rate, it averages the coarse quantization leading to a much finer quantization. Since quantization noise is reduced this leads to higher resolution and S/N ratio. When N is 1 the coarse estimate and A/D converter have a 1 bit resolution and this part of the circuit is referred to the sigma-delta modulator. Basically quantisation noise is reduced because the digital filter (decimator) rejects quantisation noise above the signal. Over sampling stretches noise but

keeps the signal the same. Generally quantisation noise is flat over the oversampled frequency range. Higher order sigma-delta modulators shape the quantisation noise (eg low at low frequency and high at high frequency) hence filtering will reject a higher proportion.

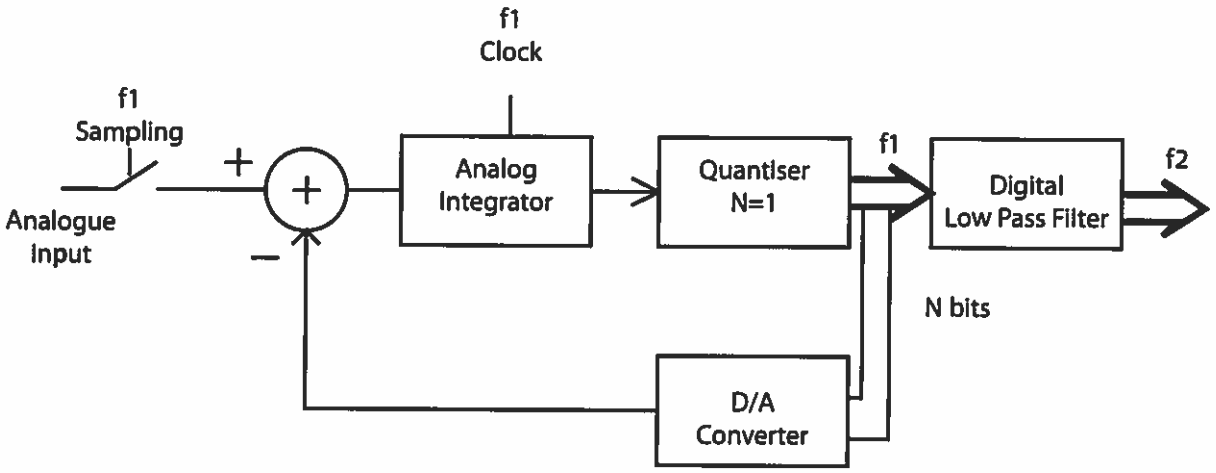


Figure 8. Sigma Delta Converter.

**Describing one of the two converters and drawing it [10]**

**3.b)**

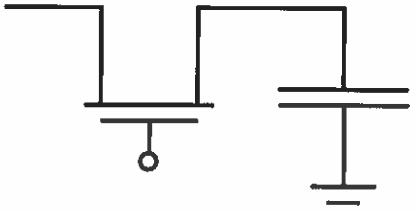

Figure 9. Sampling Switch Configuration.

$$DR \therefore V_{Ref} / Noise = 2^N$$

RMS noise of switch capacitance $\sqrt{\frac{kT}{C}}$

Assume

$f_C = \frac{1}{10.R.C}$ Then solving for C gives

$$DR = 2^N = V_{Ref} / \sqrt{kT\,10Rf_C}$$

$$R_{On} = \frac{1}{2\beta(V_{gs} - V_T)} \approx \frac{1}{(2\beta \times 4)} = 100k\Omega \; ; \beta = \left(\frac{kW}{2L}\right)$$

Can now find DR 40kHz,

$$DR = 3.88\times10^{5} \Rightarrow N = 18.5- > 18$$

**Calculation of the resolution [10]**

## Q4

Specs:

A=80dB; S.R.=5V/us, GB=3MHz

| MODEL PARAMETERS | $Kp\ (\mu A/V^2)$ | $\lambda\ (V^{-1})$ | $V_{T0}\ (V)$ |
|---|---|---|---|
| PMOS | 20 | 0.03 | -0.8 |
| NMOS | 30 | 0.02 | 1.0 |

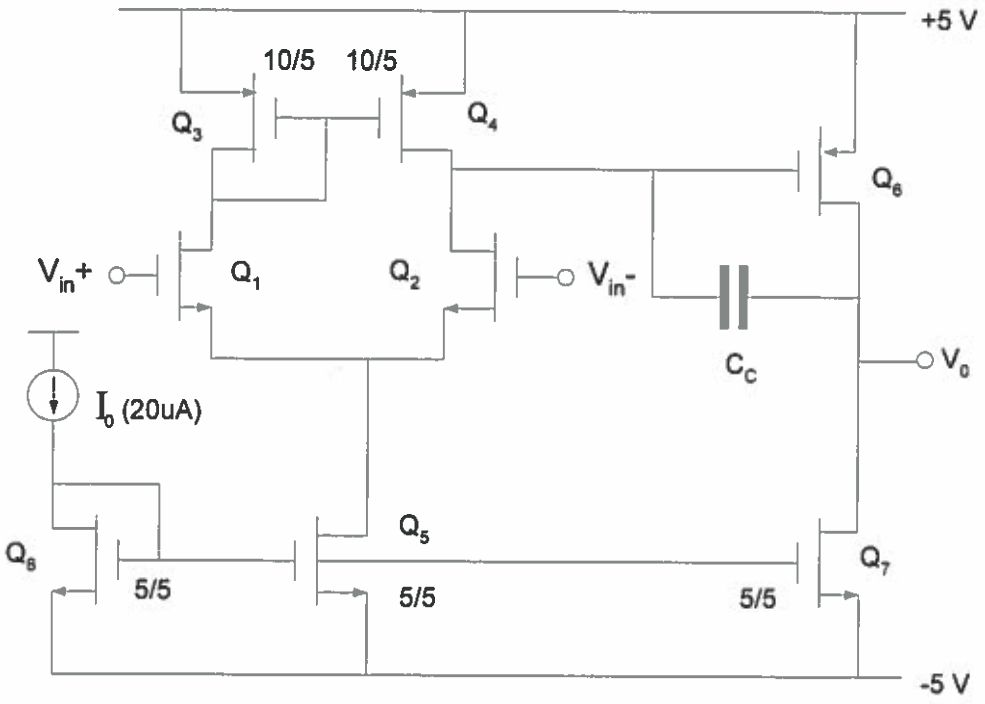


Figure 10. Question 4 figure.

### 4.a)

$$S.R. = {I_o}/{C_C} \Rightarrow C_C = 4\,pF$$

$$GB = {g_{m2}}/{2\pi C_c} \Rightarrow g_{m2} = 7.54\times10^{-5}\ A/V$$

$$g_{m1} = g_{m2} = 2\sqrt{\beta_2 I_{D2}} \Rightarrow \beta_2 = \beta_1 = 1.42\times10^{-4} = \frac{KW}{2L} \therefore \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 9.46 = \frac{47\mu}{5\mu}$$

$$(g_{o2} + g_{o4}) = I_{D2}(\lambda_N + \lambda_P) = 10\times10^{-6}[0.05] = 5\times10^{-7}\ \Omega^{-1}$$

$$A_1 = g_{m2}/(g_{o4} + g_{o2}) \Rightarrow A_1 = 150.8$$

$$A_2 = {10^4}/{A_1} = 66$$

$$(g_{o6} + g_{o7}) = I_{D6}(\lambda_6 + \lambda_7) = 20\times10^{-6}(0.05) = 1\times10^{-6}\ \Omega^{-1}$$

$$A_2 = {g_{m6}}/{(g_{o6} + g_{o7})} \Rightarrow g_{m6} = 6.63\times10^{-5}\ A/V$$

$$\Rightarrow \beta_6 = \left(\frac{g_{m6}}{2}\right)^2 \frac{1}{I_{D6}} = 5.5\times10^{-5} \Rightarrow \left(\frac{W}{L}\right)_6 = 5.5 = \frac{27\mu}{5\mu}$$

**Calculation of the input pair transistor sizes [10]**

**Calculation of the second stage PMOS size [5]**

## 4.b)

Mismatches like λ (the Vds difference), threshold voltage VT and W/L may cause errors in offset and gain. A proper layout may help reduce the effect of such mismatches as well as gradients. Common centroid design splits the transistors over a common centroid or axis of symmetry. For example, the elements A and B in an array may be inter-digitated as in figure below. The input differential pair transistors in the Op-amp are the critical ones for the layout as they affect the offset and gain.

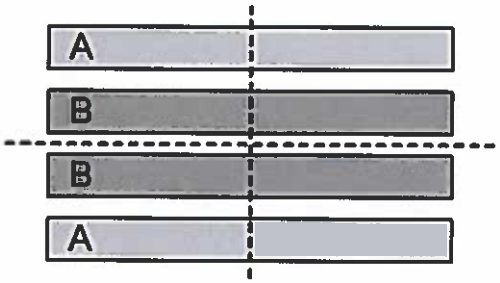


Figure 11. Question 4 part b; interdigitation over a common centroid.

**Description of common centroid concept and telling the crcitical transistors of the Op-Amp for the layout [5]**

## Q5

### 5.a)

Floating resistor RC integrator, double MOS differential eliminating Vds and Vt,

$$I_{D1} = 2\beta\left[(V_{C1} - V - V_T)(V_{In} - V) - 1/2(V_{In} - V)^2\right]$$

$$I_{D2} = 2\beta\left[(V_{C2} - V - V_T)(V_{In} - V) - 1/2(V_{In} - V)^2\right]$$

$$I_{D3} = 2\beta\left[(V_{C2} - V - V_T)(-V_{In} - V) - 1/2(-V_{In} - V)^2\right]$$

$$I_{D4} = 2\beta\left[(V_{C2} - V - V_T)(-V_{In} - V) - 1/2(-V_{In} - V)^2\right]$$

$$I_1 = I_{D1} + I_{D3}\ ;\ I_2 = I_{D2} + I_{D4}$$

$$\Rightarrow (V_{In} - (-V_{In}))/(I_1 - I_2) = 1/2\beta(V_{C1} - V_{C2}) = R$$

$$\tau = RC = \frac{C}{2\beta(V_{C1} - V_{C2})}$$

**Deriving expression for time constant of the integrator [7]**

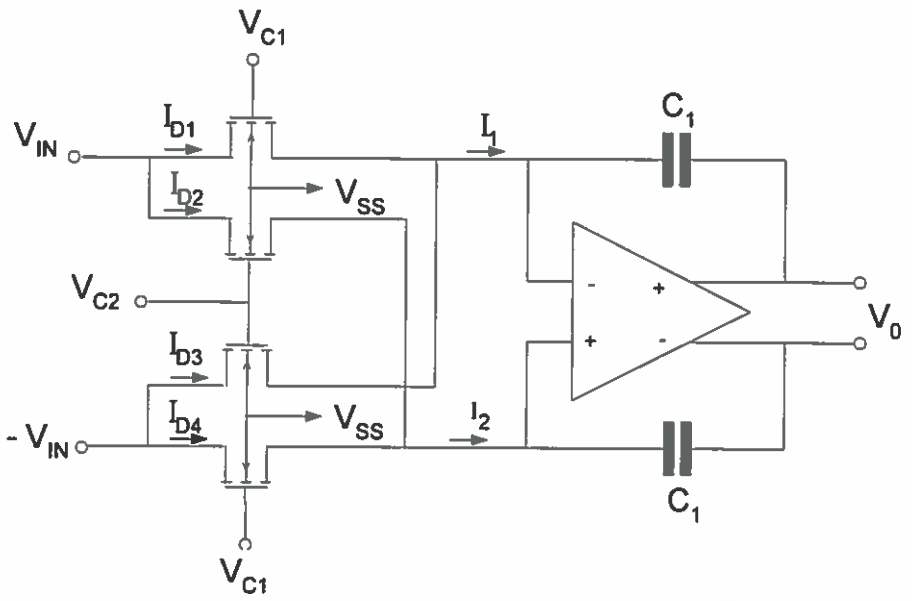


Figure 12. Question 5 part a figure; Integrator.

### 5.b)

Differential output amplifiers with high gain have no way of stabilization since outputs are undefined. Common-mode feedback sensing common-mode output and via negative feedback

stabilised DC output and rejects common-mode output signals to ensure output voltages do not drift given quiescent DC operating point.

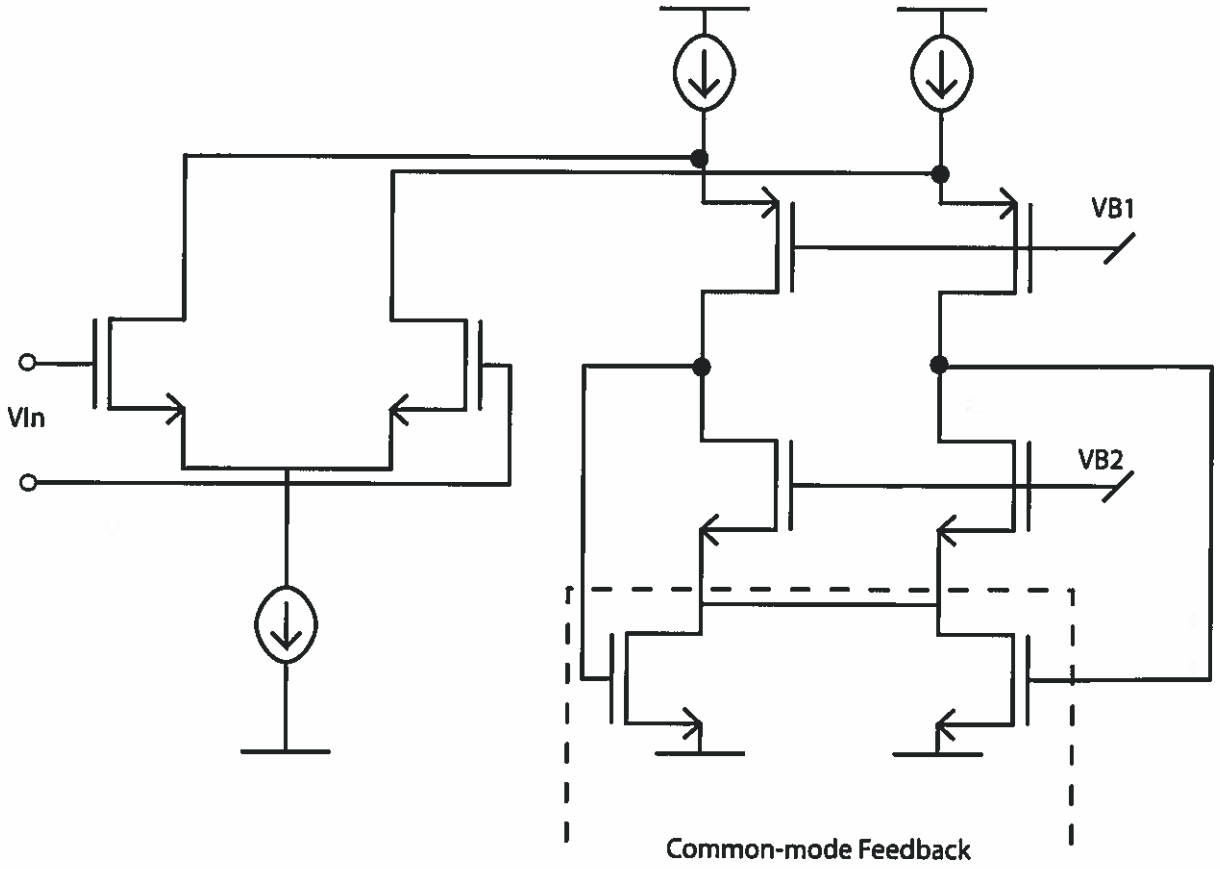


Figure 13. Question 5 part b answer; Fully Cascode Differential amplifier.

**Fully Differential Folded Cascdoe op-amp architecture [5]**

**Explain why common-mode feedback is important [3]**

## 5.c)

Current feedback amplifier

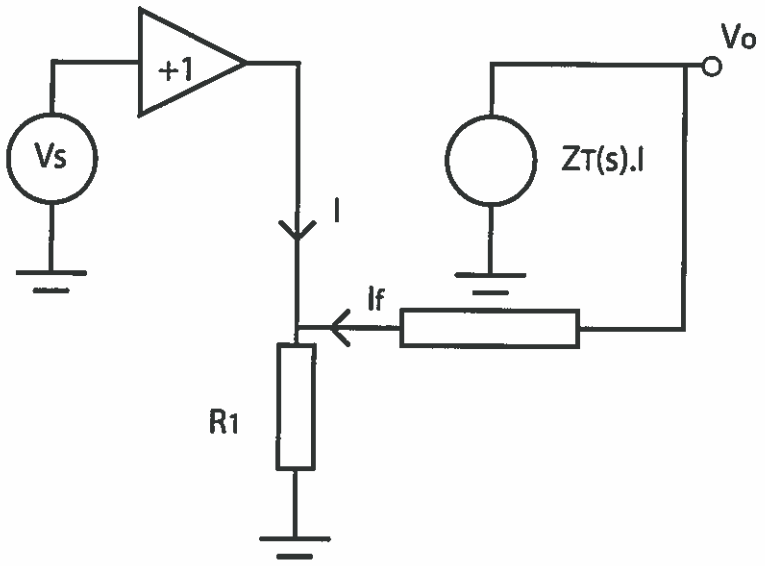


**Figure 14. Question 5 part c answer; Current Feedback Amplifier.**

$$Z_T(s) = Z_{T0} / (1 + jf/f_p)$$

Where fp is the dominant pole

From model

$$I_f = (V_o - V_s)/R_f$$

$$I_1 = V_s/R_1$$

$$V_o = Z_T I = Z_T(I_1 - I_f)$$

$$V_o/V_s = \left(1 + R_f/R_1\right)\left[\frac{Z_T(s)}{R_f + Z_T(s)}\right] = \left(1 + R_f/R_1\right)\left[\frac{Z_{T0}}{R_f + Z_{T0}}\right]\left(\frac{1}{1 + jf\Big/ f_p\left(\frac{Z_{T0} + R_f}{R_f}\right)}\right)$$

Assuming ZT0>>Rf

$$\left(V_o/V_s\right)_{j\omega} = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{1}{1 + jf\Big/ GB/R_f}\right) \quad ; GB = f_p Z_{T0}$$

$$f_{p-closed} = GB/R_f$$

$$A_{closed} = \left(1 + \frac{R_f}{R_1}\right)$$

Therefore the bandwidth is defined by Rf and gain by R1

**Explaining why gain is independent of bandwidth in current feedback amplifier [5]**

## Q6

### 6.a)

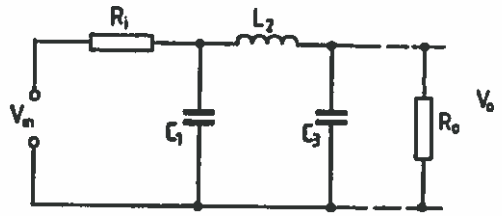


Figure 15. Question 6 part a andwer; 3rd Order Ladder Chebyshev Filter.

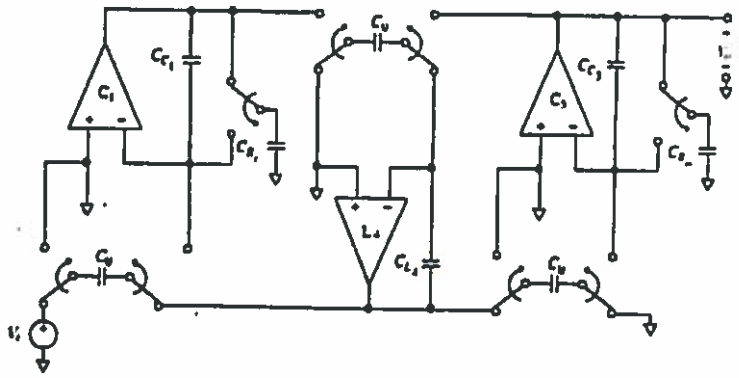

Figure 16. Question 6 part a answer; 3rd-order Chebyshev Low-pass Switched-capacitor Ladder Filter.

**Drawing the 3rd order Chebyshev low pass filter and its switched capacitor ladder equivalent [10]**

### 6. b)

$$f_c = \frac{2\pi f_o}{L_2}\frac{C_{L2}}{C_u} = \frac{2\times 3.14\times 5\times 10^3}{1.096}\frac{3.49}{1} = 99.99kHz \approx 100kHz$$

$$C_1 = C_3 = \frac{1.596}{2\pi f_o} = \frac{1.596}{2\times 3.14\times 5\times 10^3} = 5.08\times 10^{-5}\,F$$

$$\frac{C_{c1}}{C_u} = f_c C_1 R_s\,;\, R_s = 1 \Rightarrow C_{c1} = C_{c3} = 100\times 10^3 \times 5.08\times 10^{-5}\times 10^{-12} = 5.08\,pF$$

$$L = \frac{1.096}{2\pi f_o} = 3.489 \times 10^{-5}$$

$$\frac{C_{L2}}{C_u} = \frac{f_c L_2}{R_s}; R_s = 1 \Rightarrow C_{L2} = 3.489 \times 10^{-5} \times 100 \times 10^3 \times 10^{-12} = 3.49 pF$$

**Calculating the clock frequency required for 5kHz cut off and showing selected capacitance values are proper [10]**