

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2009

EEE/ISE PART I: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 1

Corrected Copy

Monday, 8 June 10:00 am

Time allowed: 2:00 hours

There are FOUR questions on this paper.

Q1 is compulsory.

Answer Q1 and any two of questions 2-4.

Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s) :	A.S. Holmes, A.S. Holmes
	Second Marker(s) :	S. Lucyszyn, S. Lucyszyn

1. **This question is compulsory.** You should attempt all six parts. State clearly any assumptions made in your calculations.

- a) For the circuit in Figure 1.1, choose the value of R_B so that the transistor is saturated with an overdrive factor of 3 when $V_{IN} = 5\text{ V}$.

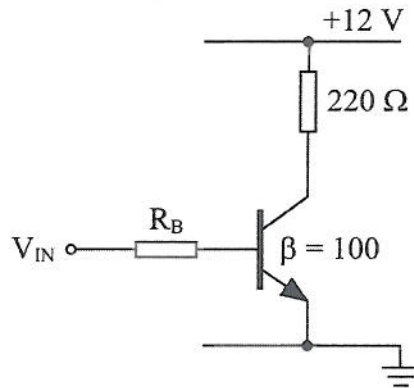


Figure 1.1

[5]

- b) Determine the drain current and drain voltage of the MOSFET in Figure 1.2 when $V_{DD} = 5\text{ V}$. What is the minimum supply voltage for which the MOSFET will remain active?

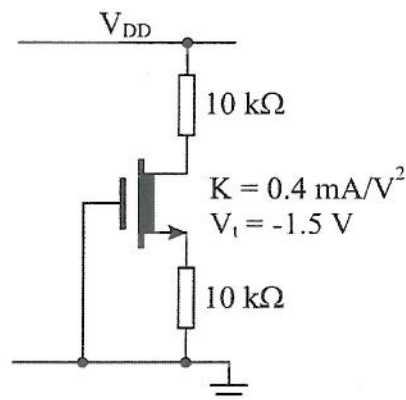


Figure 1.2

[9]

- c) Sketch the circuit for a simple BJT current mirror and, assuming matched transistors, derive an expression for the finite beta error between the input and output currents.

[6]

Question 1 continues on the next page...

Question 1 continued

- d) A depletion type active load is formed by shorting the gate and source of an n-channel depletion mode MOSFET. Sketch the I-V characteristic for this device for $V \geq 0$, and annotate your graph to identify clearly the triode and active regions. [6]
- e) For the circuit in Figure 1.3, determine the operating modes of the two transistors and the value of the current I.

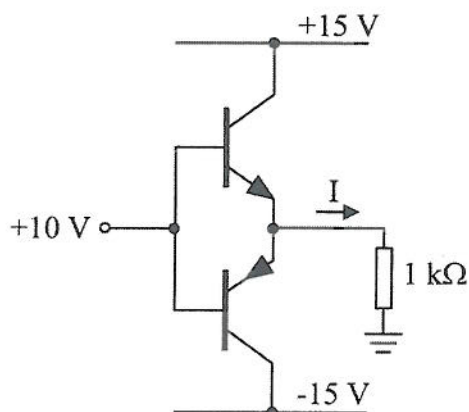


Figure 1.3

[6]

- f) The voltage V_{IN} in Figure 1.4 changes to +5 V at time $t = 0$, after having been held at zero for a long time. Calculate the time T taken for the current in the inductor to reach its final value, and sketch the time variations of the inductor current and the output voltage V_{OUT} from just before $t = 0$ to $t = 2T$.

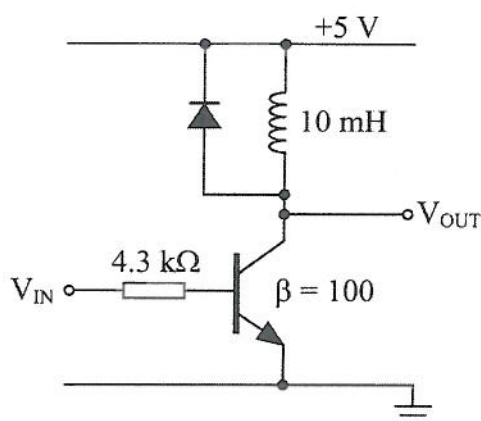


Figure 1.4

[8]

2. a) For the amplifier in Figure 2.1 below, choose the values of R_B and R_C to give a collector bias current of 0.5 mA and a quiescent output voltage of 5 V. State clearly any assumptions you make. [6]
- b) Draw a small-signal equivalent circuit of the amplifier in Figure 2.1, assuming your calculated resistor values, and hence determine the small-signal macromodel parameters i.e. input resistance, output resistance and voltage gain. [12]
- c) An amplifier similar to that in Figure 2.1, with the resistor values you calculated, is inserted between a signal source and a capacitive load as shown in Figure 2.2. Determine the overall voltage gain v_L/v_S for this arrangement in the mid-band, where the input coupling capacitor is effectively short-circuit and the load is effectively open-circuit. Also draw a dimensioned sketch showing the variation of $|v_L/v_S|$ with frequency over the range 1 Hz to 100 kHz. [12]

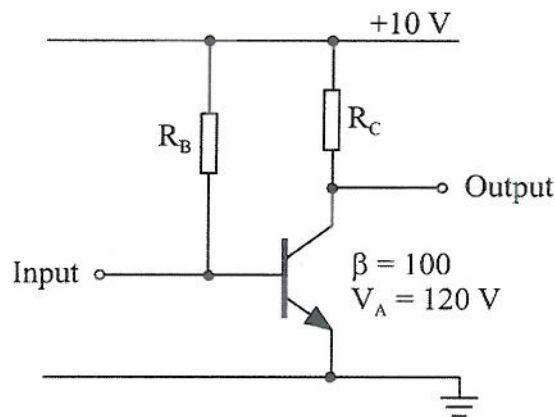


Figure 2.1

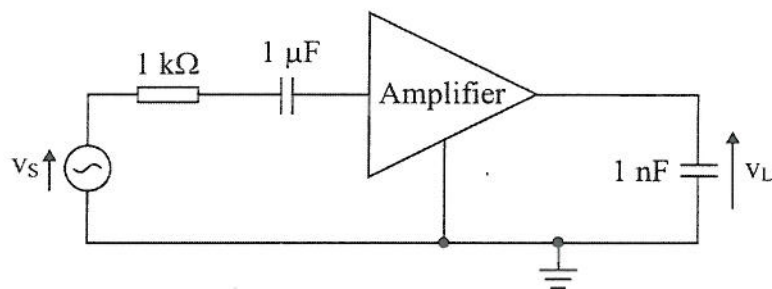


Figure 2.2

3. Figure 3 shows a single-stage CMOS amplifier in which both MOSFETs contribute to the small-signal gain.

- a) Determine the gate voltage V_G at which the drain currents in the two MOSFETs are equal. Hence choose the value of R_{G2} to give a quiescent output voltage of 2.5 V. You should assume that the current in the bias network is negligible compared to the drain current. [12]

- b) Draw a small-signal equivalent circuit of the amplifier, including all components, and show that the mid-band small-signal voltage gain is given by:

$$A_V = -(g_{m1} + g_{m2} - 1/R_{G1}) \cdot (r_{o1} // r_{o2} // R_{G1})$$

where the symbols g_m and r_o denote the usual MOSFET parameters, and the subscripts 1 and 2 refer to Q1 and Q2 respectively. Hence evaluate A_V . Also determine the mid-band small-signal input resistance of the circuit, assuming the value of R_{G2} you calculated in part a). [12]

- c) Estimate the maximum amplitude of mid-band sinusoidal signal that can be applied to the input of the amplifier without either of the MOSFETs entering the triode region. [6]

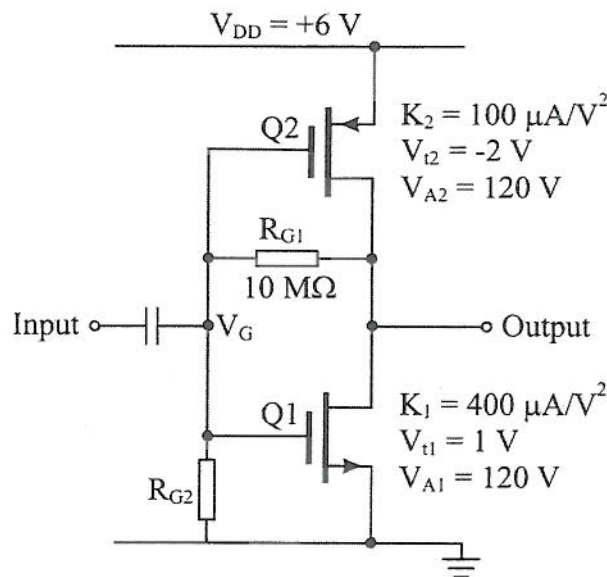


Figure 3

4. Figure 4 shows a variable-gain differential amplifier in which the gain can be adjusted by means of a control voltage V_C . All four transistors are matched, with $\beta = 100$, and you may assume that they have infinite small-signal output resistance.

- Assuming all transistors are active, calculate the tail current I and the quiescent output voltage V_{OUT} when $V_C = 0$ and $V_{IN1} = V_{IN2}$. You may ignore base currents. [6]
- Draw a small-signal macromodel for the amplifier, expressing any bias-dependent parameters in terms of the tail current, and defining the differential input voltage as $(V_{in1} - V_{in2})$. [8]
- Derive an expression relating the differential voltage gain to the control voltage V_C . Hence plot the variation of the differential voltage gain with control voltage over the range $-5\text{ V} \leq V_C \leq +5\text{ V}$. [8]
- Illustrate, with the aid of a sketch, the variation in the input common mode voltage range of the amplifier as V_C is varied over the range $-5\text{ V} \leq V_C \leq +5\text{ V}$. [8]

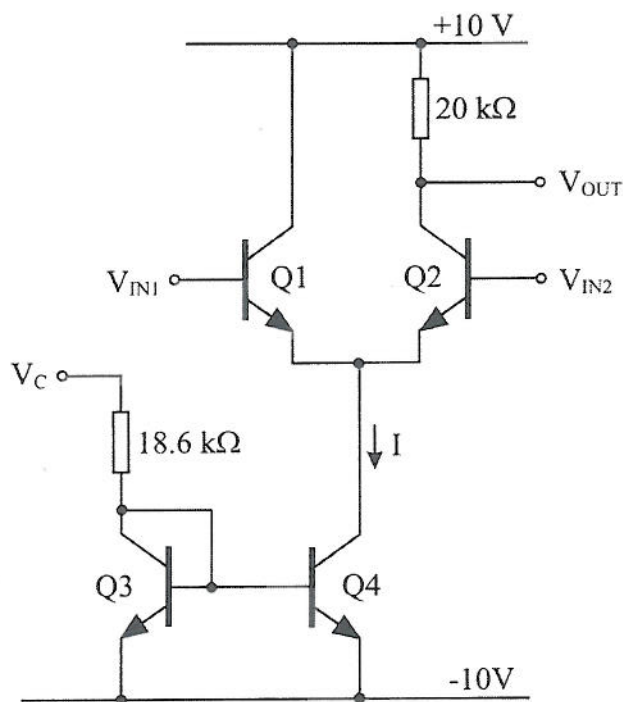


Figure 4

1 a) Collector current at onset of saturation is $\hat{I}_C = \frac{11.3V}{220\Omega} = 51.4 \text{ mA}$

Base current required for 3x overdrive is $I_B = \frac{3\hat{I}_C}{\beta} = 1.54 \text{ mA}$

$$R_B = (5 - 0.7)/I_B = \underline{2.79 \text{ k}\Omega} \quad [5]$$

b) Assuming MOSFET active $I_D = K(-V_S - V_t)^2$

Also $V_S = I_D R_S$ where R_S is resistor in source

So :

$$\frac{V_S}{KR_S} = V_S^2 + V_t^2 + 2V_t V_S$$

$$V_S^2 + \left(2V_t - \frac{1}{KR_S}\right)V_S + V_t^2 = 0$$

$$V_t = -1.5 \text{ V}, \quad KR_S = 4 \text{ V}^{-1}$$

$$\Rightarrow V_S^2 - \left(\frac{13}{4}\right)V_S + \frac{9}{4} = 0$$

$$4V_S^2 - 13V_S + 9 = 0$$

$$(V_S - 1)(4V_S - 9) = 0$$

$$V_S = 1 \text{ V or } V_S = 2.25 \text{ V}$$

Larger root rejected because MOSFET subthreshold

$\Rightarrow V_S = 1 \text{ V}$ if MOSFET active

$$\text{In this case } I_D = K(-V_S - V_t)^2 = \underline{0.1 \text{ mA}}$$

$$\text{With } V_{DD} = 5 \text{ V}, \quad V_D = 5 - 0.1 \text{ mA} \times 10 \text{ k} = \underline{4 \text{ V}}$$

$$\text{Check mode: } V_{DS} = 4 - 1 = 3, \quad V_{GS} = -1, \quad V_t = -1.5 \text{ V}$$

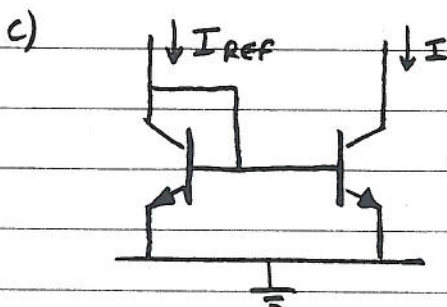
$\Rightarrow V_{DS} > V_{GS} - V_t$ and active assumption correct.

MOSFET will remain active provided

$$V_{DD} - I_D R_D - V_S \geq V_{GS} - V_t$$

$$\text{or } V_{DD} \geq I_D R_D - V_t \quad (\text{NB } V_G = 0)$$

$$\Rightarrow \text{Min } V_{DD} \text{ is } 0.1 \text{ mA} \times 10 \text{ k} + 1.5 = \underline{2.5 \text{ V}} \quad [9]$$



Transistors have same I_B & I_C values

$$\Rightarrow I_{REF} = I_C + 2I_B = I_C \left(1 + \frac{2}{\beta}\right)$$

$$I = I_C = I_{REF} / \left(1 + \frac{2}{\beta}\right)$$

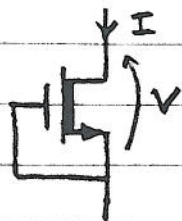
and finite β error is

$$FBE = I_{REF} - I$$

$$= I_{REF} \left[1 - \frac{1}{1 + \frac{2}{\beta}} \right] \quad [6]$$

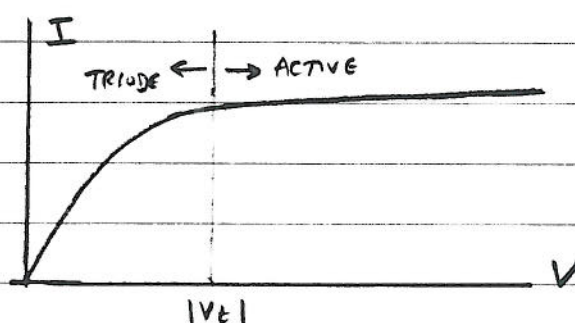
$$= I_{REF} \left[\frac{2}{2 + \beta} \right]$$

1 d) Depletion load:



I-V characteristic is o/p curve for fixed

V_{GS} :



[6]

e) Class B o/p stage w $V_{in} > +0.7V$

\Rightarrow Upper transistor is conducting, and ACTIVE since $V_C > V_B$

Both transistors have $V_B = +10V$, $V_E = +9.3V$

lower (PNP) transistor is CUT-OFF since $V_{BE} > 0$, $V_{BC} > 0$

$$I = 9.3V / 1k = \underline{9.3 \text{ mA}}$$

[6]

f) Inductor current I_L is zero at $t=0^-$ and can't change instantaneously $\Rightarrow I_L = 0$ at $t=0^+$

\Rightarrow transistor is initially saturated with $V_{out} = V_{CESAT} \approx 0.2V$

Inductor current builds up at rate of

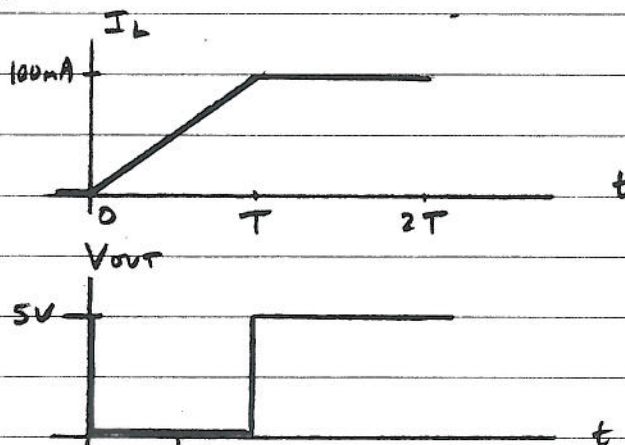
$$dI_L/dt = (5 - 0.2)/L = 480 \text{ A/sec}$$

This continues until transistor comes out of saturation

ie until $I_L = \beta I_B = 100 \times (5 - 0.7)/4.3k = 100 \text{ mA}$

Time taken for this is $T = 100 \text{ m}/480 = \underline{208 \text{ } \mu\text{sec}}$

for $t > T$ the transistor is active, I_L is fixed at 100 mA and $V_{out} = 5V$



[8]

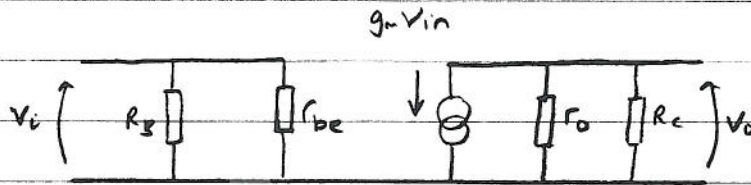
$$2a) I_B = 0.5\text{mA}/100 = \frac{10^{-0.7}}{R_B} \Rightarrow R_B = \frac{10^{-0.7}}{0.5\text{mA}} \times 100 = \underline{1.86\text{M}\Omega}$$

$$V_{out} = 10 - I_C R_C$$

$$R_C = (10 - 5)/0.5\text{mA} = \underline{10\text{k}\Omega}$$

[6]

b) SSEC:



$$g_m = I_C/V_T = 0.02\text{S}$$

$$r_{be} = \beta/g_m = 5\text{k}\Omega$$

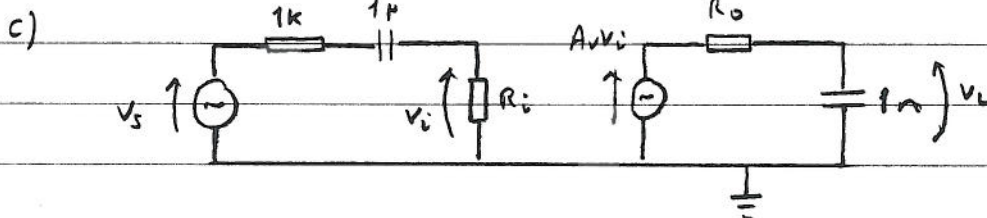
$$r_o = V_A/I_C = 240\text{k}\Omega$$

$$R_i = R_B \parallel r_{be} = 1.86\text{M} \parallel 5\text{k} = \underline{4.99\text{k}\Omega}$$

$$R_o = R_C \parallel r_o = 10\text{k} \parallel 240\text{k} = \underline{9.6\text{k}\Omega}$$

$$A_v = -g_m R_o = -0.02 \times 9600 = \underline{-192}$$

[12]

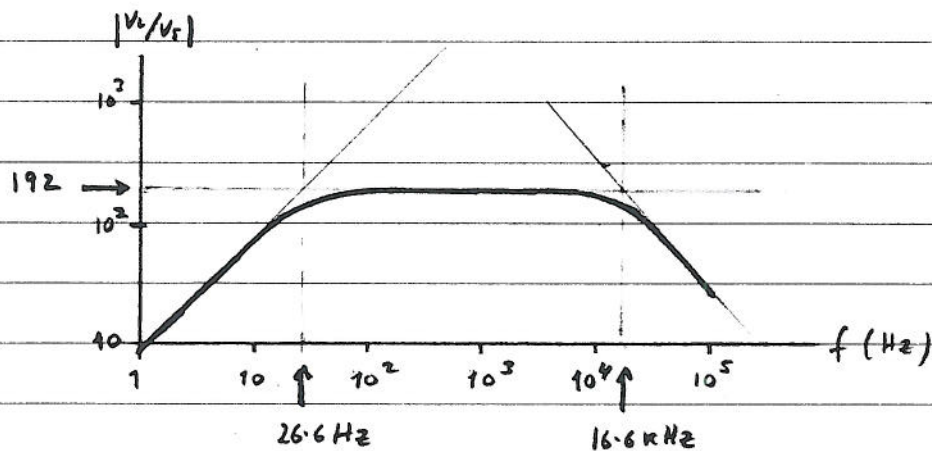


Overall gain in mid-band is

$$V_L/V_S = \frac{R_i}{R_i + 1\text{k}} \cdot A_v = \frac{4.99}{5.99} \cdot (-192) = \underline{-160}$$

l/p side filter is high-pass with cut-off $f_{c1} = [2\pi(R_i + 1\text{k}) \cdot 1\mu]^{-1} = 26.6\text{Hz}$

o/p side filter is low-pass with cut-off $f_{c2} = [2\pi R_o \cdot 1\text{n}]^{-1} = 16.6\text{kHz}$



[12]

3 a) Drain currents (assuming active mode) are

$$I_{D1} = K_1 (V_G - V_{t1})^2 \quad I_{D2} = K_2 (V_G - V_{DD} - V_{t2})^2$$

When $I_{D1} = I_{D2}$ we have $\sqrt{K_1} (V_G - V_{t1}) = \pm \sqrt{K_2} (V_G - V_{DD} - V_{t2})$

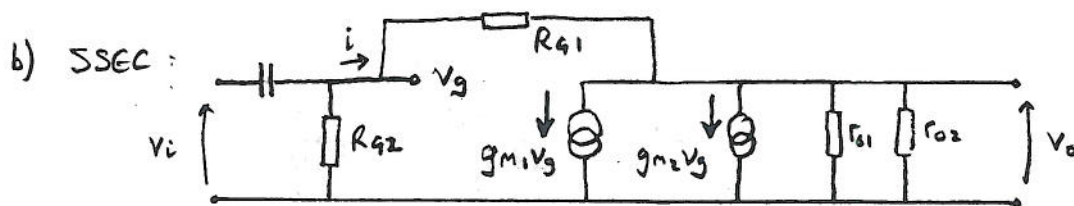
Taking -ve sign (to ensure both MOSFETs conducting):

$$V_G = \frac{V_{DD} + V_{t2} + \sqrt{K_1/K_2} V_{t1}}{1 + \sqrt{K_1/K_2}} = \frac{6 - 2 + 2 \times 1}{1 + 2} = \underline{\underline{2V}}$$

For $V_{out} = 2.5V$ require $(1 + \frac{R_{G1}}{R_{G2}}) \times 2 = 2.5 \Rightarrow R_{G2} = 4R_{G1} = \underline{\underline{40M\Omega}}$

Check modes: Q1 has $V_{GS} = 2V$, $V_{DS} = 2.5V$, $V_t = 1 \Rightarrow V_{DS} > V_{GS} - V_t$ ✓ ACTIVE NMOS

Q2 has $V_{GS} = -4V$, $V_{DS} = -3.5V$, $V_t = -2V \Rightarrow V_{DS} < V_{GS} - V_t$ ✓ ACTIVE PMOS [12]



In mid-band, i/p capacitor has negligible impedance $\Rightarrow V_G = V_i$

$$\text{KCL @ o/p} \Rightarrow g_{m1} V_i + g_{m2} V_i + \frac{V_o}{r_{o1}} + \frac{V_o}{r_{o2}} + \frac{V_o - V_i}{R_{G1}} = 0$$

$$\text{Rearranging: } A_v = \frac{V_o}{V_i} = -\left(g_{m1} + g_{m2} - \frac{1}{R_{G1}}\right) \cdot (r_{o1} \parallel r_{o2} \parallel R_{G1})$$

Quiescent drain current is $I_D = K_1 (V_G - V_{t1})^2 = 0.4 \text{ mA}$

$$g_{m1} = 2\sqrt{K_1 I_D} = 0.8 \text{ mA/V}$$

$$r_{o1} = r_{o2} = V_A / I_D = 300 \text{ k}\Omega$$

$$g_{m2} = 2\sqrt{K_2 I_D} = 0.4 \text{ mA/V}$$

$$R_{G1} = 10 \text{ M}\Omega \Rightarrow A_v = \underline{\underline{-177}}$$

$$\text{Current } i = (V_i - V_o) / R_{G1} \Rightarrow V_i / i = \frac{R_{G1}}{1 - A_v} = 56.2 \text{ k}\Omega$$

$$\text{Input resistance } R_i = R_{G2} \parallel (V_i / i) = 40 \text{ M}\Omega \parallel 56.2 \text{ k}\Omega = \underline{\underline{56.1 \text{ k}\Omega}}$$

[12]

c) Gain is quite high so calculation ignoring movement of V_G is acceptable. In this case

Q1 enters triode when $V_{out} = V_G - V_{t1} = 1V$

Corresponding i/p signal level is $(1 - 2.5) / A_v = +8.47 \text{ mV}$

Q2 enters triode when $V_{out} = V_G - V_{t2} = 4V$

Corresponding i/p signal level is $(4 - 2.5) / A_v = -8.47 \text{ mV}$

\Rightarrow Max amplitude is 8.47 mV

(Calculation including movement of V_G gives 8.43 mV)

[6]

4 a) When $V_c = 0$, i/p current to current mirror is $9.3V/18.6k = 0.5mA$

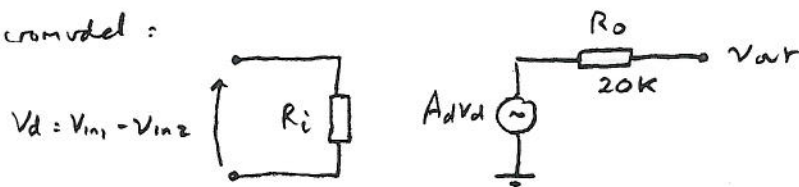
Ignoring base currents so $I = \underline{0.5mA}$

If $V_{in1} = V_{in2}$, $I_{c1} = I_{c2} = I/2 = 0.25mA$

and $V_{out} = 10 - 20k \times 0.25m = \underline{+5V}$

[6]

b) Macromodel:



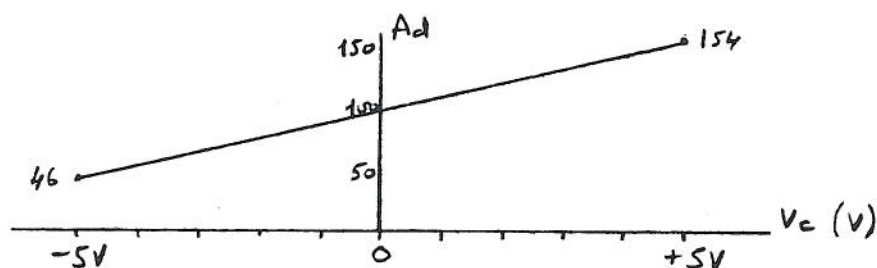
$$A_d = \frac{g_m R_o}{2} = \frac{I R_o}{4V_T} = 2 \times 10^5 I \quad (I \text{ in A})$$

$$R_i = 2r_{be} = 2\beta/g_m = \frac{4V_T\beta}{I} = 10/I \quad (1)$$

[8]

c) $I = (V_c + 9.3)/18.6k \Rightarrow A_d = 10.75 \times (V_c + 9.3)$

Gain varies linearly with control voltage



[8]

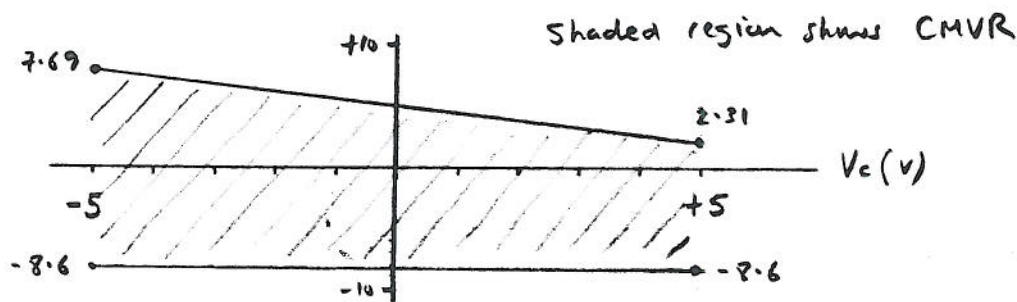
d) Lower limit of CMVR is determined by saturation of Q4

This occurs when $V_{E1} = V_{E2} \approx -10 + 0.7$, corresponding to a CM input voltage of $-10 + 0.7 + 0.7 = \underline{-8.6V}$. This has negligible dependence on V_c .

Upper limit is where Q2 enters saturation i.e. where $V_{in} = V_{out}$

Since V_{out} varies with V_c this does show V_c dependence.

We have $V_{out} = 10 - 20k \cdot I/2 = 10 - (V_c + 9.3) \times 10/18.6$



[8]