UNIVERSITY OF LONDON
IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 1997

BEng Honours Degree in Computing Part III
BEng Honours Degree in Information Systems Engineering Part III
MEng Honours Degree in Information Systems Engineering Part III
MSc Degree in Advanced Computing
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the
Diploma of Membership of Imperial College
Associateship of the City and Guilds of London Institute

PAPER 3.18 / I3.4

CUSTOM COMPUTING

Friday, May 2nd 1997, 2.30 - 4.30

Answer THREE questions

For admin. only: paper contains 4 questions

1a Provide a recursive definition of $\mathsf{row}_n\ R$. Express $\mathsf{rdl}_n\ R$ using $\mathsf{row}_n\ R$.

b Provide a recursive definition of $\mathsf{rdl}_n\ R$. What method will you use to prove that your definition is compatible with the description of $\mathsf{rdl}_n\ R$ in part a? (You do not need to carry out the proof.)

c Recall that:

$$\begin{array}{lll} \langle x, y\rangle & \pi_2 & y \\ \langle x, \langle y_1, y_2, \ldots, y_n\rangle\rangle & apl_n & \langle x, y_1, y_2, \ldots, y_n\rangle \end{array}$$

Provide two designs, $sum1_n$ and $sum2_n$, for summing a list of n numbers using a network of two-input adders described by rdl. $sum1_n$ should involve π_2, while $sum2_n$ should involve apl (or suitably reflected versions of these components). Explain the strengths and limitations of $sum1_n$ and $sum2_n$.

d A combinational design means that a computation will be completed within each clock cycle, and no information will be passed between cycles. Provide a combinational design IP_m for computing the inner product of two vectors of length m using $sum1_m$.

e Provide a combinational design $MV_{m,n}$ for multiplying an m by n matrix and an n-element vector. Your design should involve IP_n, and the wiring component $dstl_m$ which is given by

$$\langle x, \langle y_1, y_2, \ldots, y_m\rangle\rangle \quad dstl_m \quad \langle\langle x, y_1\rangle, \langle x, y_2\rangle, \ldots, \langle x, y_m\rangle\rangle$$

At each cycle, the matrix is represented as a list of lists, with the first list corresponding to the top row in the matrix, while the vector is represented as a list, with the first element corresponding to the top element of the vector. Show that your design produces the correct answer for the matrix $\langle\langle a, b, c\rangle, \langle d, e, f\rangle\rangle$ and the vector $\langle p, q, r\rangle$.

f Find A and B such that the design MM_n, given by

$$MM_n \quad = \quad \mathsf{snd}\ A\ ;\ B\ ;\ \mathsf{map}_n\ MV_{n,n}$$

corresponds to a combinational design for multiplying two n by n square matrices. Show that your design produces the correct answer for the matrices $\langle\langle a, b\rangle, \langle c, d\rangle\rangle$ and $\langle\langle p, q\rangle, \langle r, s\rangle\rangle$.

The six parts carry, respectively, 15%, 15%, 20%, 15%, 15% and 20% of the marks.

2a The component zip_n is given by

$$\langle\langle x_1, x_2, \ldots, x_n\rangle, \langle y_1, y_2, \ldots, y_n\rangle\rangle \quad zip_n \quad \langle\langle x_1, y_1\rangle, \langle x_2, y_2\rangle, \ldots, \langle x_n, y_n\rangle\rangle$$

Provide three different ways of laying out $[Q, R]\backslash zip_2$, given that wires can be placed above circuit components if required.

b Find A, B and C such that

$$([A, B] \setminus zip_2) \setminus\!\setminus C \;=\; \mathsf{row}_n([Q, R]\backslash zip_2).$$

Draw a diagram showing the design on the left-hand side of this equation for $n = 3$.

c Provide a recursive definition of $\mathsf{irow}_n\, R$ for describing a row of components R_0, R_1, ..., R_{n-1}. Revise the equation in part b so that it can be used for $\mathsf{irow}_n\, R$.

d Given that R^v corresponds to reflecting R in a vertical axis, find S such that

$$\begin{aligned}&((\mathsf{row}_n Q) \leftrightarrow (\mathsf{row}_n R)) \updownarrow swap \;;\; \mathsf{snd}\; fork^{-1} \;;\; \pi_1\\ &\quad = \;([\mathsf{row}_n\, Q, \mathsf{row}_n\, R^v]\backslash zip_2) \setminus\!\setminus S \;;\; \mathsf{snd}\; fork^{-1} \;;\; \pi_1\end{aligned}$$

Sketch diagrams to describe both sides of the above equation when $n = 3$. Does this equation remain correct if the component π_1 is removed from both sides of the equation? Justify your answer.

e Using appropriate results from parts a, b and d, obtain a design with a repeating unit T described by $[Q, R^v]\backslash zip_2$. Given that both Q and R are both of height h and width w, sketch a diagram to show that $\mathsf{row}_n\, T$ can be laid out such that its height is h and its width is $2nw$. Sketch another diagram to show that $\mathsf{row}_n\, T$ can also be laid out such that its height is $2h$ and its width is nw.

The five parts carry, respectively, 10%, 20%, 20%, 30% and 20% of the marks.

Turn over...

3a Define a recursive function nat_n which maps a list of n bits (most significant bit first) into a natural number. Your answer can include the component *mult2*, given by

$$x \quad mult2 \quad 2x$$

which multiplies its inputs by 2.

b Explain why the circuit $div3_n$, specified by

$$div3_n \;=\; nat_n \;;\; ([nat_n \;;\; mult3,\; nat_2] \;;\; add)^{-1}$$

corresponds to a design which can be used to divide a given signal x by 3 to give the quotient q and the remainder r. The component *mult3* is similar to *mult2* except that it multiplies its inputs by 3.

c Sketch two block diagrams to describe expressions on both sides of the following equation:

$$\begin{aligned} &\langle a, \langle xs, u\rangle\rangle \quad (\mathsf{snd}\ apr_n \;;\; \mathsf{row}_{n+1}\, R \;;\; \mathsf{fst}\ apr_n^{-1}) \quad \langle\langle ys, v\rangle, w\rangle \\ &\quad \Leftrightarrow\ \exists r \quad . \quad \langle a, xs\rangle \quad (\mathsf{row}_n\, R) \quad \langle ys, r\rangle \quad \wedge \quad \langle r, u\rangle \quad R \quad \langle v, w\rangle \end{aligned}$$

You can include composite expressions in a single block.

d Given that

$$x \quad div3_n \quad \langle q, r\rangle \;\Leftrightarrow\; \langle\langle 0, 0\rangle, x\rangle \quad (\mathsf{row}_n\, dcell) \quad \langle q, r\rangle$$

where *dcell* has three inputs r_0, r_1 and u in its domain and three outputs w_0, w_1 and v in its range, show that the inputs and outputs of *dcell* satisfy the constraint equation

$$4r_0 + 2r_1 + u \;=\; 3v + 2w_0 + w_1$$

Hint: consider $apr_n \;;\; div3_{n+1} \;;\; \mathsf{fst}\,(apr_n^{-1})$.

e Generate a truth table for *dcell* using the result in part d.

The five parts carry, respectively, 10%, 20%, 10%, 30% and 30% of the marks.

4a Provide a recursive definition for a function $\mathsf{trail}_n\ R\,S$, which describes a square array with the component S on the trailing diagonal and the component R elsewhere.

b Given timeless R and the delay element $\mathcal{D}$, find P and Q such that

$$\mathsf{trail}_k\ R\,R \;=\; (\mathsf{trail}_k\ P\,Q)\ ;\ \mathcal{D}^{-1}$$

You do not need to supply a proof.

c Provide a theorem (no proof is needed) which can be used to pipeline a rectangular grid of timeless circuits. Use this theorem to derive

$$\begin{aligned}&\mathsf{grid}_{m,n}(\mathsf{grid}_{k,k}\ R)\\ &\quad=\ \mathsf{grid}_{m,n}\,(\mathsf{trail}_k\ R\,(R\ ;\ \mathcal{D}))\ \backslash\!\backslash\ [\triangle\,\mathcal{D}, \tilde{\triangle}\,\mathcal{D}]^{-1}\ ;\ [\mathcal{D}^{-m}, \mathcal{D}^{-n}]\end{aligned}$$

d The band matrix multiplier $BM0$ is given by

$$BM0 \;=\; \mathsf{grid}_{mk,nk}\,Ma0$$

where $Ma0 = Mac\ ;\ \mathsf{snd}\,(\mathsf{fst}\,\mathcal{D})$ and Mac is a combinational circuit with two connections on every side, inputs on the left and top, and outputs on the right and bottom. Derive an expression for $BM1$, a band matrix multiplier obtained by pipelining every k cells of $BM0$.

e How many latches, excluding those at the interface for skewing dataflow, are there in $BM1$?

The five parts carry, respectively, 15%, 20%, 35%, 15% and 15% of the marks.

End of paper