MATTER

E1.2

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2005

EEE/ISE PART I: MEng, BEng and ACGI

DIGITAL ELECTRONICS 1

Monday, 23 May 10:00 am

Time allowed: 2:00 hours

There are FOUR questions on this paper.

Q1 is compulsory.
Answer Q1 and any two of questions 2-4.
Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung
Second Marker(s) : K. Masselos

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X[7:0] is an eight bit bus with X7 being the most significant bit (MSB) and X0 the least significant bit (LSB).

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

[Question 1 is compulsory]

1 a) Given that the hexadecimal code for the ASCII character 'A' is 41, and assuming that all numbers are represented using 8 bits, complete the missing entries which are not shaded in the following table. (No marks will be awarded for this question unless you show how the solutions are derived.)

Binary	Hexadecimal	Unsigned Decimal	Signed Decimal	ASCII
?		71		?
10011011	?		?	

[8]

b) Simplify the following Boolean expressions using De Morgan's theorem and Boolean algebra.

i) $\overline{A \bullet \overline{(B + \overline{C})} \bullet D}$

ii) $\overline{(P + \overline{Q}) \bullet (\overline{P} + Q)}$

[6]

c) Simplify the following Boolean equation using Karnaugh map.

i) $x = \overline{A} \bullet \overline{B} \bullet \overline{C} + \overline{A} \bullet B \bullet C + A \bullet B \bullet C + A \bullet \overline{B} \bullet \overline{C} + A \bullet \overline{B} \bullet C$

ii) $y = \overline{(C + D)} + \overline{A \bullet C \bullet \overline{D}} + A \bullet \overline{B} \bullet \overline{C} + \overline{A} \bullet B \bullet C \bullet D + A \bullet C \bullet D$

[8]

d) Draw the truth table for the circuits shown in *Figure 1.1* and *Figure 1.2*.

[8]

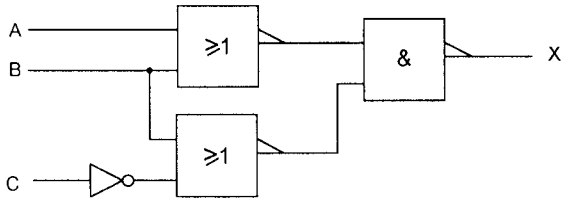


Figure 1.1

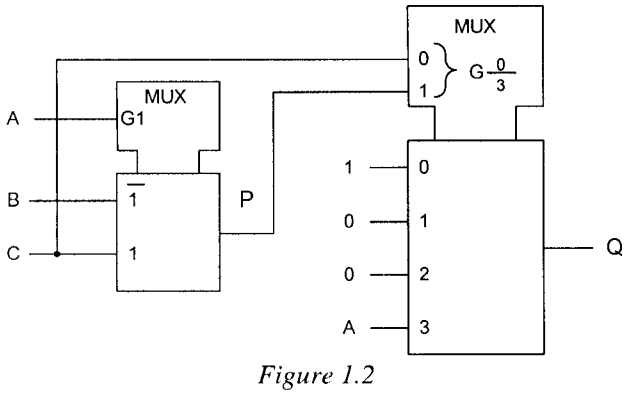
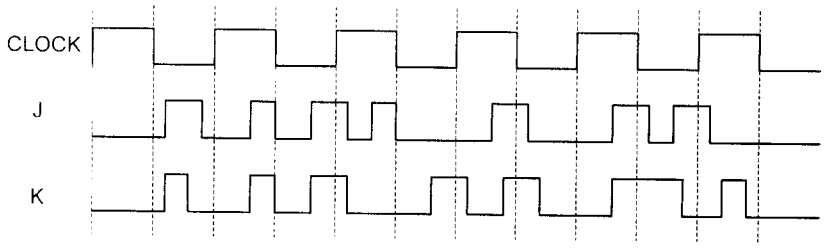


Figure 1.2

e) Sketch out the following Boolean equation using a programmable logic device (PLD).

$$f = A \bullet (B \oplus C)$$

[5]



g) Draw a state transition table for the Moore finite state machine (FSM) specifed by the state diagram shown in *Figure 1.4*.

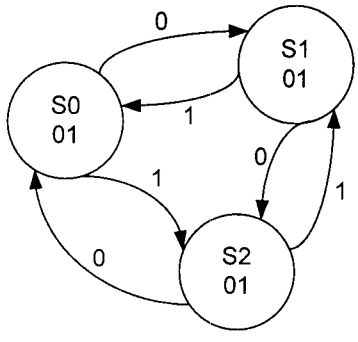


Figure 1.4

[5]

2. *Figure 2.1* shows the circuit schematic of a synchronous finite state machine (FSM) containing two D-type flip-flops, an 8-to-1 multiplexer and different types of logic gates. The FSM has two inputs X and Y, one output Z, and two internal state variables A and B. The output P of the multiplexer is connected to the D input of flip-flop A. The internal signal Q is connected to the D input of flip-flop B.

a) Derive the Boolean equations for P, Q and Z.

[8]

b) Derive the state transition table of the FSM assuming that the four states are known as S0, S1, S2 and S3, and that the following encoding is used:

S0: A = 0, B = 0
S1: A = 0, B = 1
S2: A = 1, B = 0
S3: A = 1, B = 1

[12]

c) Hence or otherwise, draw the state diagram of the FSM.

[10]

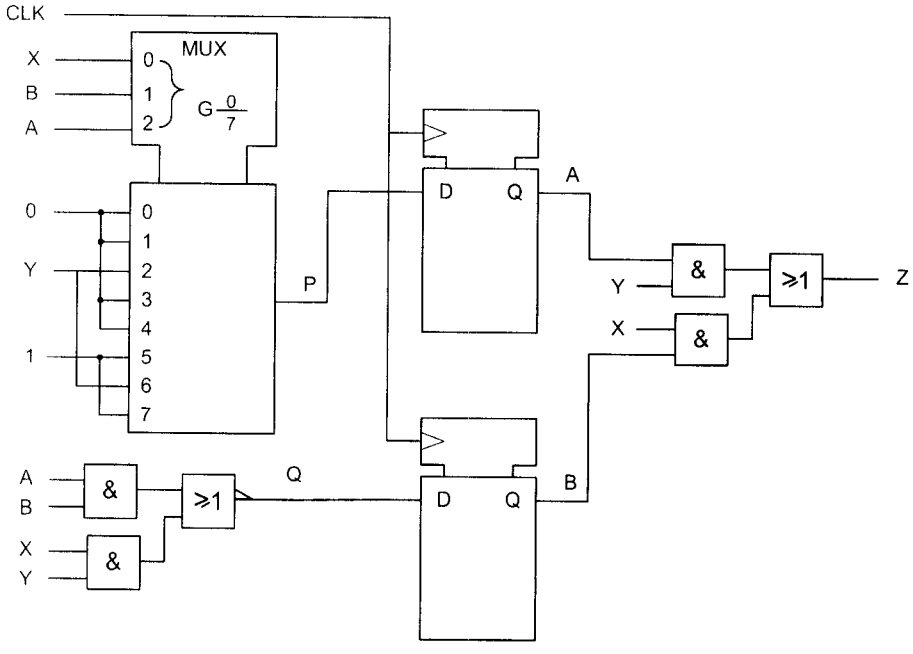


Figure 2.1

3. Figure 3.1 shows an 8 × 2 bit read-only-memory (ROM) used as 1-bit full adder circuit. Its address signals are connected to A, B and C, where A is the least significant bit (LSB) and C is the most significant bit (MSB) of the address bus. The LSB and MSB of the data bus provide the sum S_OUT and carry COUT signals respectively.

a) Draw a table showing the contents of the ROM.

[8]

b) Using four of the ROMs defined in part a) and other suitable logic gates, design a circuit that performs the operation (P – Q), where P and Q are 4-bit signed numbers in 2's complement form.

[10]

c) A different ROM is required to implement an adder that adds together two 2-bit unsigned numbers.

i) What is the minimum size of the ROM required?

[2]

ii) How many data bits are required and why?

[2]

iii) Draw a table showing the contents of this ROM.

[8]

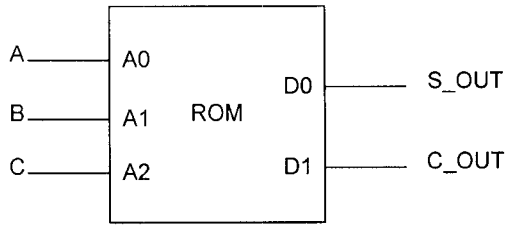


Figure 3.1

4. *Figure 4.1* shows a finite state machine (FSM) with 7 output signals A, B, C, D, E, F and G driving a 7-segment display. A segment of the display is turned on when the corresponding input signal is high. *Figure 4.2* shows the segment patterns that are turned on when the numbers 1, 2, 4 and 8 are displayed.

a) Draw a state diagram for the FSM such that the 7-segment display cycles through the number sequence 1 → 2 → 4 → 8 → 1 → 2 → 4..... Indefinitely.

[2]

b) Hence or otherwise, derive the state transition table for the FSM.

[8]

c) Assuming D type flip-flops are used for storage, design the FSM in the form of Boolean equations.

[10]

d) Implement the FSM using flip-flops and logic gates.

[10]

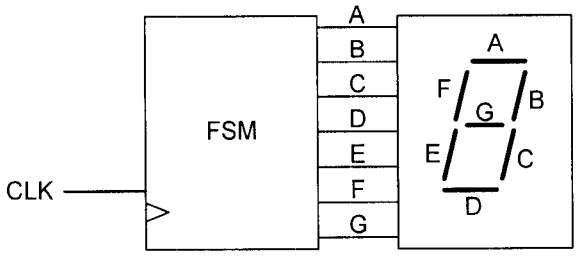


Figure 4.1

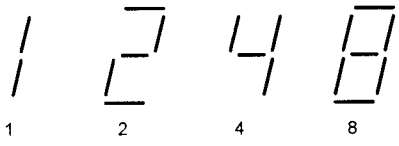


Figure 4.2

[THE END]

MASTER

E1.2 Digital Electronics 1
Solutions 2005

All questions are unseen.

Question 1 is compulsory.

a)

Binary	Hexadecimal	Unsigned Decimal	Signed Decimal	ASCII
10011011	**9B**		**-101**	
01000111		71		**'G'**

[8]

b) i) $\overline{A \bullet \overline{(B + \overline{C})} \bullet D} = \overline{A \bullet (\overline{B} \bullet C) \bullet D} = \overline{A} + B + \overline{C} + \overline{D}$

ii) $\overline{(P + \overline{Q}) \bullet (\overline{P} + Q)} = \overline{P} \bullet Q + P \bullet \overline{Q} = P \oplus Q$

[6]

c) Simplify the following Boolean equation using Karnaugh map.

	AB	$A\overline{B}$	$\overline{A}\,\overline{B}$	$\overline{A}B$
C	1	1	0	1
$\overline{C}$	0	0	1	1

i) $x = \overline{A} \bullet \overline{B} \bullet \overline{C} + \overline{A} \bullet B \bullet C + A \bullet B \bullet C + A \bullet \overline{B} \bullet \overline{C} + A \bullet \overline{B} \bullet C$

$= AC + BC + \overline{A}\,\overline{C}$ *or* $\overline{B}\,\overline{C} + BC + A\,\overline{B}$

[4]

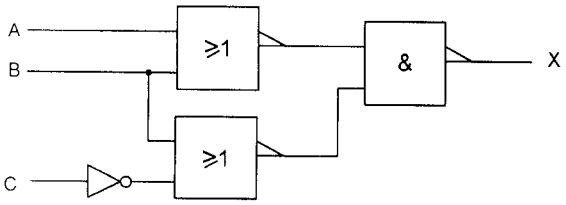
	$A\overline{B}$	AB	$\overline{A}B$	$\overline{A}\,\overline{B}$
$\overline{C}\,\overline{D}$	1	1	1	1
$\overline{C}D$	1	1	1	1
CD	1	1	1	1
$C\overline{D}$	0	0	1	1

ii) $y = \overline{(C + D)} + \overline{A \bullet C \bullet \overline{D}} + A \bullet \overline{B} \bullet \overline{C} + \overline{A} \bullet B \bullet C \bullet D + A \bullet C \bullet D$

Simplifies to $y = \overline{A} + \overline{C} + D$

[4]

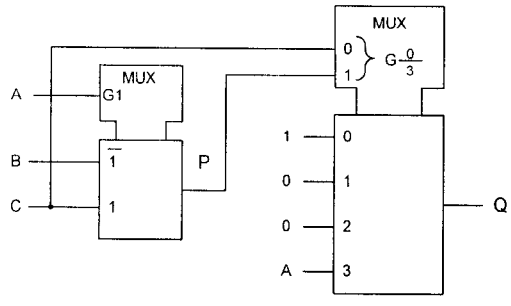
d) i)



A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

[4]

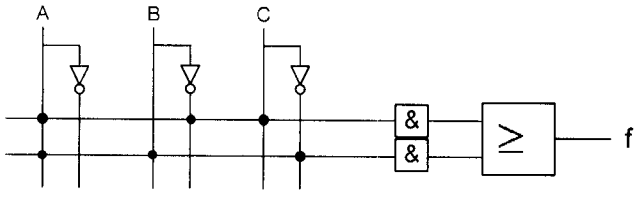
ii)



A	B	C	P	Q
0	0	0	0	1
0	0	1	0	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	1	1
1	1	0	0	1
1	1	1	1	1

[4]

e) $f = A \bullet (B \oplus C) = A\overline{B}C + AB\overline{C}$



[5]

f)

Students asked to ignore part f).

g)

Current State	X	Next state	Current output P:Q
S0	0	S1	01
S0	1	S2	01
S1	0	S2	01
S1	1	S0	01
S2	0	S0	01
S2	1	S1	01

[5]

2. a)

$$P = A^+ = AX + B\overline{X}Y$$

$$Q = B^+ = \overline{XY + AB}$$

$$Z = AY + BX$$

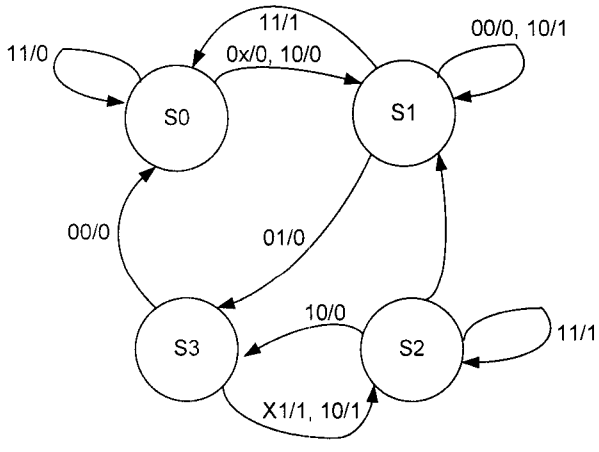
[8]

b)

State	A	B	X	Y	$P=A^+$	$Q=B^+$	Z
S0	0	0	0	0	0	1	0
	0	0	0	1	0	1	0
	0	0	1	0	0	1	0
	0	0	1	1	0	0	0
S1	0	1	0	0	0	1	0
	0	1	0	1	1	1	0
	0	1	1	0	0	1	1
	0	1	1	1	0	0	1
S2	1	0	0	0	0	1	0
	1	0	0	1	0	1	1
	1	0	1	0	1	1	0
	1	0	1	1	1	0	1
S3	1	1	0	0	0	0	0
	1	1	0	1	1	0	1
	1	1	1	0	1	0	1
	1	1	1	1	1	0	1

[12]

c)



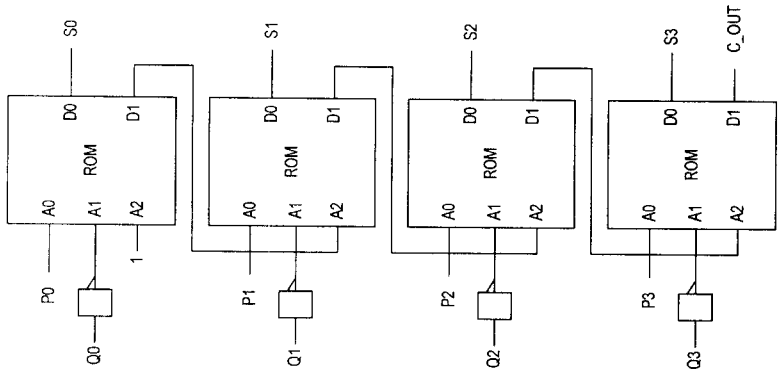
[10]

3 a)

Address	C_OUT	S_OUT	Content of ROM
000	0	0	0
001	0	1	1
010	0	1	1
011	1	0	2
100	0	1	1
101	1	0	2
110	1	0	2
111	1	1	3

[8]

b)



[10]

c) i) ROM which 16 locations is required (4 address bits).

[2]

ii) 3 data bits because the maximum sum value is 6, which need 3 bits to represent.

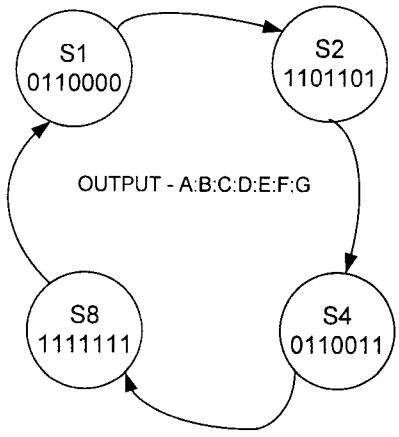
[2]

iii)

Address	**Content**
0	0
1	1
2	2
3	3
4	1
5	2
6	3
7	4
8	2
9	3
10	4
11	5
12	3
13	4
14	5
15	6

[8]

4 a)



[2]

b)

Display value	Current FSM output A B C D E F G	Next FSM output A^+ B^+ C^+ D^+ E^+ F^+ G^+
1	0 1 1 0 0 0 0	1 1 0 1 1 0 1
2	1 1 0 1 1 0 1	0 1 1 0 0 1 1
4	0 1 1 0 0 1 1	1 1 1 1 1 1 1
8	1 1 1 1 1 1 1	0 1 1 0 0 0 0

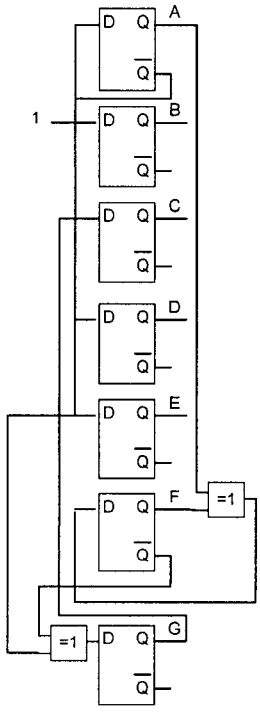
[8]

c) Assuming the use of D-type FF. By inspection:

$$A^+ = \overline{A}$$
$$B^+ = 1$$
$$C^+ = G$$
$$D^+ = \overline{A}$$
$$E^+ = \overline{A}$$
$$F^+ = A\overline{F} + \overline{A}F$$
$$G^+ = \overline{A} + \overline{F}$$

[10]

d)



[10]