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AO8

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2006

MSc and EEE PART III/IV: MEng, BEng.and ACGI

ADVANCED ELECTRONIC DEVICES

Corrected Copy

Thursday, 27 April 2:30 pm

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer Question ONE and THREE other questions.

All questions carry equal marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : K. Fobelets, K. Fobelets
Second Marker(s) : W.T. Pike, W.T. Pike

Special information for invigilators: Q1 is Compulsory

Information for candidates

Electron charge:	$e = 1.6\ 10^{-19}$ C
Permittivity of free space:	$\varepsilon_o = 8.85 \times 10^{-12}$ F/m
Permeability of free space:	$\mu_o = 4\pi \times 10^{-7}$ H/m
Density of states:	$N_C = 7\ 10^{18}$ cm^{-3} for both GaAs and AlGaAs
Relative permittivity:	$\varepsilon = 13$ for both GaAs and AlGaAs
Bandgap GaAs:	$E_G^{GaAs} = 1.4eV$
Bandgap AlAs:	$E_G^{AlAs} = 2.1eV$
Thermal energy:	$kT/e = 0.026\ eV$ at $T = 300K$

Formulae

$$\left.\begin{aligned} J_n(x) &= e\mu_n n(x)E(x) + eD_n \frac{dn(x)}{dx} \\ J_p(x) &= e\mu_p p(x)E(x) - eD_p \frac{dp(x)}{dx} \end{aligned}\right\}$$

Drift and diffusion currents in a semiconductor

$$I_{DS} = \frac{\mu C_{ox} W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

Drain current in MOSFET (Metal-Oxide-Field-Effect-Transistor)

$$V_T = \frac{1}{e}(\phi_b - \phi_n) - \frac{eN_D a^2}{2\varepsilon}$$

Threshold voltage of MESFET (Metal Semiconductor Field Effect Transistor) Note: first term is built-in voltage.

$$V_T = \frac{1}{e}[\phi_b - \Delta E_c] - \frac{eN_D d^2}{\varepsilon}$$

Threshold voltage in HEMT (High Electron Mobility Transistor)

$$n = N_C \exp\left[\left(E_F - E_c\right)\Big/ kT\right]$$

Free electron concentration

$$S = \left(\frac{d\log(I_{DS})}{dV_{GS}}\right)^{-1}$$

Sub-threshold slope

1. **Compulsory.**

a) What type of gate is used in a GaAs/AlGaAs HEMT? [2]

b) V_{T1} and μ_1 is respectively the threshold voltage and the mobility of an enhancement mode n-MOS with a bulk doping N_{A1}. V_{T2}, μ_2 and N_{A2} are the parameters of a second enhancement n-MOS of the same geometry. Give the relationship (>,< or =) between the threshold voltages and between the mobilities of the two MOSFETs when $N_{A1}>N_{A2}$. [2]

c) In the formulae list the bandgap of GaAs and AlAs at the Γ point in k-space are given. Calculate the bandgap of $Al_{0.3}Ga_{0.7}As$ at the Γ point. [2]

d) Give the reason for the discrepancy between the theoretical (dashed line) and measured (full line) drain current characteristics of a MOSFET given in fig.1.1. You can assume no short channel effects occur. The theoretical curve is calculated using the I_{DS} equation in the formulae list. [2]

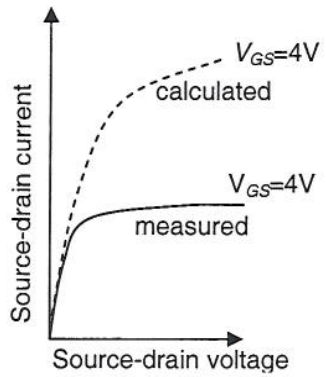

Figure 1.1: the calculated (dashed line) and measured (full line) characteristics of an enhancement mode MOSFET.

e) Given the energy band diagram of the an-isotype heterojunction in fig.1.2, do you expect the energy level in the quantum well E_0 to be populated with holes, electrons or no carriers. Explain your answer **briefly**. [2]

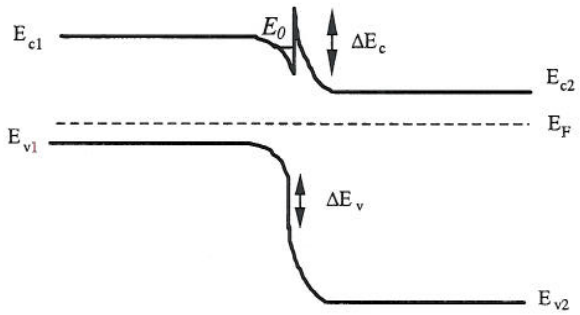

Figure 1.2: Energy band diagram of an an-isotype heterojunction.

f) Which two scattering effects, normally present in a MOSFET, would be reduced when using a modulation-doped buried-channel field-effect-transistor? [2]

Question continues on next page

g) In fig. 1.3 a TEM (transmission electron microscope) picture is given of the cross section of a relaxed SiGe graded layer (virtual substrate). What are the white lines that occur in the graded SiGe layer? [2]

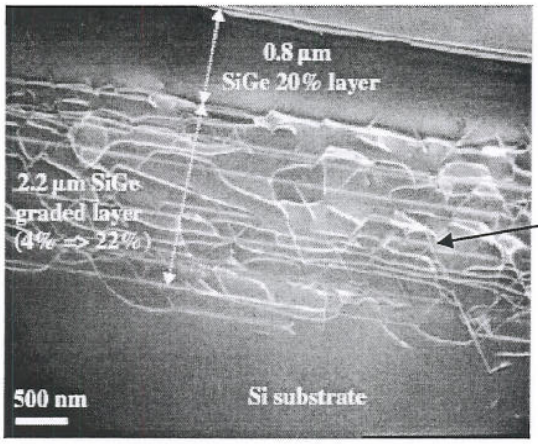

Figure 1.3: the TEM cross section of a Si/SiGe graded layer/$Si_{0.8}Ge_{0.2}$ heterojunction (pic. J.M. Hartmann).

h) Which type of strain is preferred in the channel of a strained channel **p**-MOS? [2]

i) Sketch a mushroom gate and explain briefly why it is used. [2]

j) What is the difference between fully depleted (FD) and partially depleted (PD) SOI when applied to MOSFETs? [2]

2. Heterojunction FETs.

a) A student, who did not join the AED course, fabricates an n-channel strained-Si enhancement-mode MOSFET using a **non**-self-aligned process. Why is there no current flowing from source to drain at relatively low drain voltage? [2]

b) The conduction band minimum of Si is six-fold degenerate. Does applying tensile strain in Si via the use of a SiGe virtual substrate change the degeneracy? If yes, what is the resulting degeneracy value? If no, why not? [2]

c) The lattice constant of Si is $a_{Si} = 5.4$ Å and Ge is $a_{Ge} = 5.65$ Å and the band offsets are given in fig.2.

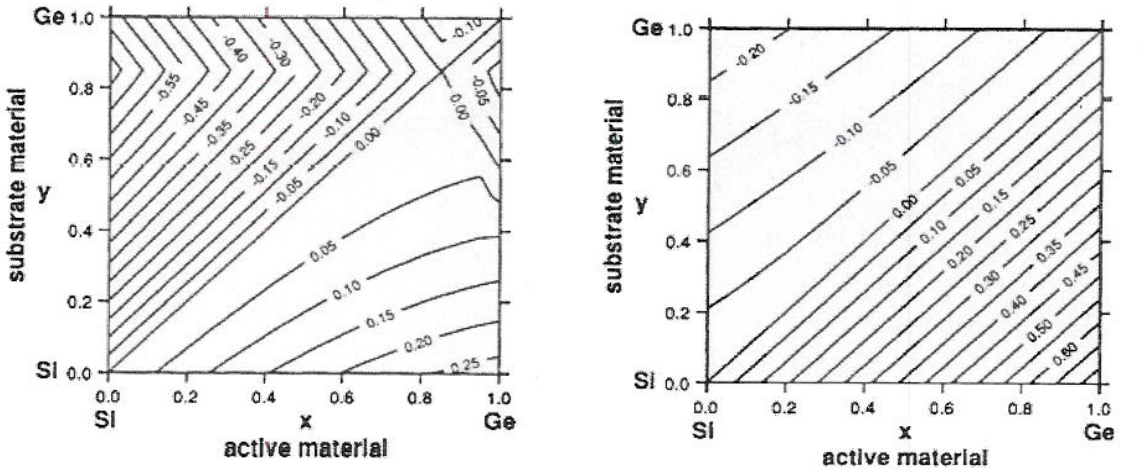

Figure 2: Left: conduction band offset and right: valence band offset between the strained active layer and the relaxed substrate as a function of Ge concentration.

Answer the following two questions.

i) Is the strain tensile or compressive in a strained $Si_{0.4}Ge_{0.6}$ layer epitaxially grown on top of a relaxed $Si_{0.8}Ge_{0.2}$ substrate? [2]

ii) Sketch the conduction and valence band across the $Si_{0.4}Ge_{0.6}/Si_{0.8}Ge_{0.2}$ heterojunction (on separate graphs). Add an approximate value of the band offsets. You can ignore any charge re-distribution that might occur. [6]

d) An n-channel depletion mode HEMT is made from un-GaAs and n-AlGaAs.

i) In which material is the conducting channel formed? [2]

ii) Why is there an undoped AlGaAs spacer layer between the GaAs and the n-AlGaAs layers? [2]

iii) Give the expression of the difference between the threshold voltage of the MESFET and HEMT if you know that the Fermi level is pinned at the same distance from the conduction band in both devices. You can use the 60/40 rule for the band offsets between AlGaAs and GaAs. [4]
ϕ_b/e = 0.8V for a GaAs MESFET.
N_D = 7 10^{17} cm^{-3} for both devices
$a = d$ = 50nm
T = 300K

3.

a) Give two reasons that explain why the introduction of high-k dielectrics for the gate insulator is unsuccessful? [2]

b) The oxide thickness of the MOS-gate is t_{ox}= 2nm. What must the thickness of the high-k dielectric be to give the same gate insulator capacitance when the relationship between the dielectric constants is $\varepsilon_{high\text{-}k}=4\varepsilon_{ox}$. [2]

c) Fig. 3 gives the cross section of two identical MOSFETs apart from the retrograde well.

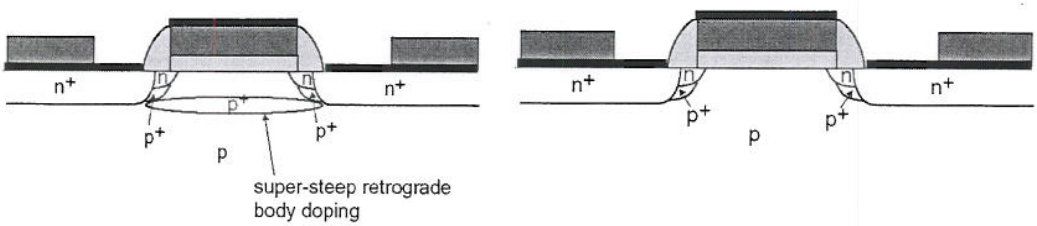

Figure 3: Left: the material cross section of a Si MOSFET with a retrograde well. Right the same Si MOSFET but without retrograde well doping.

i) Sketch the energy band diagram, from gate to bulk (substrate), in the middle between source and drain, for the two MOSFETs when all contacts are grounded. You can assume that the workfunction of the gate contact and the semiconductor are identical. [4]

ii) Sketch the energy band diagram from gate to bulk (substrate), in the middle between source and drain, for the same two MOSFETs but now applying a positive voltage on the bulk contact, leaving all other contacts grounded. Assume the p^+ layer acts as a metal. [5]

iii) Which of the two MOSFETs sees the biggest threshold voltage change when the bulk is positively biased? [2]

d) Sketch the source-drain current versus the source-drain voltage (I_{DS}-V_{DS}) characteristics of a long channel enhancement mode NMOS in strong inversion, for **both positive** and **negative** drain voltages. Give a brief reason for your graph.
Tip: look carefully at the voltage relationship for current saturation. [5]

4.

a) Consider a fully depleted SOI nMOS and a fully depleted n-channel finFET with the same geometrical parameters and the same channel doping and gate material. Compare both devices by choosing the correct relationship below and add a **brief** reason for your answer.

i) Drain induced barrier lowering: $DIBL_{FDSOI} \left\{ \begin{matrix} > \\ < \\ \approx \end{matrix} \right\} DIBL_{finFET}$ [3]

ii) Sub-threshold slope: $S_{FDSOI} \left\{ \begin{matrix} > \\ < \\ \approx \end{matrix} \right\} S_{finFET}$ [3]

iii) On-current: $I_{on_{FDSOI}} \left\{ \begin{matrix} > \\ < \\ \approx \end{matrix} \right\} I_{on\ finFET}$ [3]

b) Sketch the different steps needed for fabricating strained-Si on insulator (s-SOI). Label each step. [5]

c)

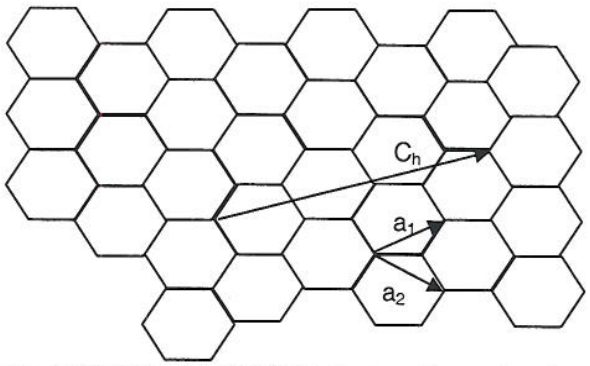

Figure 4: Honeycombed lattice of a graphene sheet.

i) Given the unit vectors a_1 and a_2 and the angle θ between the direction of a_1 and the chirality vector C_h as given in fig.4, plot the chirality vector for a zig zag and for a stair case carbon nanotube. [4]

ii) Which of these two graphene folding methods (zig zag or staircase) gives always a metallic carbon nanotube? [2]

5. Questions based on reading assignments

a) What physical process causes current in the sub-threshold region of MOSFETs? [2]

b) Discuss why the threshold voltage V_T controls the off-state leakage current I_{off}. Remember that the sub-threshold current is given by the expression:

$$I_D \cong I_0 \exp\left(\frac{q(V_{GS}-V_T)}{\left(1+C_{depl}/C_{ox}\right)kT}\right)$$

With I_0, a constant depending on temperature, C_{depl} and C_{ox} the depletion and oxide capacitance, respectively. [4]

c)

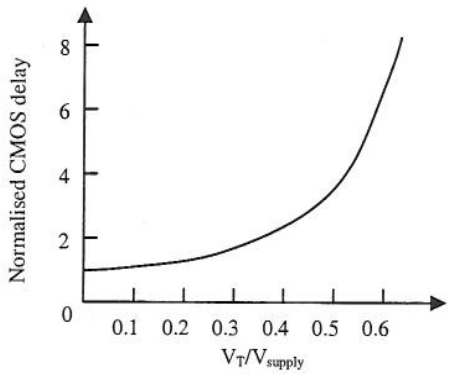

Figure 5: Gate delay/stage of a 1.5V CMOS inverter versus the threshold voltage-supply voltage ratio.

Given fig.5 and your answer in b), explain why there is little performance to be gained by scaling the supply voltage below 1V. [4]

d) Derive an expression for the subthreshold slope S in terms of oxide thickness and depletion width. [4]

e) Sketch the cross section of a *tensile* strained-Si MOSFET for both local and global strain. Indicate all materials used and indicate the strain direction in the channel in both cases. Ensure you label your sketches. [6]

6. Essay based on coursework research.

Describe, using diagrams as appropriate, what is understood by **Si nanowires**. For instance what are the general dimensions of Si nanowires?
Describe two application areas for Si nanowires and comment on their potential impact on electronic devices in the future.
What do you see as the main stumbling block in the future exploitation of nanowire technology.
Ensure your answer is concise (suggested word count: 300 – 400 words). [20]

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Answers AED 2006

1. **Compulsory.**

a) Schottky gate or metal-semiconductor contact. [2]

b) $V_{T1} > V_{T2}$
and
$\mu_1 < \mu_2$ [2]

c) $E_G^{AlGaAs} = 0.7E_G^{GaAs} + 0.3E_G^{AlAs} = 0.7 \times 1.4eV + 0.3 \times 2.1eV = 1.61eV \cong 1.6\,eV$. [2]

d) Current saturation in the measured curve is due to velocity saturation happening before the pinch-off of the channel at the drain side is reached. [2]

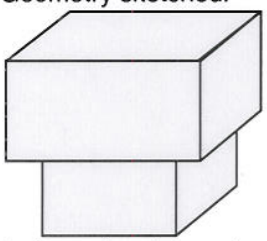
e) No carriers because the position of the Fermi level E_F is far away in energy from the energy level in the conduction band, so the chance of finding an electron is small. Since the energy level is in the conduction band: no holes. [2]

f) Impurity scattering and interface scattering at the gate. [2]

g) Are the dislocations that occur due to the relaxation in the graded layer. [2]

h) Compressive strain. [2]

i) For reducing the gate resistance and thus reducing the gate RC constant.
Geometry sketched: [2]



bottom of metal mushroom gate is attached to semiconductor and is small to allow small gate lengths. Top is made wider to reduce the resistance

j) In FDSOI the channel region is completely depleted when $V_{GS}=0V$ whilst in PDSOI a narrow undepleted region remains. [2]

2.

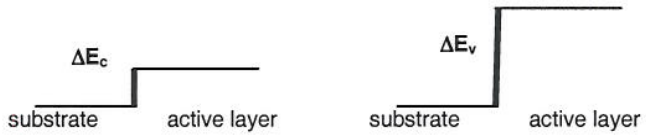
a) When an enhancement mode device is processed non-self-aligned then the ohmic contact implants from source and drain do not touch the region that is controlled by the gate. This means that there are access regions where source and drain do not contact the inversion region. [2]

b) yes, 2 (lowest lying levels) [2]

c)

i) Compressive strain because the lattice constant of bulk $Si_{0.4}Ge_{0.6}$ is larger than bulk $Si_{0.8}Ge_{0.2}$. $a(Si_{0.4}Ge_{0.6})=0.4a_{Si} + 0.6a_{Ge}$ and $a(Si_{0.8}Ge_{0.2})=0.8a_{Si} + 0.2a_{Ge}$. [2]

ii) [6]



Conduction band
ΔE_c=0.1eV and ΔE_v=0.35eV

Valence band

d)

i) GaAs [2]

ii) To reduce coulomb scattering [2]

iii) Due to Fermi level pinning the Schottky barrier is the same in each material, thus the remaining difference is: [4]

$$V_T^{MESFET} - V_T^{HEMT} = \frac{1}{e}\left(-\phi_n + \Delta E_c\right)$$

$$\Delta E_c = 0.6\left(\Delta E_g\right) = 0.6\left(2.1-1.4\right) = 0.42eV$$

$$\phi_n / e = \left(E_c - E_f\right)/e = \frac{kT}{e}\ln\left(\frac{N_C}{n}\right) = 0.026\ln\left(\frac{710^{18}}{710^{17}}\right) = 0.06eV$$

$$V_T^{MESFET} - V_T^{HEMT} = 0.36V$$

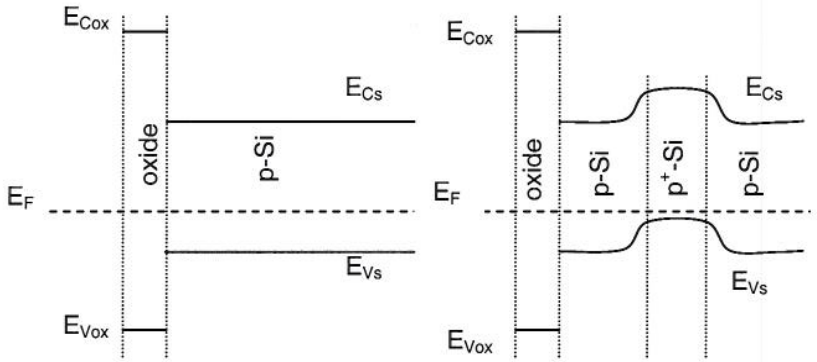
3.

a) Because of the poor quality of the interface between deposited dielectric and silicon surface (high interface-state density) and because of the large amount of charges in the dielectric. [2]

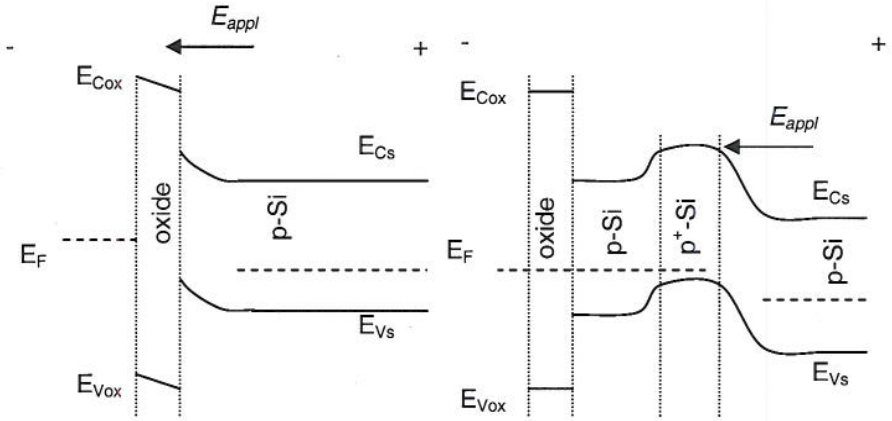
b) $t_{high\text{-}k}$ = 8nm. [2]

c)

i) [4]

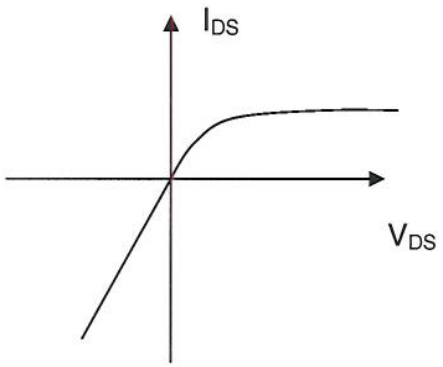


ii) [5]



iii) The MOSFET without retrograde doping sees the largest threshold voltage change as the p^+ doping screens the action of the bulk on the channel region underneath the oxide. [2]

d) Current saturation is reached when $V_{DS}>V_{GS}-V_T$. When V_{DS} is positive this implies that the current I_{DS} becomes constant at this drain voltage. However when V_{DS} is negative, the condition for saturation cannot be met because $V_{GS}>V_T$ in order for the MOSFET to be "on" and thus $V_{GS}-V_T>0$ or $V_{DS}<V_{GS}-V_T$ always when $V_{DS}<0$. Note that current saturation can occur for velocity saturation. [5]



4.

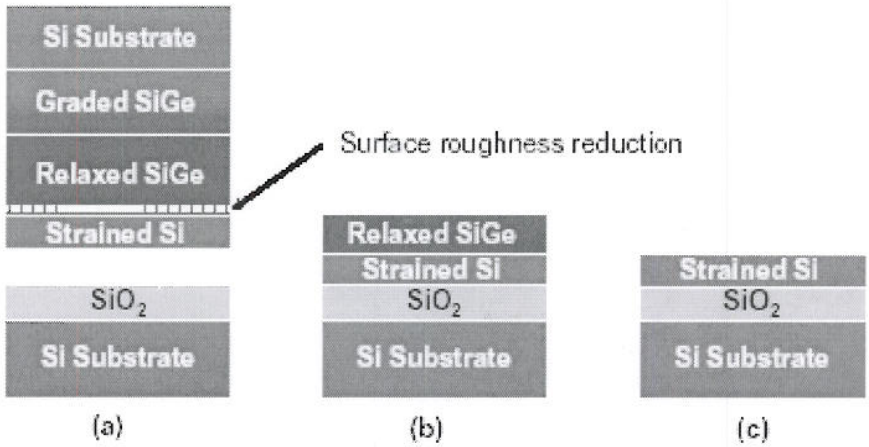
a)

i) Drain induced barrier lowering: $DIBL_{FDSOI} > DIBL_{finFET}$. DIBL in the finFET is smaller because of the double gate action. [3]

ii) Sub-threshold slope: $S_{FDSOI} \approx S_{finFET}$. S is more or less equal. The sub-threshold slope is determined by the ratio of the depletion capacitance C_B to the oxide capacitance, C_{ox}. As C_{ox} is the same for both devices and FDSOI is fabricated on SOI, whilst the body of the finFET is always depleted (for all V_{GS}), C_B will be equally small in both cases. [3]

iii) On-current: $I_{on_{FDSOI}} < I_{on_{finFET}}$ because the finFET has two conducting channels whilst the FDSOI has only one. [3]

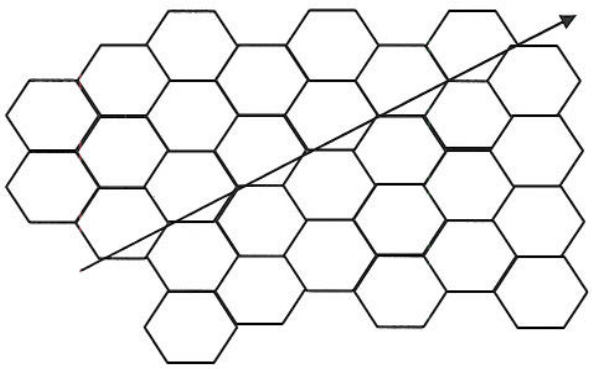
c) Using Smart-cut process [5]



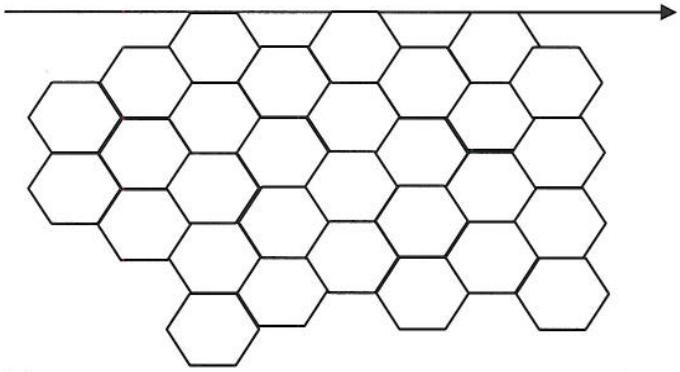
(a) H_2 implantation in strained-Si on virtual substrate wafer (implant peak into relaxed SiGe). Then cleaned.
Thermally oxidised wafer is cleaned and then the two wafers are pushed together (Van der Waals bonding) → wafer bonding
(b) Anneal of the bonded wafers splits them at the H_2 peak.
(c) CMP (chemical mechanical polishing) is done to remove the SiGe layer and to smoothen the surface of the strained-Si layer.

d)

i) [4]



zig zag



staircase

ii) zig zag [2]

5. Questions based on reading assignments

a) Diffusion - which is due to the larger amount of free carriers at high energies at the source than at the drain. [2]

b) I_{off} is the sub-threshold current at $V_{GS}=0$ in enhancement mode devices. Thus:

$$I_{OFF} \cong I_0 e^{\left(\frac{-q(V_T)}{\left(1+C_{depl}/C_{ox}\right)kT}\right)}$$

This implies that the off current is exponentially dependent on the threshold voltage such that off-current increase exponentially with a linear decrease in V_T. [4]

c) From b) we know that if we reduce the threshold voltage, the off-currents will increase. This will limit the minimum value for the threshold voltage. If we would decrease the supply voltage whilst having to keep V_T at a minimum but non-zero value, we would limit the gate voltage swing and thus the gate overdrive V_{GS}-V_T degrading performance. From fig.5 we also see that the gate delay increases rapidly when the ratio V_T/V_{supply} increases leading to no gain in performance via further downscaling of V_{supply}. [4]

d) Thus S decreases with decreasing oxide thickness t_{ox}. [4]

$$I_{DS} \cong I_0 \exp\left(\frac{q(V_{GS}-V_T)}{nkT}\right)$$

$$n = \left(1+C_{depl}/C_{ox}\right)$$

$$S = \left(\frac{dLog(I_{DS})}{dV_{GS}}\right)^{-1}$$

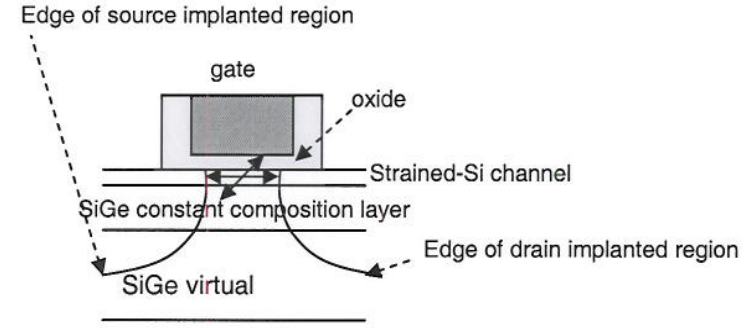
$$S = \frac{kT}{q}n = \left(1-\frac{C_{depl}}{C_{ox}}\right)$$

$$C_{ox} = \frac{\varepsilon}{t_{ox}}$$

$$S = \frac{kT}{q}\left(1+t_{ox}\varepsilon_{depl}/t_{depl}\varepsilon_{ox}\right)$$

e) [6]

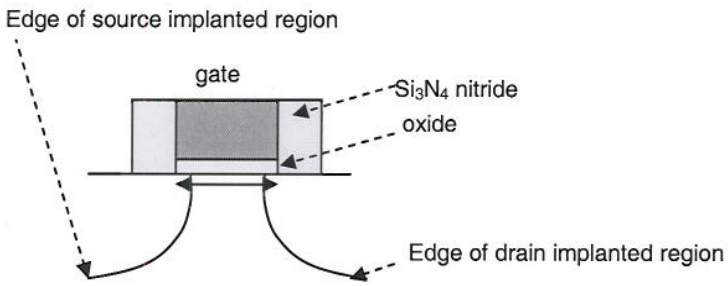
GLOBAL STRAIN



Si substrate

Strain in two directions (biaxial) indicated in channel

LOCAL STRAIN



Si substrate

Strain in one directions (uniaxial) indicated in channel

6. Essay based on coursework research.

Describe, using diagrams as appropriate, what is understood by **Si nanowires**. For instance what are the general dimensions of Si nanowires?
Describe two application areas for Si nanowires and comment on their potential impact on electronic devices in the future.
What do you see as the main stumbling block in the future exploitation of nanowire technology.
Ensure your answer is concise (suggested word count 300 – 400 words). [20]