Paper Number(s): **E1.2**

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2002

EEE/ISE PART I: M.Eng., B.Eng. and ACGI

DIGITAL ELECTRONICS I

Friday, 24 May 10:00 am

There are FIVE questions on this paper.

Question 1 is compulsory.

Answer THREE questions, including Question 1.

Time allowed: 2:00 hours

Examiners responsible:

First Marker(s): Naylor,P.A.

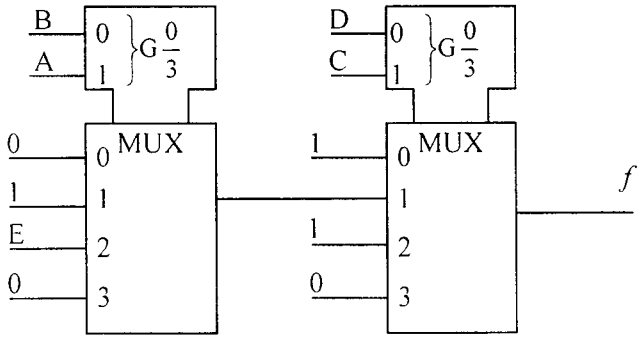
Second Marker(s): Aleksander,I.

Corrected Copy

Nine

[Question 1 is compulsory]

1. a) Determine the Boolean function f.



[3]

b) (*No marks will be awarded for this question unless you show your working.*) [3]

Convert $(1.6875)_{10}$ to twos-complement binary.
Express $(-39)_{10}$ in 8-bit sign-magnitude binary form.
Express $(-39)_{10}$ in twos-complement binary form.

c) (*No marks will be awarded for this question unless you show your working.*)

Express the following bit pattern as a hexadecimal number. [4]

0 1 0 0 0 1 1 0 1 1 1 1 1 1 1 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Interpret the same bit pattern as a single precision floating point number and give its value to base 10.

d) Draw the Karnaugh map of the following function:

$$f = (\overline{A} + \overline{B})(\overline{B} + \overline{D})(\overline{A} + \overline{D})(\overline{C} + \overline{D})$$ [4]

State the number of gates required to implement this function, not counting inverters and sketch the circuit diagram.

e) Draw the flip-flop transition table for a JK flip-flop. [4]

Clearly show how the operation of a toggle flip-flop could be deduced from this flip-flop transition table.

f) Sketch the symbol for a Schmitt trigger and describe in summary its operation and application. [2]

2. The symbol for a 4-bit bi-directional shift register is shown in Fig. 1 The device has four modes as determined by the binary value of S1:0. Deduce the features of these four modes and give your answer by copying and completing Table 1. [6]

State the meaning and effect on the operation of the device of each of the inputs and outputs in Table 2. [7]

Sketch the circuit diagram of the internal structure of the device using gates and flip-flops. [7]

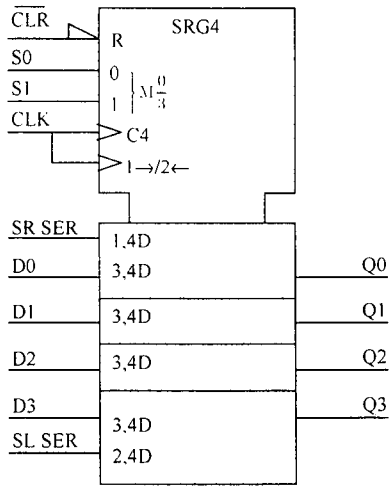


Fig. 1

Mode	S1	S0	Action of the device
0	0	0	
1	0	1	
2	1	0	
3	1	1	

Table 1

Signal	Meaning
CLK C4	
CLK 1→/2←	
CLR	
SR SER	
SL SER	
D3:0	
Q3:0	

Table 2

3. a) Prove using Boolean algebra $A + \overline{A}B = A + B$. [4]

b) Simplify the following expression using Boolean algebra. [4]

$$\overline{AB + AC} + \overline{A}.\overline{B}C$$

c) Express $\overline{\overline{A + B} + C}$ in canonical SOP form. [4]

d) Using a Karnaugh map, find minimal SOP and POS expressions for [4]

$$f = \sum 0,2,4,6,7,10,13,14,15$$

e) Draw the circuit diagram of the implementation of an XNOR gate using [4]
(i) the minimum number of discrete AND, OR and NOT gates
(ii) a multiplexer having 1 select input.

4. Draw a Moore-model state diagram of a 3-bit UP/DOWN gray code counter. [6]

Write down the state transition table for this state machine. [5]

Draw the circuit diagram of the implementation of this state machine using D-type flip-flops and give any relevant Boolean equations. [9]

5. State and compare the main features of synchronous and asynchronous binary counters. [4]

Using falling-edge triggered, resetable, J-K flip-flops, design an asynchronous binary counter which counts the sequence

0, 1, 2, ..., 10, 11, 0, 1, 2, ...

Show a labelled circuit diagram for the counter. [7]

Sketch a timing diagram of duration 14 counts and indicate the position of any glitches. [6]

State which device parameter limits the maximum speed of operation of the counter. Suggest a typical value for this parameter and hence calculate the maximum speed of operation for this suggested value. [3]

DIGITAL ELECTRONICS 1

E1.2 SOLUTIONS 2002
[Question 1 is compulsory]

1. a) $p = \overline{A}B + A\overline{B}E$

$f = \overline{C}.\overline{D} + \overline{C}Dp + C\overline{D} = \overline{D} + \overline{C}p = \overline{D} + \overline{A}.B.\overline{C} + A.\overline{B}.\overline{C}.E$

b) $(1.6875)_{10}$ -> 01.1011

$(-39)_{10}$ -> 1010 0111

$(-39)_{10}$ ->1101 1001

c) 46FDC000
3.248×10^{4}

d) $f = (\overline{A} + \overline{B})(\overline{B} + \overline{D})(\overline{A} + \overline{D})(\overline{C} + \overline{D})$

		AB			
		00	01	11	10
	00	1	1	0	1
CD	01	1	0	0	0
	11	0	0	0	0
	10	1	1	0	1

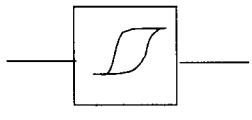
$SOP: f = A.\overline{B}.\overline{D} + \overline{A}.\overline{D} + \overline{A}.\overline{B}.\overline{C}$
4 gates

e) JK flip-flop.

S	S+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Toggle flip-flop by avoiding 1st and 4th row, i.e. J=K=1.

f) Schmitt trigger will sharpen rise/fall time of input signal using different thresholds for 0->1 and 1->0 transitions.



2.

Mode	S1	S0	Action of the device
0	0	0	None
1	0	1	Shift Right, input data bit from SR SER
2	1	0	Shift Left, input data bit from SL SER
3	1	1	Parallel load from D3:0

Table 1

Signal	Meaning
CLK C4	Clock
CLK 1→/2←	indicates that a right shift occurs (Q0 towards Q3) when the mode inputs S1:0=1 and that a left shift occurs when S1:0-2
CLR	Reset outputs to zero
SR SER	Input bit when shifting right
SL SER	Input bit when shifting left
D3:0	Parallel data inputs; data is loaded in when S1:0=3
Q3:0	Output bits of the 4 stages of FFs

Table 2

Circuit Diagram

3. a) $A + \overline{A}B = (A + A.B) + \overline{A}.B = A + B(A + \overline{A}) = A + B$.

b) $\overline{AB + AC} + \overline{A}.\overline{B}.C = \overline{AB}.\overline{AC} + \overline{A}.\overline{B}.C$

$= (\overline{A} + \overline{B})(\overline{A} + \overline{C}) + \overline{A}.\overline{B}.C$

$= \overline{A} + \overline{A}.\overline{C} + \overline{A}.\overline{B} + \overline{B}.\overline{C}$

$= \overline{A} + \overline{A}.\overline{B} + \overline{B}.\overline{C} = \overline{A} + \overline{B}.\overline{C}$

c) $\overline{\overline{A + B + C}} = A.B.\overline{C} + A.\overline{B}.\overline{C} + \overline{A}.B.\overline{C}$

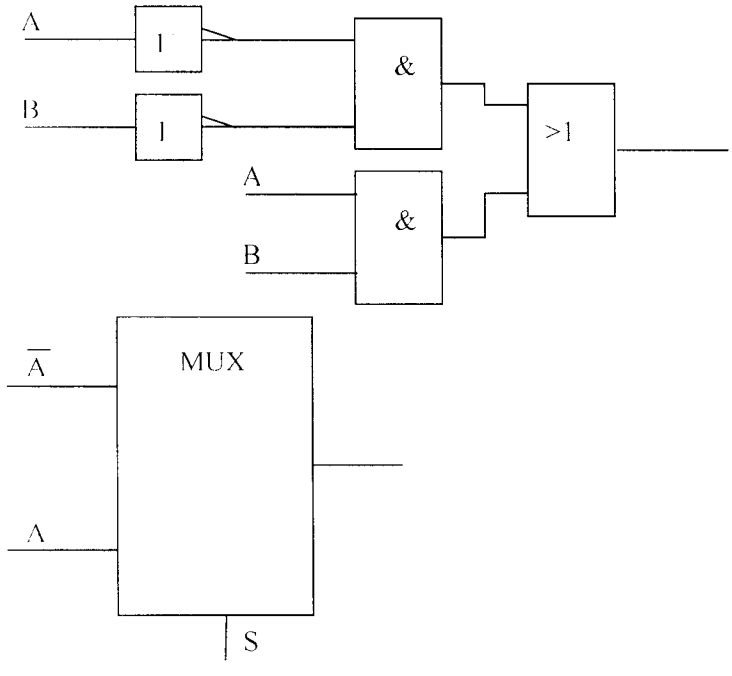
d) Using a Karnaugh map, find minimal SOP and POS expressions for

		A B			
		00	01	11	00
	00	1	1	0	0
C	01	0	0	1	0
D	11	0	1	1	0
	10	1	1	1	1

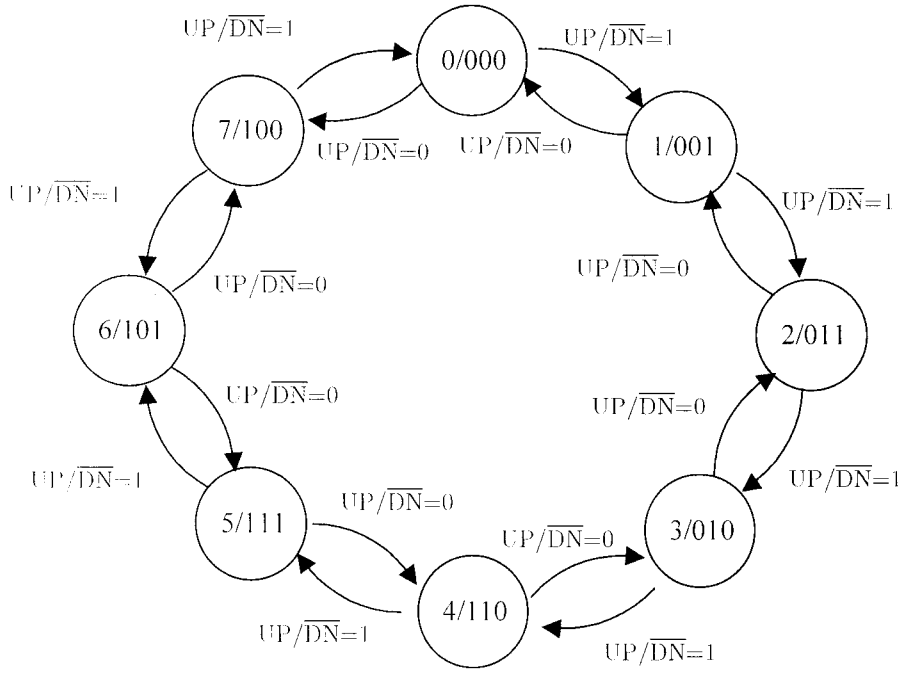
$f = C.\overline{D} + B.C + \overline{A}.\overline{D} + A.B.D$

$f = (B + \overline{D})(\overline{A} + C + D)(A + C + \overline{D})$

e)



4. Draw a Moore-model state diagram of a 3-bit UP/DOWN gray code counter.



Present State			Next State					
			UP/$\overline{DN}$=0			UP/$\overline{DN}$=1		
Q2	Q1	Q0	Q2+	Q1+	Q0+	Q2+	Q1+	Q0+
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	1
0	1	1	0	0	1	0	1	0
0	1	0	0	1	1	1	1	0
1	1	0	0	1	0	1	1	1
1	1	1	1	1	0	1	0	1
1	0	1	1	1	1	1	0	0
1	0	0	1	0	1	0	0	0

Let Y=UP/DN

D2

Q2,Q1 \ Q0,Y	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	1	1	1
10	1	0	1	1

$$D_2 = \overline{Q_1}.\overline{Q_0}.\overline{Y} + Q_1.\overline{Q_0}.Y + Q_2.Q_0$$

D1

Q2,Q1 \ Q0,Y	00	01	11	10
00	0	0	1	0
01	1	1	1	0
11	1	1	0	1
10	0	0	0	1

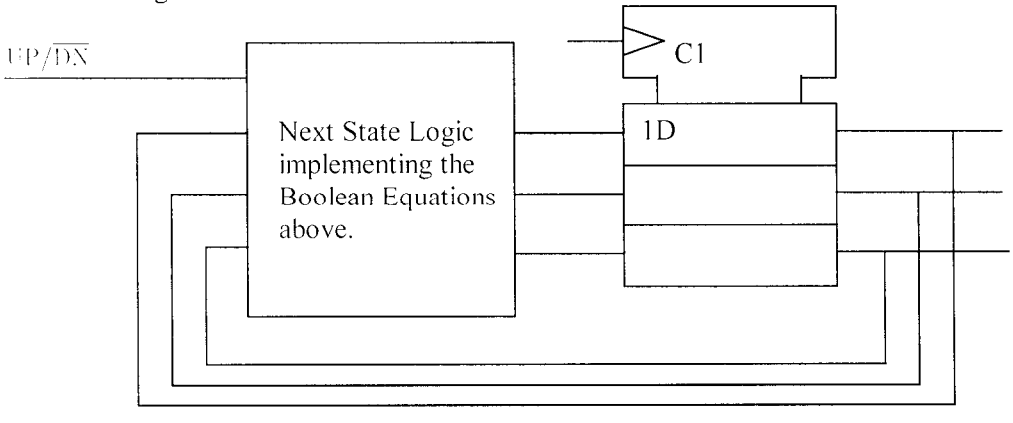
$$D_1 = Q_2.Q_0.\overline{Y} + \overline{Q_2}.Q_0.Y + Q_1.\overline{Q_0}$$

D0

Q2,Q1 \ Q0,Y	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	0	1	1	0
10	1	0	0	1

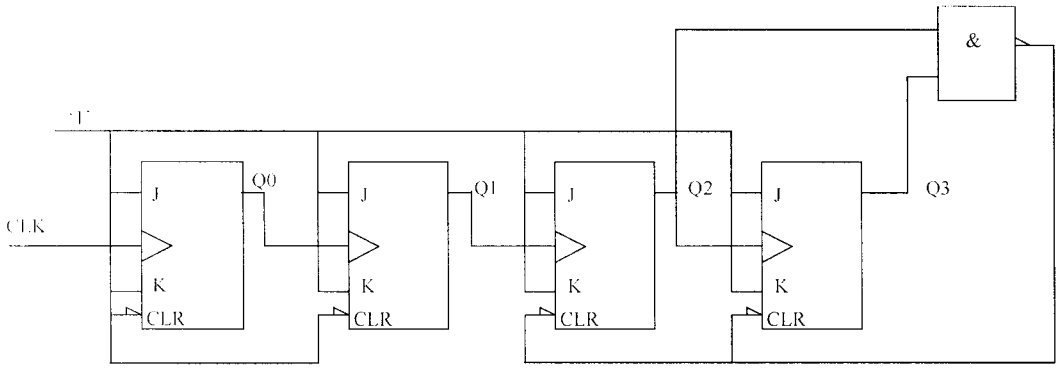
$$D_0 = Q_2.Q_1.Y + \overline{Q_2}.\overline{Q_1}.Y + Q_2.\overline{Q_1}.Y + \overline{Q_2}.Q_1.Y$$

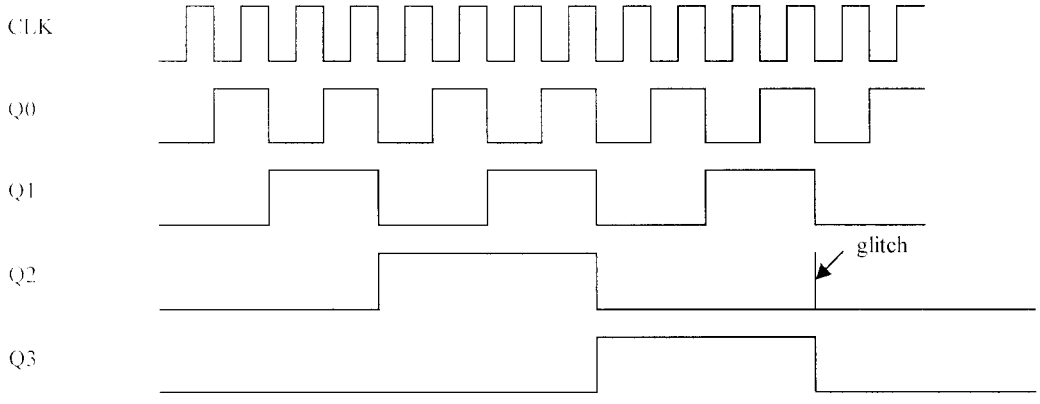
The circuit diagram is of the form



5. Asynchronous: series of toggle ffs with output of one stage driving clock input of next. Ripple effect of clocking limits max speed. Clocking delay increases with number of stages hence max speed decreases.

Synchronous: Registered output controlled by next-state logic. Fixed delay irrespective of length of count sequence.





The maximum speed of operation of the counter depends on the Clock-to-Q delay of the flip-flops. This is typically of the order of a nanosecond. Min clock period at which the counter will operate correctly is approximately 4 times the Clock-to-Q delay.