EE4-53

Part A: Answer any 2 questions out of 3 from this part

1. a) Explain two major drawbacks of using the line commutated converter (LCC) technology for connecting offshore wind farms through HVDC links.

[5]

1. Footprint
With LCC, both the converter stations require large footprint to support the reactive power (50-60% of active power flow) demand of the converters and also filter out low order harmonics. Such large footprint is not available on offshore platforms.

2. Sub-sea cables
For LCC HVDC, power flow reversal is achieved by reversal of voltage polarity as current can only flow in one direction. Reversal of voltage polarity rules out use of polymeric cables (e.g. XLPE) which are lighter, stronger and particularly suited for sub-sea applications.

3. Dependence on strong AC system
LCC fundamentally relies on presence of strong AC voltage for commutation which could be a problem at the offshore wind farm end.

[Any two points are OK, 2.5 marks for each point]

b) State and explain two problems that are only likely to be encountered at the inverter end of a LCC HVDC link but not at the rectifier end.

[5]

1. Commutation failure
Failure to complete commutation of current from one switch to the next one before reversal of commutating (line) voltage. At high currents and low voltages or low extinction advance angles, the outgoing switch might fail to turn off before the commutating voltage reverses in which case the current in the incoming valve would go down to zero. This is not a problem at the rectifier end as much longer margin is available for the commutation of current before reversal of the commutating voltage.

2. Spurious turn-on of switches
Voltages across the switches are mostly negative (reverse bias) for rectifier operation while those are mostly positive (forward bias) for inverter operation. So switches in the inverters are more susceptible to spurious turn-on if a firing signal is released accidentally.

[3 marks for commutation failure, 2 marks for spurious turn on]

c) Considering a non-zero overlap angle (μ) less than 60°, determine the firing angle (α) at which the reactive power drawn by the 6-pulse rectifier of a LCC HVDC link would be maximum.

[5]

For μ <60°, only three switches can conduct simultaneously.

In such case, power factor at the rectifier end is approximately

$$\text{pf} = \cos\varphi = \left[\frac{\cos\alpha + \cos(\alpha+\mu)}{2}\right]$$

Maximum reactive power demand corresponds to zero power factor

$$\cos\alpha + \cos(\alpha+\mu) = 0$$

$$\alpha = \pi - (\alpha+\mu)$$

$$\alpha = \frac{\pi-\mu}{2}$$

[2 marks for correct expression of power factor; 1 mark for equating to zero, 2 marks for correct expression for firing angle]

d) Discuss the role of commutation resistance in the context of LCC HVDC and explain physically (not from expressions) what decides the value of the commutation resistance. There is no need to derive any expressions.

[5]

Commutation resistance is not a physical resistance. Instead, it is used to represent the reduction in average DC voltage as a result of commutation overlap. This reduction in average voltage is proportional to the direct current. Hence, it can be represented as a voltage drop across a resistance which is referred to as 'commutation resistance'.

The duration of commutation overlap (i.e. overlap angle) depends primarily on the equivalent AC side inductance. Higher overlap causes a larger reduction in average DC voltage. So the value of the commutation resistance, which captures the average voltage reduction, should depend on the equivalent AC side inductance.

[2 marks for discussion of the role of commutation resistance; 3 marks for explaining the dependence on AC side inductance]

2. a) What are the three important considerations towards designing the smoothing reactor for a LCC HVDC link?

[5]

1. Value of the smoothing reactor needs to be high to
   a) Reduce the direct current ripple
   b) Prevent discontinuous conduction
   c) Minimise consequent commutation failure

2. Value of the smoothing reactor needs to be low to avoid resonance at low (non-characteristics) frequencies

3. Partial air core is required to prevent saturation with manageable dimensions

[1 mark each for 1(a), 1(b), 1(c), 2 and 3]

b) Explain how a short circuit on a LCC HVDC overhead line is detected, limited and cleared.

[5]

Detection
- Rectifier current increase, inverter current decrease
- Faults detected by collapse of DC voltage and decrease in inverter current

Fault current limiting
- Constant current (CC) control restores the rectifier current back to normal
- Inverter switches from CEA to CC to hold the decreasing current
- Rectifier tries to maintain I_{ord} and inverter $I_{ord} - I_m$ in opposite direction both being in CC mode
- Fault current is thus limited to only margin current I_m (10-15% of rated current)

Fault clearing
- Rectifier is driven to inversion ($a = 140^0$) keeping the inverter as it is ($b < 80^0$)
- Current attempts to reverse, cannot because of valves and is rapidly (10 ms) reduced to zero

[1 mark each for detection; 2 marks each for limiting and clearing]

c) Consider a set of balanced 3-phase voltages with a-b-c phase sequence. The expression for phase 'a' voltage (e_a) is given below in equation (2.1). Using this, derive an expression for the no-load ideal direct voltage (V_{d0}) for a 6-pulse LCC in terms of the AC line voltage (E_{LL}). Neglect firing delay (α) and commutation overlap (μ).

$$e_a = E_m \sin \omega t \tag{2.1}$$

[5]

Phase voltages (considering a-b-c phase sequence)

$$e_a = E_m \sin \omega t; e_b = E_m \sin\left(\omega t - \frac{2\pi}{3}\right); e_c = E_m \sin\left(\omega t + \frac{2\pi}{3}\right)$$

Line voltages

$$e_{ab} = e_a - e_b = \sqrt{3}E_m \sin\left(\omega t + \frac{\pi}{6}\right)$$
$$e_{bc} = e_b - e_c = \sqrt{3}E_m \sin\left(\omega t - \frac{\pi}{2}\right)$$
$$e_{ca} = e_c - e_a = \sqrt{3}E_m \sin\left(\omega t + \frac{5\pi}{6}\right)$$

For a 6-pulse converter, width of each pulse is $\pi/3$

Average no-load ideal DC voltage

$$V_{d0} = \frac{3}{\pi}\int_{\pi/3}^{\pi/2} \sqrt{3}E_m \sin\left(\omega t + \frac{\pi}{6}\right) d(\omega t) = \frac{3\sqrt{3}E_m}{\pi} = \frac{3\sqrt{6}E_{LN}}{\pi} = \frac{3\sqrt{2}E_{LL}}{\pi}$$

[2 marks for phase and line voltages; 3 marks for correct derivation. Use of other line voltages with appropriate limits of integral is OK]

d) Describe the roles of bridge control, pole control, master control and system level control as part of LCC HVDC control hierarchy.

[5]

- Bridge control determines the firing instants of the valves within limits for a bridge and takes care of protection (e.g. commutation failure protection)
- Pole control coordinates control of bridges in a pole and provides firing angle orders to individual converters
- Master control determines the current order and suitable current margins to the poles
- System level control decides the dc link power flow based on scheduled transactions or ac system stabilization

[3 marks for bridge and pole control; 2 marks for master and system level control]

3. The planned 2.2 GW, ±600 kV (bipole) Western HVDC link in the UK would be connected to the 400 kV AC grid at Hunterston and Connah's Quay terminals. The resistance of the DC cable in each pole is 2.0 Ω. Under normal condition, the HVDC link operates with the rectifier end controlling the direct current (I_d) and the inverter end maintaining a constant extinction advance angle (γ) with the following:

Commutation resistance at each end $R_{cr} = R_{ci} = 3.0\ \Omega$
Firing angle at the rectifier end $\alpha = 12°$
Extinction advance angle at the inverter end $\gamma = 18°$
Minimum firing angle limit $\alpha_{lim} = 5°$
AC line voltage at the rectifier bus $E_r = 405$ kV
Direct current through the link $I_d = 1.8$ kA
Current margin $I_m = 15\%$

A short-circuit within the AC system nearer to the inverter end (Connah's Quay terminal) causes a 20% reduction in AC voltage on the inverter bus and a 2% reduction in AC voltage at the rectifier bus. Considering the ±600 kV bipole Western HVDC link as an equivalent 1200 kV monopolar link with 12-pulse converters (as shown in Figure 3.1) calculate the following: Neglect activation of VDCOL and change of transformer tap ratio due to the short-circuit.

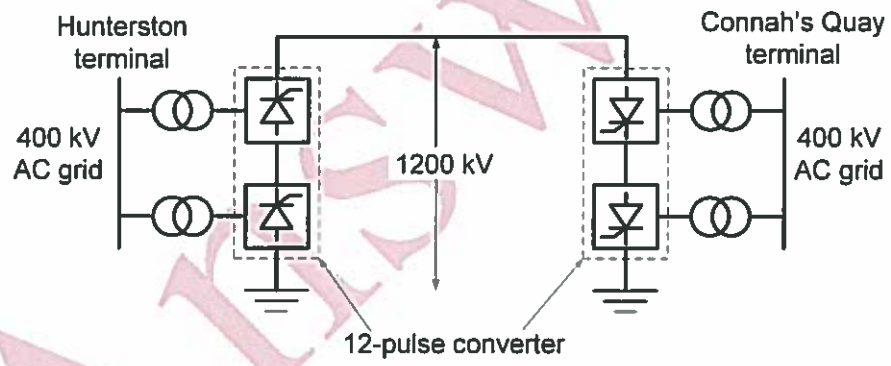


Figure 3.1 - Equivalent monopolar representation of planned Western HVDC link

i) A
Active and reactive power at both ends under normal condition

[4×3]

Under normal condition:

At the rectifier end:

$$V_{dor} = \frac{3\sqrt{2}}{\pi} E_r B = 1107.4\ \text{kV}$$

$$V_{dr} = V_{dor} \cos\alpha - R_{cr} B I_d = 1072.4\ \text{kV}$$

$$\text{pf} = \cos\varphi_r = \frac{V_{dr}}{V_{dor}} = 0.96839$$

$$P_r = V_{dr} I_d = 1.93 \text{ GW}$$

$$Q_r = P_r \tan\varphi_r = 497.17 \text{ MVAr}$$

[2 marks for V_{dor}, V_{dr} and pf; 1 mark for P_r Q_r]

At the inverter end:

$$V_{di} = V_{dr} - 2 \times R_L I_d = 1065.2 \text{ kV}$$

$$V_{doi} = \frac{V_{di} + R_{ci} B I_d}{\cos\gamma} = 1131.4 \text{ kV}$$

$$\text{pf} = \cos\varphi_i = \frac{V_{di}}{V_{doi}} = 0.94151$$

$$P_i = V_{di} I_d = 1.92 \text{ GW}$$

$$Q_i = P_i \tan\varphi_i = 686.25 \text{ MVAr}$$

[2 marks for V_{doi}, V_{di} and pf; 1 mark for P_i Q_i]

ii) Firing angle (in degrees) of the rectifier under short-circuit condition

[4]

Under short-circuit condition:

Rectifier stays in current control mode while the inverter continues to maintain a constant extinction angle. Neglecting VDCOL, the direct current remains the same
Rectifier controls the current to the same value by increasing the firing angle

$$V'_{doi} = 0.8 V_{doi} = 905.09 \text{ kV}$$

$$V'_{dor} = 0.98 V_{dor} = 1085.2 \text{ kV}$$

$$V'_{di} = V'_{doi} \cos\gamma - R_{ci} B I_d = 849.99 \text{ kV}$$

$$V'_{dr} = V'_{di} + 2 \times R_L I_d = 857.19 \text{ kV}$$

$$\alpha' = \cos^{-1}\left[\frac{V'_{dr} + R_{ci} B I_d}{V'_{dor}}\right] = 36.88°$$

[1 mark each for V'_{di} and V'_{dr}; 2 marks for α']

iii) Active and reactive power at both ends under short-circuit condition

[4×1]

At the rectifier end:

$$P'_r = V'_{dr} I_d = 1.54 \text{ GW}$$

$$\text{pf} = \cos\varphi'_r = \frac{V'_{dr}}{V'_{dor}} = 0.78986$$

$$Q'_r = P'_r \tan\varphi'_r = 1.198 \text{ GVAr}$$

At the inverter end:

$$P'_i = V'_{di} I_d = 1.53 \text{ GW}$$

$$\text{pf} = \cos\varphi'_i = \frac{V'_{di}}{V'_{doi}} = 0.93912$$

$$Q'_i = P'_i \tan\varphi'_i = 559.74 \text{ MVAr}$$

[1 mark each for P'_r, Q'_r, P'_i, Q'_i]

Part B: Answer any 2 questions out of 3 from this part

4. Classic Voltage Source Converter

a) Present the differences (both pros and cons) between Voltage Source Converters (VSC) and Current Source Converters (CSC) and especially why cable-based transmission HVDC schemes (e.g. offshore windfarms) are based on VSCs?

[4]

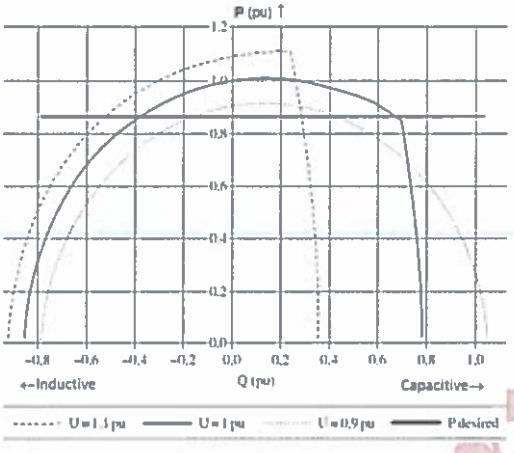
As their names imply Current Source Converters rely on a DC current source to operate while Voltage Source Converters rely on a DC voltage source. As a consequence, CSCs construct their AC current by the action of their valves and VSCs control the current running through their AC phase reactor by acting on the AC voltage. Furthermore, the Line Commutated Converter (LCC) which is the most well-known CSC topology generates a large amount of lagging reactive power because of the way its valves operate. Furthermore, these same valves require a strong AC network to be switched, making the LCC unsuitable to power isolated AC networks such as wind farms. In addition to the last two points, CSC's reliance on a DC current source implies that the direction of the DC current cannot be altered, resulting in DC voltage reversal when the power flow needs to be reversed. These last three points are no longer issues when dealing with VSCs, thanks to their reliance on a DC voltage sources.

[KEYWORDS]: CSC = DC current source, VSC = DC voltage source, reactive power, power ratings, power losses, strength of the AC grid, DC voltage reversal when power reverses

b) Explain using a simple drawing of a P-Q diagram the maximum active and reactive power conversion capability of a classic VSC, especially what are the main limiting factors under varying AC voltage magnitudes (e.g. 0.9-1.1 pu).

[4]

VSC are capable of providing independently active and reactive power. The main limitation is set by the maximum current capability of the converter, thus describe a circle in the P-Q diagram. This circle is however truncated in the capacitive power plane because this type of reactive power requires the VSC to generate higher AC voltage magnitude which peaks cannot be higher than the DC terminal voltage. For this reason, if the AC grid voltage magnitude decreases (e.g. 0.9 pu), the VSC reactive power capability increases and the opposite happens with higher AC grid voltage magnitude.



[KEYWORDS]: independent P and Q, maximum current rating, limited capacitive power due to converter voltage clipping to DC terminal voltage, lower grid AC voltage increases capacitive power capability and vice versa.

c) A 900 MW Voltage Source Converter (VSC) is shown in Figure 4.1. It is connected to a 400 kV (line-to-line) AC grid at 50 Hz and a DC network at ±350 kV.

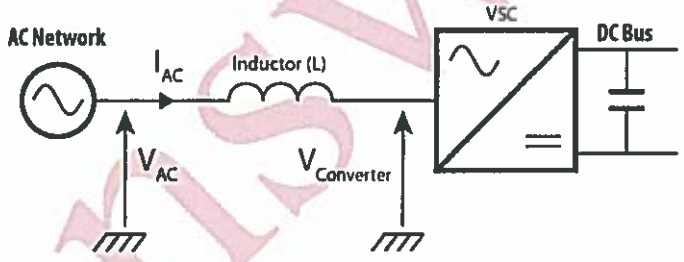


Figure 4.1: Voltage Source Converter

i) When the converter is inverting 600 MW (power going from DC to AC) and generating 300 MVAr of capacitive reactive power, compute the magnitude and phase angle of the AC current.

[3]

$$I = \frac{S^*}{\sqrt{3}\, V_{line}} = 968\, A_{RMS}\ and\ 153°$$

ii) Assuming that the phase reactors are 190 mH, compute the magnitude and angle of the converter voltage.

[3]

$$V_{converter} = V_{AC} - j\omega L\, I = 246.1\, kV_{RMS}\ and\ 6.3°$$

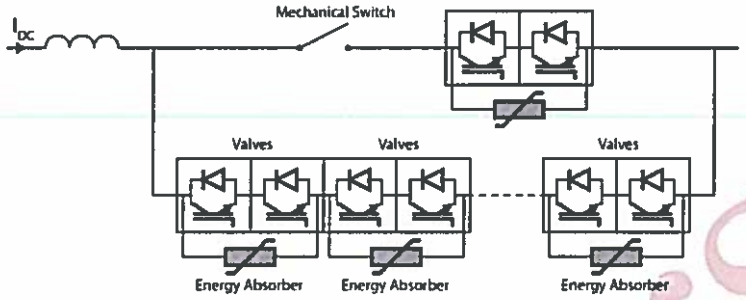
iii) Determine the modulation index at which the VSC is running?

[2]

$$k = \frac{\hat{V}_{converter}}{V_{DC_{terminal}}} = 99.42\ \%$$

d) Draw the electrical diagram of a hybrid DC circuit breaker and explain how it operates, detailing the timing and rating criteria of the different elements of the breaker.

[4]



The hybrid DC circuit breaker operates in several steps. First, the small solid state switch consisting of few IGBT modules opens in order to raise the resistivity of the main conduction path. The current is thus directed through the fully DC voltage rated solid state switch which is still closed and located in parallel of the main path. Second, fast moving the mechanical switch opens. Third, once the mechanical switch is in its open position, the large solid state switch finally opens, resulting in the extinction of the fault current. Importantly, when a DC fault occurs, the DC current starts to rise quickly with its rate of rise mainly limited by the large DC inductor (e.g. 100mH). Its value must be chosen such that the magnitude of the magnitude of the fault current when the large solid state switch opens is still lower than the maximum current rating of the IGBT module (e.g. 5 kA). The whole breaking process takes around 5 ms

[KEYWORDS]: small / auxiliary solid state switch, fact moving mechanical switch, fully DC bus voltage rated parallel solid state switch, DC inductor limiting fault current rate of rise, 5 ms breaking time.

5. Modular Multilevel Converter

a) Explain the working principles of the Modular Multilevel Converter topology.

[5]

The MMC essentially retain the advantages of the classic VSC (e.g. constant DC voltage, full 4-quadrant P-Q operation, black start capability…) but gains from its high number of cells (or submodules). This fact enables the MMC to generate a converter voltage waveform with numerous voltage steps, reducing significantly the need for high frequency PWM switching of its IGBT modules, thus increasing the converter's power efficiency. Other positive consequences of this operating mechanism consists in the saving on both the AC and DC filter banks and the modular design.

On the negative side, the MMC requires a larger valve hall because of its numerous bulky cells. The control of the converter has been significantly made more complex because of the large number of modules needing to be switch independently. Finally, the half-bridge MMC is still weak against DC-side fault as the fault current can still run through the anti-parallel diodes.

[KEYWORDS]: Pros: higher power efficiency, lower waveform distortion, no AC and DC filters, and modular design. Cons: larger valve hall, more complex control system and still weak against DC-side fault.

b) A 1.2 GW MMC is connected to the latest DC cable technology rated a ±525 kV. Assuming that each half-bridge submodule is rated at 2 kV.

i) Compute a device count for: the number of IGBT module, submodule capacitors.

[3]

Number of submodules per arm: $\frac{V_{DC}}{V_{cell}} = 525$

Total number of IGBT modules: $6 \times 2 \times N_{cell} = 6300\ IGBTs$

Total number of capacitors: $6 \times N_{cell} = 3150\ Capacitors$

ii) Estimate the minimal capacitance of the cell capacitors assuming that their voltage has to be kept within ±10% of their nominal value and the maximum peak-to-peak energy deviation of a stack is 2.546 MJ for the specified operating envelope of this converter.

[3]

Cell Capacitor: $\frac{\Delta E}{2\, N_{cell}\, V_0^2\, \Delta V} = 6.06\ mF$

iii) Calculate the total capacitive energy stored per unit power (provide the answer in kJ/MVA).

[3]

Energy per unit: $\frac{6\, N_{cell} \frac{C_{cell}}{2} V_{cell}^2}{S_{rated}} = 32\ kJ/MVA$

c) Explain how the Double Clamped Submodule, shown in Figure 5.1, operates.

[6]

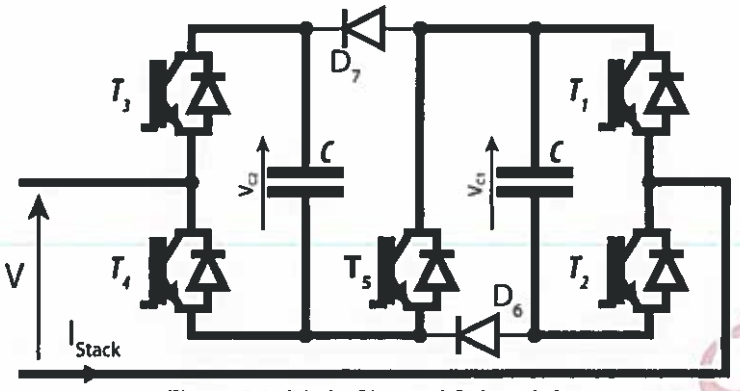


Figure 5.1: Diode Clamped Submodule

The Double Clamp Submodule (DCS) has been designed to offer a compromise between the full and half-bridge types of submodules. The DCS looks like a H-bridge submodule but with two capacitors, one additional switch T5 and two diodes D6 and D7. Under normal operation, T5 is closed, thus the diodes D6 and D7 are reversed biased by the cells capacitors. The DCS will thus act as two half-bridge cells connected together through the bidirectional switch T5. Since the DCS has always three switches in the current path for two equivalent half-bridge cells, it exhibits 50% higher power losses than the half-bridge submodule but still 25% lower than its full H-bridge counterpart. The advantage of the DCS comes when the switch T5 is switched off. In this operating mode, the diodes D6 and D7 start conducting but at the condition that the current going through the stack is positive since a diode is unidirectional.

[KEYWORDS]: mix between full H-bridge and half-bridge submodule, 50% more losses than 2 half-bridges but 25% less than using only full H-bridge submodules.

6. Alternate Arm Converter

a) Explain how the Alternate Arm Converter (shown in Figure 6.1) operates.

[5]

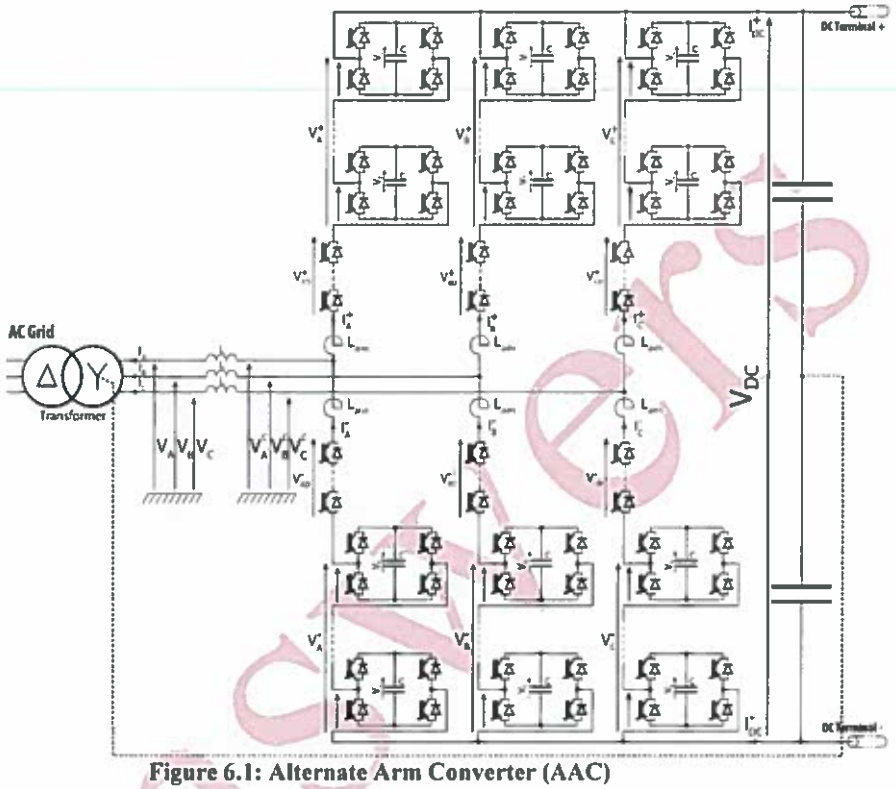


Figure 6.1: Alternate Arm Converter (AAC)

The Alternate Arm Converter (AAC) is a hybrid topology which combines the IGBT switches (here called the director switches) of a 2-level converter with stacks of capacitor modules similar to those of the Modular Multilevel Converter (MMC). The AAC presents a high power efficiency (>99%) and is able to block DC-side faults. The director switches are composed of series connected IGBT modules operating together at the fundamental frequency and directing the AC current toward either the top arm or the bottom arm. This mechanism effectively rectifies the AC currents into a DC current with a 6-pulse ripple. The stacks of cells work in conjunction with their respective director switch and shape the converter voltage into a multilevel staircase voltage waveform, thus ensuring low distortion and minimising the required switching frequency of the semiconductor devices. Given that a 6-pulse ripple is present in the DC current waveform of the AAC, a passive DC filter may be required in the form of a large DC inductor and bus capacitor, the size of which can be significant. The AAC has an optimal operating point, referred to as the sweet-spot, where the converter is at its most efficient as the AC and DC energies are equal. This is defined as the linear relationship (Vac = 2/pi Vdc) between the AC and DC voltage magnitudes.

[KEYWORDS]: Pros: high power efficiency, low waveform distortion, no AC filters, modular design, DC-side fault blocking. Pros: larger valve hall, more complex control system, 6-pulse ripples in the DC current waveform. Important: sweet spot.

b) A 1.2 GW AAC, operating with 25-degree overlap is connected to the latest DC cable technology rated a ±525 kV. Assuming that each H-bridge submodule is rated at 2 kV.

i) Compute a device count for: the number of IGBT module, submodule capacitors. [3]

Number of submodules per arm: $\frac{1}{V_{SM}}\left(\frac{V_{DC}}{2} + \hat{V}_{AC}\, sin\left(\frac{\Phi_{over}}{2}\right)\right) = 335$

Number of series-IGBT modules per director switch (1 arm): $\frac{V_{DC}}{V_{SM}} = 262$

Total number of IGBT modules: $6 \times 2 \times N_{SM} = 9612\ IGBTs$

Total number of capacitors: $6 \times N_{SM} = 2010\ Capacitors$

ii) Estimate the minimal capacitance of the cell capacitors assuming that their voltage has to be kept within ±10% of their nominal value and the maximum peak-to-peak energy deviation of a stack is 765 kJ for the specified operating envelope of this converter. [3]

Cell Capacitor: $\frac{\Delta E}{2\, N_{SM}\, V_{SM}^2\, \Delta V} = 2.85\ mF$

iii) Calculate the total capacitive energy stored per unit power (provide the answer in kJ/MVA) [3]

Energy per unit: $\frac{6\, N_{SM} \frac{C_{SM}}{2} V_{SM}^2}{S_{rated}} = 9.55\ kJ/MVA$

d) During a DC fault event, the AAC can act as a STATCOM and provide reactive power to the grid without the need for a DC bus. Assuming only the bottom stacks are operating and ignoring the inductors' voltage drops, as illustrated in Figure 6.2, calculate the maximum reactive power that a 50 Hz AAC can provide before the 2.5 mF capacitors in its 400 submodules per stack exceed their designed maximum voltage deviation of ±10%. [6]

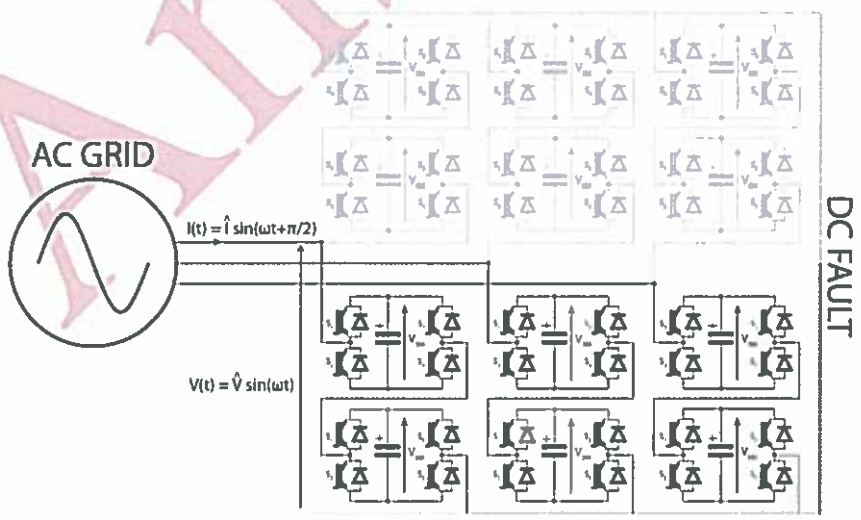


Figure 6.2: AAC as STATCOM

Clue I: For this, it is recommended (i) to find the equation describing the instantaneous power of a stack, (ii) from this obtain the energy equation of a stack, (iii) find the min and max points as a function of the amount of reactive power and (iv) conclude on the maximum power.

Clue II: The relationship between peak-to-peak energy deviation of a single stack and the size of its submodule capacitors for a given maximum relative voltage deviation is: $\Delta E = 2\, N_{SM}\, V_{SM}^2\, \Delta V\, C$ and also use $Q = 3\frac{\hat{V}\hat{I}}{2} = 3\, V_{RMS}\, I_{RMS}$

(i) $P_{stack}(t) = V(t)\, I(t) = \hat{V}\hat{I}\sin(\omega t)\sin\left(\omega t + \frac{\pi}{2}\right) = \frac{Q}{3}\sin(2\omega t)$

(ii) $E(t) = \int P(t)\, dt = \frac{Q}{6\omega}\cos(2\omega t)$

(iii) $\hat{E} = \frac{Q}{6\omega}$ and $\check{E} = -\frac{Q}{6\omega}$ thus $\Delta E = \hat{E} - \check{E} = \frac{Q}{3\omega}$

(iv) $C = \frac{\Delta E}{2\, N_{SM}\, V_{SM}^2\, \Delta V} \rightarrow Q = 6\omega\, C\, N_{SM}\, V_{SM}^2\, \Delta V = 754\ MVAr$