IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2011

EEE/ISE PART II: MEng, BEng and ACGI

DIGITAL ELECTRONICS 2

Wednesday, 1 June 2:00 pm

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : D.M. Brookes
Second Marker(s) : T.J.W. Clarke

Information for Candidates:

The following notation is used in this paper:

1. Unless explicitly indicated otherwise, digital circuits are drawn with their inputs on the left and their outputs on the right.
2. Within a circuit, signals with the same name are connected together even if no connection is shown explicitly.
3. The notation X2:0 denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0.
4. Signed binary numbers use 2's complement notation.

1. (a) *Figure 1.1* shows the circuit of a synchronous state machine. The logic block is defined by the following Boolean equations:

$$NS1 = (A + \overline{S1}) \cdot S0 + \bar{A} \cdot S1 \cdot \overline{S0}$$
$$NS0 = A \cdot \overline{S1} + \bar{A} \cdot \overline{S0}$$

Construct the state table for the circuit and draw its state diagram. [8]

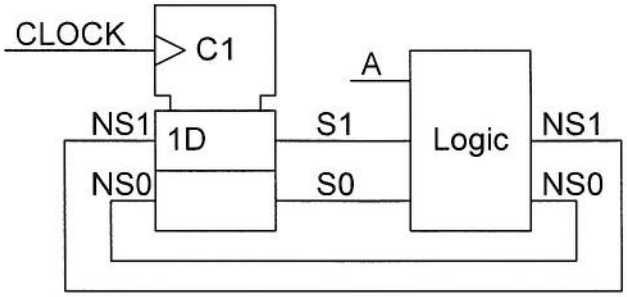


Figure 1.1

(b) In the circuit of *Figure 1.2*, the flipflops have a propagation delay t_P and setup/hold times of t_S and t_H respectively. The non-inverting blocks A and B have propagation delays t_A and t_B respectively. The clock, CK, is a symmetric square wave with period T.

(i) Write down the setup and hold inequalities that apply to the rightmost flipflop. [4]

(ii) Calculate the minimum and maximum values of t_B for reliable operation if $t_S = 3$, $t_H = 2$, $t_P = 7$, $t_A = 13$ and $T = 20$ where all times are in nanoseconds. [4]

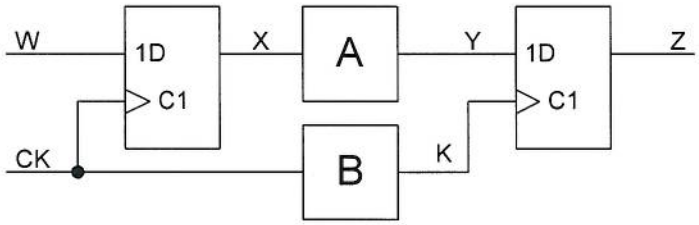


Figure 1.2

(c) *Figure 1.3* shows the circuit of a 2-bit flash converter whose input voltage, V, lies in the range -5 to $+3$ Volts and whose 2-bit signed output is given by

$$x = \text{round}\left(\frac{V}{2}\right).$$

The comparator outputs, A, B and C go high if V exceeds the corresponding reference voltage. Thus A=1 whenever $V > 1$ V. Construct a table listing all the combinations of A, B, C that can occur, the input voltage ranges for which they arise and the corresponding values of X1 and X0. [5]

Hence give simplified Boolean expressions for X1 and X0 in terms of A, B and C. [3]

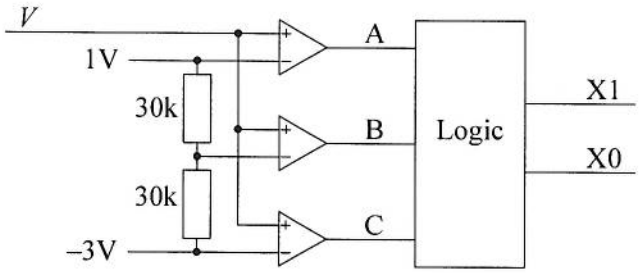


Figure 1.3

(d) *Figure 1.4* shows the two least significant bits of a carry-lookahead adder. The CG and CGP outputs from each adder stage are defined by

$$\text{CG} = \text{P} \cdot \text{Q}$$

$$\text{CGP} = \text{P} + \text{Q}.$$

(i) Explain the terms "carry generate" and "carry propagate" in the context of a carry-lookahead adder. [4]

(ii) Give a Boolean expression for C0 in terms of CG0, CGP0 and CIN. [4]

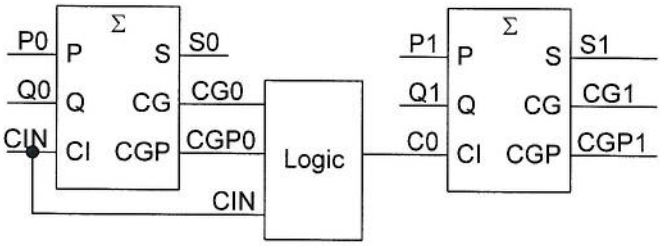


Figure 1.4

(e) Suppose that x denotes the value of an 8-bit signed number, X7:0, such that $-128 \leq x \leq 127$. Give simplified Boolean expressions that are true under the following conditions:

(i) $x \geq 64$ [2]

(ii) $-32 \leq x < 32$ [3]

(iii) x is a positive multiple of 8 [3]

2. The circuit of *Figure 2.1* comprises a 3-bit adder, a 4-bit register and a 4-bit counter. The counter increments on the rising edge of CLOCK provided that Q3 is high.

(a) Suppose the binary number N2:0 has the decimal value 3.

(i) Draw a timing diagram extending for ten CLOCK cycles showing the value of Q3:0 in each clock cycle and also the waveform of Q3. The initial value of Q3:0 is 4. [7]

(ii) Determine the average frequency (i.e. the number of pulses in one second) at Q3 and at X3. [5]

(iii) Giving your reasons fully, determine the minimum and maximum number of CLOCK cycles between successive rising edges of X3. [5]

(b) Give a formula for the average frequency of X3 in terms of n, the value of the unsigned 3-bit number N2:0. [5]

(c) Suppose now that the circuit uses an m-bit adder, an $(m+1)$-bit register and a k-bit binary counter. The CLOCK frequency remains at 8.192 MHz.

(i) Determine the smallest value of m that will allow the average frequency of Qm to be set to any exact multiple of 20 kHz in the range 0 to 1 MHz. [3]

(ii) Determine the value of the m-bit input number, n, for your circuit to give an output frequency of 100 kHz. [2]

(iii) Explain why the size of the adder, m, can be reduced if the output is taken from $X(k-1)$ instead of from Qm. Determine the counter size, k, that results in the smallest possible adder size while permitting the average output frequency at $X(k-1)$ to be set to any exact multiple of 20 kHz in the range 0 to 1 MHz. [3]

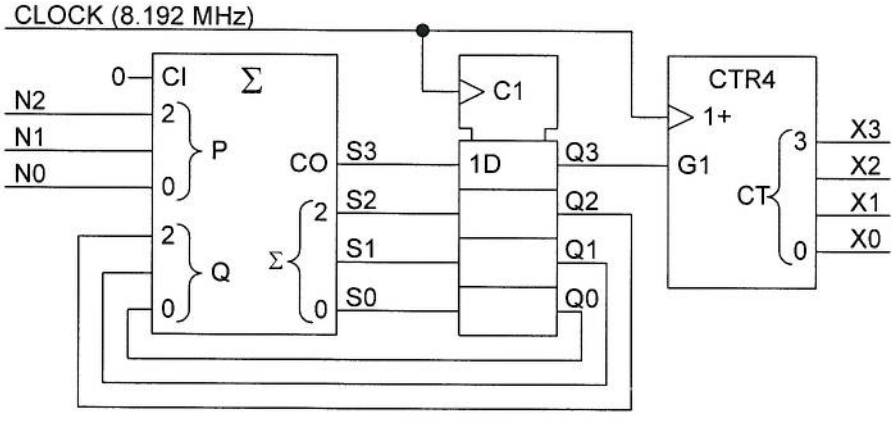


Figure 2.1

3. *Figure 3.1* shows a circuit that receives serial data at its input, X, and stores the received 4-bit values (nibbles) in a random-access memory (RAM). Each nibble is transmitted on X as a "1" followed by the four data bits e.g. 1011 is transmitted as 11011. Successive nibbles are separated by an arbitrary number of "0"s (including none). All transitions in X occur shortly after the rising edge of CLOCK. If the logic-block output, R, is high, the address counter (labelled CTR8) is reset on the next CLOCK rising edge.

(a) The register and logic block in the centre of the diagram form a synchronous state machine with a single input, V0, and with outputs R, P, W and L. The state diagram is shown in *Figure 3.2*: all outputs are zero except in the states indicated.

Complete the timing diagram in *Figure 3.3* by showing (i) the decimal value of the shift register output, V3:0, (ii) the state machine state, $a - k$, and (iii) the waveforms of P, W and L. The vertical dashed lines in the figure correspond to CLOCK rising edges and the cycles are numbered for convenience. [14]

(b) The state machine output L acts as the clock enable input for a register whose data inputs are V3:0.

(i) Explain why this register is necessary for the circuit to work correctly. [2]

(ii) Assuming that D3:0 and A7:0 are initially zero, determine the decimal values taken by these quantities in each of the CLOCK cycles shown in *Figure 3.3*. [4]

(iii) Give the address and new value of any RAM locations that are altered. [2]

(c) Explain carefully how, regardless of its initial state, the circuit will normally synchronize itself so that the correct values are stored in the RAM. Describe precisely the conditions that must be satisfied by the serial data in order to ensure that correct synchronization is guaranteed to occur. [8]

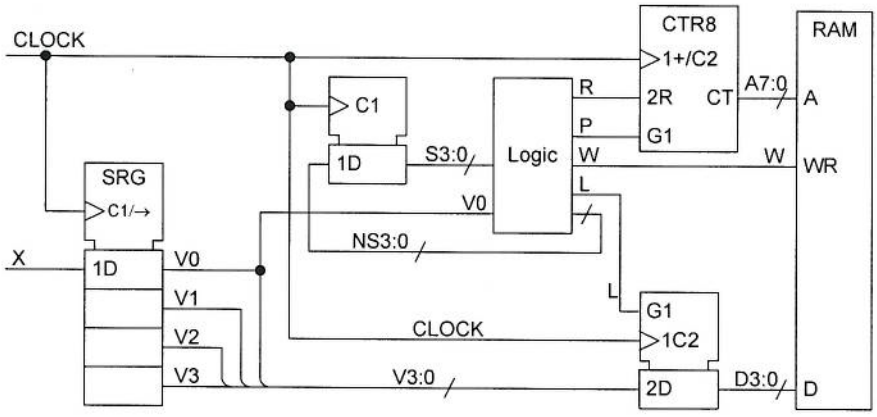


Figure 3.1

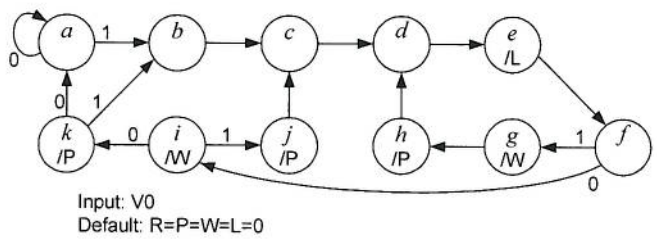


Figure 3.2

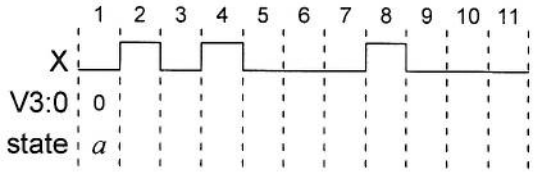


Figure 3.3

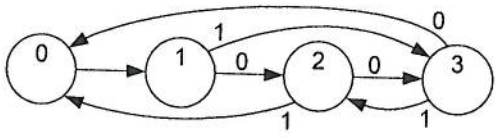
2011 Paper E2.1/ISE2.2: Digital Electronics II- Solutions

Key to letters on mark scheme: B=Bookwork, C=New computed example, A=Analysis of new circuit, D=design of new circuit

1. (a) (i) The state table is: [5A]

	NS1:0/X	A=0	A=1
S1:0	00	01	01
	01	10	11
	11	00	10
	10	11	00

(ii) The state diagram is: [3A]



(b) (i) Setup: $t_P + t_A + t_S < T + t_B$

Hold: $t_B + t_H < t_P + t_A$ [4A]

(ii) Constraints are: $t_P + t_A + t_S - T < t_B < t_P + t_A - t_H$

leading to: $3 < t_B < 18$ [4A]

(c) The table is: [5A]

A,B,C	Voltage range	X1,X0
111	$V > 1$	01
011	$-1 < V < 1$	00
001	$-3 < V < -1$	11
000	$V < -3$	10

From this we get [3A]

$$X1 = \bar{B}$$
$$X0 = A \cdot B + C$$

(d) (i) If $P_i \cdot Q_i = 1$ then column i "generates" a carry since C_i will be high regardless of C_{i-1}.

If $P_i \oplus Q_i = 1$ then column i "propagates" a carry since C_i will be high if and only if C_{i-1} is high. [4B]

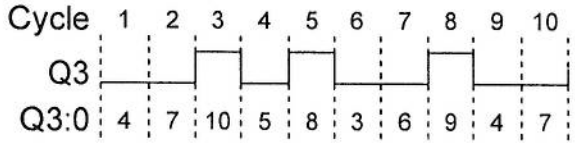
(ii) $C_0 = CG_0 + C_{IN} \cdot CGP_0$. [4B]

(e) (i) $\overline{X7} \cdot X6$ [2D]

(ii) $X7 \cdot X6 \cdot X5 + \overline{X7} \cdot \overline{X6} \cdot \overline{X5}$ [3D]

(iii) $\overline{X7} \cdot \overline{X2} \cdot \overline{X1} \cdot \overline{X0}$ [3D]

2. (a) (i) After each CLOCK pulse, the new value of Q3:0 is 3+Q2:0 i.e. 3+(Q3:0 modulo 8). The timing diagram is therefore: [7A]



(ii) Q3 has three pulses every eight CLOCK cycles so its average frequency is $\frac{3}{8} \times 8.192 = 3.072$ MHz.

The average frequency of X3 is one sixteenth the average frequency of Q3 and is therefore $\frac{3072}{16} = 192$ kHz. [6A]

(iii) Successive rising edges of X3 occur every 16 Q3 pulses. Since we get 3 pulses every 8 CLOCK cycles, 15 pulses take exactly $5 \times 8 = 40$ CLOCK cycles. It follows that 16 pulses take $40 + 2 = 42$ or $40 + 3 = 43$ CLOCK cycles since the gap between successive pulses on Q3 is either 2 or 3 clock cycles. The answer is therefore 42 and 43. [5A]

(b) Q3 is now high for n CLOCK cycles out of every eight. The average frequency of X3 is therefore $8192 \times \frac{n}{8} \times \frac{1}{16} = 64n$ kHz. [5A]

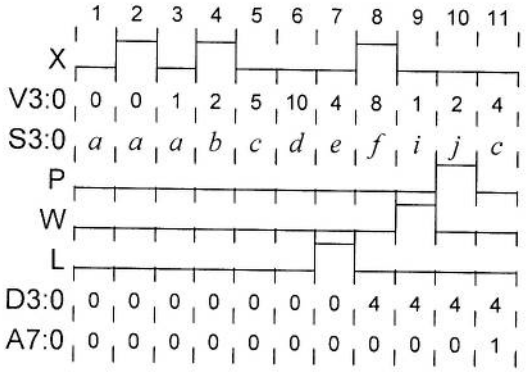
(c) (i) The easiest way to meet the specification is to have a 13 bit adder. We would now get n output pulses on Q13 every $2^{13} = 8192$ CLOCK cycles for an output frequency of n kHz.

However, since the value of n is always a multiple of 20, its two least significant bits are always zero and the corresponding adder bits are not needed. Thus we only need $m = 11$. [3D]

(ii) The output frequency at Q11 is $4n$ kHz, so setting $n = 25$ will give the desired output frequency. [2A]

(ii) If we multiply n by 8, we will multiply the average frequency at Q11 by 8 (to give a maximum of 8 MHz which is still less than the CLOCK frequency). We can then divide the frequency at Q11 by 8 by setting $k = 3$ and taking the output from X2. The three least significant bits of n are now zero, so m can be reduced to 8. [3D]

3. (a,b) The completed timing diagram is:



V3:0 is the output of a shift register and so is just the decimal value of the previous 4 bits of X. [14A]

D3:0 changes to a new value on the rising edge after L goes high in state 4. It is necessary to save the shift register outputs in this way because another value is being received by the shift register while the previous value is being written into RAM.

A7:0 changes to a new value on the rising edge after P goes high in state 10. The value 4 is stored in location 0 when W goes high in state 8. [8A]

(c) If a continuous sequence of nibbles is transmitted without any intervening zeros, the state machine will cycle through the states *d,e,f,g,h* with V0 being high (corresponding to the prefix bit) whenever in state *e*. We can see from the state diagram, that whenever we are in state *e*, V0 must have been high 5 cycles previously. If the phase of this sequence is incorrect, the value of V0 in state *e* will be one of the data bits rather than the prefix bit. The wrong phase will persist until this data bit happens to equal 0 at which point additional CLOCK cycles will be inserted before reaching state 5 again. Thus the phase will repeatedly slip until it is correct since only then is V0 always high in state *e*.

If there are no intervening zeros between nibbles, synchronization will fail if any of the data bits is high in every nibble for this will allow the path *d,e,f,g,h* to be followed even though the phase is incorrect. Similarly if there is one intervening zero between nibbles, synchronization will fail if all nibble include "01" in a fixed position, for this will allow the cyclic path *d,e,f,i,j,c* to be followed. If any pair of nibbles are separated by "0000" then synchonization is guaranteed for the second nibble. [8A]