ANSWERS – EE10A 2017

1. Use of basic principles to understand the use of a pn diode as a temperature sensor. New application not seen before by the students but based on fundamental knowledge of semiconductor devices applied to pn junctions.

a) . [5]

From formulae sheet:

$$p = N_V \, exp\left(\frac{E_V - E_F}{kT}\right)$$

$$n = N_C \, exp\left(\frac{E_F - E_C}{kT}\right)$$

definition of intrinsic energy E_i:

$$p_i = n_i = N_V \, exp\left(\frac{E_V - E_i}{kT}\right)$$

$$n_i = N_C \, exp\left(\frac{E_i - E_C}{kT}\right)$$

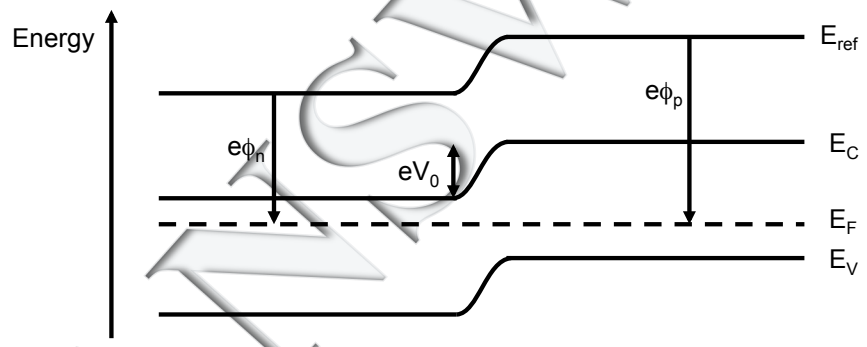
product of these two equations:

$$n_i^2 = N_C \, N_V exp\left(\frac{E_i - E_C}{kT}\right) exp\left(\frac{E_V - E_i}{kT}\right) = N_C \, N_V \, exp\left(\frac{E_V - E_C}{kT}\right) = N_C \, N_V \, exp\left(\frac{-E_G}{kT}\right)$$

Although this question looks like a 1st year question, the knowledge of the concepts is still important and these formulae are also important in the calculations and energy band diagrams related to the 2nd year concept of high level injection. The purpose is to clearly show the temperature dependence of n_i. Many had this correct.

b). [5]

Draw energy band diagram:



ϕ_n and ϕ_p are the workfunction of n and p type region, respectively.

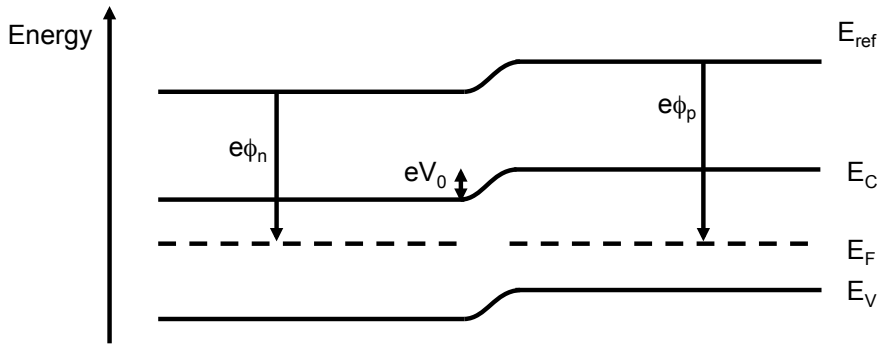
From the plot it is easy to see that: $V_0 = \phi_p - \phi_n$

Very few students had this correct, it seems that the concept of workfunctions and its definition was mostly forgotten by the student cohort. Not having this question right should not hinder the following questions as long as the correct energy band diagram was drawn.

c). [7]

From the solution in a) we can see that the intrinsic carrier concentration is increasing with increasing temperature, assuming that the bandgap and the effective density of state vary more slowly than the exponential function of T. The density of ionized doping atoms will not vary much for temperatures around room temperature (nearly complete ionization at room temperature). This means that with increasing T and thus increasing n_i, the effective carrier concentration will be more and more determined by n_i rather than the doping. Thus

the Fermi levels will move closer to the intrinsic level. This makes the energy band diagram in b) change to the plot below for higher temperatures. [4]



Thus the workfunctions change thus the build-in voltage decreases.
When the build in voltage decreases then less voltage needs to be applied across the diode to lower the potential barrier eV_0 to switch the diode on. Thus for T increase V_{on} decreases. [3]

Most students did associate a higher temperature with a higher density of free carriers. However, the connection between more electrons and holes due to an increase in **intrinsic** carriers and the shift in position of the Fermi level was overlooked. The higher density was associated with higher N_D and N_A, which is wrong as those are constant as these are determined by the fabrication process.

d) bookwork with a twist (explicit influence of temperature is new) and without giving the switching circuit as done in previous exam questions. This thus also tests the students' knowledge on terminology. [8]

Assume that the delay is mainly caused by the minority carrier holes (derivation is same when assuming this for electrons).

From coursenotes derive switching equations:

$$\frac{dQ_p(t)}{dt} = i_p(t) - \frac{Q_p(t)}{\tau_p}$$

For $0 < t < t_{sd}$ with t_{sd} the storage delay time, we know that i_p remains constant at $-I_r$, thus:

$$\frac{dQ_p(t)}{dt} = -I_r - \frac{Q_p(t)}{\tau_p}$$

Separation of variables:

$$\frac{dQ_p(t)}{Q_p(t) + \tau_p I_r} = -\frac{dt}{\tau_p}$$

Integrate:

$$\int_{Q_p(0)}^{Q_p(t)} \frac{dQ_p(t)}{Q_p(t)+\tau_p I_r} = -\int_0^t \frac{dt}{\tau_p}$$

$$\ln\left(Q_p(t)+\tau_p I_r\right)\Big|_{\tau_p I_f}^{Q_p(t)} = -\frac{t}{\tau_p}$$

$$\ln\left(Q_p(t)+\tau_p I_r\right) - \ln\left(\tau_p I_F + \tau_p I_r\right) = -\frac{t}{\tau_p}$$

$$\ln\frac{\left(Q_p(t)+\tau_p I_r\right)}{\left(\tau_p I_F + \tau_p I_r\right)} = -\frac{t}{\tau_p}$$

$$Q_p(t) = -\tau_p I_r + \left(\tau_p I_F + \tau_p I_r\right)\exp\left(-\frac{t}{\tau_p}\right)$$

or

$$Q_p(t) = \tau_p\left[-I_r + \left(I_f + I_r\right)\exp\left(\frac{-t}{\tau_p}\right)\right]$$

valid for $0 < t < t_{sd}$ only.
Approximate that at $t=t_{sd}$, $Q_p(t_{sd})=0$. Thus:

$$0 = \tau_p\left[-I_r + \left(I_f + I_r\right)\exp\left(\frac{-t_{sd}}{\tau_p}\right)\right]$$

The storage delay time is then:

$$t_{sd} \cong \tau_p \ln\left[1+\frac{I_f}{I_r}\right]$$ [4] marks for the derivation

Calculating t_{sd} at T = 25 °C and 75 °C using I_f from figure 1.1 at diode voltage of 0.45V.
[Note: the IVs are plotted such that these values can be easily extracted with a ruler.]

T = 25 °C I_f = 100 μA - $t_{sd}(\mu s) = 1\times ln\left[1+\frac{100}{200}\right] = 0.41\mu s$

T = 75 °C I_f = 1000 μA - $t_{sd}(\mu s) = 1\times ln\left[1+\frac{1000}{200}\right] = 1.79\mu s$

The storage delay time increases by almost a factor of 2 (1.93) [4]

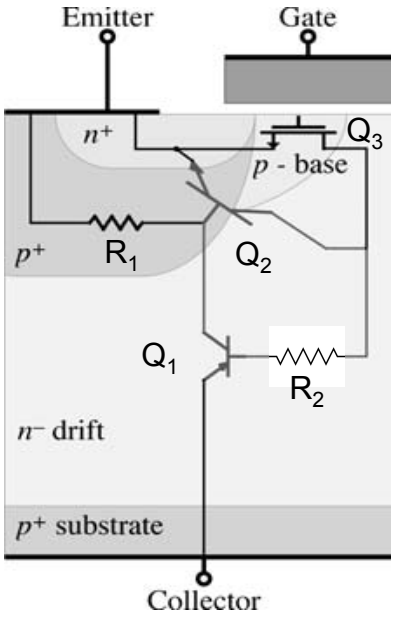
[Note: this will cause even more heating of the diode (thermal runaway).]

The derivation of the storage delay time has been done in the lecture, the class and in multiple past exam papers. Errors against this cannot be accepted. There were quite a bit of sign errors made for I_r positive or negative in relationship to the reverse bias current of 200μA given in the question.

Marks were given for reading correct approximate values from the graph given in the figure in the question. Many who did not get the previous part correct wrote a short reasoning down of why they expected the delay time to increase. Marks were given when this reasoning was correct.

2. This question is bookwork

a) A half cell is drawn below. [8]

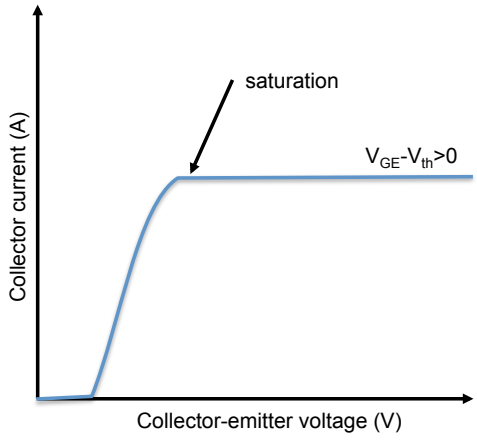


Main error here was not having the p-type collector bulk contact and thus drawing an npn rather than pnp IGBT. The problem was that some students draw such small messy sketches that sometimes these cannot be marked as they cannot be read or there are too many conflicting parameters.

Make messy sketches on scrap paper to focus the mind on the important items and then make a big neat sketch in the answer book!!!!

b) main IGBT components are Q3: MOSFET for control of base current (input) and Q1 pnp BJT for output current generation. [8]
The parasitics are: Q2 across the MOSFET, this is normally off by shorting the p+ (can also be made p) and n+ region via the top contact, however a voltage drop across the bulk resistor R1 can create a voltage difference turning the parasitic BJT on. R2 is the parasitic resistor from the lowly doped n- drift region.
The question asked explicitly to draw the equivalent circuit in the material cross section, when not done, marks were subtracted. For the parasitics the main resistance is that due to the lowly doped drift region, the other resistance was not observed by the majority of the student cohort.

c) Saturation is due to pinch-off of the MOSFET Q3. [4]



Important in the characteristics sketch is that the IV characteristic does not immediately increase for small VEC due to the initially large recombination current.

d) A typical transient characteristic of an IGBT is given in fig. 2.1. Answer the following questions.

i) charging of the gate capacitance until the threshold voltage is reached. [2]

ii) removal of the excess minority carrier charge in the drift region via recombination. [2]

iii) In the EE2-10A module loads are resistive and therefore no overshoots are observed. Overshoots occur when loads are inductive. [1]

This was an easy question. Only few had iii) correctly associated with inductance influences. Those doing power electronics next year better remember.