Final copy - June 03 E2.2

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2003

ANALOGUE ELECTRONICS 2

Monday, 16 June 2:00 pm

Time allowed: 2:00 hours

There are FIVE questions on this paper.

Question 1 is compulsory. Answer question 1 and two others

Question 1 has 10 multiple choice questions labelled a-j, all carrying equal marks. There is only one correct answer per question.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : E Rodriguez-Villegas
Second Marker(s) : C. Papavassiliou

Special Information for Invigilators: none

Information for Candidates

1. The candidates MUST answer Question 1 (group of 10 multiple choice questions) **and any two of the remaining four questions.**

2. The multiple choice question **MUST** be done in the separate answer sheet provided. No credit will be given for answers not recorded on this sheet.

3. The symbol || has been used to represent parallel connection of impedances.

1) Mandatory question: 10 multiple choice questions.

Please answer on separate handout.

Answer each of the following questions on the separate answer sheet provided. Note that there is only one correct statement in each group of 3 statements.

Each correct answer carries 2 marks. If you do not attempt a question you do not earn (or lose) any marks.

Each wrong answer carries a 1 mark penalty. If the total mark for Question 1 is negative it will be reported as zero.

(a)

(i) The input of a simple CMOS current mirror is low impedance.

(ii) The input of a simple CMOS current mirror is high impedance.

(iii) The impedance at the input of a CMOS current mirror is much higher than at the output.

(b)

(i) The gain of a common-source amplifier is $-g_{m3}(r_{ds3} \| r_{ds2})$, where g_{m3} and r_{ds3} are the transconductance and output resistance of the input transistor respectively, and r_{ds2} is the resistance of the load transistor.

(ii) The gain of a common-source amplifier is $-g_{m3}(r_{ds3} \| r_{ds2})$, where g_{m3} and r_{ds3} are the transconductance and output resistance of the load transistor respectively, and r_{ds2} is the resistance of the input transistor.

(iii) The gain of a common-source amplifier is $-g_{m3}r_{ds3}$, where g_{m3} and r_{ds3} are the transconductance and output resistance of the input transistor respectively.

(c)

(i) The DC level at the output of a source follower does not depend on the bias current.

(ii) The DC level at the output of a source follower does not change because of technological variations in the threshold voltage.

(iii) The DC level at the output of the source follower depends on the sizing of the input transistor.

(d)

(i) The common-gate amplifier is used as a gain stage when a relatively small input impedance is desired.

(ii) The common-gate amplifier is used as a gain stage when a relatively small output impedance is desired.

(iii) The common-gate amplifier is not adequate to terminate a 50Ω transmission line.

(e)

(i) The cascode current mirror improves the performance of the simple current mirror thanks to its increased output resistance.

(ii) The cascode current mirror improves the performance of the simple current mirror thanks to its increased input resistance.

(iii) The cascode current mirror increases the maximum output-signal swings before transistors enter the triode region.

(f)

(i) Source follower circuits can exhibit large amounts of overshoot and ringing under certain conditions.

(ii) The parasitic capacitances and output impedance in practical source followers typically result in high overshoot.

(iii) If a source follower exhibits overshoot there is nothing the designer can do.

For the opamp below:

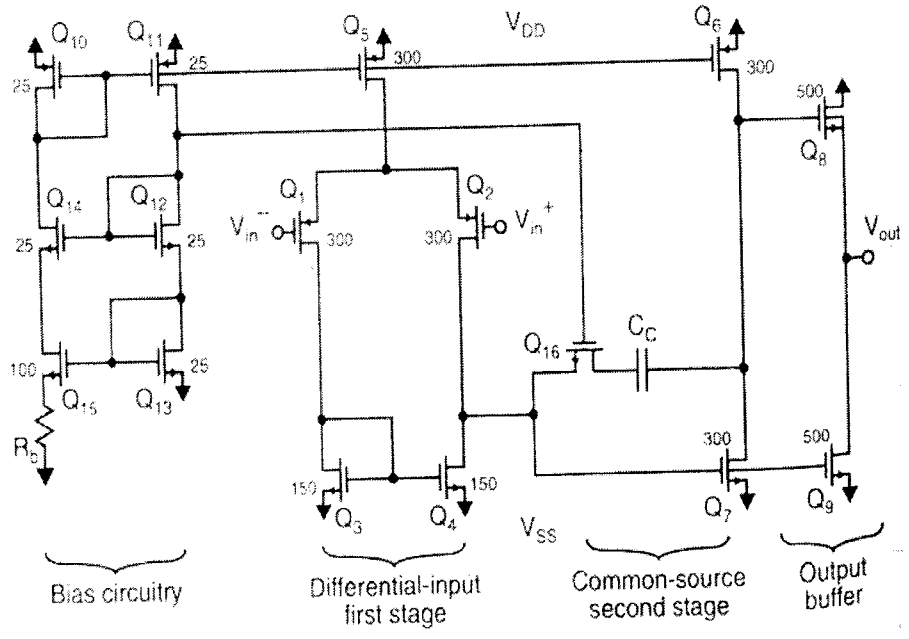


Figure 1.1: Three-stage opamp.

(g)

(i) The Slew Rate can be improved by increasing the tail current, I_{D5} (drain current of Q_5).

(ii) If the SR is improved (for a given value of C_c) the unity gain frequency does not change.

(iii) For large signals the output voltage can change faster than the limit imposed by the SR.

(h)

(i) The transconductance at the input of the second stage will not have any influence on the pole at the output of the first stage.

(ii) The pole at the output of the first stage can be moved towards a higher frequency by decreasing the output resistance of the second stage.

(iii) The zero at the output of the first stage can be moved towards a higher frequency by decreasing the output resistance of the second stage.

(i) Assuming that the gain of the third stage is exactly one, for midband frequencies, the unity gain frequency is:

(i) g_{m1}/C_c
(ii) increased by decreasing the tail current of the first stage.
(iii) independent on C_c.

(j)

(i) For a given power dissipation, the Slew Rate is better in a p-channel input stage.
(ii) For a given power dissipation, the Slew Rate is better in a n-channel input stage.
(iii) The Slew Rate is independent of the input stage.

END MULTIPLE CHOICE QUESTIONS

[20]

2.

(a) In figure 2.1 we give a partial small signal equivalent circuit model of a Bipolar Junction Transistor (BJT). Complete this diagram:

i. Identify the transistor terminals
ii. Identify the components given
iii. Add and identify one resistance that is missing
iv. Add and identify 4 capacitances that are missing.

For each component of the complete equivalent circuit write an expression giving its value and its dependence on transistor terminal voltages or currents, as the case may be.

[6]

(b) Define the output resistance of a 2-port network. Define also the output admittance of a two port network. Why, in general, is the output admittance different than the inverse of the output resistance?

[6]

(c) Consider the amplifier of figure 2.2 biased at a given current (for example at 1 mA), in the limit of very large R_C.

i. Draw the equivalent circuit for this amplifier at high enough frequencies so that you may neglect a resistance connected in parallel with a capacitance.

[3]

ii. Derive an expression for the output impedance of this amplifier at high frequencies. Show that the output impedance approaches a real value.

[5]

HINT: The frequency is high but not infinite. In the limit of infinite frequency the output impedance evidently approaches zero.

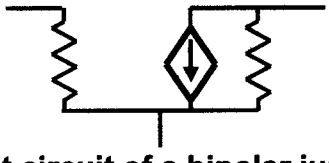


Figure 2.1: Partial equivalent circuit of a bipolar junction transistor

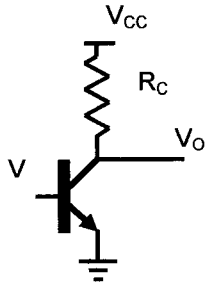


Figure 2.2: Amplifier in question 2(c)

3.

(d) Write equations defining the small signal 2-port Y matrix of an electronic device with 3 or 4 terminals. Define all the matrix entries in terms of voltages and currents applied to, and measured on, the device terminals.

[5]

(e) Derive an expression for the input impedance of a 2-port device when its output is connected to a load impedance Z_L. Express your answer in terms of the device's Y parameters.

[5]

(f) A length l of coaxial cable has the following Y matrix representation:

$$\mathbf{Y} = \frac{1}{jZ_0 b}\begin{bmatrix} a & 1 \\ 1 & a \end{bmatrix}$$

where Z_0 is the "characteristic impedance" of the cable and *a*, and *b* relate to the length of the cable (λ is the wavelength of the AC signal on the cable):

$$a = \cos\frac{2\pi l}{\lambda} \quad , \quad b = \sin\frac{2\pi l}{\lambda}$$

(i) What is the input impedance of this piece of coaxial cable when its output is connected to a load Z_L ? (**hint:** observe that $a^2 + b^2 = 1$)

(ii) What is the cable input impedance when the load is an open circuit?

(iii) What is the cable input impedance when the load is a short circuit?

(iv) For what values of the cable length is the input impedance, Z_{in}, given by:

$$Z_{in} = \frac{Z_0^2}{Z_L}$$

for any load impedance Z_L ?

[10]

4. Read all the instructions for this question before attempting to write your answer.

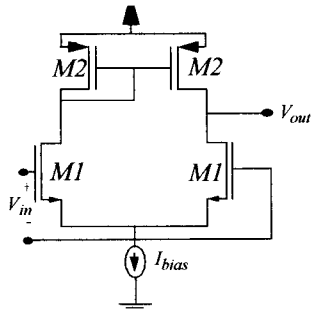
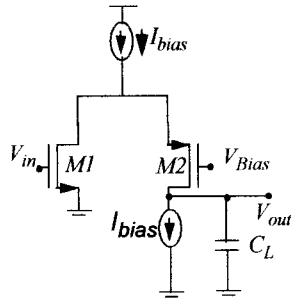
The objective of this question is to complete the table below. Part of the table has already been completed for you. The information required to complete the table can be ascertained by analysing the two circuits at the top of the table. What follows is a detailed description of the table and what you are expected to write in it.

The three rows under the two circuits are labelled **A**, $\mathbf{r_{in}}$ and $\mathbf{r_o}$. These perfomances parameters are the voltage gain (**A**), the input resistance ($\mathbf{r_{in}}$) and the output resistance ($\mathbf{r_o}$) of the circuits. You are required to write the correct mathematical expression or correct numerical value for each performance parameter for the two circuits. If you decide that a mathematical expression is the correct answer your expression should use only the small signal parameters g_m and g_{ds} of the transistors. For example, the voltage gain (**A**) of the left hand circuit is: $g_{m1}/(g_{ds1}+g_{ds2})$. This expression has already been included for you. The numeric subscript i refers to the transistor M_i. For example, g_{m1} is the gate to source transconductance of transistor M_1. The expression for the output resistance ($\mathbf{r_o}$) and input resistance ($\mathbf{r_{in}}$) of the right hand circuit has also been included.

In the lower part of the table you are required to indicate the effect on the absolute value of the voltage gain (**A**), the input resistance ($\mathbf{r_{in}}$) and the output resistance ($\mathbf{r_o}$) of **increasing**, one at a time, the following design parameters: W_1, W_2, L_1, L_2 and I_{bias}. The design parameters W_i and L_i are the width and length of the i^{th} transistors respectively. I_{bias} is the biasing current of each circuit and determines the operating point. You should indicate your answer using one of the following symbols: ↑, ↓, – . The symbol ↑ indicates that the performance parameter **increases** when you **increase** the circuit design parameter. The symbol ↓, indicates that the performance parameter **decreases** when you **increase** the circuit design parameter. The symbol **-** indicates that the performance parameter **does not change** when you **increase** the circuit design parameter. For example, for the right hand circuit, increasing W_1 does not affect either r_{in} or r_o, but increasing L_1 increases r_o and increasing I_{bias} decreases r_o. For the left hand circuit increasing I_{bias} reduces A and it is not possible to say what the affect of L_1 on A will be. These examples have already been included in the table. Note that the entry X is not

required any where else in the table. **You should only use the symbols ▲, ▼ and -.**

You will be given marks for correct answers only. Marks will **not** be deducted for incorrect answers.

Design Tradeoff ("Thumbs") Table						
CIRCUIT						
A	$g_{m1}/(g_{ds1}+g_{ds2})$					
r_{in}				∞		
r_o				$g_{m2}/(g_{ds1}g_{ds2})$		
INCREASE	***A***	r_{in}	r_o	***A***	r_{in}	r_o
W_1					-	-
W_2						▲
L_1	X					
L_2	▼					▼
I_{bias}						

[20]

5. **Read all the instructions for this question before attempting to write your answer. At the end of these instructions there is some useful data and assumptions that you will need to work out your answers.**

For the opamp in Figure 5.1 answer the following questions:

(a) Calculate the gain of the first stage.

[3]

(b) Calculate the gain of the second stage.

[3]

(c) Calculate the gain of the third stage.

[3]

(d) Calculate the overall gain.

[2]

(e) What is the dominant pole frequency of this circuit? Hence, or otherwise, calculate the unity-gain frequency in Hz. For this part of the problem you can assume the gain of the output buffer to be unity.

[3]

(f) Calculate the Slew Rate. How can the circuit be modified so that the Slew Rate is doubled while the unity gain frequency and bias are kept constant?

[3]

(g) If Q_3 and Q_4 widths are reduced from 150μm to 120μm and the output stage has a bias current of 150μA, find the widths of Q_6 and Q_7, such that there is no systematic offset voltage.

[3]

You may use the following data and assumptions:

- The subscript i refers to the transistor Q_i in Figure 5.1.

- The widths of the transistors are given by the numbers in μm which appear beside them in Figure 5.1. All transistor lengths are 1.6μm. For example, Q_5 has a width of 300μm and a length of 1.6μm.

- The bias current (drain current of transistor Q_5) of the input differential pair is

I_{D5}= 100μA and the power supplies are V_{DD}=-V_{SS}=2.5V. Also, R_L=10kΩ, and C_c=5pF.

- The following process parameters also apply:

  $\mu_n C_{ox}=3\mu_p C_{ox}=96\mu A/V^2$, $\gamma=0.5V^{1/2}$, $\phi_F=0.35V$

  $\alpha = 5\times 10^6 (\sqrt{V})/m$ and V_{tn}=- V_{tp}=0.8V

- To estimate output impedances, assume that $r_{ds} \approx \alpha \frac{L}{I_D}\sqrt{V_{DG}+V_{tn}}$ and $r_{ds} \approx \alpha \frac{L}{I_D}\sqrt{|V_{DG}|+|V_{tp}|}$, for the n and p transistors respectively, the drain-to-gate voltages of the first-stage transistors equal to 0.5V, whereas the transistors in the second and third stages have V_{DGi}=1V. Finally, the substrate of Q8 is connected to the negative power supply ($g_s = \frac{g_m \gamma}{2\sqrt{V_{SB}+2\phi_F}}$), so that V_{SB8}=2.5V.

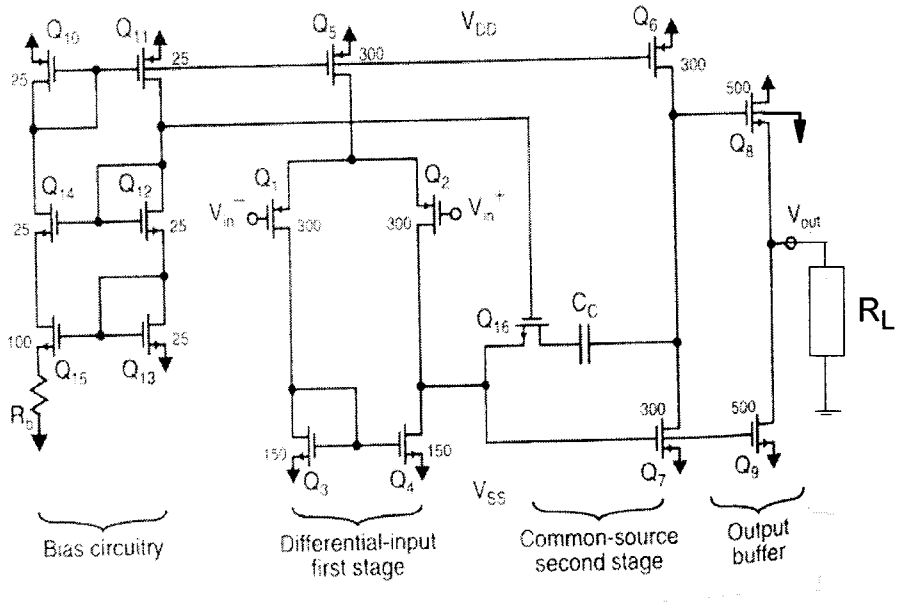


Figure 5.1: Three-stage opamp.

Final – June 2003

Department of Electrical and Electronic Engineering Examinations 2003 Confidential		
Model Answers and Mark Schemes	First Examiner:	Esther Rodriguez-Villegas
Paper Code: EE2.2	Second Examiner:	Christos Papavassiliou

1. **(bookwork)**

(a)

(i) The input of a simple CMOS current mirror is low impedance.

(ii) The input of a simple CMOS current mirror is high impedance.

(iii) The impedance at the input of a CMOS current mirror is much higher than at the output.

(b)

(i) The gain of a common-source amplifier is: $-g_{m3}(r_{ds3} \| r_{ds2})$, being g_{m3} and r_{ds3} the transconductance and output resistance of the input transistor respectively, and r_{ds2} the resistance of the load transistor.

(ii) The gain of a common-source amplifier is: $-g_{m3}(r_{ds3} \| r_{ds2})$, being g_{m3} and r_{ds3} the transconductance and output resistance of the load transistor respectively, and r_{ds2} the resistance of the input transistor.

(iii) The gain of a common-source amplifier is: $-g_{m3}r_{ds3}$, being g_{m3} and r_{ds3} the transconductance and output resistance of the input transistor respectively.

(c)

(i) The DC level at the output of the source follower does not depend on the bias current.

(ii) The DC level at the output of the source follower does not change because of technological variations in the threshold voltage.

(iii) The DC level at the output of the source follower depends on the sizing of the input transistor.

(d)

(i) The common-gate amplifier is used as a gain stage when a relatively small input impedance is desired.

(ii) The common-gate amplifier is used as a gain stage when a relatively small output impedance is desired.

(iii) The common-gate amplifier is not adequate to terminate a 50Ω

Department of Electrical and Electronic Engineering Examinations 2003 Confidential

Model Answers and Mark Schemes First Examiner: Esther Rodriguez-Villegas

Paper Code: EE2.2 Second Examiner: Christos Papavassiliou

transmission line.

(e)

(i) The cascode current mirror improves the performance of the simple current mirror thanks to its increased output resistance.

(ii) The cascode current mirror improves the performance of the simple current mirror thanks to its increased input resistance.

(iii) The cascode current mirror increases the maximum output-signal swings before transistors enter the triode region.

(f)

(i) Source follower circuits can exhibit large amounts of overshoot and ringing under certain conditions.

(ii) The parasitic capacitances and output impedance in practical source followers typically result in high overshoot.

(iii) If a source follower exhibits overshoot there is nothing the designer can do.

For the opamp below:

Department of Electrical and Electronic Engineering Examinations 2003 Confidential		
Model Answers and Mark Schemes	First Examiner:	Esther Rodriguez-Villegas
Paper Code: EE2.2	Second Examiner:	Christos Papavassiliou

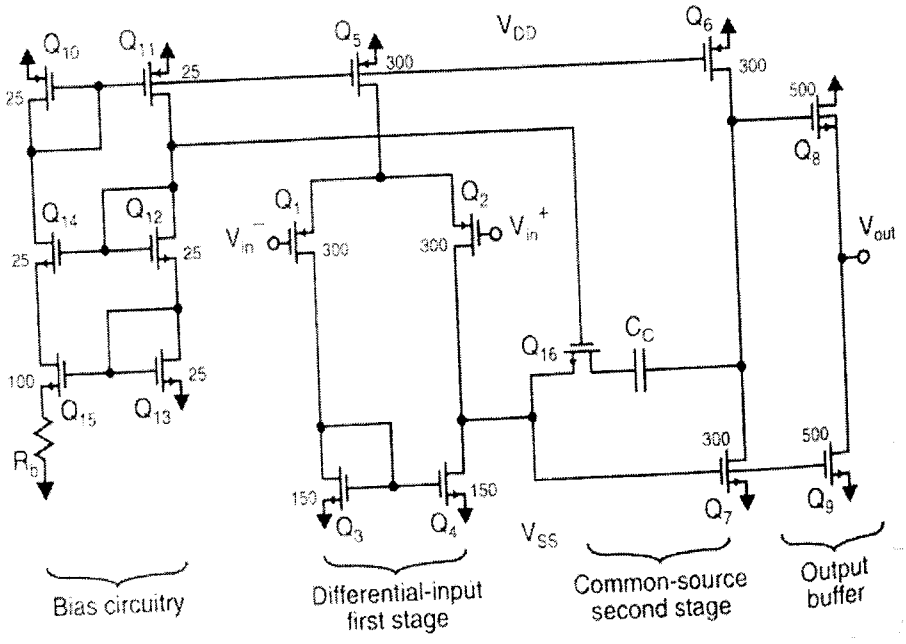


Figure 1.1: Three-stage opamp.

(g)

(i) The Slew Rate can be improved by increasing the tail current, I_{D5}.

(ii) If the SR is improved (for a given value of C_c) the unity gain frequency does not change.

(iii) For large signals the output voltage can change faster than the limit imposed by the SR.

(h)

(i) The transconductance at the input of the second stage will not have any influence on the pole at the output of the first stage.

(ii) The pole at the output of the first stage can be moved towards a higher frequency by decreasing the output resistance of the second stage.

(iii) The zero at the output of the first stage can be moved towards a higher frequency by decreasing the output resistance of the second stage.

(i) Assuming that the gain of the third stage is exactly one, for midband

Department of Electrical and Electronic Engineering Examinations 2003		Confidential
Model Answers and Mark Schemes	First Examiner:	Esther Rodriguez-Villegas
Paper Code: EE2.2	Second Examiner:	Christos Papavassiliou

frequencies, the unity gain frequency is:

(i) g_{m1}/C_c

(ii) increased by decreasing the tail current of the first stage.

(iii) independent on C_c.

(j)

(i) For a given power dissipation, the SR is better in a p-channel input stage.

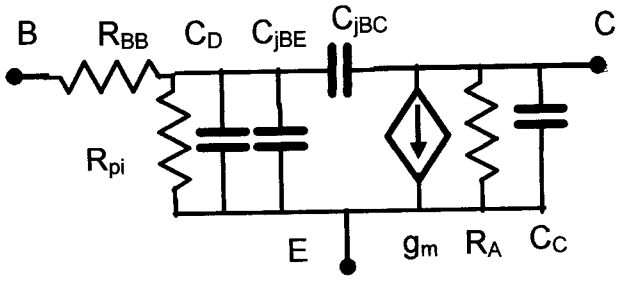
(ii) For a given power dissipation, the SR is better in a n-channel input stage.

(iii) The SR is independent of the input stage.

Department of Electrical and Electronic Engineering Examinations 2003		Confidential
Model Answers and Mark Schemes	First Examiner:	Esther Rodriguez-Villegas
Paper Code: EE2.2	Second Examiner:	Christos Papavassiliou

2.

(a) (bookwork)



r_{bb} base contact resistance, no dependence on V,I

r_{be} input resistance, $r_{be} = \frac{\beta V_T}{I_C}$

C_d Diffusion capacitance, C_d ; $g_m/(2\pi f_T)$

C_J junction emitter-base capacitance, $C_j = \frac{C_{j0}}{\sqrt{1-\frac{V_{BE}}{\Phi}}}$ (or denominator to power 1/(m+2) where m is the power of the doping profile, m=0 for uniform doping.

C_{cb} junction base-collector capacitance, similar dependence as C_J

g_m transconductance, $g_m = \frac{I_C}{V_T}$

r_{CE} output (Early) resistance, $r_{CE} = \frac{V_A}{I_C}$

C_{CE}: output capacitance

[5]

(b) (Bookwork)

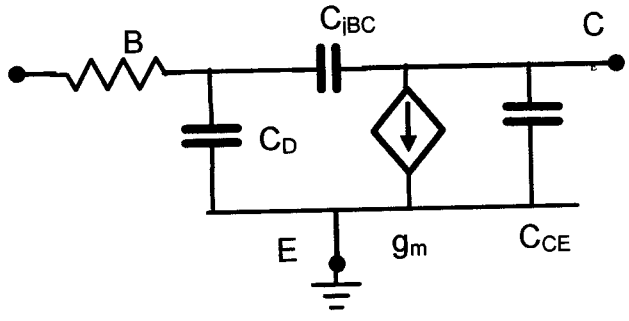
$Y_{out} = \left.\frac{\partial I_o}{\partial V_o}\right|_{V_k=0}$, $Z_{out} = \left.\frac{\partial V_o}{\partial I_o}\right|_{I_{j=0}}$ Y is measured with other terminals open circuited, (I=0) while Z with other terminals short circuited. For a 2-port network Y_{out} is the output entry of the admittance matrix, while Z_{out} is the output entry of the impedance matrix. The two matrices are the inverse of each other, but not the corresponding entries.

[5]

Department of Electrical and Electronic Engineering Examinations 2003		Confidential
Model Answers and Mark Schemes	First Examiner:	Esther Rodriguez-Villegas
Paper Code: EE2.2	Second Examiner:	Christos Papavassiliou

(c) New computed example

Ignore R_{pi} and R_A as suggested. Also ignore C_j in base-emitter. Can also ignore C_D. What is left of the circuit is:



The capacitive divider between collector and emitter give the base voltage:

$$V_B = V_C \frac{C_{BC}}{C_{BC}+C_D}$$

The collector current is:

$$I_C = j\omega V_C\left(C_{BC}+C_{CE}\right)+V_B g_m = V_C\left(j\omega\left(C_{BC}+C_{CE}\right)+\frac{g_m C_{BC}}{C_{BC}+C_D}\right)\Rightarrow$$

$$Z_c = \frac{V_C}{I_C} \approx \left(j\omega\left(C_{BC}+C_{CE}\right)+\frac{g_m C_{BC}}{C_{BC}+C_D}\right)^{-1} \approx \frac{C_{BC}+C_D}{g_m C_{BC}} \approx \frac{C_D}{g_m C_{BC}} = \frac{1}{C_{BC}\omega_T}$$

[10]

(a) (bookwork)

$$\begin{aligned} I_1 &= Y_i V_1 + Y_r V_2 \\ I_2 &= Y_f V_1 + Y_o V_2 \end{aligned} \quad or \quad \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_i & Y_r \\ Y_f & Y_o \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$\left.\frac{\partial I_1}{\partial V_1}\right|_{v_2=0} = Y_i \qquad \left.\frac{\partial I_1}{\partial V_2}\right|_{v_1=0} = Y_r$$

$$\left.\frac{\partial I_2}{\partial V_1}\right|_{v_2=0} = Y_f \qquad \left.\frac{\partial I_2}{\partial V_2}\right|_{v_1=0} = Y_o$$

[5]

Department of Electrical and Electronic Engineering Examinations 2003		Confidential
Model Answers and Mark Schemes	First Examiner:	Esther Rodriguez-Villegas
Paper Code: EE2.2	Second Examiner:	Christos Papavassiliou

(b) (extension of bookwork)

$$I_2 = Y_f V_1 + Y_o V_2 = -V_2 / Z_L \Rightarrow V_2 = -V_1 \frac{Y_f}{Y_o + Y_L}$$

(note convention for current into the 2-port)

$$I_1 = Y_i V_1 + Y_r V_2 = V_1 \left(Y_i - \frac{Y_r Y_f}{Y_o + Y_L} \right) = V_1 \left(\frac{Y_i Y_L + \Delta_Y}{Y_o + Y_L} \right) \text{ then,}$$

$$Z_{in} = \frac{Y_o + Y_L}{Y_i Y_L + \Delta_Y} \text{ with } \Delta_Y = Y_i Y_o - Y_f Y_r$$

[5]

(c) (new computed example)

For the matrix given,

$$\Delta_Y = \frac{1}{Z_0^2}$$

substituting from above,

$$Z_{in} = \frac{Y_o + Y_L}{Y_i Y_L + \Delta_Y} = \frac{\dfrac{\cos\theta}{jZ_0 \sin\theta} + \dfrac{1}{Z_L}}{\dfrac{1}{Z_0^2} + \dfrac{\cos\theta}{jZ_0 Z_L \sin\theta}} = Z_0 \frac{Z_L + jZ_0 \tan\theta}{Z_0 + jZ_L \tan\theta}$$

[5]

open (short) termination : capacitive (inductive) in $n\frac{\lambda}{2} \le l \le (2n+1)\frac{\lambda}{4}$,

inductive (capacitive) otherwise.

Impedance inversion for $l = (2n+1)\frac{\lambda}{4}$

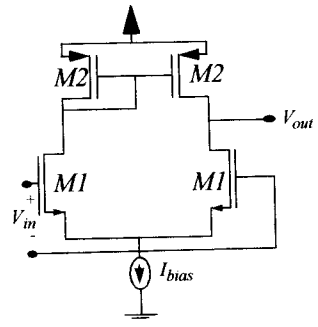
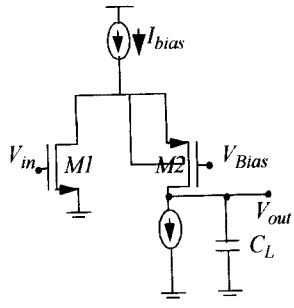
(note : full credit even if candidate does not notice the periodic behaviour.)

[5]

Department of Electrical and Electronic Engineering Examinations 2003		Confidential
Model Answers and Mark Schemes	First Examiner:	Esther Rodriguez-Villegas
Paper Code: EE2.2	Second Examiner:	Christos Papavassiliou

4. (new theoretical application)

Thumb Table

CIRCUIT						
A	$g_{m1}/(g_{ds1}+g_{ds2})$			$-g_{m2}g_{m1}/(g_{ds1}g_{ds2})$		
r_{in}	∞			∞		
r_o	$1/(g_{ds1}+g_{ds2})$			$g_{m2}/(g_{ds1}g_{ds2})$		
INCREASE	**A**	**r_{in}**	**r_o**	**A**	**r_{in}**	**r_o**
W_1	↑	-	-	↑	-	-
W_2	-	-	-	↑	-	↑
L_1	$\frac{\sqrt{\downarrow}}{(g_{ds2}+\downarrow)}$	-	↑	↑	-	↑
L_2	↑	-	↑	↑	-	↑
I_D	↓	-	↓	↓	-	↓

[20]

Department of Electrical and Electronic Engineering Examinations 2003		Confidential
Model Answers and Mark Schemes	First Examiner:	Esther Rodriguez-Villegas
Paper Code: EE2.2	Second Examiner:	Christos Papavassiliou

5. **(new computed example)**

(a)

First the bias current are calculated. Since $I_{D5} = 100\mu A$, we have:

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{D5}/2 = 50\mu A$$

$$I_{D6} = I_{D7} = (W_6/W_5)I_{D5} = 100\mu A$$

$$I_{D8} = I_{D9} = (W_9/W_7)I_{D7} = 167\mu A$$

The transconductances, using $g_{mi} = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)I_{Di}}$ are:

$$g_{m1} = g_{m2} = 0,775mA/V \qquad g_{m7} = 1,90mA/V \qquad g_{m8} = 3,16mA/V$$

The next step is to estimate the output impedances of the transistors, using $r_{ds} \approx \alpha \frac{L}{I_D}\sqrt{V_{DG} + V_t}$:

$$r_{ds1} = r_{ds2} = r_{ds3} = r_{ds4} = 182k\Omega \qquad r_{ds6} = r_{ds7} = 107k\Omega$$

$$r_{ds8} = r_{ds9} = 64k\Omega$$

The last parameter we need to calculate is the body-effect conductance of Q8, using $g_s = \frac{g_m\gamma}{2\sqrt{V_{SB} + 2\phi_F}}$ and assuming V_{SB8}=2.5V, $g_{s8} = 0,44mA/V$

(a)

$$A_{v1} = g_{m1}(r_{ds2} \| r_{ds4}) = -70,2$$

(b)

Department of Electrical and Electronic Engineering Examinations 2003 **Confidential**

Model Answers and Mark Schemes | First Examiner: Esther Rodriguez-Villegas

Paper Code: EE2.2 | Second Examiner: Christos Papavassiliou

$$A_{v2} = -g_{m7}(r_{ds6} \| r_{ds7}) = -102$$

(c)

$$A_{v3} \cong \frac{g_{m8}}{G_L + g_{m8} + g_{s8} + g_{ds8} + g_{ds9}} = 0,85$$

(d)

The total gain: $A_{v1}A_{v2}A_{v3} = 6090$

(e)

$$f_{ta} = \frac{g_{m1}}{2\pi C_c} \approx 24,5 Mrad/s$$

(f)

$$SR = \frac{2I_{D1}}{C_c} = 20(V/\mu s)$$

To double the SR, C_c should be set to 2.5pF. To maintain the same unity-gain frequency, g_{m1} should be halved, which can be accomplished by decreasing the widths of Q1 and Q2 by 4.

(g)

Since I_{D6} determines the bias current of the output stage, and since it should have 50 percent more current than I_{D5}, its width should be 50 percent greater than W5, resulting in:

$$W_6 = 450\mu m$$

The necessary condition to ensure that no-input offset voltage is present is:

$$\frac{(W/L)_7}{(W/L)_4} = 2\frac{(W/L)_6}{(W/L)_5}$$

This gives:

$$W_7 = 360\mu m$$