IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2017

EEE PART I: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 1

Corrected copy

Wednesday, 14 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : A.S. Holmes
Second Marker(s) : C. Papavassiliou

The Questions

1. For each part of this question, state clearly any assumptions made in your calculations.

   a) For the circuit in Figure 1.1, determine the operating mode of the MOSFET and the value of the voltage V.

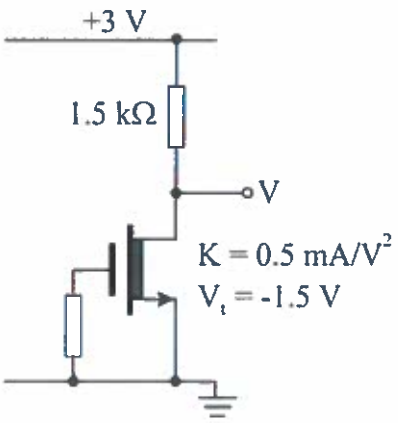

Figure 1.1 [6]

   b) Calculate the small-signal voltage gain of the amplifier in Figure 1.2. Also, on separate diagrams, sketch the output waveforms corresponding to sinusoidal input signals with amplitudes of 25 mV peak-to-peak and 200 mV peak-to-peak.

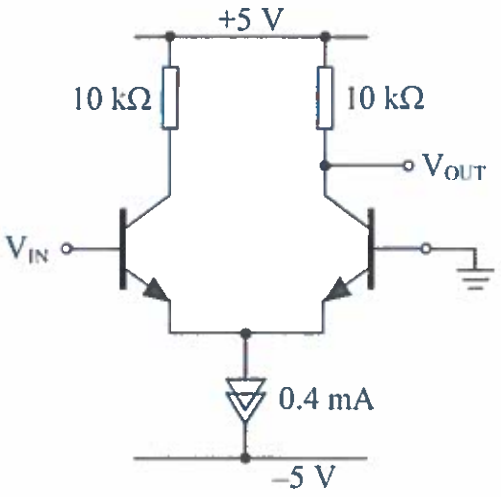

Figure 1.2 [10]

   c) A diode-connected MOSFET is a 2-terminal device formed by connecting together the gate and drain of a MOSFET. Sketch the I-V characteristic for such a device, assuming an n-channel enhancement mode transistor. Show clearly any boundaries between different operating modes. [6]

Question 1 continues on the next page...

Question 1 continued

d) For the partial circuit in Figure 1.3, draw a small-signal equivalent and derive an expression for the small-signal output resistance in terms of R_S and the small-signal parameters g_m and r_o of the transistor. You may assume that $V_G > V_t$ and that the drain is held at a sufficiently high potential for the transistor to be in active mode.

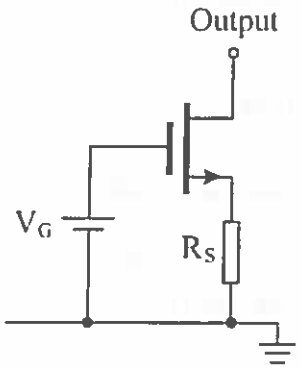

Figure 1.3

[6]

e) The input voltage V_{IN} applied to the circuit in Figure 1.4 changes suddenly from zero to +5 V at time t = 0, having previously been at zero for a long time. If V_{IN} remains at +5 V for t > 0, calculate how long the transistor remains in saturation. Also derive an expression for the time variation of the output voltage V_{OUT} once the transistor has come out of saturation. Hence draw a dimensioned sketch showing the time variation of V_{OUT} for $-10\ \mu s \le t \le 50\ \mu s$.

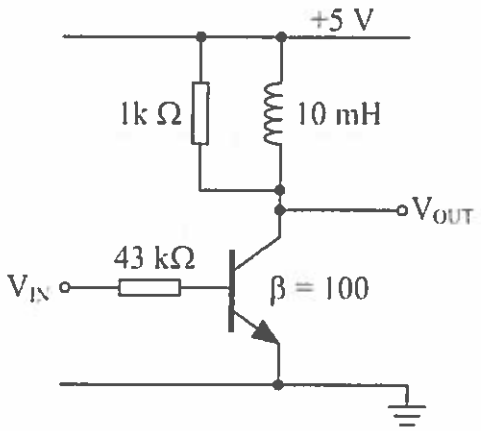

Figure 1.4

[8]

f) The characteristic equation for a phase-shift oscillator is of the form:

$$(1+K)u^3 + 6u^2 + 5u + 1 = 0$$

where K is the voltage gain of the amplifier, and $u = sRC$, with s being complex frequency and R, C being the component values in the phase-shifting network. Starting from this equation derive an expression for the frequency of stable oscillation.

[4]

2. a) Determine the collector bias current and the quiescent output voltage for the amplifier shown in Figure 2.1, stating clearly any assumptions you make. Your calculations should take into account the base current of the transistor. [8]

b) Draw a small-signal equivalent circuit of the amplifier, and hence determine the small-signal macromodel parameters, i.e. the input resistance, output resistance and voltage gain. You may assume the transistor has infinite small-signal output resistance. [12]

c) The amplifier is inserted between a signal source and a load as shown in Figure 2.2. Calculate the overall voltage gain v_L/v_S for this arrangement in the mid-band, where the coupling capacitors C_1 and C_2 are effectively short-circuit. [6]

d) Choose the values of C_1 and C_2 so that cut-off frequencies of the input and output networks in Figure 2.2 are both 100 Hz. [4]

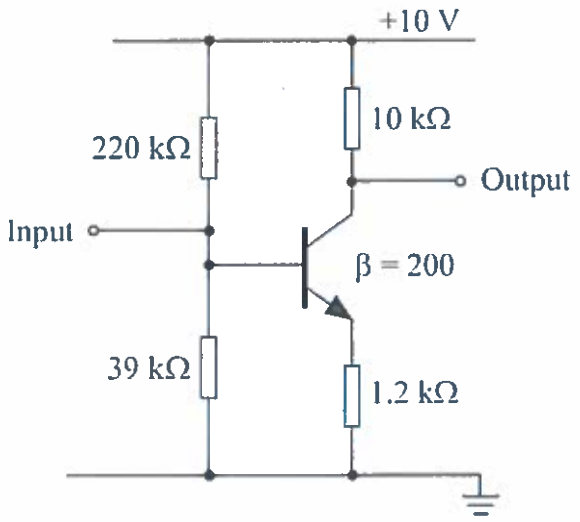

Figure 2.1

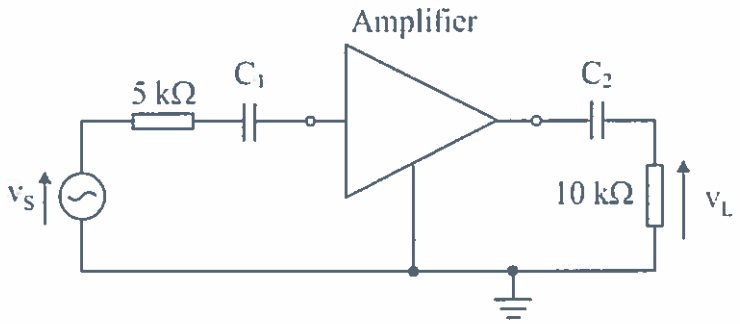

Figure 2.2

3. Figure 3.1 shows a CMOS amplifier in which a p-channel MOSFET acts as an active load for an n-channel MOSFET. The active load is biased by applying a DC voltage V_{BIAS} to the gate.

a) Assuming both transistors are active under quiescent conditions, calculate the value of V_{BIAS} that will give a quiescent drain current of 0.2 mA. Also determine the gate voltage of the lower MOSFET under quiescent conditions. [8]

For the gate voltages you calculated above, calculate the range of output voltages over which both MOSFETs will remain active. Hence calculate the value of R_G that will give a quiescent output voltage at the midpoint of this range. [6]

b) Draw a small-signal equivalent circuit of the amplifier, and hence determine the small-signal voltage gain in the mid-band. Also calculate the small-signal input resistance of the circuit. You should assume the V_{BIAS} and R_G values you calculated in part a). [12]

c) If the upper MOSFET is replaced by a passive load resistor, chosen such that the operating point of the lower MOSFET remains the same, what will be the new value for the small-signal voltage gain? [4]

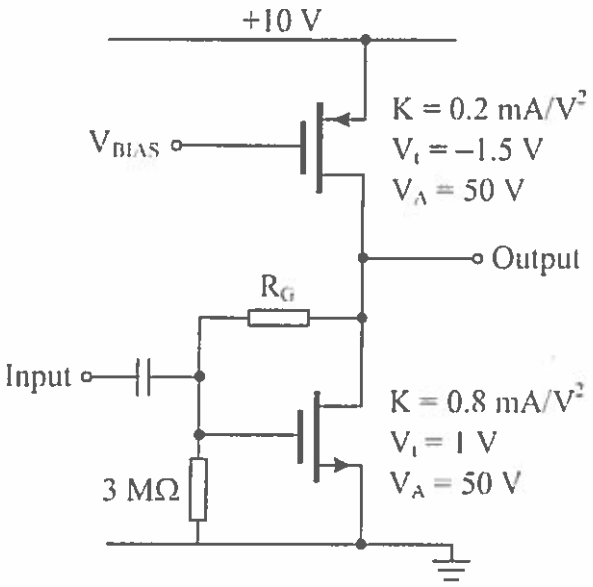

Figure 3.1