UNIVERSITY OF LONDON
IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2002

BEng Honours Degree in Computing Part II
MEng Honours Degrees in Computing Part II
BEng Honours Degree in Information Systems Engineering Part II
MEng Honours Degree in Information Systems Engineering Part II
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER C210=I2.3

ARCHITECTURE II

Tuesday 30 April 2002, 14:30
Duration: 90 minutes
(Reading time 5 minutes)

Answer THREE questions

Paper contains 4 questions
Calculators required

1a Define two's complement number representation. Using inverters and fulladders, provide a diagram of a 4-bit subtractor for numbers in two's complement representation.

b Use a diagram to show how the circuit in Part 1a can be modified to become a 4-bit programmable adder/subtractor. At each cycle when a control input is zero, the circuit performs addition; when the control input is one, the circuit performs subtraction.

c Use a diagram to show how an 8-bit programmable carry-select adder/subtractor can be developed using several 4-bit programmable adder/subtractors described in Part 1b.

d Explain what sign extension means for numbers in unsigned representation and in two's complement representation. Provide circuit diagrams of sign extension circuits for these two number representations.

e Provide a circuit diagram of a sign extension circuit that can deal with both unsigned number representation and two's complement number representation, given that in every cycle a control signal indicates which representation is used.

The five parts carry, respectively, 15%, 10%, 25%, 25% and 25% of the marks.

2a The parallel statement of the Occam language terminates when all its branches have terminated. Provide a diagram of a control circuit using SR-flipflops for implementing the parallel statement in hardware based on the token-passing method. Explain briefly how the circuit works.

b Provide a diagram of an alternative control circuit to the one in Part 2a which involves D flipflops, and-gates, or-gates and an inverter. Explain briefly how the circuit works.

c Provide a diagram of an alternative control circuit to the one in Part 2a that involves a fulladder, when the parallel statement contains only two branches. Explain briefly how the circuit works.

The three parts carry, respectively, 30%, 35% and 35% of the marks.

3a An 8-bit processor P with two registers, R0 and R1, supports the following instructions (note that r is a value specifying R0 or R1; r=0 corresponds to R0 and r=1 corresponds to R1):

operation	bit 7–5	bit 4	bit 3–0	meaning
add	000	r	not used	place the sum of the values in R0 and R1 in the register r
loadc	001	r	c	load the sign-extended constant value c into the register r
load	010	r	c	load the contents of the memory location at the address c into the register r
store	011	r	c	store the contents of the register r into the memory location at the address c
jump	100	r	not used	unconditional jump to the instruction in memory whose address is specified by the register r

Provide a description of the above five instructions using a suitable Register Transfer Language.

b In addition to having two registers, the datapath for P in Part 3a also has a program counter PC, an instruction register IR, an instruction memory IM situated between the PC and IR, an incrementer INC for incrementing the PC, an ALU whose inputs are from R0 and R1, and whose output is connected to the ALUout register. There is a data memory DM with a data input from ALUout and address input from selected bits of IR. There are also a sign-extension circuit SX, and three multiplexers for controlling information flow. The ALU can add its two inputs, or select one of its inputs and pass it to the output.

Provide a diagram showing how these components are connected together to form a multi-cycle datapath for P. The diagram does not need to include the control unit.

c Provide a state diagram showing the appropriate register transfer actions in each state for a control unit controlling the multi-cycle datapath in Part 3b. For example, one of the states may contain the register transfer action IR = IM[PC].

The three parts carry, respectively, 25%, 40% and 35% of the marks.

4a Explain what is meant by n-way set-associative mapping in a memory hierarchy, and how it relates to direct-mapped and fully-associative mapping.

b Explain briefly two methods of implementing fully-associative mapping, such that the first is commonly used for caches while the second is commonly used for virtual memory systems. What are the number of comparisons that needs to be carried out for each of these two methods?

c Explain briefly what a TLB is, and why TLBs are often implemented as fully-associative caches.

d Consider a TLB of size m implemented as an n-way set-associative cache, processing p-bit page addresses. Calculate the total number of bits in this TLB.

The four parts carry, respectively, 15%, 30%, 20% and 35% of the marks.