E3.05
ISE3.19

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2006

EEE/ISE PART III/IV: MEng, BEng and ACGI

Corrected Copy

DIGITAL SYSTEM DESIGN

Wednesday, 3 May 10:00 am

Time allowed: 3:00 hours

There are SEVEN questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung
Second Marker(s) : T.J.W. Clarke

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X[7:0] is an eight bit bus with X7 being the MSB and X0 the LSB.

Hexadecimal numbers are prefixed with '$'. For example the decimal number 10 is written as $A.

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

1. The Huffman variable-length code given in *Figure 1.1* is used to transmit messages composed of symbols from the set (`A, B, C, D, E` and `F`) over a serial link. The signal at the receiver is a continuous stream of bits corresponding to a message composed of symbols from the set. An example of a received signal for the message `EBBA...` is shown in *Figure 1.2*. All signals changes occur just after the rising edge of the clock signal.

   A finite state machine (FSM) depicted in *Figure 1.3* is required to decode the transmitted message from this bit-stream. The circuit must detect the end of each transmitted symbol. In the next clock period, it must produce the fixed-length code on `DATA_OUT` for the symbol according to *Figure 1.1*, and an active high `DATA_VALID` signal at the output as shown in *Figure 1.2*. Assume that a `RESET` pulse is available to reset the circuit just before the first bit of the first symbol is received.

   a) Draw a state diagram of the finite state machine.

   [5 marks]

   b) Assuming the use of "one-hot" state encoding, design the FSM in the form of state transition table and Boolean equations. It is not necessary to minimise these equations.

   [10 marks]

   c) If the FSM is on a Xilinx Virtex-II or an Altera Flex10K FPGA, estimate how many 4-input Logic Elements (LE) or equivalent resources are required.

   [5 marks]

Symbol	Fixed-length Code	Variable-length Code
A	000	00
B	001	01
C	010	10
D	011	110
E	100	1110
F	101	1111

Figure 1.1

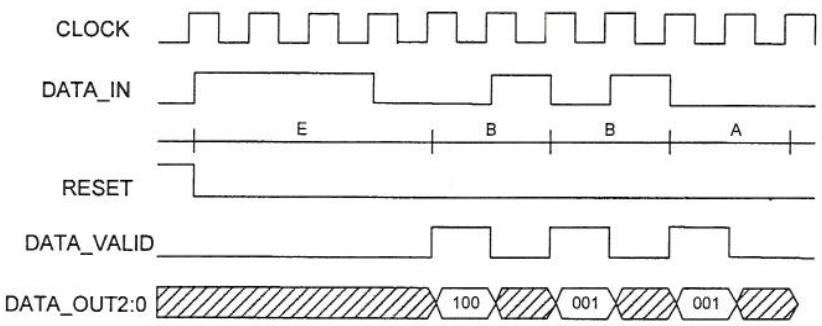

Figure 1.2

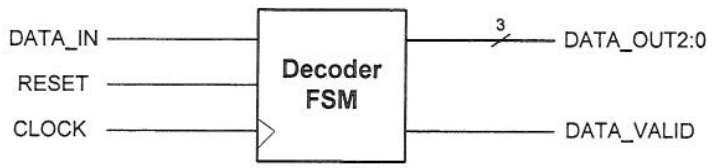

Figure 1.3

2. *Figure 2.1* shows a circuit for calculating the square root of an 8-bit unsigned binary number. The circuit consists of a multiplexer, a register and a 6-bit adder. The register is initially cleared, and then, beginning with the two most significant bits, the 8-bit number is applied, two bits at a time, to `X1:0` and a clock pulse `CLK` is applied to the registers. After four pulses on `CLK`, the desired square root is available on `Y3:0`.

   a) For each of the unsigned numbers `P5:0`, `Q5:0`, `S5:0` and `Y3:0`, write down an algebraic expression giving its value after the next `CLK` pulse in terms of the current values of `P`, `Q`, `S`, `X` and `Y`. You will need to give two expressions in some cases depending on whether the current value of `Y` is odd or even, and on whether or not the future value of `S` is less than 32. Note that `S5` and `Y0` are the same signal.

   [10 marks]

   b) Give the values of `X`, `P`, `Q`, `S` and `Y` after each clock cycle on `CLK` for input numbers i) 16 (00010000) and ii) 172 (10101100).

   [10 marks]

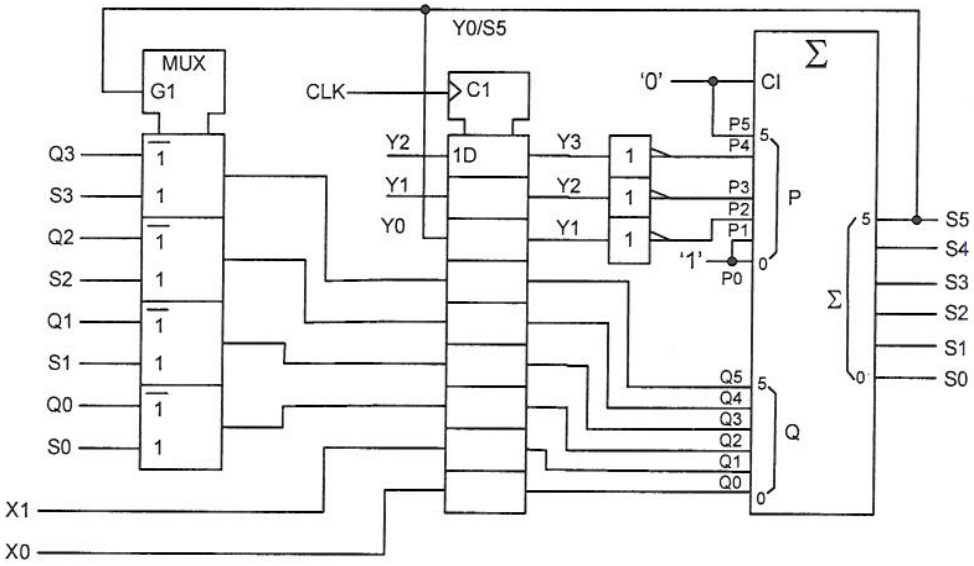

Figure 2.1

3. A Xilinx Virtex-II field programmable gate array (FPGA) contains 18Kbit Block RAMs that can be configured as 1K x 18 bit ROM. The content of one such is given by the equation `65535*sin(π*A/2048)` rounded to the nearest 18-bit signed integer in 2's complement form, where A is the address of the ROM from 0 to 1023.

   a) Design a circuit using this Block RAM and other Configurable Logic Blocks (CLBs) on the FPGA to generate an output Y in 2's complement form, such that:

      `Y = 65535*sin(π*N/2048)`

      where N is an input to the circuit representing an unsigned integer in the range of 0 to 4095 and Y is rounded to the nearest integer. State clearly the width of the datapaths in your design.

      [14 marks]

   b) Explain the factors that limit the operating system clock frequency for your circuit and show how the frequency can be maximized.

      [4 marks]

   c) Demonstrate that your circuit gives the correct answer for input of $C00.

      [2 marks]

4. *Figure 4.1a* depicts a 2K x 16 bit synchronous first-in-first-out (FIFO) memory module that is implemented using a Xilinx Virtex-II FPGA device. All operations are synchronous to a system clock signal `clk`. On the rising edge of `clk`, input data `d_in` is stored in the FIFO if the `put_get` signal is high and output data is read out to `d_out` if `put_get` is low. Data words are read out in the same order that they are stored. If the number of data stored in the FIFO is 2046 or higher, the signal `full` goes high. Similarly if the number of data stored is 2 or less, the signal `empty` goes high. The signal `reset` initializes the FIFO to an empty state. The FIFO is enabled by the `strobe` signal which goes high for one cycle when there is either a read or a write operation. You may assume that circuits external to the FIFO ensure that it never overflows or underflows.

   a) Using counters as address pointers, static RAM and other circuit components, sketch the functional design of this synchronous FIFO. You may use any functional logic blocks such as adders, subtractors and comparators. Do not show any gate level design of your circuits.

   [10 marks]

   b) *Figure 4.1b* depicts a BlockRAM found in Xilinx Virtix-II family of FPGAs. Each Select BlockRAM can be configured as 16K x 1, 8K x 2, 4K x 4, 2K x 9, 1K x 18 or 512 x 36 RAM. The data output can be registered or unregistered depending on how the BlockRAM is configured as shown in Figure 4.1b.

      (i) With the aid of a diagram, explain how you would use multiple BlockRAMs to implement the memory used in the FIFO.

      [2 marks]

      (ii) Estimate with justification the approximate number of slices required to implement the FIFO. Each slice consists of two 4-inputs-1-output lookup tables (LUTs) and two optional registers.

      [4 marks]

      (iii) Explain why one may want to register the output data from the BlockRAM memory as shown in Figure 4.1b.

      [4 marks]

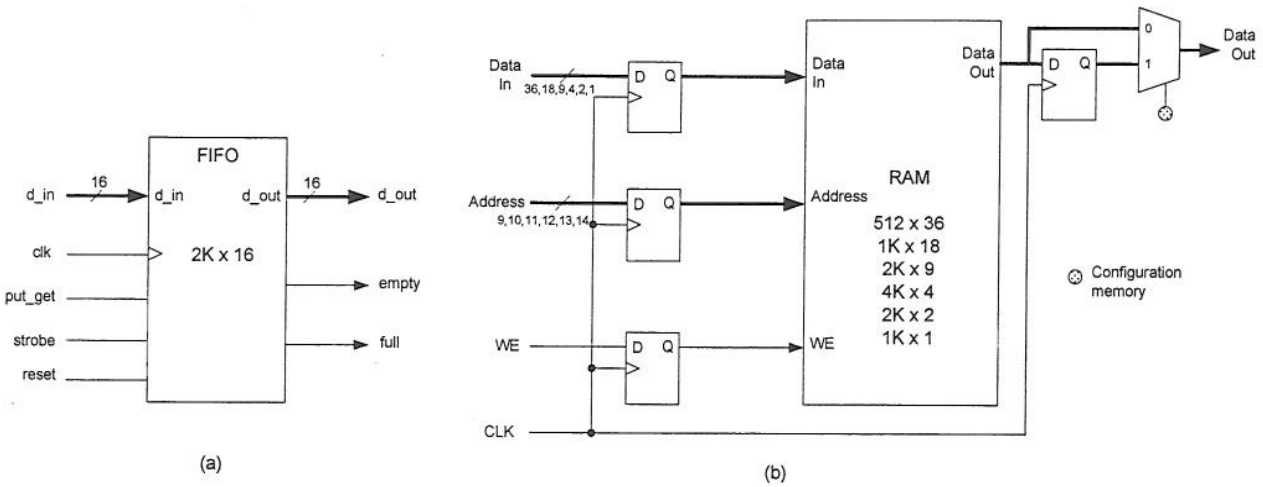

Figure 4.1

5. *Figure 5.1* shows part of the input circuit of a logic analyser. The input signal DIN is sampled at 100MHz and eight successive samples are stored in the shift register. The contents of the shift register are then transferred to a holding register and are written into the memory at an address determined by the counter. The counter is then incremented by 1 in preparation for the storage of the next eight input samples.

   To write a word into the memory, the $\overline{WE}$ input must be taken low for at least 40 ns, and the address must remain constant from 5 ns before the start of the $\overline{WE}$ pulse until 5 ns after it has ended. The data inputs to the memory must remain constant from 12 ns before until 5 ns after the end of the $\overline{WE}$ pulse.

   Design circuitry to generate the three control signals PEN, $\overline{WE}$ and CCK using the 100Mhz signal $CLOCK$ to provide all the timing of the signals. If PEN is high, data will be stored in the holding register at the rising edge of $CLOCK$. You may assume that all gates have a propagation delay of 2 ns and that all counters and registers have a clock-to-output delay of 3 ns, a setup time of 1ns and a hold time of 0 ns.

   [12 marks]

   Draw a timing diagram showing all the important signals in your circuit and verify that the memory timing specifications are satisfied by calculating the values of the time intervals mentioned above.

   [8 marks]

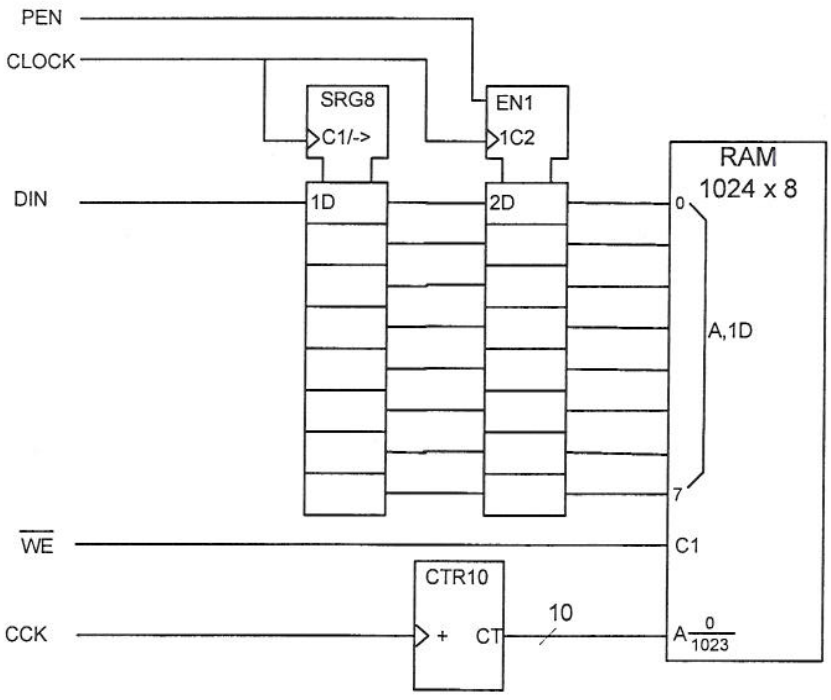

Figure 5.1

6. Figure 6.1 shows the circuit for an 8-bit successive approximation A/D converter. It consists of three components: a voltage comparator, an 8-bit D/A converter and a successive approximation register (SAR). The SAR operates synchronously with the rising edge of *clock*. A conversion sequence begins on the rising edge of clock after the signal *start* goes high. At the same time, the *end_conv* signal should go low indicating that the SAR output *z7:0* is not valid. Then after 8 clock cycles, the converted digital output on *z7:0* becomes valid and the *end_conv* signal returns high.

Figure 6.2 shows a possible implementation of the SAR in which the block marked FSM represents a finite state machine.

a) Design the finite state machine for the SAR either as an ASM chart or as a state transition diagram. State any assumptions regarding the behaviour of the signal *start*.

[12 marks]

b) Draw the timing diagram for the SAR when an input voltage corresponding to a digital value of 10110100 is being converted. Your diagram should show the following signals: *clock, start, comp_out, end_conv, x7:0, y7:0, z7:0*. Values of *x, y* and *z* should be given in hexadecimal form.

[8 marks]

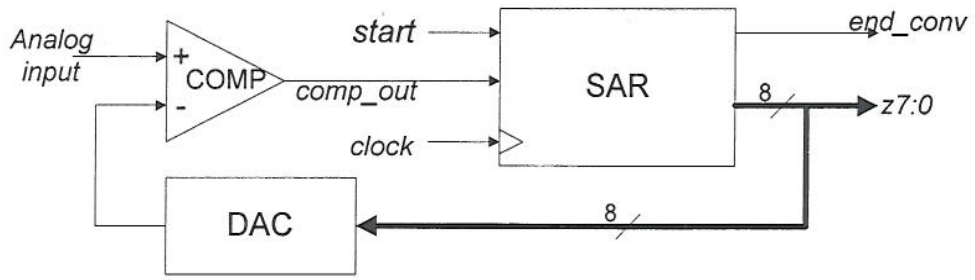

Figure 6.1

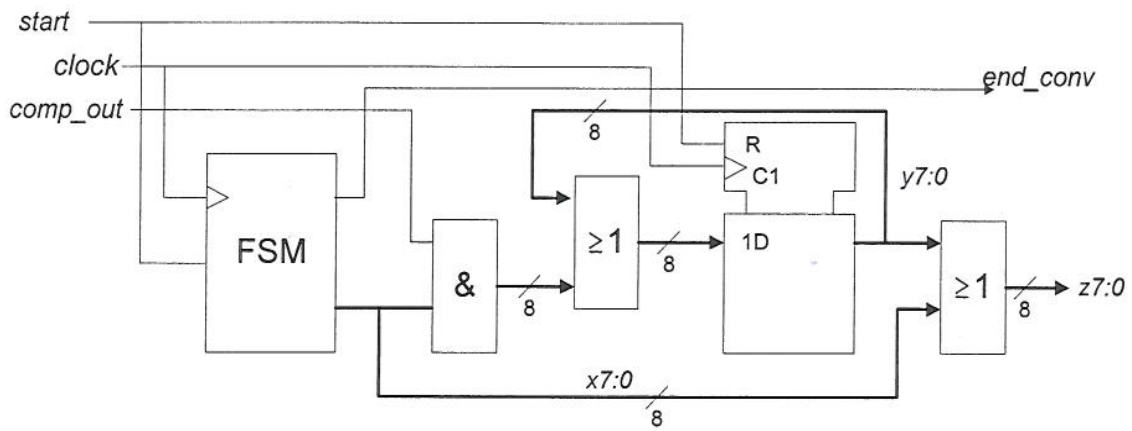

Figure 6.2

7. a) Briefly explain the operating principle of JTAG boundary scan. Discuss why the JTAG boundary scan test standard is important in testing modern electronic systems. Brief explain how a circuit containing JTAG compliant components can be tested for interconnection faults

[4 marks]

b) Explain what is meant by metastability in a digital system and the circumstances under which it can arise. Explain how a circuit can be protected against the effects of metastability.

[4 marks]

c) Explain the cause of ground bounce found in digital circuits. How may ground bounce be reduced?

[4 marks]

d) With the help of a schematic, explain what is a bus-hold circuit. What is the use of such a circuit?

[4 marks]

e) Single bit error correction is required for a 16-bit memory system. If Hamming error correction codes are used, how many check bits are needed for each 16-bit word?

[4 marks]

[END]

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IMPERIAL COLLEGE OF SCIENCE TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
M.Eng., B.Eng., B.Sc(Eng.) and A.C.G.I. EXAMINATIONS 2006

PART III and PART IV

DIGITAL SYSTEM DESIGN

SOLUTIONS

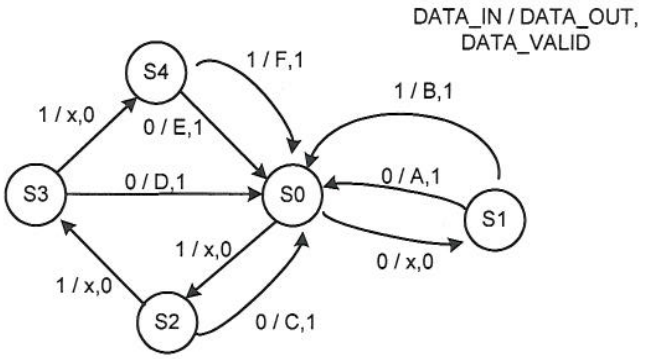
First Marker: *Peter Y. K. Cheung*

Second Marker: *Thomas Clarke*

Answer to Question 1

This question tests students' understanding of FSM design, one-hot state encoding and basic FPGA architectures.

(a)



[5 marks]

(b) State Assignment: use one-hot encoding

State Transition Table:

s4	s3	s2	s1	s0	data_in	n4	n3	n2	n1	n0	data_out	data_valid
0	0	0	0	0	x	0	0	0	0	1	xxx	0
0	0	0	0	1	0	0	0	0	1	0	xxx	0
0	0	0	0	1	1	0	0	1	0	0	xxx	0
0	0	0	1	0	0	0	0	0	0	1	000	1
0	0	0	1	0	1	0	0	0	0	1	001	1
0	0	1	0	0	0	0	0	0	0	1	010	1
0	0	1	0	0	1	0	1	0	0	0	xxx	0
0	1	0	0	0	0	0	0	0	0	1	011	1
0	1	0	0	0	1	1	0	0	0	0	xxx	0
1	0	0	0	0	0	0	0	0	0	1	100	1
1	0	0	0	0	1	0	0	0	0	1	101	1

n0 = !s4!s3!s2!s1!s0 + s1 + s2 !data_in + s3 !data_in + s4 (deduct marks for not catching all 0 case)

n1 = s0 !data_in

n2 = s0 data_in

n3 = s2 data_in

n4 = s3 data_in

d2 = s4

d1 = s2 !data_in + s3 !data_in

d0 = s1 data_in + s3 !data_in + s4 data_in

data_valid = s1 + s2 !data_in + s3 !data_in + s4

[10 marks]

(c) All equations except n0 and data_valid requires less than 4 inputs, therefore can be implement in 1 LUT, n0 and data_valid require 2 LUTs. Therefore total LUTs used = 11.

[5 marks]

Answer to Question 2

This question tests students' ability to analyse a reasonably complicated digital circuit for complex arithmetic operation.

a)

$$
\begin{aligned}
Q'(\text{next}) &= (4Q + X) \bmod 64 \quad \text{if } S < 32 \\
&= (4S + X) \bmod 64 \quad \text{if } S \geq 32 \\
P'(\text{next}) &= 31 - 4Y \\
S'(\text{next}) &= P' + Q' \\
Y'(\text{next}) &= 2Y \quad \text{if } S' < 32 \\
&= 2Y + 1 \quad \text{if } S' \geq 32
\end{aligned}
$$

The remainder after 4 clock cycles is Q if Y is even or S-32 if Y is odd. (Not expected or required in answer from students.)

In order to work these algebraic equations out, students could substitute a few values into the circuit and then assert a clock cycle and work out what happens.

(b)

For X = 16 (00010000):

After Clk cycle	X	P	Q	S	Y
0	0	-	0	-	0
1	1	31	0	31	0
2	0	31	1	32	1
3	0	27	0	27	2
4	-	23	0	23	**4**

[10 marks]

For X = 172 (10101100):

After Clk cycle	X	P	Q	S	Y
0	2	-	0	-	0
1	2	31	2	33	1
2	3	27	6	33	3
3	0	19	7	26	6
4	-	7	28	35	**13**

[10 marks]

Answer to Question 3

This question tests students' ability to apply a modern FPGA using its logic and memory to evaluate a sine function.

a)

The Block RAM in 1K x 18 bit configuration stores ¼ cycle of a sine table such that:

$$Mem[K] = 65535 * \sin(\pi * K / 2048) \text{ for } K = 0 \text{ to } 1023.$$

[2 marks]

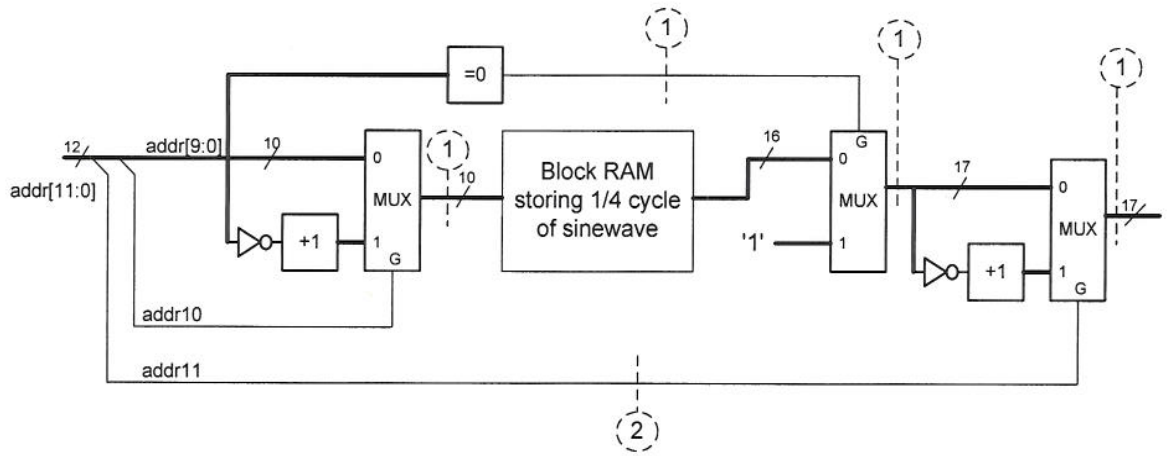
Generate the other quadrants by manipulating the address and negating the ROM/RAM values. The rule to generate the ROM address 'reflection' and amplitude negation are:-

Addr11	Addr10	Address to ROM	Negation
0	0	addr[9:0]	No
0	1	2048 – addr[9:0]	No
1	0	addr[9:0]	Yes
1	1	2048 – addr[7:0]	Yes

[4 marks]

This works except for N=1024 and 3072 when addr[9:0] = 0. Therefore, detect this condition and force output to either +65535 or –65535.

[2 marks]



[6 marks]

To maximize the clock frequency that this module can work under, insert pipelines at vertical lines as shown. Shown in circles are the numbers of pipeline stages required.

[4 marks]

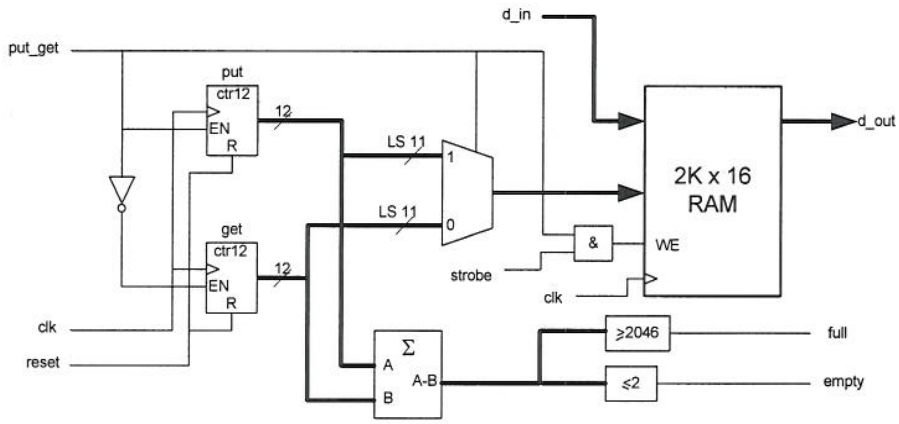
When N = $C00, ROM output not selected. Addr11 = 1, therefore output jammed to –65535.

[2 marks]

Answer to Question 4

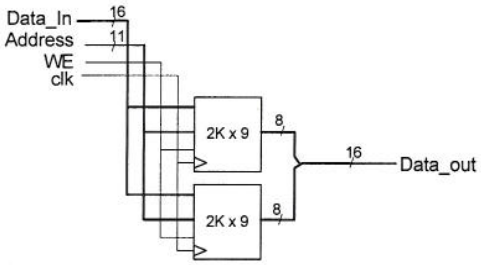
This question tests students' ability to design a reasonably complex circuit module.

a)



[10]

b) (i)



[2]

(ii)

Component	Resources
Memory	2 BlockRAMs
Put Counter	6 slices
Get Counter	6 slices
Subtractor	6 slices
MUX	5.5 slices
<= 2 circuit	1.5 slices
>=2046 circuit	1.5 slices
AND gate, inverter	1 slice
Total	**2 BlockRAMs, 27.5 slices**

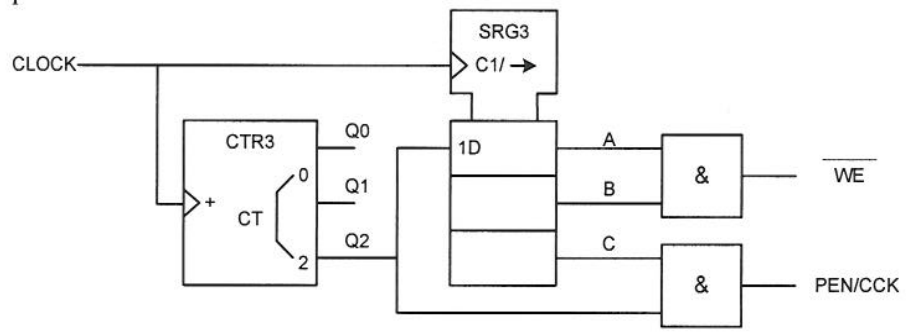
[4]

(iii) With a register at the output, data will be available for reading from the FIFO all through the next FIFO read operation. This provides far better flexibility in the read time available for external circuits and more predictable timing (since it is relative to a clock edge).

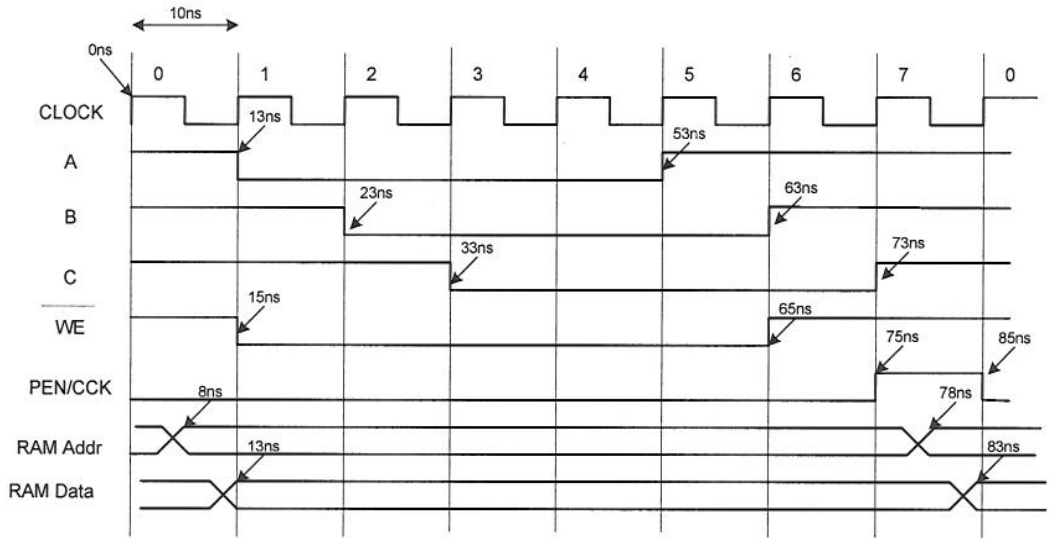
[4]

Answer to Question 5

This question tests students' ability to design a circuit to do a job, and verify that the timing specifications are met.



[12 marks]



[5 marks]

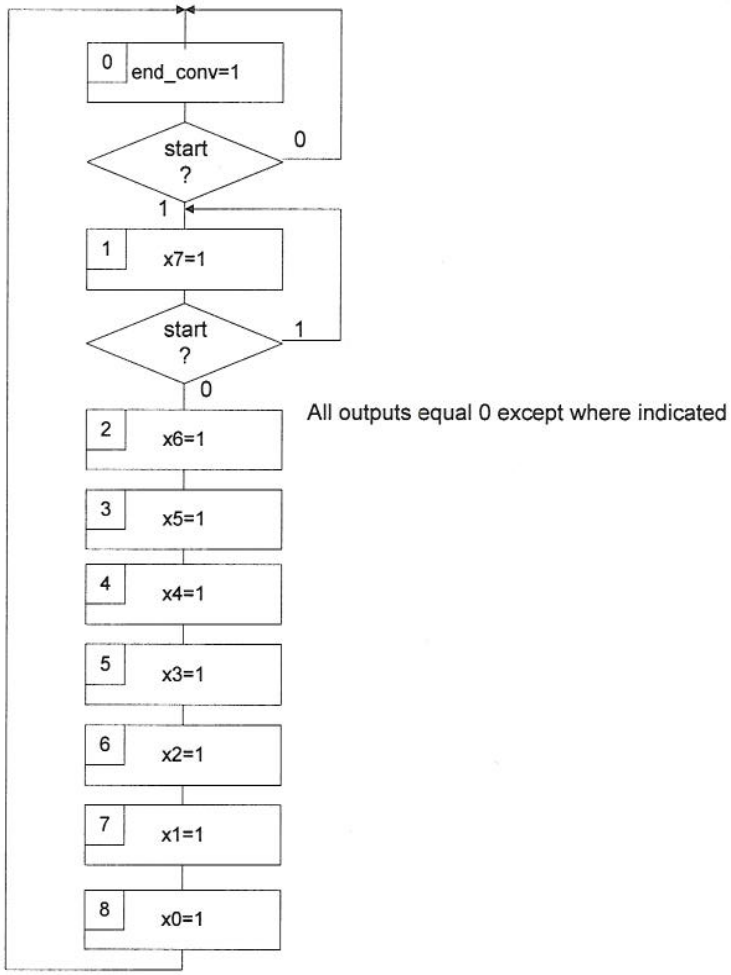
Timing for signal	Specification (ns)	Actual (ns)
/WE pulse length	≥40	50
ADDR setup	≥5	7
ADDR hold	≥5	13
Data setup	≥12	52
Data hold	≥5	18

[3 marks]

Answer to Question 6

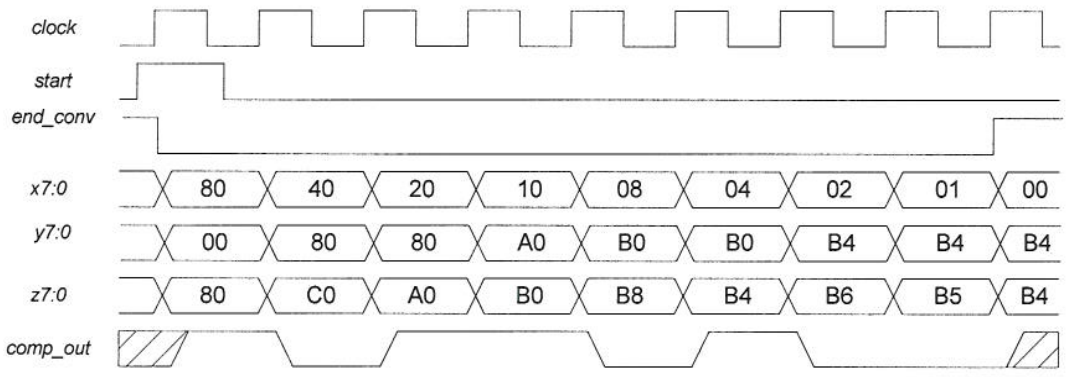
This question tests students' ability to analyse a FSM and the circuits that the FSM controls, drawing of timing diagrams etc.

a)



[12 marks]

b)



[8 marks]

Answer to Question 7

This is question is mostly based on book work and knowledge, rather than based on design/analysis.

a) Modern electronic systems have high density PCB with surface mount components. Impossible to get at any pins of devices. Therefore testing becomes very difficult if not impossible. JTAG boundary scan provides a means of accessing both the internal circuits on components as well as external circuit outside the components.

Students should explain how JTAG actually work.

JTAG test configuration includes EXTEST for testing external devices. Test patterns can be strobed serially into the JTAG compliant device to drive external interconnect to 1 or 0. Another JTAG compliant device would act as 'receiver' and parallel load the pattern. This is then strobed out and compare to expected pattern.

[4 marks]

b) Metastability can occur in any synchronous system interfacing to one or more asynchronous input. Since the input signal is not synchronised to the system clock, it may violate the setup or hold time of the synchronous system. Metastability may be reduced by a synchronizer circuit using one or more D-FF connected in series.

[4 marks]

c) Cause of ground bounce:

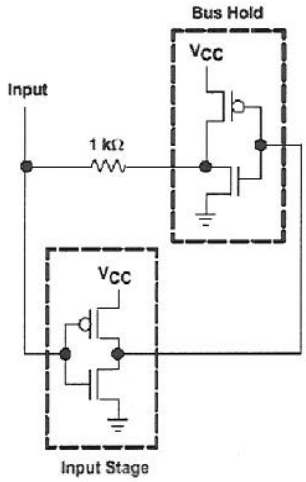
- Ground Bounce is a voltage oscillation between the ground pin on a component package and the ground reference level on the component die.
- Ground Bounce is one of the primary causes of false switching in high speed components and is a major cause of poor signal quality.
- It is caused by a current surge passing through the lead inductance of the package.
- The effect is most pronounced when all outputs switch simultaneously, (hence the alternate name, Simultaneous Switching Noise).
- While the inductance is the combined effect of the package lead, the package lead frame, the bond wire and the inductance in the die pad, most of the inductance is caused by the bond wire.

Ground Bounce effect can be reduced by:

1. Using all Vcc/Gnd pins available
2. Avoid pullup/pulldown resistors (i.e. use bus hold circuit)
3. Possibly use series damping resistors
4. Control output slew rate
5. Extra care in holding clock signals to solid voltage level (Vh) and fast clock transistions

[4 marks]

d) The schematic for a bus-hold circuit is:



- Bus-hold circuits are used to help solve the floating-input problem and eliminate the need for pullup and pulldown resistors.
- Bus-hold circuits consist of two back-to-back inverters with the output fed back to the input through a resistor.
- To understand how the bus-hold circuit operates, assume that an active driver has switched the line to a high level. This results in no current flowing through the feedback circuit.
- Now, the driver goes to the high-impedance state and the bus-hold circuit holds the high level through the feedback resistor.
- The current requirement of the bus-hold circuit is determined only by the leakage current of the circuit.
- The same condition applies when the bus is in the low state and then goes inactive.

[4 marks]

e)

N check bits can check 2^N - N -1 data bits. Therefore we need 5 check bits.

[4 marks]

[END]