E4.17
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IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2009

MSc and EEE PART IV: MEng and ACGI

Corrected Copy

HIGH PERFORMANCE ANALOGUE ELECTRONICS

Thursday, 30 April 2:30 pm

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s) :	E. Rodriguez-Villegas
	Second Marker(s) :	C. Papavassiliou

The Questions

1.

(a) The following two signals are connected to two inputs of an ideal mixer:

$$V_1 = A_1 sin(w_1 t),\ V_2 = A_2 sin(w_2 t)$$

where $w_1 > w_2$. Sketch the frequency spectrum of the signals produced at the output of the mixer. Only positive frequencies are required.

[4]

(b) Sketch the frequency spectrum of the signal at the output of a mixer assuming that:

- One of the inputs of the mixer, V_1, can be any band limited signal with bandwidth BW and centre frequency w_c;
- The second input is:

$$V_2 = A_2 sin(w_2 t), \qquad w_2 >> w_c ;$$

- The mixer is not ideal, that is, its output is given as:

$$V_{out} = V_1 V_2 + V_2^2$$

[4]

(c) Explain how you would recover the signal V_1 from the output of the mixer in (b).

[4]

(d) Give an example of an electronic system where a mixer is a fundamental block and explain why it is important in such a system.

[4]

(e) In the system you described in (d) explain which performance related parameter (specification) would be degraded by having a non-ideal mixer such as the one described in Question 1 (b).

[4]

2. For the circuit in Figure 2.1:

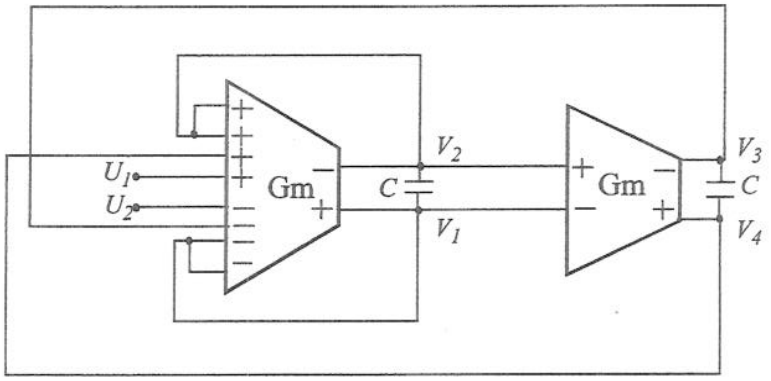

Figure 2.1

(a) Find the transfer functions $\frac{(V_1 - V_2)}{(U_1 - U_2)}$ and $\frac{(V_3 - V_4)}{(U_1 - U_2)}$ in the Laplace domain. What kind of systems do these transfer functions correspond to?

[5]

(b) How would you implement the same functionality if only capacitors (of any value) and transconductors like the one in Figure 2.2 are available? Draw the circuit.

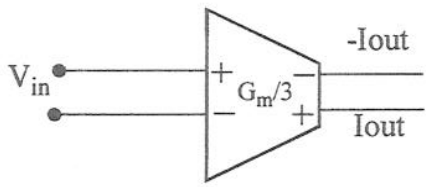

Figure 2.2

[5]

(c) Draw at the transistor level the schematic of a transconductor you could use to implement the system in (b) which meets the following specifications:

- At least one of the transistors is operating in the strong inversion ohmic region (indicate which one).
- The input is the largest impedance node you have in your circuit
- Internal feedback is used to improve linearity

[5]

(d) Draw at the transistor level the schematic of a transconductor you could use to implement the system in (b) which meets the following specifications:

- All transistors are MOS devices operating in the strong inversion saturation region.
- The value of the transconductance can be changed by changing voltages in source terminals.

[5]

3. For the circuit in Figure 3.1, where the input is Vd:

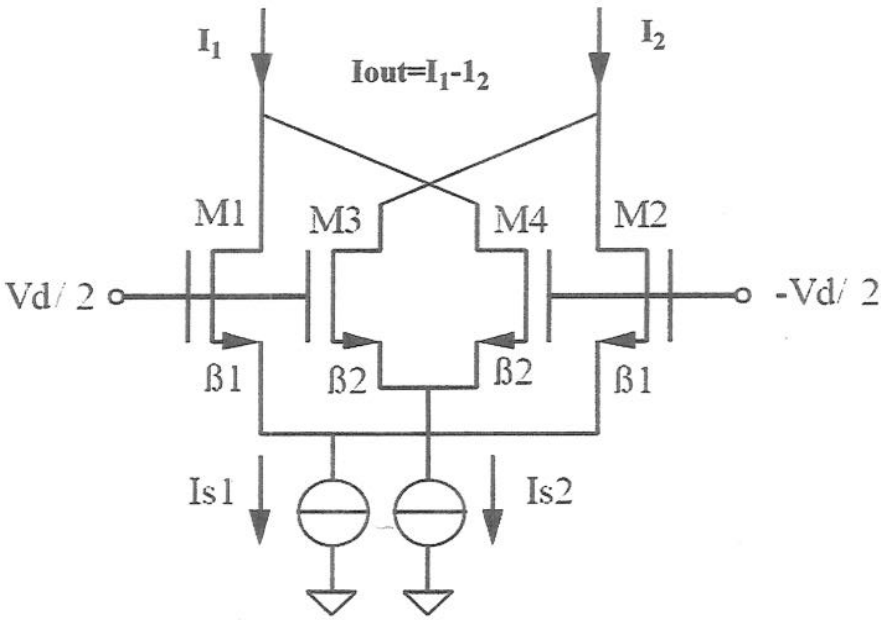

Figure 3.1

(a) Derive the relationship between the bias currents, I_{S1}, I_{S2} and the β parameters that would result in third order harmonic cancellation in I_{out} and hence in optimum performance in terms of linearity.

[5]

(b) List two disadvantages of the circuit in Figure 3.1 versus the conventional differential pair.

[5]

(c) What is the name of the circuit configuration you would use to design an LC ladder if only capacitors and differential transconductors, such as the one in Figure 3.1, are available? Using the symbol of a differential transconductor, draw the schematic of the circuit configuration you are describing.

[5]

(d) For the circuit configuration described in (c), what value would you have to choose for your transconductances if you only have 1pF capacitances and the equivalent inductance has to be 1pH?

[5]

4.

(a) Name all the noise sources in an n-channel MOS transistor assuming perfect gate insulation. Write expressions for the power spectral density of each noise source assuming the FET is in the strong inversion saturation region.

[2]

(b) Draw a small signal model for an n-channel MOS transistor incorporating all the noise sources you identified in (a). Derive an expression for the equivalent power spectral density of noise at the gate of the transistor.

[3]

(c) Derive an expression for the noise power spectral density at the input terminal (V_{in}) of the circuit in Figure 4.1 (a). You can ignore parasitic capacitances.

[3]

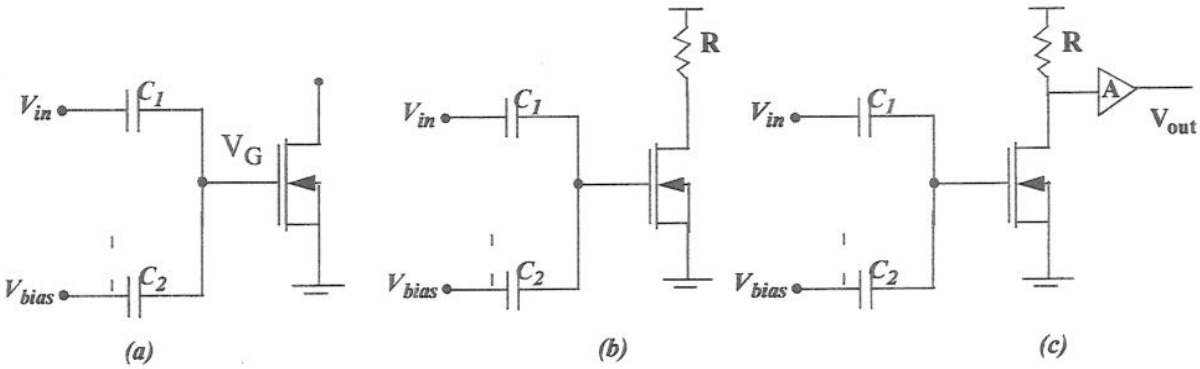

Figure 4.1

(d) Find an expression for the noise power spectral density at the input terminal (V_{in}) of the circuit in Figure 4.1 (b).

[4]

(e) Find an expression for the noise power spectral density at the input terminal (V_{in}) of the circuit in Figure 4.1 (c). Assume that the amplifier has an equivalent noise power spectral density referred to its input equal to N_A (V^2/Hz) and a voltage gain A.

[4]

(f) If the input referred noise of the circuit in Figure 4.1 (a) is 1uV/Hz and the noise of the amplifier referred to its own input is 2uV/Hz, what would be the total noise at the output of the circuit in Figure 4.1 (c) assuming that the gain of the circuit in Figure 4.1 (b) is 10, the gain of the amplifier is 5, and the bandwidth of interest is 10Hz.

[4]

5. Given the LC ladder in Figure 5.1.

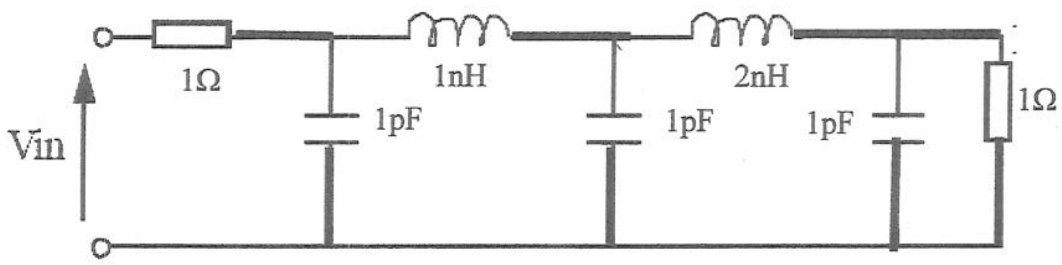

Figure 5.1

(a) Find the ladder state space equations.

[5]

(b) Draw a signal flow graph for the circuit in Figure 5.1 implementing the state space equations you derived in (a).

[10]

(c) Sketch an active implementation for the LC-ladder in Figure 5.1 assuming ideal lossless integrators are available.

[5]

6. Figure 6.1 shows the schematic and equivalent symbol of a p-channel FGMOS transistor. Ignoring parasitic effects and assuming that the capacitors connected to the floating gate have value C_i (for $i=[1,N]$), the voltage at the floating gate is given by:

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i$$

where C_T is approximately the sum of all the input capacitances connected to the floating gate.

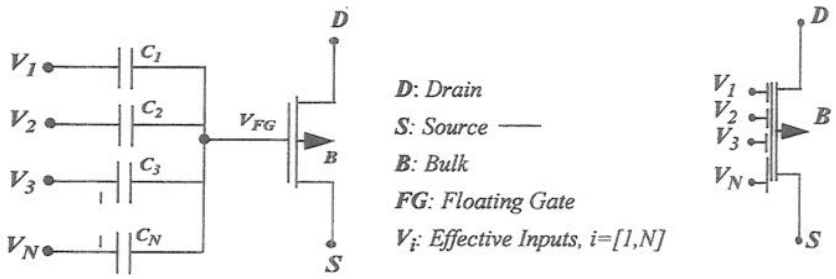

Figure 6.1

Neglecting second order effects, the current in a p-channel FGMOS transistor in strong inversion saturation region is given by:

$$I \approx \beta \left(V_S - \sum_{i=1}^{N} \frac{C_i}{C_T} V_i - |V_T| \right)^2$$

where all the parameters have their usual meaning.

(a) Derive an expression for the large signal output current, I_{out}, of the circuit in Figure 6.2 as a function of β, $(V_{i+}-V_{i-})$ and I_s, given:

- All the input capacitances have the same value: $C_{in}=0.5C_T$.
- All the transistors are identical, with equal values of β and V_T.

[5]

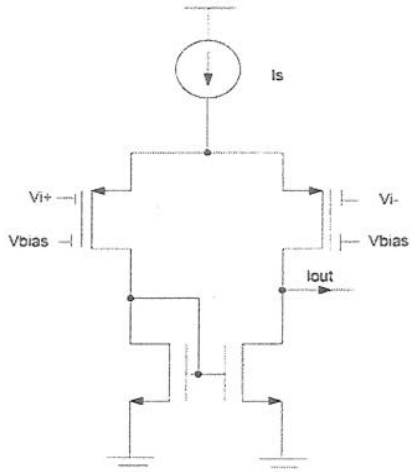

Figure 6.2

(b) Without doing any extra calculation explain how you could derive the expression for the output current of a differential pair with normal p-channel MOS transistors at the input instead.

[4]

(c) Derive an expression for the small signal transconductance of the circuit in Figure 6.2.

[3]

(d) What is the relationship between the transconductance value you obtained in (c) and the transconductance of a differential pair built with MOS devices? By what factor would you need to increase the biasing current in the circuit in Figure 6.2, with respect to the biasing current in a MOS differential pair, to obtain the same transconductance value?

[3]

(e) List two disadvantages of the circuit in Figure 6.2 when compared with a normal MOS differential pair.

[3]

(f) List one advantage of the circuit in Figure 6.2 when compared with a normal MOS differential pair.

[2]

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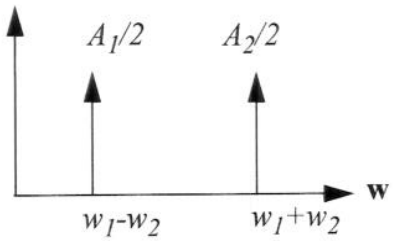
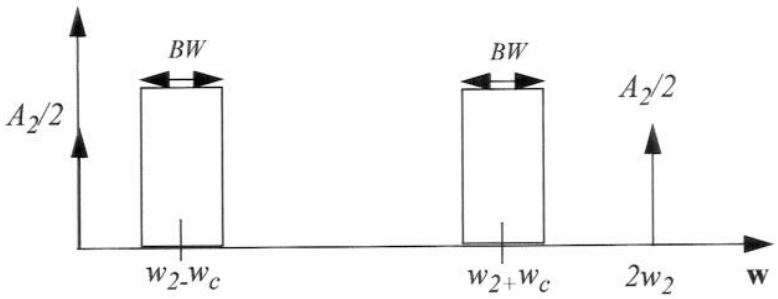
1.

(a) (Application of theory. New computed example)



(b) (Application of theory. New computed example)



(c) (Application of theory)

First use a low pass filter with a cut-off frequency $w_2+w_c>w_o> w_2-w_c$ (the closest to w_2-w_c the better). Then use another mixer having the output of the filter as one of the inputs and V2 as the other. Then use another low pass filter with cutoff frequency $w_c<w_o<2w_2-w_c$.

(d) (Theory)

A mixer is a fundamental block in a receiver. The reason is that if we are trying to select one particular frequency channel from the complete RF spectrum, then we need a bandpass filter to reject any unwanted frequencies. Generally this filter has to be narrowband, and high Q filters are difficult to

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design at high frequencies. This problem is compounded if the input signal frequency is variable (i.e. the signal is transmitted in one of a number of possible channels, each with the same bandwidth). A tuneable, high Q bandpass filter with constant bandwidth is now required.

The solution is to use a superhet receiver (supersonic heterodyne). This system downconverts the input signal to an intermediate frequency (IF), and a bandpass IF filter is then used to select the wanted signal. The design of the bandpass IF filter is eased since it doesn't have to be tuneable, and the IF centre frequency is much lower than the input RF signal.

The downconversion is performed by 'mixing' (multiplying) the RF input signal (fRF) with a local oscillator signal (fLO), such that the resulting output is at the required IF frequency (fIF).

Received RF signal = 2Acos[(fRF)t *Local oscillator signal LO = cos(fLO)t*

Mixer output = 2A cos(fLO)t cos[(fRF)t] = Acos[(fLO - fRF)t] + Acos[(fLO + fRF) t]
i.e. sum and difference components

The sum components are at a very high frequency and are removed by filtering. The difference frequency component is a replica of the RF component in terms of amplitude and phase, but is shifted down to an intermediate frequency (IF):
fIF = fLO - fRF

The oscillator frequency fLO is often tuneable to ensure that a range of input RF frequencies can be selected.

(e) (Application of theory)

The spurious response rejection

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2.

(a) (New computed example. Application of theory)

The state space equations for the circuit are:

$$\dot{x_1} = -2k_o x_1 - k_o x_2 + k_o u$$

$$\dot{x_2} = k_o x_1$$

where $x_1 = (V_1 - V_2)$, $x_2 = (V_3 - V_4)$, and $u = (U_1 - U_2)$ and $k_o = G_m/C$. Applying Laplace transform to the state space equations.

$$X_2(s) = \frac{k_o^2}{s^2 + 2k_o s + k_o^2} U(s) \text{ Lowpass filter}$$

$$X_1(s) = \frac{sk_o}{s^2 + 2k_o s + k_o^2} U(s) \text{ Bandpass filter}$$

(b) (Application of theory)

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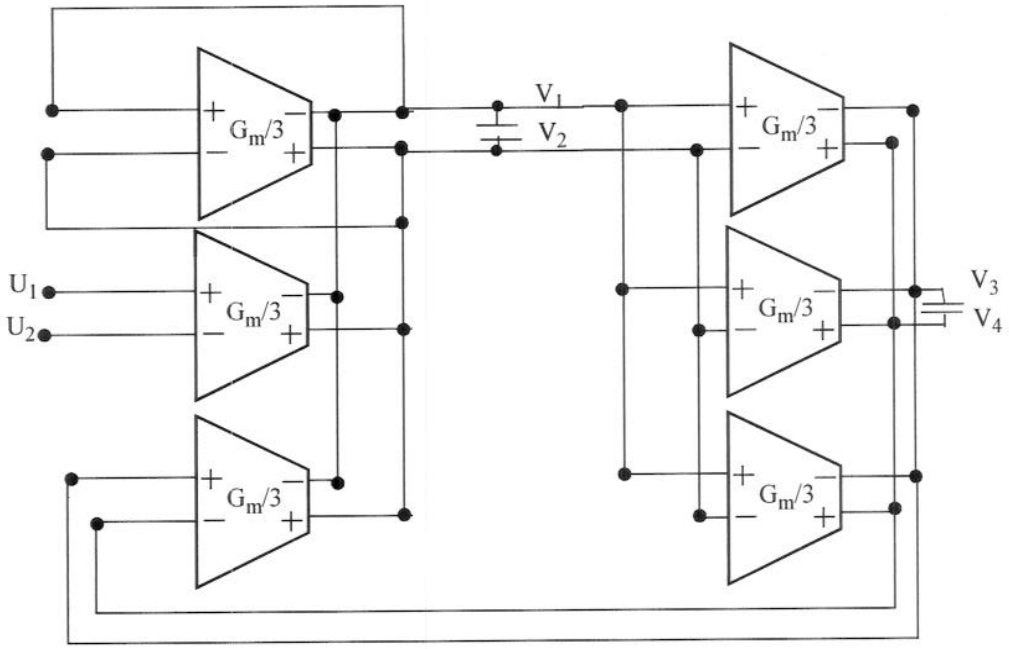
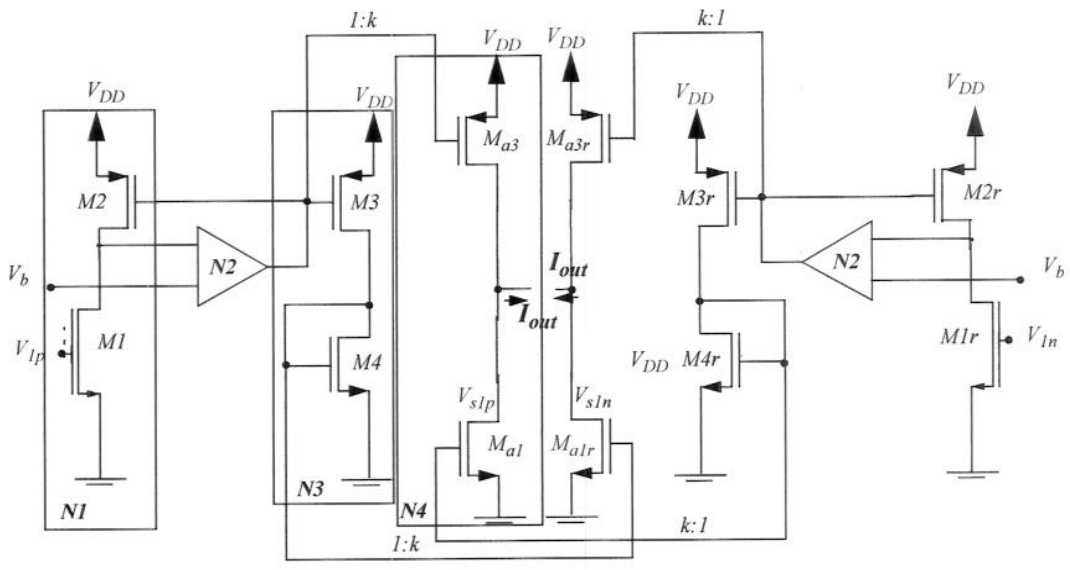


(c) (Application of theory)

The input transistor can be a MOS device operating in the strong inversion ohmic region. Feedback is used to keep the value of V_{DS} constant and hence linearity. An example could be:



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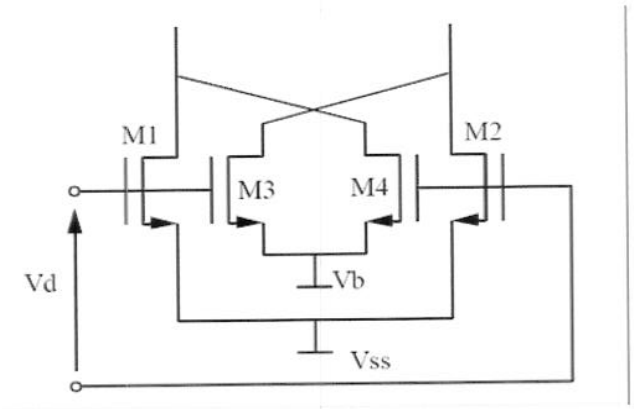
(d) (Application of theory)

The transconductor below with differential input Vin=Vd, and tuning voltages Vb and Vss meets the required characteristics.



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3.

(a) (Theory)

For a single transistor:

$$Id = Ido + \left(\frac{\partial Ic}{\partial Vin}\right)Vin + \left(\frac{\partial^2 Id}{\partial Vin^2}\right)\frac{Vin^2}{2} + \left(\frac{\partial^3 Id}{\partial Vin^3}\right)\frac{Vin^3}{6} + \ldots\ldots$$

where the derivatives are evaluated at the quiescent point Id = Ido

For the circuit above:

$$Iout = (Id1 - Id2) - (Id3 - Id4)$$

Thus $$Iout = \frac{Vd}{2}\left(\left(\frac{\partial Id}{\partial Vd}\right)_1 + \left(\frac{\partial Id}{\partial Vd}\right)_2 - \left(\frac{\partial Id}{\partial Vd}\right)_3 - \left(\frac{\partial Id}{\partial Vd}\right)_4\right)$$

$$+ \quad \frac{Vd}{48}\left(\left(\frac{\partial^3 Id}{\partial Vd_3}\right)_1 + \left(\frac{\partial^3 Id}{\partial Vd^3}\right)_2 - \left(\frac{\partial^3 Id}{\partial Vd^3}\right)_3 - \left(\frac{\partial^3 Id}{\partial Vd^3}\right)_4\right)$$

where $\left(\frac{\partial^n Id}{\partial Vd^n}\right)_m$ is the n^{th} derivative of the m^{th} transistor

Since M1 and M2 are matched, and M3 and M4 are matched, then

$$\left(\frac{\partial^n Id}{\partial Vd^n}\right)_1 = \left(\frac{\partial^n Id}{\partial Vd^n}\right)_2 \text{ and } \left(\frac{\partial^n Id}{\partial Vd^n}\right)_3 = \left(\frac{\partial^n Id}{\partial Vd^n}\right)_4$$

To eliminate the third harmonic term, the transistors should be scaled appropriately so that $\left(\frac{\partial^3 Id}{\partial Vd^3}\right)_1 = \left(\frac{\partial^3 Id}{\partial Vd^3}\right)_3$ however we must ensure that $\left(\frac{\partial Id}{\partial Vd}\right)_1$ and $\left(\frac{\partial Id}{\partial Vd}\right)_3$ don't also cancel.

First order derivative $\frac{\partial Id}{\partial Vd} = \sqrt{\beta Is}$ Third order derivative $\frac{\partial^3 Id}{\partial Vd^3} = \sqrt{\beta^3 / 8Is}$

For cancellation of the third order coefficients:

$$(\beta 1/\beta 2)^{3/2} = \sqrt{(Is1/Is2)} \qquad \text{thus} \qquad \frac{(W1/L1)^3}{(W2/L2)^3} = \frac{Is1}{Is2}$$

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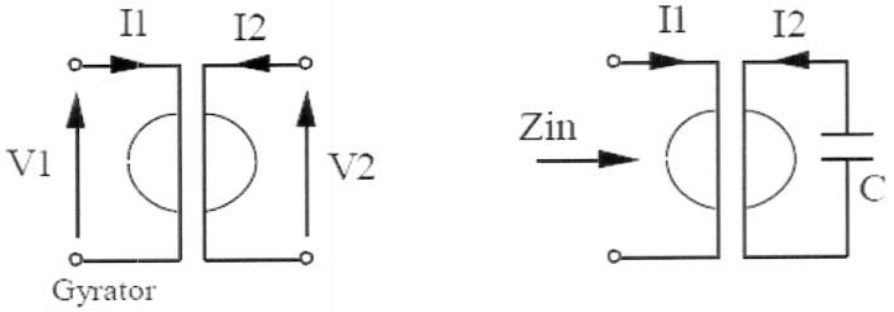
(b) (Application of theory)

The transconductance is reduced for the same power consumption and the area is larger

(c) (Application of theory)

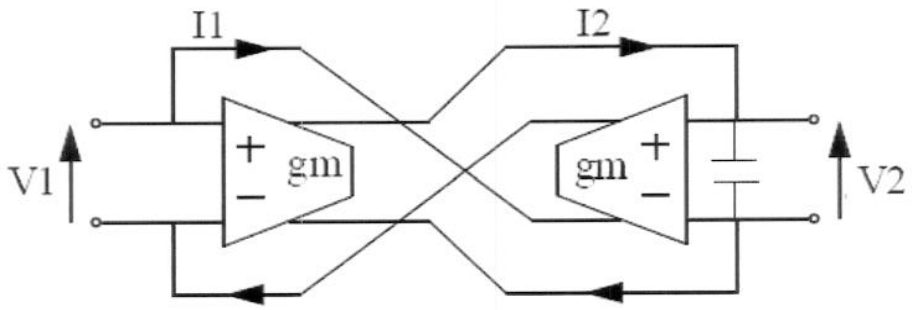
A gyrator configuration, this is:



$I1 = G\,V2 \qquad I2 = -G\,V1$
(G = 'gyration conductance')

To simulate an inductor, connect a capacitor across port 2:

$$V1 = -\frac{I2}{G} = \frac{C}{G}\frac{dV2}{dt} = \left(\frac{C}{G^2}\right)\frac{dI1}{dt} = L\frac{dI1}{dt}$$



(d) (Application of theory. Computed example)
Following from the last equation in (c), 1S.

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4.

(a) (Theory)

Thermal noise due to the resistance of the channel:

$$ind^2 = \frac{8kTgm\Delta f}{3} A^2$$

This noise source can also be represented by an equivalent channel resistance rd = 3/2gm.

Flicker (1/f) noise in series with the gate:

$$vng^2 = \frac{k_f \Delta f}{CoxWLf} V^2$$

kf is a flicker noise coefficient which is process dependent.

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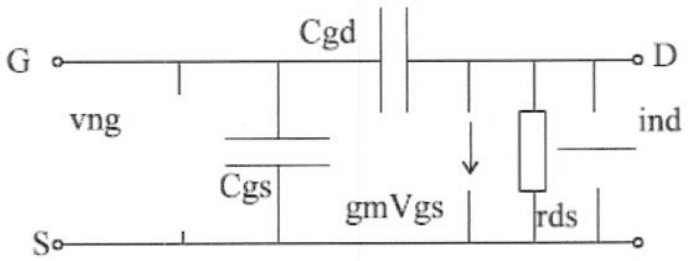
(b) (Theory)



And the equivalent noise at the input can be obtained transfering *ind* back, dividing by the square of the transconductance, this is:

$$vn^2 = \frac{ind^2}{gm^2} + vng^2 = \frac{8kT}{3gm} + \frac{k_f}{WLCox\,f}$$

(c) (Application of theory)

The noise at the input of that circuit can be obtained dividing the equivalent noise at the input of the MOS transistor (obtained in (b)) by the square value of the gain from the input to the gate. Since the parasitic capacitances have been ignored and there is no current through the gate, that gain can be obtained simply by inspection and it is given by:

$$\frac{V_G}{V_{in}} = \frac{C_1}{C_1 + C_2}$$

Then the power spectral density at the input is:

$$v_n^2\left(\frac{C_1 + C_2}{C_1}\right)^2$$

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(d) (Application of theory)

The noise can be obtained adding the equivalent thermal noise of the resistor at the input of the circuit to the equation obtained in (c). The former is given by the thermal noise of the resistor, divided by the square value of the gain from V_{in} to the drain of the transistor. Hence the noise is given by:

$$v_n^2\left(\frac{C_1+C_2}{C_1}\right)^2+\frac{4kTR}{g_m^2}\left(g_{ds}+\frac{1}{R}\right)^2\left(\frac{C_1+C_2}{C_1}\right)^2$$

(e) (Application of theory)

The equivalent noise given for the amplifier is at the same node as the thermal noise of the resistor, therefore:

$$v_n^2\left(\frac{C_1+C_2}{C_1}\right)^2+\frac{(4kTR+N_A)}{g_m^2}\left(g_{ds}+\frac{1}{R}\right)^2$$

(f) (Application of theory)

Transfering the noise from the first stage to the output and integrating over the bandwidth results in 500uV, and for the second stage 100uV. Hence the total noise is 600uV.

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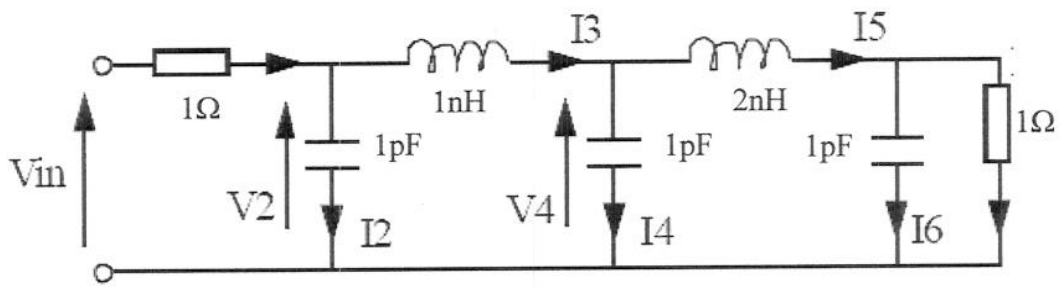
5.

(a) (Application of theory. New computed example)



$$V1 = Vin - V2 \qquad I2 = I1 - I3 \qquad V3 = V2 - V4$$

$$I1 = V1 \qquad V2 = I2/10^{-12}s \qquad I3 = V3/(10^{-9}s)$$

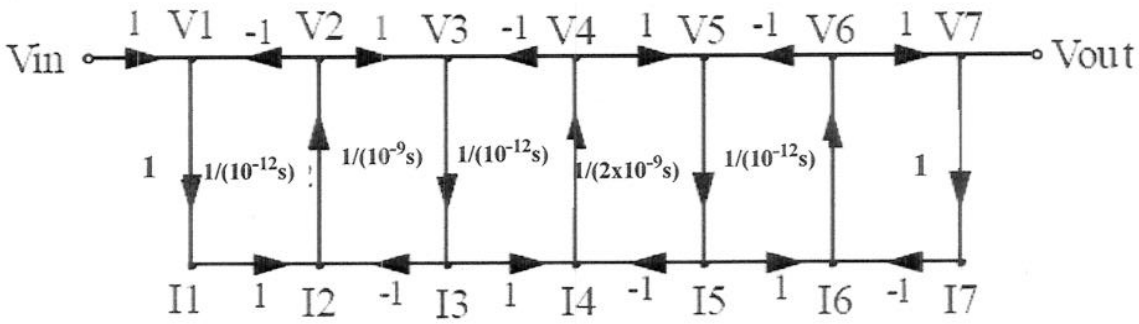
$$I4 = I3 - I5 \qquad V5 = V_4 - V6 \qquad I6 = I5 - I7$$

$$V4 = I4/(10^{-12}s) \qquad I5 = V5/(2 \cdot 10^{-9}s) \qquad V6 = I6/(10^{-12}s)$$

$$V7 = V6$$

$$I7 = V7$$

(b) (Application of theory)



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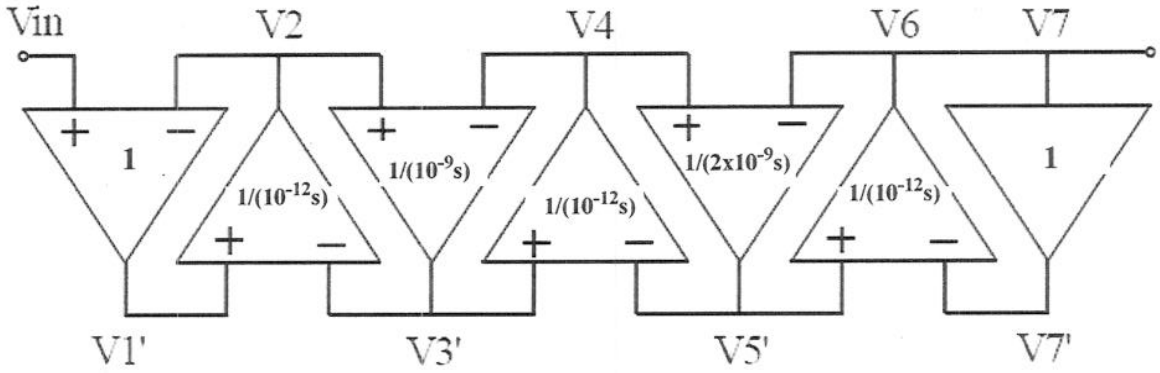
(c) (application of theory)



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6.

(a) (New theory)

Following the same reasoning and calculations as for the MOS differential pair:

$$I_{out} = \frac{C_i}{C_T} V_{in} \sqrt{2\beta I_s} \sqrt{1 - \frac{\left(\frac{C_i}{C_T}\right)^2 V_{in}^2 \beta}{2I_s}} = \frac{1}{2} V_{in} \sqrt{2\beta I_s} \sqrt{1 - \frac{0,25 V_{in}^2 \beta}{2I_s}}$$

(b) (New theory)

The FGMOS and MOS have the same functional dependence if C_i=C_T, this is if there is only one input. Hence, from the equation obtained in (a), the output current in a MOS differential pair is given by:

$$I_{out} = V_{in} \sqrt{2\beta I_s} \sqrt{1 - \frac{V_{in}^2 \beta}{2I_s}}$$

(c) (New computed example)

For small signals the second square root in the expression of the output current can be neglected. Hence the transconductance for this circuit is given by:

$$G_m = \frac{1}{2} \sqrt{2\beta I_s}$$

(d) (New computed example)

Using the same reasoning as in (c) but with the equation obtained in (b), the small signal transconductance for a MOS differential pair is given by:

$$G_m = \sqrt{2\beta I_s}$$

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This is double the value than for the circuit in Figure 6.1. The only way of compensating for this "transconductance reduction" in Figure 6.1 is to biase the circuit with four times more current.

(e) (New theory)

Area and (from (d)) power

(f) (New theory)

It is more linear, since the non-linear term in the expression of I_{out} is scaled down by the ratio between the input capacitance and the total capacitance