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Paper Number(s): **E2.1**
ISE2.2

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2002

EEE/ISE PART II: M.Eng., B.Eng. and ACGI

DIGITAL ELECTRONICS II

Wednesday, 5 June 2:00 pm

There are FIVE questions on this paper.

Answer THREE questions.

Time allowed: 2:00 hours

Examiners responsible:

First Marker(s): Brookes,D.M.

Second Marker(s): Clarke,T.J.W.

E2.1
ISE2.2
2002

Notation: *Unless explicitly indicated otherwise, digital circuits throughout this paper are drawn with their inputs on the left and their outputs on the right. The notation X2:0 denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0.*

1. *Figure 1.1* shows the circuit of a CMOS gate. The on-resistance of the n-channel and p-channel transistors is $100/W$ and $200/W$ ohms respectively where W represents the transistor width in arbitrary units. The width of transistor Q1 is denoted by W_1, etc.

   (a) Derive a Boolean expression for OUT in terms of A, B and C. [4]

   (b) Determine the minimum widths that should be used for transistors Q4, Q5 and Q6 to ensure that the output impedance of the circuit never exceeds 100 Ω when OUT is low. You may assume that $W_4 = W_5$. [3]

   (c) Show that if $W_1 = W_2 = \dfrac{2W_3}{W_3 - 2}$ then the output impedance of the circuit when OUT is high will never exceed 100 Ω. Hence determine the widths that should be used for transistors Q1, Q2 and Q3 to ensure that the output impedance of the circuit never exceeds 100 Ω when OUT is high and that the sum $W_1 + W_2 + W_3$ is as small as possible. [7]

   (d) Using as few transistors as possible, design a CMOS circuit that will generate both of the following signals at the same time [6]

$$X = A + B \cdot C + \overline{E}$$
$$Y = (A + B \cdot C) \cdot \overline{F}$$

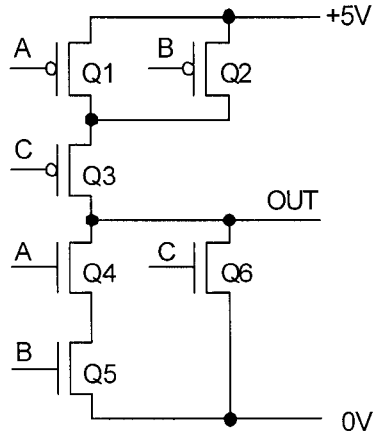


Figure 1.1

2. The circuit of *Figure 2.1* forms the interface between two systems, A and B, and consists of a register and a synchronous state machine whose state diagram is as shown. The signals RA and GA control the flow of data from System A to the register as follows: (i) System A sets RA=1 when new data is available at DA, (ii) the state machine then sets GA=1 to confirm that the data has been stored in the register, (ii) System A responds by setting RA=0 and finally (iv) the state machine sets GA=0. The signals RB and GB control the flow of data to System B in a similar manner. The signal L goes high to enable loading of the register on the following CLOCK rising edge. All signal transitions occur slightly after the rising edge of CLOCK.

(a) Complete the timing diagram of *Figure 2.2* by showing the sequence of states that the state machine follows and the waveform of the output signals L, GA and RB. You should also indicate on your timing diagram the clock edges on which DB changes. The vertical dashed lines in the figure denote CLOCK rising edges and the system is initially in state 0 as shown. [7]

(b) Determine the maximum rate at which data can be transferred from system A to system B. Draw a timing diagram showing the sequence of states followed and the waveforms of RA, GA, RB, GB and L when transferring data at this rate. [6]

(c) Explain how the state diagram must be modified if System B requires that DB should be valid at least two clock cycles before RB goes high. [7]

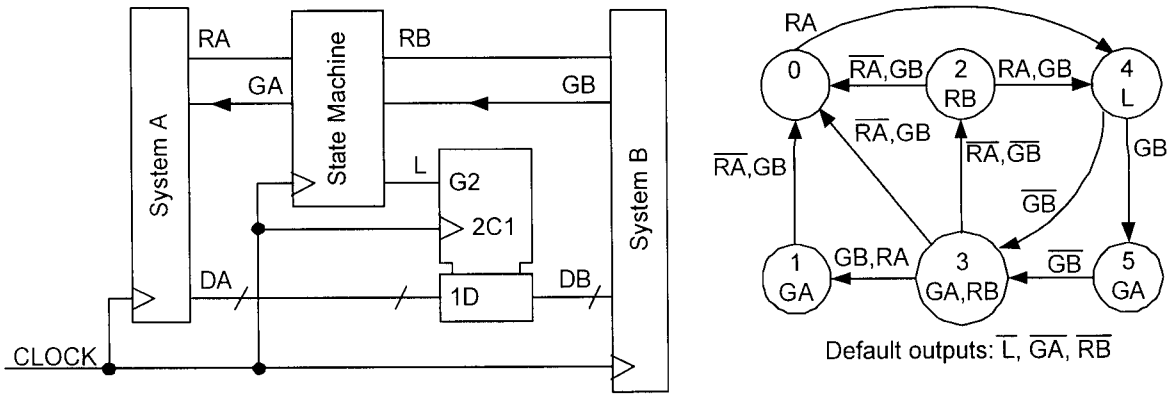


Figure 2.1

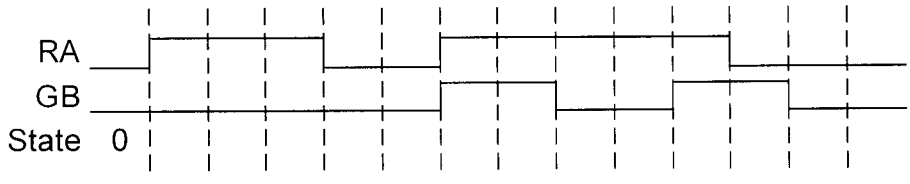


Figure 2.2

3. The circuit of *Figure 3.1* decodes the stream of data bits received at its input, IN. The waveform of IN for the bit sequence 0101 is shown in *Figure 3.2*. Each bit is transmitted within a cell of duration T with logical 0 and 1 bits transmitted as pulses of duration $2T/3$ and $T/3$ respectively. The circuit consists of two flipflops, an AND gate and a 10-bit binary counter. Only the most significant counter output, Q9, is used in the circuit and the counter value changes on the CLOCK rising edge according to the following table:

RST	IN	Q9	Action	
0	1	0	$q = q + 1$	} Counter wraps around between 1023 and 0
0	0	0	$q = q - 1$	
1	X	X	$q = 0$	
all other combinations			no action	

All transitions of IN occur just after a rising edge of the 1 MHz CLOCK signal.

(a) Explain why RST will be true for only one clock cycle per bit cell. [4]

(b) If the duration $T = 0.3$ ms, determine the value in the counter at the time that IN goes low for a bit cell that contains (i) a logical 0 and (ii) a logical 1. [4]

(c) If the duration $T = 0.3$ ms, determine the value in the counter the time that IN goes high at the end of a bit cell that contains (i) a logical 0 and (ii) a logical 1. [4]

(d) If the duration $T = 0.3$ ms, draw a timing diagram showing the waveforms of IN, RST, Q9 and OUT when the input corresponds to the bit sequence 0101. Explain the relationship between the waveform of OUT and the received sequence of bits. [4]

(e) Determine the maximum value of T for which the circuit will function correctly. Explain how the circuit will fail if T is slightly greater than this value. [4]

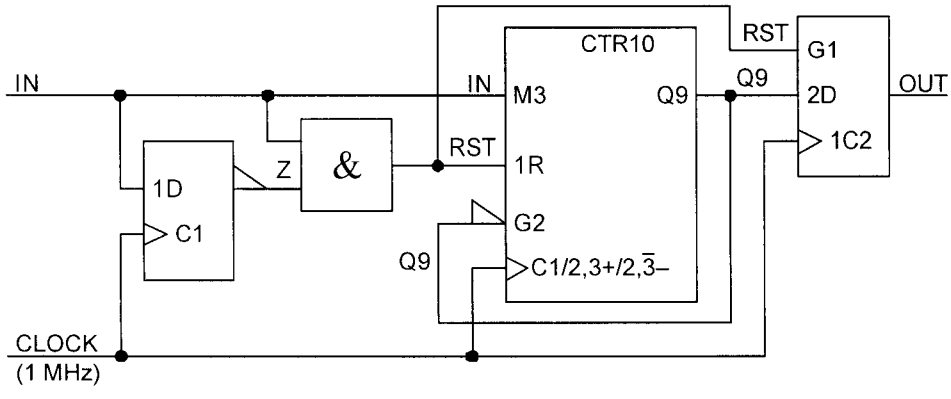


Figure 3.1

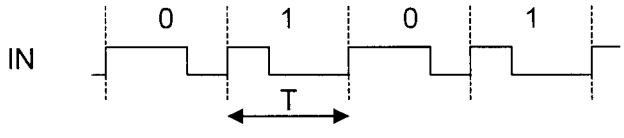


Figure 3.2

4. (a) *Figure 4.1* shows the circuit of an n-bit carry-save adder module that is implemented using n independent full-adders. If p, q, ... represent the values of the unsigned binary numbers $P_{n-1:0}$, $Q_{n-1:0}$, ... show that $p+q+r=2c+s$. [4]

(b) If $n \geq 4$ and the numbers p, q and r lie in the range 0 to 9, determine the maximum values of c and s showing your reasoning clearly. In each case, give an example of input number p and q that cause the maximum to be attained. [4]

(c) *Figure 4.2* shows four carry-save adder modules connected to add together six input numbers. The signal busses A, B, C, ... do not necessarily all have the same width but may be assumed to be wide enough to represent the unsigned values a, b, c, ... without overflow. [4]

The modules marked "×2" multiply their inputs by 2. Explain how these "×2" modules can be implemented without using any logic gates and show that $a+b+c+d+e+f=2y+x$.

(d) If a, b, ..., f lie in the range 0 to 9, determine the maximum value that can be taken by each of g, h, i, j, k and l. Determine the number of full-adder modules required to implement each of the four carry-save adders. The adders are labelled 1,2,3 and 4 for reference. [8]

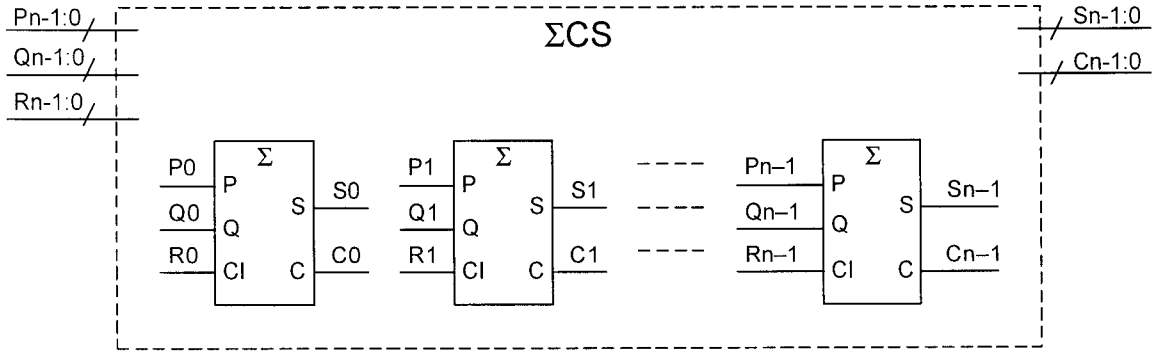


Figure 4.1

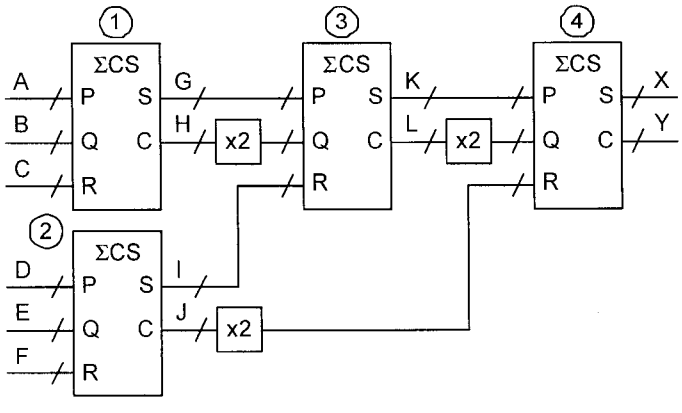


Figure 4.2

5. *Figure 5.1* shows part of the circuit for an integrating Analogue to Digital converter. The circuit contains a resistor, capacitor, operational amplifier, comparator and switch. The operational amplifier and comparator may be assumed ideal. The voltages at points W, X, Y and Z are respectively $w(t)$, $x(t)$, $y(t)$ and $z(t)$.

(a) Assuming that w is a constant, derive an expression for $\frac{dz}{dt}$ in terms of y and w. [4]

(b) To perform a conversion, the switch is placed in position A for a time $T = 20$ ms then changed to position B until COMP becomes high and finally changed to position C. The time spent in position B is denoted by t.

Derive an expression for x in terms of T, t and w under the assumption that z is initially at 0 V and that x and w remain constant throughout the conversion. [6]

(c) Draw a dimensioned sketch showing the waveforms of y, z and COMP during a conversion when $x = 3$ V, $w = -5$ V, R = 22 kΩ and C=1 μF. Assume that the switch is in position C prior to the conversion and that z is initially zero. [6]

(d) Given that the output voltage of the operational amplifier is restricted to ±10 V, determine the maximum and minimum values x for which the circuit will function correctly when $w = -5$ V, R = 22 kΩ and C = 1 μF. Assume that the initial conditions are the same as in part (c). [4]

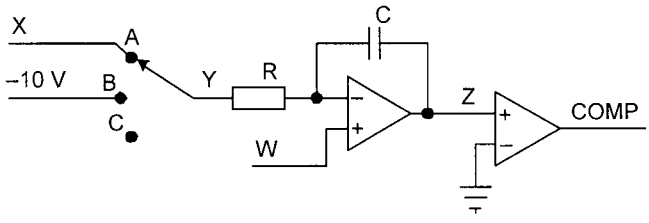


Figure 5.1

2002 E2.1/ISE2.2 Solutions

1. (a) $\overline{OUT} = AB + C \Rightarrow OUT = \overline{AB + C} = \overline{AB} \cdot \overline{C} = (\overline{A} + \overline{B}) \cdot \overline{C}$ [4]

(b) Q6 should have an impedance of 100Ω and so $W_6 = 1$. [3]

Q4 and Q5 should total 100Ω impedance which implies that $W_4 + W_5 \leq W_4 W_5$. If we assume that Q4 and Q5 have the same width (which actually minimizes the total width) then $W_4 = W_5 = 2$.

(c) The worst case is when only one of Q1 and Q2 is on. We want

$$200/W_1 + 200/W_3 = 100$$
$$\Rightarrow 2/W_1 = 1 - 2/W_3 = (W_3 - 2)/W_3$$
$$\Rightarrow W_1/2 = W_3/(W_3 - 2) \Rightarrow W_1 = 2W_3/(W_3 - 2)$$

We want to minimise the expression

$$W_1 + W_2 + W_3 = \frac{4W_3}{W_3 - 2} + W_3$$

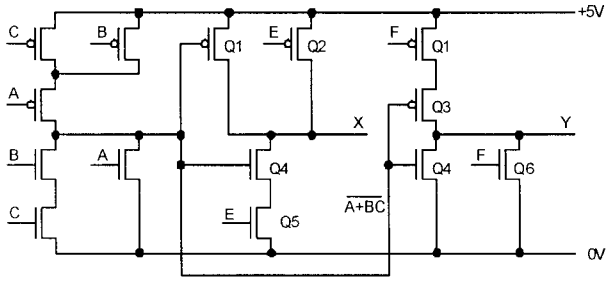
Differentiating this and setting it to zero gives:

$$\frac{4(W_3 - 2) - 4W_3}{(W_3 - 2)^2} + 1 = 0 \quad \Rightarrow \quad W_3^2 - 4W_3 - 4 = 0$$

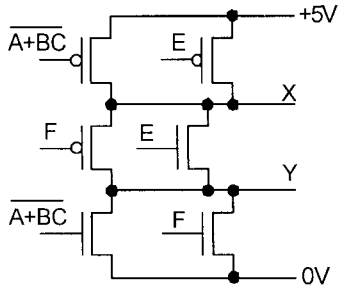
$$\Rightarrow \quad 2 \pm \sqrt{4 + 4} = -0.83 \text{ or } 4.83$$ [7]

The positive answer is the correct one. Hence $W_1 = W_2 = 2 + \sqrt{2} = 3.41$.

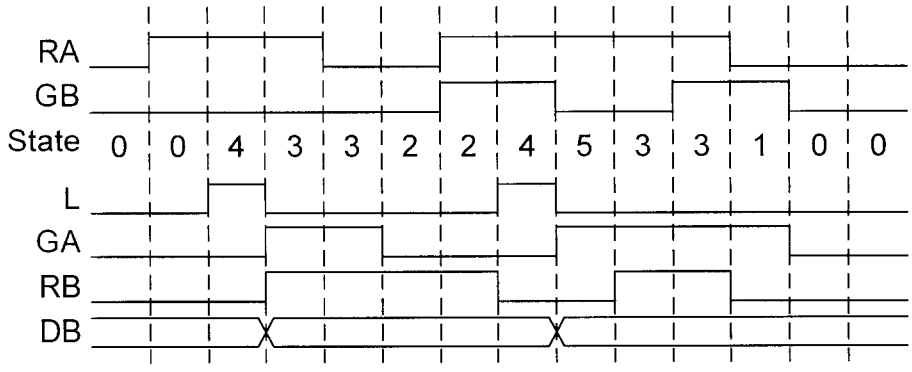
(d) We make a circuit for $\overline{A + BC}$ and then combine this with E and F to get the required expressions. [6]



The circuit on the right is appealing but doesn't work since the power supply is short-circuited if A,E and F are all true.

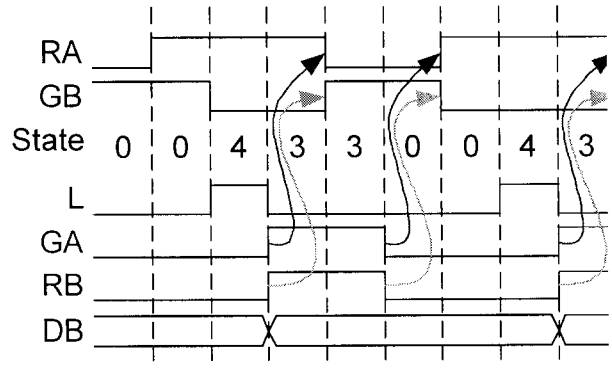


2. (a)



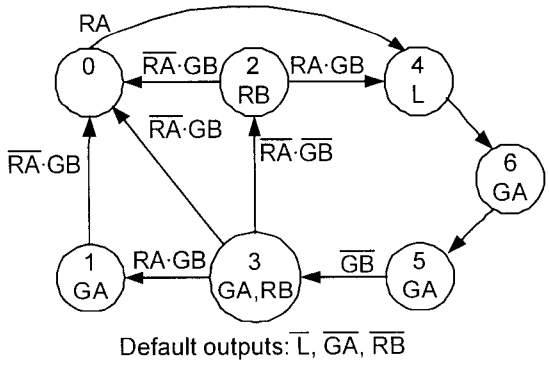
[7]

(b) The following sequence of five events must happen: RA↑, L↑, GA↑, RA↓, GA↓ and so the minimum number of clock cycles is five. Another way of looking at things is to realise that the maximum transfer rate occurs when RA and GB respond as soon as possible to changes in GA and RB respectively. Since transitions can only occur on clock rising edges, "as soon as possible" means the next rising edge of the CLOCK.



[6]

(c) DB becomes valid at the end of state 4, so we must wait at least two cycles before taking RB high. We do this by inserting an additional state (state 6) between states 4 and 5 and by deleting the short-cut between 4 and 3.



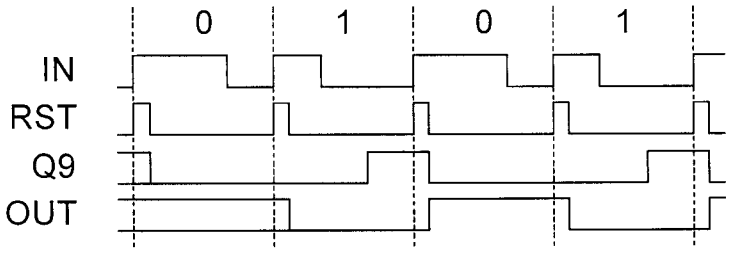
[7]

3. (a) Z is the inverse of IN but delayed by one clock cycle. RST is high when IN=1 and Z=1 which is when the current value of IN=1 and the previous value of IN=0. This occurs for one cycle immediately following the rising edge of IN at the beginning of each bitcell. [4]

(b) The counter is held at 0 for 1 μs and then counts up for as long as IN remains high. If IN stays high for n μs then the counter will reach the value n. The answers are therefore (i) 200 and (ii) 100. More precisely, when IN goes high, RST=1 during the first cycle so q=0 in the second cycle and reaches 199 or 99 just after IN goes low. [4]

(c) The counter then counts downwards but stops counting if Q9 goes high. Thus the answers are (i) 100 (or 99 to be exact), (ii) –1 (or 1023). Note that we assume the counter wraps around from 0 to 1023 when counting down. [4]

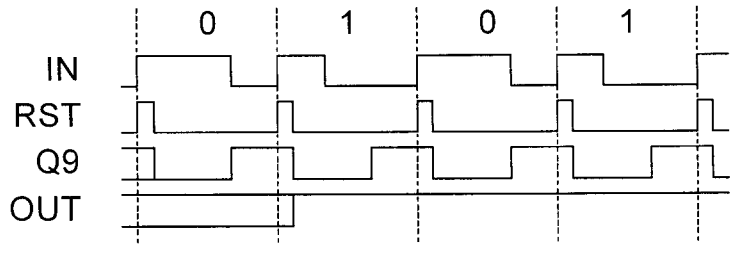
(d) The width of the RST pulse is one clock cycle: this has been exaggerated in the diagram below.



[4]

During each bitcell, OUT has the value of the bit that was received in the previous bitcell.

(e) The circuit will fail if an input pulse length is >511 clocks since then Q9 will go high which will freeze the counter. Thus we must have $2T/3 \leq 512$ μs which means $T \leq 768$ μs. For T slightly longer than this we will have OUT permanently high:



[4]

4. (a) For each full-adder, the output C and S can be viewed as a 2-bit number whose value equals the number of inputs that are high. I.e.

$$P_i + Q_i + R_i = 2C_i + S_i$$

Hence $p + q + r = \sum_{i=0}^{n-1} 2^i (P_i + Q_i + R_i) = \sum_{i=0}^{n-1} 2^i (2C_i + S_i) = 2c + s$ [4]

(b) Only the 4 least significant bits of p, q and r are ever non-zero so, since the full-adders are not connected to each other, this must also be true of c and s.

s can equal 15 if $p = 8$, $q = 7$ and $r = 0$.

C3 can only equal 1 if two output of the three inputs P3, Q3 and R3 are high. But is P3=1, then p = 8 or 9 and so P2=P1=0 (similarly for Q and R). It follows that if C3=1, then C2=C1=0 and so the largest possible value of c is 9. An example is p = q = 9 and r = 0. [4]

(c) A ×2 module can be implemented merely by relabelling the bits of the input number and introducing a 0 as the new least significant bit.

We have $2y + x = k + 2l + 2j = (g + 2h) + (i + 2j) = (a + b + c) + (d + e + f)$. [4]

(d) For adders 1 and 2, $g \le 15$, $h \le 9$, $i \le 15$ and $j \le 9$. Each adder is 4-bits wide and requires 4 full adder modules.

For adder 3, the q input now has 5 bits so the maximum value of k is 31. The maximum value of l is however only 15 since only one of the inputs, q, can have Q4=1. The width of the adder is 5 bits but the circuitry needed for the MSB is trivial with S4 = Q4 and C4 = 0. Thus only 4 full-adders are required.

For adder 4, the maximum inputs are p = 31, q = 30 and r = 18. These are all 5-bit numbers so the width of the adder is 5-bits. However the LSB this time is trivial sing q and r are necessarily even with Q0 = R0 = 0. Hence S0 = P0 and C0 = 0 and only 4 full-adders are needed. [8]

[The maximum values of x and y are 31 and 22 respectively but this hard to prove and is not requested in the question].

5. (a) $\frac{dz}{dt} = \frac{w-y}{RC}$ [4]

(b) While the switch is in position A, $\frac{dz}{dt} = \frac{w-x}{RC}$. So since w and x are constant, we can integrate to get $z(T) = \frac{T}{RC}(w-x)$.

While the switch is in position B, $\frac{dz}{dt} = \frac{w+10}{RC}$ so z will increase by $\frac{t}{RC}(w+10)$.

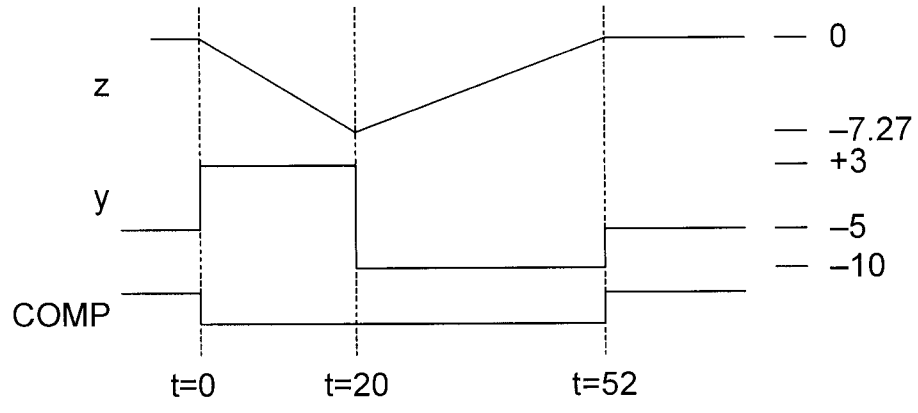
Since t ends when z reaches 0, we must have

$$z(T) = \frac{T}{RC}(w-x) = -\frac{t}{RC}(w+10)$$

$$\Rightarrow x = w + \frac{t}{T}(w+10)$$

[6]

(c) We have $z(T) = \frac{T}{RC}(w-x) = -7.27$ V, and $t = -T\frac{w-x}{w+10} = 32$ ms. In the diagram below, times are in ms and voltages in volts.



[6]

(d) The maximum input is limited by the op-amp.

$$z(T) = \frac{T}{RC}(w-x) \geq -10 \Rightarrow x \leq w + \frac{10RC}{T} = 6\text{ V}$$

[4]

The minimum input is $x \geq w = -5$ V since otherwise z will never go negative and COMP will remain high always.