Paper Number(s): **E4.20**
AC3
ISE4.19

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2002

MSc and EEE/ISE PART IV: M.Eng. and ACGI

INTRODUCTION TO DIGITAL INTEGRATED CIRCUIT DESIGN

Friday, 10 May 10:00 am

There are SIX questions on this paper.

Answer FOUR questions.

Time allowed: 3:00 hours

Corrected Copy

Examiners responsible:

First Marker(s): Cheung,P.Y.K.

Second Marker(s): Clarke,T.J.W.

Information for Invigilators:

Students may bring any written or printed aids into the examination.

Information for Candidates:

Students may need red, green, blue, yellow and black coloured pens.

1. a) *Figure 1.1* (See the colour supplementary sheet) shows the layout of a CMOS cell with four inputs `IN1`, `IN2`, `IN3` and `IN4`, and one output `OUT`. Extract and draw the transistor-level schematic diagram.

[10 marks]

b) Draw the vertical cross sections through the chip along the lines `AA'` and `BB'`. Label your diagram and indicate the different types and levels of doping (e.g. p^-, n^+ etc).

[8 marks]

c) What function does this circuit perform?

[2 marks]

2. A vector with coordinate (x,y) is rotated by 30° counter clockwise to (x',y') by applying *equation 1*:

$$\begin{pmatrix} x' \\ y' \end{pmatrix} = \begin{pmatrix} a & b & e \\ c & d & f \end{pmatrix} \begin{pmatrix} x \\ y \\ 1 \end{pmatrix} \qquad \textit{Equation } 1$$

where $a = d = 0.1101111_2$, $b = 0.1_2$, $c = -0.1_2$ and $e = f = 0$. The input coordinates lie in the range +511 to –512, and are expressed in 2's complement form.

a) By employing distributed arithmetic, design at architectural level a circuit to implement this coordinate rotation engine. Show the widths of the datapaths and the positions of the binary points in your design so that there is no loss of precision throughout the circuit.

[12 marks]

b) Determine the contents of the read-only memories used in your design.

[8 marks]

3. *Figure 3.1a* shows a 0.35μm CMOS implementation of an 8-input AND function using 2-input NAND gates, 2-input NOR gates and an inverter. *Figure 3.1b* shows the transistor level circuit diagram of the NAND gate for stage 1 only.

This 8-input AND module is driving a capacitance load that is equivalent to 29.4 μm of gate width. The parasitic capacitance factor is assumed to be 1.

a) Using the method of logic effort, estimate the best path delay from A to B achievable with optimal transistor sizing of stages 2 to 4. The delay should be expressed in terms of τ, the unit inverter delay.

[5 marks]

b) Calculate the sizes of pull-up and pull-down transistors for the gates used in stages 2-4 in order to achieve this delay.

[12 marks]

c) The process is calibrated with a 13-stage ring oscillator. The oscillation frequency is found to be 641MHz. Estimate the absolute path delay from A to B. State clearly any assumptions made.

[3 marks]

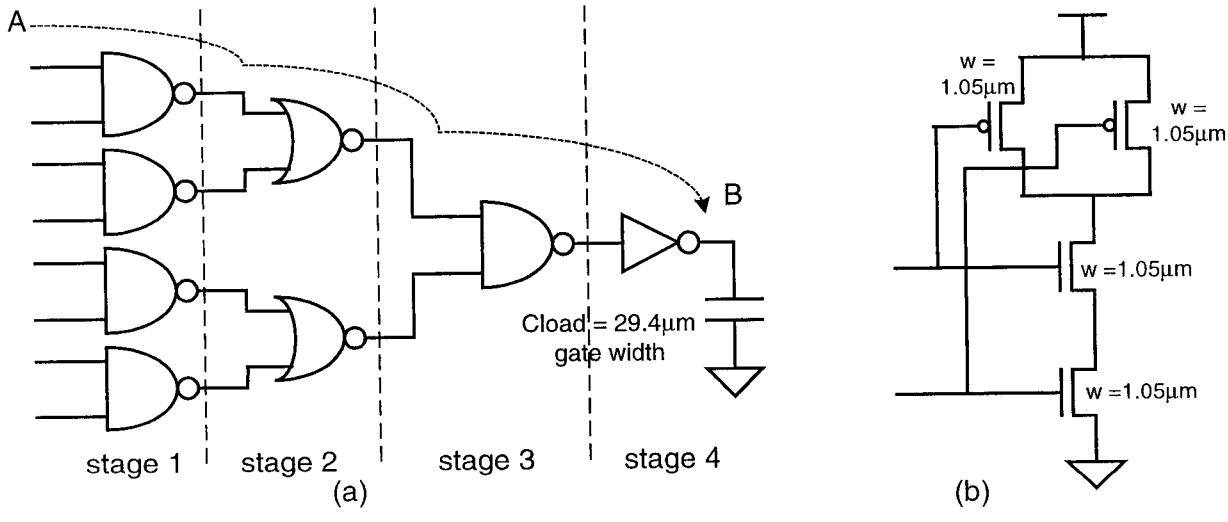

Figure 3.1

4. *Figure 4.1* shows a clocked gate with four dual-rail logic inputs A, B, C and D, and a dual-rail output X.

a) Using symbolic layout representation (for example a stick diagram), design the layout of the circuit.

[10 marks]

b) By drawing a truth table for the gate, or otherwise, derive with explanation the logic function performed by this gate circuit.

[10 marks]

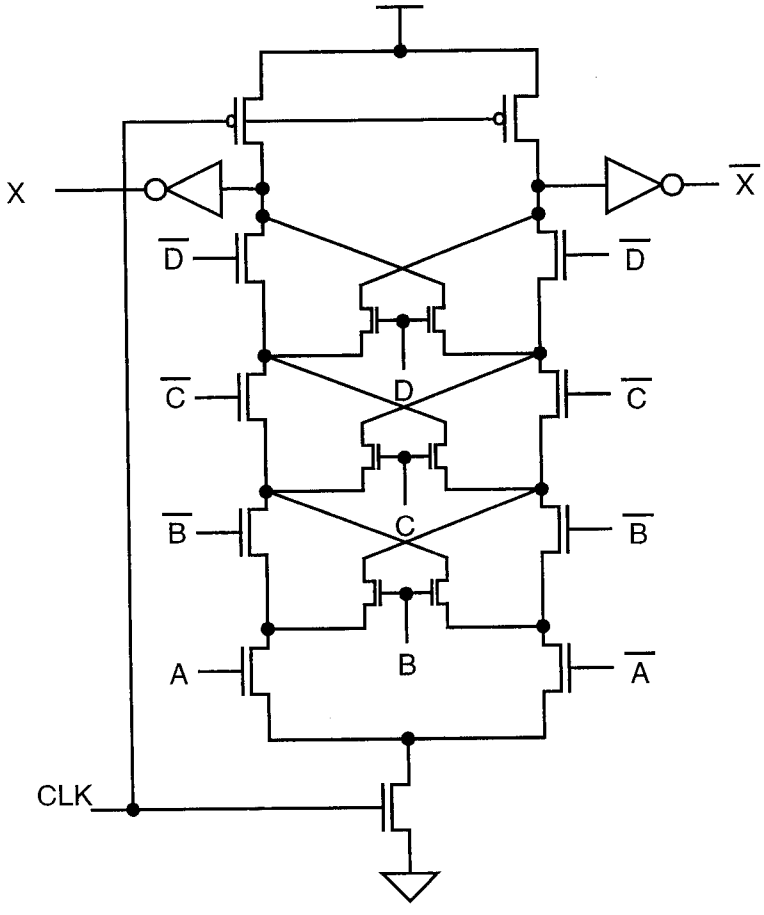

Figure 4.1

5. a) Explain the principle behind the operation of a pulse-triggered latch.

[2 marks]

b) *Figure 5.1* shows a synchronous circuit used in the AMD K-6 microprocessor. *Figure 5.2* shows the signals at CLK and D. Draw a timing diagram showing the signals CLK, D, X, Y and Z, and the state of transistors T1, T2, T3 and T4. The timing diagram should be labelled with the following signal states:

driven low (DL) - a path to ground exists,
driven high (DH) - a path to Vdd exists,
charged low (CL) - high impedance with no stored charge, and
charged high (CH) - high impedance with stored charge at Vdd
don't know (X) - unknown level.

[18 marks]

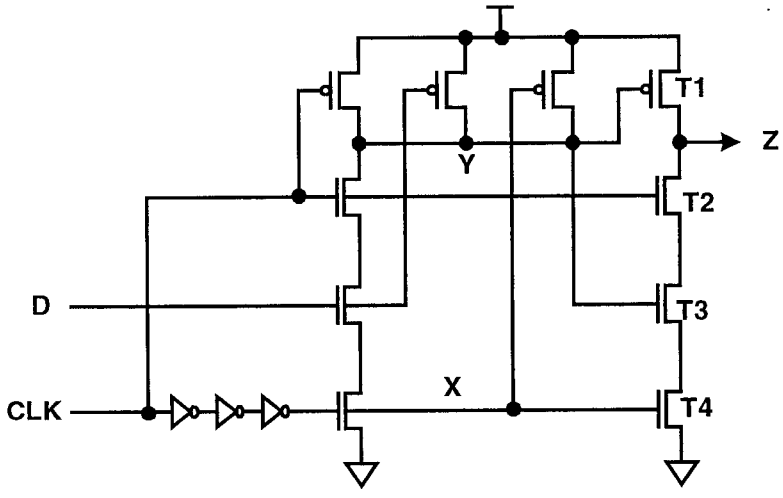

Figure 5.1

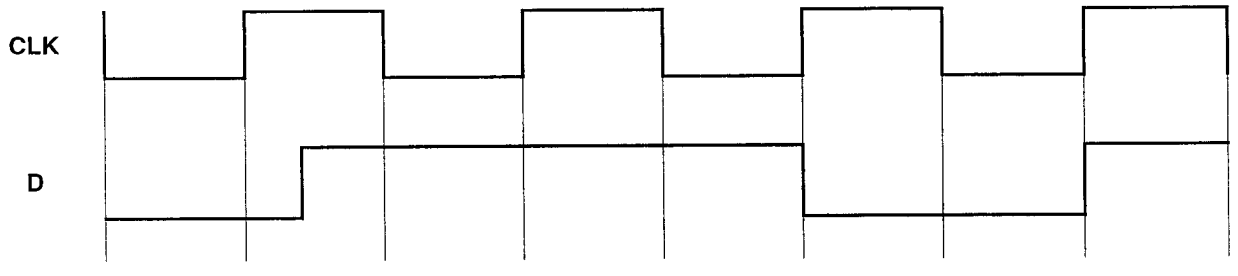

Figure 5.2

6. a) Design a complex CMOS gate to implement the Boolean function with inputs A, B, C and output Z defined by the truth table shown in *Figure 6.1*.

[5 marks]

b) Determine the size of all the transistors in order to ensure approximately equal rise and fall time at the output of your circuit.

[4 marks]

c) The CMOS gate in a) performs the function of a 1-bit binary comparison. Explain in plain English the functional behaviour of the gate.

[3 marks]

d) Using this gate, or otherwise, design an n-bit datapath circuit that performs the function:

$$R = max\ (x, y).$$

[8 marks]

C	B	A	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Figure 6.1

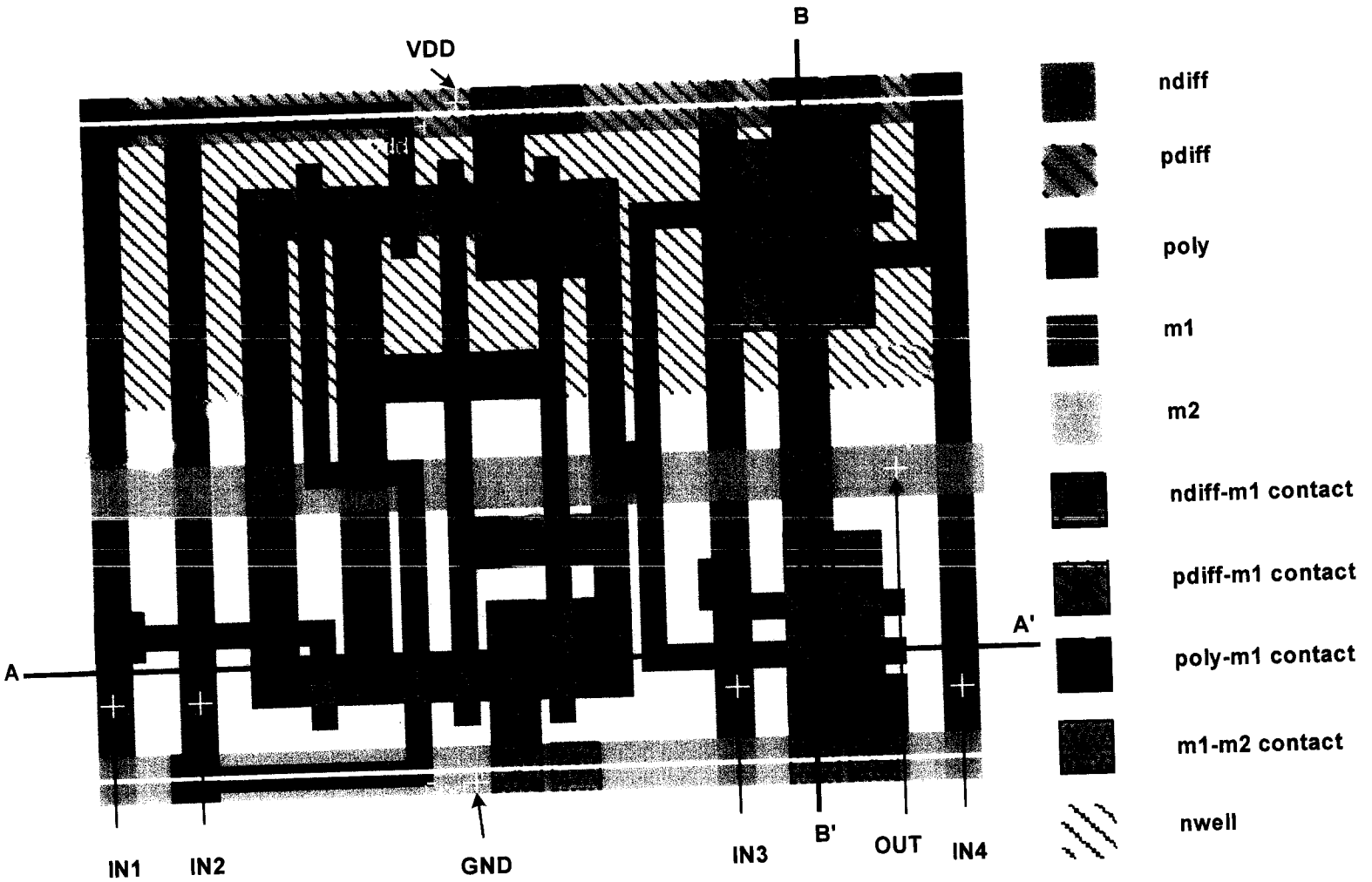

Figure 1.1 Layout of a full-custom cell for Question 1

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PART IV

INTRODUCTION TO DIGITAL IC DESIGN

SOLUTIONS

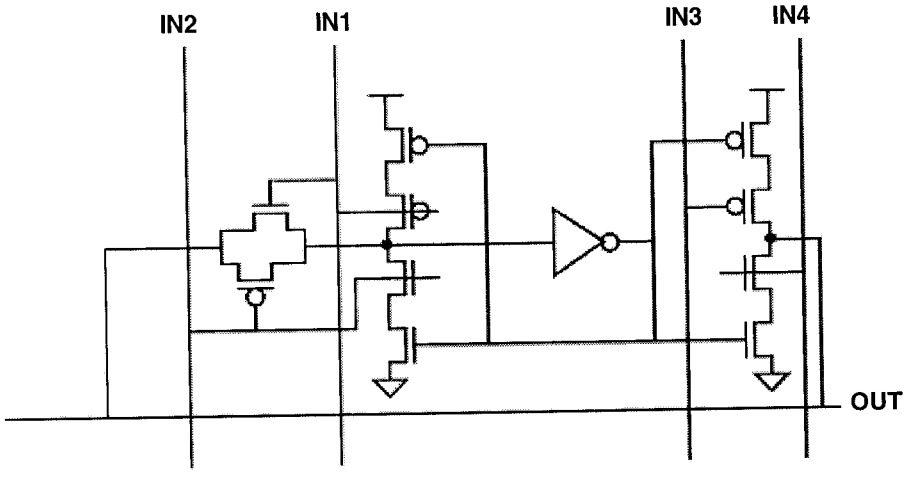
This is an open-book examination.

You may need red, green, blue, yellow and black coloured pens.

First Marker: *PYKC/TJWC*
Second Marker: *TJWC/PYKC*

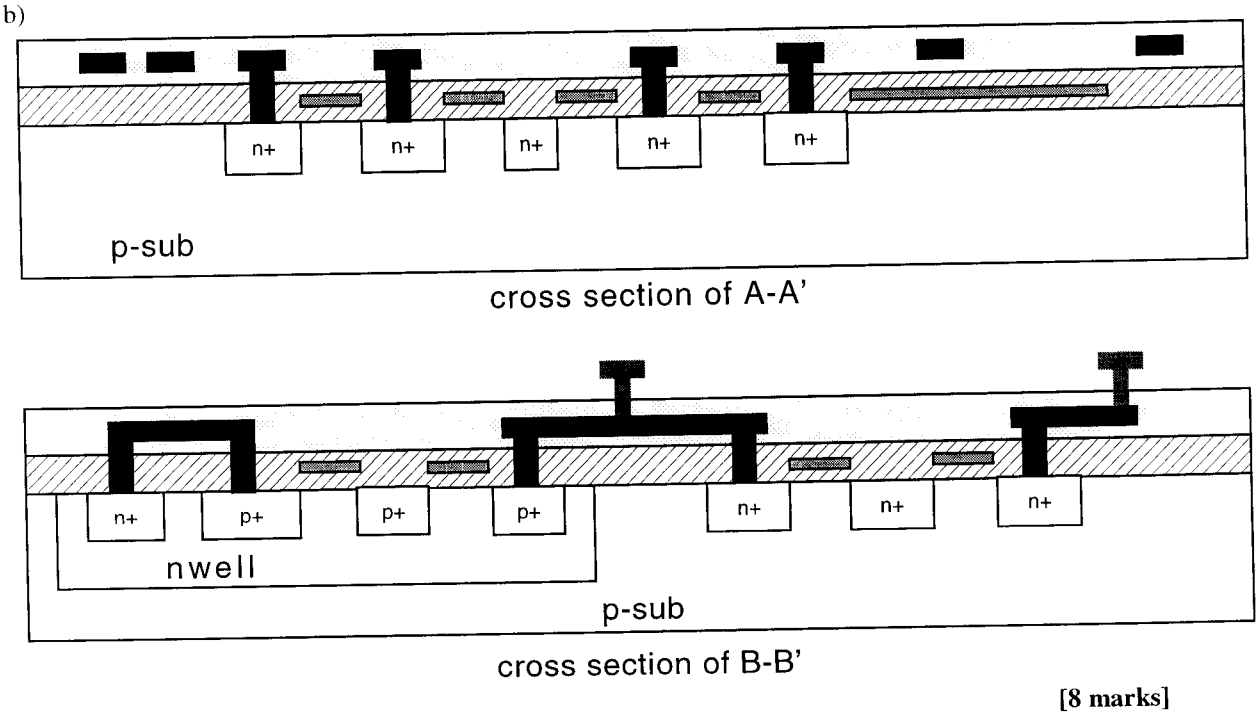
Solution to Question 1

a)



[10 marks]

b)



[8 marks]

c)

This is a D-register or a register backed 1-bit memory cell.

[2 marks]

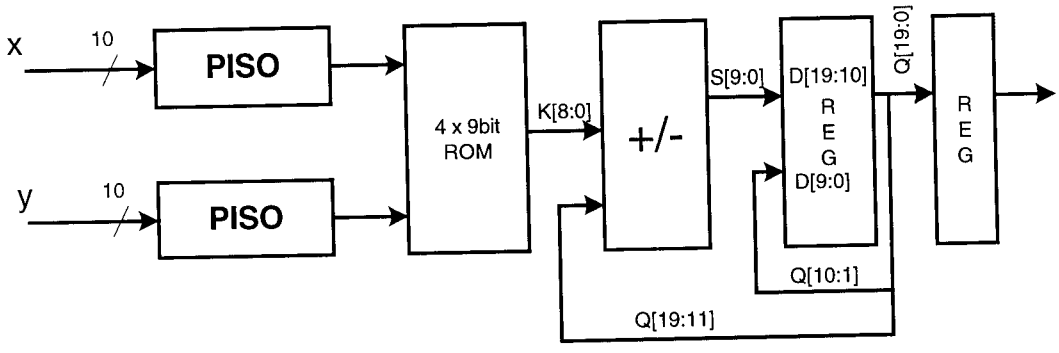
Solution to Question 2

Students have designed a digital filter using distributed arithmetics as the course work for this course. This question tests their ability to apply what they have learned to a problem they have not come across before.

(a) Two inner products:-

$$x' = \begin{pmatrix} a & b & e \end{pmatrix} \begin{pmatrix} x \\ y \\ 1 \end{pmatrix} \quad and \quad y' = \begin{pmatrix} c & d & f \end{pmatrix} \begin{pmatrix} x \\ y \\ 1 \end{pmatrix}$$

Each inner product can be computed using a distributed arithmetic engine as shown below.



This circuit takes 10 cycles to compute each coordinate transformation. During the last cycle the add/subtractor work as a subtractor.

[12 marks]

(b)

Use 9-bit ROM in 2's complement fix-point format: S I . I I I I I I I, where S= sign, I = 0 or 1. L

ROM1 (ax+by)

Address	**Contents**
0	0
1	a = 00.1101111
2	b = 00.1000000
3	a+b = 01.0101111

ROM2 (cx+dy)

Address	**Contents**
0	0
1	c = 11.1000000
2	d = 00.1000000
3	c+d = 00.0101111

[8 marks]

Solution to Question 3

(a) Normalise all sizes to 0.35μm. Then input capacitance = 6 (i.e. 6 x 0.35 μm gate width). The load capacitance is 29.4/0.35 = 84.

Logic Effort	G = (4/3) x (5/3) x (4/3) x 1 = 80/27
Electrical Effort	H = 84/6 = 14
Branching Effort	B = 1
Path Effort	F = GBH = 41.481
Best stage effort	$f = F^{1/4} = 2.54$
Delay	D = path delay + parasitic delay = 2.54 x 4 + 7 x 1 = 17.15τ.

[5 marks]

(b)
Use normalised gate width – absolute value = width x 0.35um.

Stage	Gate	g	H = 2.54/g	input width (normalised)	pull-up	pull-down
1	NAND	4/3	1.91	6	3	3
2	NOR	5/3	1.524	1.91x6 = 11.43	9.14	2.29
3	NAND	4/3	1.91	1.52x11.43=17.42	8.71	8.81
4	INV	1	2.54	1.91x17.42=33.27	22.18	11.09
5	Output			2.54x33.27=84.5		

[12 marks]

(c)

Assumptions: 1) parastic delay = inverter delay, 2) measuring oscillator frequency does not load the oscillator itself.

Then unit inverter delay τ = 1/(4x stages x oscillation frequency) = 30 ps.

Therefore path delay = 17.15τ = 0.51ns.

[3 marks]

Solution to Question 4

(a) Layout depends on student's design. Full marks for topologically correct design with sensible layout. Deduce marks for poor layout of transistors that potentially takes lots of room.

[10 marks]

(b) Precharge on low phase of the clock. The truth table (at least a few entries of it) can be found by tracing the evaluate path during the high phase of the clock. The rest of the entry to the truth table may be inferred.

A	B	C	D	X
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

The function of the circuit is X = parity = A $\oplus$ B $\oplus$ C $\oplus$ D.

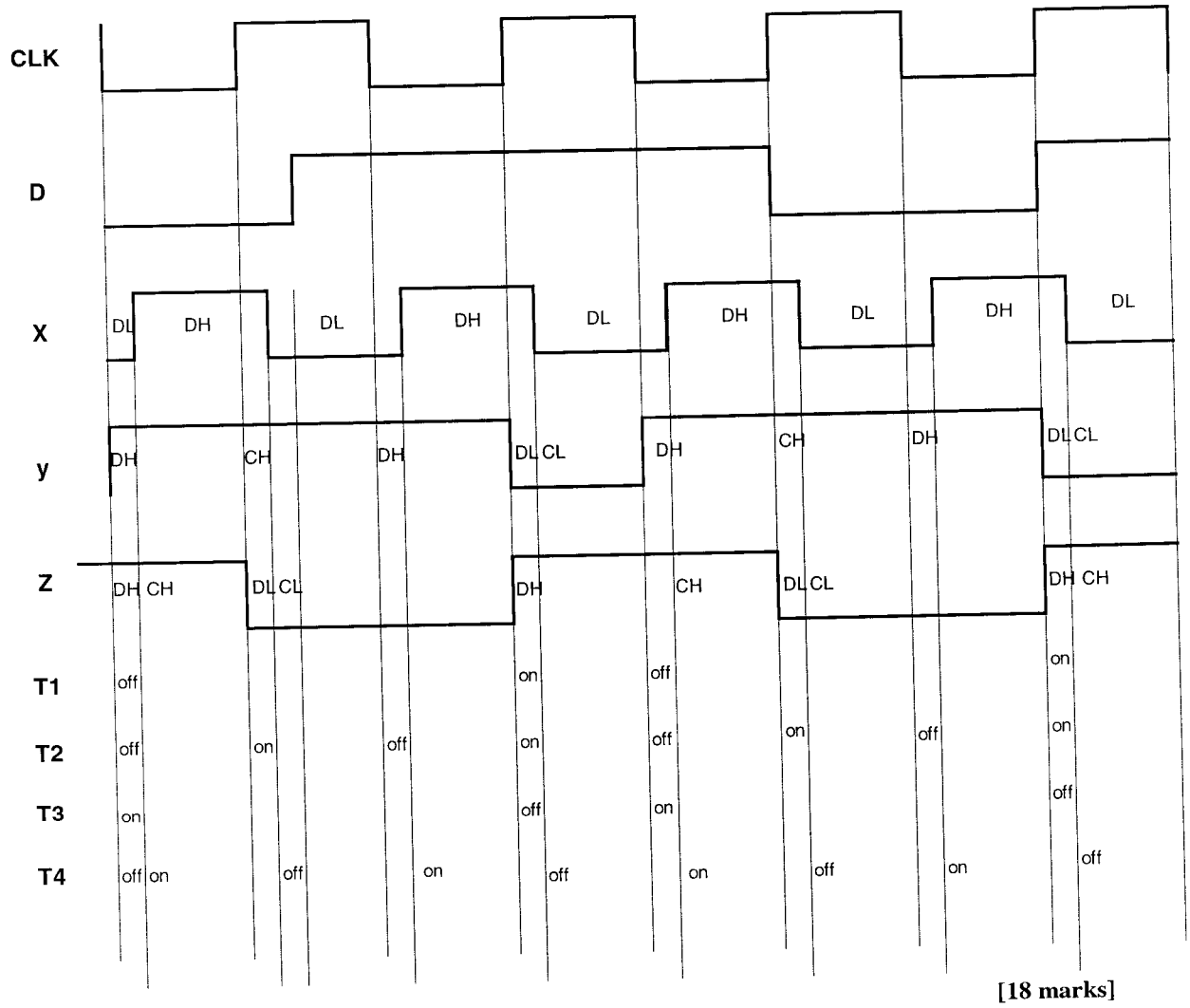
[10 marks]

Solution to Question 5

(a) A pulse-trigger latch/flip-flop consists of a pulse generator connected to the clock signal. A valid clock edge triggers a pulse the the latch/register which samples and store the input data value. The advantage of the pulse-trigger latch is that it can yield negative setup time. The disadvantage is that the pulse width may not be that well controlled and the pulse generation circuit dissipates power no matter if the input data is changed or not.

[2 marks]

(b)

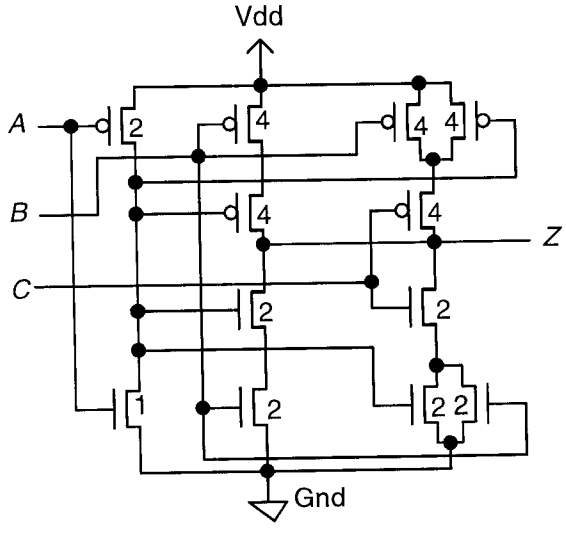


[18 marks]

Solution to Question 6

(a) and (b) The function is $Z = \overline{A} \bullet B + \overline{A} \bullet C + B \bullet C$

[5 marks]
[4 marks]

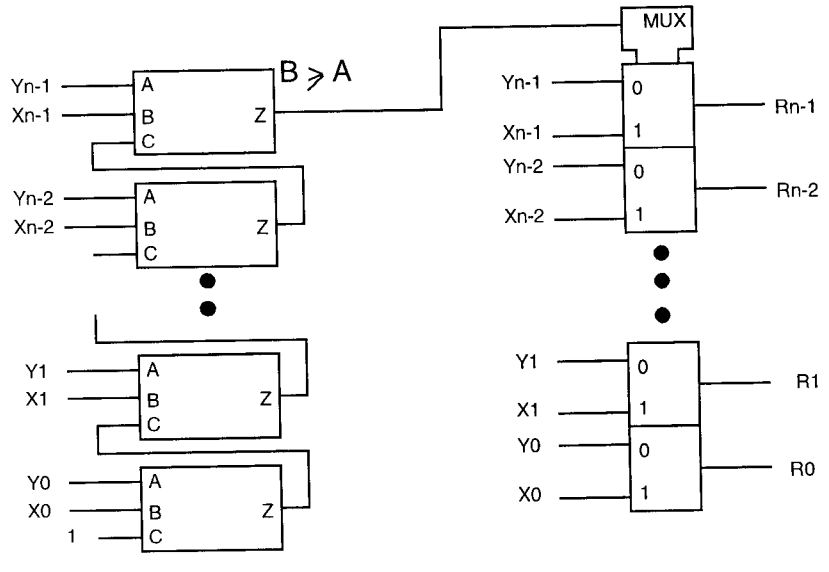


(c) This is a 1-bit comparator performing the function:

IF (C=0), Z = (B>A)
Else
Z = (B==A).

[3marks]

(d)



[8 marks]