UNIVERSITY OF LONDON

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2003

BEng Honours Degree in Computing Part III
BEng Honours Degree in Information Systems Engineering Part III
MEng Honours Degree in Information Systems Engineering Part III
MEng Honours Degree in Information Systems Engineering Part IV
MEng Honours Degrees in Computing Part IV
MSc in Advanced Computing
PhD
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER C318=I3.4=I4.18

CUSTOM COMPUTING

Friday 9 May 2003, 14:30
Duration: 120 minutes

Answer THREE questions

Paper contains 4 questions
Calculators required

1a Define *series composition* and *converse* in Ruby.

b Provide a recursive definition for repeated series composition, R^n.

c Given that $Q \ ; \ R = R \ ; \ Q$, show by induction that

$$Q \ ; \ R^n = R^n \ ; \ Q$$

d Use the result in Part c to show by induction that

$$(Q \ ; \ R)^n = Q^n \ ; \ R^n$$

e The string matcher *M0* calculates the number of matches of corresponding characters in two strings stored in two linear arrays of registers:

$$\begin{aligned} M0 &= MC^n \ ; \ \pi_1 \\ MC &= \mathsf{snd}\,([D, D] \ ; \ fork \ ; \ \mathsf{fst}\, eql) \ ; \ rsh \ ; \ \mathsf{fst}\, add \end{aligned}$$

where D denotes a register, *eql* denotes a character comparator, *add* denotes an adder, and *rsh* is given by

$$\langle x, \langle y, z \rangle \rangle \ rsh \ \langle \langle x, y \rangle, z \rangle$$

i) Provide a diagram of *M0* when n=4.

ii) Show how the transformation in Part d can be used to derive a pipelined matcher, *M1*.

The five parts carry, respectively, 10%, 10%, 20%, 20% and 40% of the marks.

2 The core of a pipelined adder consists of m pipeline stages, each containing k fulladders and a register.

a Provide a circuit diagram of the pipelined adder when m=3 and k=2. The diagram should include appropriate arrays of registers at the inputs and outputs of the core for data alignment.

b How many registers are there in a design description with any given m and k, including both core and data alignment registers?

c Describe the core and the data alignment circuits for the pipelined adder in the Ruby language. Provide a Ruby transformation (no proof is required) which can be used to derive the pipelined adder from the corresponding unpipelined version.

The three parts carry, respectively, 25%, 25% and 50% of the marks.

3a Recall that:

$$\begin{array}{ccc} \langle x, y\rangle & \pi_2 & y \\ \langle x, \langle y_1, y_2, \ldots, y_n\rangle\rangle & apl_n & \langle x, y_1, y_2, \ldots, y_n\rangle \end{array}$$

Provide two designs, $sum1_n$ and $sum2_n$, for summing a list of n numbers using a network of two-input adders described by rdl, the left reduction combinator. $sum1_n$ contains n adders and should involve π_2, while $sum2_n$ contains $(n-1)$ adders and it would involve *apl* (or suitably reflected versions of these components).

b A combinational design means that a computation will be completed within each clock cycle, and no information will be passed between cycles. Provide a combinational design IP_m for computing the inner product of two vectors of length m using $sum1_m$.

c Provide a diagram of the wiring block $dstl_3$, where $dstl_m$ is given by

$$\langle x, \langle y_1, y_2, \ldots, y_m\rangle\rangle \quad dstl_m \quad \langle\langle x, y_1\rangle, \langle x, y_2\rangle, \ldots, \langle x, y_m\rangle\rangle$$

d Provide a combinational design $MV_{m,n}$ for multiplying an m by n matrix and an n-element vector. Your design should involve IP_n and $dstl_m$. At each cycle, the matrix is represented as a list of lists, with the first list corresponding to the top row in the matrix, while the vector is represented as a list, with the first element corresponding to the top element of the vector. Show that your design produces the correct answer for the matrix $\langle\langle a, b, c\rangle, \langle d, e, f\rangle\rangle$ and the vector $\langle p, q, r\rangle$.

e Find A and B such that the design MM_n, given by

$$MM_n \;=\; \mathsf{snd}\, A \;;\; B \;;\; \mathsf{map}_n\, MV_{n,n}$$

corresponds to a combinational design for multiplying two n by n square matrices. Show that your design produces the correct answer for multiplying the matrices $\langle\langle a, b\rangle, \langle c, d\rangle\rangle$ and $\langle\langle p, q\rangle, \langle r, s\rangle\rangle$.

The five parts carry, respectively, 30%, 15%, 15%, 20% and 20% of the marks.

4a A hexagonally-connected architecture can be described by the following combinator,

$$hex_{m,n}\, R \;=\; \mathsf{grid}_{m,n}\,(W \updownarrow R)$$

where

$$\langle a, \langle a, b\rangle\rangle \; W \; \langle\langle b, c\rangle, c\rangle$$

Provide a diagram for such an architecture when $m = n = 3$.

b A barrel shifter can be used to shift its data input by an amount given by its control input.

i) Provide the circuit diagram of a barrel shifter with 3-bit data input, 7-bit control input and 5-bit output, using a rectangular array of 15 multiplexors. Only one bit of the control input will be high at any time; the 7 possible control input configurations correspond to left shift or right shift from 0 up to 3 places. One or more zeroes will be introduced when the input is shifted for one or more places to the left or right. Label the input data, control input and output values on your circuit diagram, given that the 7-bit control input is 0000010.

ii) Describe the above barrel shifter in Ruby using the *hex* combinator.

The two parts carry, respectively, 25% and 75% of the marks.