

UNIVERSITY OF LONDON  
IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2005

BEng Honours Degree in Computing Part III  
MEng Honours Degree in Electrical Engineering Part IV  
MSci Honours Degree in Mathematics and Computer Science Part IV  
BSc Honours Degree in Mathematics and Computer Science Part III  
MSc in Advanced Computing  
for Internal Students of the Imperial College of Science, Technology and Medicine

*This paper is also taken for the relevant examinations for the  
Associateship of the City and Guilds of London Institute  
This paper is also taken for the relevant examinations for the  
Associateship of the Royal College of Science*

PAPER C332=I3.26=I4.56=E4.31

ADVANCED COMPUTER ARCHITECTURE

Thursday 5 May 2005, 10:00  
Duration: 120 minutes

*Answer THREE questions*

Paper contains 4 questions  
Calculators not required

- 1 This question concerns out-of-order execution in the IBM Power5 processor, as described in the paper “IBM Power5 Chip: A Dual-core Multithreaded Processor” (IEEE Micro March-April 2004), which you should have available to you in the examination. **See, in particular, pages 43–44.** Where the paper is incomplete, you are invited to speculate using your understanding of the underlying architectural principles.
  - a The PowerPC instruction set has 32 integer (“general-purpose”) registers and 32 floating-point registers. The Power5 has 120 physical general-purpose registers and 120 physical floating point registers. Suppose the instruction set were extended to support 120 logical registers. Give *two* reasons why register-renaming (“mapping”) might still be useful.
  - b What data structure is used at instruction dispatch to determine the physical source registers for an instruction?
  - c How is the mapping from a thread’s logical to physical registers modified when a branch misprediction is discovered?
  - d How is the GCT (global completion table) affected when a thread suffers a branch misprediction?
  - e Physical registers are allocated dynamically. When are they allocated? What conditions determine when a physical register can be freed for re-allocation?
  - f The Power5 maintains a load reorder queue and a store re-order queue, to detect out-of-order execution hazards. When do you think this mechanism is used? Under what conditions would this mechanism delay execution of a load?

*The six parts carry, respectively, 20%, 10%, 10%, 10%, 35%, and 15% of the marks.*

- 2 This question requires access to the paper “IBM Power5 Chip: A Dual-core Multithreaded Processor” (IEEE Micro March-April 2004), which you should have available to you in the examination. Where the paper is incomplete, you are invited to speculate using your understanding of the underlying architectural principles.

This question concerns an alternative to the Power5 design philosophy (based loosely on the CELL POWERPC Processing Element). Assume, for the purposes of this question, the following architectural features:

- In-order, dual-issue pipeline
  - Integer pipeline with 11 stages
  - One fully-pipelined floating-point add/subtract unit
  - One fully-pipelined floating-point multiply unit
  - Two-way simultaneous multithreading (SMT)
  - L1, L2, L3 caches and memory system similar to Power5
  - A tournament branch predictor like the Power5's
  - Clock rate twice as fast as the Power5
- a Suggest a sensible structure for the integer pipeline. Explain briefly the function of each of the 11 stages. Take care to include how the branch predictor is accessed.
- b Identify *two* forwarding paths required to avoid unnecessary stalls in your pipeline.
- c Give three circumstances in which instruction issue might stall in this design.
- d This design supports two-way simultaneous multithreading. At which pipeline stage does this processor select between the two threads? What information is required to make this decision?
- e Outline briefly the characteristics of an application program that would run faster on the Power5 than on this design. Justify your answer carefully.

*The five parts carry, respectively, 45%, 15%, 20%, 10%, and 10% of the marks.*