

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING  
EXAMINATIONS 2008

EEE/ISE PART I: MEng, BEng and ACGI

**ANALOGUE ELECTRONICS 1**

Monday, 9 June 10:00 am

Corrected Copy  
*none*

Time allowed: 2:00 hours

There are FOUR questions on this paper.

Q1 is compulsory.

Answer Q1 and any two of questions 2-4.

Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s) :	A.S. Holmes, A.S. Holmes
	Second Marker(s) :	S. Lucyszyn, S. Lucyszyn

1. **This question is compulsory.** You should attempt all six parts. State clearly any assumptions made in your calculations.

- a) For the circuit in Figure 1.1, choose the value of  $R_B$  to give a voltage of +5 V at the collector of the transistor.

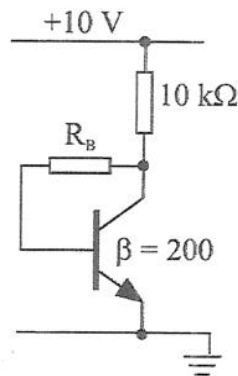


Figure 1.1

[6]

- b) For the circuit in Figure 1.2, determine the operating modes of both MOSFETs and the value of the current  $I$ . The MOSFETs are matched and have large signal parameters  $K = 0.2 \text{ mA/V}^2$  and  $V_t = 1 \text{ V}$ .

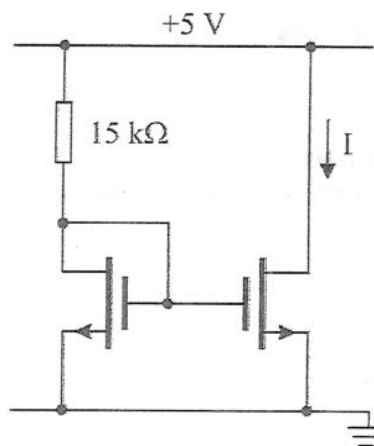


Figure 1.2

[8]

- c) Sketch the circuit for a Class B push-pull output stage, and explain why such a circuit exhibits cross-over distortion. To aid your explanation sketch the output waveform you would expect to see if the stage were driven by a sinusoidal signal of peak-to-peak amplitude 4 V.

[8]

Question 1 continues on the next page...

- d) For the Darlington pair shown in Figure 1.3, derive an expression for the overall current gain  $I_{OUT}/I_{IN}$  when both transistors are active, in terms of the individual transistor current gains  $\beta_1, \beta_2$ . Also state the maximum output current that the pair can deliver to the  $1\text{ k}\Omega$  load resistor.

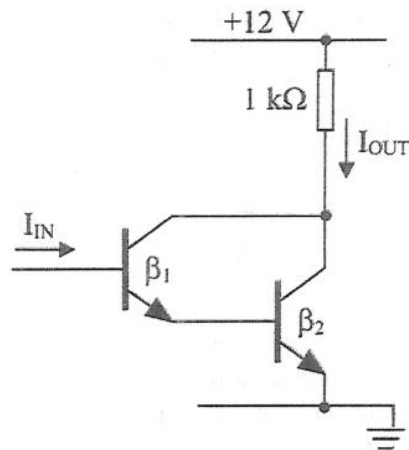


Figure 1.3

[6]

- e) For the circuit in Figure 1.4, determine the operating mode of the MOSFET and the value of the voltage  $V$ .

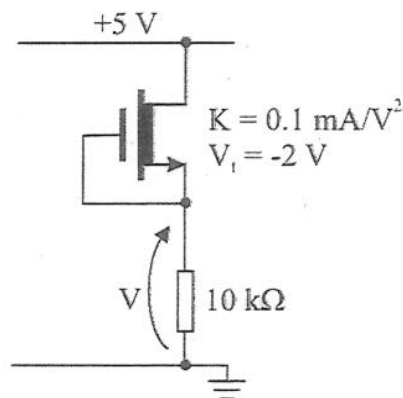


Figure 1.4

[6]

- f) The characteristic equation for a phase-shift oscillator is of the form:

$$(1 + K)u^3 + 6u^2 + 5u + 1 = 0$$

where  $K$  is the voltage gain of the amplifier, and  $u = sRC$ , with  $s$  being complex frequency and  $R, C$  being the component values in the phase-shifting network. Starting from this equation show that the amplifier gain required for stable oscillation is  $K = 29$ .

[6]

2. Figure 2.1 shows a common-emitter amplifier which is to be manufactured using transistors with a nominal  $\beta$  value of 200.

- a) Determine the quiescent output voltage and the collector bias current when  $\beta = 200$ , taking into account the base current of the transistor. Also evaluate the collector bias current in the cases  $\beta = 150$  and  $\beta = 250$ . Explain briefly why the bias conditions of this circuit are relatively insensitive to  $\beta$  variations. [10]
- b) Draw a small-signal equivalent circuit of the amplifier, and hence show that the voltage gain may be written as:

$$\frac{-\alpha R_C}{r_e + R_E}$$

where  $\alpha$  is the common-base current gain of the transistor, and  $r_e$  is its emitter resistance. Evaluate this expression assuming  $\beta = 200$ , and also determine the small-signal input and output resistances of the amplifier in this case. You may neglect the transistor's small-signal output resistance. [14]

- c) By what ratio would the mid-band voltage gain of the amplifier be increased if the emitter resistor  $R_E$  were bypassed using a capacitor? [6]

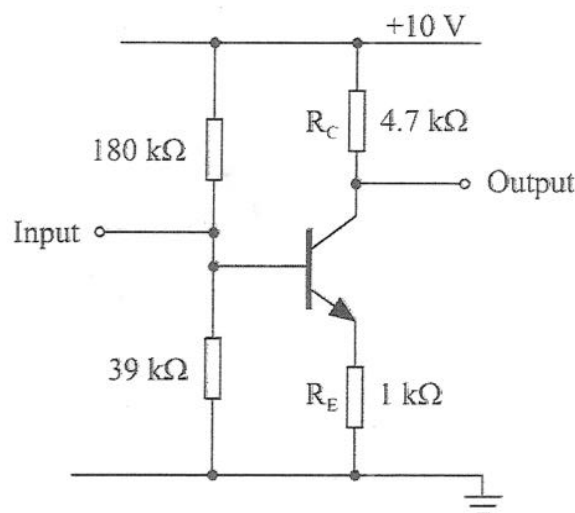


Figure 2.1

3. Figure 3.1 shows a single-stage CMOS amplifier in which a p-channel MOSFET provides the active load for an n-channel MOSFET. The active load is biased using an externally applied voltage  $V_G$ .

- a) Show that, provided both MOSFETs are active, the quiescent output voltage of the circuit is given by:

$$V_{OUT} = V_{t1} + \sqrt{\frac{K_2}{K_1}} \cdot (V_{DD} + V_{t2} - V_G)$$

where  $K$  and  $V_t$  are the usual MOSFET parameters, and the subscripts 1 and 2 refer to the lower and upper MOSFETs respectively.

Hence evaluate the value of  $V_{OUT}$  for the case  $V_G = +4$  V. Verify that both MOSFETs are indeed active under these bias conditions. [12]

- b) Draw a small-signal equivalent circuit of the amplifier, including the  $10\text{ M}\Omega$  resistor, and hence determine the small-signal voltage gain of the amplifier when  $V_G = +4$  V. Also calculate the input resistance of the circuit. You may assume the input capacitor is effectively short-circuit at signal frequencies. [14]

- c) Explain briefly why a smaller voltage gain would be obtained if the upper MOSFET were replaced by a passive resistive load. [4]

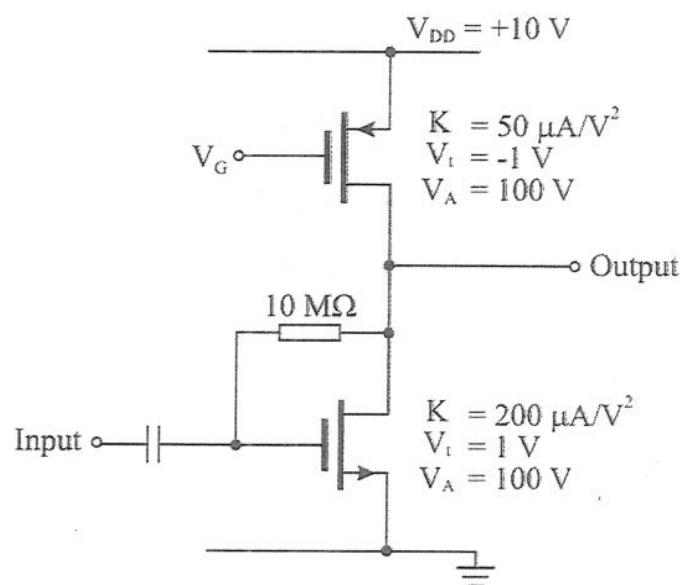


Figure 3.1

4. Figure 4.1 shows a simple differential amplifier. The two transistors are matched, each with  $\beta = 200$ , and you may assume that they have infinite small-signal output resistance.

a) Taking base currents into account, calculate the tail current  $I$  and the output voltage  $V_{OUT}$  when  $V_{IN1} = V_{IN2} = 0$ . Repeat your calculation for the case  $V_{IN1} = V_{IN2} = -2$  V. [10]

b) Draw a small-signal equivalent circuit and, by considering the response to a purely differential input signal (i.e. one with zero common mode signal voltage), derive an expression for the single-ended differential voltage gain  $A_d$ .

In light of your answer to part a), would you expect  $A_d$  to vary with the common mode input voltage? [12]

c) Calculate the common mode voltage gain of the amplifier, and suggest one method by which this could be reduced. [8]

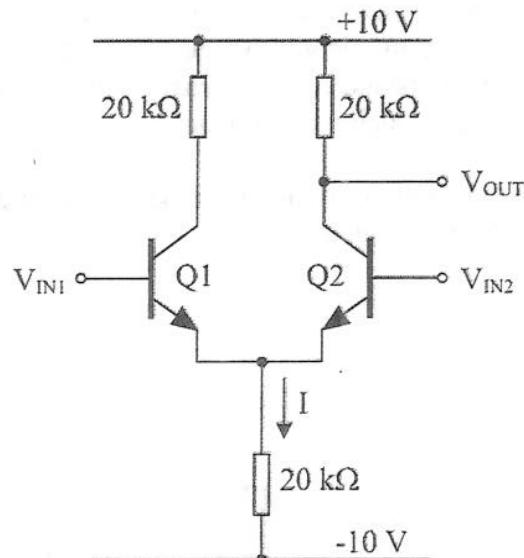


Figure 4.1