EJ.11/E4.42/A08

2008

Answers

1. **Compulsory.**

a) n-type [4]

b) 1. the workfunction of the polySi gate can be changed via doping such that polySi can be used for both n and pMOS.
2. polySi can withstand high temperatures and thus a self-aligned ohmic contact process can be implemented. [4]

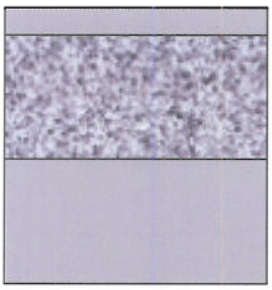
c) The threshold voltage is the voltage that needs to be applied on the gate such that the density of inverted carriers (opposite to those in the bulk) near the Si/SiO_2 interface is equal to the density of carriers in the bulk. [4]

d) No, a current flows that is exponentially dependent on gate voltage. The sub-threshold current is the result of carrier diffusion as the density of carriers at the source is higher than the density of carriers near the drain. In other words in sub-threshold the MOSFET behaves as a BJT where the base-emitter voltage is replaced by the gate voltage that is divided between the oxide and bulk capacitance. [4]

e) Two of the following
1. gives a better control of the effective gate length
2. gives a reduced overlap capacitance
3. reduces the electric field at the drain side and thus controls short channel effects

[4]

f) [4]

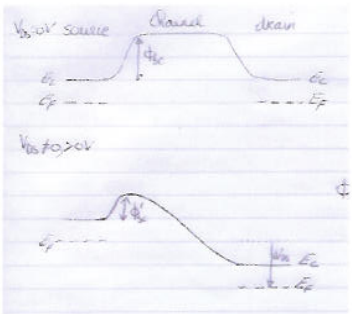


Si film - crystalline

SiO_2 buried oxide layer BOX

Si substrate

g) DIBL gives a measure of the influence of the drain voltage on the threshold voltage. The drain voltage lowers the source channel potential barrier ϕ_{sc} to ϕ'_{sc}. [4]



h) To remove the doping atoms from the channel region and as such cancel impurity scattering and increase mobility of the carriers in the channel. It also ensures that the carrier density is sufficiently high as carrier transfer happens from the doped layer into the channel layer. [4]

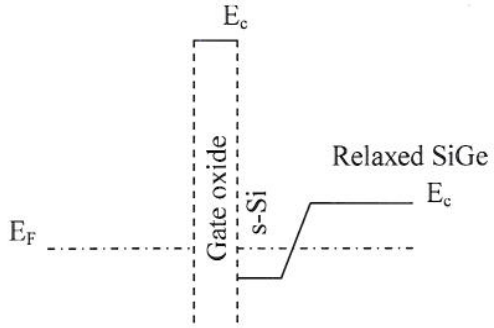
i) It increases the control of the combined gates on the carrier density in the channel and combats the influence of the drain voltage on the carrier density. It controls DIBL. A double gate FET will also generate twice the current drive as two channels can be generated. [4]

j) A GaAs MESFET has a schottky gate. A schottky contact is a rectifying contact and thus will conduct current in forward bias. This would result in high gate leakage currents that are unacceptable. [4]

2.

a) Introducing tensile strain will increase the carrier mobility of the electrons in the channel. [2]

b) Since $V_{th}<0V$ the device is depletion mode and thus there are carriers in the channel, thus EF must lie above the bottom of the conduction band in the s-Si quantum well. Since there is no workfunction difference between gate and channel we have flat band condition when no voltage is applied (assumes an ideal oxide) [4]



c)

i) Triode region: $V_{th}^{lin} \approx 0.29V$ (via tangential in V_{GS} where gm is max)
Saturation region: $V_{th}^{sat} \approx 0.2V$ (via extrapolation of linear part of $\sqrt{I_{DS}}$) [8]

ii) $$DIBL = \left|\frac{V_{th}^{lin} - V_{th}^{sat}}{V_{DS}^{lin} - V_{DS}^{sat}}\right| \approx \left|\frac{0.29V - 0.2V}{0.1V - 1V}\right| = 100mV/V$$ [2]

iii) From triode region transfer characteristic we find
$I_{DS}^{lin} = \frac{\mu C_{ox} W}{L}(V_{GS} - V_{th})V_{DS}$. Thus the transconductance takes the form:

$$g_m = \frac{dI_{DS}^{lin}}{dV_{GS}} = \frac{\mu C_{ox} W}{L} V_{DS} = \frac{\mu \varepsilon_0 \varepsilon_{ox} W}{L t_{ox}} V_{DS} \text{ and}$$

$$\mu^{\max} = \left(\frac{\varepsilon_0 \varepsilon_{ox} W}{L t_{ox}} V_{DS}\right)^{-1} g_m^{\max} = \frac{0.5\times10^{-4} \times 4\times10^{-7} cm^2 \times 7.5\times10^{-4} S}{8.85\times10^{-14} F/cm \times 4\times5\times10^{-3} cm \times 0.1V} \approx 85 cm^2/Vs$$

[4]

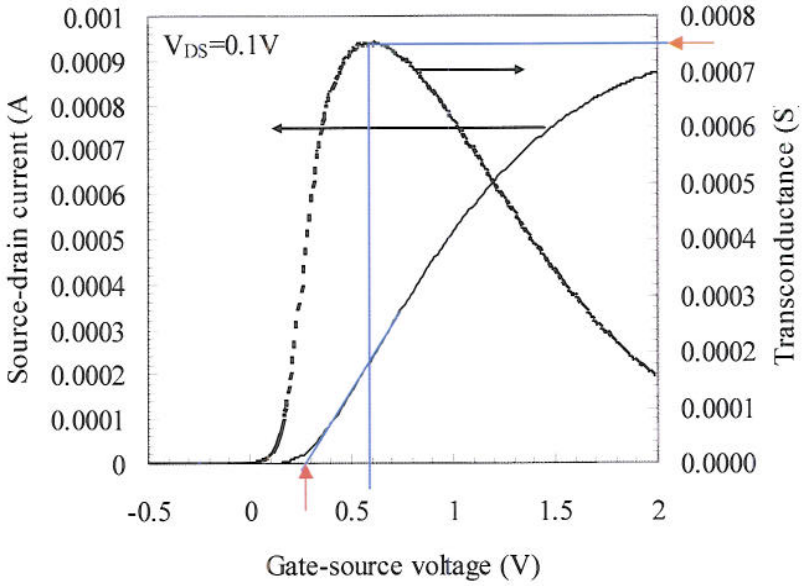


Figure 2.2 a): The transfer characteristic I_{DS}-V_{GS} of the s-Si MOSFET in the triode region and the transconductance g_m. g_m in bold dashed line.

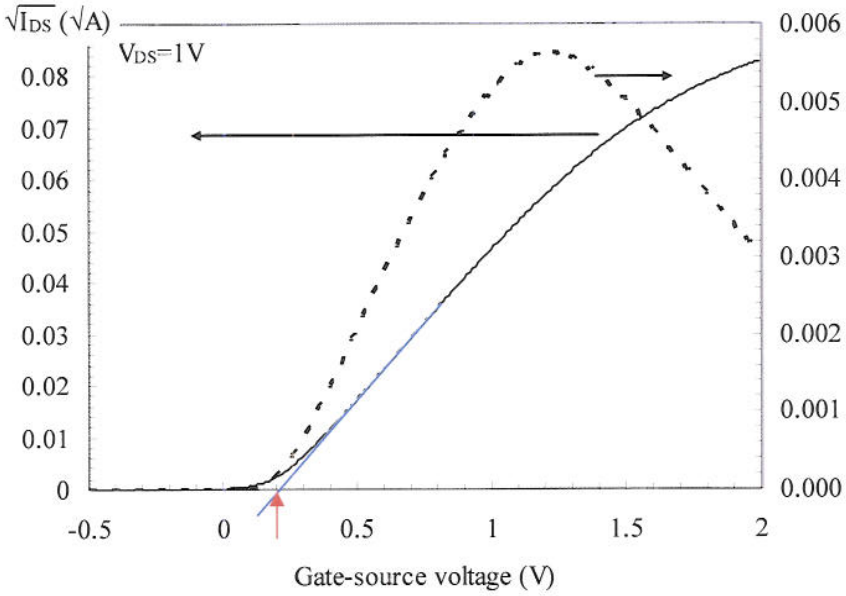
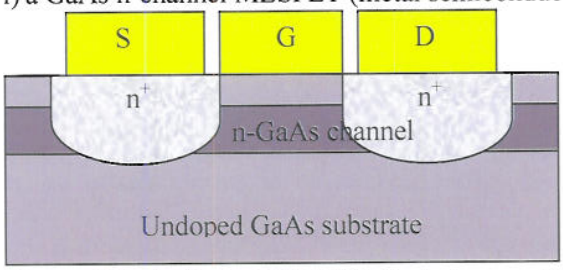


Figure 2.2 b): The square root of the source-drain current $\sqrt{I_{DS}}$ as a function of gate voltage V_{GS} of the s-Si MOSFET in the saturation region and the transconductance g_m. g_m in bold dashed line.

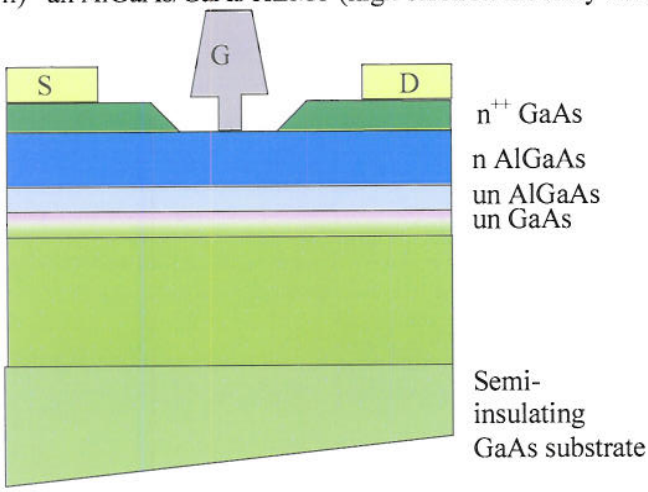
3.

a)

i) a GaAs n-channel MESFET (metal semiconductor field effect transistor). [2]



ii) an AlGaAs/GaAs HEMT (high electron mobility transistor). [4]



b)

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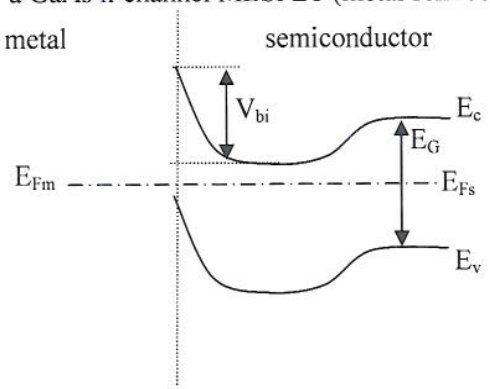

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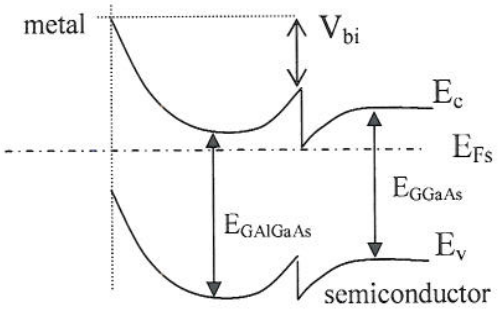
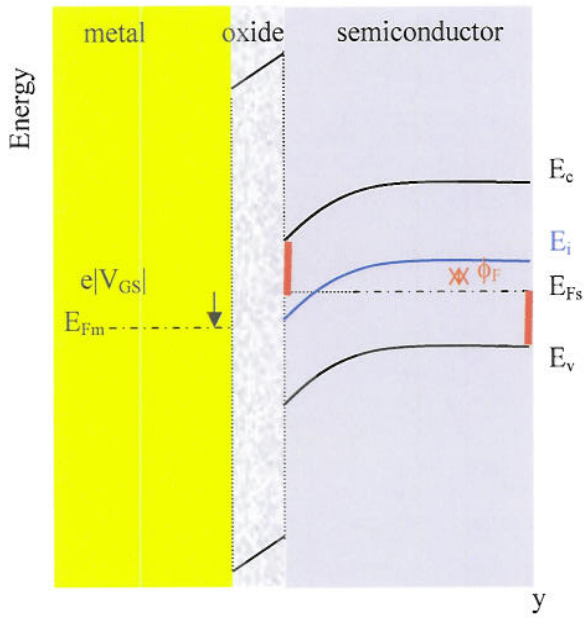


c) This is the result of interface states. Interface states cause energy levels to occur in the bandgap of the semiconductor at the interface. These states are characterised by a neutral level equivalent to the Fermi level. Thus the neutral level is dependent on the interface state density. At contact the Fermi level in the semiconductor will align to the neutral level of the interface states and thus V_{bi} is determined by the interface state density. [3]

d) The threshold voltage V_{th} in HEMTs is dependent on the conduction band offset ΔE_c between the GaAs and the $Al_xGa_{1-x}As$. $\Delta E_c \approx 0.6\ \Delta E_G$ in this system. Or ΔE_c increases with increasing difference in energy gap between GaAs and $Al_xGa_{1-x}As$. The energy gap in $Al_xGa_{1-x}As$ can be approximated by: $E_G^{AlGaAs}(x) = xE_G^{AlAs} + (1-x)E_G^{GaAs}$ or the bandgap of $Al_xGa_{1-x}As$ increases with increasing x. Thus the conduction band offset for $Al_{0.5}Ga_{0.5}As$ is larger than for $Al_{0.3}Ga_{0.7}As$ and thus the quantum well will be deeper for x=0.5 and therefore V_{th} will be smaller for x=0.5. [3]

4.

a) [4]



b) $V_s = 2\phi_F$ at $V_{GS} = V_{th}$ [4]

c) $V_{GS} = V_{ox} + V_s$. [2]

d) [6]

$Q_G + Q_I + Q_{depl} = 0$ charge neutrality ignoring any charge in oxide

$Q_G = C_{ox}V_{ox}$ is the charge on the gate

Q_I is the charge in the inversion layer. Is small at $V_{GS}=V_{th}$.

Q_{depl} is the depletion layer charge in the maximum depletion width.

e) At threshold the surface potential is $V_s = 2\phi_F$ and $V_{GS}=V_{th}$

$Q_I << Q_{depl}$

$$Q_G + Q_{depl} \approx 0 \rightarrow Q_G \approx -Q_{depl}$$

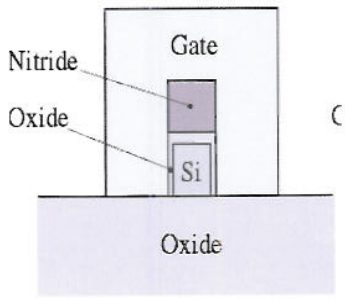
$$Q_G = C_{ox}V_{ox} \rightarrow V_{ox} = \frac{Q_G}{C_{ox}} \approx \frac{-Q_{depl}}{C_{ox}}$$

$$V_{th} = V_{ox} + V_s \approx \frac{-Q_{depl}}{C_{ox}} + 2\phi_F$$

[4]

5.

a)

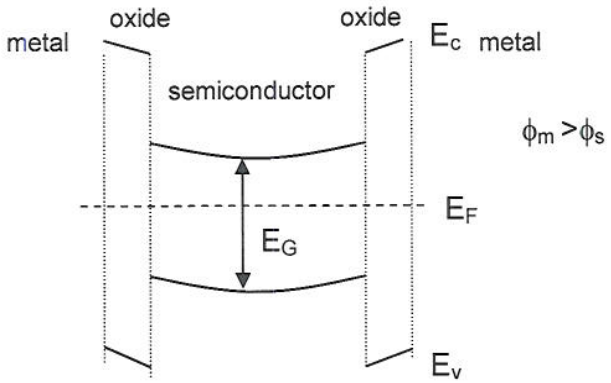


Double-Gate [4]

b) 2 [2]

c) 3 [2]

d) [4]



e) Start from reasoning:
Subthreshold slope is defined in weak inversion. In that region the current is exponential as in a BJT and is determined via the capacitive gate voltage division between the oxide C_{ox} and bulk C_B capacitance. Since the body in a finFET is thin C_B is very small and C_{ox} is 2× that of a single gate device. Thus $C_B << 2C_{ox}$ and the weak inversion current is $I = I_s \exp(eV_{GS}/kT)$. $S = \left(\frac{d\log(I_{DS})}{dV_{GS}}\right)^{-1} \rightarrow$

$S = \ln(10)\frac{kT}{e} \approx 60mV/dec$ at T=300K.

Start from memorised expression of S:

$S = \ln(10)\frac{kT}{e}\left(1+\frac{C_B}{C_{ox}}\right)$. $C_{ox} >> CB$ see above thus $S = \ln(10)\frac{kT}{e}$. [4]

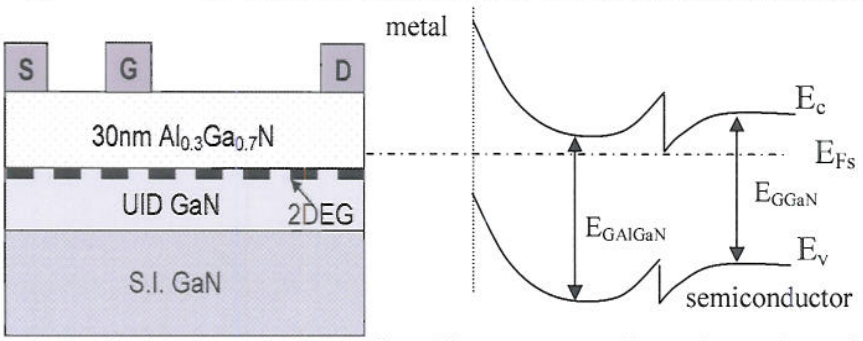
f) DIBL is caused by the capacitive coupling of the channel with the drain that is taking over the capacitive control of the channel by the gate. In a finFET we have two gates and a narrow region for control by these gates and therefore the combined capacitive control of the two gates becomes more important than the drain. [4]

6. Essay based on coursework research.

One of the following two subjects/questions can be chosen to write an essay:

a) Essential ingredients in the answer are:
Due to microscopic instabilities the 2DEG (electrons in the channel of the FET) behave like a plasma. This is a longitudinal wave with periodic regions of high and low electron density. The velocity of the 2DEG plasma is a lot larger than the drift velocity of the electrons in the plasma and can be of the order of THz. A coupling between impinging THz and this plasma generates a DC output at the drain of a FET configuration with an antenna input and an open output.
Improving the detector efficiency can be done by making FETs with high electron mobilities and long momentum scattering times (thus few scattering events). Additionally the coupling between THz wave and 2DEG plasma can be improved by e.g. the correct antenna design or by arrays of FETs.
Most of the current THz detectors are bulky or can only be operated at low temperatures. The FET approach allows large integration possibilities and might be operational at room temperature.

b) Essential ingredients in the answer are:
GaN is a wide bandgap material with high carrier mobility and one can make this material into heterojunctions to form e.g. modulation doped structures. As a consequence GaN is useful for high power and high speed applications.
A typical AlGaN/GaN structure is given below. The energy band structure is as a typical HEMT.



In the beginning these devices suffered from current collapse due to the surface and bulk states. This was ameliorated by two improvements: 1) deposition of a dielectricum over the surface and underneath the metal gate and 2) the field plate. The insulator reduces surface currents and the influence of surface states and the function of the field plate is to modify the electric field profiles and decrease its peak value as thus reducing the trapping and increasing the breakdown voltage. Moreover GaN is a direct bandgap material that allows emission of light. GaN makes a whole range of ternary alloys that span a wide direct bandgap range and can thus be made into lasers and LED over a wide wavelength range including blue and white light. The latter would mean that light bulbs could be replaced by low power semiconductors reducing energy consumption dramatically.

[20]