Question 1

1. a) (i)

$$A + \overline{A}B = (A + A.B) + \overline{A}.B = A + B\left(A + \overline{A}\right) = A + B$$

[4]

(ii)

$$\begin{aligned}\overline{A}BC + \overline{\overline{AB} + \overline{AC}} &= \overline{A}BC + \overline{AB}.\overline{AC} \\ &= \overline{A}BC + \left(\overline{A} + \overline{B}\right)\left(\overline{A} + \overline{C}\right) \\ &= \overline{A}BC + \overline{A} + \overline{A}.\overline{C} + \overline{A}.\overline{B} + \overline{B}.\overline{C} \\ &= \overline{A} + \overline{A}.\overline{C} + \overline{A}.\overline{B} + \overline{B}.\overline{C} \\ &= \overline{A} + \overline{B}.\overline{C}\end{aligned}$$

[4]

b) (i)

AB \ CD	00	01	11	10
00	0	1	x	1
01	0	x	x	x
11	0	x	x	x
10	1	0	1	0

$$f = CD + \overline{A}D + \overline{A}C + A\overline{B}\overline{C}\overline{D}$$

Here, 1 mark for the Karnaugh map with the correct values, 1 for the grouping in the map, and 2 for the SOP final expression.

[4]

(ii)

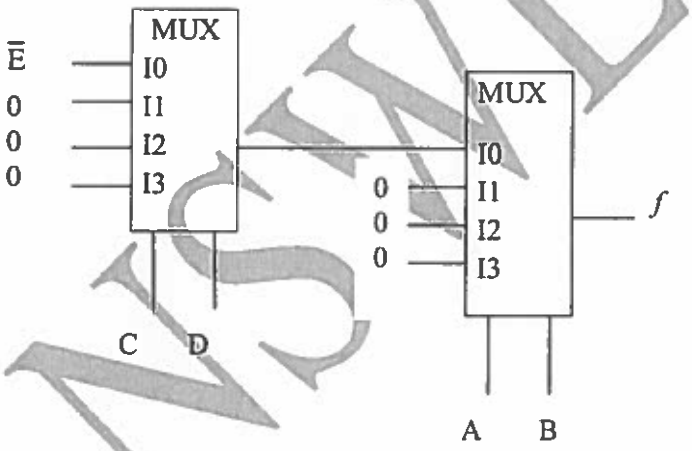
AB \ CD	00	01	11	10
00	0	1	x	1
01	0	x	x	x
11	0	x	x	x
10	1	0	1	0

$$f = \left(\overline{B}\right)\left(\overline{A}+C+\overline{D}\right)\left(\overline{A}+\overline{C}+D\right)\left(A+C+D\right)$$

Here, 1 mark for the grouping in the map, and 2 for the SOP final expression.

[3]

c)



Here,

$$f = \overline{ECD\left(\overline{AB}\right)} = \overline{\overline{ABCDE}}$$

$$= \overline{\left(\overline{ABCDE}\right)} = \overline{A+B+C+D+E}$$

Give 1 mark for understanding the type of multiplexer needed, i.e. a 4 x 1 multiplexer, 2 marks for the connections, and 2 marks for showing why this creates a NOR gate.

[5]

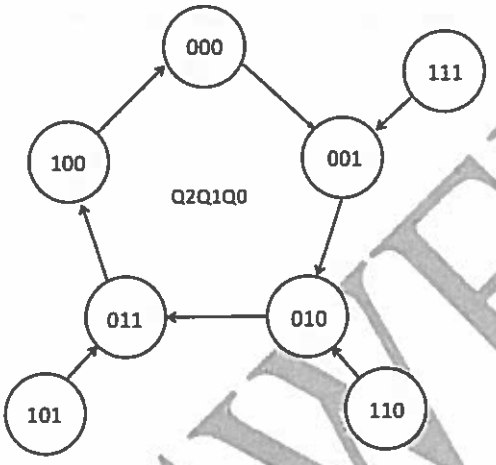
d)

Decimal	Hexadecimal	Signed binary (8 bits wide)	Octal
256			400
-15		1111 0001	
	195		625

Give 2 marks per answer.

[6]

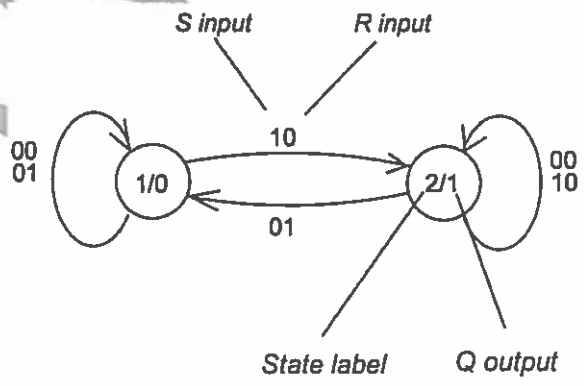
e)



Give 2 marks for the correct number of states, 2 marks for the correct labels, and 2 marks for the correct interconnections.

[6]

f) (i) The state diagram for the SR flip-flop is as follows:



1 mark for states, 1 mark for interconnections, and 2 for labelling.

[4]

(ii) To find the characteristic Boolean equations for the flip-flop, we first draw the assigned state table from the state diagram:

Present Output	Next output inputs: SR			
	00	01	11	10
0	0	0	X	1
1	1	0	X	1

Re-drawing this as a Karnaugh map for next state output Q^+, with inputs Q (the present state), S and R:

Q\SR	00	01	11	10
0	0	0	X	1
1	1	0	X	1

The Karnaugh map gives the following Boolean equations:

$$Q^+ = Q\bar{R} + S \qquad \overline{Q^+} = \bar{Q}\bar{S} + R$$

1 mark each for the assigned state table and Karnaugh map, and 1 mark each for the Boolean equation.

[4]

Question 2

(a) (i) Odd parity implies that the count of 1's in the binary number PABCD is an odd number. The value of P must then be adjusted, depending on the count of 1s in ABCD. Including the requirement in the question that for all input low the output is high (this information, while not necessary, is to help the candidate), implies the following truth table:

A	B	C	D	P
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

This give the following Karnaugh map and Boolean expression:

AB \ CD	00	01	11	10
00	1	0	1	0
01	0	1	0	1
11	1	0	1	0
10	0	1	0	1

No grouping is possible, giving the following SOP expression:

$$P = \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}CD + \overline{A}B\overline{C}D + \overline{A}BC\overline{D} + A\overline{B}\overline{C}\overline{D} + ABCD + A\overline{B}CD + A\overline{B}C\overline{D}$$

Here, give 1 marks for showing an understanding of parity, 2 marks for the truth table and/or the Karnaugh map (done separately, or with the later written directly), and 1 mark for the SOP Boolean expression.

[4]

(ii) Conversion to an expression with only XNOR gates requires spotting both XNOR and XOR term in the Boolean expression for (i), which can then be rearranged as XNOR gates only (this can be tricky). It is possible to build up the required expressions as follows:

Exp. 1: $\overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}CD = \overline{A}\overline{B}\left(\overline{C}\overline{D} + CD\right) = \overline{A}\overline{B}\left(\overline{C \oplus D}\right)$

Exp. 2: $A\overline{B}\overline{C}\overline{D} + AB\overline{C}D = A\overline{B}\left(\overline{C}\overline{D} + CD\right) = A\overline{B}\left(\overline{C \oplus D}\right)$

Exp. 3: $\overline{A}\overline{B}CD + \overline{A}BC\overline{D} = \overline{A}B\left(\overline{C}D + C\overline{D}\right) = \overline{A}B\left(C \oplus D\right)$

Exp. 4: $A\overline{B}\overline{C}D + A\overline{B}C\overline{D} = A\overline{B}\left(\overline{C}D + C\overline{D}\right) = A\overline{B}\left(C \oplus D\right)$

We can then combine Exp. 1 and 2, and Exp. 3 and 4, to build the required expression for P, with three two-input XNOR gates, as follows:

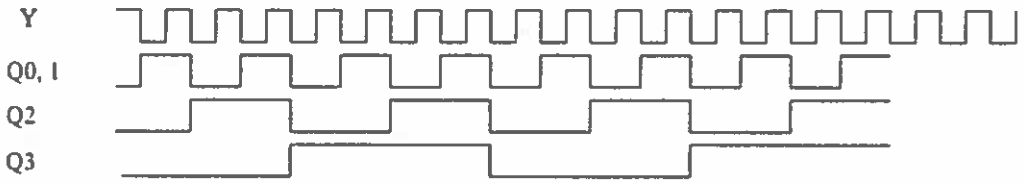
$$P = \overline{A}\overline{B}\left(\overline{C \oplus D}\right) + A\overline{B}\left(\overline{C \oplus D}\right) + \overline{A}B\left(C \oplus D\right) + A\overline{B}\left(C \oplus D\right)$$
$$= \left(\overline{C \oplus D}\right)\left(\overline{A}\overline{B} + AB\right) + \left(C \oplus D\right)\left(\overline{A}B + A\overline{B}\right)$$
$$= \left(\overline{C \oplus D}\right)\left(\overline{A \oplus B}\right) + \left(C \oplus D\right)\left(A \oplus B\right)$$
$$= \left(\overline{C \oplus D}\right)\left(\overline{A \oplus B}\right) + \overline{\left(C \oplus D\right)\left(A \oplus B\right)}$$
$$= \overline{\left(\overline{C \oplus D}\right) \oplus \left(A \oplus B\right)}$$

Give 4 marks for the Exps. 1 – 4, and 2 marks for the final transformation. Students may also approach this question if they already know the XNOR circuit for an odd parity generator, then work out the SOP expression from this and show that this is the same as in (i). This approach is fine as well.

[6]

b)

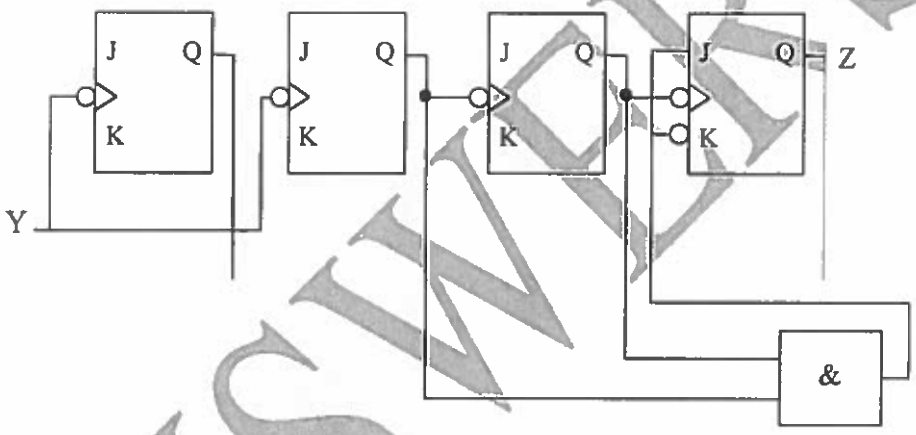
(i)



Give 1 mark per waveform for Q0 – Q3.

[4]

(ii)



Here, 2 marks for seeing that an AND gate is needed to trigger *Z*, 2 marks for seeing that this triggers on the negative clock edge after Q1 = Q2 = 1, and 2 marks for the connections.

[6]

(c) (i) A signed, two's complement, four bit number can be used to express the decimal range -8 to +7. Hence, multiplication by 5 implies that the answer lies in the range -40 to +35. Here, the negative range (up to -40) requires the greater number of bits. To express -40 in two's complement binary requires N = 7 bits. This would give the range -64 to +63, sufficient to accommodate -40 to 35. In contrast, 6 bit would only give the range -32 to +31, which is insufficient.

Give 2 marks for determining the range for a four-bit number, and 2 for finding the value of N.

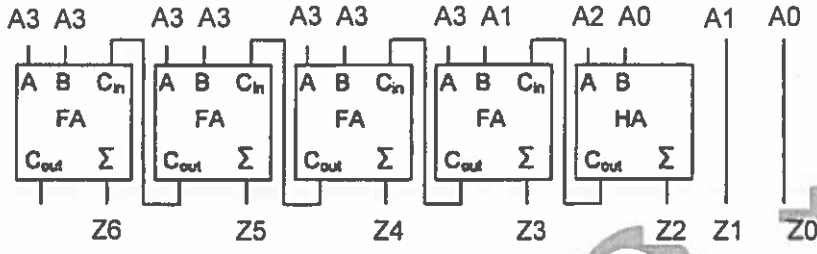
[4]

(ii) Multiplication of A by 5, correspond to 5A = (4A add A) = (2^2A add A). The first term is a left shift of A by two places and the second term is an addition of A to the shifted number. Using sign-extension to 7 bits, this gives the following addition:

A3 A3 A3 A3 A2 A1 A0 (sign extended version of 'A')
A3 A3 A2 A1 A0 0 0 ('A' left shifted by two places)

Give 1 mark for the sign extension, 1 marks for the correct shift, and 1 mark for the order of addition.

Here the first two column additions are just A1 and A0, and the remaining are with the bits as shown. This allows the construction of the following circuit:

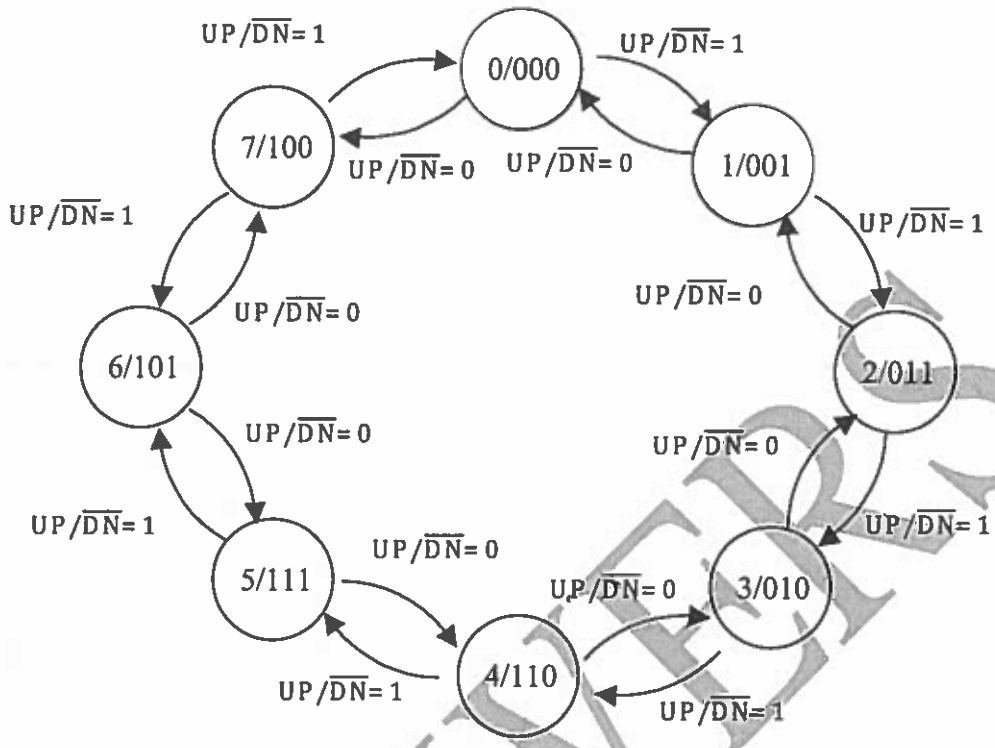


Give 3 marks for the circuit.

[6]

Question 3

3. a) i) Using states Q2Q1Q0 to define the FSM:



Give 2 marks for the grey code sequence, 2 marks for the eight states, 2 for labelling and 2 for correct interconnections.

[8]

b) Using Q2Q1Q0 as the present state of the FSM, and $Q2^{+}Q1^{+}Q0^{+}$ as the next state:

Present State			Next State					
			UP/$\overline{DN}$= 0			UP/$\overline{DN}$= 1		
Q2	Q1	Q0	Q2+	Q1+	Q0+	Q2+	Q1+	Q0+
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	1
0	1	1	0	0	1	0	1	0
0	1	0	0	1	1	1	1	0
1	1	0	0	1	0	1	1	1
1	1	1	1	1	0	1	0	1
1	0	1	1	1	1	1	0	0
1	0	0	1	0	1	0	0	0

Give 1 mark for each correct row of the table.

[8]

c)

The FSM can be implemented using three D flip-flops, one each to store Q2, Q1 and Q0. Using the state transition table in (b), it is possible to fill out Karnaugh maps for each D flip-flop input, D0 – D2. In the following, we indicate $UP / \overline{DN} = Y$.

For D2:

D2

Q2,Q1 \ Q0,Y	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	1	1	1
10	1	0	1	1

$$D_2 = \overline{Q_1}.\overline{Q_0}.\overline{Y} + Q_1.\overline{Q_0}.Y + Q_2.Q_0$$

For D1:

D1

Q2,Q1 \ Q0,Y	00	01	11	10
00	0	0	1	0
01	1	1	1	0
11	1	1	0	1
10	0	0	0	1

$$D_1 = Q_2.Q_0.\overline{Y} + \overline{Q_2}.Q_0.Y + Q_1.\overline{Q_0}$$

For D0

D0

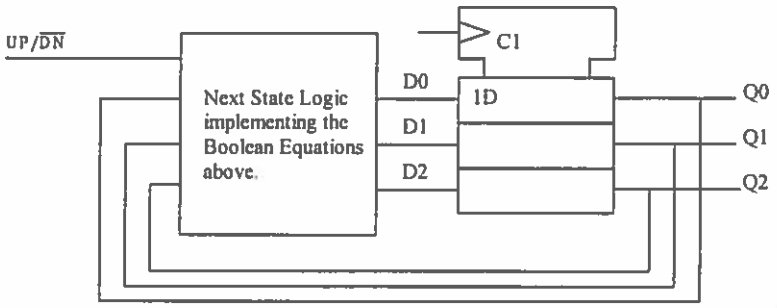
Q2,Q1 \ Q0,Y	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	0	1	1	0
10	1	0	0	1

$$D_0 = Q_2.Q_1.Y + \overline{Q_2}.\overline{Q_1}.Y + Q_2.\overline{Q_1}.\overline{Y} + \overline{Q_2}.Q_1.\overline{Y}$$

Give 1 marks for identifying the correct four inputs, 2 marks for each Karnaugh map, and, 1 mark for each Boolean expression.

[10]

d)



Give 1 mark for indicating three D flip-flops, and 3 marks for the interconnection scheme. Note that the diagram above does not show the Boolean expressions for D0 – D2, which are as in (c) above.

[4]