EE4-53
EE9-FPN1-02

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2016

EEE PART IV: MEng and ACGI

Corrected copy

HVDC TECHNOLOGY AND CONTROL

Wednesday, 4 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer 2 questions from Part A and 2 questions from Part B. Use a separate answer book for each section.

All questions carry equal marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : B. Chaudhuri, M Merlin
Second Marker(s) : B.C. Pal,

Part A: Answer any 2 questions out of 3 from this part

1. a) Sketch the equivalent circuit of a point-to-point LCC HVDC link and explain what each component on either side represents.

[5]

b) Explain the problem of consequent commutation failure (or further commutation failure) and state how it can be minimised during operation and also at the design level.

[5]

c) Explain, with the help of the rectifier and inverter control characteristics, how the power reversal is executed in a LCC HVDC link.

[5]

d) One end of a planned LCC HVDC link is to be connected at a 400 kV substation where the equivalent system impedance is 7.19 Ω. What should be the maximum rated capacity (in GW) of the HVDC link to ensure safe operation without the need for any fast voltage compensation? Assume that the reactive power consumption of the LCC is 55% of active power under the rated condition and an effective short-circuit ratio (ESCR) of 5 or more is required for safe operation.

[5]

2. a) State what is the voltage-dependant current order limit (VDCOL) and why is it necessary for LCC HVDC control? Sketch the converter control characteristics including VDCOL and explain its operation.

[5]

b) Explain the typical sequence of events following a fault within the AC system at the rectifier side of a LCC HVDC link. Assume appropriate control duty at both ends under the pre-fault condition.

[5]

c) Two separate 400 kV AC systems are interconnected by a 500 kV, 1.2 GW monopolar LCC HVDC link. The resistance of the DC line is 4 Ω and the commutation resistances at the rectifier and inverter ends are 6 Ω and 8 Ω, respectively. The minimum limit on the firing angle (α) is 4°. Under the normal condition with the rated voltage at the rectifier end, the link carries the rated current and operates with a firing angle (α) of 15°, extinction advance angle (γ) of 20° and 10% current margin. Due to a load event the rectifier side AC system voltage reduces to 85% of its normal value. Calculate the following under this reduced voltage condition. You may neglect the transformer tap changer action and activation of VDCOL.

(i) Reactive power consumption of the rectifier.

[6]

(ii) Reactive power consumption of the inverter.

[4]

3. a) Explain the variation of the reactive power consumed by the converter of a LCC HVDC link as the firing angle (α) is varied over the entire range covering the rectifier and the inverter operation. You may neglect the commutation overlap (μ).

[4]

b) Explain the need for control mode stabilisation and state how it is usually achieved for control of LCC HVDC.

[5]

c) State why one of the converter transformers used within a pole of a bipole LCC HVDC link use a star-delta (Y-Δ) configuration.

[3]

d) A 1000 kV, 2.5 GW monopolar LCC-HVDC link is made up of 6-pulse converter bridges at both ends. The capacitor and filter banks installed at the inverter end of the link can provide reactive power support up to 60% of the rated active power of the link under normal AC system voltage. The DC line resistance is 5 Ω and the commutation resistance at either end is 4 Ω. The margin current setting is 8%. Calculate the maximum allowable extinction advance angle (γ) (in degrees) so that the reactive power demand of the inverter can be met locally by the capacitor and filter banks under the following conditions. Assume that the rated DC voltage is at the rectifier side and neglect any switching of capacitor and filter banks. Also assume that the inverter is in the current control mode under both conditions and maintains the same direct current. Consider appropriate reduction in reactive support due to reduction in AC system voltage at the inverter side.

(i) Rated power flow condition with normal AC system voltage at both ends.

[5]

(ii) Rated power flow condition but when the AC system voltage at the inverter end is 75% of that under normal condition.

[3]

Part B: Answer any 2 questions out of 3 from this part

4. Voltage Source Converters

a) Detail the main parts of a converter station, explaining their main purposes. Explain how these parts have changed between Voltage Source Converters (VSC) and Current Source Converters (CSC) and why. [3]

b) Using the electrical diagram of the ±200 kV DC multilevel Flying Capacitor converter depicted in Figure 4.1, complete the table using the format and example given below in order to answer this following questions:

i) What are the possible AC voltage levels? [2]

ii) How many individual capacitors are conducting the AC current? [3]

iii) What are the corresponding combinations of activated switches? [3]

iv) Assuming that the AC current sign is positive, which semiconductor devices between the Diodes (Dx) and the Transistors (Tx) are carrying the current? [2]

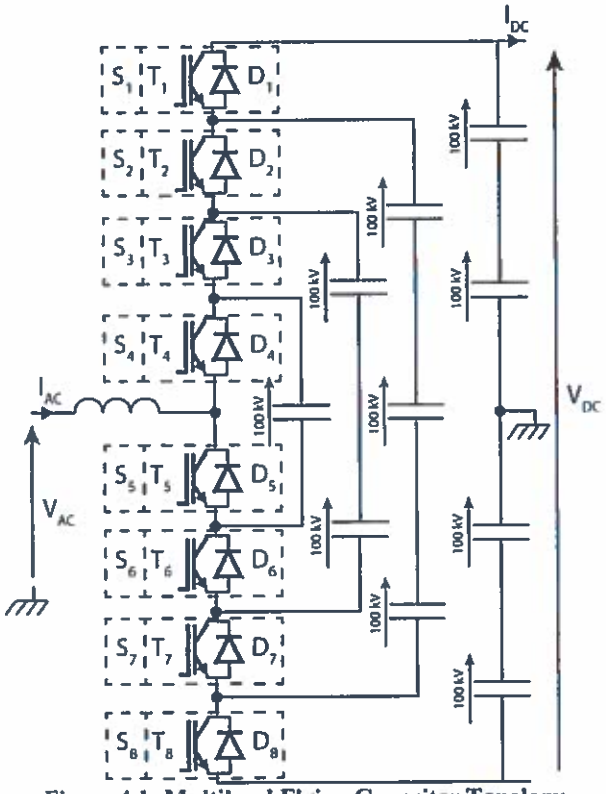

Figure 4.1: Multilevel Flying Capacitor Topology

Voltage Levels	Conducting Capacitors	Switch Combinations	Conduction Devices
0 kV	4	S1, S2, S5, S6	D1, D2, T5, T6
…	…	…	…

c) Explain the reasons for the Flying Capacitor (FC) topology to be more suitable to use when the number of voltage levels is greater than 3 when compared to the Neutral Point Clamped (NPC) topology.

[3]

d) Explain, through a diagram, the components and operation of a full solid state DC circuit breaker. Comment on its strength and weaknesses.

[4]

5. Modular Multilevel Converter

a) For an MMC, explain the following:

(i) The importance of the energy balancing.

[2]

(ii) The difference between the horizontal and vertical energy balancing.

[3]

b) A 800 MW MMC is connected to the latest DC cable technology rated a ±350 kV. Assuming that each half-bridge submodule is rated at 1.4 kV:

(i) Compute a device count for the following: the number of IGBT modules, submodule capacitors.

[3]

(ii) Estimate the minimal capacitance of the cell capacitors assuming that their voltage has to be kept within ±5% of their nominal value and the maximum peak-to-peak energy deviation of a stack is 1.700 MJ for the specified operating envelope of this converter.

[3]

(iii) Calculate the total capacitive energy stored per unit power (provide the answer in kJ/MVA).

[3]

c) What are the motivations behind using mixed stacks in the MMC?

[6]

6. Hybrid Voltage Source Converter

a) Using the general converter diagram shown in Figure 6.1:

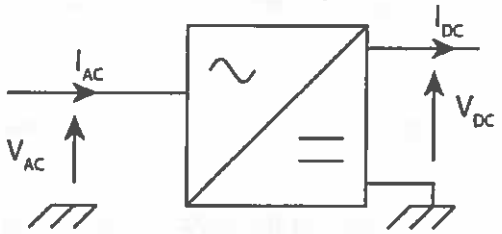

Figure 6.1: Alternate Arm Converter (AAC)

(i) Explain how the AC and DC quantities are related (assuming no power losses). [2]

(ii) Furthermore, if the converter consists of stacks of submodules, what is the main operating principle which needs to be observed to ensure the proper operation of the converter? [3]

b) Consider the rudimentary converter made of 3 stacks as illustrated in Figure 6.2. The AC and DC quantities can be expressed by following equations:

$$V_{AC}(t) = V_{AC}\sin(\omega t)$$
$$I_{AC}(t) = I_{AC}\sin(\omega t)$$
$$V_{DC}(t) = V_{DC}$$
$$I_{DC}(t) = I_{DC}$$

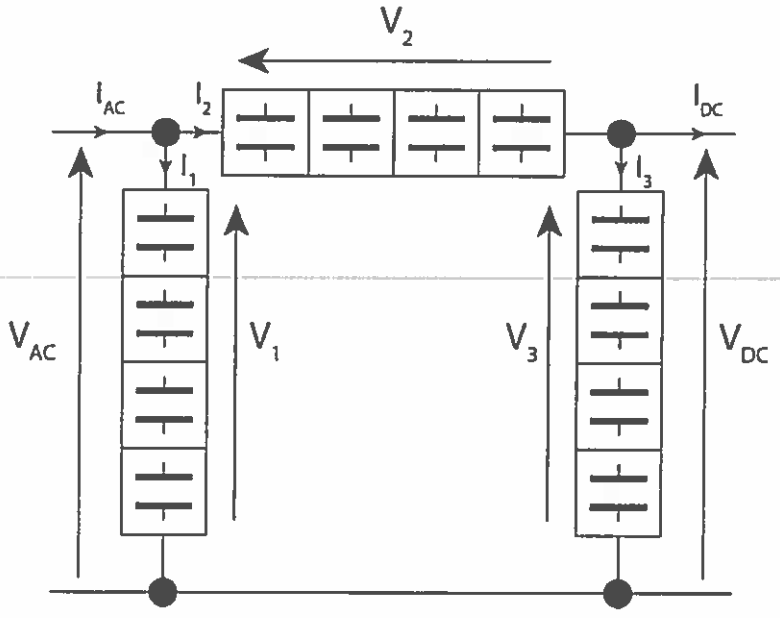

Figure 6.2: AAC as STATCOM

i) Derive the voltage waveform equations ($V_1(t)$, $V_2(t)$, $V_3(t)$) for Stacks 1, 2 and 3.
[3]

ii) If $V_{AC} = k \times V_{DC}$, state the maximum and minimum voltage characteristics of these stacks.
[3]

iii) Infer what type of submodules can be used in order to minimize the power losses.
[3]

iv) State the expression for the current waveforms in stacks 1, 2 and 3 to ensure proper operation of the converter? Justify your answers.
[6]