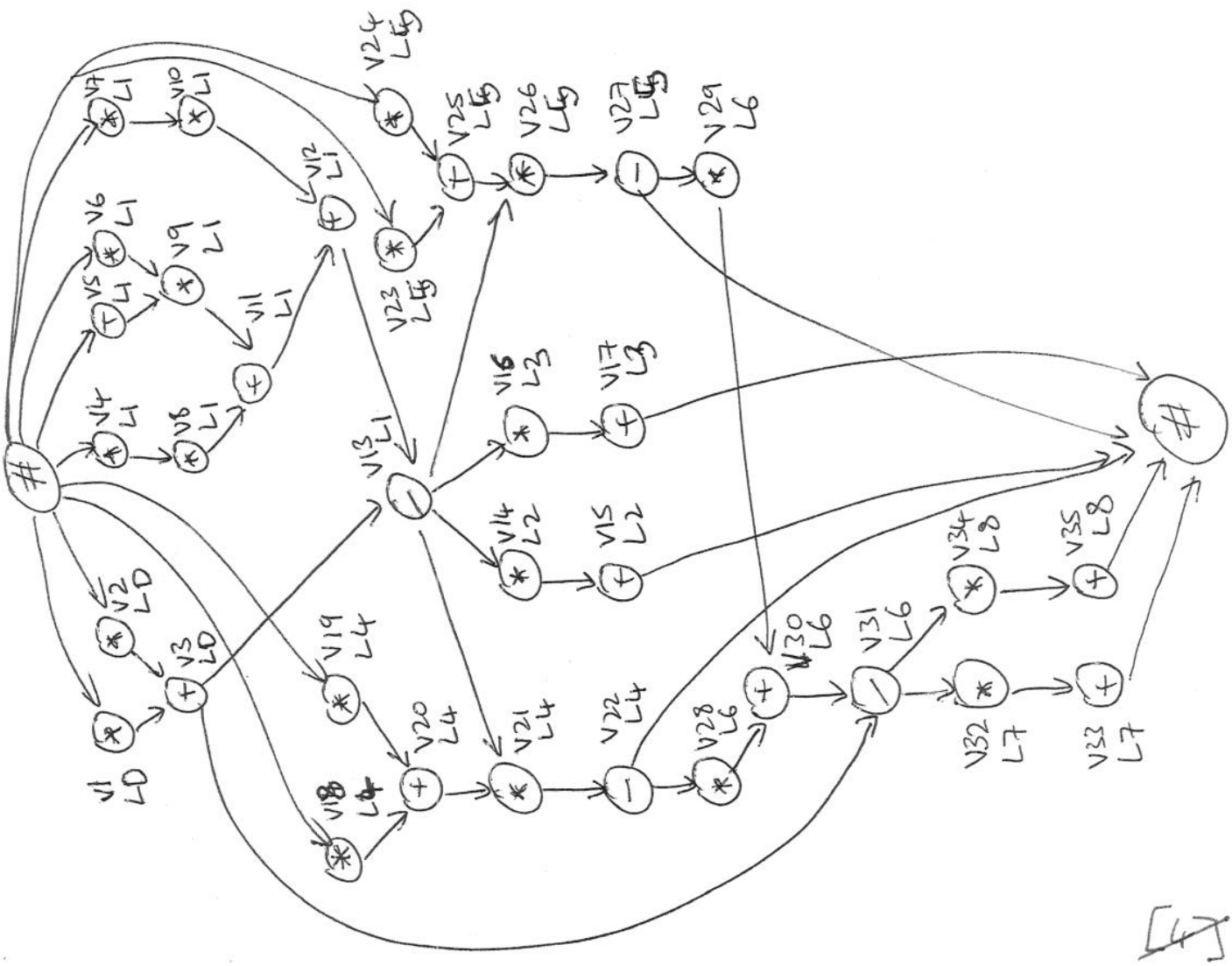
1a) A01

SYNTHESIS of DIGITAL ARCHITECTURES

SOLUTIONS 2008



[4]

[5]

1.b) Resource constrained list scheduling.

ALAP TIMES (for URGENCY) – coded in reverse, i.e. 0 is high ALAP, greater # ⇒ more urgent.

SOURCE	13	V19	9
V1	10	V20	8
V2	10	V21	7
V3	9	V22	6
V4	12	V23	9
V5	12	V24	9
V6	12	V25	8
V7	11	V26	7
V8	11	V27	6
V9	11	V28	5
V10	10	V29	5
V11	10	V30	4
V12	9	V31	3
V13	8	V32	2
V14	2	V33	1
V15	1	V34	2
V16	2	V35	1
V17	1	SINK	0
V18	9		

SCHEDULE

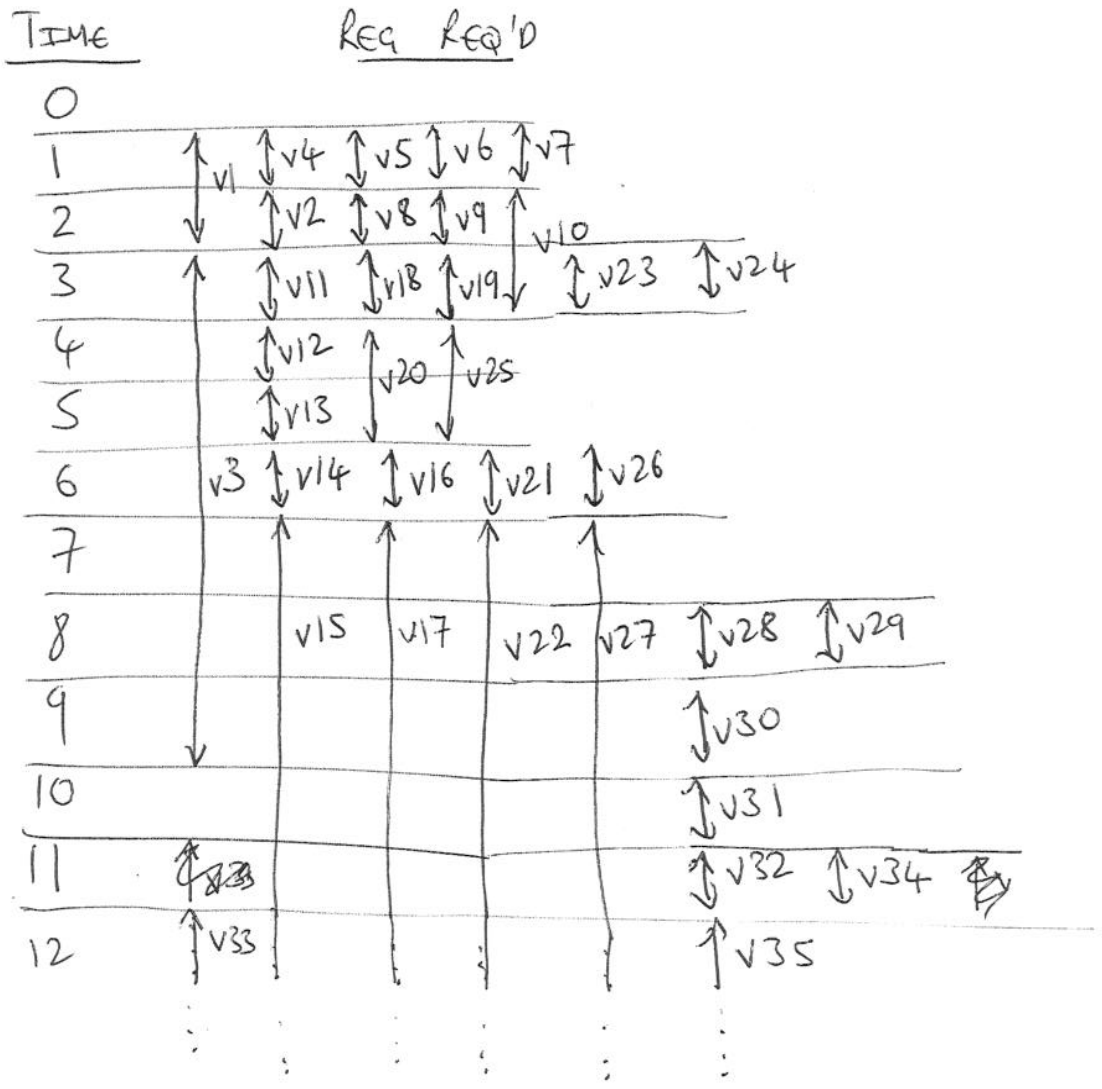
TIME	CANDIDATES	CHOSEN
0:	V1, V2, V4, V5, V6, V7, V18, V19, V23, V24	V4, V5, V6, V7, V1
1:	V2, V18, V19, V23, V24 V8, V9, V10	V8, V9, V2, V10
2:	V18, V19, V23, V24, V11, V3	V11, V3, V18, V19, V23, V24
3:	V12, V20, V25	V12, V20, V25
4:	V13	V13
5:	V21, V14, V16, V26	V21, V14, V16, V26
6:	V22, V15, V17, V27	V22, V15, V17, V27
7:	V28, V29	V28, V29

1 b) [Continued]

TIME	CAND.	CHOSEN
8:	v30	v30
9:	v31	v31
10:	v32, v34	v32, v34
11:	v33, v35	v33, v35

~~[4]~~
[5]

c) Consider each node i.d. as the label for its output register. Then



1. c) [Continued]

$\chi(G) = \kappa(G) = 7.$

~~[4]~~ [5]

d)

Node	Binding	Node	Binding
V_1	(*, 1)	V_{19}	(*, 2)
V_2	(*, 4)	V_{20}	(+, 2)
V_3	(+, 1)	V_{21}	(*, 1)
V_4	(*, 2)	V_{22}	(+, 1)
V_5	(+, 1)	V_{23}	(*, 3)
V_6	(*, 3)	V_{24}	(*, 4)
V_7	(*, 4)	V_{25}	(+, 3)
V_8	(*, 1)	V_{26}	(*, 4)
V_9	(*, 2)	V_{27}	(+, 4)
V_{10}	(*, 3)	V_{28}	(*, 1)
V_{11}	(+, 2)	V_{29}	(*, 2)
V_{12}	(+, 1)	V_{30}	(+, 1)
V_{13}	(/, 1)	V_{31}	(/, 1)
V_{14}	(*, 2)	V_{32}	(*, 1)
V_{15}	(+, 2)	V_{33}	(+, 1)
V_{16}	(*, 3)	V_{34}	(*, 2)
V_{17}	(+, 3)	V_{35}	(+, 2)
V_{18}	(*, 1)		

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~~[4]~~

[5]

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5/8

2. a) $\text{Min.} \sum_{t=ASAP_v}^{ALAP_v} t \cdot x_{v_2 t}$

s.t. $\forall v \in V: \sum_{t=ASAP_v}^{ALAP_v} x_{vt} = 1$

$\forall (u,v) \in E: \sum_{t=ASAP_v}^{ALAP_v} t \cdot x_{vt} \geq \sum_{t=ASAP_u}^{ALAP_u} t \cdot x_{ut} + d_u$

$\forall r \in R, \forall t \in \{0, \ldots, \lambda\}$

$$\sum_{v \in V \cdot T(v)=r} \sum_{t' \in \{t-d_v+1, \ldots, t\} \cap \{ASAP_v, \ldots, ALAP_v\}} x_{vt'} \leq a_r$$

$$\sum_{r \in R} c_r a_r \leq A$$

[10]

2. b) 7/9
6/8

$$\text{Min} \sum_{t=ASAP_{v_2}}^{ALAP_{v_2}} \sum_{q=1}^{4} t \cdot x_{v_2 t q}$$

$$\text{s.t.} \quad \forall v \in V \sum_{t=ASAP_v}^{ALAP_v} \sum_{q=1}^{4} x_{vtq} = 1$$

$$\forall (u,v) \in E \sum_{t=ASAP_v}^{ALAP_v} \sum_{q=1}^{4} t \cdot x_{vtq} \geq \sum_{t=ASAP_u}^{ALAP_u} \sum_{q=1}^{4} t \cdot x_{utq} + d_u + \underbrace{\epsilon_{uv}}_{\text{communication latency variable}}$$

$$\forall v \in V \quad \forall q \quad \underbrace{y_{vq}}_{\text{placement variable}} = \sum_{t=ASAP_v}^{ALAP_v} x_{vtq}$$

$$\forall (u,v) \in E \quad \forall q \quad \epsilon_{uv} \geq y_{vq} - y_{uq} \quad \| \text{ Force } \epsilon_{uv} \geq 1 \text{ if in different quadrants.}$$

$$\forall r \in R, \forall t \in \{0, \dots, \lambda\}, \forall q$$

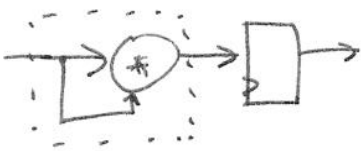
$$\sum_{v \in V : T(v) = r} \sum_{t' \in \{t - d_v^{-1}, \dots, t\} \cap \{ASAP_v, \dots, ALAP_v\}} x_{vt'q} \leq \underbrace{a_{rq}}_{\text{per-quadrant bound}}$$

$$\forall q \quad \sum_{r \in R} c_r a_{qr} \leq A/4$$

[10]

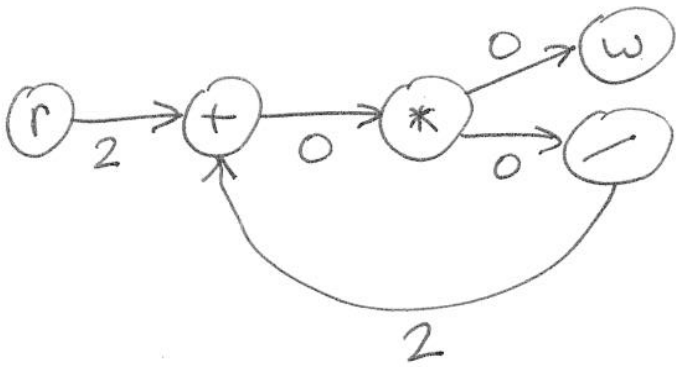
~~8/9~~ 7/8

3. a) Need to find an appropriate initial state for registers, e.g.



If this register is initialised to -1, there is no corresponding initial state before the squarer (thing the dashed line encloses a "black box". [2]

b)



[3]

c) Min: $L + \alpha \sum_{v \in V} r_v$ ← # regs at o/p of node v

s.t. ~~$\forall v \in V$~~ ~~$\forall u \in V$~~ $\forall (v,u) \in E$ $r_v \geq w_r(v,u)$ → NEW CONSTRAINT. CAN RE-USE REGISTERS.

$\forall (u,v) \in E \quad s_v \geq s_u + d(u) + w_r(u,v) N$

$\forall v \in V \quad s_v + d(v) \leq L$

$\forall (u,v) \in E \quad w_r(u,v) = w(u,v) + r(v) - r(u) \geq 0$

$r(v) \in \mathbb{Z}$ for all $v \in V$.

} As per note.

[10]

3 d) Code for (a):

```
while (true)
begin
    read x;
    y = x2 + z1;
    q = y * 3;
    z = 5/q1;
    write q;
    x2 = x1;
    x1 = x;
    z1 = z;
    q1 = q;
end
```

Code for (b):

```
while (true)
begin
    read x;
    ~~y = x1~~
    z = 5/q1;
    y = x1 + z;
    q = y1 * 3;
    write q;
    q1 = q;
    x1 = x;
    y1 = y;
end
```

for (a), N = 4. for (b), N = 3.

for (a), Tclk ≥ 3 (limited by divider)

for (b), Tclk ≥ 4 (divider – adder chain)

~~α_2~~ ~~It~~ is clear that $\alpha_2 > \alpha$.

~~Also 3 + 4 α >~~

[5]