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IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2010

MSc and EEE PART III/IV: MEng, BEng.and ACGI

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Friday, 14 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : C. Toumazou
Second Marker(s) : S. Lucyszyn

1. Figure 1 (a, b c, and d) show four popular biasing schemes typically used in analogue integrated circuits.

   (a) Briefly explain the function of each of the circuits in Figure 1 (a, b, c and d) and derive expressions for the constant output parameter in each case, clearly indicating component design requirements and any approximations you have made. You may ignore bulk effects in the CMOS circuits.

   [16]

   (b) Design the constant current generator of Figure 1(c) to give an output current of 5 μA. Assuming R is a polysilicon resistor with a temperature coefficient of 1500 ppm/°C, calculate the fractional temperature coefficient of the circuit at room temperature.

   [4]

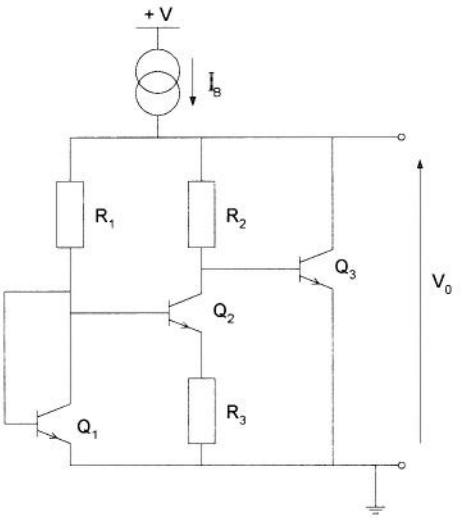

Figure 1(a)

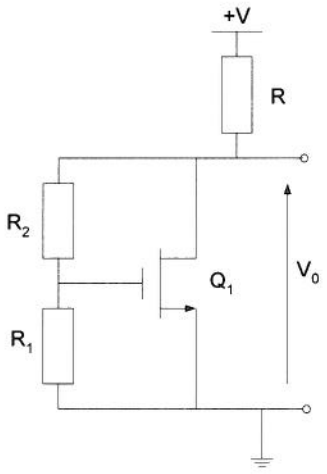

Figure 1(b)

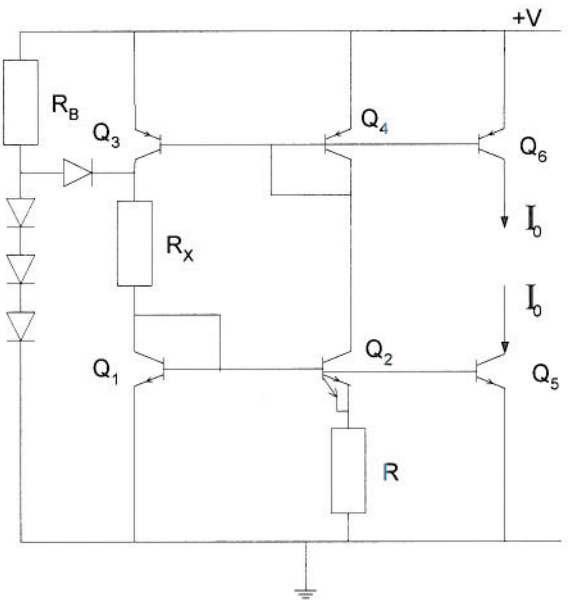

Figure 1(c)

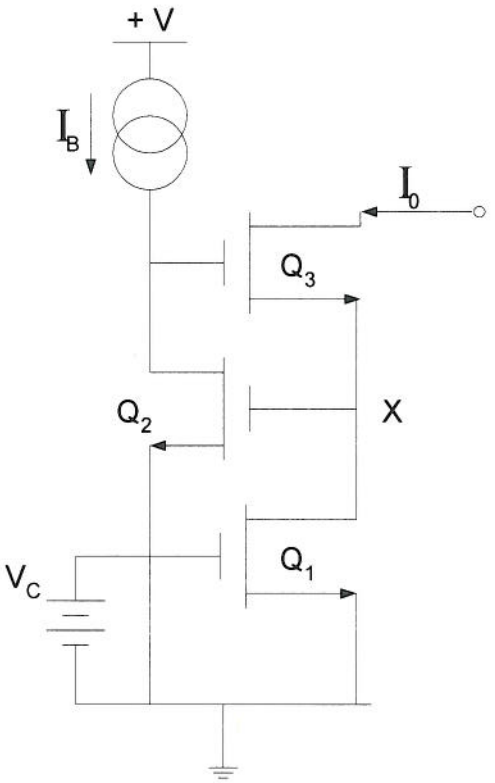

Figure 1(d)

2. (a) Two high-performance analogue-to-digital converters are the current-mode algorithmic converter and the sigma-delta converter. Sketch a typical architecture for ONE of these converter types and explain its principles of operation.

[10]

(b) Assume that the maximum resolution of any sampled-data converter is limited by switch noise (kT/C). Calculate the maximum resolution of a stereo-audio system running at a sample rate of 40 kHz. Assume a MOSFET switch aspect ratio $(W/L) = 1/8$, transconductance parameter $Kp = 20\ \mu A/V^2$ and a device threshold voltage $V_T = 1\ V$. The on voltage of the switch is a $5\ V$ reference (i.e. $V_{GS}on = V_{ref} = 5\ V$). You may also assume that the switch settles in $10\ \tau$ (where τ = time constant) over one period of the clock frequency.

Boltzmanns constant $k = 1.38 \times 10^{-23}\ J/K$ and the ambient temperature is $300\ K$.

[10]

3. Figure 3 shows a partially-designed two-stage CMOS op-amp required to give a voltage gain of approximately 80 dB, a slew-rate of 5 *V/μs* and a gain-bandwidth product of 3 MHz.

(a) Given that the technology is a fixed 5 μm double metal CMOS process, design the channel widths of transistors Q1, Q2 and Q6 for the op-amp to meet the above performance specifications. Aspect ratios of all other devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below.

[15]

(b) Give a reason why the introduction of a single integrated resistor in series with the compensation capacitor should significantly improve the amplifier's phase margin.

[5]

CMOS TRANSISTOR MODEL PARAMETERS

MODEL PARAMETERS	$Kp\ (\mu A/V^2)$	$\lambda\ (V^{-1})$	$V_{T0}\ (V)$
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

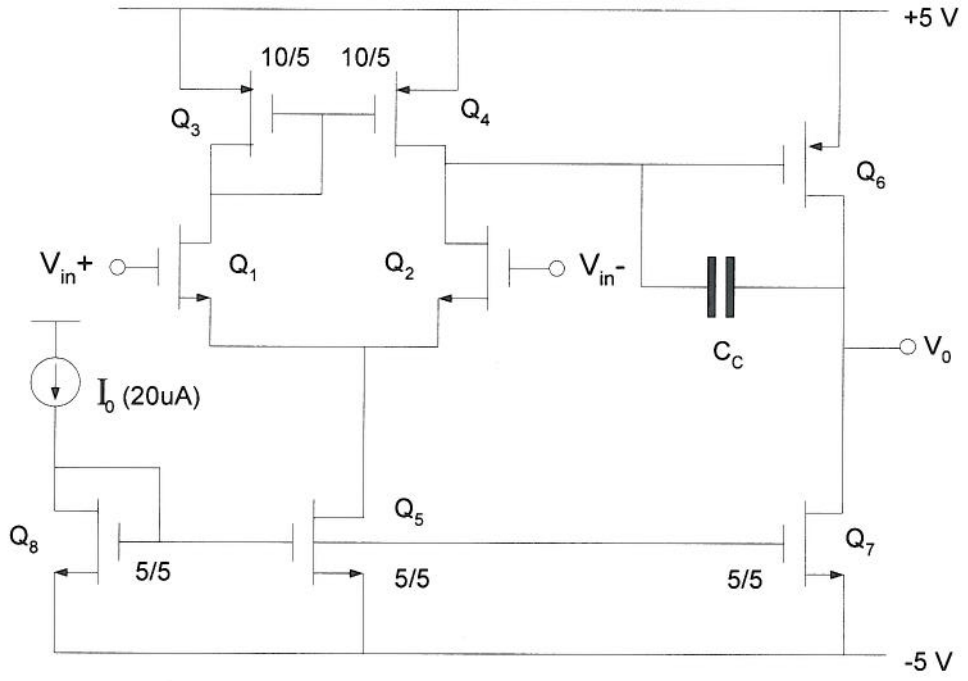

Figure 3

4. Figure 4 shows the basic design of an analogue sampled-data precision integrator.

   (a) Derive an expression for the transfer function of the integrator. Assume that the integrator is driven by non-overlapping clocks and that the switches are ideal.

   [10]

   (b) (i) Sketch the basic design of a 3rd-order Chebyshev low pass switched-capacitor ladder filter.

   The filter is to have a cut-off frequency of 5kHz. Assume a clocking frequency of 100 kHz. The values of integration capacity for the capacitor based sections are 6.44pF and inductive section is 3.164pF. All other switched capacitors are 1pF.

   (ii) From the circuit, estimate normalised passive component values for the original double-terminated LC prototype of the filter. All values should be normalised to 1 rad/s. You may assume that the clocking frequency is so high that the integrators can be assumed lossless.

   [10]

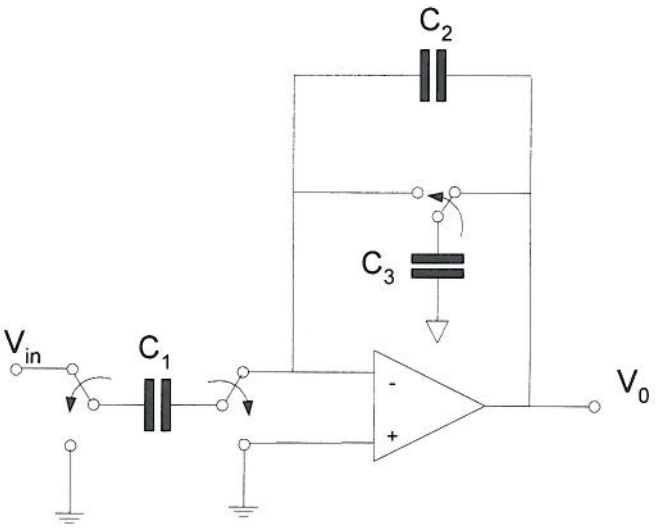

Figure 4

5. (a) Give two advantages of current-mode analogue signal processing compared to traditional voltage-mode processing.

[4]

(b) With the aid of a suitable macromodel, explain the theoretical concept of current feedback and how it results in constant bandwidth amplification. Using a current-feedback op-amp, design a closed-loop non-inverting gain stage with a bandwidth of 10 MHz for a fixed voltage gain of 100. Assume an internal compensation capacitance of 4pF and that the open-loop transresistance gain of the amplifier is very much larger than the amplifier feedback resistor.

[16]

6. Figure 6 shows the basic design of an integrated circuit precision integrator.

   (a) Derive an expression for the time constant of the integrator.

   [10]

   (b) Why is it important for the MOSFETS in Figure 6 to operate in their triode region? Discuss the three key sources of non-linearity in the triode region.

   [4]

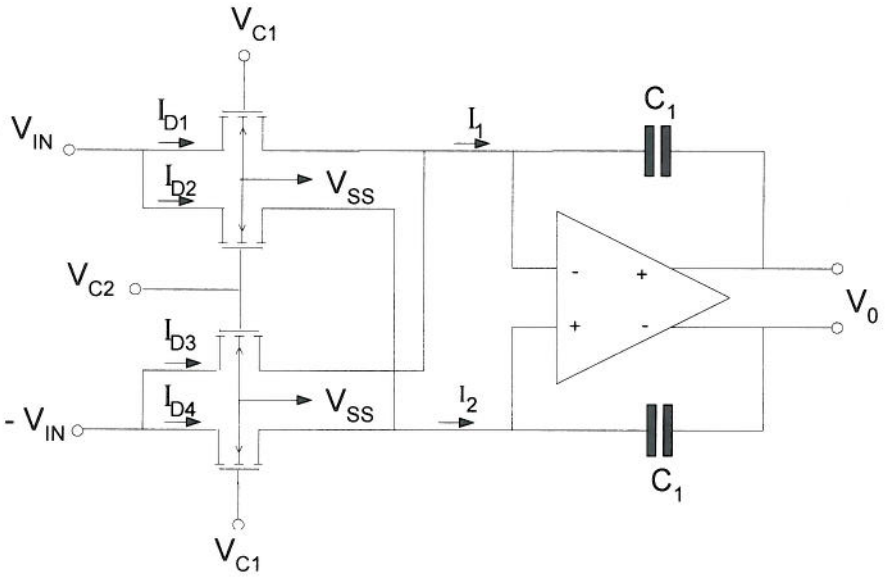

Figure 6

   (c) Sketch suitable fully differential folded cascade op-amp architecture for Figure 6. Why is it important for the amplifier to have common-mode feedback?

   [6]

EXAM SOLUTIONS

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ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

2010

1 MARKER. C. TOUMAZOU

2 MARKER. S. LUCYSZYN

Q1

a) Bandgap reference. Output voltage reference independent of temperature.
Assumes $V_{BE} \approx -2.5mV/°C$
And $\beta >> 1$

$$V_{BE3} - V_{BE2} = V_T \ln(I_1/I_2) = I_2 R_1$$

Thus $V_o = V_{BE3} + (R_2/R_3)(V_T) \ln I_1/I_2$

For $dV_o/dt = 0$, then $(R_2/R_3) \ln I_1/I_2 \approx 24.5$, $V_o = 1.283V$ (4)

b) V_{gs} multiplier. Can replace stacked diodes with a single resistor for biasing purposes.

$$V_o \approx V_{GS}[1 + R_2/R_1]$$

$$\simeq (1 + R_2/R_1)[V_T + \sqrt{I_D/\beta}]$$ (4)

c) PTAT (proportional to absolute temperature) constant current source/sink. The output current is virtually independent of the power supply voltage. Diode chain R_B and R_A form automatic start-up circuitry ensures circuit behaves in correct output state. (4)

Analysis – Assume matched devices $\beta >> 1$

then $I_O = \Delta V_{be}/R = [V_T \ln(I_N/I_O)(I_{S3}/I_{S1})]/R$

$(I_{S3} = 2I_{S1})$ then $I_O = (V_T \ln 2)R$. ✱

(4)

Question 4 – continued.

Fig 4d →

Regulated Cascode current sink, since drain-source voltage of Q1 is regulated by the feedback amplifier Q2 the circuit has a very high output impedance equivalent to that of a double cascode.

Analysis, $I_O = \beta (V_G - V_T)^2$

assume FET Q1 is saturated (4)

b) $I_O = (V_T \ln 2)/R$

assuming $V_T = 25\,mV$ at $300°k$

then $R = 3.465\,k\Omega$.

$$T_{CF} = \frac{1}{V_T}\frac{\partial V_T}{\partial T} - \frac{1}{R}\frac{\partial R}{\partial T}$$

$$\approx \frac{1}{T} - \left(\frac{1}{R}\frac{\partial R}{\partial T}\right)$$

$$= (1/300) - 1500 \times 10^{-6}$$

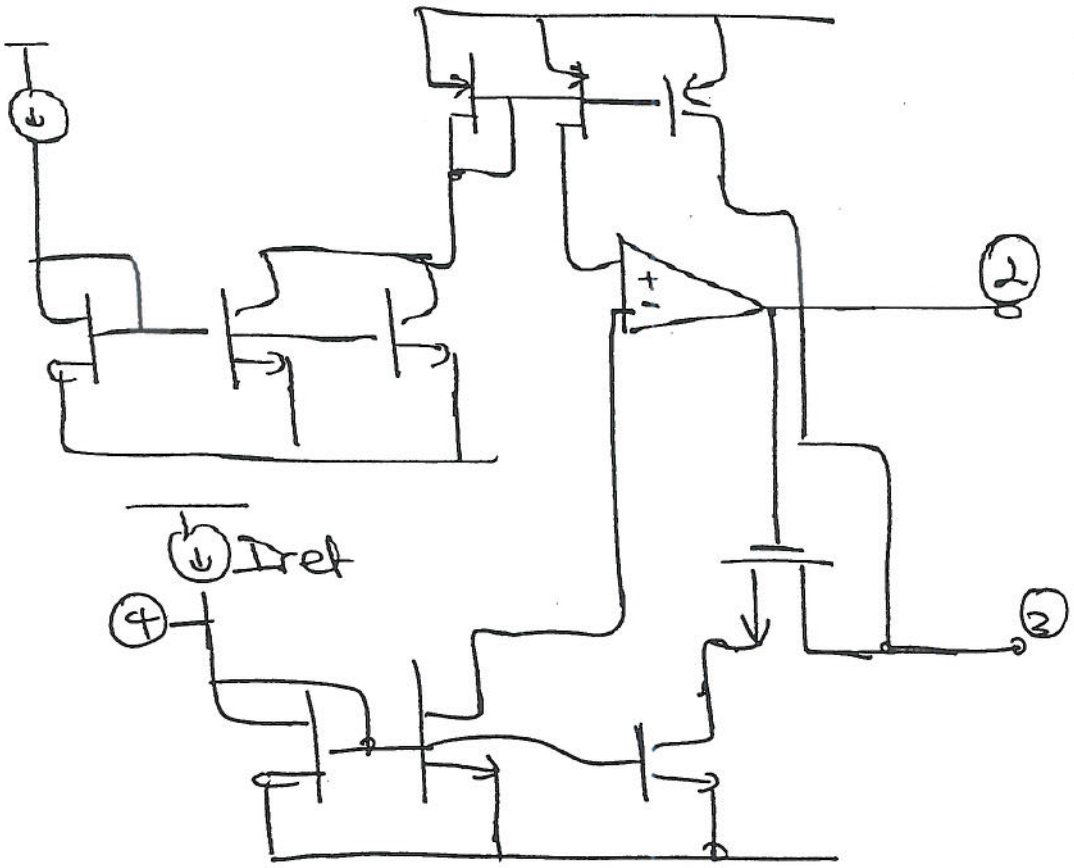
$$= 1833\ ppm/°C$$

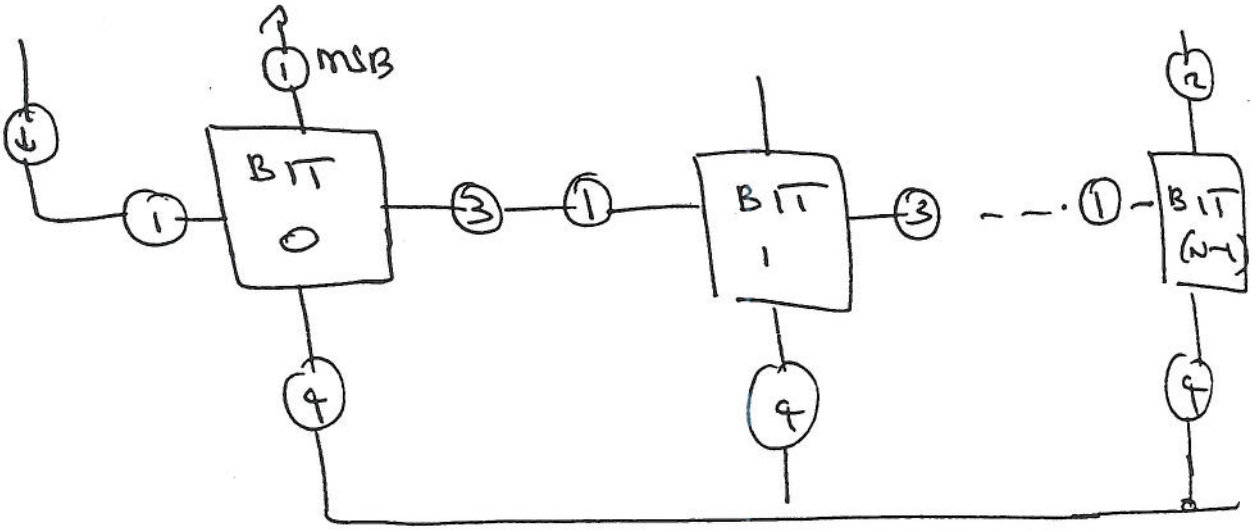
(4)

CT

Question 2

Algorithmic Converter 1 Bit





BASIC ARCHITECTURE

CT

Question 2 – cont

If $2I_{IN} < I_{ref}$

Comp goes low, digital output = 0

and analogue output $2I_{in}$

If $2I_{IN} > I_{ref}$, comp output goes high, digital = 1

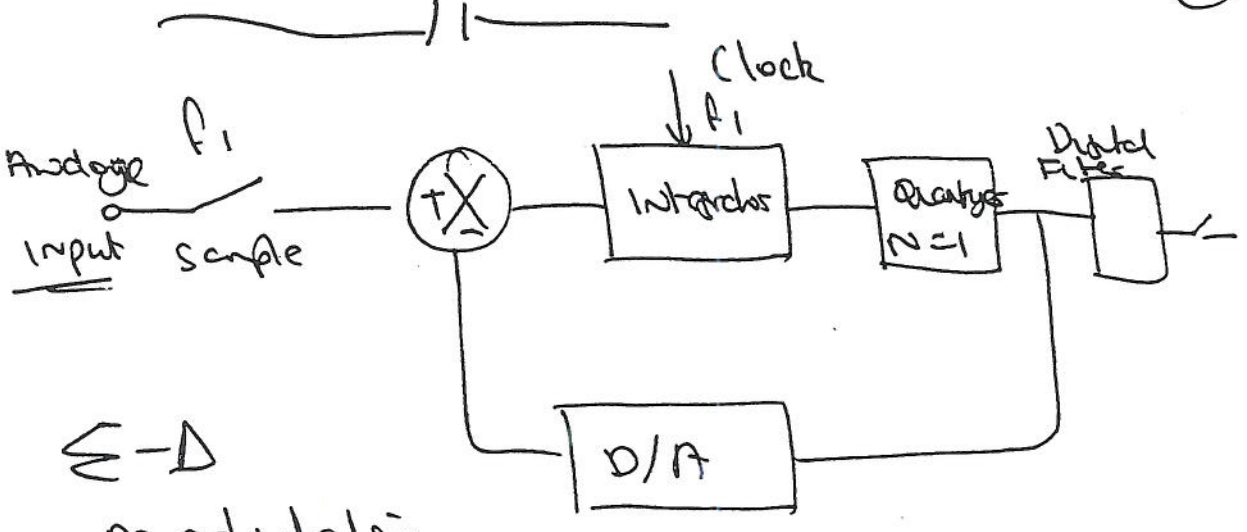
analogue output $(2I_{IN} - I_{ref})$

Analogue output consequently feeds into following 'bit', which

performs exactly the same function.

The process is repeated as many times as necessary to achieve desired resolution.

(10)



Σ-Δ modulator

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Question 2 – cont

Coarse quantization at high sampling rate combined with negative feedback and digital filtering to achieve increased resolution at lower sampling rates.
A means of trading resolution in time for resolution in amplitude avoiding the need for precision analogue components.

Negative feedback produces coarse estimate that oscillates about the true value of the input, the digital filter averages the coarse estimate to give a finer approximation.

Feedback A/D + integrator →
quantization error to have a high frequency spectrum, filtered out by digital filter.

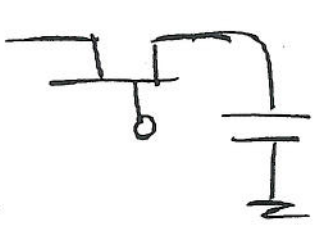
Noise shaped and all high frequency noise filtered giving very high (S/N) at low frequency. (10)

(T

Question 2 cont

DR $\triangleq$ Vref / Noise = 2^N

Switch



RMS Noise of switch capacitor

$$\sqrt{\frac{kT}{C}}$$

Assume $f_C = \frac{1}{10 R \cdot C}$, then

Solving for C gives

$$DR = 2^N = V_{ref} / \sqrt{kT\, 10 \cdot R \cdot f_c}$$

$$R_{on} = \frac{1}{2\beta(V_{GS} - V_T)} \approx \frac{1}{(2\beta \times 4)}$$

$$\beta = \left[\frac{kW}{2L}\right]$$

Can now find DR at 40 kHz (10)

CT

3// Specs $A = 80dB$, $S.R = 5V/\mu s$, $GB = 3MHz$

a) $A_1 = g_{m2}/(g_{04}+g_{02}) \Rightarrow (g_{02}+g_{04})$

$= I_{D2}(\lambda_N + \lambda_P)$

$= 10\times10^{-6}[0.05]$

$= 5\times10^{-7}\ \Omega^{-1}$

$g_{m2} = 2\sqrt{\beta_2 I_{D_2}} \Rightarrow$ but $G.B = \frac{g_{m2}}{2\pi C_c}$

require C_c. From $S.R = I_D/C_c$

Then $C_c = 4pF \Rightarrow g_{m2} = 7.54\times10^{-5}$

$\therefore A_1 = -150.8$

From $g_{m2} = g_{m1} = 2\sqrt{\beta I_D}$

$\beta_2 = \beta_1 = 1.42\times10^{-4} = \frac{KW}{2L}$

$\therefore (W/L)_2 = (W/L)_1 = 9.46$

$= \underline{\underline{47/5}}$ 10

Since $A_1 = 150.8$, $A_2 = 10^4/(150.8)$

$= 66$

$A_2 = g_{m6}/(g_{06}+g_{07})$

CT $(g_{06}+g_{07}) = I_{D1}(\lambda_6 + \lambda_7)$ CT

(3) cont

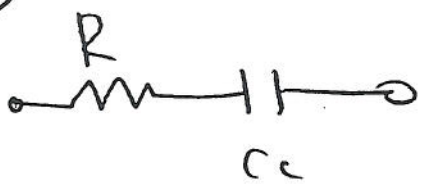
$(g_{o6}+g_{o7}) = 20\times10^{-6}(0.05) = 1\times10^{-6}\,\Omega^{-1}$

given $g_{m6} = 6.63\times10^{-5}$

$\Rightarrow \beta_6 = \left(\frac{g_{m6}}{2}\right)^2 \frac{1}{I_{D6}} = 5.5\times10^{-5}$

Thus given $(W/L)_6 = 5.5 = \underline{\underline{27/5}}$ 5

6)



Function of R is to provide feedforward compensation to eliminate RHP zero from transfer function of OP-Amp.

with $R \Rightarrow$ zero $= g_{m6}/C_c$,

with R $\quad Z = \dfrac{1}{(1/g_{m6} - R)C_c}$

① $R = 1/g_{m6}$ → remove zero improve ϕ 5

② $R \Rightarrow$ non-dominant pole cancels with zero.

↳ $> 1/g_{m6}$

GT MT

Q4 - lossy Integrator.

During ϕ_1 of switch, $I_{out} = C_1 V_{in}/T$

$\phi_2 - C V_{IN}/T = V_o[j\omega C_2] + \frac{C_3 V_o}{T}$

Transfer of Charge

Recurring yields

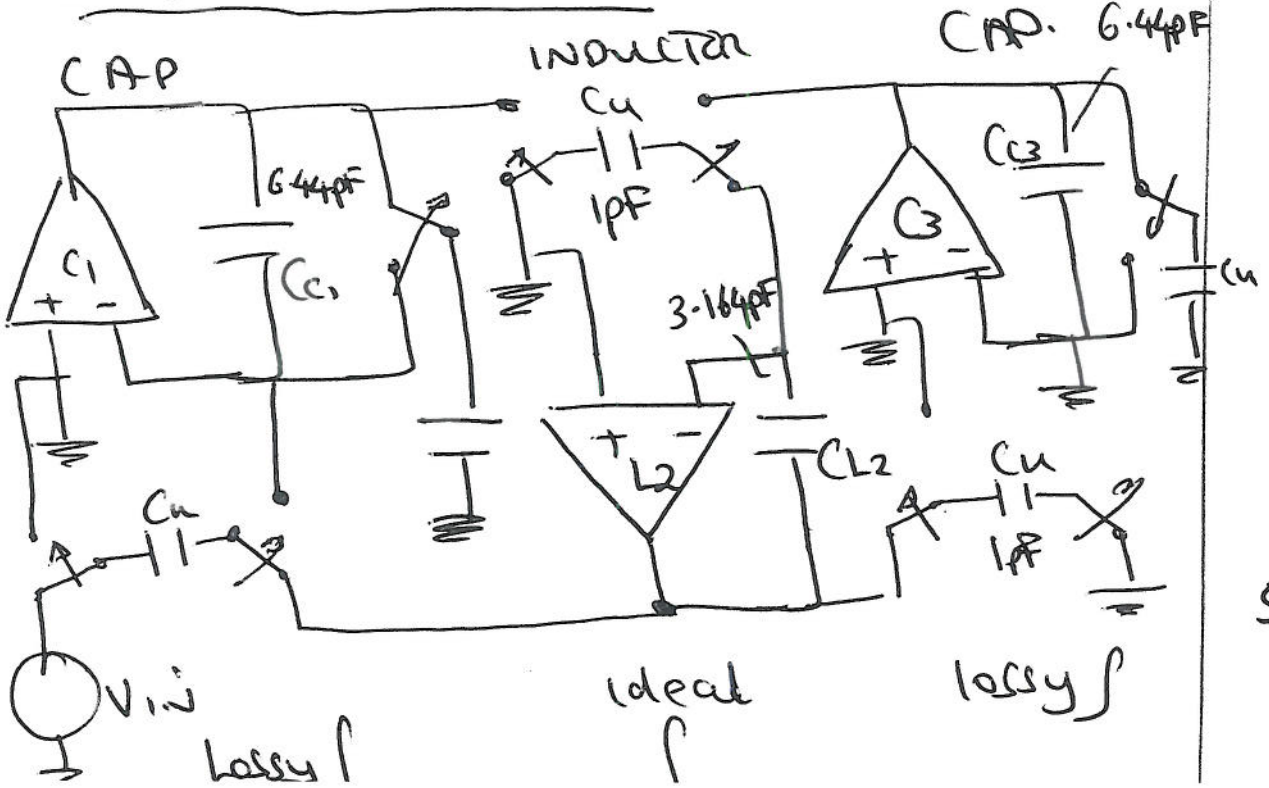
$$V_o/V_{IN} = -C_1/C_3 \left[\frac{1}{\left(1 + j\omega \frac{C_2 T}{C_3}\right)} \right]$$

$$= -\frac{C_1}{C_3} \frac{1}{(1 + jf/f_c)}$$

$$f_p = \frac{1}{2\pi \frac{C_2}{C_3}} f_c$$

10

b) 3rd order SC low pass



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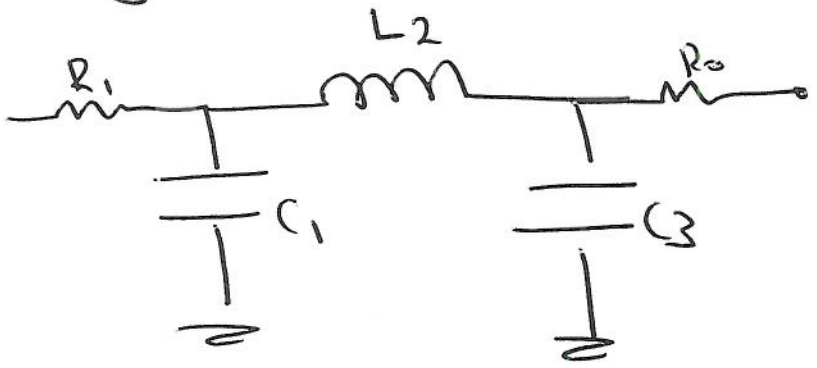
Q4 cont

Doubly Terminated Ladder.



Conversion into differential integrator

$$\left.\begin{aligned} C_{c1}/C_u &= f_c C_1 \\ C_{c3}/C_u &= f_c C_3 \\ C_{L2}/C_u &= f_c L_2 \end{aligned}\right\}$$ general transformation

$R_1 = R_o = 1\Omega = R_s$.

Assuming $f_c = 100\text{kHz}$, $C_u = 1\text{pF}$

then $C_1 = C_3 = 6.44 \times 10^{-5}\text{F}$

$C_2 = 3.164 \times 10^{-5}\text{F}$

Normalized $2\pi f$

where $f = 5\text{kHz}$.

then $C_1 = C_3 = 2.0236$

$C_2 = 0.994$

5

FT

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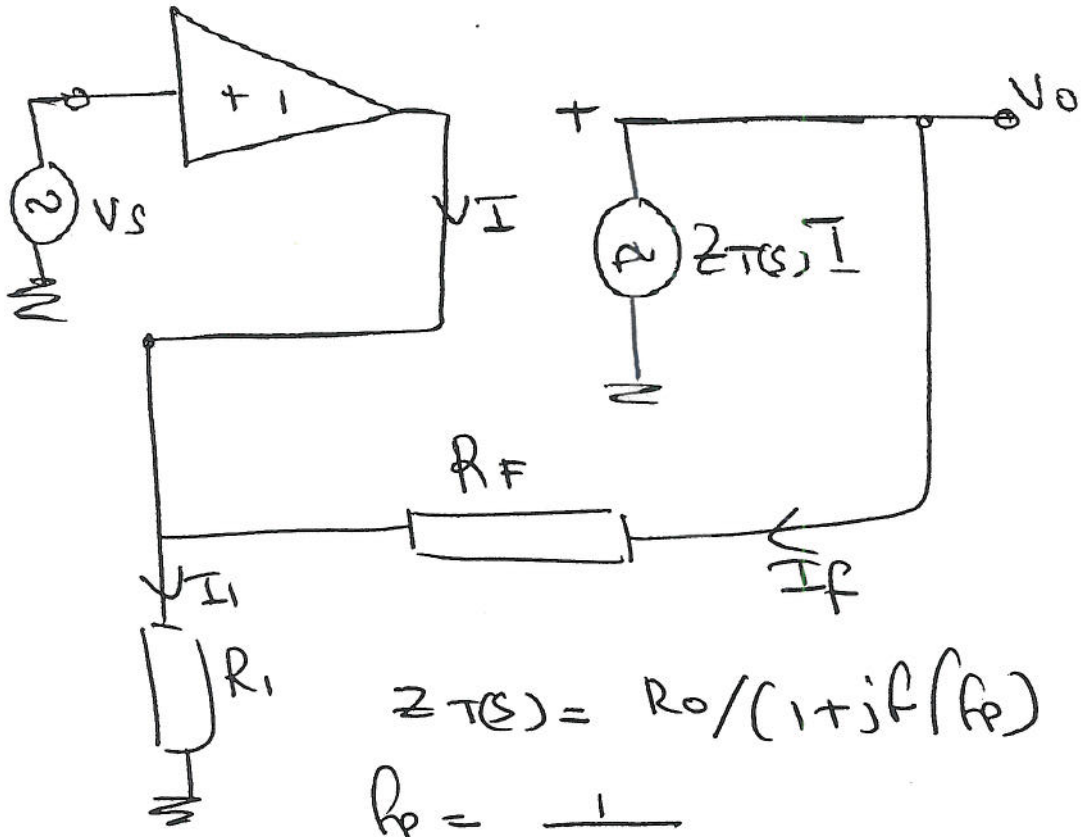
Advantages of Current-mode

High frequency performance, wide dynamic range

Lower power supply voltage

4



$$Z_{T(s)} = R_o/(1+jf/f_p)$$

$$f_p = \frac{1}{2\pi R_o C}$$

C = compensation capacitor

3 equations

$$I_f = (V_o - V_s) R_F \quad - (1)$$

$$I_1 = V_s/R_1 \quad - (2)$$

$$V_o = Z_{T(s)} I = Z_{T(s)} [I_1 - I_f] \quad - (3)$$

8

CT

CT

Subs ① and ② into ③ gives,

$$\left(V_o/V_s\right) = \left(1+R_F/R_1\right) Z_T(s)/\left(R_F+Z_T s\right)$$

Subs for $Z_T(s)$ — gain

$$\left(V_o/V_s\right)_{sw} = \left(1+R_F/R_1\right)\left[\frac{R_o}{R_o+R_F}\right] \times \frac{1}{\left(1+jf/f_p\left[\frac{R_o+R_F}{R_F}\right]\right)}$$

BW

Assuming $R_o \gg R_F$

then

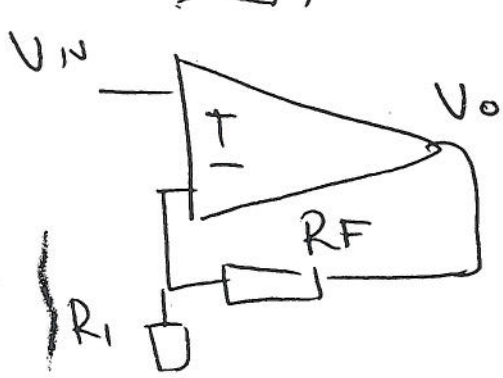
Closed loop gain $\simeq \left(1+R_F/R_1\right)$ — *

Closed loop Bandwidth $\simeq \frac{f_p R_o}{R_F} = \frac{1}{2\pi R_F C}$

L*.

Hence R_F sets the amplifiers constant BW

and R_1 chosen to set the gain



$BW = \frac{1}{2\pi R_F C} = 10\text{MHz}$

$\therefore$ given $C = 4\text{pF}$

$R_F = 3.98\text{k}\Omega$

Since $A = \left(1+R_F/R_1\right) = 100$

$R_1 \simeq 40\Omega$

8

6) a) Floating integrated R.C integrator

Double mos resistor

$$R = \frac{V_{in} - (-V_{in})}{(I_1 - I_2)} = \frac{1}{2\beta(V_{c1} - V_{c2})}$$

Expect student to give full derivation.

$$\tau = RC = \frac{C}{2\beta(V_{c1} - V_{c2})}$$

$$\beta = \frac{kW}{2L}$$

-11-

b) Linear Triode region important to avoid transistor entering its saturation region giving a square law characteristic.

When $V_{DS} << (V_{GS} - V_T)$

$$I_D = \frac{kW}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right](1 + \lambda V_{DS})$$

3 sources of non-linearity

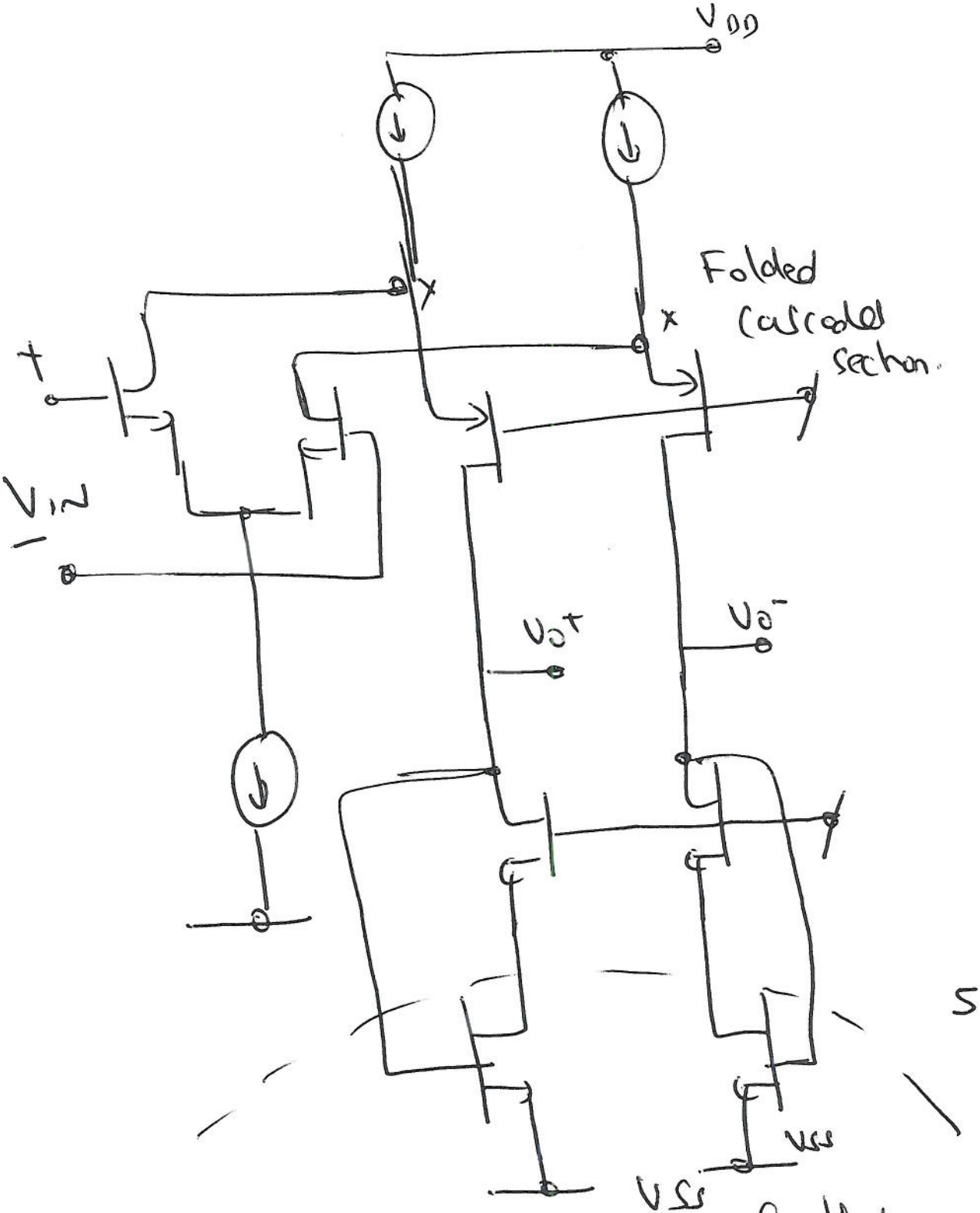
(i) V_{BS} changing V_T due to body effect.

(ii) V_{DS} approaching $(V_{GS} - V_T)$ hence saturation for pos the V_{DS}

(iii) Large values, $V_{DS}^2/2$ term makes resistor non-linear.

CT

6 (c)



$$A = \frac{1}{2}\left(\frac{g_m}{g_D}\right)^2$$

Common-mode feedback is necessary to reduce output differential offset and to ensure rejection of common-signal at output.

5

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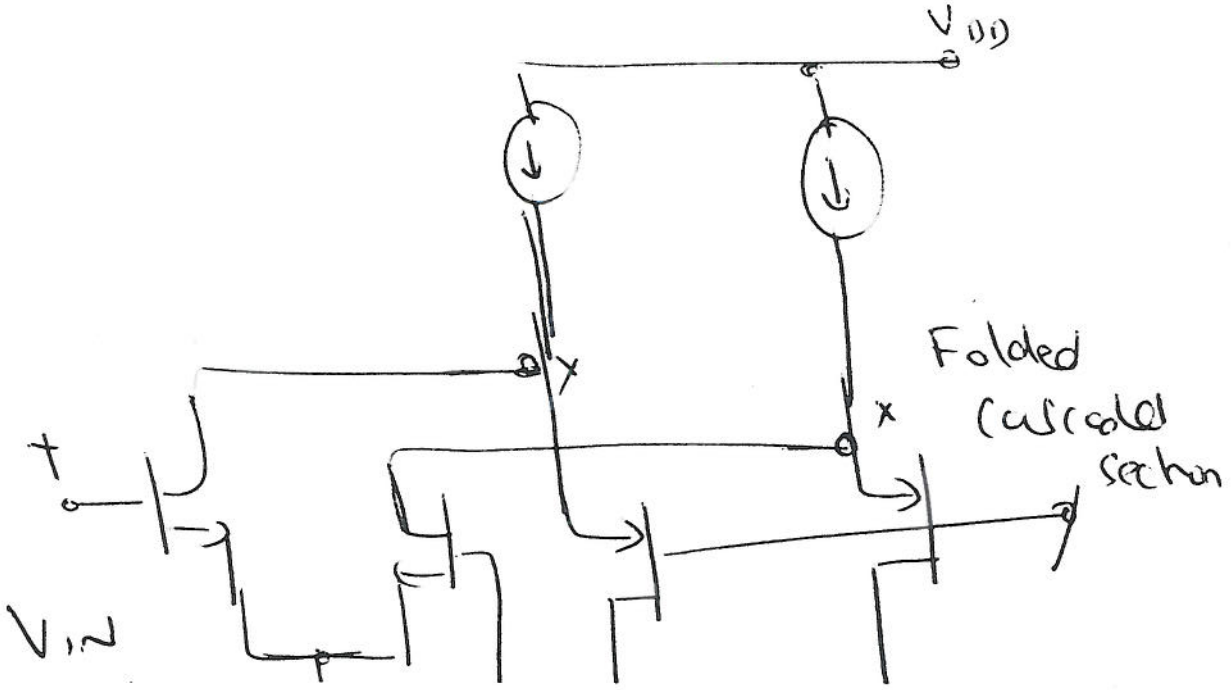
V_{DD}
x
x
Folded
cascaded
section
+
V_{in}