1. This question consists of 6 sub-questions. Each item can be answered in a few words or a short paragraph with use of a diagram and/or expression where helpful. Please answer all sub-questions and simplify expressions where possible stating any assumptions made.

a) Derive expressions (by inspection) for the *voltage gain* of the amplifier circuits shown below in Fig. 1.1 (include r_O). [10]

(i) (ii)

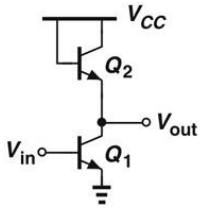


Fig. 1.1(a)

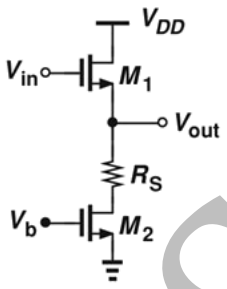


Fig. 1.1(b)

(i) Q_1 is a common emitter amplifier and Q_2 is a diode connected NPN BJT load. [1]
Thus, $A_v = -g_{m1}R_{out} = -g_{m1}(r_{o1}||r_{o2}||1/g_{m2}||r_{\pi 2})$ [2]
Assuming that $1/g_m << r_{\pi 2}, r_o$ [1] -> $\underline{A_v = -g_{m1}/g_{m2}}$ [1]

(ii) M_1 is a source follower (CD amplifier) and R_S in series with M_2 is the load. [1]
From formula sheet, $A_v = R_S||r_o/(R_S||r_o + 1/g_m)$ [1] -> $\underline{A_v = (R_S+r_{o2})||r_{o1}/((R_S+r_{o2})||r_{o1}+1/g_{m1})}$ [3]

b) Derive expressions (by inspection) for the *output resistance* of the amplifier circuits shown below in Fig. 1.2 (include r_O). [10]

(i) (ii)

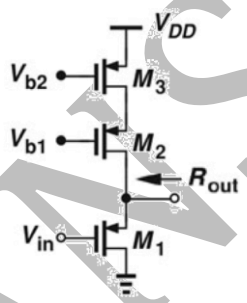


Fig. 1.2(a)

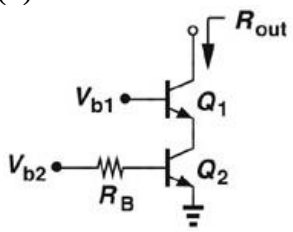


Fig. 1.2(b)

(i) $R_{out} = R_{up}||R_{down}$ [1]
R_{up} = PMOS cascode = $g_{m2}r_{o2}r_{o3} + r_{o2} + r_{o3} \approx g_{m2}r_{o2}r_{o3}$ [1] (assuming $g_m r_o >> 1$) [1]
R_{down} = NMOS source = $1/g_{m1} \,||\, r_{o1} \approx 1/g_{m1}$ (assuming $1/g_m << r_o$) [1]
$R_{out} = 1/g_{m1} \,||\, g_{m2}r_{o2}r_{o3} \approx \underline{1/g_{m1}}$ [1]

(ii) Similarly
R_{out} = NPN cascode [1] = $g_{m1}r_{o1}(r_{o2}||r_{\pi 1}) + r_{o1} + r_{o2}||r_{\pi 1}$ [1] $\approx \underline{g_{m1}r_{o1}(r_{o2}||r_{\pi 1})}$ [2]
(assuming $g_m r_o >> 1$) [1]

The main issue with 1(a) and 1(b) is many students not attempting to make any simplifying assumptions and/or stating assumptions.

c) Compare the key features (and limitations) between an *integrated circuit* and *printed circuit board* based analogue circuit implementation. [5]

Integrated circuit

- High integration density - complex circuits with many components. -> small size [1]
- Low power (compared to PCB based) [1]
- Low cost for volume (+ high cost for prototyping) [1]

PCB

- Low prototyping cost (IC costs £k's) [1]
- Quick development time (IC takes months/years in comparison) [1]

d) Explain how the circuit implementation of an operational amplifier (op-amp) can affect its *bandwidth (-3dB)*. [5]

In general, the -3dB bandwidth of an amplifier is defined by its dominant pole (i.e. its lowest frequency pole). [1] The dominant pole is thus the one with the highest impedance (RC) to ground. [1] For circuits with a physical capacitance – (i.e. a drawn capacitor) this is normally the largest capacitance to ground (as much higher than parasitics). [1] For circuits without, the parasitic capacitance (and impedance) is normally highest at input to a CS or CE amplifier (due to the Miller effect). [1]

Amplifier circuits with just low impedance nodes (e.g. fully-balanced OTA) typically thus have higher frequency response, thus -3dB. Also circuit "tricks" to minimize miller effect (e.g. using a cascode after CS/CE reduces the gain of first CS/CE stage and thus the Miller capacitance). [1]

This was not answered very well. Most students confused gain-bandwidth product with -3dB bandwidth and as such did not include the key points.

e) Determine expressions for the *open loop gain*, *feedback factor*, and *closed loop output impedance* for the circuit shown in Fig 1.3 (excluding r_0). [5]

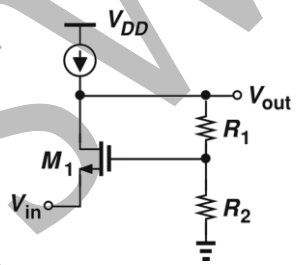


Fig 1.3.

$A_{OL}=+g_{m1}(R_1+R_2)$ [2 including for correctly breaking loop]
$K=R_2/R_1+R_2$ [1]
Loop gain = $A_{OL}K= g_{m1}(R_1+R_2)[R_2/(R_1+R_2)]$ [1]
$R_{out,OL}=R1+R2$
$R_{out,CL}=(R1+R2)/[1+ g_{m1}(R_1+R_2)(R_2/(R_1+R_2))]$ [1]

f) Calculate the transfer function of the circuit shown below in Fig. 1.4 if $A_0=\infty$. What choice of component values reduces $|V_{out}/V_{in}|$ to unity at all frequencies? [5]

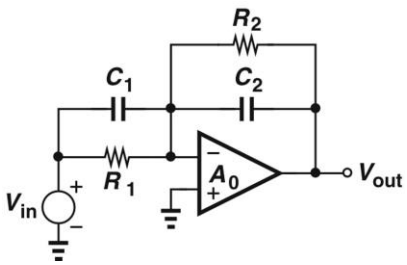


Fig 1.4.

- Can draw a simplified circuit replacing $C_1||R_1$ with Z_1 and $R_2||C_2$ with Z_2 [1]
- $Z_1=R_1||1/sC_1=R_1/(1/sR_1C_1+1)$, $Z_2=R_2||1/sC_2=R_2/(1/sR_2C_2+1)$ [1]
- $V_{out}/V_{in} = -Z_2/Z_1$ -> $|V_{out}/V_{in}| = 1$ at all frequencies??
- $|R_2/(1/sR_2C_2+1) / R_1/(1/sR_1C_1+1)| = 1$ [1] -> $R_2=R_1$ and $C_2=C_1$ [2]

2. The circuit below shows the transistor-level implementation of a two stage operational amplifier (Fig 2.1(a)), and this configured as a non-inverting amplifier (Fig. 2.1(b)).

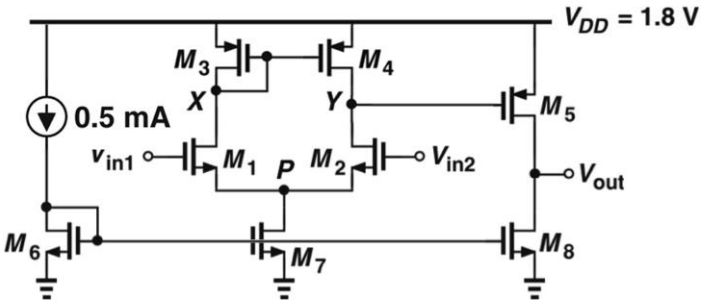


Fig. 2.1(a)

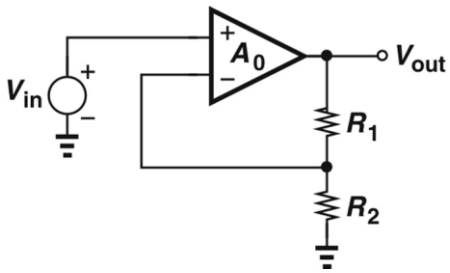


Fig. 2.1(b)

a) Derive an expression for the open loop gain (A_0) giving the polarities of V_{in1} and V_{in2} (i.e. which is V_+ and which V_-). [6]

$A_v=V_{out}/(V_{in2}-V_{in1}) = V_{out}/V_Y * V_Y/(V_{in2}-V_{in1})$
$A_v=-g_{m1}(r_{o2}||r_{o4})$ [2] * $-g_{m5}(r_{o5}||r_{o8})$ [2] = $g_{m1}g_{m5}(r_{o2}||r_{o4})(r_{o5}||r_{o8})$ [1]
V_{in1}=inverting input, V_{in2}=non-inverting input [1]

b) Given the following parameters calculate the open loop gain. [6]

$\mu_nC_{ox} = 200\mu A/V^2$, $V_{THN} = 0.4V$, $\lambda_N = 0.1V^{-1}$, $\mu_pC_{ox} = 100\mu A/V^2$, $V_{THP} = -0.5V$, $\lambda_P = 0.2V^{-1}$

Device	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8
W/L	200/0.5	200/0.5	2/2	2/2	100/2	4/4	8/4	40/4

$g_m=\sqrt{(2\mu C_{ox}(W/L)I_D)}$
-> $g_{m1}=\sqrt{(2*200\mu(200/0.5)0.5m)}=8.9mS$, $g_{m5}=\sqrt{(2*100\mu(100/2)5m)}=7.1mS$ [2]

$ro=1/\lambda I_D$
-> $r_{o2}=1/0.1(0.5m)=20K\Omega$, $r_{o4}=1/0.2(0.5m)=10K\Omega$, $r_{o5}=1/0.2(5m)=1K\Omega$, $r_{o8}=1/0.1(5m)=2K\Omega$ [2]
$A_v= g_{m1}g_{m5}(r_{o2}||r_{o4})(r_{o5}||r_{o8}) = (8.9m)(7.1m)(20K||10K)(1K||2K) = 280$ [1]
$A_v= 20\log_{10}(280) =48.9dB$ [1]

Gain not expressed in dB by several students. Also many units missing (e.g. Kohms).

c) Derive an expression for the gain error (for a finite open loop gain, but assuming an ideal output resistance) for the non-inverting configuration shown and evaluate for R_1=9KΩ and R_2=1KΩ: [8]

Ideally, $A_v = V_{out}/V_{in} = 1 + R_1/R_2 = 1+9K/1K= 10$ [1]
Considering finite $A_v = V_{out}/V_{in} =(1 + R_1/R_2)[1-(1 + R_1/R_2)(1/A_0)]$ [2 for cct. + 3 for expression]
Gain error = $(1 + R_1/R_2)(1/A_0)$ [1] = 10/280 = 3.6% [1] (A_v=9.6)

In many cases no working/derivation included.

d) Derive an expression for the closed loop gain considering the op-amps finite output impedance (Rout) and calculate the closed loop gain. [8]

$R_{out} = (r_{o5}||r_{o8})=10K\Omega||20K\Omega = 6.6K\Omega$ [1]
$A_v = V_{out}/V_{in} = [A_0(R_1+R_2)/(R_{out}+R_1+R_2)]/[1+(A_0R_2/(R_{out}+R_1+R_2)]$ [2 for cct. + 4 for expression]
$A_v = [280(10K)/(16.6K)]/[1+(280*1K/(16.6K)] = 9.4$ [1]

In many cases no working/derivation included.

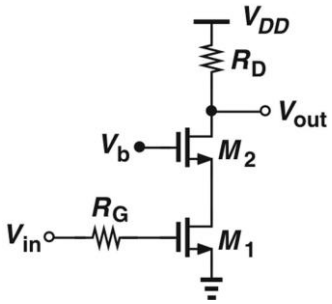
e) Give 2 improvements to the op-amp circuit (shown in Fig. 2.1(a)) if it is to be used in the non-inverting configuration (shown in Fig. 2.1(b)). [any 2 of the 3 given below] [2]

- Add compensation capacitor across the 2nd gain stage to improve the phase margin and stability of the amplifier when configured with feedback. [1]
- Add a buffer at the output to drive a resistive load. Current class A output is not appropriate for directly driving a resistive load. [1]
- Increase the open loop gain. [1]

Generally irrelevant and/or negligible improvements were stated. E.g. improving current mirror, gain bandwidth, compensating for bias currents, etc.

3. The circuit shown below is a two-stage amplifier consisting of a common source amplifier (M_1) followed by a common gate (M_2) stage (often referred to as a cascode).

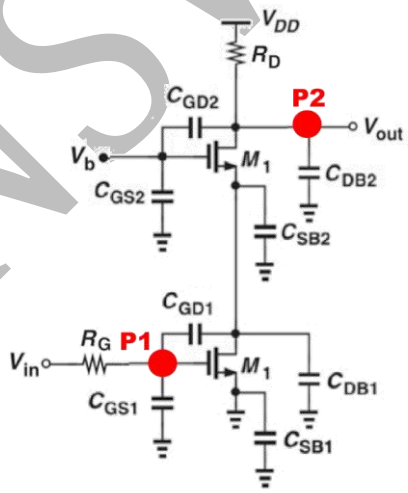
   Use the following parameters: V_{DD}=1.8V, $(W/L)_1=(W/L)_2$=50µm/0.18µm, $I_{D1}=I_{D2}$=2mA, $C_{GS}=(2/3)(WL)C_{ox}$, C_{ox}=15fF/µm^2, $\mu_n C_{ox}$=200µA/V^2, λ=0, $C_{SB}=C_{DB}$=0 and $C_{GD}=C_0W$, where C_0=0.2fF/µm denotes the gate-drain capacitance per unit width.



   a) Compare the frequency responses of a common source and common gate amplifier. [5]

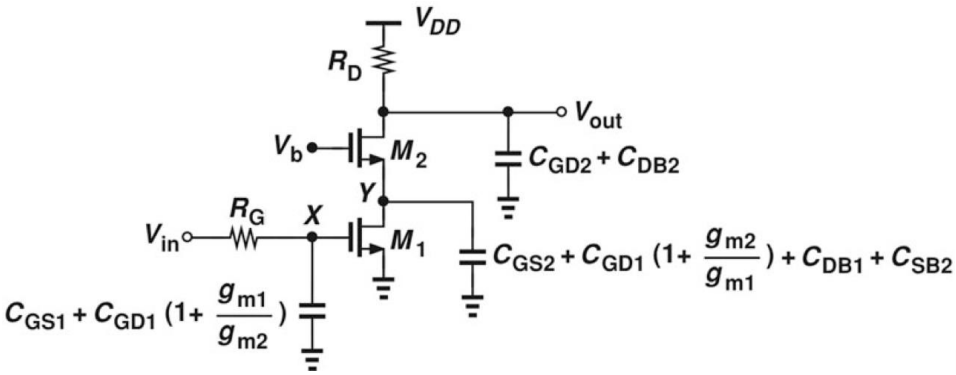
Common Source (CS) and Common Gate (CG) amplifiers have similar low frequency voltage gain (g_mR_D) except that CS is inverting and CG is non-inverting. [1] However, CG amplifier has better high frequency response than the CS due to the parasitic capacitances. [1] In case of the CS amplifier, the gate drain capacitance appears across the input/output terminal and is therefore subject to Miller multiplication (at the input). [1] This significantly impacts the amplifier bandwidth by lowering the frequency of the input pole (since the input-referred capacitance is C_{GD} multiplied by the gain). [1] In the case of the CG amplifier since the gate is at AC ground, there is no Miller effect. [1]

   b) Redraw the circuit above to: (i) identify any nodes that are associated with poles and (ii) include all the parasitic device capacitances (within $M_{1\text{-}2}$). [6]



[1] for identifying poles, [1] for disgarding V_{S1} node, [4] for parasitic capacitances.

   c) Redraw the circuit drawn in your answer to (b) to remove any redundant capacitances and lump together any parallel capacitances. Determine expressions for the different pole frequencies using Miller's theorem where appropriate. [6]



[4]

$F_{p1}=1/[2\pi*R_G*(C_{GS1}+C_{GD1}(1+A_{v1}))]$ [1]
$F_{p2}=1/[2\pi*R_D*(C_{DB2}+C_{GD2})]$ [1]

d) Determine an expression for the DC (low frequency) gain of the amplifier.

[3]

$A_v=A_{v1}*A_{v2} = -(g_{m1}/g_{m2}) * (g_{m2}R_D)$ [2] $= -g_{m1}R_D$ [1]

e) Evaluate the DC gain and pole frequencies, for $R_D=R_G=600\Omega$.

[6]

$g_{m1}= g_{m2}=\sqrt{(2I_{D1}(W/L)_2*\mu_nC_{ox})} = \sqrt{(2*2m*50/0.18*200\mu)} = 14.9mS$ [1]

$C_{GS1} = (2/3) * (WL) * Cox = (2/3) * (50 * 0.18) * 15f = 90fF$
$C_{GD1} = C_{GD2} = C_0W_1 = 0.2fF/\mu m * 50\mu m = 10fF$

$A_v = -g_{m1}R_D = 14.9mS * 600 = -8.9$ [1]

$F_{p1}=1/[2\pi*R_G*(C_{GS1}+C_{GD1}(1+A_{v1}))] = 1/[2\pi*600*(90f+10f(1+1))] = 2.4GHz$ [2]
$F_{p2}=1/[2\pi*R_D*(C_{DB2}+C_{GD2})] = 1/[2\pi*600*(0+10f)] = 26.5GHz$ [2]

Many students did not disregard the internal pole (VS1 node).

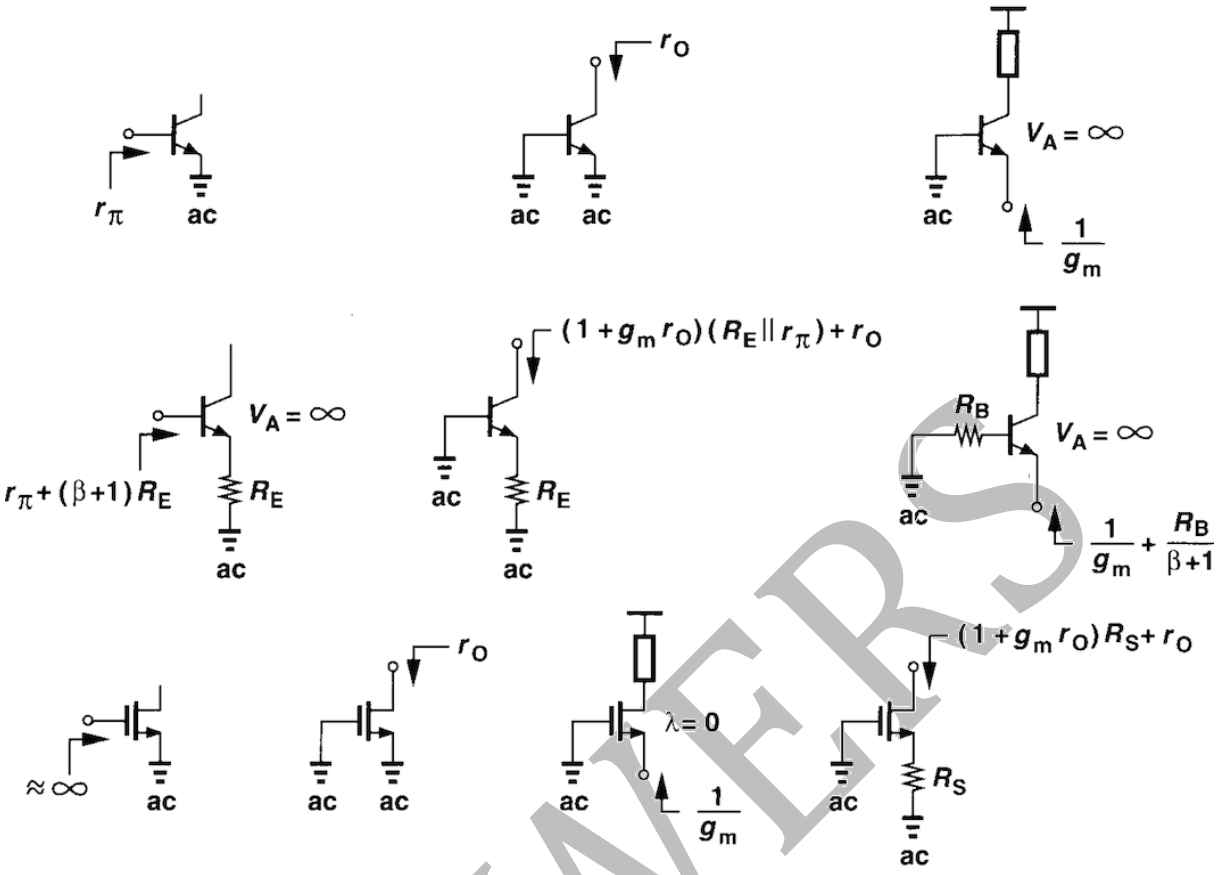
f) Describe how the DC gain can be increased. What is the limit?

[4]

DC gain expression (g_mR_D) implies gain can be increased by increasing transconductance (through either W/L or I_D) or R_D. [1] However I_DR_D places a fundamental limit on headroom which is power supply dependant. [1] Therefore, for a given $V_{DD,}$ a maximum value of R_D can be determined (based on I_D and V_{DD}) and then only W/L can be increased. [2]

Few students identified that the maximum gain is in fact limited by power supply.

Input and Output Impedances



Voltage Gain Equations