UNIVERSITY OF LONDON
IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2003

MSc in Computing Science
for Internal Students of the Imperial College of Science, Technology and Medicine

PAPER M2

ARCHITECTURE AND OPERATING SYSTEMS

Thursday 1 May 2003, 15:30
Duration: 120 minutes

Answer THREE questions

Paper contains 4 questions
Calculators required

Section A (Use a separate answer book for this section)

1 a The following are the data declarations for an 8086 assembler program

```
.data
cw      db 'west'      ; clockwise
acw     db 'east'      ; anticlockwise
inc     dw  25         ; up
dec     dw -25         ; down
```

List the contents of the corresponding byte locations in memory in hexadecimal (ASCII 'a' = 97 decimal, '$' = 36 decimal)

b i) How many memory locations can be addressed by a microprocessor with a 24-bit address bus?

ii) How many 256K x 4bit RAM chips are required to fill the address space?

iii) Using word-aligned memory with high-order interleave, which address lines are used for bank select? (Assume word = 16 bits).

c i) I/O (Input/Output) may be memory-mapped or use a separate I/O space. Describe them both, including any advantages and disadvantages of each technique.

ii) Explain *briefly* programmed I/O and interrupt-driven I/O.

iii) Differentiate between internal and external interrupts on the 8086. Explain how each is generated and how they are handled by the CPU.

The three parts carry, respectively, 30%, 30%, 40% of the marks.

Section B (Use a separate answer book for this section)

2 a i) Provide the Truth tables for the logical functions A OR B and A NAND B

ii) State DeMorgan's Rules.

iii) Explain how an OR gate can be built out of NAND gates. Sketch the circuit, showing how the inputs are connected via the NAND gates to the output.

b i) Derive expressions for the range of numbers that can be represented in n bits using Two's Complement, Sign and Magnitude and Bias-N. Include an advantage and disadvantage of each representation.

ii) Suppose that you need to extend the number of bits in a Two's Complement integer from n bits to m bits (m > n). Describe what is involved in preserving the value represented.

c The following C function returns the nth number in the Fibonacci series.

```
int fib(int n)
{
        if (n == 1) || (n == 2) /* n is 1 or n is 2 */
           return 1;
        else return fib(n-1) + fib(n-2)
}
```

Write the equivalent subroutine in 8086 assembler. Your solution should use a stack frame, preserve the contents of any registers used, and include **EQU**ate statements and informative comments

The three parts carry, respectively, 30%, 30%, 40% of the marks.

Section C *(Use a separate answer book for this Section)*

3 a McCann's fast food restaurant has four kinds of employees:

(1) Ordertakers, who take customers' orders (written on a piece of paper and placed on an order rack);
(2) Cooks, who take the order from the order rack and prepare the food and put it on a hotplate;
(3) Packaging Specialists, who put the food into bags from the hotplate;
(4) Cashiers, who give the bags to customers and take their money.

Each employee can be regarded as a communicating sequential process.

i) What form of interprocess communication do they use?

ii) The *Cook* and *Packaging Specialist* use an enclosed hot plate with only one door to open it to deposit and pick up burgers respectively. Write pseudocode for employee relationship operation using *semaphores*.

b Five batch jobs A through to E, arrive at the computer at almost the same time. They have estimated running times of 10, 6, 2, 4 and 8 minutes. Their (externally determined) priorities are 3, 5, 2, 1 and 4 respectively, with 5 being the highest priority. For each of the following scheduling algorithms, determine the mean processing turnaround time (process switching overhead should be ignored).

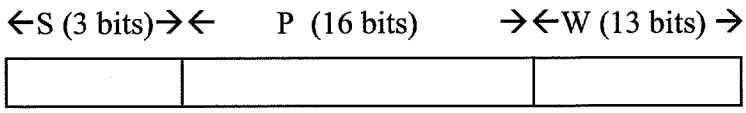
i) Round Robin
ii) Priority scheduling
iii) First-come first served (run order 10, 6, 2, 4, then 8)
iv) Shortest job first

For (i), assume that the system is multiprogrammed, and that each job gets its ***fair*** share of the CPU. For (ii) through (iv) assume that only one job at a time runs, until it finishes. All jobs are completely CPU bound.

The three parts carry, respectively, 60%, 40% of the marks.

Section D *(Use a separate answer book for this section)*

4 An operating system with a paged and segmented memory system has the following virtual address format:



a. Give two advantages of a paged and segmented memory system from a compiler writer's point of view. What is the primary disadvantage from a performance engineer's point of view?

b. What combination of read, write and execute protection bits are appropriate for a stack segment? Under what circumstances would it be appropriate to associate more than one stack segment with a process?

c. How big is the virtual address space associated with a process in the scheme described above? If there are 6 processes currently running on the system, how many segment tables and how many page tables are required? How many entries will there be in each segment table and in each page table?

d. Suppose a Translation Lookaside Buffer (TLB) is added to speed up address translation.

   i.) Given that the TLB is to be installed on a system that supports a maximum of 1GB RAM, draw a diagram to show the layout of each entry in the TLB (i.e. show the main components of each TLB entry with corresponding bit widths).

   ii.) If address translation time using the TLB is 10 times faster than using the usual segment and page table lookups, determine the TLB hit ratio necessary to reduce the average address translation time by 50%. You may assume that that segment and page table lookups only begin (where necessary) after a TLB miss.

The four parts carry, respectively, 15%, 15%, 25% and 45% of the marks.

End of paper