E3.11
AO8

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2004

MSc and EEE PART III/IV: MEng, BEng.and ACGI

ADVANCED ELECTRONIC DEVICES

Friday, 30 April 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer Question ONE and THREE other questions.

Question One carries 30 marks. All other questions carry 20 marks.

Corrected Copy

Nine

Any special instructions for invigilators and information for candidates are on page 1.

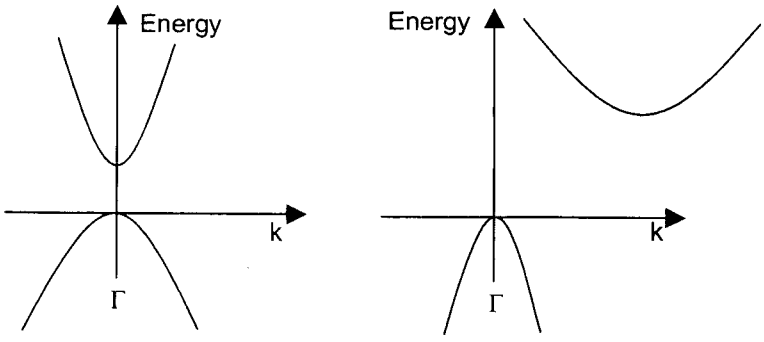
Examiners responsible First Marker(s) : K. Fobelets
Second Marker(s) : A.S. Holmes

1. **This question is obligatory. Weighting is 3/2.**

a) The dispersion relations of two semiconductors (semiconductor 1 and semiconductor 2) are given in Figure 1.1.

i) In each case indicate if the semiconductor is a direct or indirect bandgap material. [2/3]

ii) Give the relative relationship (>,<,=) of the effective mass of the conduction band between the two materials and give a short reason for this. [2/3]



Semiconductor 1, m_1^* Semiconductor 2, m_2^*

Figure 1.1: The dispersion relation of two semiconductors

b) Consider an n-channel JFET and an n-channel MESFET, both in GaAs, with the same geometrical dimensions and doping densities in channel and substrate.

i) Which of the two FETs will have the most leaky gate and why? [2/3]

ii) Which of the two FETs will switch fastest and why? [2/3]

c) Take the layer structure given in Figure 1.2.

i) Sketch the energy band diagram of this structure without external bias. [4/3]

ii) Sketch the current-voltage (IV) characteristic of the device and add the energy band diagrams associated to i) the IV region before substantial current is flowing, ii) the IV region before the negative differential resistance, iii) at the peak current and iv) the IV region after the negative differential resistance. [8/3]

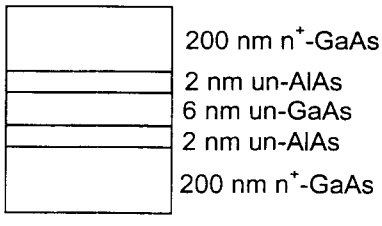


Figure 1.2: Hetero-junction layer structure consisting of AlAs and GaAs

d)

i) In CMOS, give the reason why the gate of the MOSFET is highly doped polySi and not metal. [4/3]

ii) Give the processing steps (briefly) and equipment needed to define 60 nm (short gate length) polySi gates on the gate oxide. [6/3]

e)

i) Draw the energy band diagram (E_c, E_v, and E_F) from emitter to collector of a n+ AlGaAs – p GaAs – n GaAs Heterojunction bipolar transistor. Indicate any conduction or valence band offsets. [6/3]

ii) Why is the current gain of the HBT improved compared to the BJT? [2/3]

f) Drain induced barrier lowering (DIBL) is a FET short-channel effect that influences the characteristics of especially short channel FETs.

i) Demonstrate the reason for increased currents when DIBL is important. Use the device cross-section (including depletion regions) and the potential distribution to compare a long gate to a short gate FET, at low V_{DS}. [8/3]

ii) Suggest a method to reduce DIBL in short channel devices. [2/3]

g) Si and Ge are miscible for all concentrations. The lattice constant of Ge is 4% larger than the lattice constant of Si. Assume a thin layer of Si is grown on a thick good quality layer of $Si_{0.7}Ge_{0.3}$.

i) Sketch the lattice constant of the Si atoms in relation to the lattice constant of the SiGe layer parallel and perpendicular to the growth direction. [4/3]

ii) Give two parameters, related to the mobility of the carriers in the thin Si layer, that will be changed in this heterojunction compared to these parameters in bulk Si. Explain briefly their influence on the mobility. [8/3]

2. The energy band diagram of both un GaAs and p^+ AlGaAs is given relative to the vacuum level in Figure 2.1.

a) Draw the energy band diagram when the two materials are brought into contact. [8]

b) What is the use of the resulting heterojunction? [2]

c) Derive the expression for the depletion width in this heterojunction. [10]
Remember that the Poisson equation is given by:

$$\frac{d}{dx}\varepsilon(x)E(x) = q\rho(x)$$

the carrier density is given by:

$$n = N_C \exp\left(-\frac{E_c - E_F}{kT}\right)$$

$$p = N_v \exp\left(-\frac{E_F - E_v}{kT}\right)$$

Make sure that in your derivation you write down the boundary conditions.

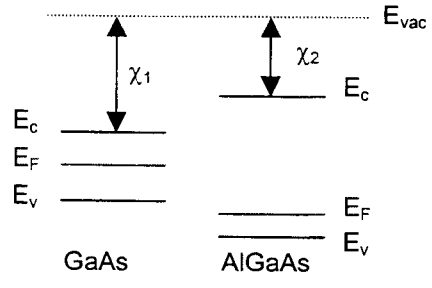


Figure 2.1: Heterojunction energy band diagram of p^+-AlGaAs and un-GaAs before contact, relative to the local vacuum level

3.

a) Why is it usually important in epitaxial growth of semiconductor materials that the materials are lattice matched? Describe what happens during the growth of unmatched materials (e.g. SiGe on Si) and describe the way in which the stress is finally relieved. Use sketches of the relative lattice constants variation to make your explanations clear. [7]

b) Give three mobility limiting mechanisms in classical n-channel Si MOSFETs and give an alternative layer structure that solves these three problems? Describe why the proposed layer structure reduces the mobility limiting mechanisms. [7]

c) Usually the *unstrained* ternary compound InGaAs is grown on top of an InP substrate. From the diagram given in Figure 3.1, *estimate* with an explanation of your reasoning:

i) the bandgap of the chosen InGaAs compound; [3]

ii) the composition of InGaAs for unstrained growth. [3]

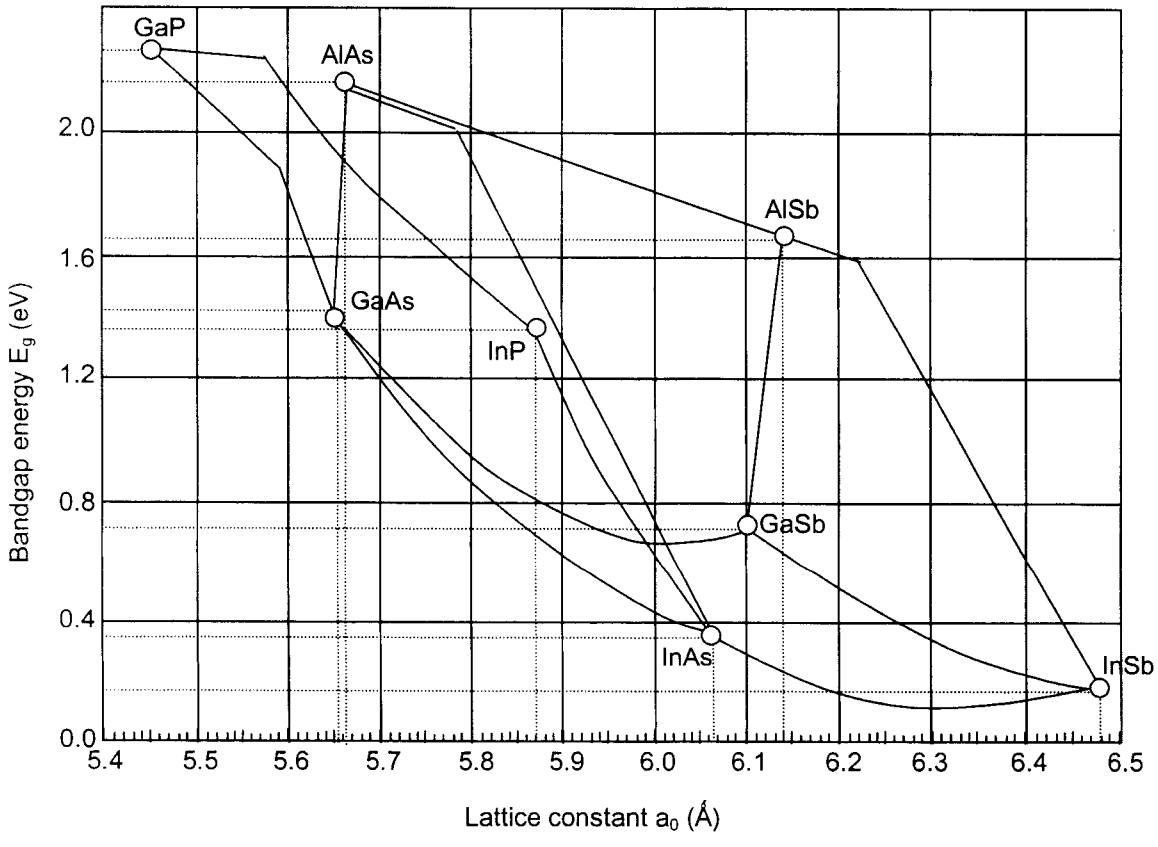


Figure 3.1 Bandgap energy and lattice constant of various III-V materials at room temperature [from Tien, 1988]

4.

a) Sketch simplified cross-sections of the two following devices.

i) processed planar npn AlGaAs/GaAs HBT. [3]

ii) processed Si n-channel GaAs MESFET. [3]

Ensure you have the doping type and relative doping density correct in all the areas of interest. Define the contacts E,B,C (emitter, base, collector) and S,G,D (source, gate, drain) as applicable.

b) Sketch the energy band diagrams under equilibrium (no voltages applied) for the above structures

i) AlGaAs/GaAs HBT. [4]

ii) GaAs MESFET. [4]

From emitter to collector and gate to substrate, respectively.

c) Calculate the ratio of the input resistance of a depletion mode MESFET to the input resistance of an HBT when the following parameters of your devices are known. [6]

i) HBT: is in active mode, the output resistance r_{ce} is large, the base spreading resistance $r_{bb'}$ is small, $\beta = 500$ and $g_m = 0.1$ S.

ii) MESFET: the gate is biased at $V_{GS} = -0.1$V, R_s is small, $I_{off} = 10$ nA and $g_m = 0.2$ S.
Assume $\frac{kT}{q} = 0.0259\,V$.

5.

a) Sketch the external connections to an FET in DT-mode (dynamic threshold) operation. [6]

b) Explain how the threshold voltage is varying under DT-mode operation and explain how this differs from the normal case where the bulk is connected to the source. [5]

c) The sub-threshold slope S in FETs is given by the simplified expression:

$S = 2.3\frac{kT}{q}\left(1+\frac{C_D}{C_i}\right)$ with C_D the depletion capacitance and C_i the insulator capacitance. Is the sub-threshold slope S of a MOSFET in DT-mode operation larger or smaller than in normal operation? Give an explanation for your answer. [4]

d) Estimate the sub-threshold slope S of an FET for which the transfer characteristics at low drain voltage are given in Figure 5.1. [5]

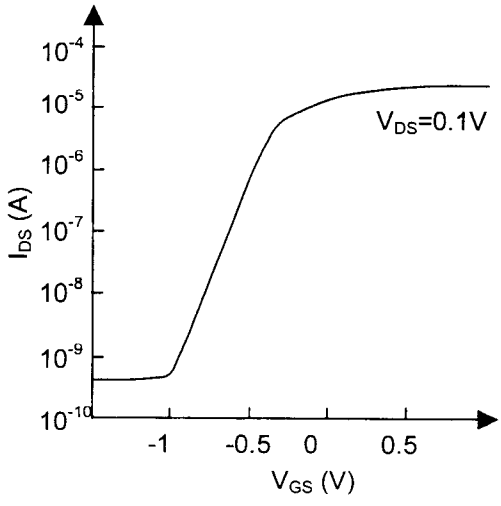


Figure 5.1: Logarithmic transfer characteristic of an FET

6. To describe static low dimensional semiconductor structures, the Schrödinger equation is used:

$$\left[-\frac{\hbar^2}{2m}\frac{d^2}{dx^2}+V(x)\right]\Psi(x)=E\Psi(x)$$

a) Consider the situation of an infinitely deep quantum well, as shown in Figure 6.1.

i) Write the Schrödinger equation inside the quantum well. [1]

ii) Give the expression of the general solution to the Schrödinger equation in the quantum well. [2]

iii) Give the equations needed to find the integration constants in the general solution given in ii). What is the physical interpretation of these equations? [2]

iv) Sketch the wave functions on energy levels 1, 2 and 3 in the quantum well. [3]

b) Compare and discuss the wavefunctions on the different energy levels in the quantum well with infinitely high potential barriers to the case with a finite potential well. [4]

c) Consider a finite potential barrier of width *a*.

i) Sketch the amplitude of the electron wave through the single barrier structure in the case of a thin barrier (a = 5 nm). [3]

ii) Sketch the amplitude of the electron wave through the single barrier structure in the case of a thick barrier (a = 500 nm). [3]

iii) Can a resonant tunnelling diode be made using 500 nm barriers? Explain your answer. [2]

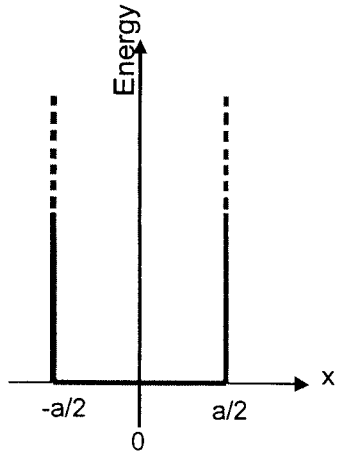


Figure 6.1: Quantum well with infinite potential barriers

Solutions - 2004

ADVANCED ELECTRONIC DEVICES [E3.11] ~~[E4.42]~~ A08

1 **Obligatory question. Total mark is 30.**

a)

i) semiconductor 1 has a direct bandgap
semiconductor 2 has an indirect bandgap [1]

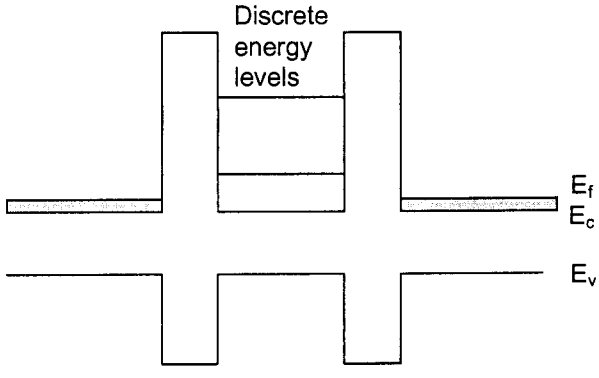
ii) $m_1^* < m_2^*$. The effective mass is given by the relationship: $m^* = \frac{\hbar^2}{d^2E/dk^2}$. As the curvature of the dispersion relation in the conduction band minimum of semiconductor 1 is higher than that of semiconductor 2, thus its effective mass is smaller. [1]

b)

i) MESFET is most leaky because the Schottky barrier reverse bias current is larger than the pn junction reverse bias current of the JFET. [1]

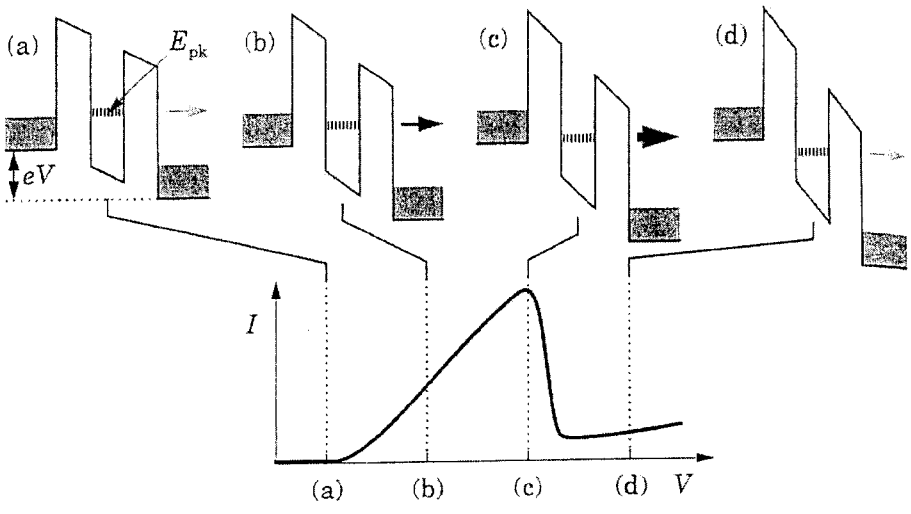
ii) The MESFET will switch fastest as it is a majority carrier device and does not store minority carriers at the junction that will take time to disappear before switching can happen. [1]

c) i)



[2]

ii)



[4]

d)

i) To enable a self-aligned source-drain process where the gate is used as implantation mask for source and drain contact after which a high temperature annealing steps needs to be done that would melt the metal.

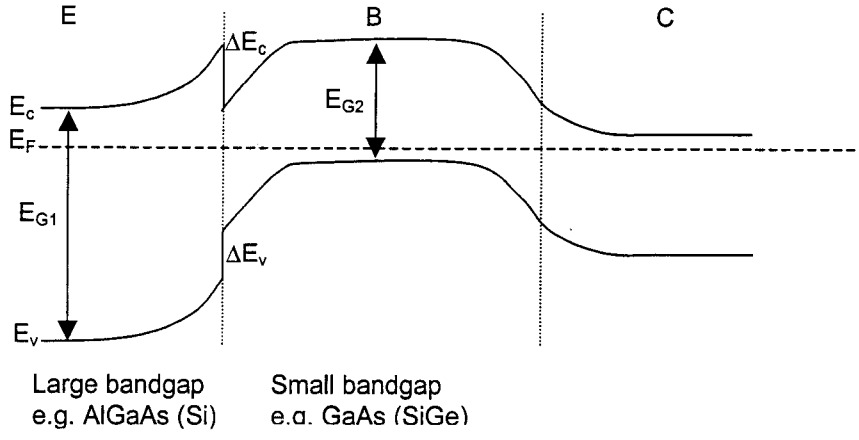
[2]

ii) a) deposit polySi using a CVD (chemical vapour deposition)
b) implant polySi using an ion implanter
c) lithography to define the gates using e-beam lithography

[3]

e)

i)

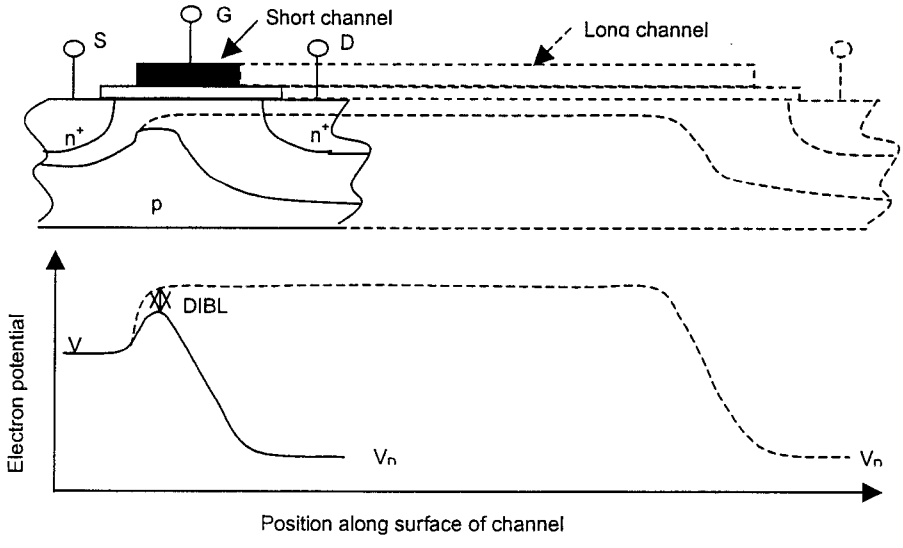


[3]

ii) because the loss of holes from the base into the emitter under forward bias emitter-base junction is blocked by the valence band offset in the valence band at the E-B junction. [1]

f)

i)

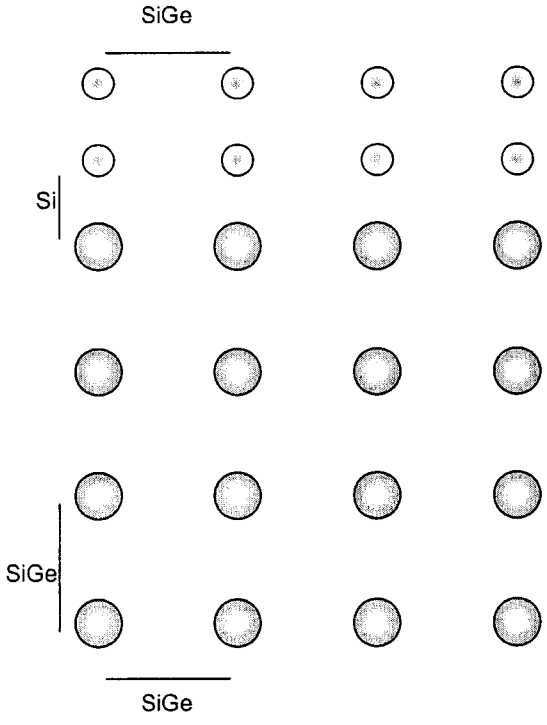


[4]

ii) Increase the doping density underneath the gate channel such that depletion from the barrier does not easily extend into the weakly doped region underneath the channel. [1]

g)

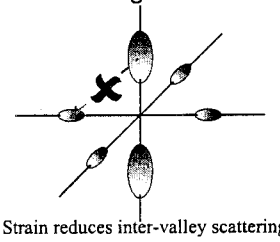
i)



[2]

ii) The thin Si layer is under tensile strain, this will split the degenerate conduction band minima, lowering the two Δ2 levels in energy and increasing the four Δ4 levels in energy. This has two consequences:

a) Intervalley scattering between the Δ2 and Δ4 valleys. Remember that $\mu \propto \frac{\tau}{m}$. τ (average time between scattering events) increases due to the removal of scattering event.



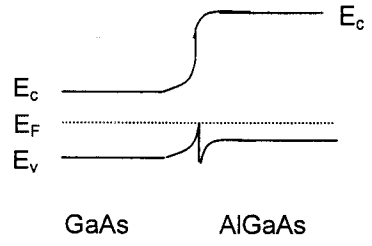
Strain reduces inter-valley scattering

b) In tensile strain, only the transverse mass of the Δ2 valleys contribute to the transport perpendicular to the growth directions. The transverse mass is smaller than the longitudinal mass. [4]

Remember that $\mu \propto \frac{\tau}{m}$, for smaller m (mass) we find higher mobility.

2.

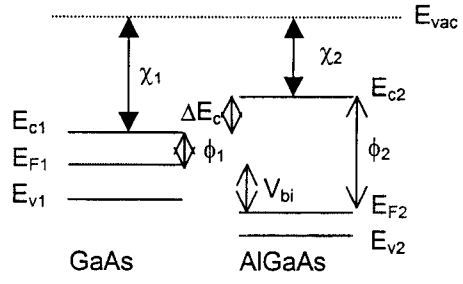
a)



[8]

b) p-HEMT [2]

c)



The built-in voltage is the difference between the Fermi level at either side of the junction:

The poisson equation is:

$$\frac{dE(x)}{dx} = \frac{q}{\varepsilon}(p - n + N_d^+ - N_a^-)$$

In the transition region we neglect n and p, then we have two regions with constant space charge for we can write (abrupt junction) :

$$E_{F2} + \phi_2 - \Delta E_c - \phi_1 = E_{F1}$$

$$E_{F1} - E_{F2} = -\Delta E_c + \phi_2 - \phi_1$$

$$eV_{bi} = -\Delta E_c - kT\ln\left(n_2/N_{C2}\right) + kT\ln\left(n_1/N_{C1}\right)$$

$$eV_{bi} = -\Delta E_c - kT\ln\left(n_2 N_{C1}/n_1 N_{C2}\right) \quad (0)$$

In the GaAs depletion region: $-w_{n1}<x<0$:

$$\frac{dE}{dx} = \frac{eN_{D1}}{\varepsilon_1}$$

In the AlGaAs depletion region: $0<x<w_{n2}$:

$$\frac{dE}{dx} = \frac{eN_{D2}}{\varepsilon_2}$$

Integrate across depletion width for the two regions:

$$E_1 = \frac{eN_{D1}}{\varepsilon_1}x + C_1$$

$$E_2 = \frac{eN_{D2}}{\varepsilon_2}x + C_2$$

Taking into account that the electric field outside the depletion regions is zero gives:

@ x=$-w_{n1}$ E=0

$$E_1 = \frac{eN_{D1}}{\varepsilon_1}(x + w_{n1})$$

@ x=w_{n2} E=0

$$E_2 = \frac{eN_{D2}}{\varepsilon_2}(x - w_{n2})$$

Continuity in displacement field is: $D_1=D_2$ @ x=0

$$\varepsilon_1 E_1 = \varepsilon_2 E_2 \,@\, x = 0 \rightarrow (eN_{D1}w_{n1}) = (eN_{D2}w_{n2}) \quad (1)$$

Integrating a second time for the potential: V=-dE/dx

$$-\Delta V = \int_{-w_{n1}}^{w_{n2}} E\,dx = \int_{-w_{n1}}^{0} \frac{eN_{D1}}{\varepsilon_1}(x + w_{n1})dx + \int_{0}^{w_{n2}} \frac{eN_{D2}}{\varepsilon_2}(x - w_{n2})dx$$

$$-\Delta V = -V_{bi} = \frac{eN_{D1}}{2\varepsilon_1}\left(w_{n1}^2\right) + \frac{eN_{D2}}{2\varepsilon_2}\left(w_{n2}^2\right) \quad (2)$$

solving (1) and (2) gives:

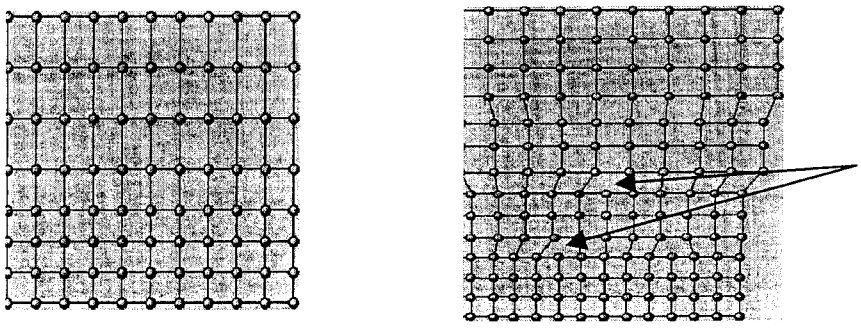
$$w_{n1}^2 = \frac{2\varepsilon_1\varepsilon_2 N_{D2}V_{bi}}{eN_{D1}(\varepsilon_1 N_{D1} + \varepsilon_2 N_{D2})}$$

$$W_{n2}^2 = \frac{2\varepsilon_1\varepsilon_2 N_{D1}V_{bi}}{eN_{D2}(\varepsilon_1 N_{D1} + \varepsilon_2 N_{D2})}$$

The expression of V_{bi} can be found in (0). [12]

3.

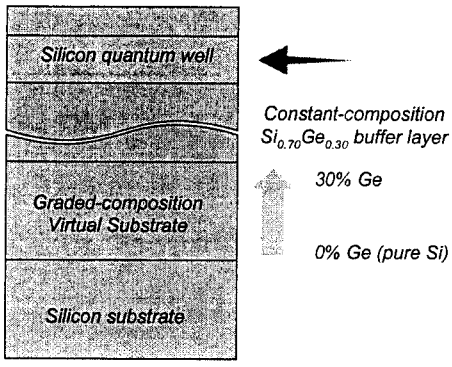
To allow *single crystalline* material. For growth of thin layers on top of a lattice relaxed thick layer, the *thin* layer will *adapt* to the in-plane lattice constant of the thick layer. When the layer becomes wider than the critical thickness, *strain relaxation* will occur and the grown layer will try to *recover* its *own* lattice constant. This relaxation manifests itself as *dislocations* that propagate through the layer that is being grown. Under controlled growth conditions the dislocations are *in-plane* (perpendicular to the growth direction) while in uncontrolled growth the dislocation will *propagate in the direction* of the growth.



Left: thin strained layer, in-plane lattice constant equal to substrate. Right: thick strain-relaxed layer, strain relaxation due to misfit dislocations (see arrows).

[7]

b) Intervalley scattering
Oxide roughness scattering
Impurity and defect scattering



Strained Si MODFET
Modulation doping removes the doping atoms from the channel and reduces impurity and defect scattering.
Strain in the Si layer: splits the conduction band valleys (Δ_2 are lowered and Δ_4 are increased) such that intervalley scattering is negligible.
The buried channel configuration places the channel away from the SiO_2 interface.

[7]

c) For unstrained growth, the lattice constant of the InGaAs alloy must be the same as InP and from fig.3.1 we find 5.87Å. The line on the figure that connects GaAs with InAs, gives the variation of the bandgap of the InGaAs alloy. *estimate* with an explanation of your reasoning

i) The value of the InGaAs alloy line at 5.87Å gives the bandgap and gives roughly 0.7 eV. (values between 0.6 and 0.8 are acceptable as estimation). [3]

ii) To make an **estimation,** we assume that the energy bandgap varies linearly with composition. That means that for $In_{1-x}Ga_xAs$ we can write the bandgap variation as:

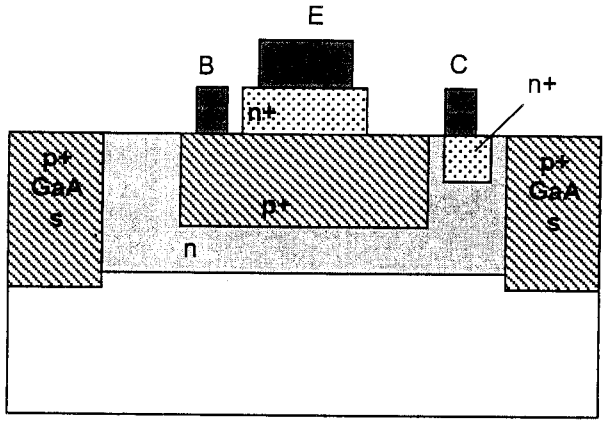
$$E_g^{InGaAs}(x) = xE_g^{GaAs} + (1-x)E_g^{InAs}$$

0.7 = x 1.4 + (1-x) 0.4
x = 0.3 [3]

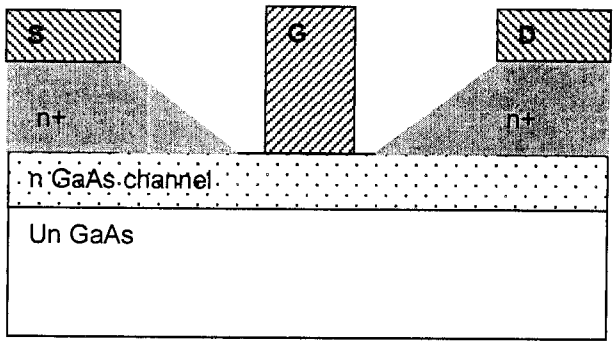
4.

a)

i) GaAs HBT. [3]

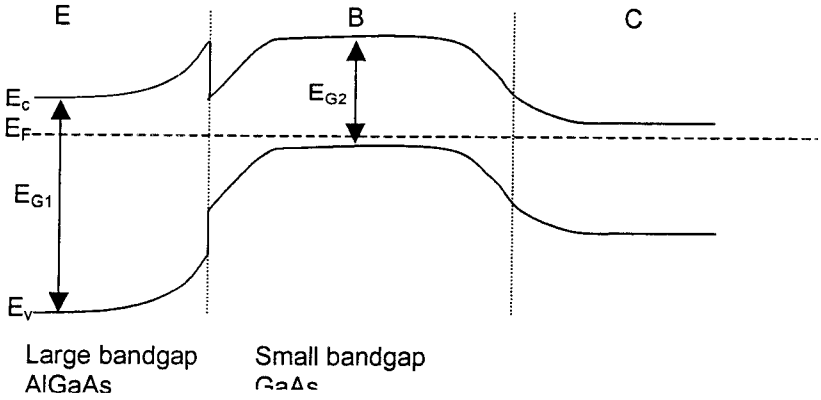


ii) GaAs MESFET. [3]



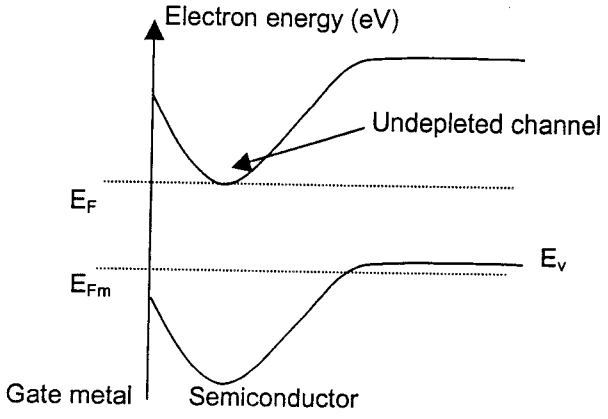
b) Sketch the energy band diagram under equilibrium (no voltages applied) for the above structures

i) AlGaAs/GaAs HBT: from emitter to drain. [4]



[E3.11]
[E4.42]
A08
[4]

ii) GaAs MESFET: from gate to substrate.



c) Calculate the ratio of the input resistance of the MESFET (in reverse bias) to the input resistance of the HBT (in active mode) when the following parameters of your devices are known. [6]

i) The input resistance of the HBT under the given circumstances is $r_{b'e}$.

$$r_{b'e} = \frac{v_{b'e}}{i_b}$$

$$g_m = \frac{dI_c}{dV_{b'e}} = \frac{i_c}{v_{b'e}} \quad \text{when } r_{ce} \text{ is large}$$

$$i_c = \beta i_b$$

$$r_{b'e} = \frac{\beta}{g_m} = \frac{500}{0.1} = 5000\Omega$$

ii) Input resistance of a FET is defined as:

$$r_{in} = \left(\frac{dI_g}{dV_g}\right)^{-1}$$

$$I_g = I_{off}\left(e^{\frac{qV_g}{kT}} - 1\right)$$

$$\frac{dI_g}{dV_g} = \frac{qI_{off}}{kT} e^{\frac{qV_g}{kT}} = \frac{q}{kT}\left(I_g + I_{off}\right)$$

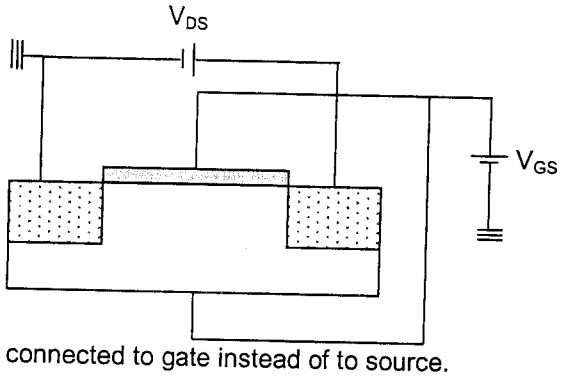
For V_{GS}=-0.1:

$$r_{in} = \left(\frac{qI_{off}}{kT} e^{\frac{-0.1}{0.0259}}\right)^{-1} = \left(\frac{10^{-8}}{0.0259} 0.021\right)^{-1} = 1.23\,10^8\Omega$$

The ratio of the input resistances:

$$\frac{r_{in}}{r_{b'e}} = \frac{1.23\,10^8\Omega}{5000\Omega} = 24.6\,10^3$$

5. a)



substrate is connected to gate instead of to source. [6]

b) Assume an n-type FET. Applying a positive voltage on the gate will create an inversion layer at the same time a positive voltage is applied to the substrate which forward biases the inversion layer n – substrate p junction decreasing the depletion at both sides of the junction and thus decreasing the threshold voltage. This implies that the FET will switch on at lower gate voltage.
When applying a negative voltage on the gate, the inversion layer is reduced and the inversion layer n – substrate p junction because reverse biased and thus the depletion region from the substrate is extending into the channel region, switching off the channel faster. Thus the threshold voltage is shifted to improve resp. switch on and switch off performance. In normal mode the threshold voltage for on and off is the same [5]

c) The sub-threshold slope is smaller in DT mode operation due to the smaller depletion capacitance C_D in the DT mode configuration. [4]

d) $$S = \left(\frac{d\log(I_{DS})}{dV_{GS}}\right)^{-1} = \left(\frac{-6-(-9)}{-0.3-(0.9)}\right)^{-1} = 200\frac{mV}{dec}$$ [5]

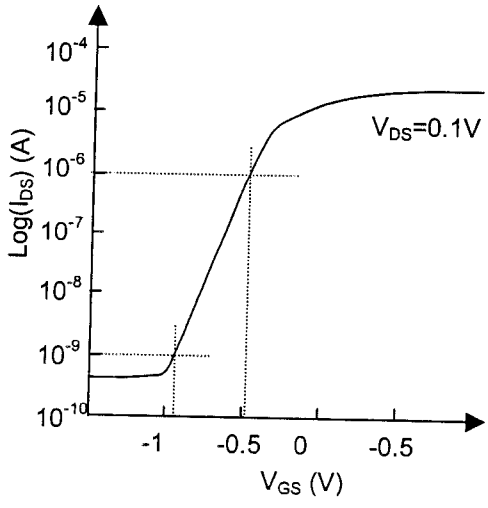


Figure 5.1: Logarithmic transfer characteristic of an FET with estimated values (dotted lines).

6.

[E3.11]
[E4.42]
A08

a)

i) $$-\frac{\hbar^2}{2m}\frac{d^2\Psi(x)}{dx^2} = E\Psi(x)$$ [1]

ii) $$\psi(x) = A\exp(ikx) + B\exp(-ikx)$$ [marks]

with k the wave vector $k = \sqrt{\frac{2mE}{\hbar^2}}$, A and B integration constants. [2]

iii)

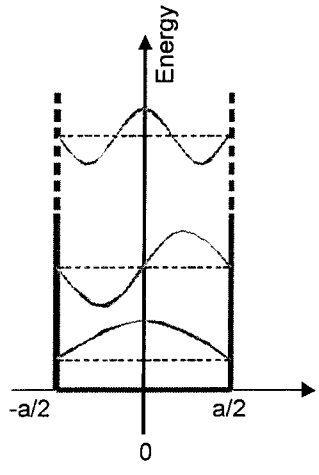
$$\psi\left(x = -\frac{a}{2}\right) = 0 = \psi\left(x = \frac{a}{2}\right)$$

or

$$\begin{cases} A\exp\left(ik\frac{a}{2}\right) + B\exp\left(-ik\frac{a}{2}\right) = 0 \quad \text{at } x = \frac{a}{2} & \text{(i)} \\ A\exp\left(-ik\frac{a}{2}\right) + B\exp\left(ik\frac{a}{2}\right) = 0 \quad \text{at } x = -\frac{a}{2} & \text{(ii)} \end{cases}$$

These expressions describe the continuity of the wavefunction in the quantum well at the boundary. In the infinitely high quantum well, no wave can exist outside the well. [2]

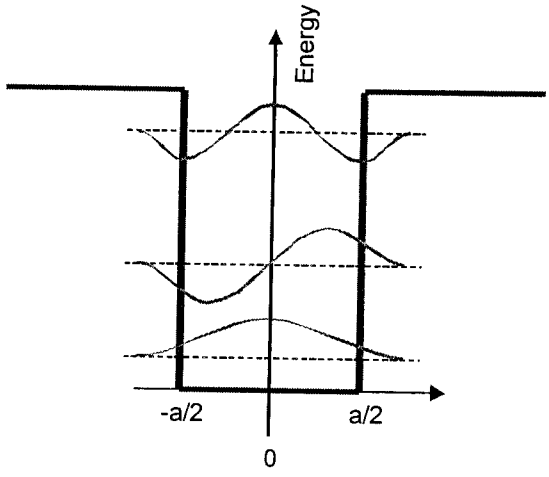
iv)



[3]

[E3.11]
[E4.42]
A08

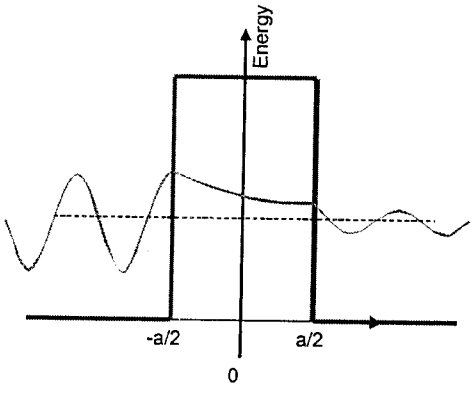
b)



In the infinite quantum well, the wavefunctions are zero at the boundary while in the case of the finite barrier quantum well, the wavefunctions decay exponentially into the barriers. [4]

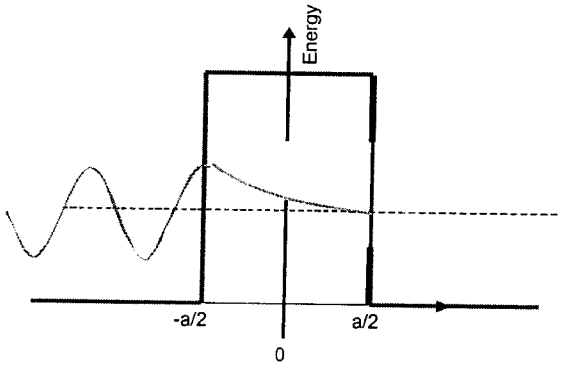
c)

i)



[3]

ii)



[3]

[E3.11]
[E4.42]
A08

iii) No because the probability for tunnelling through a thick barrier is almost zero.

OR

See the thick single barrier wavefunction for the thick barrier as given in c)ii). The wavefunction at the right edge of the barrier (output) is equal to zero and therefore no wave can exist after the barrier as a consequence of the boundary condition. [2]