IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2004

EEE/ISE PART I: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 1

Monday, 24 May 10:00 am

Time allowed: 2:00 hours

There are FIVE questions on this paper.

Answer THREE questions.

All questions carry equal marks

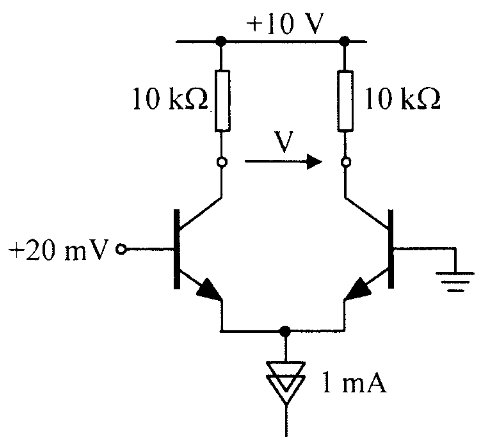
Corrected Copy

Any special instructions for invigilators and information for candidates are on page 1.

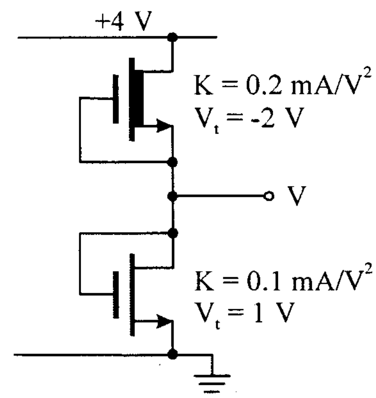
Examiners responsible First Marker(s) : A.S. Holmes
Second Marker(s) : S. Lucyszyn

1. For each of the circuits in Figure 1 below, determine the operating mode(s) of the transistor(s), and calculate the value of the current I or voltage V. State clearly any assumptions made in your calculations.

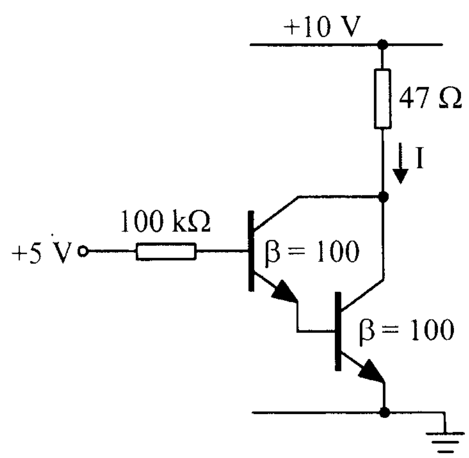
(a) [6 marks]



(b) [5 marks]



(c) [5 marks]



(d) [4 marks]

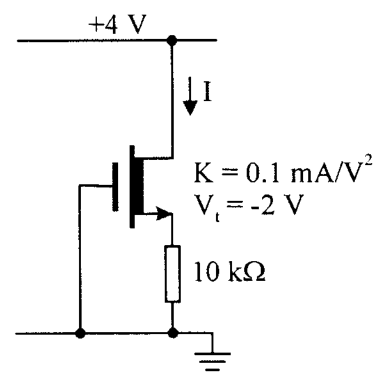


Figure 1

2. Figure 2 shows a band-pass filter comprising a common-emitter amplifier with a resonant load. You may assume in parts (a), (b) and (c) that the reactive components are ideal.

(a) Choose the value of R_B to give a collector bias current of 1 mA, stating clearly any assumptions you make. Also determine the quiescent output voltage of the circuit. [4]

(b) Draw a small-signal equivalent circuit of the filter, assuming the input capacitor to be a short-circuit. Hence show that the small-signal voltage gain A_v is given by:

$$A_v = -g_m (Z_{LC} // r_o)$$

where g_m and r_o are the transconductance and output resistance of the transistor, and Z_{LC} is the impedance of the resonant load. What is the numerical value of A_v at resonance? [8]

(c) Assuming the bias conditions in part (a), choose the values of L and C to give a centre frequency of 1 MHz and a Q of 100. [4]

(d) A filter is constructed with the component values derived by you in parts (a) and (c). When tested it is found to have a Q of only 60. Estimate the equivalent series resistance of the inductor, assuming this is responsible for the lower Q. [4]

Note: the Q of a parallel RLC network is $2\pi foRC$ where fo is the centre frequency.

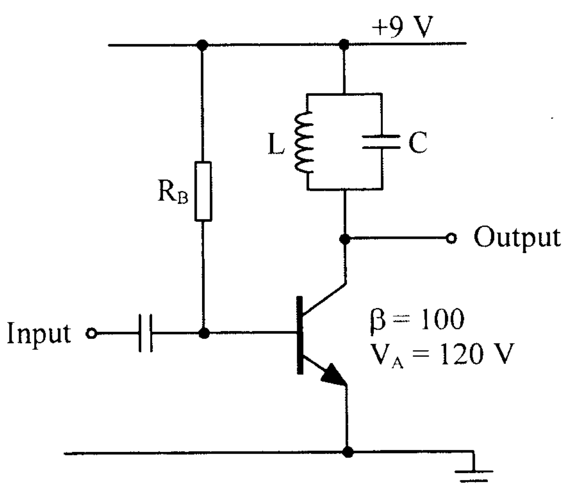


Figure 2

3. Figure 3 shows a single-stage CMOS amplifier in which both MOSFETs contribute to the small-signal gain.

(a) Explain the role of the resistor R_G, and show that the quiescent output voltage V_{OUT} is given by:

$$V_{OUT} = \frac{V_{DD} + V_{t2} + V_{t1}\sqrt{(K_1/K_2)}}{1 + \sqrt{(K_1/K_2)}}$$

where the symbols K and V_t denote the usual MOSFET parameters, and the subscripts 1 and 2 refer to Q1 and Q2 respectively.

Hence determine the value of V_{OUT}, and the quiescent drain current in each MOSFET. [8]

(b) Draw a small-signal equivalent circuit of the amplifier, including R_G, and calculate the small-signal voltage gain at frequencies for which the input capacitor is effectively short-circuit. Also determine the small-signal input resistance. [8]

(c) If a sinusoidal input signal is applied to the amplifier, over what range of input signal amplitudes will both transistors remain active? You may assume that the input capacitor has negligible impedance at the signal frequency. [4]

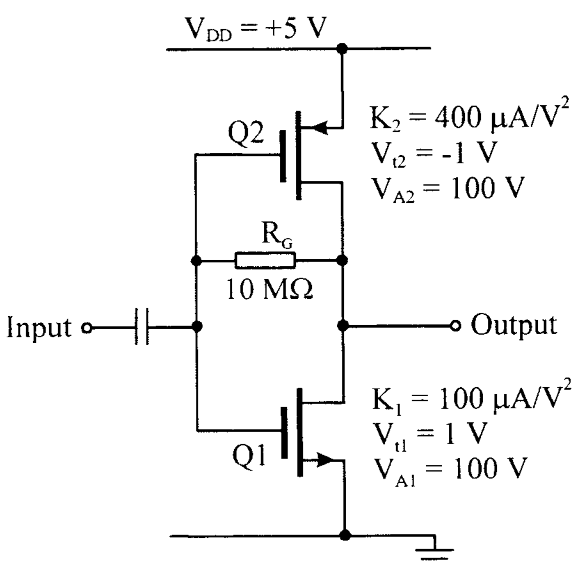


Figure 3

4. (a) Discuss briefly the relative merits of Class A, Class AB and Class B output stages. [4]

(b) Figure 4 shows an idealised Class AB output stage in which the output transistors are biased using two voltage sources, each of magnitude V_B.

Show that, if the transistors are matched and base currents are neglected, the collector currents I_N and I_P satisfy the following relations:

$$I_N - I_P = I_L \quad \text{and} \quad I_N I_P = I_Q^2$$

where I_L is the current into the load, and $I_Q = I_S \exp(V_B / V_T)$.

What is the significance of the quantity I_Q? [6]

(c) On the same axes, sketch the variations of I_N and I_P with load current for load currents in the range $-10I_Q < I_L < +10I_Q$. Also calculate the relative magnitudes of I_N and I_P for the cases $I_L = I_Q$ and $I_L = 10I_Q$. [6]

(d) Give one example of how the bias sources of Figure 4 can be implemented in a practical circuit. Your answer should include a circuit diagram of your chosen configuration. [4]

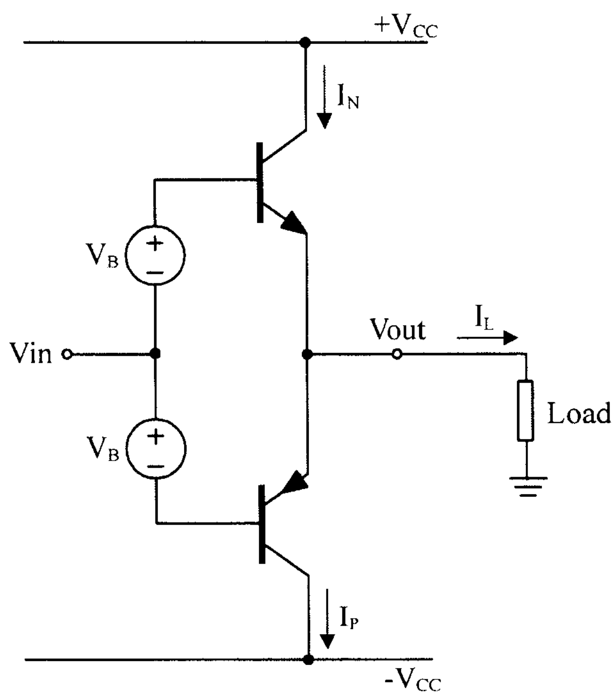


Figure 4

5. The circuit in Figure 5 is to be used to generate a positive-going, square pulse each time the push-button S1 is pressed. Both transistors have $\beta = 200$.

(a) What will be the voltages at the base and collector terminals of Q1 and Q2 when the switch has been open for a long time? Explain your reasoning. [6]

(b) Assuming starting conditions as in (a), derive an expression for the time variation of the base voltage of Q2 when the switch is pressed and held. Sketch this function, and show on the same axes the corresponding time variation of V_{OUT}. Your sketch should start just before the switch is pressed, and continue until just after the end of the output pulse.

What is the duration of the output pulse? [10]

(c) What is the purpose of the resistor R_F? How would the behaviour of the circuit differ if this resistor were omitted? [4]

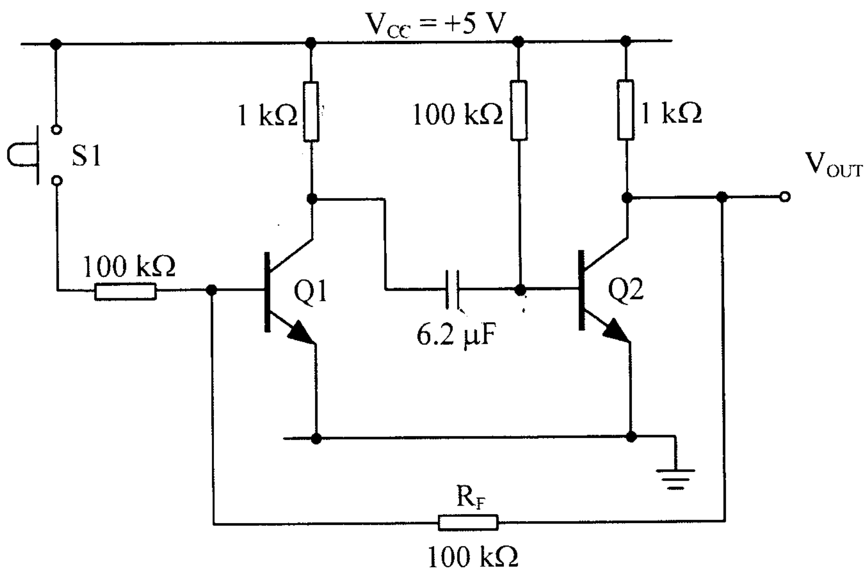


Figure 5

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E1.4

1 (a) Differential input voltage $\sim V_T$ $\Rightarrow$ use large signal equations

$$I_{C1} = \frac{I}{1 + e^{-V_D/V_T}}, \quad I_{C2} = \frac{I}{1 + e^{V_D/V_T}} \quad \text{where } I = 1\,\text{mA}$$

$V_D = 20\,\text{mV}$, $V_T = 25\,\text{mV}$

$\Rightarrow I_{C1} = 0.69\,\text{mA}$, $I_{C2} = 0.31\,\text{mA}$

$V_{C1} = 10 - I_{C1} \times 10k = 3.1\,V$, $V_{C2} = 10 - I_{C2} \times 10k = 6.9\,V$

So: $\underline{\underline{\text{Both transistors ACTIVE}}}$, with $\underline{\underline{V = 6.9 - 3.1 = 3.8\,V}}$

NB: Small-signal analysis leading to $V = 4V$ also acceptable 6

(b) Lower FET Q1 is ACTIVE ($V_{GD} = 0$); Upper FET Q2 needs checking

If both active, then $I_D = K_2 V_{t2}^2 = 0.8\,\text{mA} = K_1(V - V_{t1})^2$

$\Rightarrow V = 1 + 2\sqrt{2} = 3.83\,V$. But this value of V is inconsistent with Q2 being active, since in implies $V_{DS2} = 0.17 < -V_{t2}$.

So: $\underline{\underline{\text{Lower FET ACTIVE}}}$, $\underline{\underline{\text{Upper FET TRIODE}}}$

Now have to solve $I_D = K_2\left[2(-V_{t2})(4-V) - (4-V)^2\right] = K_1(V - V_{t1})^2$

$\Rightarrow 2V(4-V) = (V-1)^2$ or $3V^2 - 10V + 1 = 0$ $\Rightarrow V = 3.23$ or 0.1

second solution puts Q1 below threshold, $\Rightarrow$ $\underline{\underline{V = 3.23\,V}}$ 5

(c) Input current $I_{B1} = \frac{5 - 1.4}{100k} = 36\,\mu A$

If both transistors active then $I = [\beta + (1+\beta)/\beta]\, I_{B1} = 367\,\text{mA}$

But this would imply $V_{C1} = V_{C2} = 10 - 47 \times 0.367 = -7.26\,V$

$\Rightarrow$ $\underline{\underline{\text{LH transistor SATURATED}}}$, $\underline{\underline{\text{RH transistor ACTIVE}}}$ 5

In this case $V_{C1} = V_{C2} = V_{BE2} + V_{CESAT1} \simeq 0.9\,V$

and $\underline{\underline{I = (10 - 0.9)/47 = 194\,\text{mA}}}$

(d) Assuming FET is active, we have

$$I_D = K(-V_S - V_t)^2 = V_S/R \quad \text{or} \quad (2 - V_S)^2 = V_S \quad (KR = 1\,V^{-1})$$

$$\Rightarrow V_S^2 - 5V_S + 4 = 0$$

$$(V_S - 4)(V_S - 1) = 0 \quad \Rightarrow V_S = 4 \text{ or } V_S = 1$$

First solution puts FET below threshold $\Rightarrow V_S = 1$

and $\underline{\underline{I = K(-1 - V_t)^2 = 0.1\,\text{mA}}}$

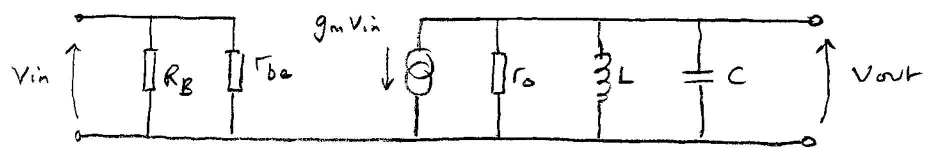
Check mode: $V_{DS} = 3$; $V_{GS} - V_t = 1$ $\Rightarrow$ $\underline{\underline{\text{ACTIVE}}}$ 4

2. (a) $I_C = 1\,mA$, $\beta = 100$ $\Rightarrow$ require $I_B = 10\,\mu A$

$I_B = \dfrac{V_{CC} - V_{BE}}{R_B}$ $\Rightarrow$ $\underline{\underline{R_B = 830\,k\Omega}}$ assuming $V_{BE} \sim 0.7V$

Inductor is short-circuit at DC $\Rightarrow$ $\underline{\underline{V_{OUT} = +9V}}$ 4

(b) SSEC :



KCL @ o/p : $g_m V_{in} + \dfrac{V_{out}}{r_o} + \dfrac{V_{out}}{Z_L} + \dfrac{V_{out}}{Z_C} = 0$

$Z_L = j\omega L$, $Z_C = 1/j\omega C$

$$A_V = \frac{V_{out}}{V_{in}} = -g_m\left(r_o // Z_L // Z_C\right) = -g_m\left(r_o // Z_{LC}\right)$$

At resonance $|Z_{LC}| \to \infty$ and $A_V \to -g_m r_o = -\dfrac{I_C}{V_T} \cdot \dfrac{V_A}{I_C}$

Putting $V_A = 120\,V$, $V_T = 25\,mV$ $\underline{\underline{A_V = -4800}}$ 8

(c) Centre frequency is $f_0 = \dfrac{1}{2\pi\sqrt{LC}}$, and $Q = 2\pi f_0 RC = \dfrac{R}{2\pi f_0 L}$

Require $Q = 100$, $f_0 = 1\,MHz$ with $R = r_o = 120\,k\Omega$ $\Rightarrow$ $\underline{\underline{C = 133\,pF}}$

$\underline{\underline{L = 191\,\mu H}}$ 4

(d) Actual Q is 60 $\Rightarrow$ $R = \dfrac{60}{100} \times 120\,k = 72\,k\Omega$

So equivalent <u>parallel</u> resistance of inductor R_L is such that $R_L // 120\,k = 72\,k\Omega$ $\Rightarrow$ $R_L = 180\,k\Omega$

To transform R_L to series resistance r_L use

$r_L = \dfrac{R_L}{Q_L^2} = \dfrac{(2\pi f_0 L)^2}{R_L}$ $\Rightarrow$ $\underline{\underline{r_L = 8.0\,\Omega}}$ 4

3 (a) R_G sets operating point by imposing the condition $V_{GD} = 0$ on both FETs.

Both FETs active, and $I_{D1} = I_{D2} = I_D$ (since $I_G = 0$)

$$\Rightarrow \quad I_D = K_1 (V_{OUT} - V_{t1})^2 = K_2 (V_{OUT} - V_{DD} - V_{t2})^2$$

$$\sqrt{\ } \rightarrow \quad \sqrt{K_1/K_2}\,(V_{OUT} - V_{t1}) = \pm (V_{OUT} - V_{DD} - V_{t2})$$

Both FETs above threshold $\Rightarrow$ take $-$ve sign

$$\Rightarrow \quad V_{OUT}\left[1 + \sqrt{K_1/K_2}\right] = V_{DD} + V_{t2} + \sqrt{k_1/k_2}\,V_{t1}$$

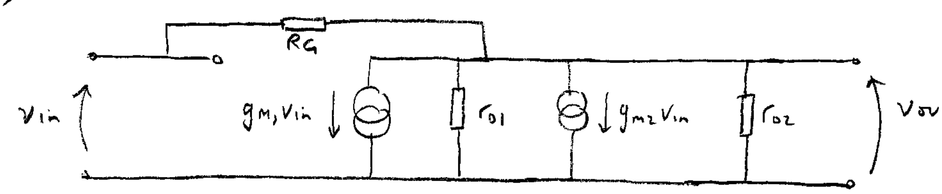
$\Rightarrow$ given result

Putting $V_{DD} = 5$, $V_{t1} = 1$, $V_{t2} = -1$, $\sqrt{K_1/k_2} = 0.5$

$$\Rightarrow \quad V_{OUT} = (5 - 1 + 0.5)/(1 + 0.5) \qquad \underline{\underline{V_{OUT} = 3V}}$$

$$I_D = K_1 (V_{OUT} - V_{t1})^2 \quad \Rightarrow \quad \underline{\underline{I_D = 0.4\ mA}}$$ 8

(b) Q1, Q2 in parallel in SSEC:



KCL @ o/p:

$$g_{m1}v_{in} + g_{m2}v_{in} + \frac{v_{out}}{r_{01}} + \frac{v_{out}}{r_{02}} + \frac{v_{out} - v_{in}}{R_G} = 0$$

$$\Rightarrow \quad A_v = \frac{v_{out}}{v_{in}} = -\left(g_{m1} + g_{m2} - \frac{1}{R_G}\right)\cdot\left(r_{01} /\!/ r_{02} /\!/ R_G\right)$$

$g_{m1} = 2\sqrt{k_1 I_D} = 0.4\ mS$, $g_{m2} = 0.8\ mS$, $r_{01} = r_{02} = \dfrac{V_A}{I_D} = 250\ k\Omega$

$$\Rightarrow \quad \underline{\underline{A_v = -148}}$$

$$i_{in} = \frac{v_{in} - v_{out}}{R_G} = \frac{v_{in}[1 - A_v]}{R_G} \qquad R_{in} = \frac{v_{in}}{i_{in}} = \frac{R_G}{[1 - A_v]} \Rightarrow \underline{\underline{R_{in} = 67\ k\Omega}}$$ 8

(c) Gain is large, so can ignore deviations in V_{GS} when determining output voltage swing.

$V_{GS1} = 3V \quad \Rightarrow$ Q1 active provided $V_{OUT} > 3 - 1 = 2V$

$V_{GS2} = -2V \quad \Rightarrow$ Q2 active provided $V_{OUT} - 5 < -2 + 1$ or $V_{OUT} < 4V$

$\Rightarrow$ V_{OUT} range is $2 < V_{OUT} < 4$

ie. max o/p amplitude $= 2V$ pk-pk

and corresponding max i/p amplitude $= \dfrac{2}{148} = \underline{\underline{13.5\ mV\ pk\text{-}pk}}$ 4

4 (a) Class A : No cross-over distortion, but high power dissipation

Class B : Low power, but with severe distortion at cross-over

Class AB : good compromise ; slightly higher power than Class AB, but with much lower distortion 4

(b) If base current are neglected, $I_N - I_P = I_L$ follows trivially from KCL at output. Also we have ;

$$I_N = I_S \exp\left(\frac{V_{in} + V_B - V_{out}}{V_T}\right), \quad I_P = I_S \exp\left(\frac{V_{out} - V_{in} + V_B}{V_T}\right)$$

Taking product of these equations gives $I_N I_P = I_S^2 \exp\left(\frac{2V_B}{V_T}\right) = I_Q^2$

I_Q is the quiescent current in each output transistor when $I_L = 0$ 6

(c) Eliminating I_P from the given equations gives :

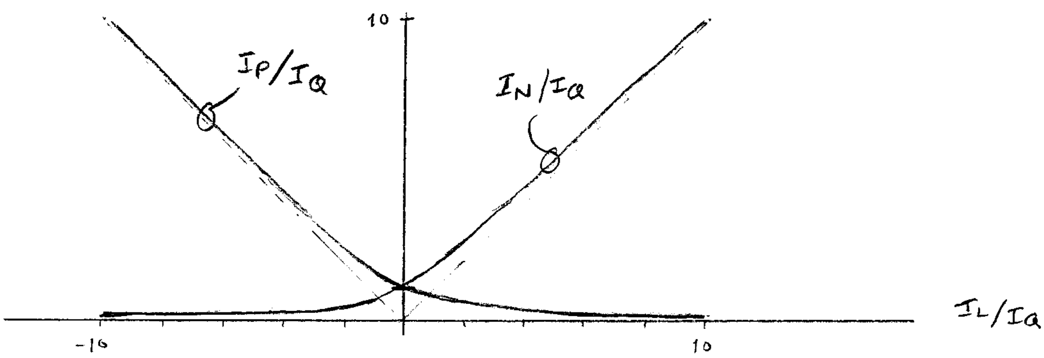
$$I_N - \frac{I_Q^2}{I_N} = I_L \quad \text{or} \quad I_N^2 - I_L I_N - I_Q^2 = 0$$

$$\Rightarrow \quad I_N = \frac{I_L \pm \sqrt{I_L^2 + 4I_Q^2}}{2}$$

$I_N > 0 \Rightarrow$ take +ve sign

For $I_L = I_Q$: $I_N = \left(\frac{1+\sqrt{5}}{2}\right) I_Q = 1.62\, I_Q \Rightarrow I_P = 0.62\, I_Q$

For $I_L = 10\, I_Q$: $I_N = \left(\frac{10 + \sqrt{104}}{2}\right) I_Q = 10.1\, I_Q \Rightarrow I_P = 0.099\, I_Q$



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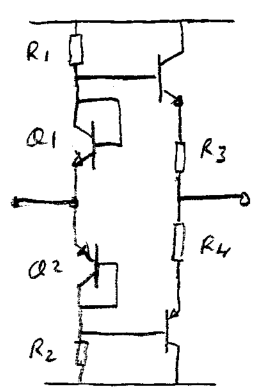
(d) Bias source provides V_{BE} corresponding to desired bias current, and needs to track thermal variations in o/p transistors to avoid thermal instability. Diode or diode-connected transistor is obvious candidate. R_1, R_2 provide biasing for Q1, Q2. R_3, R_4 included for improved stability.



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5 (a) In steady state, $I_{CAP} = 0 \Rightarrow I_{B2} = \frac{5-0.7}{100k} = 43\mu A$, $\underline{\underline{V_{B2} = 0.7V}}$

also $\beta I_{B2} = 8.6\ mA > \frac{5V}{1k} \Rightarrow$ Q2 saturated with $\underline{\underline{V_{C2} = 0.2V}}$

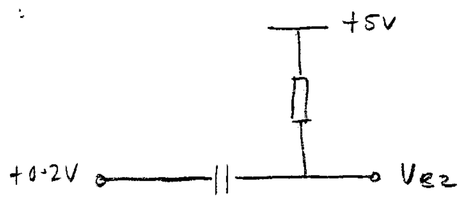
Since $V_{C2} << 0.5V$, and S1 open, $I_{B1} \sim 0 \Rightarrow$ $\underline{\underline{V_{B1} = 0.2V}}$

$\underline{\underline{V_{C1} = 5V}}$ 6

(b) When S1 is closed $(t=0)$, Q1 turns ON (saturated), and V_{C1} drops to $\sim 0.2V$. V_{CAP} cannot change instantaneously, so V_{B2} at $t = 0^+$ is

$$V_{B2}\Big|_{t=0^+} = V_{C1} - V_{CAP} = 0.2 - (5 - 0.7)$$
$$= -4.1\ V$$

While Q2 remains OFF, V_{B2} varies as for following configuration:



Steady state for this config is $V_{B2}\Big|_{t\to\infty} = +5V$

$\Rightarrow$ Quoting standard result:

$$V_{B2} = 5 + (-4.1 - 5)e^{-t/\tau} \quad \text{while Q2 is OFF}$$

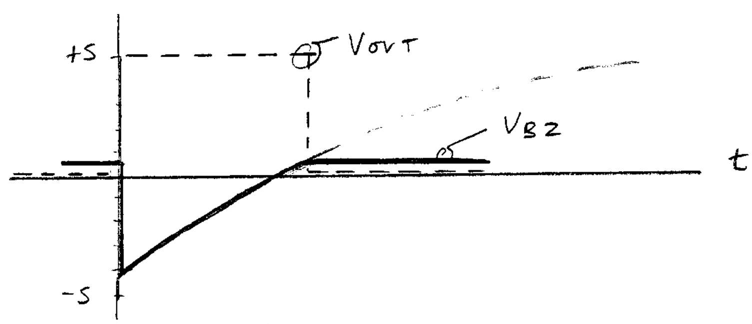
where $\tau = RC = 6.2\mu F \times 100k\Omega = 620$ msec

When V_{B2} reaches ~ 0.7, Q2 turns ON again and clamps V_{B2} at this level.

$\Rightarrow$ overall time variation is

$$V_{B2} = \begin{cases} 5 - 9.1\,e^{-t/\tau} & t \le T \\ 0.7 & t \ge T \end{cases}$$

where T is given by $0.7 = 5 - 9.1\,e^{-T/\tau}$ or $T = \tau \ln(9.1/4.3)$
$= \underline{\underline{465\ msec}}$



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(c) R_F provides +ve feedback, holding Q1 ON until $t = T$, even if S1 is released early. Without R_F, releasing S1 early would terminate pulse. 4