IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2016

EEE PART II: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 2

Corrected copy

Thursday, 26 May 2:00 pm

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 carry equal marks (30% each).

Basic expressions for voltage gain, input and output resistance for single stage amplifiers are given on the last page.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : T. Constandinou
Second Marker(s) : C. Toumazou

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1. This question consists of 6 sub-questions. Each item can be answered in a few words or a short paragraph with use of a diagram and/or expression where helpful. Please answer all sub-questions and simplify expressions where possible stating any assumptions made.

a) Derive expressions (by inspection) for the *voltage gain* of the amplifier circuits shown below in Fig. 1.1 (include r_O). [10]

(i)

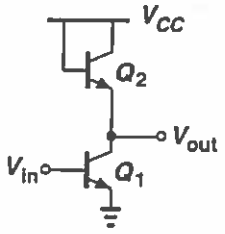

Fig. 1.1(a)

(ii)

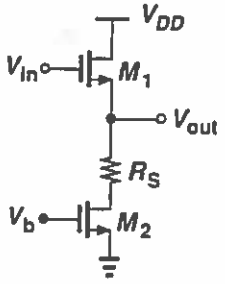

Fig. 1.1(b)

b) Derive expressions (by inspection) for the *output resistance* of the amplifier circuits shown below in Fig. 1.2 (include r_O). [10]

(i)

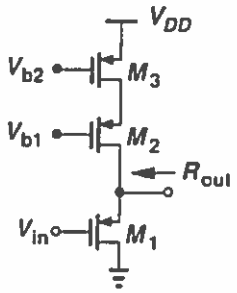

Fig. 1.2(a)

(ii)

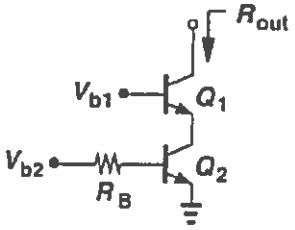

Fig. 1.2(b)

c) Compare the key features (and limitations) between an *integrated circuit* and *printed circuit board* based analogue circuit implementation. [5]

d) Explain how the circuit implementation of an operational amplifier (op-amp) can affect its *bandwidth (-3dB)*. [5]

e) Determine expressions for the *open loop gain*, *feedback factor*, and *closed loop output impedance* for the circuit shown in Fig 1.3 (excluding r_0). [5]

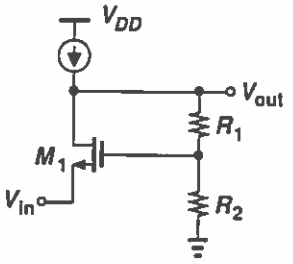

Fig 1.3.

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f) Calculate the transfer function of the circuit shown below in Fig. 1.4 if $A_0=\infty$. What choice of finite component values reduces $|V_{out}/V_{in}|$ to unity at all frequencies? [5]

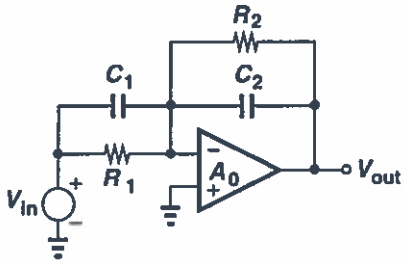

Fig 1.4.

2. The circuit below shows the transistor-level implementation of a two stage operational amplifier (Fig 2.1(a)), and this configured as a non-inverting amplifier (Fig. 2.1(b)).

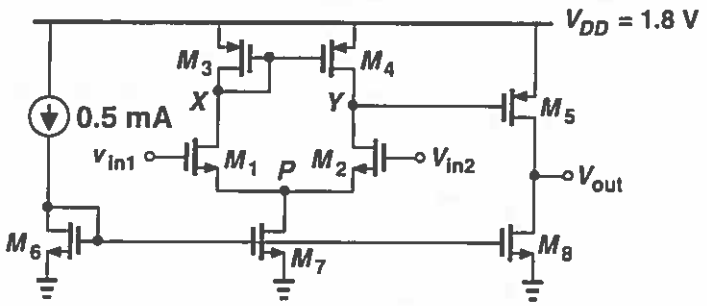

Fig. 2.1(a)

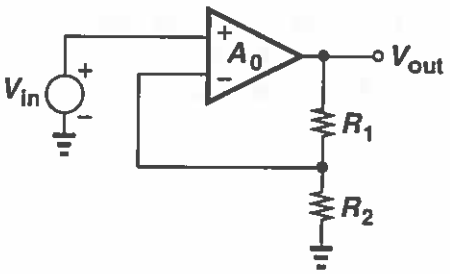

Fig. 2.1(b)

a) Derive an expression for the open loop gain (A_0) giving the polarities of V_{in1} and V_{in2} (i.e. which is V_+ and which V_-). [6]

b) Given the following parameters calculate the open loop gain. [6]

$\mu_n C_{ox} = 200\mu A/V^2$, $V_{THN} = 0.4V$, $\lambda_N = 0.1V^{-1}$, $\mu_p C_{ox} = 100\mu A/V^2$, $V_{THP} = -0.5V$, $\lambda_P = 0.2V^{-1}$

Device	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8
W/L	200/0.5	200/0.5	2/2	2/2	100/2	4/4	8/4	40/4

c) Derive an expression for the gain error (for a finite open loop gain, but assuming an ideal output resistance) for the non-inverting configuration shown and evaluate for R_1=9KΩ and R_2=1KΩ. [8]

d) Derive an expression for the closed loop gain considering the op-amps finite output impedance (Rout) and calculate the closed loop gain. [8]

e) Give 2 improvements to the op-amp circuit (shown in Fig. 2.1(a)) if it is to be used in the non-inverting configuration (shown in Fig. 2.1(b)). [2]

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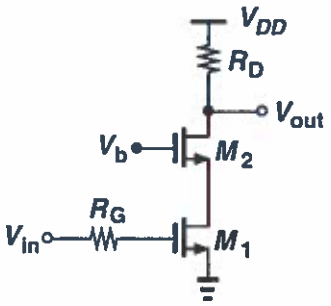
3. The circuit shown below is a two-stage amplifier consisting of a common source amplifier (M_1) followed by a common gate (M_2) stage (often referred to as a cascode).

Use the following parameters: V_{DD}=1.8V, $(W/L)_1=(W/L)_2$=50μm/0.18μm, $I_{D1}=I_{D2}$=2mA, C_{GS}=(2/3)(WL)C_{ox}, C_{ox}=15fF/μm^2, $\mu_n C_{ox}$=200μA/V^2, λ=0, $C_{SB}=C_{DB}$=0 and $C_{GD}=C_0W$, where C_0=0.2fF/μm denotes the gate-drain capacitance per unit width.



a) Compare the frequency responses of a common source and common gate amplifier. [5]

b) Redraw the circuit above to: (i) identify any nodes that are associated with poles and (ii) include all the parasitic device capacitances (within M1-2). [6]

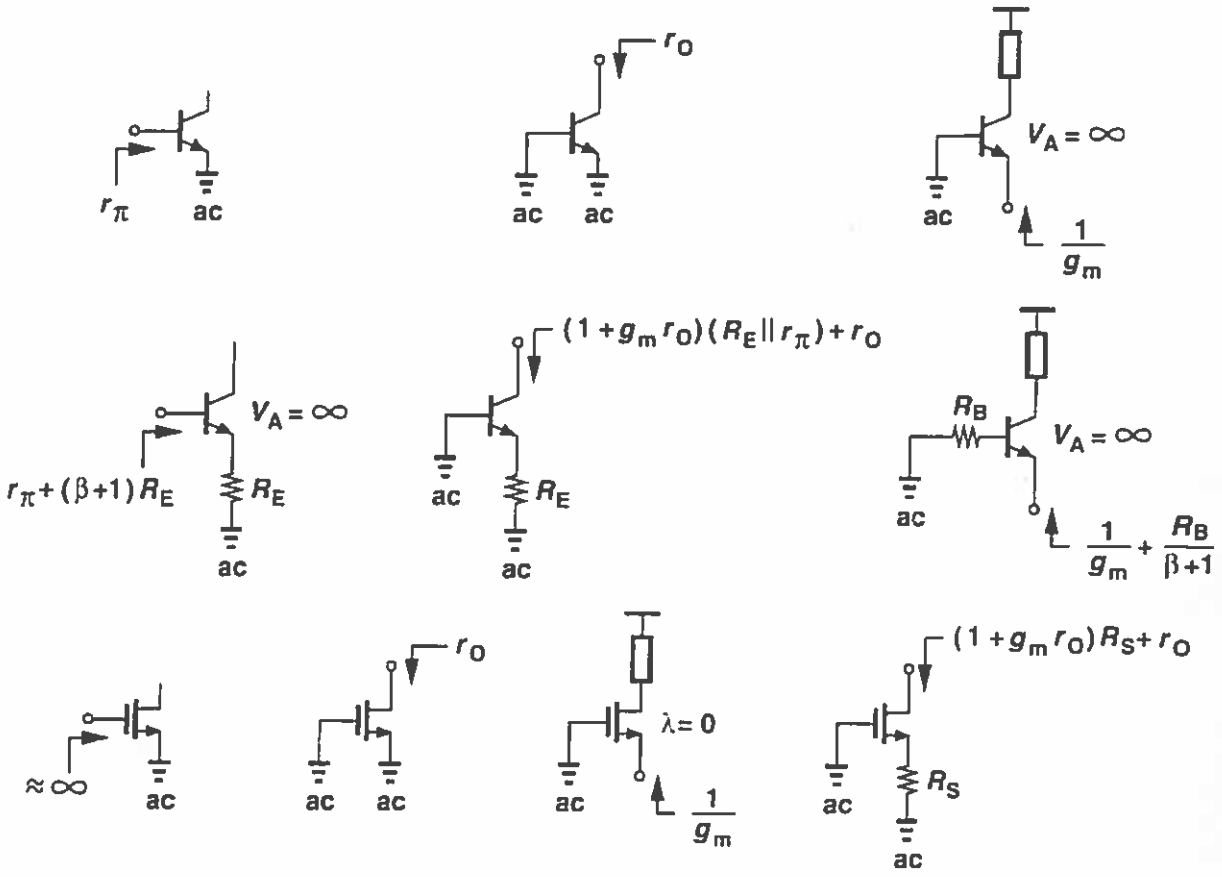
c) Redraw the circuit drawn in your answer to (b) to remove any redundant capacitances and lump together any parallel capacitances. Determine expressions for the different pole frequencies using Miller's theorem where appropriate. [6]

d) Determine an expression for the DC (low frequency) gain of the amplifier. [3]

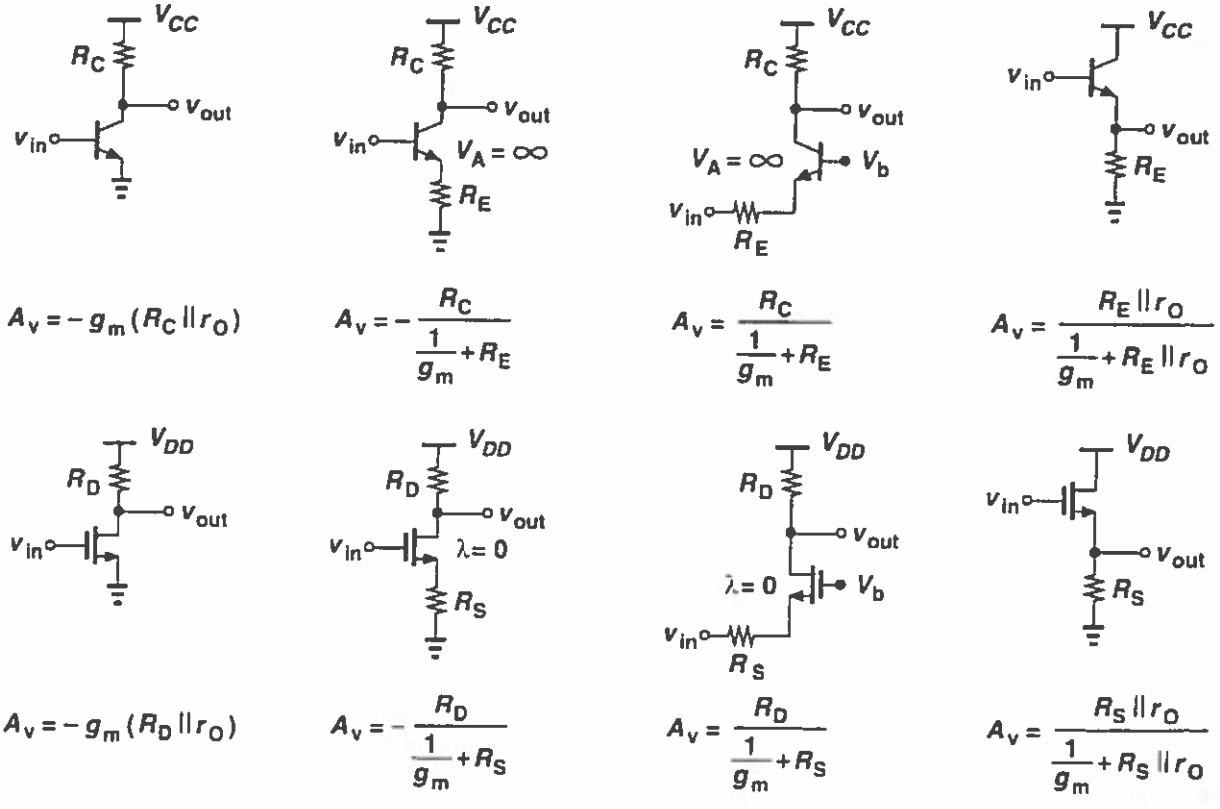
e) Evaluate the DC gain and pole frequencies, for RD=RG=600Ω. [6]

f) Describe how the DC gain can be increased. What is the limit? [4]

Input and Output Impedances



Voltage Gain Equations



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