UNIVERSITY OF LONDON

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 1999

BEng Honours Degree in Computing Part III
BEng Honours Degree in Information Systems Engineering Part III
MEng Honours Degree in Information Systems Engineering Part III
BSc Honours Degree in Mathematics and Computer Science Part III
MSci Honours Degree in Mathematics and Computer Science Part III
MEng Honours Degree in Information Systems Engineering Part IV
MSc Degree in Advanced Computing
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the
Diploma of Membership of Imperial College
Associateship of the City and Guilds of London Institute
Associateship of the Royal College of Science

PAPER 3.18 / I 4.18

CUSTOM COMPUTING

Thursday, May 6th 1999, 10.00 – 12.00

Answer THREE questions

For admin. only:
paper contains 4 questions

1 The core of a pipelined incrementer consists of m pipeline stages, each containing k halfadders and a latch.

a The core part of the pipelined incrementer can be described in the Pebble language as two nested FOR-loops:

```
c(0) <- Cin;
GENERATE FOR i = 0 ..(m-1)
BEGIN
        GENERATE FOR j = 0 .. (k-1)
        BEGIN
            hadd [C(...),in(...)] [C(...),out(...)]
        END;
        D [C(...)] [C(...)]
END;
cout <- C(...)
```

Provide appropriate input and output expressions indicated by "..." for the components `hadd`, `D` and `cout`.

b Provide a circuit diagram of the pipelined incrementer when m=3 and k=2. The diagram should include appropriate arrays of latches at the inputs and outputs of the core for data alignment.

How many latches are there in a design description with any given m and k, including both core and data alignment latches?

c Describe the core and the data alignment circuits for the pipelined incrementer in the Ruby language. Provide a Ruby transformation (no proof is required) for deriving the pipelined incrementer from the corresponding unpipelined version.

The three parts carry, respectively, 30%, 30% and 40% of the marks.

2a Given that $[P, Q]\ ;\ R = R\ ;\ Q$, show by induction that $[P, Q]^n\ ;\ R = R\ ;\ Q^n$.

b Provide inductive definitions for $\mathsf{rdr}_n\, R$ and $\triangle_n\, R$.

c Horner's Rule is given by:
if $[P, Q]\ ;\ R = R\ ;\ Q$ then $[\triangle_n\, P, Q^n]\ ;\ \mathsf{rdr}_n\, R = \mathsf{rdr}_n\, (\mathsf{snd}\ Q\ ;\ R)$.
Provide a diagram for the circuits described above when n=3.

d Prove Horner's Rule by induction.

e What are P, Q and R when Horner's Rule is applied to optimise polynomial evaluation?

The five parts carry, respectively, 20%, 20%, 20%, 25% and 15% of the marks.

3a Provide a diagram of $Q|R : [U, V] \sim [X, Y]$, given that $Q : U \sim [Z, Y]$ and $R : [Z, V] \sim X$, and that $Q|R = \mathsf{fst}\, Q\ ;\ (\mathsf{snd}\ swap)\backslash rsh\ ;\ \mathsf{fst}\, R$.

b Prove that $(Q \mid R)^{-1} = (R^{-1})|(Q^{-1})$.

c Draw diagrams for the two sides of the following equation when n=3:

$$(\mathsf{rdr}_n\, Q)^{-1} \mid (zip_n\ ;\ \mathsf{map}_n\, R) \quad = \quad \mathsf{row}_n(Q^{-1}|R)$$

d Use the results from part b and part c to prove that:

i) $\mathsf{col}_n\, (Q^{-1}|R) = (\mathsf{map}_n\, Q^{-1}\ ;\ zip_n^{-1})|(\mathsf{rdr}_n\, R)$,

ii) $(\mathsf{rdr}_m\, (zip_n\ ;\ \mathsf{map}_n\, Q))^{-1}|(zip_m\ ;\ \mathsf{map}_m\, (\mathsf{rdr}_n\, R)) = \mathsf{grid}_{m,n}\, (Q^{-1}|R)$.

e An N-tap FIR filter with input x and coefficients $w_0, \ldots, w_{N-1}$ is required to produce output y such that:

$$y_t \quad = \quad \sum_{0 \le i < N} w_i \times x_{t-i}$$

Use a diagram to illustrate how a 2 by 3 heterogeneous grid of $(Q|R_i)$, with appropriate additional circuitry, can be used to implement a 6-tap FIR filter.
(Hint: let $Q = fork\ ;\ \mathsf{snd}\ D$ and let each R_i contain a multiply-adder.)

The five parts carry, respectively, 15%, 15%, 20%, 30% and 20% of the marks.

[Turn over...

4a What is the purpose of pipeline morphing?

Provide diagrams to show how pipeline morphing can be applied to:

i) a 3-stage linear array,

ii) a 2 by 2 square mesh.

b Explain how pipeline morphing can be used to map a large virtual pipeline into a smaller physical pipeline.

Provide diagrams to illustrate the following mapping:

i) a 6-stage virtual linear array into a 3-stage physical linear array.

ii) a 4 by 4 virtual square mesh into a 2 by 2 physical square mesh.

The two parts carry, respectively, 45% and 55% of the marks.

[End of paper