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IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2003

MSc and EEE PART IV: M.Eng. and ACGI

HIGH PERFORMANCE ANALOGUE ELECTRONICS

Friday, 2 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

Corrected Copy

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : J.A. Georgiou
Second Marker(s) : E Rodriguez-Villegas

Special Information for Invigilators:

A Smith chart should be provided on each desk.

Information for candidates:

- *A Smith chart is provided.*
- *Boltzmann constant* $k=1.38\times10^{-23}$ *J/K*
- *Electron charge* $e=1.6\times10^{-19}$ *C*
- *For all relevant calculations assume room temperature i.e. 300 K*

1.(a) (i) What is meant by the term 'image signal' in a wireless communications receiver?

[3]

Explain how the problem of the image signal is overcome in the following receiver architecture:

(ii) Superheterodyne receiver

[4]

(iii) Image-reject receiver (Draw architecture for Image reject receiver)

[5]

(b) Figure 1.1 shows the front-end of a superheterodyne receiver. If the low noise amplifier (LNA) ***is omitted***, the sensitivity of the receiver is found to be –115 dBm, when the input is power-matched. Assuming the filters are noiseless with unity gain at the signal frequencies of interest, the equivalent noise bandwidth of the system is 25kHz and all the system noise can be attributed to the first mixer section,

(i) What is the noise figure of the system?

[5]

A power-matched LNA with a power gain of 18dB is re-connected in front of the first stage mixers,

(ii) Calculate the maximum noise figure of the LNA if the system is to achieve a sensitivity of –127 dBm

[3]

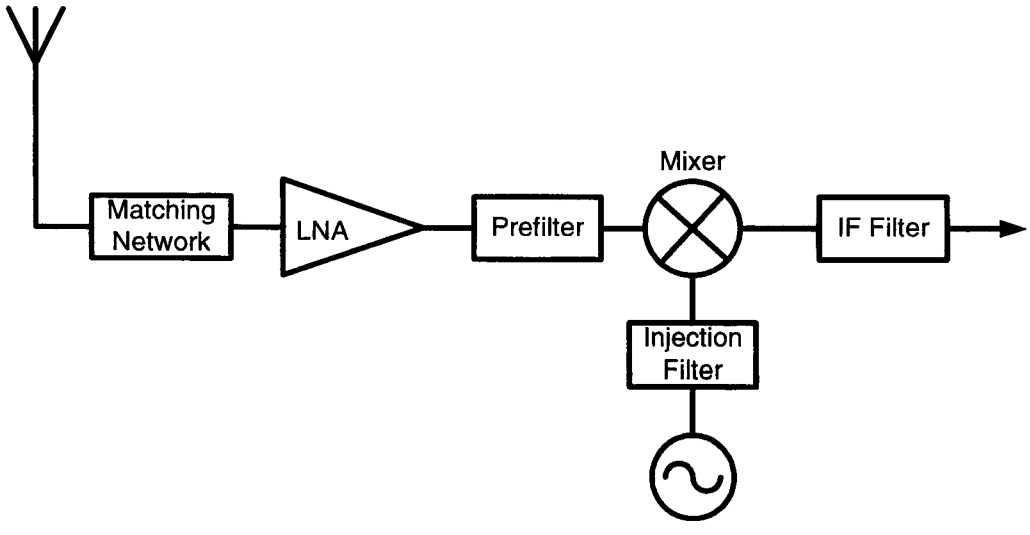


Figure 1.1

2.(a) List the three traditional parameter sets that are used to characterise a two-port network and describe their limitations with respect to S-parameters. How are S-parameters measured?

[7]

(b) An amplifier is driven by a source with reflection coefficient ρ_s and is driving a load with reflection coefficient ρ_l.

(i) Construct an S-parameter signal flow graph, assuming that the amplifier was accurately characterised to in terms of S-parameters

[2]

(ii) Simplify this graph to obtain an expression relating the power transfer between the source and the load.

[5]

(iii) Calculate the resulting power gain given that $\rho_s = 0.75 + j0.0$ and $\rho_l = 0.4 + j0.6$ and that the amplifier's S-parameters are:

$S11 = 0.2 + j0.51$ $\quad$ $S21 = 1.8 + j1.81$
$S12 = 0.3 + j1.0$ $\quad$ $S22 = 0.3 + j0.82$

(at operating frequency of 2.4 GHz and referenced to 50Ω)

[4]

(iv) Passive networks are now designed to match the source and the load to the amplifier so $\rho_s = \rho_l = 0$. What is the power gain under these matched conditions?

[2]

3.(a)

(i) Sketch and label the hybrid-π small-signal equivalent circuit of an n-channel MOS transistor operating in the strong inversion saturation region, including all major sources of noise within the device.

[3]

(ii) Briefly describe the origin of each noise source, and give expressions by which the mean square value of each of these noise sources can be calculated.

[3]

(b) Figure 3.1 shows an NMOS transistor connected in a common-source configuration, which is used to amplify a voltage signal (Vin) from a source (d.c. bias components are ignored).

(i) By referring all noise sources to the input, derive an expression for the total equivalent input mean square noise voltage (veq^2), and sketch the approximate frequency response, indicating the midband noise expression.

(You may assume that the d.c. gate leakage current $I_G = 0$)

[6]

(ii) From the midband expression calculate the noise factor given that:

Quiescent (d.c.) drain current I_D=1 mA
W/L=25μm/0.5μm
Transconductance parameter K=50 μA/V²
Source resistance R_S=150 Ω
Load resistance R_L=5 kΩ

[3]

(iii) Figure 3.2 shows the same transistor reconnected in a common gate configuration. Derive an approximate expression for the noise factor of this configuration at midband frequencies, and compare this value for the common source configuration.

[5]

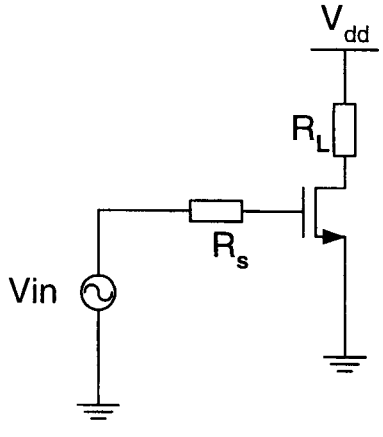


Figure 3.1

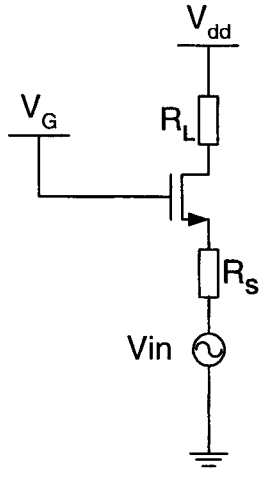


Figure 3.2

4.(a) Figure 4.1 shows the small signal hybrid π of a bipolar junction transistor (BJT).

(i) Describe the Miller Transformation applied to any admittance Y across the input and output of a voltage amplifer of gain G and show how its application to the small signal hybrid π can lead to a simplified model.

[5]

(ii) Explain qualitatively why the use of this approximation is inadequate at frequencies approaching the f_T of a device. Derive an alternative 'RF hybrid π' model that does not suffer these limitations

[5]

(b) Assume that by using the above techniques the bandwidth of an amplifier is optimised for use well beyond 3GHz operation. If the input can effectively be modelled by a resistance *R=200Ω* in parallel with a capacitor *C=1.5pF*, design a matching network using a Smith Chart, for a source resistance of 50Ω at 1.2 GHz.

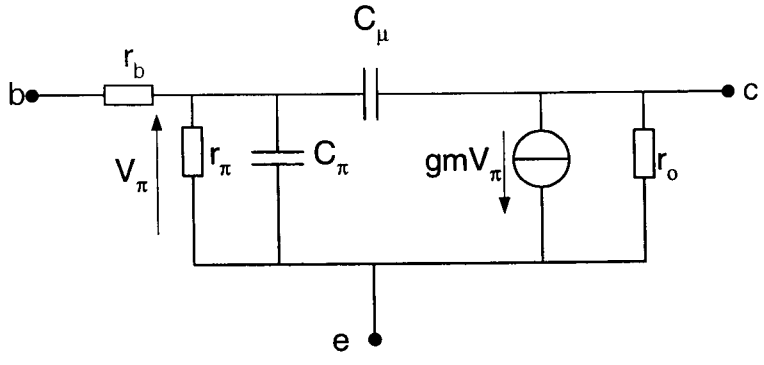


Figure 4.1

[10]

5.(a) Figure 5.1 shows the architecture of a bipolar double balanced mixer.

(i) Assuming that all transistors are in the active region of operation, and that the input signals V_A and V_B are small (less than 50mV), show that the differential output current I_1-I_2 is proportional to the product of the two input signals. Calculate the mixer conversion gain given that I_Q=1mA.

[7]

(ii) Explain why it is not a good idea to use emitter degeneration to increase the maximum linear input voltage range of V_A. Sketch a suitable predistortion circuit which may be used to increase the linear input voltage range of V_A.

[8]

(b) Figure 5.2 shows a circuit which may be used to replace transistors Q_5 , Q_6 and current source I_Q in Figure 5.1. The second input voltage signal V_B is now in the form of current I_B. Derive an expression for the mixer differential output current if this alternative circuitry is employed, and show that a high linear input signal range of I_B can be achieved.

[5]

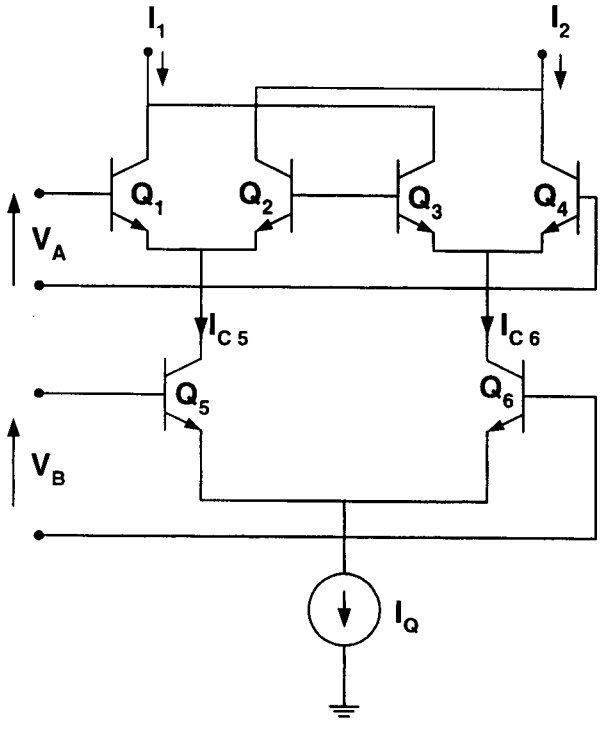


Figure 5.1

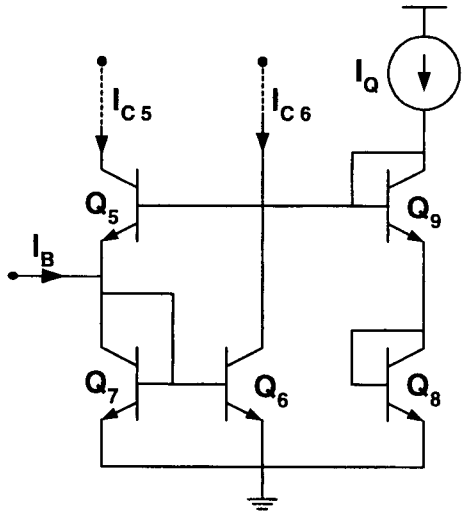


Figure 5.2

6.(a) Figure 6.1 shows a doubly-terminated passive LC-ladder lowpass filter.

(i) Give three advantages of the LC-ladder approach for implementing continuous time filters and state two reasons why passive LC ladders are unsuitable for implementing fully-integrated filters.

[5]

(ii) By constructing a signal flow graph of the ladder topology shown in Figure 6.1 , outline how this filter can be transformed into a topology suitable for integration, and sketch a block diagram of the resulting filter architecture.

[10]

(b) Figure 6.2 shows a differential input transconductor that can be used to make integrators for the above filter. Assuming that devices M1-M4 are saturated, whilst M5, M6 are in the linear region, derive an expression for the transconductance gain I_{out}/ V_{in}.

[5]

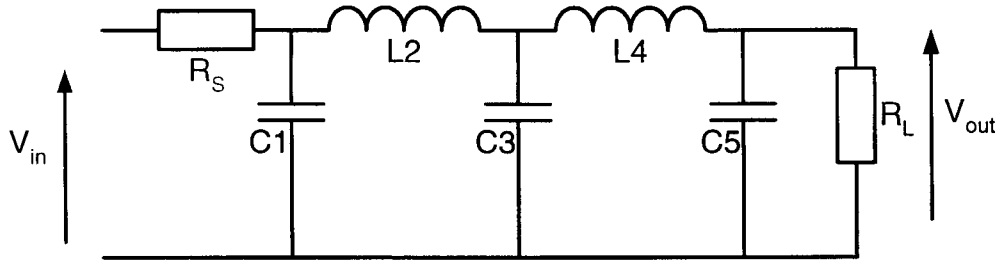


Figure 6.1

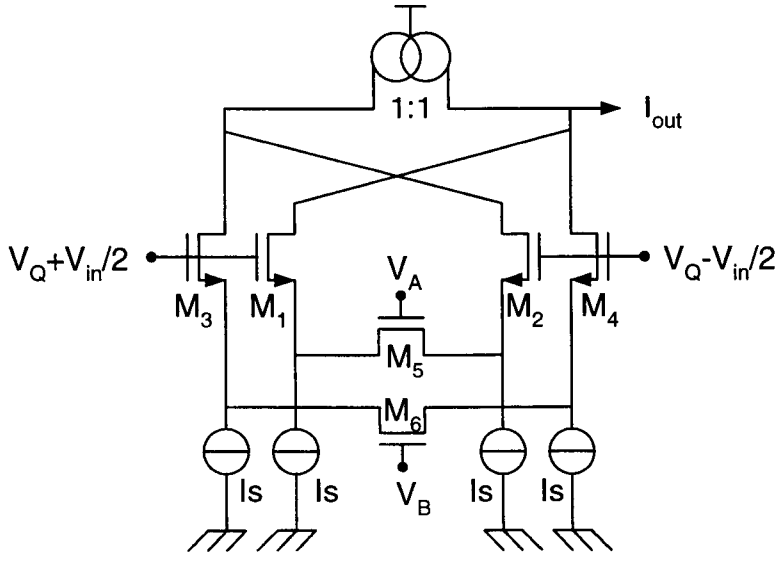
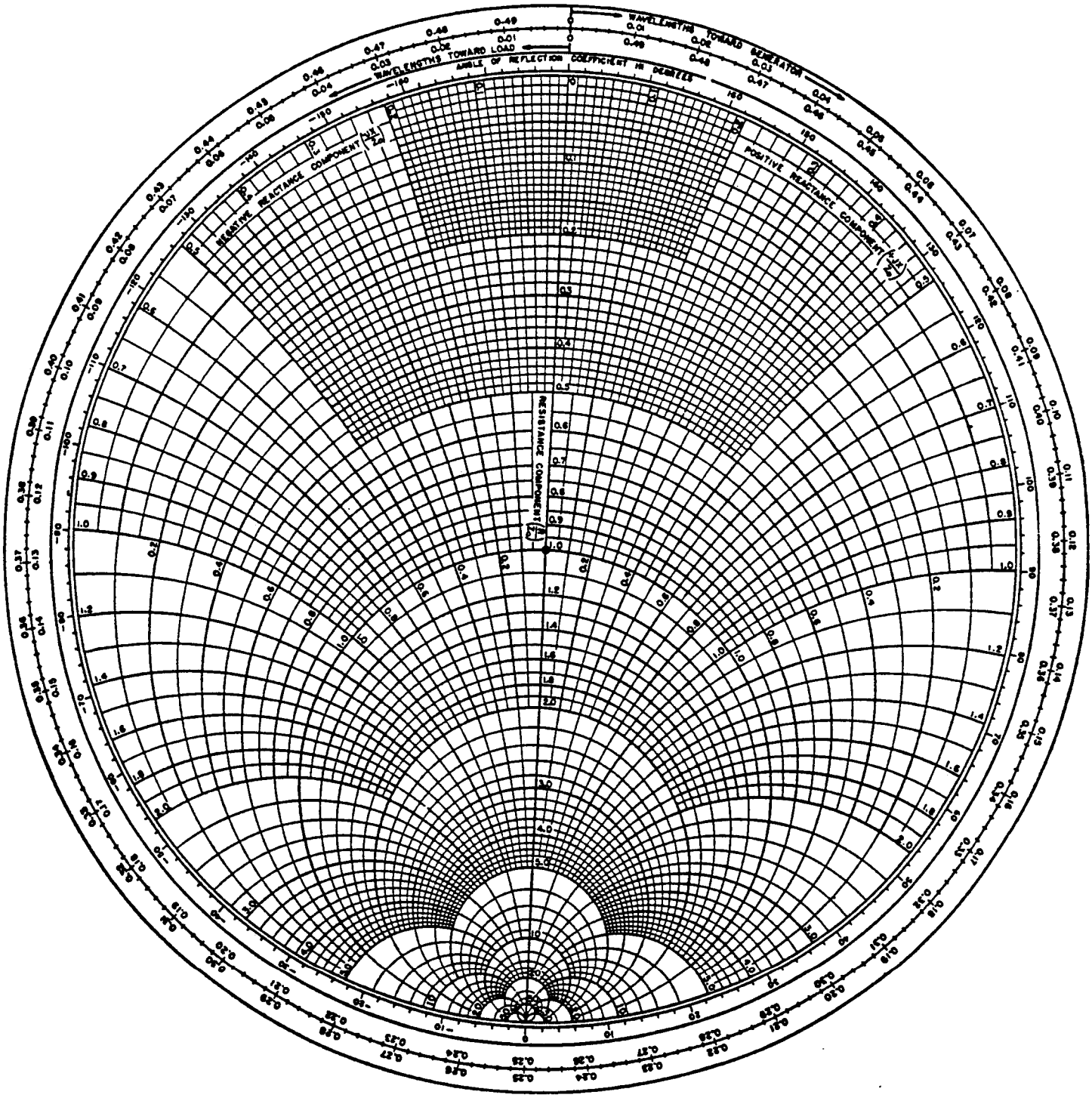


Figure 6.2


WAVELENGTHS TOWARD GENERATOR
WAVELENGTHS TOWARD LOAD
ANGLE OF REFLECTION COEFFICIENT IN DEGREES
NEGATIVE REACTANCE COMPONENT
POSITIVE REACTANCE COMPONENT
RESISTANCE COMPONENT