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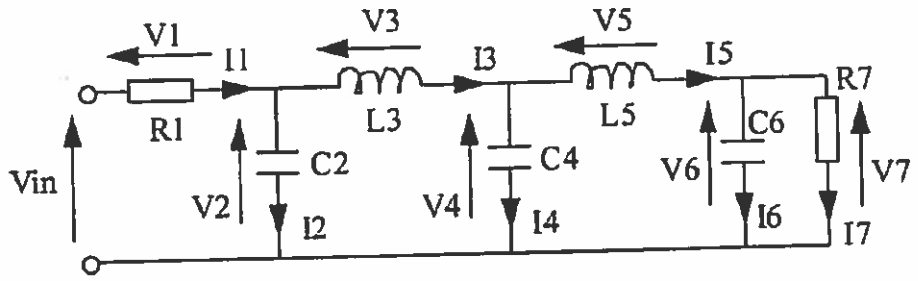
Model Answers and Mark Schemes	First Examiner:	A. Casson
Paper Code: E4.17	Second Examiner:	P. Georgiou

1.

(a)

(i) (Theory)



Ladder state equations:

$V1 = Vin - V2$
$I1 = V1/R1$

$I2 = I1 - I3$
$V2 = I2/sC2$

$V3 = V2 - V4$
$I3 = V3/sL3$

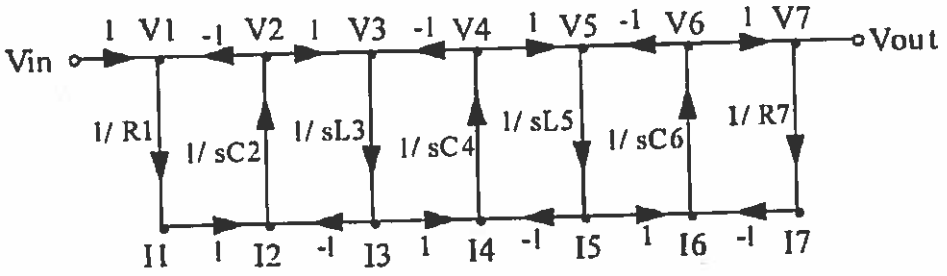
$I4 = I3 - I5$
$V4 = I4/sC4$

$V5 = V4 - V6$
$I5 = V5/sL5$

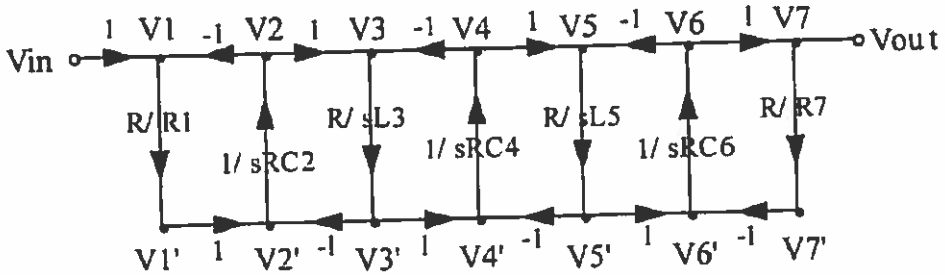
$I6 = I5 - I7$
$V6 = I6/sC6$

$V7 = V6$
$I7 = V7/R7$

Signal flow graph:



Scaled signal flow graph:



[4]

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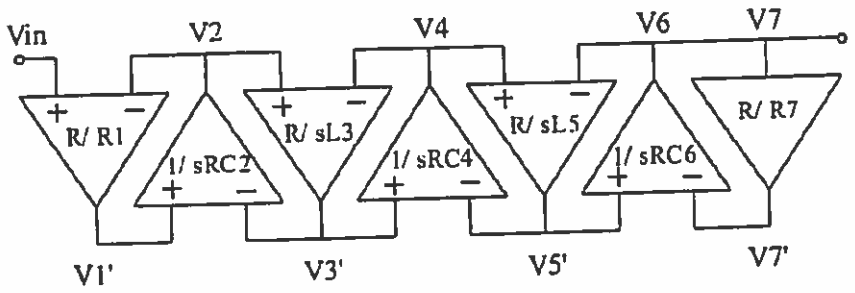
(ii) (Application of theory)

Vertical transitions become circuit blocks with two inputs and one output with the corresponding transfer function. The signs on the horizontal branches determine which input of the circuit block they connect to. The circuit voltages/states are illustrated below:



X/Y terms (the two on the ends) are amplifiers. X/sY terms (the middle five) are integrators.

[2]

(iii) (Theory)

Advantage: Parasitic insensitive: presence of virtual earth means back-plate parasitic can be between two ac grounds.

Disadvantage: Relatively low bandwidth due to the need for negative feedback.

[2]

(b)

(i) (New computed example)

For MOSFET in triode region: $I_d = GV_{ds} - \beta V_{ds}^2$ where $G = 2\beta(V_{gs} - V_{th})$.

Hence from current flow through FETs and capacitors:

$$I_{d1} = G1V1 - \beta V1^2 = -Vo1.sC$$

$$I_{d2} = G2V2 - \beta V2^2 = -Vo2.sC$$

Vout = Vo2 – Vo1: $Vout = \frac{1}{sC}[G1V1 - \beta V1^2 - G2V2 + \beta V2^2]$

If matched: G1 = G2 = G. If balanced: V2 = -V1.

Hence: $Vout = \frac{1}{sC}[GV1 - \beta V1^2 + GV1 + \beta V2^2]$ so $Vout = \frac{1}{sC}2GV1$.

$\omega u = \frac{2G}{C} = \frac{4\beta(Vc - V_{th})}{C}$.

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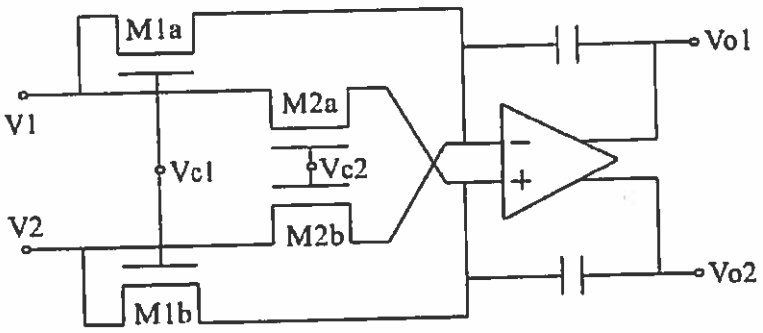
Substituting values gives Vc = 1.7 V.

[4]

(ii) (Theory)

Use cross-coupled MOS resistors:



$$Vo1 - Vo2 = \frac{1}{sC}\left(Id1a + Id2b - Id1b - Id2a \right)$$

$$= \frac{1}{sC}\left((G1 - G2)(V1 - V2) + (\beta 1 - \beta 2)\left(V2^2 - V1^2\right)\right)$$

Provided that devices are matched (equal β), then $Vout = \frac{(G1 - G2)}{sC}(V1 - V2)$

where $G1 - G2 = 2\beta(Vc1 - Vc2)$

[4]

(iii) (Application of theory)

The cross-coupled topology from (ii) is better as the unity gain frequency does not depend on the threshold voltage.

[1]

(iv) (New computed example)

For the circuit from Figure 1.3: The variation could be corrected by changing the control voltage (Vc) so that the difference (Vc – Vth) is unchanged even if Vth varies. To keep the same operating point in (i) we need (Vc – Vth) = 1V. Hence for Vc,max = 3V, Vth could be as large as 2 V, 1.3 V above nominal.

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For the circuit from (ii): the topology is already compensated for mismatch in the threshold voltages and so no adjustments are necessary. In principle any change in the threshold value is tolerable, as long as the FETs stay in the triode region.

[3]

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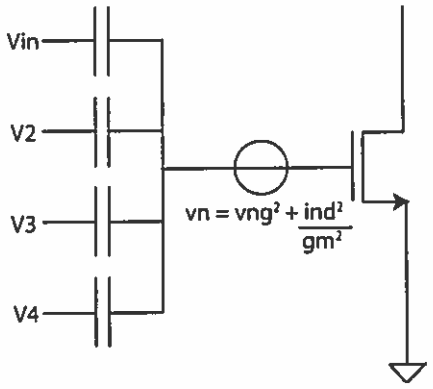
2.

(a)

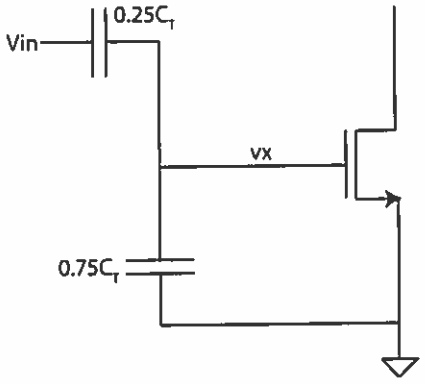
(i) (Application of theory)



[2]

(ii) (Application of theory)

If V2, V3, and V4 are constant they act as ac grounds for the noise analysis. The capacitor bank thus acts as a potential divider:



Hence by circuit analysis: $vx = \frac{0.25C_T}{0.25C_T + 0.75C_T}.Vin \rightarrow vx = 0.25Vin.$

To refer noise sources to input need to invert this, and square to deal with powers.

End result: $16(vng^2 + \frac{ind^2}{gm^2})$ V².

[5]

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(b) (Theory)

$$\text{Noise factor} = \frac{\text{Total equivalent input noise power}}{\text{Input noise power due to the source only}}$$

Noise figure is the noise factor expressed in dB.

[2]

(c)

(i) (Application of theory)

- Considering the first stage alone:

$$F1 = \frac{veq1^2}{vns^2}$$

Thus the equivalent input noise voltage $veq1^2 = F1 vns^2$
This equivalent input noise $veq1^2$ consists of the received (source) input noise, plus internal noise $vn1^2$ contributed by the first stage:

$$veq1^2 = vns^2 + vn1^2$$

$$vn1^2 = veq^2 - vns^2 = (F1-1)\, vns^2$$

- Considering the second stage alone, $vn2^2 = (F2-1)vns^2$

- Combining both stages, the total output noise:

$$vnt^2 = G1G2vns^2 + G1G2vn1^2 + G2vn2^2$$

$$= G1G2vns^2 + G1G2(F1-1)vns^2 + G2(F2-1)vns^2$$

$$= [G1G2F1 + (F2-1)G2]vns^2$$

- Noise factor of the cascaded pair,

$$F = \frac{vnt^2}{G1G2vns^2} = F1 + \frac{F2-1}{G1}$$

[3]

(ii) (New computed example)

Using given numbers: F = 2.02.

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We can define $SNR_{in} = \dfrac{\text{Received signal power}}{\text{Received noise power}} = \dfrac{vsig^2}{vns^2}$

Similarly $SNR_{out} = \dfrac{\text{Output signal power}}{\text{Output noise power}} = \dfrac{G\,vsig^2}{G\,veq^2} = \dfrac{vsig^2}{veq^2}$

Thus $\dfrac{SNR_{in}}{SNR_{out}} = \dfrac{veq^2}{vns^2} = F$

SNRin = F × SNRout.

SNRout = 50 dB = 100,000.

SNRin = 202,000 = 53.05 dB to 2 d.p..

[3]

(d) (New computed example)

By extension from part (c), for three stages:

$$F = F1 + \frac{F2-1}{G1} + \frac{F3-1}{G1G2}$$

Substituting numbers gives the noise factor as 6.1445. Hence the noise figure is 7.88 dB.

[5]

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3.

(a) (Theory)

The mixer is used for frequency conversion.

Selecting a particular frequency channel from the complete RF spectrum requires a narrowband bandpass filter. Making a high Q, tuneable, filter at RF frequencies is difficult. The mixer multiplies the RF input signal with a Local Oscillator (LO) such that the resulting output is at a lower Intermediate Frequency (IF). The design of the bandpass IF filter is eased since it doesn't have to be tunable, and the IF centre frequency is much lower than the input RF signal. The LO can be tuneable to select different channels.

[2]

(b) (New computed example)

All superhet receivers have the potential for responding to frequencies other than the desired channel. Most spurious responses originate in the mixer, especially from harmonic mixing of the RF and LO signals.

Here the LO is at 1000 MHz.

If this has a significant 2nd harmonic it will be at 2000 MHz. Input signals at 1900 MHz and 2100 MHz will mix with this to give frequencies at the sum and difference: 100 MHz, 3900 MHz, 4100 MHz.

The 100 MHz component will overlap with the wanted IF signal, causing interference.

[3]

(c) (Application of theory)

For BJT: $Ic = Ise^{\frac{Vbe}{Vt}}$. Let the emitter node voltage be Vx.
Thus $Ic1 = Is1e^{\frac{Va/2-Vx}{Vt}}$ and $Ic2 = Is2e^{\frac{-Va/2-Vx}{Vt}}$.

Assume the transistors are matched so $Is1 = Is2 = Is$.

Therefore $out = Ic1 - Ic2 = Is(e^{\frac{\frac{Va}{2}-Vx}{Vt}} - e^{\frac{\frac{-Va}{2}-Vx}{Vt}}) = Ise^{\frac{-Vx}{Vt}}(e^{\frac{\frac{Va}{2}}{Vt}} - e^{\frac{\frac{-Va}{2}}{Vt}})$.

For the constant current source: $q = Ic1 + Ic2 = Ise^{\frac{-Vx}{Vt}}(e^{\frac{\frac{Va}{2}}{Vt}} + e^{\frac{\frac{-Va}{2}}{Vt}})$.

Combining these: $\frac{Iout}{Iq} = \frac{e^{\frac{\frac{Va}{2}}{Vt}} - e^{\frac{\frac{-Va}{2}}{Vt}}}{e^{\frac{\frac{Va}{2}}{Vt}} + e^{\frac{\frac{-Va}{2}}{Vt}}}$. $Iout = Iq\tanh(\frac{Va}{2Vt})$.

Small angle approximation: $\tanh x \to x, x \to 0$.
Thus, if Va is small: $Iout = \frac{IqVa}{2Vt}$.

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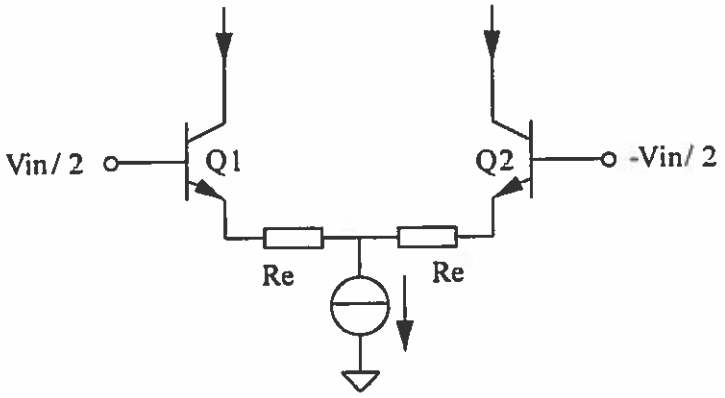
For this to be valid need: Va<<2Vt so Va << 52 mV, say |Va| < 5.2 mV. Reasonable similar values acceptable.

[6]

(d)

(i) (Application of theory and new computed example)

Emitter degeneration:



$$\begin{aligned} Vin &= Vbe1 + Re Ic1 - Vbe2 - Re Ic2 \\ &= Ic1(re1 + Re) - Ic2(re2 + Re) \end{aligned}$$

where the values of re1 and re2 depend on the instantaneous value of Vin. If Re >> re1, re2 then the non-linear variation of gm with Vin is swamped:

$$Vin = Ic1 Re - Ic2 Re = (Ic1 - Ic2)\, Re$$

if Iout = (Ic1 – Ic2); Iout/Vin = 1/Re

This can only be applied to the bottom differential pair, hence:

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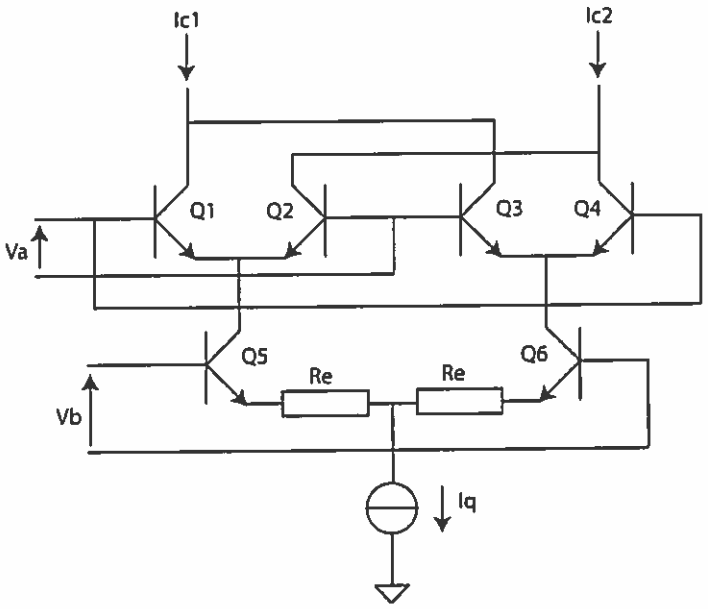


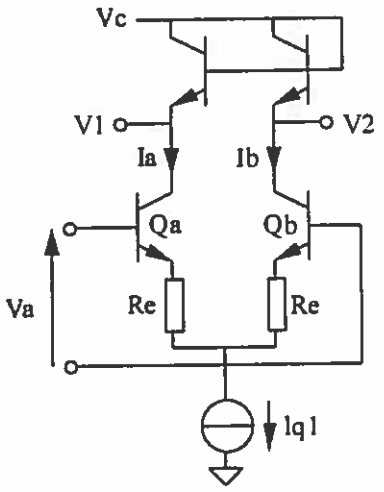
To work correctly need Re >> re → Re >> 1/gm = 1 kΩ. Hence values in excess of 10 kΩ.

[5]

(ii) (Application of theory)

Gilbert cell has a tanh(X) operation. Precede this by a $\tanh^{-1}(X)$ operation so that when cascaded the two non-linear operations cancel, leaving the wanted multiplication terms with no non-linear operation present.

A suitable circuit to implement this is:



[4]

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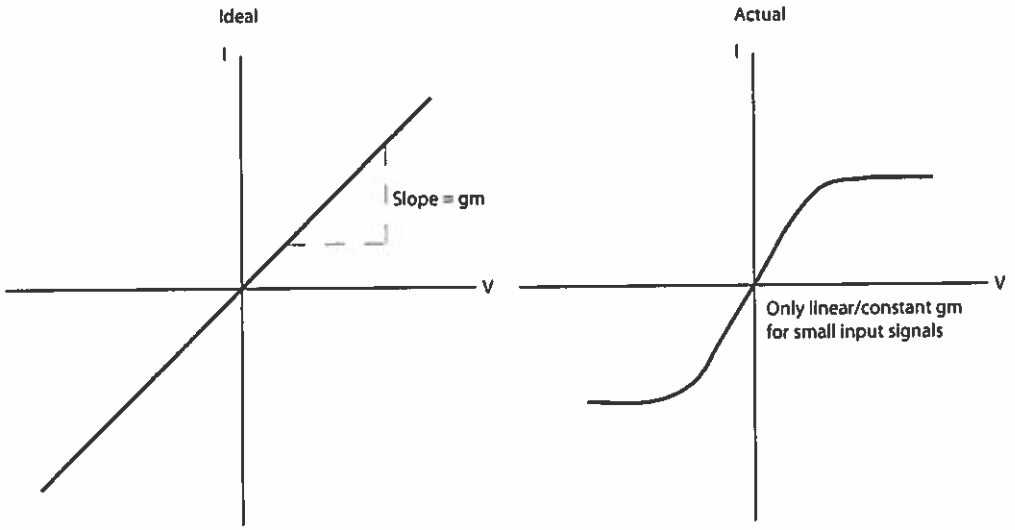
4.

(a) (Theory)



[2]

(b) (Application of theory)

For FET in saturation: $Id = \beta(Vgs - Vth)^2$ so $Vgs = \sqrt{\frac{Id}{\beta}} + Vth.$

If source voltage = Vx: $\frac{Vd}{2} - Vgs1 = Vx = -\frac{Vd}{2} - Vgs2$ so $Vd = Vgs1 - Vgs2.$

Combining these for matched transistors: $d = \frac{\sqrt{Id1} - \sqrt{Id2}}{\sqrt{\beta}}$

Know: $Is = Id1 + Id2.$

Solving for Id1: $\sqrt{\beta}Vd = \sqrt{Id1} - \sqrt{Is - Id1}$ so $\beta Vd^2 = Is - 2\sqrt{Id1}\sqrt{Is - Id1}$

So: $\sqrt{Id1Is - Id1^2} = \frac{Is}{2} - \frac{\beta Vd^2}{2}.$

Squaring and re-arranging: $0 = Id1^2 - IsId1 + \left(\frac{Is^2}{4} - \frac{\beta Vd^2 Is}{2} + \frac{\beta^2 Vd^4}{4}\right).$

This is a quadratic equation in Id1: $0 = aId1^2 + bId1 + c$ so solve using the quadratic formula.

Gives: $1 = \frac{Is}{2} \pm \frac{1}{2}\sqrt{2\beta Vd^2 Is - \beta^2 Vd^4}$.

To keep Id1 positive only the positive root is valid: $Id1 = \frac{Is}{2} + \frac{Is}{2}\sqrt{\frac{2\beta Vd^2}{Is} - \frac{\beta^2 Vd^4}{Is^2}}$

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Analogously solving for Id2: $Id2 = \frac{Is}{2} - \frac{Is}{2}\sqrt{\frac{2\beta Vd^2}{Is} - \frac{\beta^2 Vd^4}{Is^2}}$.

At the output know: $Iout = Id1 - Id2$

Thus: $Iout = Is\sqrt{\frac{2\beta Vd^2}{Is} - \frac{\beta^2 Vd^4}{Is^2}} = Vd\sqrt{2\beta Is - \beta^2 Vd^2}$.

[7]

(c) (Theory)

Let $Is = Idc + cVd^2$

$$Iout = Vd\ \sqrt{2\beta Idc + 2c\beta Vd^2 - \beta^2 Vd^2}$$

$$= Vd\ \sqrt{2\beta Idc + 2\beta Vd^2(c - \beta/2)}$$

If $c = \beta/2$, then $Iout = Vd\ \sqrt{2\beta Idc}$

Which is a linear function of the input voltage. The transconductance is given by the derivative:

$gm = \sqrt{2\beta Idc}$

[3]

(d) (Theory)

Sum output currents (instead of difference):

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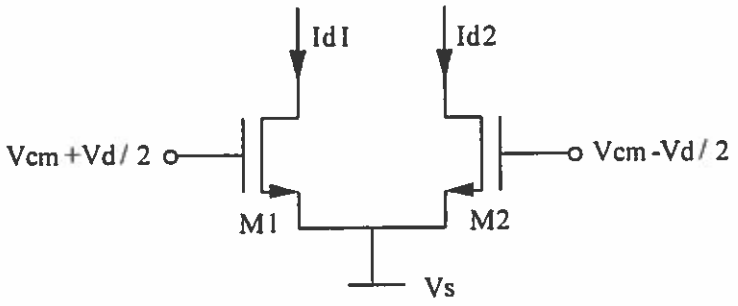

$Id1 = \beta(Vgs1-Vth)^2$

$= \beta(Vcm + Vd/2 - Vs - Vth)^2 = \beta(Vc - Vth + Vd/2)^2$

where $Vc = Vcm - Vs$

Similarly $Id2 = \beta(Vc - Vth - Vd/s)^2$

$Iout = Id1 + Id2 = \beta(2(Vc-Vth)^2+Vd^2/2) = Idc + cVd^2$

where $Idc = 2\beta(Vc - Vth)^2$ and $c = \beta/2$ as required

The sum of the drain currents is quadratically related to the differential input voltage provided that the common-mode input signal Vc remains constant.

[4]

(e)

(i) (New computed example)

$$SNR_{dB} = \frac{Power_{signal}}{Power_{noise}} = 10\log\left(\frac{(Vrms, signal)^2/R}{(Vrms, noise)^2/R}\right) = 20\log\left(\frac{Vrms, signal}{Vrms, noise}\right)$$

Signal is 100 mVpp so 35.36 mVrms. Using this in the equation above gives 36.36 µVrms.

[2]

(ii) (Application of theory)

FET flicker noise equation: $vng^2 = \frac{k\Delta f}{CoxWLf}V^2$.

Reduced by making transistors bigger, or providing more filtering so effective bandwidth is reduced. If possible can also operate circuit at a higher frequency where flicker noise is less significant due to the 1/f term. Any two or reasonable other answer.

[2]