1.

(a) (Application of Theory)

If the power gain is larger than one, the most important is the first block and the least important the last. This can be mathematically explained by the Noise Factor, which in a cascade of blocks is given by:

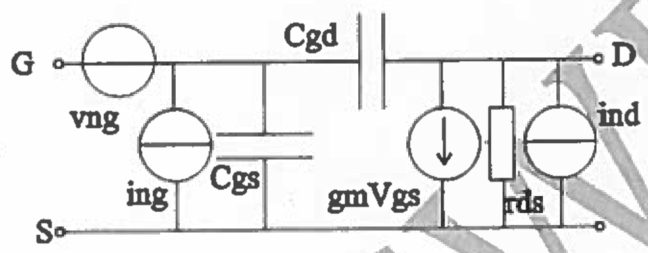
$$F = \frac{vnt^2}{G1G2G3G4vns^2} = F1 + (F2-1)/G1 + (F3-1)/G1G2 + (F4-1)/G1G2G3$$

Hence subsequent blocks have their noise contribution attenuated by the previous gains.

(b) (Application of Theory)

The second one. See mathematical explanation in (a).

(c) (Theory)



In a MOSFET, there are three main sources of noise:

(i) *Thermal noise* due to the resistance of the channel:

$$ind^2 = \frac{8kTgm\Delta f}{3} \ A^2$$

This noise source can also be represented by an equivalent channel resistance rd = 3/2gm.

(ii) *Flicker (1/f) noise* in series with the gate:

$$vng^2 = \frac{k_f \Delta f}{CoxWLf} \ V^2$$

k_f is a flicker noise coefficient which is process dependent. Note that the 1/f noise is inversely proportional to gate area, thus bigger devices are less noisy.

(iii) *Shot noise* due to the gate-source leakage current:

$$ing^2 = 2qIg\Delta f \ A^2 \quad \text{(often neglected since negligible)}$$

(d) (Theory)

(e) (Application of theory)

$veq^2 = vns^2 + vn^2 + in^2|Z_S|^2$

where :

$$vn^2 = \frac{ind^2}{gm^2} + vng^2 = \frac{8kT}{3gm} + \frac{k_f}{WLCox\,f}\ V^2$$

$in^2 = ing^2 = 2qIg\Delta f\ \ A^2$

(f) (New Theory)

Increase the width of the transistor.

2.

(a) (Application of theory)

If distortion is a problem, differential configurations (ideally) get rid of even order harmonics.

(b) (Application of theory)

There are more than one, but the simplest answer is area.

(c) (Application of theory)

Statement B is correct. The noise is generated by uncorrelated sources.

(d) (Application of theory)

No, 10dB would correspond to a distortion which is larger than 0.5%.

(e) (Application of theory)

Reduce Vc. That would keep the transistor well into the triode region

(f) (Theory)

Assuming M1 is in the triode region:

$$I_{d1} = 2\beta(V_{cm} + V_{in} - V_{th})V_c - \beta V_c^2$$

If we set $I_1 = 2\beta(V_{cm} - V_{th})V_c - \beta V_c^2$, then $I_{out} = I_{d1} - I_1 = (2\beta V_c)V_{in}$

(g) (Application of theory)

The circuit is not working. It is showing instability, which would lead to think that the bandwidth of the amplifier is not high enough and needs to be improved.

3.

(a) (Theory/Application of Theory)

Looking at the frequency limits, H1 is lowpass, H2 is high pass, H3 is bandpass and H4 is band reject.

(b) (Theory)

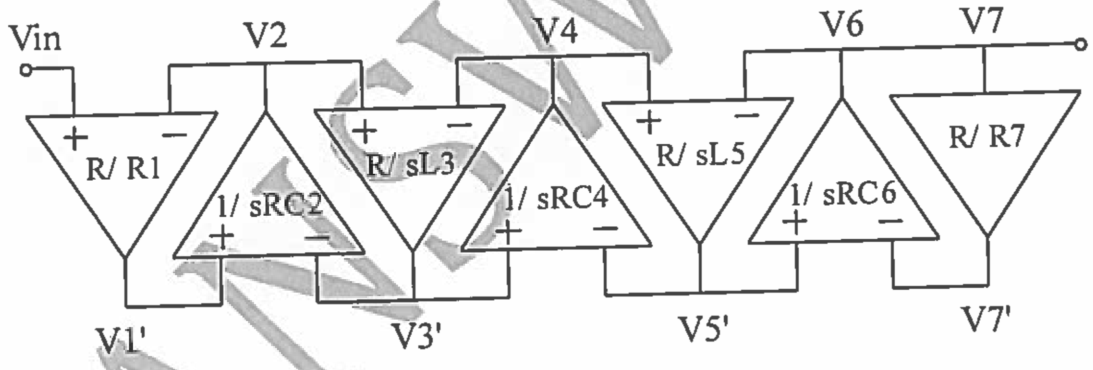
They are both integrators with transfer functions:

$$\frac{Vout}{Vin} = \frac{Gm}{sC} = \frac{\omega u}{s}$$

(c) (Theory)

The one with only one C takes less area, but the two differential outputs are asymmetrical due to the different parasitics at the top and bottom plates of the capacitor.

(d) (Computed example)



(e) (Computed example)

The equations resulting from the flow diagram are:

$V1 = Vin - V2$
$I1 = V1/R1$

$I2 = I1 - I3$
$V2 = I2/sC2$

$V3 = V2 - V4$
$I3 = V3/sL3$

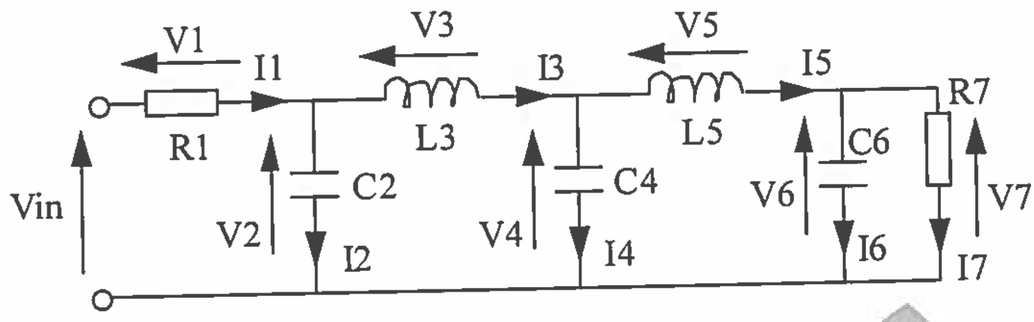
$I4 = I3 - I5$
$V4 = I4/sC4$

$V5 = V4 - V6$
$I5 = V5/sL5$

$I6 = I5 - I7$
$V6 = I6/sC6$

$V7 = V6$
$I7 = V7/R7$

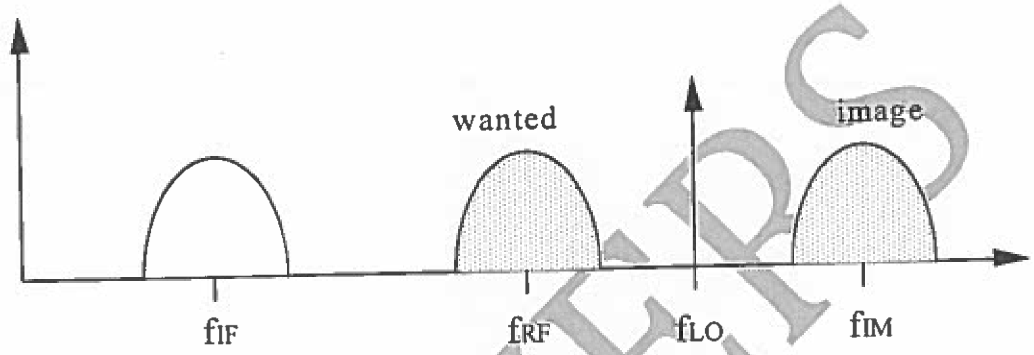
And from there, the LC ladder:



4.

(a) (Theory)

In receivers, when down converting to an intermediate frequency an undesired image channel (f_{IM}), as represented in the figure is also converted to this frequency and hence overlaps with the signal of interest. Hence, the image needs to be eliminated prior to down conversion. But the problem is that the lowest the intermediate frequency (which would be desirable to reduce the bandpass filter requirements), the less rejection of the image is going to be possible with a feasible lowpass filter.

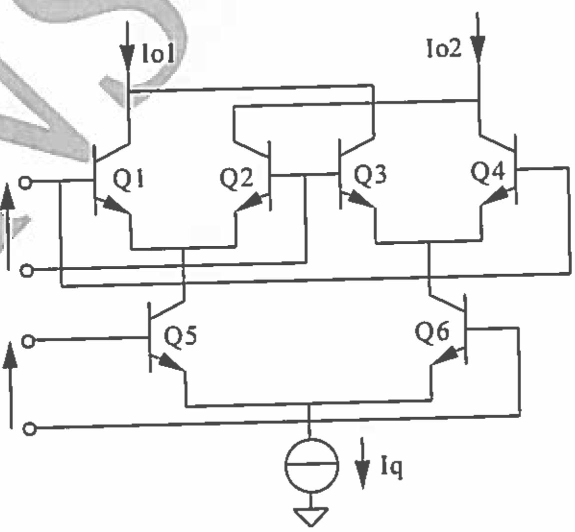


(b) (Theory)

Spurious response rejection.

(c) (Theory)

Any of the mixers in the lecture notes. For example:



(d) (Theory)

2kHz to prevent aliasing

(e) (New theory)
They didn't consider that the signal was not band limited (i.e. changing the cut-off frequency of the antialiasing filters).