UNIVERSITY OF LONDON
IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 1997

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER 1.6

HARDWARE

Wednesday, April 30th 1997, 4.00 - 5.30

Answer THREE questions

For admin. only: paper contains 4 questions

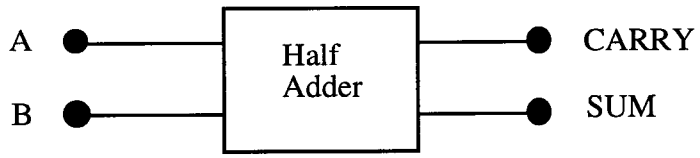
1. Computer Arithmetic

a. A half adder is defined using the equations:

$$SUM = A \oplus B$$

$$CARRY = A \bullet B$$

and can be drawn as a block diagram:



Show how two half adders and one OR gate may be connected up to make a full adder

b. A full subtractor circuit is defined by the following truth table:

A	B	P	DIFFERENCE	BORROW
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Find the simplest boolean equations for DIFFERENCE and BORROW from their respective truth tables and draw the corresponding circuits.

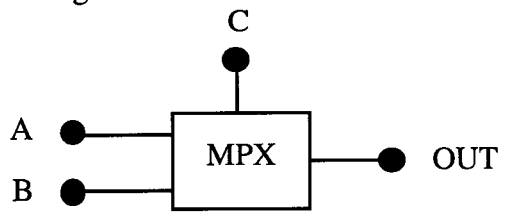
c. Show how a set of four full adders with some invertor gates can be connected up to make a four-bit two's complement subtractor circuit.

d. How many gates are required to implement one stage of the full subtractor circuit designed in part b? Is there any advantage in using the twos complement subtractor circuit designed in part c?

The four parts carry, respectively, 20%,40%, 20%,20% of the marks.

2. Registers and Multiplexors

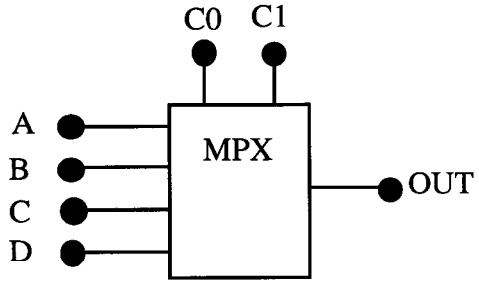
a. Design a circuit for a two way multiplexor shown diagramatically below, using AND, OR and Invertor gates.



The operation of the circuit is:

C	Function
0	OUT=A
1	OUT=B

b. A four way multiplexor has two control inputs and can be represented diagramatically as follows:



Using four way multiplexors, edge triggered D type flip flops and any other gates you need, design an n-bit general purpose register with two control inputs C0 and C1 which implements the following functions:

C0	C1	Function
0	0	Clear to Zero
0	1	Shift Left
1	0	Complement each bit
1	1	Shift Right

Show just one typical stage

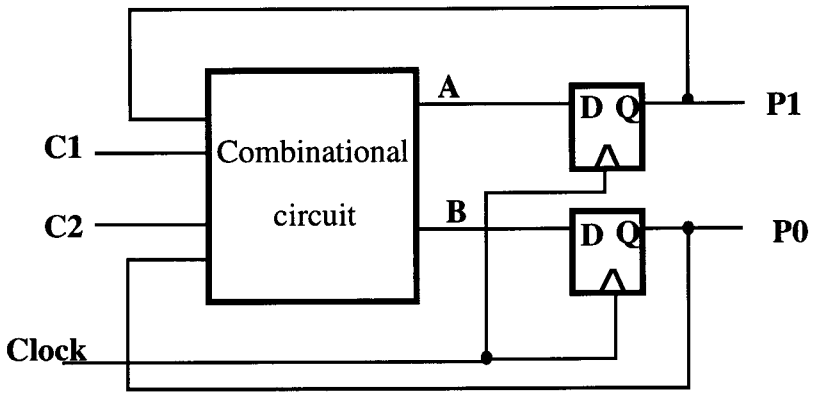
c. Show how to connect together three two input multiplexor circuits as designed in part a to make a four input multiplexor as used in part b.

The three parts carry, respectively, 25%,50%, 25% of the marks.

Turn Over

3. Counters

a. The following circuit is a controlled two-bit counter.



When the control signals C1 and C2 are set to **01** the counter becomes a binary up counter (P1,P0 = 00 --> 01 --> 10 --> 11 --> 00). When the control signal C1 and C2 are set at **10** the counter becomes a binary down counter (P1,P0 = 00 --> 11 --> 10 --> 01 --> 00). When the control signals are set at **00** the counter outputs P1,P0 remain at **00**. There is no useful function for the control inputs setting of **11**.

Draw the state transition diagram (finite state machine) for this counter and using as many "don't care" outputs as possible, complete the transition table for all combinations of C1 and C2 in the following format:

C1,C2 controls	**Current State / P1,P0**	**Next State / P1,P0**
01	**(0) 00** **(1) 01** **(2) 10** **(3) 11**	**(1) 01**
10	**(0) 00**	

b. Show the K-Maps for the two outputs **A** and **B** of the combinational circuit with inputs **C1, C2, P1,** and **P0**.

c. Design the minimum circuit and show the final transition diagram for all four input combinations. Will the described counter operate properly for all combinations of the input values?

The three parts carry 30% 40% and 30% respectively.

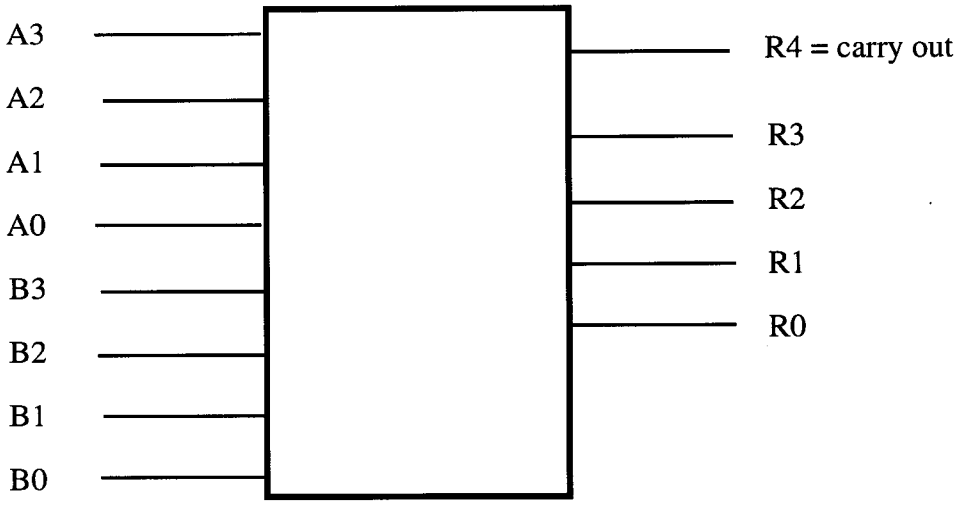
4. Binary Coded Decimal Processing

Binary coded decimal digits are represented by the **excess-3** encoding when the four bits are assigned in the following manner:

BCD digit	B3	B2	B1	B0 (bits)
0	0	0	1	1
1	0	1	0	0
2	0	1	0	1
3	0	1	1	0
4	0	1	1	1
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0

The rest of the bit combinations (**0000, 0001, 0010, 1101, 1110, 1111**) are not used and considered **invalid** BCD digit combinations.

The circuit for the BCD adder of two BCD digits is shown below:



a. Determine the Boolean equation for a four input one output circuit whose output is a **1** when an invalid BCD bit combination is input to it.

b. Show that when a simple four-bit binary adder is used to add two such BCD digits and a carry is not generated (**R4=0**) then a binary subtractor must be used to correct the resulting sum of the two BCD digits.

c. Show that when two BCD digits are added by a simple binary adder and a carry is generated (**R4=1**), then a binary adder must be used to correct the resulting sum of the two BCD digits.

d. Design the BCD adder for two BCD digits defined above (show your work and the final circuit). Assume that only valid BCD digits are used as input.

End of Paper