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AC1

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2006

MSc and EEE PART III/IV: MEng, BEng.and ACGI

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Tuesday, 9 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : C. Toumazou
Second Marker(s) : D.G. Haigh

1. (a) Figures 1(a) and 1(b) show two popular biasing schemes typically used in analogue integrated systems. Briefly outline the main feature of each of these circuits.

[3]

For the bandgap voltage reference circuit of Figure 1(a), show *that* $\delta V_0 / \delta T = 0$ (where T is temperature) if $(R_2/R_3)ln\ [\ I_1/I_2\ ] = 29$ for $V_0 = 1.283\ V$. Assume the temperature coefficient of V_{BE} to be -2.5mV/°C, the collector current of transistor Q_3 is 100μA and the device saturation current is $I_S = 1.2 \times 10^{-13} A$. Boltzmann's constant $k = 1.38 \times 10^{-23} J/K$ and the electron charge is $q = 1.6 \times 10^{-19} C$.

[6]

(b) Calculate the fractional temperature coefficient in ppm/°C for the current generator of Figure 1(b) at room temperature, given that R is a polysilicon resistor with a temperature coefficient of 1500 ppm/°C.

[3]

(c) Show that the circuit of Figure 1(b) can be developed into a current source with output current directly proportional to absolute temperature and virtually independent of supply voltage. It is likely that on power-up the output current will fall into a zero current state. Sketch a suitable start-up circuit that ensures that this condition will not occur and explain the operation of the circuit.

[8]

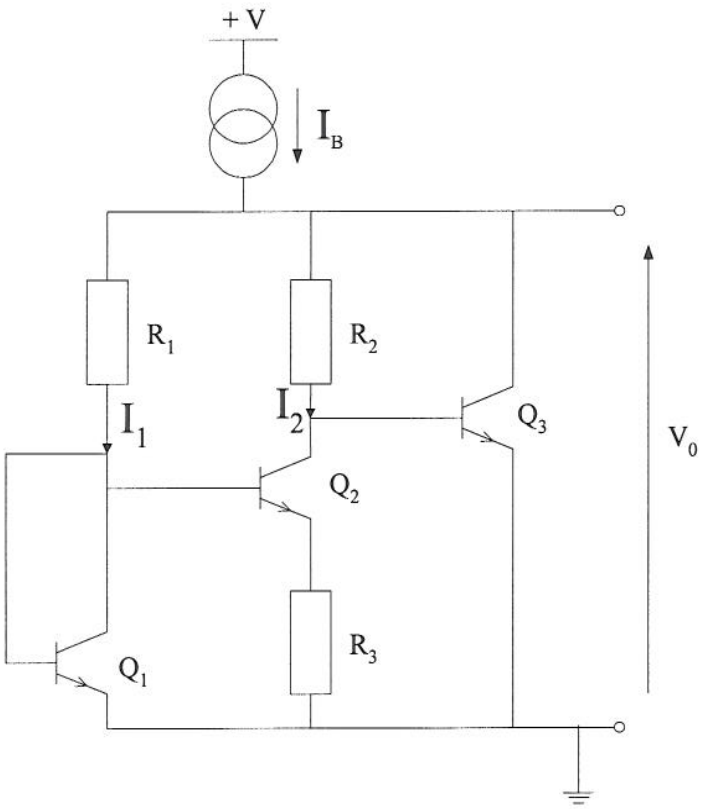

Figure 1(a)

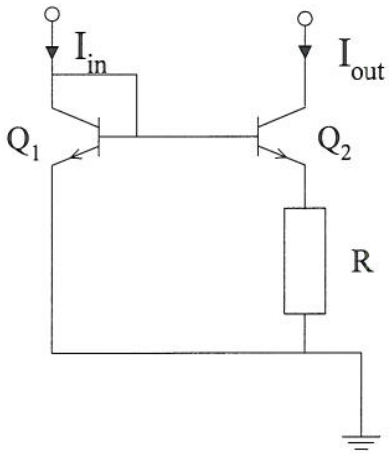

Figure 1(b)

2. Figure 2 shows the basic design of two analogue sampled-data precision integrators. Figure 2(a) is a switched-capacitor integrator and Figure 2(b) a switched-current integrator.

   (a) Derive an expression for the transfer function of both integrators. Assume that the integrators are driven by non-overlapping clocks and that the switches are ideal.

   [10]

   (b) (i) Sketch the basic design of a 3rd-order Chebyshev low pass switched-capacitor ladder filter.

   (ii) Explain the function of all components in the circuit. The filter is to have a cut-off frequency of 5kHz. Assume a clocking frequency of 100 kHz. The values of integration capacitive for the capacitor based sections are 5.06pF, inductive and the section is 3.49pF. All other switched capacitors are 1pF.

   (iii) From the circuit, estimate normalised passive component values for the original double-terminated LC prototype of the filter. All values should be normalised to 1 rad/s. You may assume that the clocking frequency is so high that the integrators can be assumed lossless.

   [10]

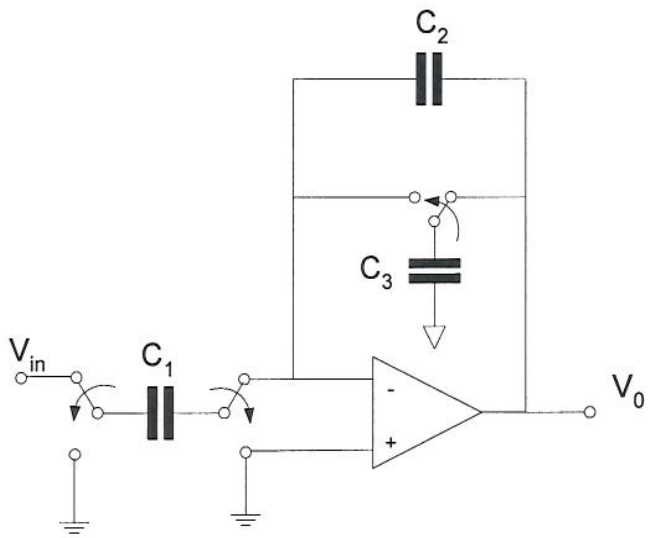

Figure 2(a)

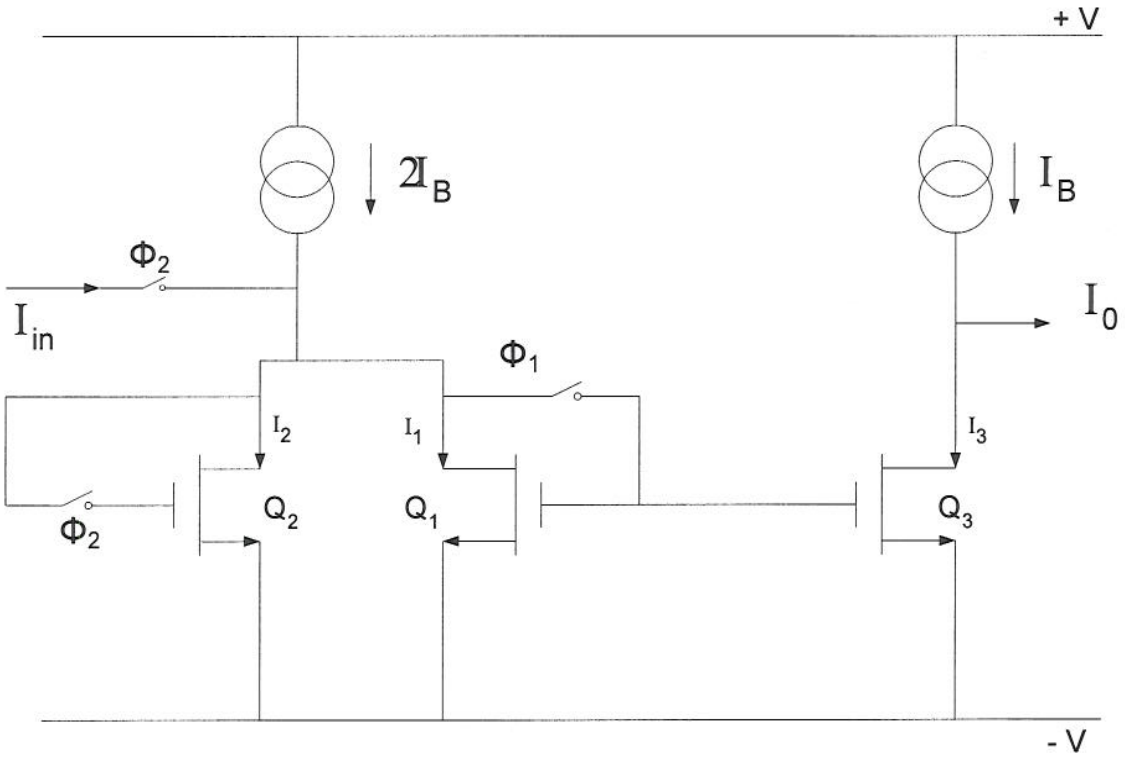

Figure 2(b)

3. (a) In mixed-mode ASIC design, the process technology is chosen to optimise digital performance specifications. Give one example of the constraints this places upon analogue circuit design performance.

[2]

(b) A fundamental limitation imposed on the Dynamic Range (DR) of any high performance A/D converter will ultimately be switch noise. Prove that the fundamental limit is given by,

$$DR = \frac{V_{ref}}{\sqrt{(10kTRf_c)}}$$

where V_{ref} is the reference voltage, k is the Boltzmann's constant, T is absolute temperature, R is switch resistance and f_c is the clock frequency of the switch. You may assume that the system settles in 10τ (where τ is the time constant), over one period of the clock frequency.

[6]

(c) A very high resolution analogue-to-digital converter is the oversampling converter sometimes referred to as the sigma-delta modulator. Sketch a typical architecture for such a converter and explain its principles of operation, in particular the feedback noise shaping mechanism.

[12]

4. (a) Under what operating conditions does the MOSFET of Figure 4(a) realise a linear floating resistor between terminals *A* and *B*? Show that under these conditions the equivalent resistance R_{AB} can be approximated by

$$R_{AB} = \frac{L}{KW(V_{GS} - V_T)}$$

stating any assumptions. All symbols have their usual meaning.

[5]

(b) Discuss three sources of non-linearity in the single MOSFET resistor realisation of Figure 4(a) and suggest one suitable circuit design to help eliminate one or more of these non-linear terms showing the necessary circuit analysis to confirm your design.

[5]

(c) For the current mirror of Figure 4(b), derive the expression for minimum output voltage while still maintaining saturated devices. Derive this voltage in terms of device threshold voltage V_T clearly stating any assumptions you make.

[4]

(d) Sketch a regulated cascode current-source and explain why the output resistance of the current source is higher than a standard cascode mirror.

[6]

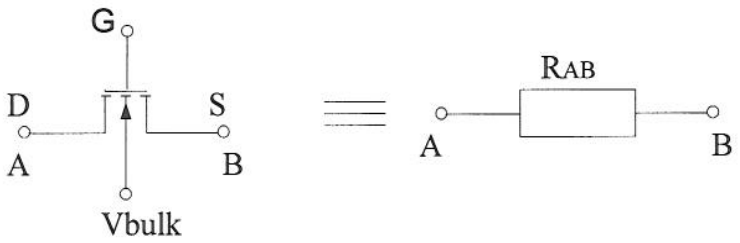

Figure 4(a)

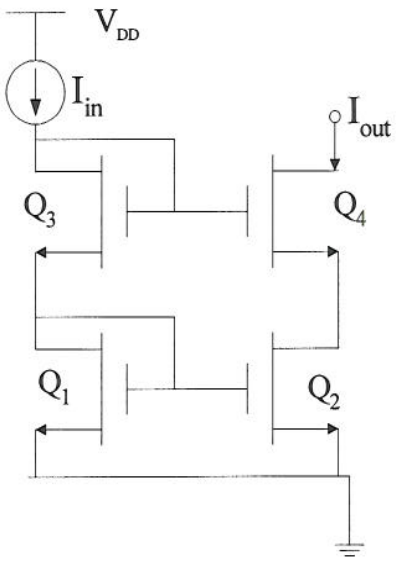

Figure 4(b)

5. Figure 5 shows a partially-designed two-stage CMOS op-amp required to give a voltage gain of approximately 80 dB, a slew-rate of 5 *V/μs* and a gain-bandwidth product of 3 MHz.

   (a) Given that the technology is a fixed 5 μm double metal CMOS process, design the channel widths of transistors Q1, Q2 and Q6 for the op-amp to meet the above performance specifications. Aspect ratios of all other devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below.

   [15]

   (b) Give a reason why the introduction of a single integrated resistor in series with the compensation capacitor should significantly improve the amplifier's phase margin.

   [5]

CMOS TRANSISTOR MODEL PARAMETERS

MODEL PARAMETERS	$Kp\ (\mu A/V^2)$	$\lambda\ (V^{-1})$	$V_{T0}\ (V)$
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

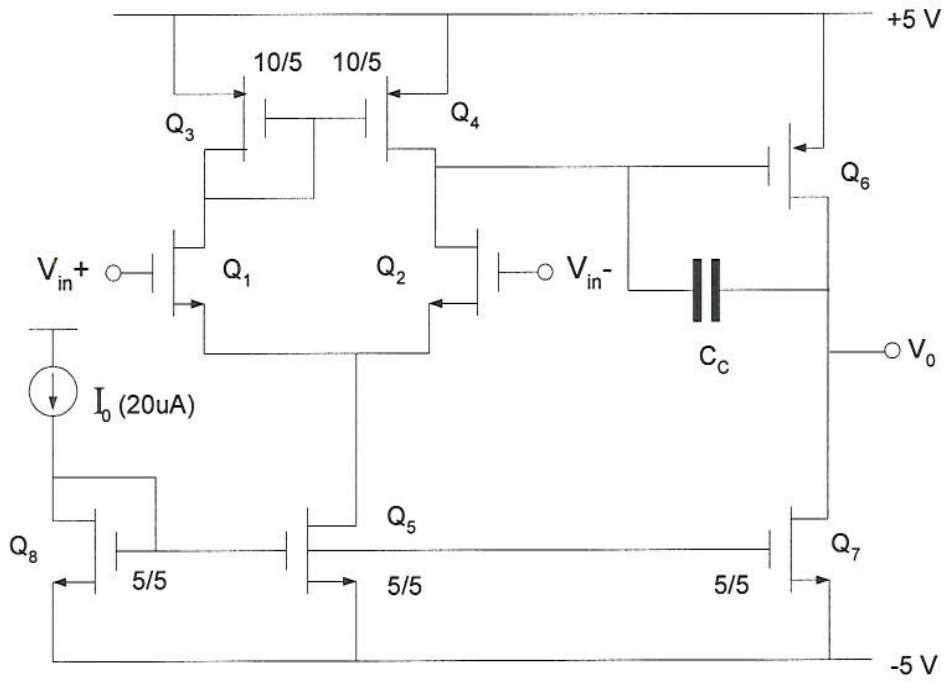

Figure 5

6. (a) Give two advantages of current-mode analogue signal processing compared to traditional voltage-mode processing.

[2]

(b) With the aid of a suitable macromodel, explain the theoretical concept of current feedback and how it results in constant bandwidth amplification. Using a current-feedback op-amp, design a closed-loop non-inverting gain stage with a bandwidth of 10 MHz for a fixed voltage gain of 100. Assume an internal compensation capacitance of 4pF and that the open-loop transresistance gain of the amplifier is very much larger than the amplifier feedback resistor.

[13]

(c) The circuit shown in Figure 6 is a single bit cell of a current-mode algorithmic analogue to digital converter. Briefly describe the operation of the cell and give reasons why this converter is particularly suitable for mixed analogue and digital VLSI.

[5]

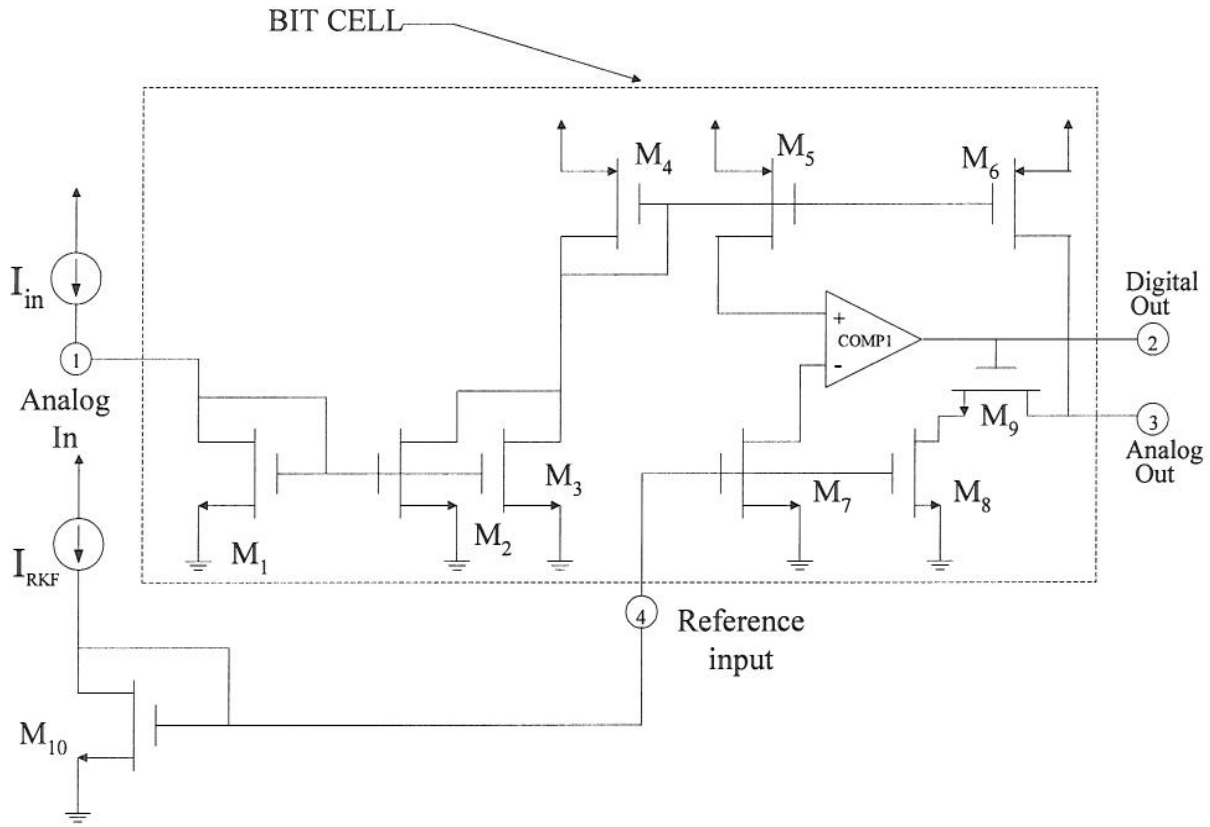

Figure 6

2006 EXAM ORIGINAL.

3rd Analogue Integrated Circuits and Systems

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SOLUTIONS

1st MARKER

C. TOUMAZOU

2nd MARKER

D. HAIGH

CT

ANALOG

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1/16

Q1/ Bandgap voltage reference circuit has almost zero temperature coefficient. Used many as stable voltage reference in ICs. 1

PTAT (Proportional to absolute temperature) current generator. Output current usually insensitive to power supply voltage. Used as a biasing circuit in most precision ICs. 2

For BG reference :- $V_{BE1} = V_{BE2} + I_2 R_3$ $(\beta \gg 1)$

Since

$$V_{BE1} - V_{BE2} = V_T \ln (I_1/I_2)$$

then $V_o = V_{BE3} + (R_2/R_3) V_T \ln (I_1/I_2)$

$V_T \ln [I_3/I_s]$ → assume room temp.

for $dv_o/dt = 0$, then $dV_{BE3}/dT = \frac{V_T}{T}\frac{R_2}{R_3}\ln\frac{I_1}{I_2}$

Since $\frac{dV_{BE}}{dt} = -2.5\,mV/°C$, $\frac{V_T}{T} = \frac{1.38\times10^{-23}}{1.6\times10^{-19}}$

then $\left(\frac{R_2}{R_3}\right)\ln\left(\frac{I_1}{I_2}\right) = 29$ and so

6

$$V_o = 1.283\,V$$

CT

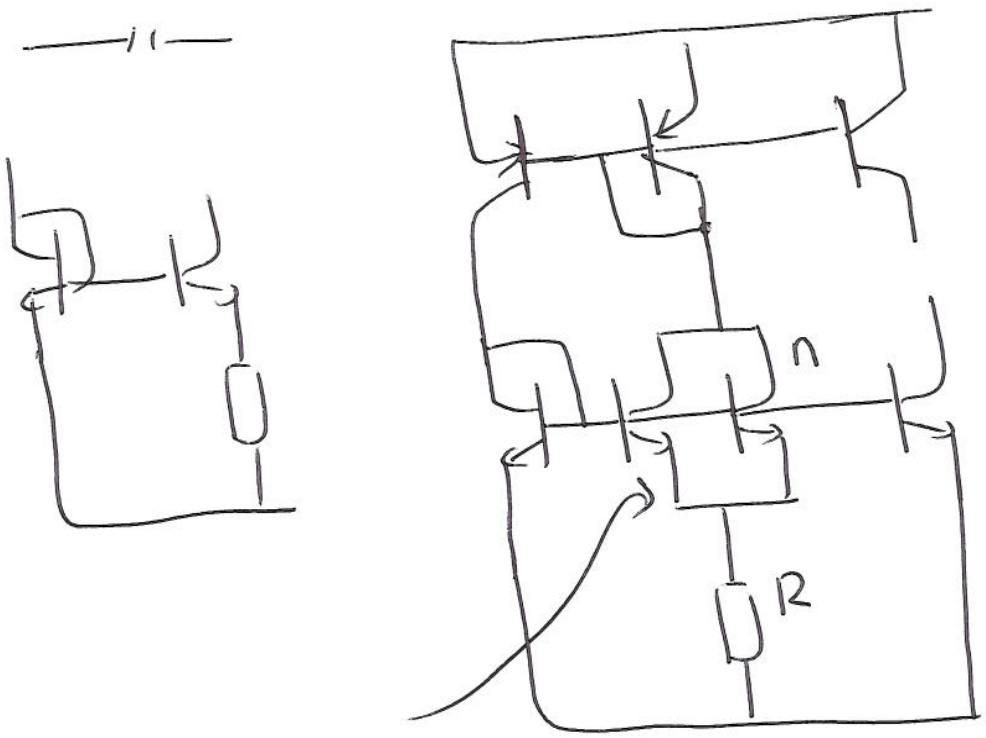
For PTAT temperature coefficient

V_T cancells with negative temperature coefficient of resistor

$$\therefore \quad TCF = \frac{1}{V_T}\,\partial V_T/\partial T - \frac{1}{R}\,\partial R/\partial T$$

$$= \frac{1}{T} - 1500\times10^{-6} \quad @ \text{ Room } T = 1833 \text{ ppm/°C}$$

3



n-emitter

Self biasing scheme

requires start-up

$$I_O = V_T \ln\left[n/R\right]$$

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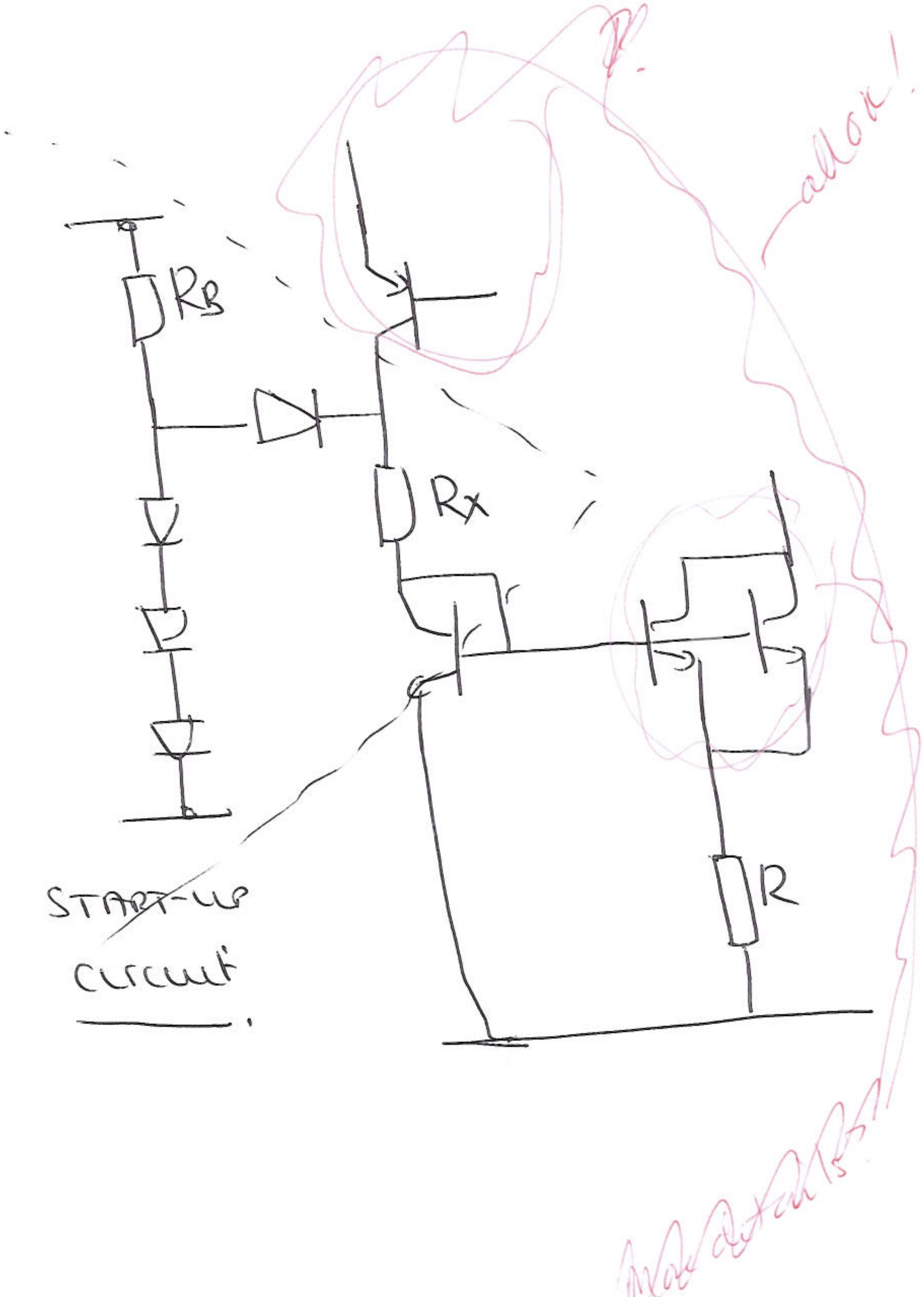

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③

Q2/

Fig 2a lossy integrator

During ϕ_1 of switch, $I_{av} = C_1 V_{IN}/T$

ϕ_2 $-C_1 V_{IN}/T = V_o[j\omega C_2] + \frac{C_3 V_o}{T}$

Transfer of charge

recovery yields

$$V_o/V_{IN} = -C_1/C_3 \left[\frac{1}{(1 + j\omega \frac{C_2}{C_3} T}\right]$$

$$= -\frac{C_1}{C_3} \frac{1}{(1 + jf/f_p)}$$

$$f_p = \frac{1}{2\pi \frac{C_2}{C_3}} f_c.$$

5

Fig 2b - switched current, ideal integrator

During ϕ_2 of period $(n-1)$, Q2 samples
Q1 holds

$$I_2(n-1) = I_B + I_{IN}(n-1) + I_o(n-1)$$

During ϕ_1 of period n, Q1 samples, Q2 holds

$$I_1(n) = 2I_B - I_2(n-1) = I_B - I_{IN}(n-1) - I_o(n-1)$$

$$\Rightarrow I_o(n) = I_{IN}(n-1) + I_o(n-1)$$

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In Z domain

$$Io(z)\left[1 - z^{-1}\right] = I_{in}(z)z^{-1}$$

$$H(z) = \left(Io/I.n\right)_z = \frac{z^{-1}}{(1 - z^{-1})}$$

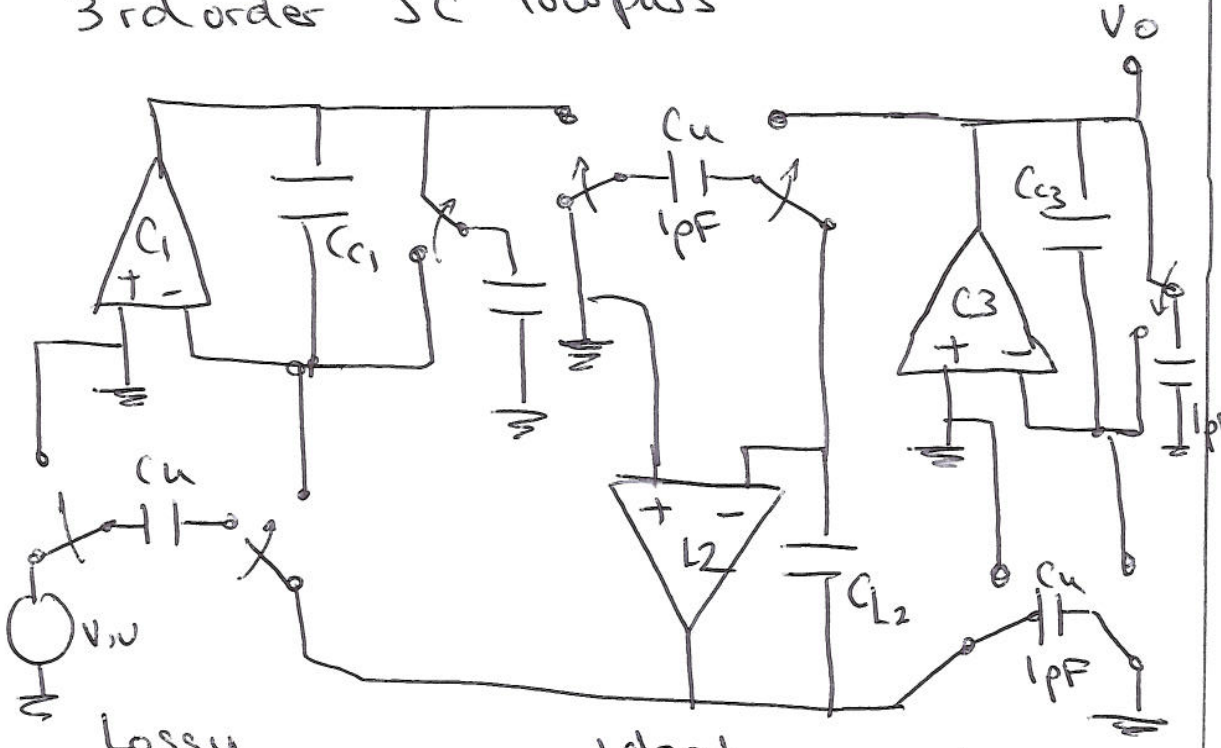
$$= \frac{1}{z - 1}$$

Since $z = e^{j\omega T}$ $\approx (1 + j\omega T)$ for

$\omega T << 1$

$\therefore H(z) = \frac{1}{j\omega T}$ lossless Integrator. 5

c) 3rd order SC lowpass



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5 CT

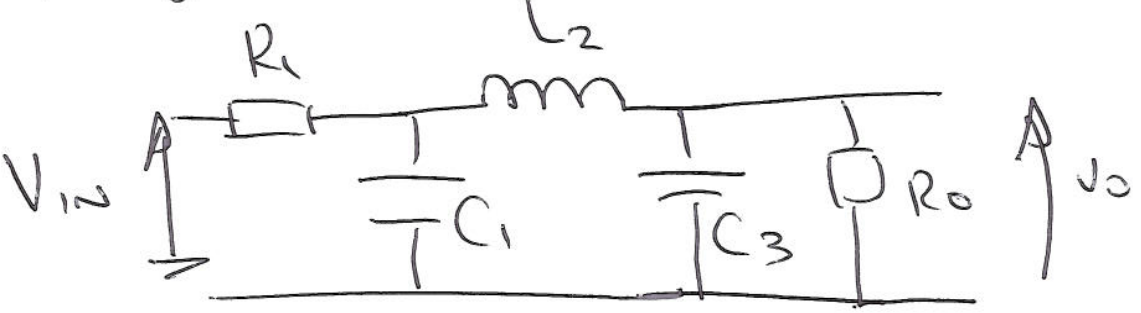
General transformation rules

$$\frac{f_c L_2}{R_s} = \frac{C_{L2}}{C_u}, \quad C_{C3}/C_u = f_c R_s C_3$$

↑ inductor ↑ capacitor

R_s (during scaling resistor)

Prototype



From Sc equivalent

$$C_{C1} = C_{C3} = 5.08\,pF, \quad C_{L2} = 3.49\,pF$$

$$C_u = 1\,pF$$

Assume $R_s = R_i' = R_o = 1\,\Omega$

$\therefore L_2 = C_{L2}/f_c = 3.49 \times 10^{-5}$

normalized ($\times 2\pi f_o$) = 1.096

$C_1 = C_3 = C_{C3}/f_c = 5.08/100 \times 10^3 = 5.08 \times 10^{-5}$

normalized $\times 2\pi f_o$ = 1.596

5

6

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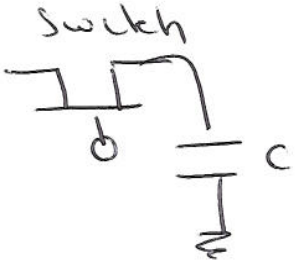
Q3/ Constraints

a) 1/ low voltage - low dynamic Range
2/ Non-Linear process technology - Distortion. 2

b) Dynamic Range $\triangleq$ Vref/Noise $= 2^N$



Rms noise of switch driving capacitor

$$= \sqrt{\frac{kT}{C}}$$

$$\therefore DR = \frac{Vref}{\sqrt{\frac{kT}{C}}} = 2^N$$

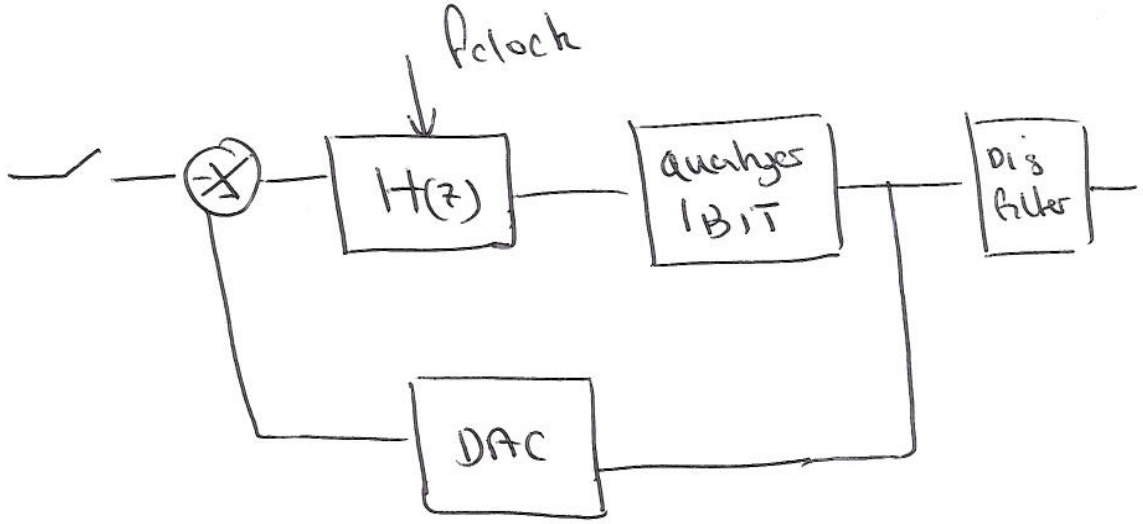
Assume $f_c = 1/(10RC)$

then solving for C gives

$$DR = 2^N = Vref/\sqrt{kT@RC}$$

6

c)



Basic idea is that coarse quantization noise gets shaped by 1/(Hz) via feedback

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CT

Generally H(z) is an integrator so noise is shaped differentially. This reduces requirements upon component accuracy. The architecture includes a negative feedback loop produces the coarse estimate that oscillates about the true value of input, the digital filter averages this coarse estimate to produce a finer approximation. The feedback DAC and forward integrator force the quantization error to have a high frequency spectrum. The output of the digital filter is down sampled and given a multibit digital representation. High frequency quantization noise is reduced. Noise shaped giving very high (S/N) at low frequency.

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CT

Q4/

Assumption is that if ($V_{DS} \approx 0$) or ($V_{DS} << V_{GS} - V_T$) device acts in Linear region. From

$$I_D = \frac{KW}{L}\left[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2\right][1 + \lambda V_{DS}]$$

for $V_{DS} << (V_{GS} - V_T)$, then $\lambda V_{DS} << 1$

so $$I_D = \frac{KW}{L}(V_{GS} - V_T)V_{DS}$$

OR $$R_{AB} = V_{DS}/I_D = L/(KW(V_{GS} - V_T))$$ 5

Three sources of Non-linearity

(i) Limited due to V_{BS} changing V_T for negative V_{BS} due to body-effect.

ie $$V_T = V_{TO} + \gamma\left[\sqrt{-V_{BS} + 2\phi_F} - \sqrt{2\phi_F}\right]$$

γ = bulk threshold parameter

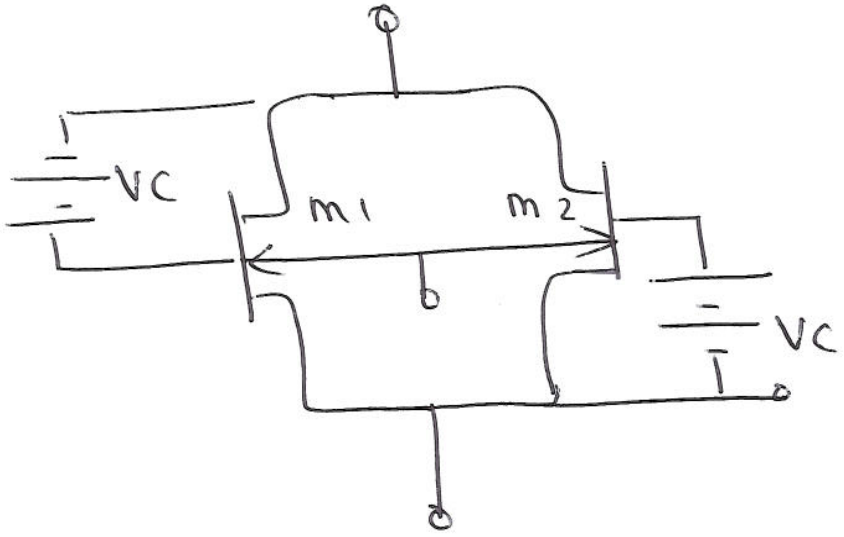
ϕ_F = Fermi-level potential

(ii) Limited due to V_{DS} approaching $(V_{GS} - V_T)$ hence saturation region for large positive V_{DS}.

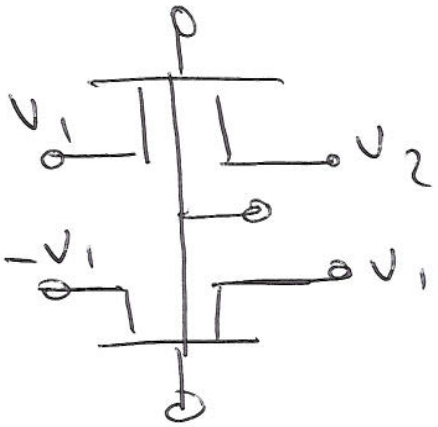
(iii) For large values of V_{DS} the $V_{DS}^2/2$ term introduces large Non-linearity. 3

GT

4 cont

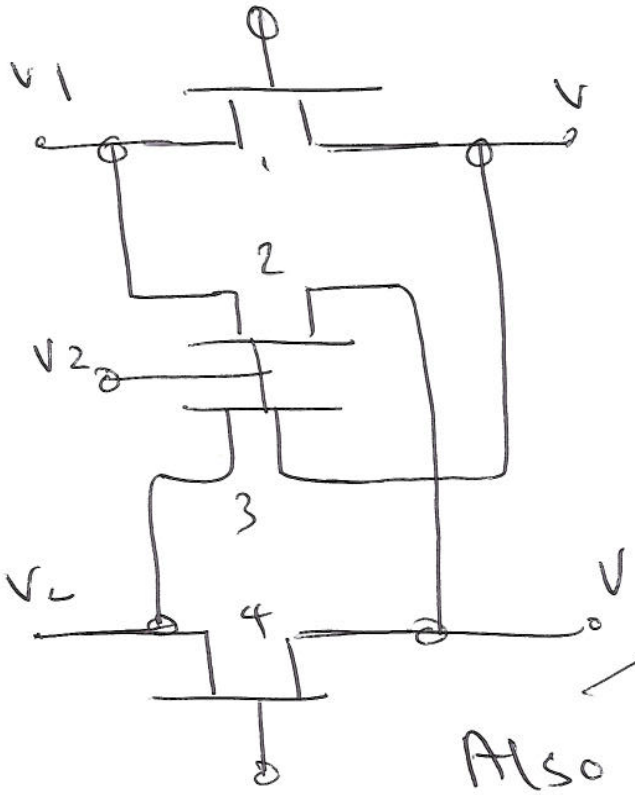


Parallel circuit - eliminates $V_{ds}^2/2$ term.



Differential scheme

Effects of V_{DS} cancelled.



Double differential MOS

Eliminates

- V_{DS} and V_T term

2

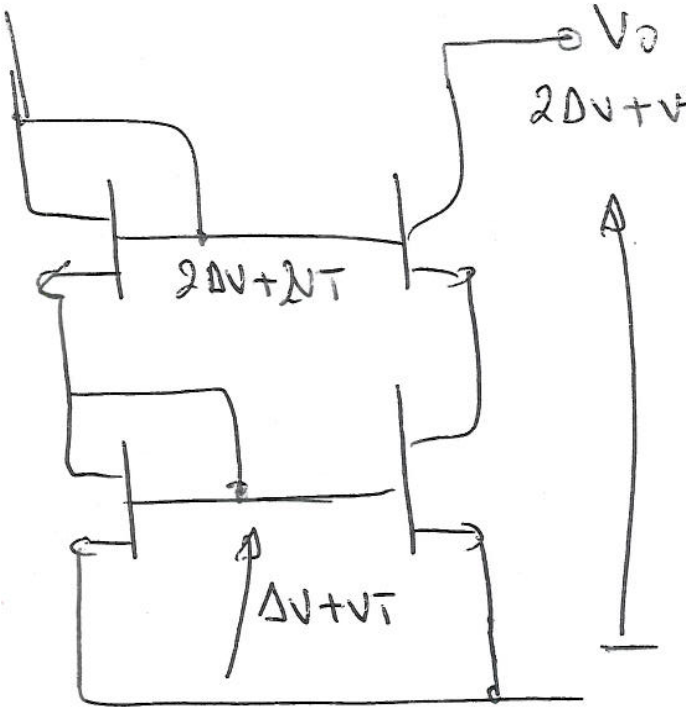
Any one would do

Also expect analysis of particular cell.

6

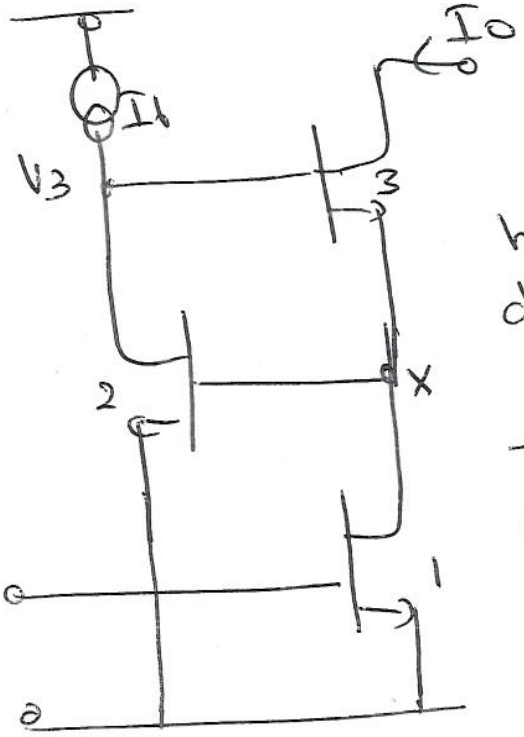
10

4 cont



Assume
$\Delta V = V_{GS} - V_T$
for sat
$V_{DS} \geq V_{GS} - V_T$

$$(V_o)_{min} = 2(\Delta V + V_T) - V_T \quad 4$$
$$= 2\Delta V + V_T$$



Q_3 cascodes Q_1 hence output resistance due to Q_3 is
$R_{o3} \approx r_{ds1} g_{m3} r_{ds3}$

Transistor Q_2 senses change in voltage at node (X) and reduces these changes by the loop gain of the amplifier (Q_2 and I_b) hence this further increases the output resistance of the circuit to
$R_{out} = R_{o3} g_{m2} r_{ds2} g_{m3} r_{ds3} r_{ds1} \approx (g_m^2/g_o^3)$ 6 (T
Assuming equal g_m and g_{ds}.

11

5// Specs $A = 80dB$, $S.R = 5V/\mu s$, $GB = 3MHz$

$A_1 = g_{m2}/(g_{04}+g_{02}) \Rightarrow (g_{02}+g_{04})$

$= I_{D2}(\lambda_N + \lambda_P)$

$= 10\times10^{-6}[0.05)$

$= 5\times10^{-7}\ \Omega^{-1}$

$g_{m2} = 2\sqrt{\beta_2 I_{D_2}} \Rightarrow$ but $G.B = \frac{g_{m_2}}{2\pi C_c}$

require C_c. From $S.R = I_D/C_c$

Then $C_c = 4pF \Rightarrow g_{m2} = 7.54\times10^{-5}$

$\therefore A_1 = 150.8$

From $g_{m2} = g_{m1} = 2\sqrt{\beta I_D}$

$\beta_2 = \beta_1 = 1.42\times10^{-4} = \frac{KW}{2L}$

$\therefore (W/L)_2 = (W/L)_1 = 9.46$

$= \underline{\underline{47/5}}$ 10

Since $A_1 = 150.8$, $A_2 = 10^4/(150.8)$

$= 66$

$A_2 = g_{m6}/(g_{06}+g_{07})$

$(g_{06}+g_{07}) = I_{D1}(\lambda_6 + \lambda_7)$

12 (T

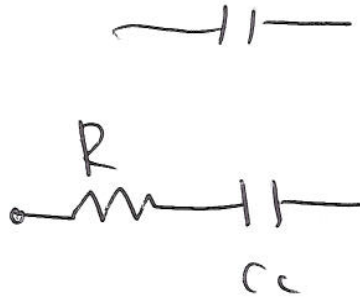
(5) cont

$$(g_{o6} + g_{o7}) = 20\times10^{-6}(0.05) = 1\times10^{-6}\,\Omega^{-1}$$

Since $g_{m6} = 6.63\times10^{-5}$

$$\Rightarrow \beta_6 = \left(\frac{g_{m6}}{2}\right)^2 \frac{1}{I_{D6}} = 5.5\times10^{-5}$$

Thus gives $(W/L)_6 = 5.5 = \underline{\underline{27/5}}$ 5



Function of R is to provide feedforward compensation and eliminate RHP zero from transfer function of OP-Amp.

With $R \Rightarrow Zero = g_{m6}/C_c$,

With R $\quad Z = \dfrac{1}{(1/g_{m6} - R)C_c}$

① $R = 1/g_{m6}$ → remove zero improve ϕ 5

② $R \Rightarrow$ non-dominant pole cancels with zero.
↳ $> 1/g_{m6}$

13 CT

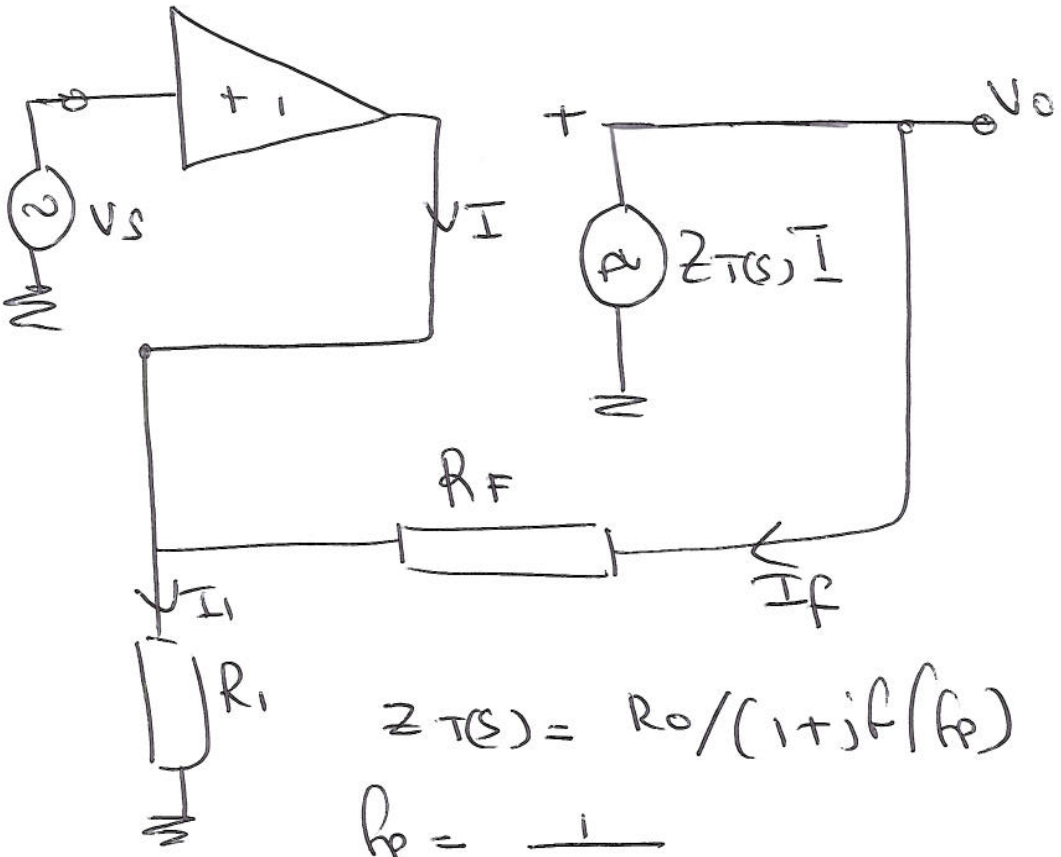
6/

Advantages of Current-mode

It has frequency performance, wide dynamic range

lower power supply voltage

2



$$Z_{T(S)} = R_0/(1+jf/f_p)$$

$$f_p = \frac{1}{2\pi R_0 C}$$

C = compensation capacitor

3 equations

$$I_f = (V_0 - V_s) R_F \quad - (1)$$

$$I_1 = V_s/R_1 \quad - (2)$$

$$V_0 = Z_{T(S)} I = Z_{T(S)} [I_1 - I_f] \quad - (3)$$

8

14

CT

Subs ① and ② into ③ gives,

$$\left(V_o/V_s\right) = \left(1+R_F/R_1\right) Z_{T(s)}/\left(R_F+Z_{T(s)}\right)$$

Subs for $Z_{T(s)}$ — gain

$$\left(V_o/V_s\right)_{fw} = \left(1+RF/R_1\right)\left[\frac{R_O}{R_O+RF}\right] \times \frac{1}{\left(1+jf/f_p\left[\frac{R_O+RF}{RF}\right]\right)}$$

BW

Assuming $R_O \gg RF$

then

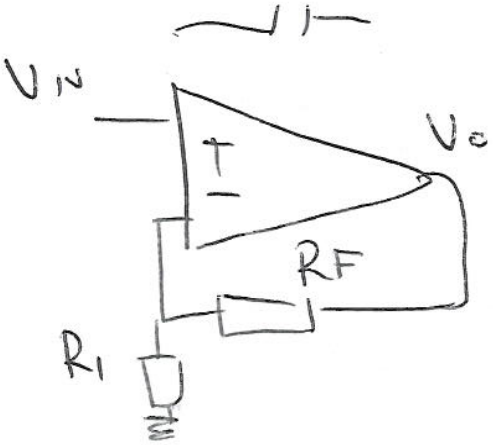
Closed loop gain $\simeq (1+RF/R_1)$ — *

Closed loop Bandwidth $\simeq \frac{f_p R_O}{RF} = \frac{1}{2\pi RFC}$

L*.

Hence RF sets the amplifiers constant BW

and R_1 chosen to set the gain



$BW = \frac{1}{2\pi RFC} = 10\text{MHz}$

$\therefore$ given $C = 4pF$

$RF = 3.98k\Omega$

Since $A = (1+RF/R_1) = 100$

$R_1 = 44\Omega$

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CT

Algorithmic Converter

$2I_{IN}$ on +ve terminal of comparator compared to I_{ref} (-ve) terminal

If $2I_{IN} < I_{ref}$, comp output goes low

digital output = 0 and analogue output = $2I_{IN}$

If $2I_{IN} > I_{ref}$, comp output goes high

digital output = 1, analogue output $2I_{IN} - I_{ref}$

Analogue output consequently feeds into following 'bit' which performs exactly the same function.

The process is repeated as many times as necessary to achieve desired resolution.

Digital VLSI — small size,
low-power
supply voltage
less stringent
upon analogue accuracy

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CK