IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2012

EEE PART I: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 1

Monday, 11 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : A.S. Holmes
Second Marker(s) : B. Clerckx

The Questions

1. For each part of this question, state clearly any assumptions made in your calculations.

   a) For the circuit in Figure 1.1, determine the operating mode of the transistor and its collector current.

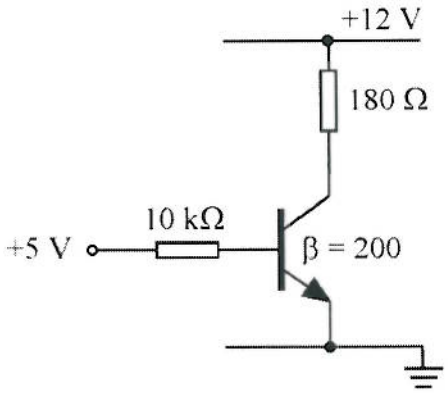

Figure 1.1 [6]

   b) For the circuit in Figure 1.2, determine the operating modes of both MOSFETs and the value of the current I. The MOSFETs are matched and have large signal parameters $K = 0.25\ mA/V^2$ and $V_t = 1\ V$.

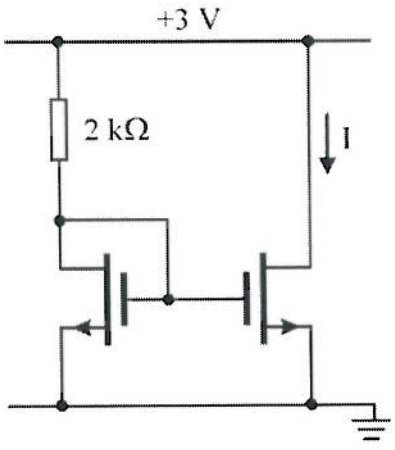

Figure 1.2 [8]

   c) Sketch the circuit for a Class B push-pull output stage, and explain why such a circuit exhibits cross-over distortion. To aid your explanation sketch the output waveform you would expect to see if the stage were driven by a sinusoidal signal with a peak-to-peak amplitude of 10 V. [8]

Question 1 continues on the next page...

Question 1 continued

d) For the circuit in Figure 1.3, determine the minimum supply voltage V_{DD} for which the MOSFET will be in the active mode.

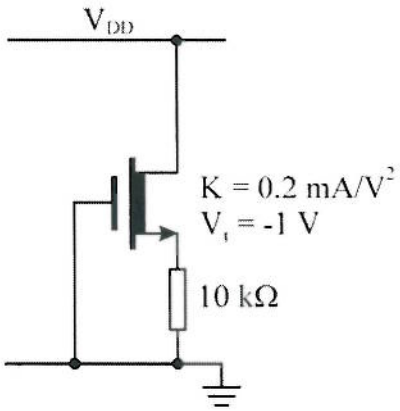

Figure 1.3 [4]

e) The voltage V_{IN} in Figure 1.4 changes to zero volts at time t = 0, after having been held at +5 V for a long time. V_{IN} remains at zero for 500 μs, and then returns to its original value of +5 V. Explain why the resulting output voltage waveform is as shown in the sketch to the right, and calculate the durations of the two ramp sections in the waveform.

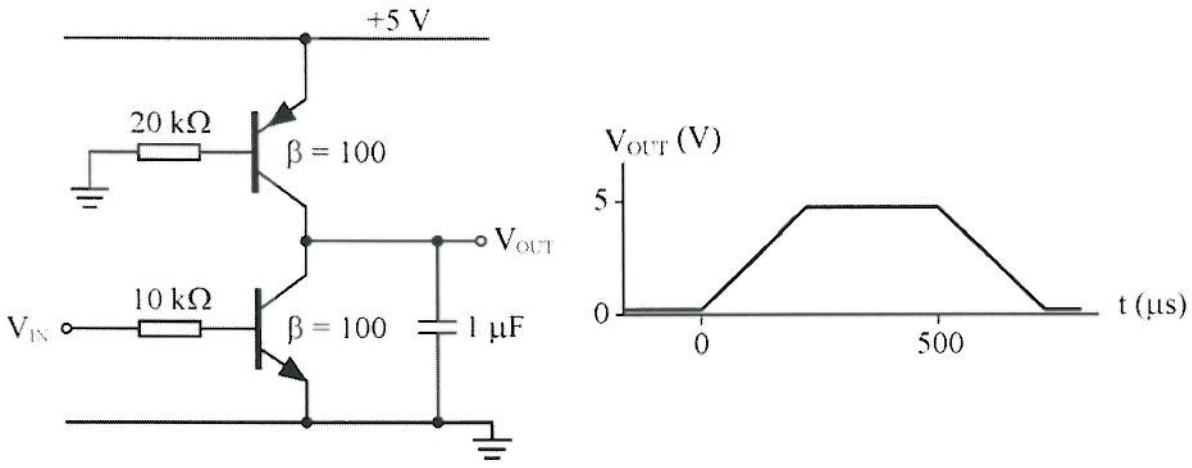

Figure 1.4 [8]

f) The characteristic equation for a phase-shift oscillator is of the form:

$$(1+K)u^3 + 6u^2 + 5u + 1 = 0$$

where K is the voltage gain of the amplifier, and u = sRC, with s being complex frequency and R, C being the component values in the phase-shifting network. Derive an expression for the frequency of stable oscillation. [6]

2. a) For the amplifier in Figure 2.1, choose values of R_B and R_C to give a collector bias current of 0.5 mA and a quiescent output voltage of 5 V. State clearly any assumptions you make. Comment on the stability of the biasing arrangement used in the circuit and how this might be improved. [8]

b) Draw a small-signal equivalent circuit for the amplifier in Figure 2.1, and determine the small-signal macromodel parameters (input resistance, output resistance and voltage gain) assuming the resistor values are as you calculated above. [12]

c) An amplifier similar to that in Figure 2.1, with the resistor values you calculated above, is inserted between a signal source and a load as shown in Figure 2.2. Determine the overall voltage gain v_L/v_S for this arrangement in the mid-band, and draw a dimensioned sketch showing the variation of $|v_L/v_S|$ with frequency over the range 1 Hz to 10 kHz. [10]

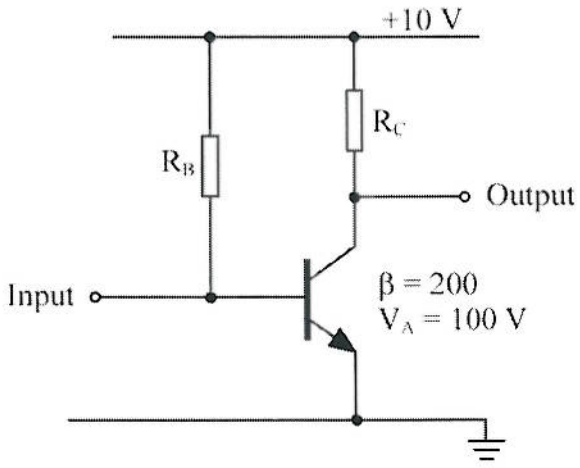

Figure 2.1

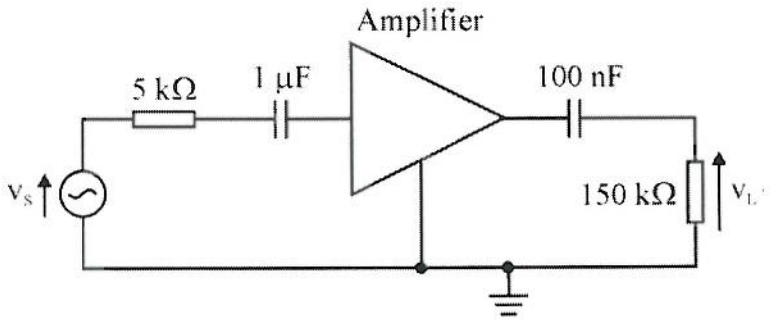

Figure 2.2

3. Figure 3.1 shows a single-stage CMOS amplifier in which a p-channel MOSFET provides the active load for an n-channel MOSFET. The active load is biased using an externally applied voltage V_G.

a) Calculate the value of V_G that will give a quiescent drain current of 0.4 mA. Also determine the quiescent output voltage of the circuit under these conditions, and verify that both MOSFETs are saturated under quiescent conditions. [8]

b) Draw a small-signal equivalent circuit of the amplifier, and hence determine its small-signal voltage gain. Also calculate the small-signal input resistance of the circuit. You may assume the input capacitor is effectively short-circuit at signal frequencies, and that V_G has the value you calculated in part a). [12]

c) Assuming the value of V_G you calculated in part a), determine the approximate range of output voltages over which both transistors will remain saturated. Show how, by adding one resistor to the circuit, the quiescent output voltage could be moved to the middle of this range. What value of resistor would be needed? [10]

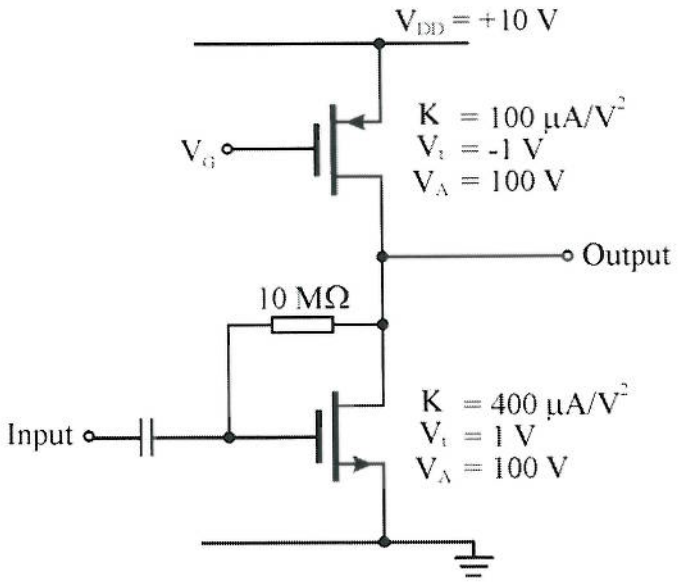

Figure 3.1

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Question 1

a) The transistor is conducting since the EBJ is forward biased. Assuming $V_{BE} = 0.7$ V, the base current is $(5 - 0.7)/10k = 0.43$ mA.

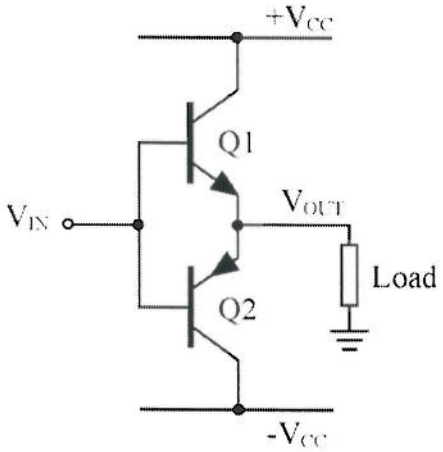
If the transistor were active, then the collector current would be $200 \times 0.43m = 86$ mA. But this would imply a collector voltage of $12 - 180 \times 86m = -3.48$ V which is not possible. Therefore the **transistor is saturated**.

Assuming $V_{CE} \sim 0.2$ V in saturation, the collector current is $(12 - 0.2)/180 =$ **65 mA**. [6]

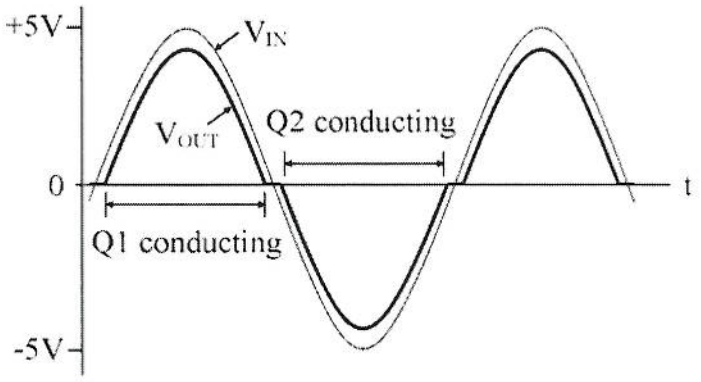
b) The **LH MOSFET** is D-G connected and since it is an enhancement mode device we know it is in **active mode**. Furthermore, since the **RH MOSFET** has the same V_{GS} and a higher V_{DS}, we know this device is also in **active mode**.

Considering the LH side of the circuit, the drain current of the LH MOSFET must satisfy $I_D = K(V - V_t)^2 = (3 - V)/2k$. With $K = 0.25$ mA/V^2 and $V_t = 1$ V, this becomes $(V - 1)^2 = 2(3-V)$. The solution is $V = \sqrt{5}$, and substituting this value back into the drain current equation gives $I_D = (3 - \sqrt{5})/2k = 382$ μA. Since the MOSFETs are matched, it follows that **I = 382 μA**. [8]

c) Class B push-pull output stage:



Output waveform with 10 Vpp input:



When V_{IN} is positive, Q1 conducts and acts as an emitter follower, so the output follows the input but dropped down by $V_{BE} \sim 0.7$ V. Conversely, when V_{IN} is negative, Q2 acts as the emitter follower and the output is raised above the input by $V_{BE} \sim 0.7$ V. However, when the input voltage is near zero, neither transistor conducts and the output goes to zero. This leads to distortion in the output waveform around the zero-crossing points, as shown. [8]

Question 1 continued

d) If the MOSFET is active, then the drain current must satisfy $I_D = K(-V_S - Vt)^2 = V_S/10k$. With $K = 0.2$ mA/V^2 and $V_t = -1$ V, this becomes $2(1 - V_S)^2 = V_S$, or $2V_S^2 - 5V_S + 2 = 0$. The roots are $V_S = 2$ V, $V_S = 0.5$ V, and we can neglect the larger root because it would make the MOSFET sub-threshold. So, we know that $V_{GS} = -0.5$ V, and in order for this solution to be valid (i.e. for the active assumption to be correct), we require $V_{DS} \geq V_{GS} - V_t = 0.5$ V. The minimum supply voltage for active mode is therefore $V_S + V_{DSmin} = 0.5 + 0.5 =$ **1.0 V**.
(Alternatively, and more easily: active mode requires $V_{GD} \leq V_t$, which in this case is equivalent to $V_{DD} \geq -V_t = 1$ V.) [4]

e) Initial condition (at $t = 0^-$): The circuit will have reached steady state, with no current in the capacitor. The transistors have the same β value, but the lower transistor has twice the base current of the upper one, so the lower transistor will be saturated and the output voltage will be $V_{CEsat} \sim 0.2$ V.

When the input voltage goes to zero, the lower transistor will switch off, and the capacitor will start to charge via the upper transistor. The charging current will be $I = \beta I_B = 100 \times (4.3/20k) = 21.5$ mA, and the voltage gradient at the output will be $I/C = 21{,}500$ V/sec. The output voltage will rise linearly until the upper transistor saturates, at which point it will level out at ~ 4.8 V. This will occur after $4.6/21500 = 214$ μs.

When the input goes high again, the capacitor will start to discharge, and once the upper transistor comes out of saturation, the net current in the capacitor will be equal and opposite to its earlier value (because lower I_C is 2× upper). The second ramp will therefore have the same duration as the first. So: **both ramps are 214 μs in duration**. [8]

f) To find the frequency of stable oscillation, we look for roots of the characteristic equation for which s is purely imaginary, i.e. roots with $s = j\omega$, ω being the frequency of oscillation. Substituting this form of s into the c.e. we obtain:

$$-j(1+K)(\omega RC)^3 - 6(\omega RC)^2 + 5j(\omega RC) + 1 = 0$$

.Considering just the real part of this equation, we see that $6(\omega RC)^2 = 1$ or $\omega =$ **$1/(\sqrt{6}RC)$.** [6]

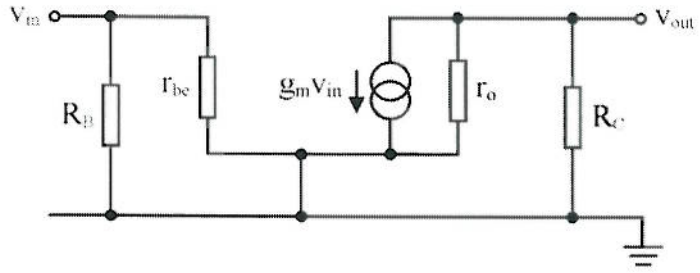
Question 2

a) Considering the output side, we have $V_{OUT} = V_{CC} - I_C R_C$. With $V_{CC} = 10$ V, $V_{OUT} = 5$ V and $I_C = 0.5$ mA, this gives $R_C = (V_{CC} - V_{OUT})/I_C = 10$ kΩ. [3]

The required base current is $I_B = I_C/\beta = 2.5$ μA $= (V_{CC} - V_{BE})/R_B$. Putting $V_{CC} = 10$ V, and assuming $V_{BE} \sim 0.7$ V, this gives $I_B = 9.3/2.5\mu = 3.72$ MΩ. [3]

The bias stability is not great because the base current is fixed and so variations in β will produce corresponding variations in I_C and hence the operating point. The bias stability can be improved by introducing some feedback, for example by connecting the top end of R_B to the output rather than to V_{CC}. [2]

b) SSEC:



$g_m = I_C/V_T = 0.5\text{m}/25\text{m} = 20$ mS

$r_{be} = \beta/g_m = 200/0.02 = 10$ kΩ

$r_o = V_A/I_C = 100/0.5\text{m} = 200$ kΩ

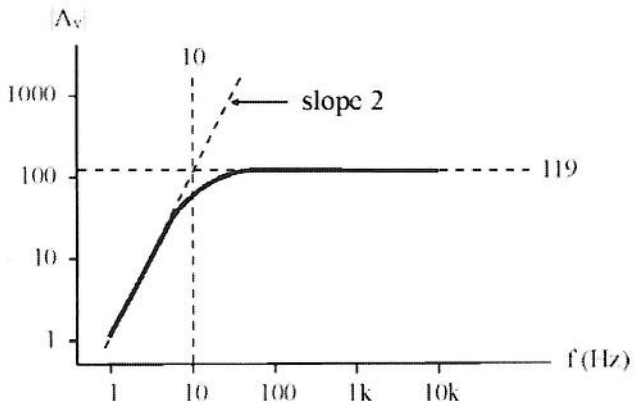
[6]

Macromodel parameters, by inspection of SSEC:
$R_i = R_B//r_{be} = 3.72\text{M}//10\text{k} = 9.97$ kΩ
$R_o = R_C//r_o = 10\text{k}//200\text{k} = 9.52$ kΩ
$A_v = -g_m R_o = -0.02 \times 9.52\text{k} = -190$ [6]

c) In the mid-band, the capacitors will be effectively short-circuit, and the overall in-circuit gain will be:

$$\frac{v_L}{v_S} = \frac{9.97}{9.97+5} \cdot (-190) \cdot \frac{150}{150+9.52} = -119$$ [4]

The cut-off frequencies associated with the coupling capacitors at the input and output are: $f_{in} = [2\pi\times(5\text{k} + 9.97\text{k})\times 1\mu] = 10.6$ Hz and $f_{out} = [2\pi\times(150\text{k} + 9.52\text{k})\times 100\text{n}] = 10$ Hz. The Bode plot is therefore that of a 2nd order high-pass filter with a ~10 Hz cut-off: [2]



[4]

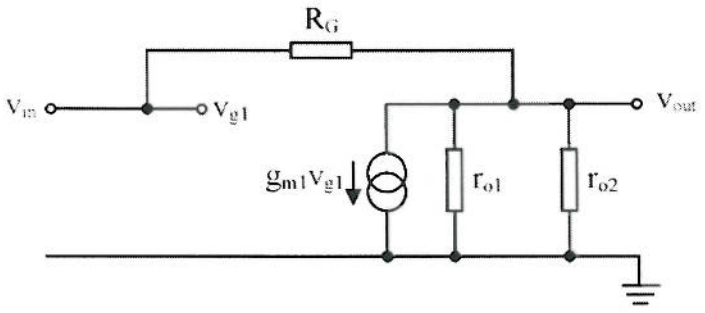
Question 3

a) Let the lower MOSFET be Q1, and the upper Q2. Assuming that the upper device is active (we are told this), its drain current is given by: $I_D = K_2(V_G - V_{DD} - V_{t2})^2$. Rearranging gives $V_G = V_{DD} + V_{t2} \pm\sqrt{(I_D/K_2)}$. Putting $V_{DD} = 10$ V, $V_{t2} = -1$ V, $I_D = 0.4$ mA, $K_2 = 100\ \mu A/V^2$, and taking the negative sign to ensure the (p-channel) device is above threshold, we obtain: $\mathbf{V_G = 10 - 1 - 2 = 7\ V}$. [3]

The 10 MΩ feedback resistor forces Q1 to have $V_G = V_D$ under quiescent conditions, and it follows that the device is active. The drain current is the same as that of Q2, so we can write: $I_D = K_1(V_{OUT} - V_{t1})^2$. Rearranging, and this time taking the positive root to ensure the (n-channel) device is above threshold, gives: $V_{OUT} = V_{t1} + \sqrt{(I_D/K_1)}$. Putting $V_{t1} = 1$ V, $I_D = 0.4$ mA, $K_1 = 400\ \mu A/V^2$ gives $\mathbf{V_{OUT} = 1 + 1 = 2\ V}$. [3]

As noted above, Q1 has $V_{GD} = 0$, so **$V_D > V_G - V_t$ which implies active mode for n-channel device**. Considering Q2, we have $V_D = 2$ V, and $V_G = 7$ V, so **$V_D < V_G - V_t$ which implies active mode for p-channel device.** [2]

b) SSEC:



$R_G = 10$ MΩ

$g_{m1} = 2\sqrt{(K_1 I_D)} = 0.8$ mS

$r_{o1} = r_{o2} = V_A/I_D = 250$ kΩ

[6]

KCL at the output node gives: $g_{m1}v_{in} + v_{out}/r_{o1} + v_{out}/r_{o2} + (v_{out} - v_{in})/R_G = 0$. Rearranging, the voltage gain is obtained as:

$$\mathbf{A_v} = v_{out}/v_{in} = -(g_{m1} - 1/R_G)(r_{o1}//r_{o2}//R_G) = \mathbf{-98.8}$$ [3]

The input current is $i_{in} = (v_{in} - v_{out})/R_G = v_{in}(1 - A_v)/R_G$, so the input resistance is:

$$\mathbf{R_i} = v_{in}/i_{in} = R_G/(1 - A_v) = 10M/99.8 = \mathbf{100.2\ k\Omega}$$ [3]

c) Q2 will remain active provided $V_{OUT} \le V_G - V_{t2} = 8$ V. Q1 will remain active while $V_{OUT} \ge V_{G1} - V_{t1}$. If we ignore the change in V_{G1} due the input signal (reasonable since the gain is quite high), then we can use the quiescent value of V_{G1}, giving $V_{OUT} \ge 1$ V. So, the approximate range of V_{OUT} over which both transistors remain active is $\mathbf{1\ V \le V_{OUT} \le 8\ V}$. [4]

The middle of the range is $V_{OUT} = 4.5$ V, and we can arrange for this to be the quiescent output voltage simply by adding a resistor R from the gate of Q1 to ground, to form a potential divider with R_G. We still need 2 V at the gate of Q1, so the value required is obtained from the potential divider equation as:

$$R/(R + 10M) = 2/4.5 \quad \Rightarrow \quad R = 10M/(4.5/2 - 1) = \mathbf{8\ M\Omega}$$ [6]