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IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2003

MSc and EEE PART IV: M.Eng. and ACGI

CURRENT-MODE ANALOGUE SIGNAL PROCESSING

Wednesday, 14 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

Corrected Copy

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : E. Drakakis
Second Marker(s) : C. Papavassiliou

Special Information for Invigilators: none

Information for candidates

Some notation

$\frac{W}{L}$ denotes the width over the length of a MOS transistor

The symbol " // " means "in parallel with"; for example $R_1 // R_2$ means "R_1 in parallel with R_2"

The Questions

1. (a) Explain the reasons why the switched-current circuit design technique constitutes an attractive alternative compared to the conventional switched-capacitor technique. **[7]**

(b) Figure 1.1 illustrates a switched-current circuit. Show that its z-domain current transfer function corresponds to an inverting lossy integrator and derive an expression for its time-constant when $\omega T << 1$ (T denotes the clock period). You may assume that the switches are ideal and that the transistors' sizing are as follows: $\left(\frac{W}{L}\right)_{M_1} = \left(\frac{W}{L}\right)_{M_2}$, $\left(\frac{W}{L}\right)_{M_4} = b_4\left(\frac{W}{L}\right)_{M_1}$ and $\left(\frac{W}{L}\right)_{M_3} = b_3\left(\frac{W}{L}\right)_{M_1}$. **[13]**

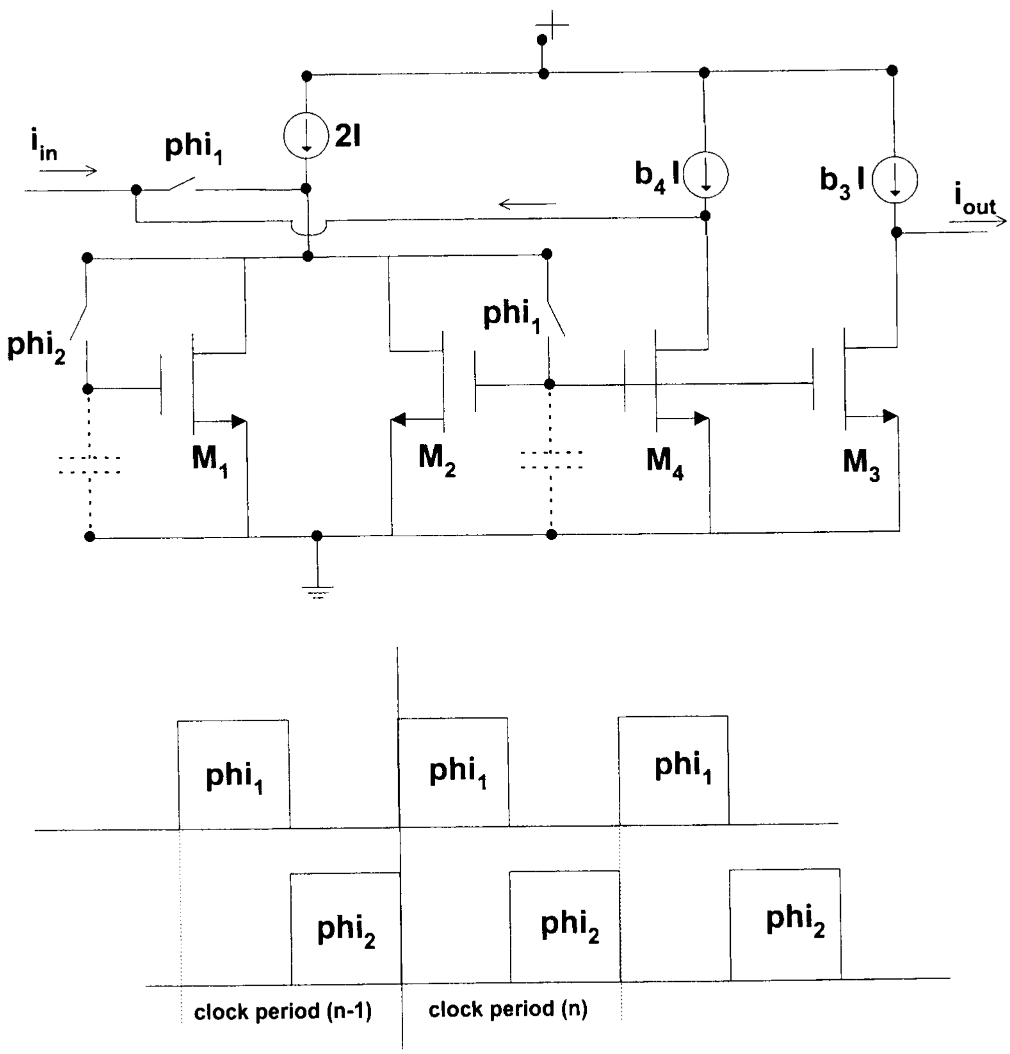

Figure 1.1

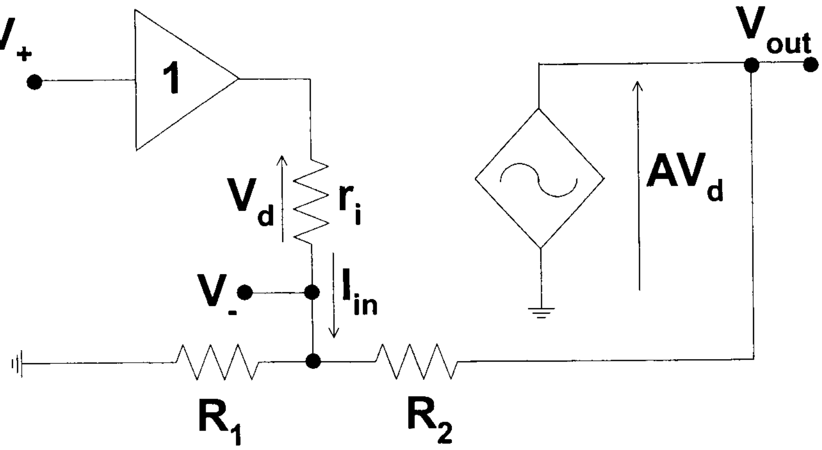

Figure 2.1

2. (a) Figure 2.1 above illustrates the equivalent circuit of a current-feedback operational amplifier (CFOA) connected in a non-inverting amplifier configuration. By means of analytical calculations show that the closed-loop bandwidth can be set independently of the closed-loop gain when

$A = A_0 \Big/ \left(1 + j\dfrac{f}{f_0} \right)$. You may assume that $1 + \dfrac{R_2}{R_1} = G$. **[12]**

(b) With respect to figure 2.1 show how the closed-loop transfer function V_{out} / V_{in} can be expressed in terms of an open-loop transimpedance gain Z_t and calculate the closed-loop bandwidth when

$Z_t = R_0 // \dfrac{1}{j\, C_0 \omega}$. **[4]**

(c) Figure 2.2 illustrates a typical CFOA. Draw a new CFOA with an input buffer stage of reduced offset voltage. Explain how the offset voltage is reduced and briefly discuss relevant design trade-offs. **[4]**

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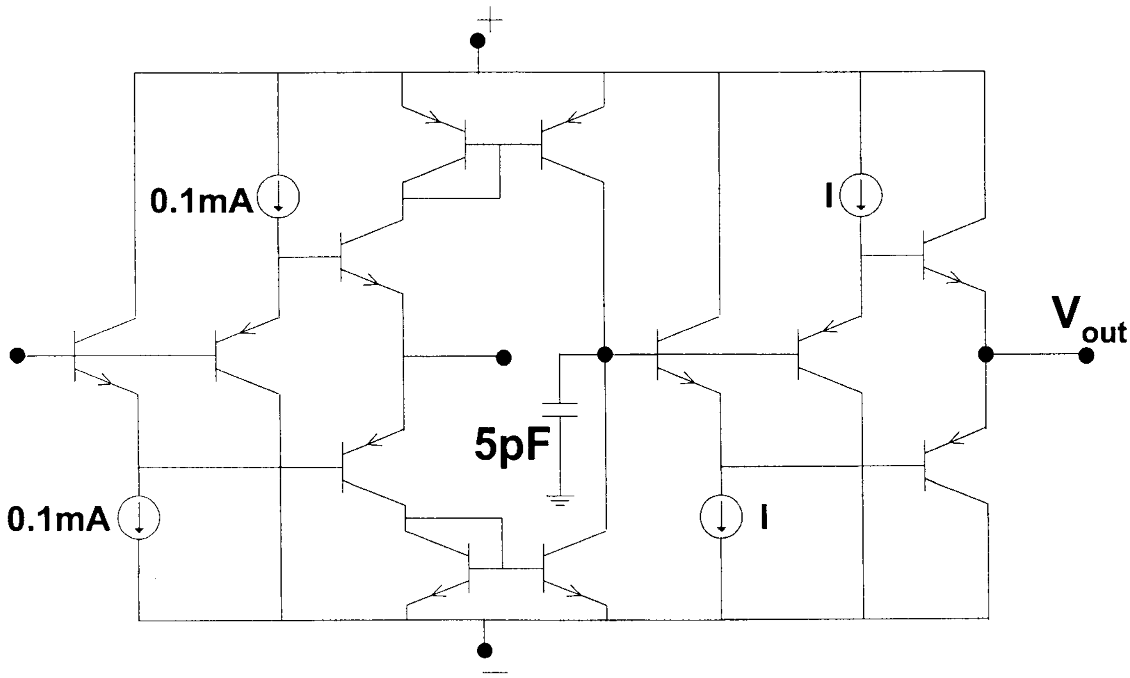

Figure 2.2

3. (a) Figure 3.1 illustrates a single op-amp-based amplifier.

   (i) Show that the output voltage can be expressed as $V_{out} = K_2V_2 - K_1V_1$ with the quantities K_2 and K_1 dependent upon R_1, R_2, R_3 and R_4 and find the appropriate condition so that the op-amp realises a difference amplifier. **[5]**

   (ii) Express the CMRR in terms of the resistors R_1, R_2, R_3 and R_4 and discuss the limitations caused by finite resistor tolerances. **[5]**

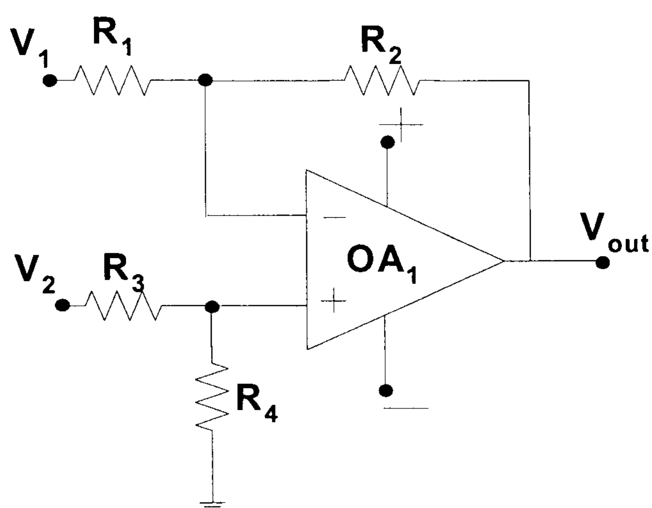

Figure 3.1

Question continued on the next page…

(b) Figure 3.2 illustrates a current-mode instrumentation amplifier. Discuss the operation of the circuit for both differential and common-mode inputs. What is the main advantage of the circuit when compared to the 3-op-amp instrumentation amplifier? What limits its accuracy and its CMRR performance? **[10]**

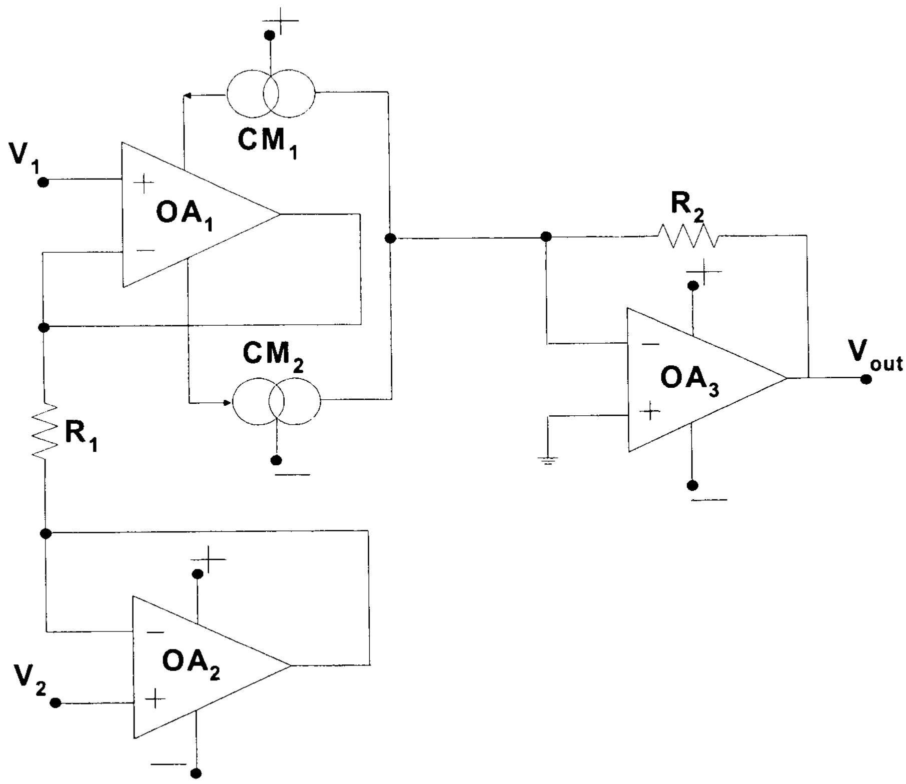

Figure 3.2

4. (a) Derive the bipolar translinear principle with reference to a loop containing 2m base-emitter junctions. State all the assumptions that you make and list the conditions which must be satisfied in order for this principle to be valid. **[5]**

Question continued on the next page...

(b) Figure 4.1 illustrates a translinear circuit whose differential current output realises a trigonometric approximation.

(i) Express the currents I_3 and I_4 in terms of I and I_x. **[3]**

(ii) Next, express the differential output $I_2 - I_1$ in terms of I and I_x and show that when $I_x = yI$ holds: $I_2 - I_1 = I\,\dfrac{y - y^3}{1 + y^2}$. You may assume that the transistors' beta value is large. **[4]**

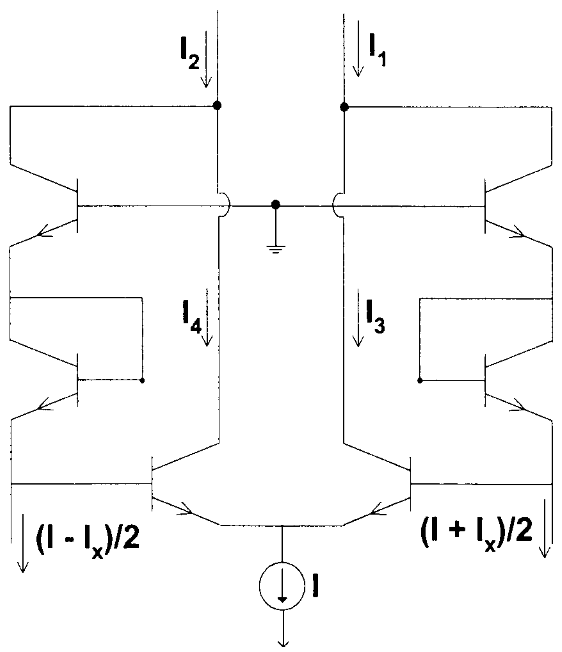

Figure 4.1

(c) Figure 4.2 illustrates a translinear circuit whose output current I_z can implement a variety of trigonometric approximations.

(i) Express the current I_2 in terms of I, I_x and the output current I_z. **[2]**

(ii) Next, express the output current I_z in terms of I, I_x and the emitter area A. **[3]**

(iii) Determine the emitter area A so that $I_z = 1.54\,I_x - 0.54\,\dfrac{I_x^{\,3}}{I^2}$. **[3]**

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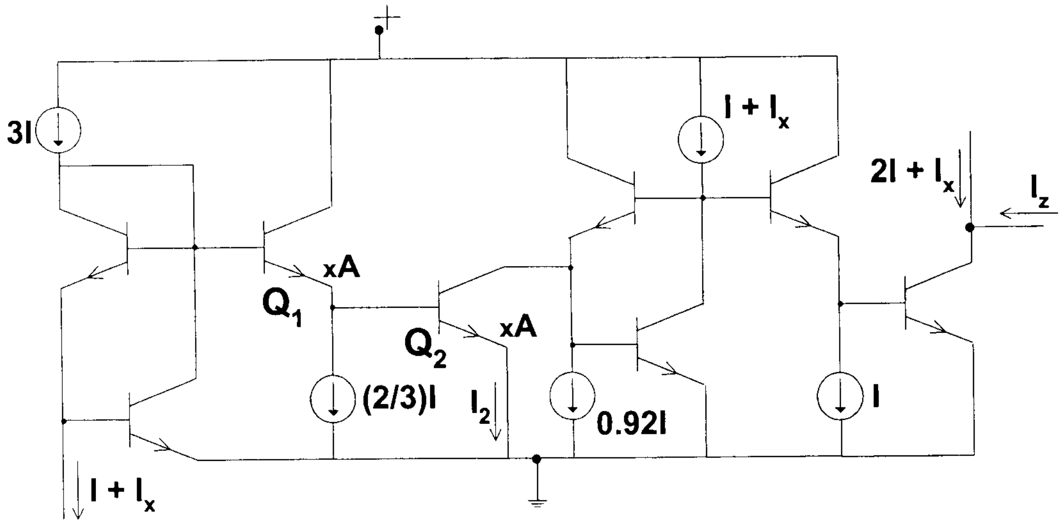

Figure 4.2

5. The transfer function for a second order topology has been decomposed into the following state-space equations:

$$\dot{x}_1 = -\left(\frac{\omega_0}{Q}\right)x_1 + \omega_0 x_2$$
$$\dot{x}_2 = -\omega_0 x_1 + \omega_0 u$$
$$y_1 = x_1$$
$$y_2 = x_2$$

where y_1 and y_2 are outputs, x_1 and x_2 are state-variables and u is the input (a dot above a variable denotes time-differentiation).

(a) Show that the output y_1 can be used to implement a second order lowpass transfer function whereas the output y_2 can be used for the implementation of a "two-pole one-zero" second order transfer function. **[4]**

Question continued on the next page…

(b) Using the exponential mappings $x_j = I_0\, exp\left(\frac{V_j}{V_T}\right)(j = 1,2)$ and

$u = I_S\, exp\left(\frac{V_u}{V_T}\right)$ show that the above linear state-space equations can be

transformed into non-linear log-domain design equations. **[7]**

(c) From these design equations sketch a transistor-level implementation of a log-domain topology which realises the two transfer functions (the lowpass and the "two-pole one-zero" ones). Assuming that all capacitors are equal to 20pF determine the dc current bias values I_0 so that $\omega_0 = 4$MHz. You may assume that $V_T \cong 26$mV. **[9]**

6. (a) State the relation which must be satisfied by two N-port networks, if these two networks are to be considered adjoint networks. Exploiting this relation derive the adjoint network of a resistor, a nullor and an open-loop "ideal" voltage amplifier. **[4]**

(b) Figure 6.1 illustrates a voltage-mode Tow-Thomas biquad implemented by means of voltage op-amps. Derive its current-mode equivalent. **[3]**

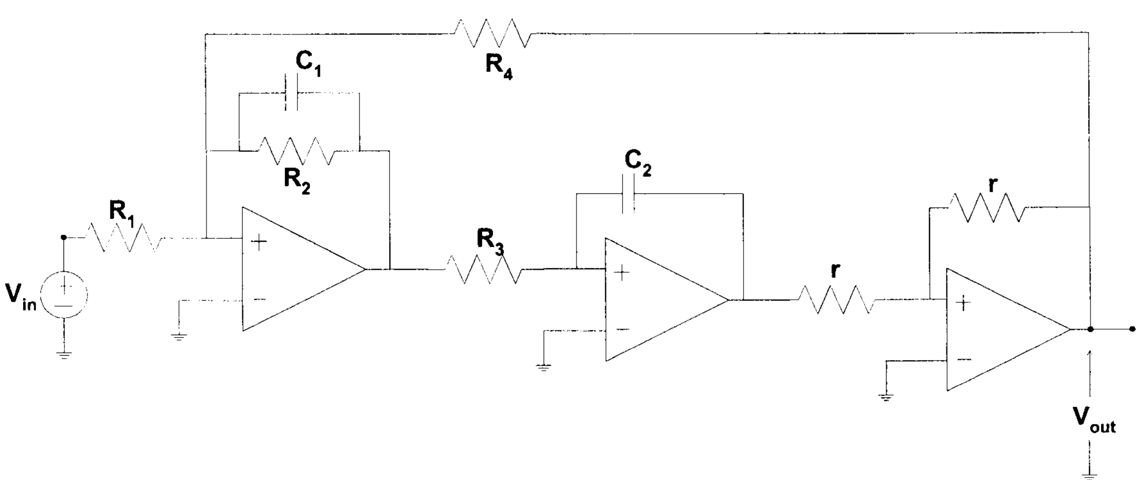

Figure 6.1

Question continued on the next page...

(c) You are asked to implement an I-I converter. What kind of amplifier would you choose to use if:

(i) high-gain ideal amplifiers of any of the four kinds were available to you. **[1]**

(ii) only practical amplifiers were available to you. **[1]**

(iii) if high-performance current-followers and voltage-followers were available to you. **[1]**

(d) Figure 6.2 shows a log-domain filter.

(i) Express the capacitor current in terms of I_{out1} and its derivatives.

(ii) Express the current u in terms of I_{out1} and known circuit parameters.

(iii) Exploiting the translinear principle determine the s-domain transfer function $\frac{I_{out2}(s)}{I_{in}(s)}$. When $I_d = 10\ \mu A$ determine the dc biasing current I_0 and the capacitor value C so that the filter has a low-frequency gain of 1 and a pole frequency of 1MHz. You may assume that $V_T \cong 26mV$ and that beta-induced errors are negligible. **[10]**

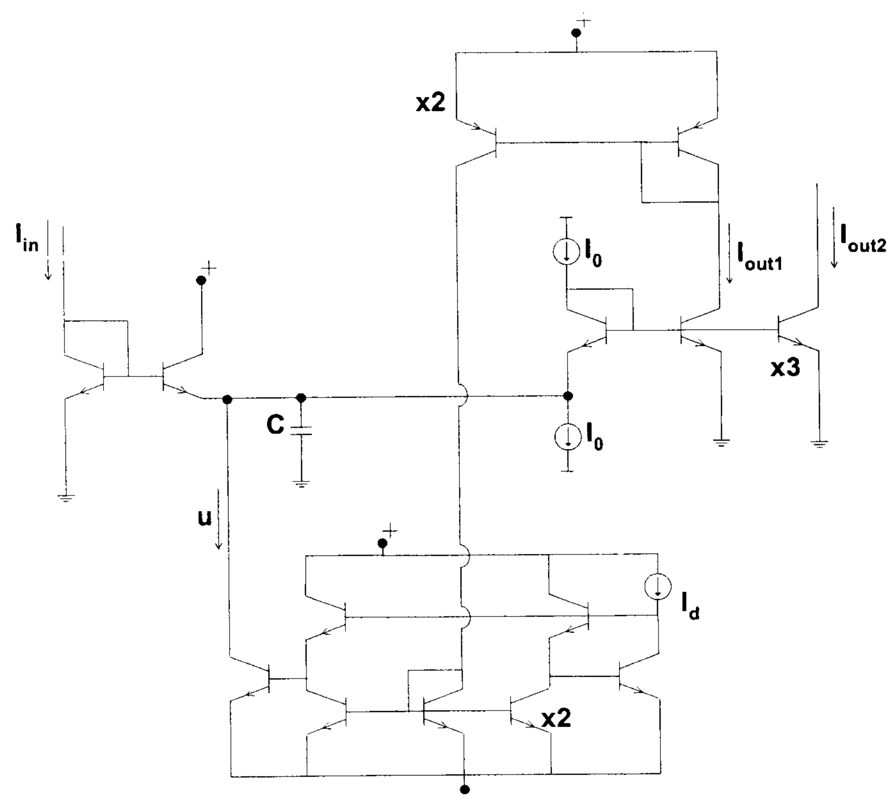

Figure 6.2