EE1-04

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2015

EEE PART I: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 1

Corrected Copy

Wednesday, 10 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : A.S. Holmes
Second Marker(s) : C. Papavassiliou

The Questions

1. For each part of this question, state clearly any assumptions made in your calculations.

   a) Calculate the collector current of the transistor in Figure 1.1, and explain briefly why the resistor in the emitter helps to stabilize this current.

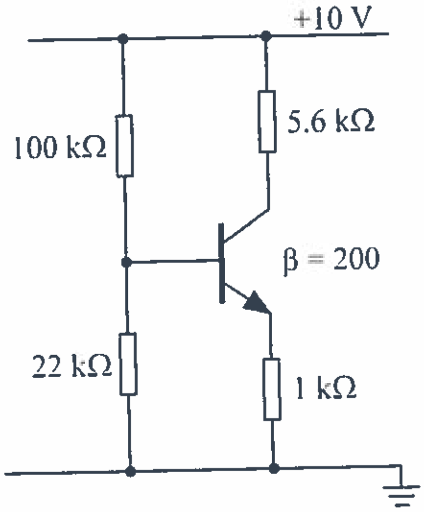

Figure 1.1 [8]

   b) Determine the operating modes of both MOSFETs in Figure 1.2, and calculate the value of the voltage V.

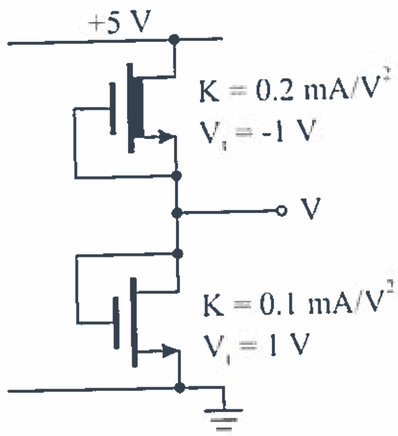

Figure 1.2 [6]

   c) Sketch the circuit for a Widlar current sink, and derive a large-signal relationship between the input and output currents. In your derivation you should ignore base currents and assume the transistors are matched. [8]

Question 1 continues on the next page...

Question 1 continued

d) Figure 1.3 shows a Darlington pair compound transistor in which an emitter resistor is used to set the relative magnitudes of the bias currents in Q1 and Q2. Making use of the resistance reflection rule, or otherwise, derive an expression for the small-signal input resistance between base and emitter of the compound device, expressing your answer in terms of R_E and the small-signal parameters of the individual transistors.

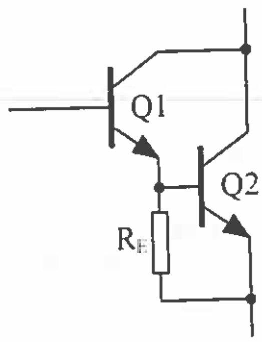

Figure 1.3

[6]

e) Figure 1.4 shows a single-transistor monostable circuit. If the voltage V_{IN} changes suddenly from +5 V to 0 V at time t = 0, after having been held at +5 V for a long time, calculate the duration T of the resulting output pulse.

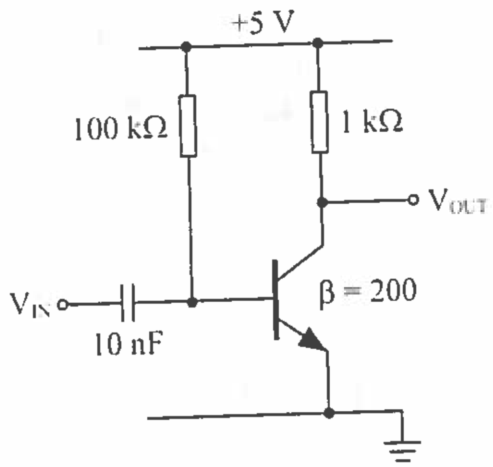

Figure 1.4

[8]

f) Name the essential circuit blocks in a sinusoidal oscillator. What conditions must be satisfied in order for such a circuit to generate sinusoidal oscillations of stable amplitude? [4]

2. Figure 2.1 shows a differential amplifier in which all four transistors are matched and have $\beta = 100$. In parts a) and b) you may assume the transistors have infinite output resistance.

a) Determine the value of the tail current, I, and hence calculate the quiescent output voltage when $V_{IN1} = V_{IN2}$ and all transistors are active. [8]

b) Draw a small-signal equivalent circuit and, by considering the response to a purely differential input signal, $v_d = (v_{in1} - v_{in2})$, derive an expression for the single-ended differential voltage gain. [10]

Also calculate the small-signal input and output resistances and hence draw a macromodel of the amplifier, assigning values to the elements. [7]

c) If the transistors have an Early voltage of 120 V, calculate the common-mode gain of the amplifier, and hence its common-mode rejection ratio. You may neglect the output resistances of Q1 and Q2 when evaluating the common-mode gain. [5]

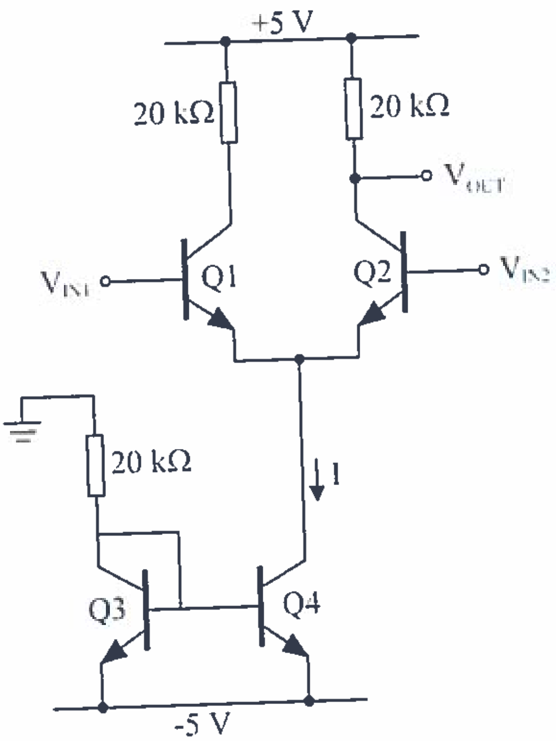

Figure 2.1

3\. a) Figure 3.1 shows a source follower, i.e. the MOSFET equivalent of an emitter follower. Using small-signal analysis show that, if the transistor's output resistance is ignored, the small-signal voltage gain and output resistance of the circuit can be written as:

$$A_v = \frac{R_S}{R_S + 1/g_m} \quad ; \quad R_o = R_S // (1/g_m) \qquad [10]$$

b) In Figure 3.2, a source follower is used to buffer the output of a common-source amplifier, so as to achieve both high gain and low output impedance. The transistor Q1 has $K = 0.25\ \text{mA/V}^2$ and $V_t = 1$ V, while Q2 has $K = 1.5\ \text{mA/V}^2$ and $V_t = 1$ V.

i) Explain the role of the 10 MΩ resistor and calculate the quiescent voltage at the output. Also determine the bias current in Q2 and the quiescent voltage at node X, assuming Q2 is active. [8]

ii) Draw a small-signal equivalent circuit of the common-source section (from the input to node X) and evaluate the mid-band small-signal voltage gain to node X if Q1 has $V_A = 100$ V. [8]

iii) Calculate the overall mid-band voltage gain and the output resistance of the amplifier. [4]

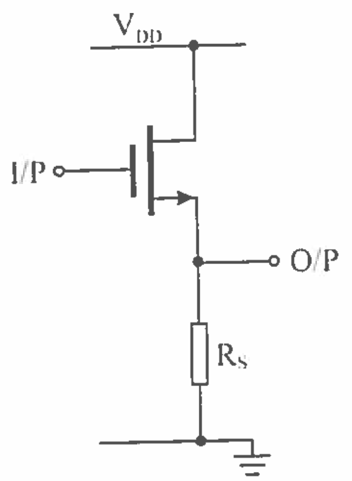

Figure 3.1

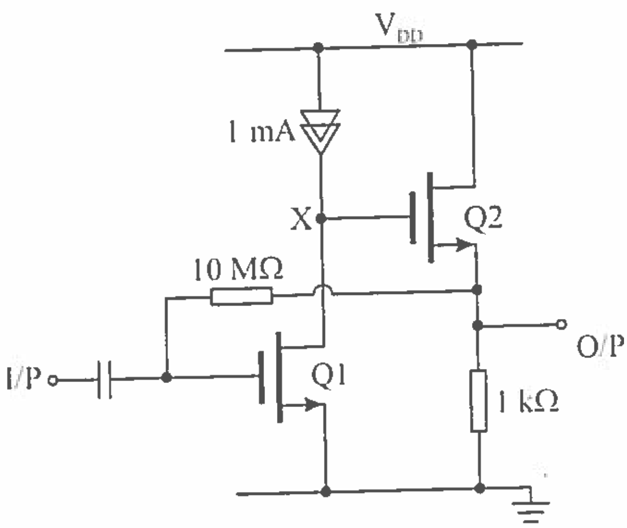

Figure 3.2