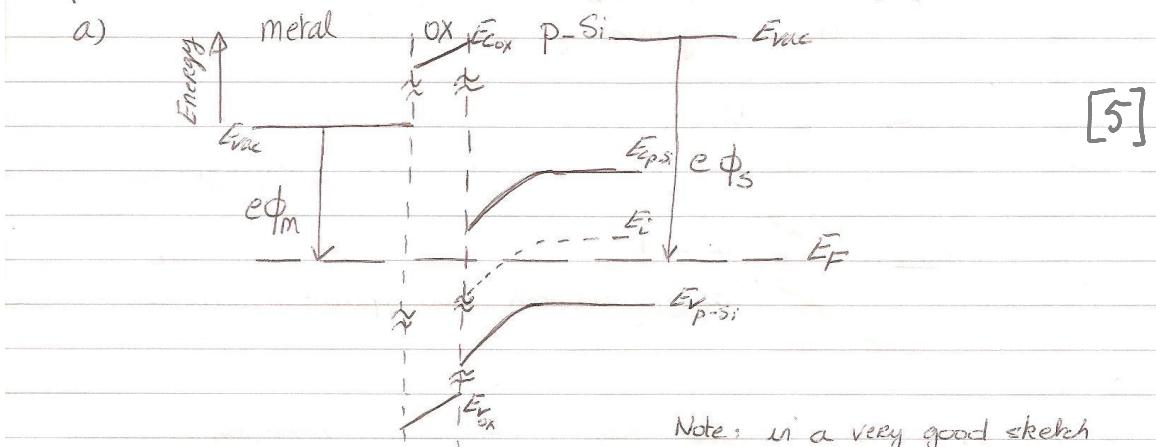


Comments to student performance in blue.

(1)

Q1

a)



(2)

$$V_s = 2\phi_F \Rightarrow n_s = N_A \exp(\phi) = N_A \quad \text{iii) [1]}$$

[1] (ii) is the definition of threshold

$$\Rightarrow V_s < 2\phi_F \quad \text{weak inversion.}$$

$$V_s > 2\phi_F \quad \text{moderate inversion.}$$

Note: both  $V_s = \phi_F$  &  $V_s = 2\phi_F$  define the boundary between two operation regimes.

Comment: bookwork

c) ideal long channel MOSFET in strong inversion

$$I_{DS} = \frac{\mu C_{ox} W}{2} \left( (V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$\text{linear region: } I_{DS} = \frac{\mu C_{ox} W}{2} (V_{GS} - V_{th}) V_{DS}$$

$$\text{threshold } V_{GS} = V_{th} \Rightarrow I_{DS} = 0$$

in  $I_{DS}$  equation:

$$0 = 8.85 \cdot 10^{-13} V_{th} - 4.425 \cdot 10^{-13}$$

$$V_{th} = \frac{4.425}{8.85} V = 0.5 V \quad [2]$$

$$\text{saturation } I_{DS} = \frac{\mu C_{ox} W}{2L} (V_{GS} - V_{th})^2 = K V_{GS}^2 - 2K V_{th} V_{GS} + V_{th}^2$$

$$\text{threshold } V_{GS} = V_{th} \Rightarrow I_{DS} = 0$$

In  $I_{DS}$  equation:

$$0 = 4.425 \cdot 10^{-11} V_{th}^2 - \frac{3.9825}{2.655} \cdot 10^{-11} V_{th} + \frac{8.960625}{2.9885} \cdot 10^{-12}$$

$$0 = 4.425 V_{th}^2 - 3.988 V_{th} + 0.8960625$$

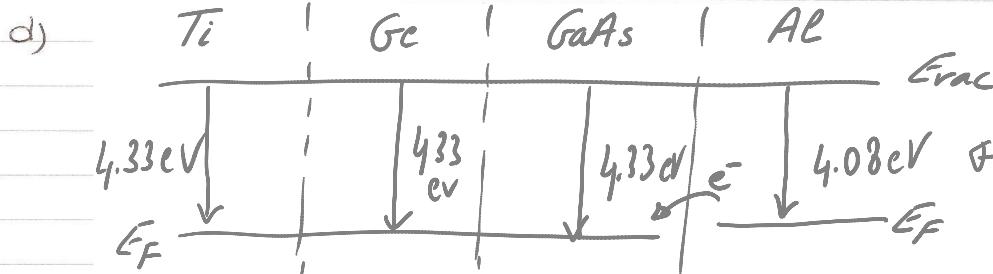
$$V_{th} = \frac{+3.9825 \pm \sqrt{(3.9825)^2 - 4 \times 4.425 \times 0.8960625}}{2 \times 4.425} \\ = 0.45 V \quad [2]$$

Comment: this was easy once  
 $\begin{cases} 1: \text{correct formulae for } I_{DS}^{\text{lin}} \& I_{DS}^{\text{sat}} \text{ were written} \\ 2: \text{factor in front of } V_{GS} \text{ resp } V_{GS}^2 \text{ is divided away.} \end{cases}$

(3)

$$DIBL = \left| \frac{V_{th}^{ein} - V_{th}^{sat}}{V_{DS}^{ein} - V_{DS}^{sat}} \right| = \frac{0.5 - 0.45}{0.01 - 1} = 0.051 \frac{V}{V} [1]$$

$$= 51 \frac{mV}{V}$$



$E_G^{Ge} = 0.66 \text{ eV}$

$\Delta E_C = 4 - 4.1 = 0.1 \text{ eV}$

$E_G^{GaAs} = 1.42 \text{ eV}$

$\Delta E_V = \Delta E_G - \Delta E_V = 0.66 \text{ eV}$

$E_C = E_G + \Delta E_C$

$E_V = E_G - \Delta E_V$

$E_C = 4.08 \text{ eV} + 0.1 \text{ eV} = 4.18 \text{ eV}$

$E_V = 4.08 \text{ eV} - 0.66 \text{ eV} = 3.42 \text{ eV}$

$\Delta E_C = 0.95 \text{ eV}$

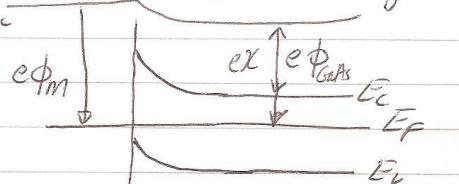
Comment: most errors happen @\*. Since  $\phi_{Ge} = \phi_{GaAs}$   $\Rightarrow$  no band bending but since  $\chi_{Ge} < \chi_{GaAs}$   $\Delta E_C \neq 0$  &  $E_C^{GaAs}$  lower than  $E_C^{Ge}$ .

e) i)  $\mu_1 = \mu_2 < \mu_3$  OR  $\mu_3 > \mu_2 = \mu_1$  [3]

ii)  $N_{sat_2} < N_{sat_3} < N_{sat_1}$  OR  $N_{sat_1} > N_{sat_3} > N_{sat_2}$  slope @ low electric field is the same.

N saturation @ high electric fields only.

f) n-type MESFET needs Schottky contact.



$\phi_{Ge} < \phi_m$  for Schottky contact.

[5]

$$\phi_{Ge} = \chi_{Ge} + \frac{(E_C - E_F)}{C}$$

$N_D = 10^{15} \text{ cm}^{-3} \rightarrow \text{very low}$

(4)

$$\phi_{GATs} = 4.1 \text{ eV} + 0.156 \text{ eV} \approx 4.26 \text{ eV}$$

$$m = N_c \exp\left(\frac{-(E_c - E_F)}{kT}\right)$$

$$E_c - E_F = kT \ln\left(\frac{N_c}{n}\right)$$

$$= 0.026 \ln\left(\frac{4.7 \cdot 10^{17}}{10^{15}}\right) = 0.156 \text{ eV}$$

$N_i$  will be the best theoretical choice because this gives the largest  $V_{bi} = \phi_m - \phi_{GATs}$ .

Comment: asked was: "the best", this means that only  $N_i$  is ok.

g)  $I_{G0}^{\text{MOSFET}} > I_{G0}^{\text{JFET}}$

The gate of a MESFET is determined by a Schottky barrier, that of a JFET by a pn-junction.

The leakage current through the gate is related to this barrier height.

[5]

Due to interface charges & traps in a metal/semiconductor contact the barrier height in a MESFET is lower than in a JFET.

$$\Rightarrow I_{G0}^{\text{MOSFET}} > I_{G0}^{\text{JFET}}$$

Comment: the important info here is the magnitude of the barrier height and the fact that MESFET gates suffer from interface states which causes the barrier [1] to remain low whatever the chosen metal.

- a) i) fin FET  
 ii) a) gate  
 b) buried oxide layer  
 c) gate oxide.  
 d) Si substrate.

[4]

To bookwork

it is important to distinguish "oxide" in b) & c)

(5)

(2) a) Small drain voltage = linear (triode) region

[8]

$W_{\max}$  = maximum depletion width from gate = @ threshold  
 $\rightarrow W_{\max} = W_{\text{depl}} (V_s = 2\phi_F)$

formulae sheet:

$$* W_{\text{depl}} = \sqrt{\frac{2\epsilon_0\epsilon_s (V_{bi} - V)}{e N_A}} \quad \text{for 1-sided junction}$$

Comment:  
main error occurs with the choice of  $V$ .  
 $V = -V_s$ , the surface potential only.  $V_{th}$  includes  $V_{ox}$ !  
Since  $V_s = 2\phi_F$  @  $W_{\text{depl max}}$   
 $V_{th}$  is not needed.

$$W_{\max} = \sqrt{\frac{2\epsilon_0\epsilon_s 2 \frac{kT}{e} \ln\left(\frac{N_A}{n_i}\right)}{e N_A}}$$

$$W_{\max} = \sqrt{\frac{4 \times 8.85 \cdot 10^{-14} \text{ F/cm}^2 \cdot 0.026 \cdot \ln\left(\frac{10^{16}}{1.45 \cdot 10^{10}}\right)}{1.6 \cdot 10^{-19} \text{ C} \cdot 10^{16} \text{ cm}^{-3}}} = 3.05 \cdot 10^{-5} \text{ cm}$$

\*  $W_{DB} = \sqrt{\frac{2\epsilon_0\epsilon_s (V_{bi} + 0.94)}{e N_A}}$  assume depletion region extends in the lowest doping side only.

Comment:  
the value  $\epsilon_0$  is given in  $F/m$  in formulae sheet but doping densities are in  $\text{cm}^{-3}$   
 $\Rightarrow$  many unit errors

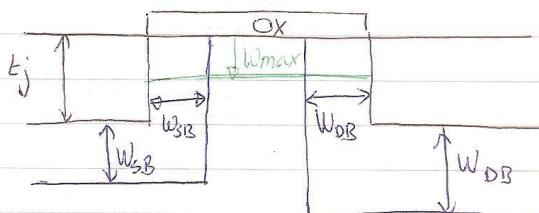
$$V_{bi} = \frac{kT}{e} \ln\left(\frac{N_A N_D}{n_i^2}\right) = 0.026 \ln\left(\frac{10^{16} \cdot 10^{20}}{(1.45 \cdot 10^{10})^2}\right) = 0.94 \text{ eV}$$

$$W_{DB} = \sqrt{\frac{2 \cdot 8.85 \cdot 10^{-14} \cdot 12 \cdot (0.94 + 0.26)}{1.6 \cdot 10^{-19} \cdot 10^{16}}} = 3.99 \cdot 10^{-5} \text{ cm}$$

\*  $W_{SB}$  & same assumption as for  $W_{DB}$  and  $V_s = 0 \text{ V}$

$$W_{SB} = \sqrt{\frac{2 \times 8.85 \cdot 10^{-14} \cdot 12 \cdot 0.94}{1.6 \cdot 10^{-19} \cdot 10^{16}}} = 3.53 \cdot 10^{-5} \text{ cm}$$

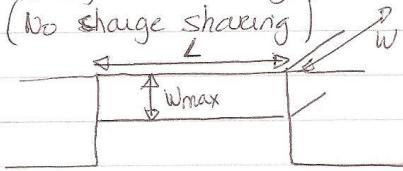
b)



[4]

(6)

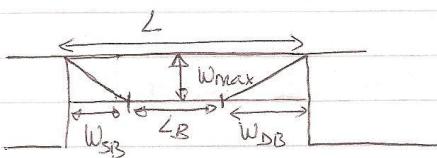
c)  $Q_G$  (No charge sharing) Charge controlled by gate when



[8]

$$Q_G = -\frac{e N_A W_{max} L W}{LW} : \text{(charge per gate area)}$$

$Q_{GCS}$  (charge controlled by gate with charge sharing)



$$\text{area trapezium: } \left( \frac{L + L_B}{2} \right) \cdot W_{max}$$

$$\begin{aligned} Q_{GCS} &= -\frac{e N_A W_{max}}{LW} \left( \frac{L + L_B}{2} \right) W \\ &= -\frac{e N_A W_{max}}{LW} \left( \frac{L + (L - W_{SB} - W_{DB})}{2} W \right) \end{aligned}$$

charge per gate area.

$$\text{charge lost: } \Delta Q = Q_G - Q_{GCS}$$

$$\begin{aligned} &= -\frac{e N_A W_{max} W}{LW} \left( L - \left( \frac{2L - W_{SB} - W_{DB}}{2} \right) \right) \\ &= -\frac{e N_A W_{max} W}{LW} \left( \frac{2L - 2L + W_{SB} + W_{DB}}{2} \right) \\ &= -\frac{e N_A W_{max} W}{LW} \left( \frac{W_{SB} + W_{DB}}{2} \right) \end{aligned}$$

$$\Delta V_{th} = -\frac{e N_A W_{max}}{2 C_{ox} L} (W_{SB} + W_{DB})$$

Note : signs are important because :

1° charge is negative

2°  $V_{th}$  decreases (threshold voltage roll off)

Comment: depletion widths often not drawn consistent with doping density.  
thus junctions & depletion width edges should be given in answer.

Ohmic contact!

(7)

3. a)

m

p<sup>+</sup>

n

p

Comment: This is a JFET  $\Rightarrow$  the m-p<sup>+</sup> junction should be Ohmic!! thus or flat band or accumulation of majority carriers.

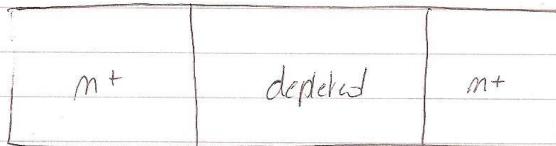
E<sub>c</sub>

E<sub>F</sub>

E<sub>V</sub>

[5]

b)

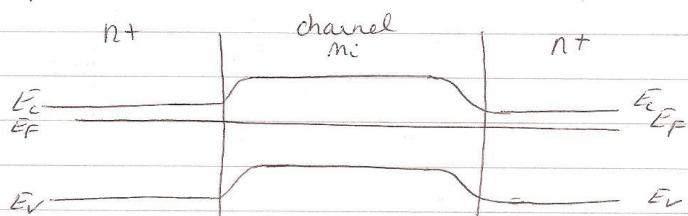


depletion width must extend in the lowest doped region.

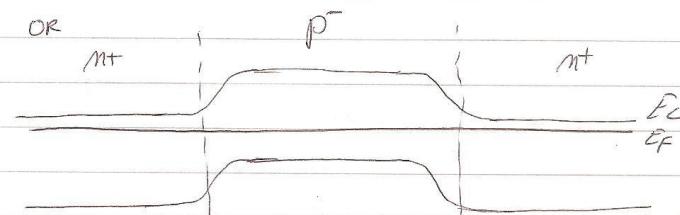
[5]

Note, in the MOSFET part of the course, we have seen that depleted means that the electron concentration  $\leq n_i$

$\Rightarrow$  possibilities



OR



\* p<sup>+</sup> in channel region is not acceptable because that would require too high a V<sub>GS</sub>. What is acceptable are plots of n+ n n<sub>i</sub> m m<sup>+</sup> or n<sup>+</sup> m p<sup>-</sup> m m<sup>+</sup>. Again extent of depletion width is important.

(8)

c) Pinch-off occurs when the channel is depleted,  $\nexists$

Since it is stated that the differences in doping concentration need to be taken into account, the depletion extending from the p<sup>+</sup>-type region & that from the bulk both need to be taken into account.

Depletion from bulk:

[10]

 $W_B$ 

channel  $N_D = 10^{17} \text{ cm}^{-3}$  } only 5x different  
bulk  $N_A = 5 \times 10^{17} \text{ cm}^{-3}$  }  $\Rightarrow$  have to take both into account

$$\text{In formulae sheet } W = \sqrt{\frac{2\epsilon_0 \epsilon_s (V_0 - V)}{e}} \left( \frac{1}{N_A} + \frac{1}{N_D} \right)$$

we only need  $W_p$

$$\text{we know that } W_n + W_p = W \quad (1)$$

$$\text{charge neutrality } W_n N_D = W_p N_A \quad (2)$$

$$(2) \quad W_n = W_p \frac{N_A}{N_D} \quad (3)$$

$$(3) \text{ in (1)} \quad W_p \left( \frac{N_A}{N_D} + 1 \right) = W$$

$$W_p \left( \frac{N_A + N_D}{N_D} \right) = W$$

$$V_B = 0 \rightarrow W_p = \sqrt{\frac{2\epsilon_0 \epsilon_s (V_0)}{e}} \left( \frac{N_A + N_D}{N_D} \right)^{-1} \left( \frac{N_D}{N_A + N_D} \right)$$

$$W_p = W_{B_p} = \sqrt{\frac{2\epsilon_0 \epsilon_s V_{0B}}{e}} \left( \frac{N_D}{N_A (N_A + N_D)} \right)^{-1}$$

Depletion from gate (p<sup>+</sup>)

$$\text{gate p}^+ : 10^{20} \text{ cm}^{-3}$$

$$\text{channel n} : 10^{17} \text{ cm}^{-3}$$

since  $N_A \gg N_D$   
assume  $W_{p^+} \ll W_n$   
 $\Rightarrow$  1-sided junction.

$$W \approx W_{p_G} = \sqrt{\frac{2\epsilon_0 \epsilon_s (V_{0G} - V_G)}{e N_D}}$$

$$@ V_{GS} = V_p \quad t_n - W_{B_p} - W_{p_G} = 0$$

$$W_{p_G} = t_n - W_{B_p}$$

Comment: this question was poorly answered. Most answers ignored the depletion from the bulk. It was asked to take doping differences into account  $\Rightarrow$  Since doping in channel & substrate are  $\pm$  same, the depletion should be taken into account. The other error was that the total depletion width was taken into account, rather than the depletion width extending into the channel only.

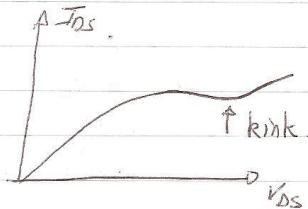
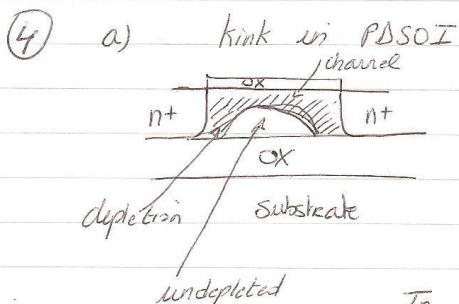
Other comments: \* This is a JFET not a MOSFET  $\Rightarrow$  different approach.  
\* too much Reproduction from course notes which is not what is asked for in this question.

(g)

$$\sqrt{\frac{2\epsilon_0 \epsilon_{si} (V_{Oe} - V_p)}{e N_D}} = t_n - \sqrt{\frac{2\epsilon_0 \epsilon_s}{e} V_{OB} \left( \frac{N_D}{N_{A_B} (N_{A_S} + N_D)} \right)}$$

$$\frac{2\epsilon_0 \epsilon_{si} (V_{Oe} - V_p)}{e N_D} = \left( t_n - \sqrt{\frac{2\epsilon_0 \epsilon_s}{e} V_{OB} \left( \frac{N_A}{N_{A_B} (N_{A_S} + N_D)} \right)} \right)^2$$

$$V_p = V_{Oe} - \frac{e N_D}{2\epsilon_0 \epsilon_{si}} \left( t_n - \sqrt{\frac{2\epsilon_0 \epsilon_{si} V_{OB}}{e} \left( \frac{N_D}{N_{A_B} (N_{A_S} + N_D)} \right)} \right)^2$$



[5]

In PDSOI, the depletion region from the gate does not reach the BOX  $\rightarrow$  there is a region of undeployed Si. When the voltage  $V_{DS}$  increases, impact ionisation occurs @ drain creating  $e^- R^+$  pairs.  $e^-$  get extracted in D but  $R^+$  build up in the undeployed region. This causes a change in charge in that region  $\rightarrow$  thus change in  $Q_{dep}$  and thus a change in  $\Delta V_{th} = \Delta Q_{dep}/C_{ox}$

$V_{th} \leftarrow \text{[redacted]} \Rightarrow I_{DS} \leftarrow \text{[redacted}] \rightarrow \text{kink Cox}$

- b) advantages :  $\circledast$  isolation between nMOS & pMOS removes latch-up  
 (late 3 out of)  $\circledast$  fewer processing steps needed

(10)

- (\*) Reduce substrate leakage  $\Rightarrow$  lower power consumption.
- (\*) Higher packing density
- (\*) smaller parasitic capacitances  $\Rightarrow$  higher speed

disadvantages.

- (take 2 out of)
- (\*) Completely surrounded by oxide  $\Rightarrow$  heating problem
  - (\*) SOI substrate more expensive
  - (\*) Transients: minority carrier <sup>generation</sup> supply only available via <sup>recombination</sup> processes

- c) for fully depleted SOI  $t_c$  needs to be depleted  
 $\text{at } V_{GS} = 0V \Rightarrow$  the depletion region from the gate  $d_g = t_c$ . This depletion region can only be formed by the workfunction difference between n-Si & ~~metal~~ gate contact.

from formulae list:

$$W_{depl} = \left[ \frac{2\epsilon(V_{bi} - V)}{e} \left( \frac{1}{N_A} + \frac{1}{N_D} \right) \right]^{1/2}$$

{ One-sided junction  $\Rightarrow$ 

$$V_{GS} = 0V$$

$$W_{depl} = \left[ \frac{2\epsilon V_{GS}}{e N_A} \right]^{1/2}$$

$$V_{bi} = 0 \text{ but } V_S \neq 0 \quad [10]$$

$$W_{depl\max} \text{ when } V_S = 2\phi_F$$

The maximum width of  $t_c$  is when  $V_{th} = 0V$   
 thus  $t_c \leq W_{depl} (V_{th} = 0V)$

V<sub>th</sub> from formulae list:

$$V_{th} = \phi_m - \phi_s + 2\phi_F + \gamma \sqrt{2\phi_F}$$

$$\gamma = \frac{\sqrt{2\epsilon\epsilon_0 N_A}}{C_{ox}}$$

(11)

$$V_{th} = 0 = \phi_m - \phi_s + 2\phi_F + \gamma \sqrt{2\phi_F}$$

$$\Rightarrow \phi_m = \phi_s - 2\phi_F - \gamma \sqrt{2\phi_F}$$

Comment:

$$V_{bi} = 0$$

$V_s \neq 0$ : draw energy band diagram.

The voltage for  $W_{dep}^{max}$

is not  $\phi_m - \phi_s$ , because

that ignores that part of

this potential difference

is dropped across the oxide:

$$V_{ox} + V_s = \phi_m - \phi_s$$

Note that  $\phi_m < \phi_s$  in order

for this to work  $\Rightarrow$  signs are important.

$$t_c^{max} = \sqrt{\frac{2\varepsilon_0 2\phi_F}{eNA}} \quad \text{with } \phi_F = V_t \ln\left(\frac{N_A}{N_D}\right)$$

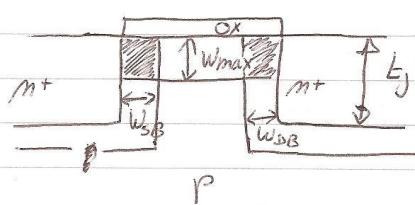
$$t_{c_{max}}^2 = \frac{4\varepsilon_0 \phi_F}{eNA}$$

$$\phi_F = \frac{eNA t_{c_{max}}^2}{4\varepsilon_0}$$

$$\phi_m = \phi_s - \frac{eNA t_{c_{max}}^2}{2\varepsilon_0 \varepsilon_s} - \gamma \sqrt{\frac{eNA t_{c_{max}}^2}{2\varepsilon_0 \varepsilon_s}}$$

$\phi_m^{min}$  = minimum value of  $\phi_m$ .

(5)



$$V_{bi} = 0 \quad V_{ds} = V_{th}$$

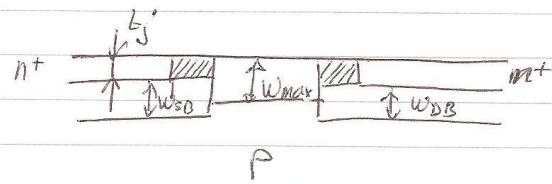
$W_{max}$ : max gate induced depletion width

$W_{SB}/W_{DB}$ : S/D depletion width

■ area of shared charge

✓

[5]



■ area of shared charge

J\_D

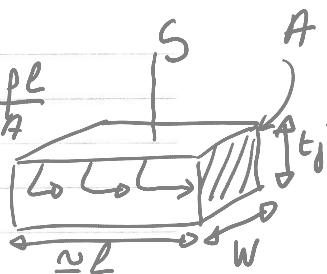
all other parameters same.

(12)

b)  $t_j \neq 0 \Rightarrow$  contact resistance  $\uparrow$  $\Rightarrow R_s \uparrow$  (source resistance)

$$R_s = \frac{pl}{A}$$

$$g_m = \frac{dI_{DS}}{dV_{GS}} \quad \text{or} \quad \frac{1}{g_m} = \frac{dV_{GS}}{dI_{DS}}$$



$$V_{GS}^{\text{ext.}} = V_{GS}^{\text{int.}} + R_s I_{DS} \quad \text{assume } \begin{cases} I_{GS} = 0 \\ I_{bulk} = 0 \end{cases}$$

$$\frac{1}{g_m^{\text{ext.}}} = \frac{dV_{GS}^{\text{ext.}}}{dI_{DS}}$$

$$= \frac{d(V_{GS}^{\text{int.}} + R_s I_{DS})}{dI_{DS}} = \frac{dV_{GS}^{\text{int.}}}{dI_{DS}} + R_s$$

$$\frac{1}{g_m^{\text{ext.}}} = \frac{1}{g_m^{\text{int.}}} + R_s$$

[8]

$$\frac{1}{g_m^{\text{ext.}}} = \frac{1 + R_s g_m^{\text{int.}}}{g_m^{\text{int.}}}$$

$$g_m^{\text{ext.}} = \frac{g_m^{\text{int.}}}{1 + R_s g_m^{\text{int.}}}$$

ext : externally measured  $g_m$ 

int : internally " " "

(without  $R_s$  parasitic)

c) Comment : important here is to derive  $g_m^{\text{ext.}}$  as a function of  $g_m^{\text{int.}}$  &  $R_s$   
 and to define what "A" is for  $R_s$ .

(13)

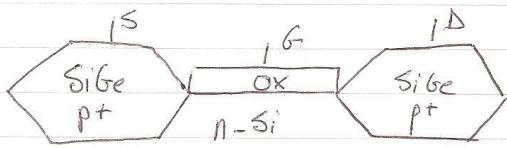
c) i) elevated source-drain technology.

[2]

ii) SiGe has a larger lattice constant than Si, thus when the Si channel is surrounded by SiGe (e.g. in the source & drain areas) it puts Si under compressive strain increasing hole mobility (for pMOS).

[2]

iii)



[3]

bookwork. one has to make the connection between elevated source-drain & local strain.