UNIVERSITY OF LONDON
IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2000

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER C112

HARDWARE

Wednesday 17 May 2000, 16:00
Duration: 90 minutes
(Reading time 5 minutes)

Answer THREE questions

Paper contains 4 questions

1. Sequential Circuit Design

A counter is to work in four modes determined by two input bits as follows.
When the input is 0 (0,0) the output remains at 0
When the input is 1 (0,1) the counter goes through the sequence 0,3,2,1,0,3,2,1 .
When the input is 2 (1,0) the counter goes through the sequence 0,1,2,0,1,2 . .
When the input is 3 (1,1) the counter goes through the sequence 1,2,3,1,2,3 . .

a. Draw the state transition diagram (using the Moore finite machine model) that corresponds to the above specification

b. Compile a state transition table in the following format:

Input		Current State		Next State	
I1	I0	Q1	Q0	D1	D0
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1				
0	1				
0	1				
0	1				
1	0				
1	0				
1	0				
1	0				
1	1				
1	1				
1	1				
1	1				

c. Draw Karnaugh maps for D0 and D1 and determine the minimum form of the Boolean equations for D0 and D1 to implement the counter.

d. Explain what the difference is between the Moore finite state machine and the Mealy finite state machine. For each, give one reason why a designer should choose to use it.

The four parts carry, respectively, 25%,20%,30%,25% of the marks.

2. Combinational Circuit Design

a. Using Boolean algebra, simplify the following Boolean expression, and draw a circuit that will implement it.

$$R = ((A.B)' + B).C)'$$

b. The exclusive NOR gate (XNOR) is defined by the following truth table

		B	
	XNOR	0	1
A	0	1	0
	1	0	1

Design a circuit to implement it, and write down its Boolean equation.

c. The full adder is defined in terms of its inputs A, B and C_{in} as

$C_{out} = A . B$
$S = A \oplus B \oplus C_{in}$

Express both boolean equations in the canonical minterm form.

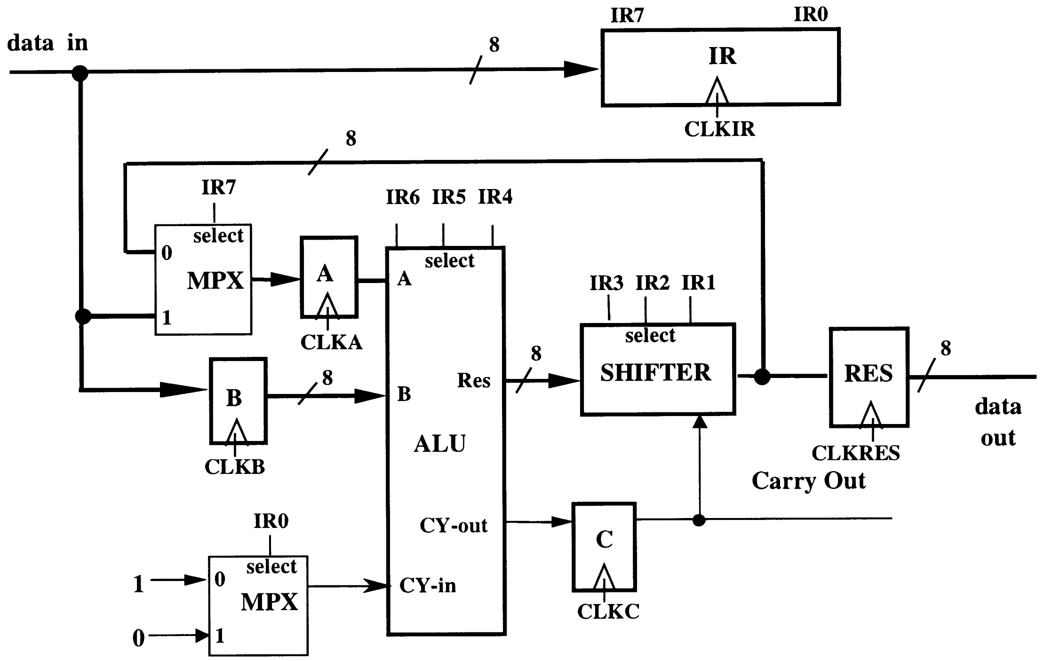
d. Find the equivalent canonical forms for the full adder using maxterms (hint: you may find it helpful to look at the truth table or Karnaugh map to do this).

e. Explain briefly why pure Boolean algebra is inadequate as a model for describing the behaviour of a flip flop.

The five parts carry equal marks.

3. The Manual Processor

An 8-bit manual processor has the following block diagram.



The functions of the various components are defined by the following tables:

Shifter:

Function Select	Shift	Carry in	Function
000	unchanged	1	unchanged
001	left	0	arithmetic/logical shift left
010	right	1	?
011	right	0	logical shift right
100	unchanged	data bit 7	unchanged
101	left	CY in	left shift with carry
110	right	data bit 7	arithmetic right shift
111	right	CY in	right shift with carry

ALU:

Selection Bits	000	001	010	011	100	101	110	111
Result	0	B mi A	A mi B	A pl B	A xor B	A+B	A.B	-1

The processor goes through a fixed cycle of five states in which the following clock gates are applied:

State	Clock
1	CLKIR
2	CLKA
3	CLKB and CLKC
4	CLKIR
5	CLKRES and CLKC

The following two instructions are to be designed for use with the processor:

ADD: which will add together two numbers on the *data in* lines, and place the result on the *data out* lines during state 5.

DEC: which will take a number from the *data in* lines, decrement it and place the result on the *data out* lines during state 5.

a. Determine the register transfers that will be carried out during each state of the processor cycle, by constructing a table in the following form.

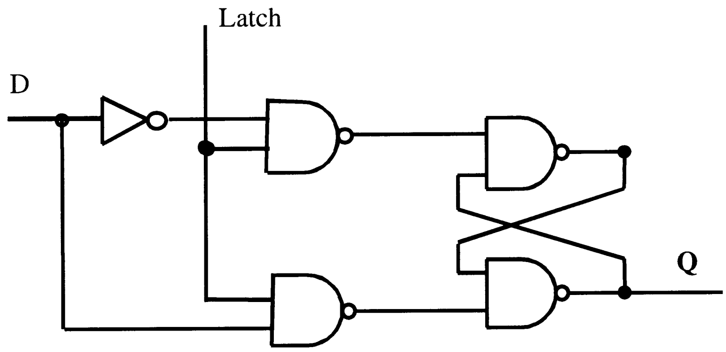
	ADD		DEC	
State	Source	Destination	Source	Destination
1	DataIn	IR		
2 etc.				

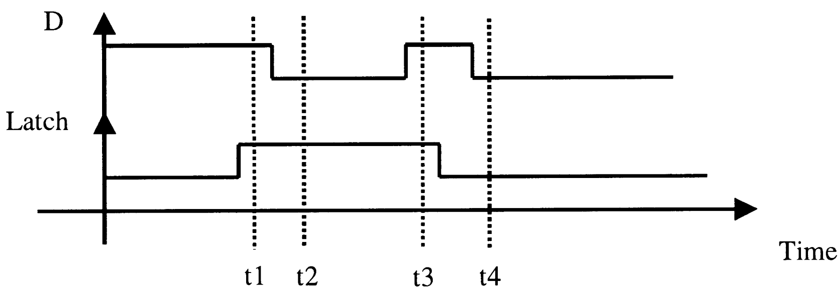
b. Find the contents of the instruction register in states 2 to 5 of the processor cycle for both the ADD and DEC instructions. This will be determined by the *data in* lines in states 1 and 4 and will contain don't care values.

The two parts carry equal marks.

4. Registers

a. The D-type latch has the following circuit. The inputs to the circuit, as a function of time are shown below can be treated as changing between 0 and 1.





Calculate the value of Q at the times t1, t2, t3 and t4 shown in the diagram.

b. Show how two D-type latches of the type shown in part a may be connected together, with other gates if required, to form a D-Q flip flop.

c. Show, with a suitable diagram, how D-Q flip flops may be connected to form a serial to parallel converter.

d. Give an example where serial to parallel conversion is used in digital computer systems. Explain briefly why it is necessary.

e. As part of a hardware design it is necessary to have a four bit register which will carry out two different functions. These are parallel load and rotate left. Draw a diagram showing the complete circuit of this register. You may use the following components in your design:

D-Q flip flops
AND gates
OR gates
INVERTER gates

The five parts carry, respectively, 20%,20%,15%,15%,30% of the marks.