IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2017

EIE PART II: MEng, BEng and ACGI

Corrected copy

COMPUTER ARCHITECTURE

Thursday, 18 May 2:00 pm

Time allowed: 1: 30 hours

There are TWO questions on this paper.

Answer TWO questions.

Answer ALL questions.

Use separate answer books for Sections A and B.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : W. Luk, D.B. Thomas
Second Marker(s) : D.B. Thomas, W. Luk

Section A (Use a separate answer book for this Section)

1 a Describe the key features of an accumulator architecture and a load-store architecture, and provide a benefit and a drawback of each of these architectures.

b An 8-bit accumulator architecture AA has the following instructions.

Instruction	Effect
`load $a`	$A = M[a]$
`store $a`	$M[a] = A$
`add $a`	$A = A + M[a]$
`sub $a`	$A = A - M[a]$
`loadc $c`	$A = c$
`jmpneg $a`	*if* $A < 0$ *then* $PC = a$
`stop`	*Program ends*

Its instruction format consists of a 4-bit opcode field, and the remaining 4 bits can be used either for a memory address or for a constant value.

i) A program P computes the sum C of A and B, where all three variables are in 8-bit BCD format (representing 2 digits, each 4 bits) and the value of A and B is between 0 and 9. Provide the instruction sequence for AA to implement P, with A in memory address 0, B in memory address 1, and C in memory address 2.

ii) How many memory accesses, including both instruction fetch and data fetch, are involved when executing P on AA in the worst case?

c Repeat Part b i) and ii) for an 8-bit load-store architecture LS, which has two general-purpose registers and the following instructions.

Instruction	Effect
`load $r $a`	$R[r] = M[a]$
`store $r $a`	$M[a] = R[r]$
`add $r1 $r2 $r3`	$R[r1] = R[r2] + R[r3]$
`sub $r1 $r2 $r3`	$R[r1] = R[r2] - R[r3]$
`loadc $r $c`	$R[r] = c$
`jmpneg $r $a`	*if* $R[r] < 0$ *then* $PC = a$
`jump $a`	$PC = a$
`stop`	*Program ends*

The three parts carry, respectively, 30%, 35%, and 35% of the marks.

Section B (Use a separate answer book for this Section)

2a i) Under what conditions would a load instruction cause a write to memory?

ii) A non-pipelined processor is to be converted to a pipelined processor with two stages. Give upper and lower bounds on the pipelined processor's clock rate, and briefly comment on how realistic those bounds are.

iii) Caches can be inserted before or after physical to virtual translation. Give one advantage of each approach.

b Most contemporary CPUs satisfy all three of these properties:

- A : They are pipelined
- B : There is a shared instruction and data address space
- C : They have separate instruction and data caches

i) Why do properties A and B imply property C?

ii) Even when property A does not hold for a CPU, it is common for property C to still hold. Give two reasons why is it still useful to have separate instruction and data caches in a non-pipelined processor

c Assume a re-useable cache design which is parametrised by cache capacity n. Extensive modelling has resulted in the following scaling properties for a given capacity (where c_a, c_h, and c_m are silicon-technology specific constants):

- Area: $a(n) = c_a\, n$
- Hit time : $h(n) = c_h \log_2 n.$
- Miss rate : $m(n) = 1/(c_m\, n)$

Two instances of the generic cache will be used to create separate data and instruction caches for a pipelined processor.

i) Explain why each of the three modelled properties are plausible, in terms of the construction and behaviour of caches. Use sketches if necessary.

ii) Given a total area budget of b for both the instruction and data cache, what is the optimal balance between the capacity of the instruction cache (n_i) and the data cache (n_d) in terms of cycle time?

The three parts carry, respectively, 35%, 30%, and 35% of the marks.