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AO5

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2009

MSc and EEE PART IV: MEng and ACGI

Corrected Copy

**CURRENT-MODE ANALOGUE SIGNAL PROCESSING**

Thursday, 14 May 10:00 am

Time allowed: 3:00 hours

No correction.

**There are SIX questions on this paper.**

**Answer FOUR questions.**

*All questions carry equal marks*

**Any special instructions for invigilators and information for candidates are on page 1.**

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Second Marker(s) : E. Rodriguez-Villegas

## The Questions

1. Figure 1.1 is an incomplete schematic diagram of the Gilbert Cell. All transistors have the same area $A_0$, the same transit frequency $f_T$ and the same DC Common Emitter current gain $\beta_0$.

   a) Complete the schematic by indicating inputs, outputs and bias sources. [5]

   b) Derive an expression for the differential DC current gain of this circuit. Neglect finite current gain effects. [5]

   c) Refine the expression you derived for the DC gain in 1(b) to include finite current gain effects. Write an expression for the frequency dependence of the transistor current gain. Comment on the effect of finite current gain at high frequencies. [5]

   d) Show that it is possible to bias the circuit so that all transistors have equal power dissipation. Show that the DC differential gain of this cell is smaller than 2. Calculate the gain if the outer transistors are biased so that $V_{CB} = V_{BE}$ [5]

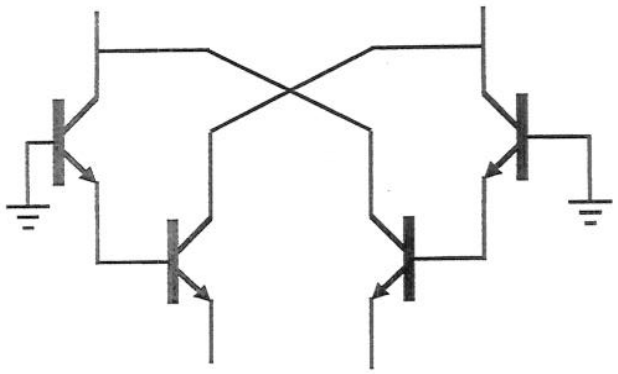

Figure 1.1

2.

a) Use n-channel MOSFETs to design a switched current circuit which can delay a signal of lowpass bandwidth $f_B$ by a time interval $\tau$, and amplify it by a constant gain C.

i) Draw a schematic diagram of this circuit.

ii) Draw all necessary timing diagrams.

iii) Include signal sources and sinks

iv) State any necessary constraints between $f_B$ and $\tau$.

[10]

b) Use the cell in part (a) to implement an integrator

[5]

c) Outline how the integrator in part (b) can be used to synthesise a 2nd order low pass filter $H(z)=\frac{1}{1-az^{-1}-bz^{-2}}$

[5]

3. Figure 3.1 shows the schematic of a current mode circuit.

a) Calculate the DC transfer function $I_{OUT} = f(I_{IN})$ of this circuit. Choose $I_{B1}$ , $I_{B2}$ , $I_{B3}$ in terms of $I_T$ so that $I_{OUT} = GI_{IN}$ . You may ignore finite current gain effects.

[5]

b) Include the capacitor current in the equation you derived in (a) to show that the circuit in figure 3.1 performs lossy current mode integration. Write an expression for the pole frequency.

HINT: Observe that the differential equation describing the behaviour of this circuit is a filter in the ratio of the input to the capacitor current. Also show that the output is proportional to this same ratio.

[15]

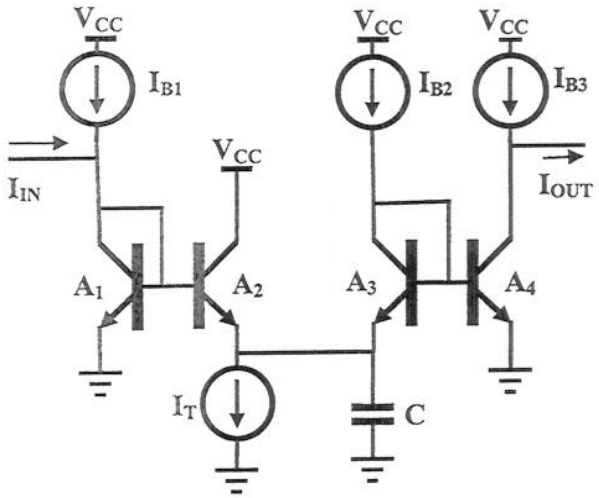


Figure 3.1

4.

a) Define the current conveyor and the Current Feedback op-amp. Write equations describing the operation of CCI, CCII, CCII∞ and CCIII.

[10]

b) Implement the filter in figure 4.1 in current mode using current conveyors of your choice. The op-amps in this circuit are ideal.

[10]

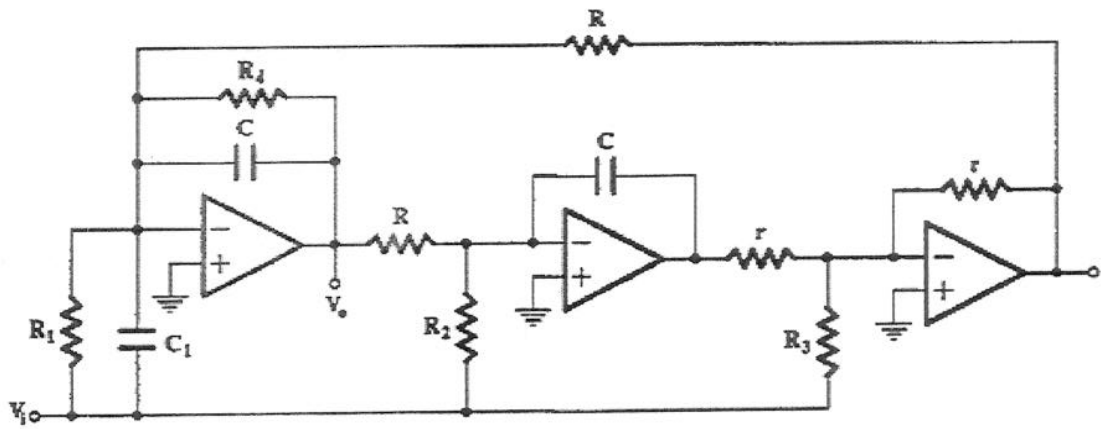


Figure 4.1

5.

a) Explain why the current feedback op-amp has a very high slew rate. Estimate the maximum slew rate of the current feedback op-amp in figure 5.1. What limits the maximum slew rate?

[3]

b) Describe an undesirable characteristic of the current feedback op-amp

[3]

c) The schematic of a current Feedback op-amp is given in Figure 5.1. Explain the role of the diodes, and how each would be implemented. What is the drawback of using these diodes?

[3]

d) Derive an expression for the open-loop transimpedance (from the inverting terminal to the output) of the circuit in Figure 5.1. Evaluate this expression for the component values given.

[2]

e) Derive an expression for the small signal open loop voltage gain (from the non-inverting terminal to the output) of the circuit in Figure 5.1. What is the unity gain frequency of the current feedback op-amp shown in figure 5.1?

HINT: The same quiescent current traverses Q1,D1 and Q3,D3

[3]

f) Explain why the gain and bandwidth of a non-inverting amp constructed with a current feedback op-amp are decoupled.

[3]

g) Calculate the feedback resistance necessary to set the bandwidth of the current feedback op-amp in figure 5.1 to 100MHz. Comment on the value you obtain.

[3]

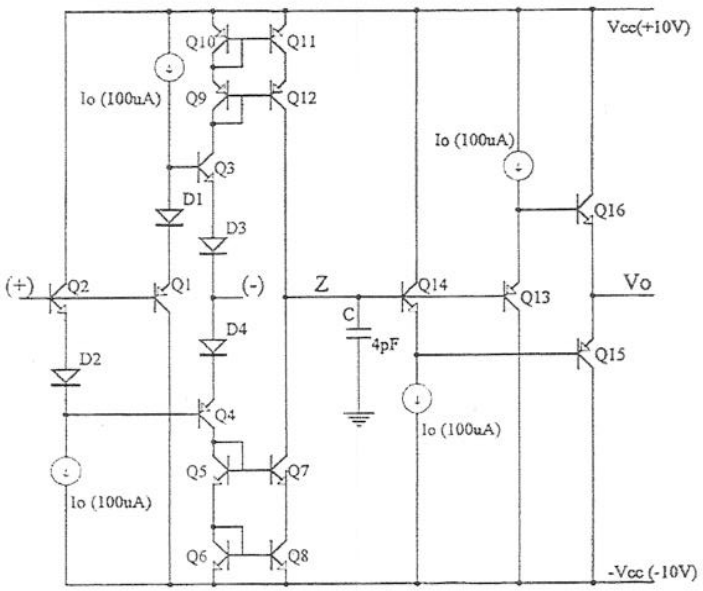


Figure 5.1

6.

a) Analyse the function of the circuit in figure 6.1

[5]

b) Analyse the function of the circuit in figure 6.2

[5]

c) Which circuit can you use to generate the input signal for part (a)?

[5]

d) Design a translinear circuit that calculates the root mean square of a signal, i.e. it takes the square of a bipolar signal, then takes the average and finally the square root.

[5]

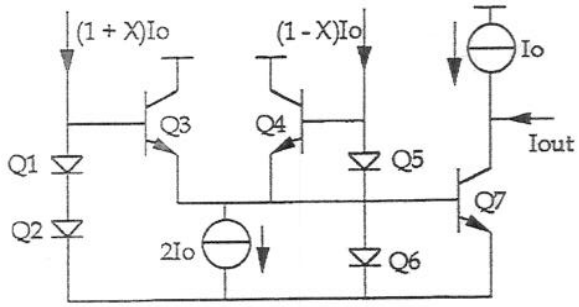


Figure 6.1

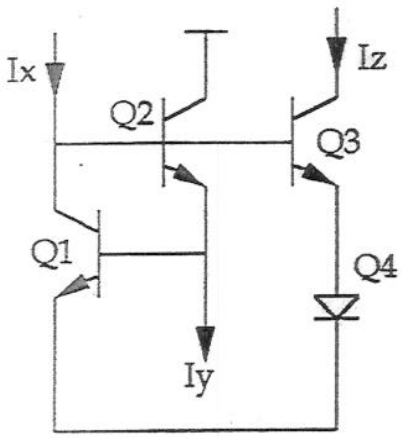


Figure 6.2

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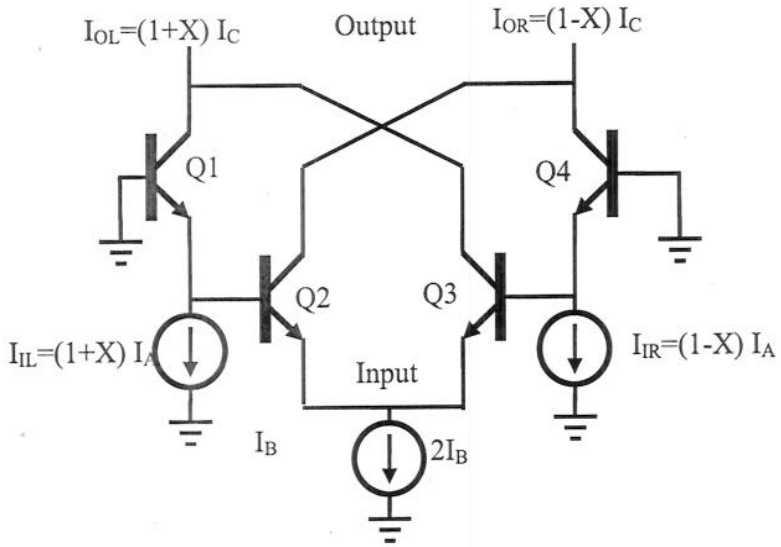
# The Answers

**ANSWER 1:**

**a)** [taught]




[5]

b) [taught]

Apply the translinear principle on the collector currents, neglecting base currents:

Let $I_3 = (1+Y)I_2$ and $I_2 = (1-Y)I_2$

$I_1 I_2 = I_3 I_4 \Rightarrow (1-Y)I_B(1+X)I_A = (1+Y)I_B(1-X)I_A \Rightarrow$

$X - Y - XY = Y - X - XY \Rightarrow X = Y$

Then the output is $I_C = I_A + I_B$ and the gain is $H = 1 + I_B / I_A$.

[5]

c) [new theory]

If the transistors have a finite gain $\beta$ then if $\delta = 1/\beta$,

$I_1 = \left((1+X)I_A - \delta(1-X)I_B\right)(1-\delta)$ , $I_2 = (1-\delta)(1-X)I_B$

$I_3 = (1-\delta)(1+X)I_B$ , $I_4 = \left((1-X)I_A - \delta(1+X)I_B\right)(1-\delta)$

$\Rightarrow I_L = I_1 + I_3 = \left((1+X)I_A - \delta(1-X)I_B\right)(1-\delta) + (1-\delta)(1+X)I_B$

$\Rightarrow I_L = (1+X)(I_A + I_B) - \delta(1+X)I_A - 2\delta I_B$

This expression now has an offset and a reduced gain.

The frequency dependent current gain is $\beta(s) = \dfrac{\beta_0}{1 + jf / f_T}$

As the transistor gain decreases at high frequencies, the cell gain decreases and phase shifts, and the offset increases.

[5]

d) [new theory]

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The collector voltages are $V_{CEQ2} = V_{CEQ3} = V_{CEQ1} + V_{BE} = V_{CEQ4} + V_{BE}$

For equal dissipation we want

$$I_A V_{CEQ1} = I_B V_{CEQ2} = I_B \left( V_{CEQ1} + V_{BE} \right) \Rightarrow \frac{I_B}{I_A} = \frac{1}{1 + \dfrac{V_{BE}}{V_{CEQ1}}} \Rightarrow$$

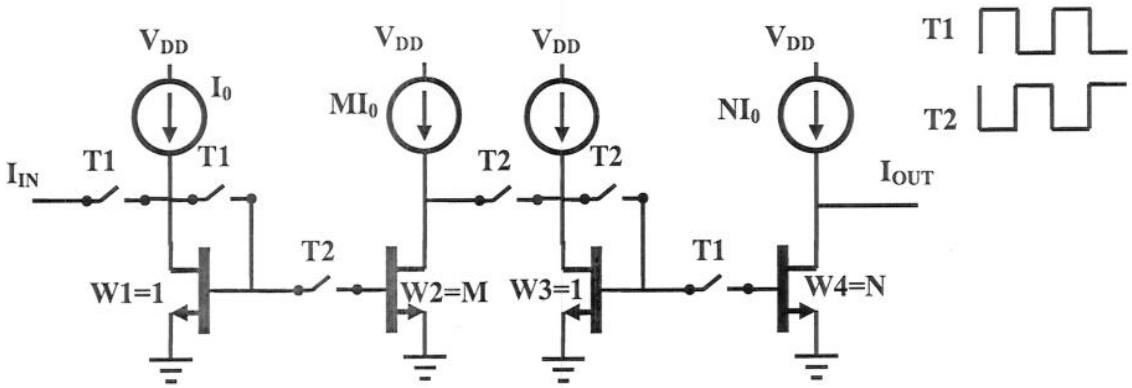
$$H = 1 + \frac{I_B}{I_A} = 1 + \frac{1}{1 + \dfrac{V_{BE}}{V_{CEQ1}}} = 1 + \frac{V_{CEQ1}}{V_{CEQ1} + V_{BE}} < 2$$

If $V_{CB} = 0 \Rightarrow V_{CE} = 2V_{BE} \Rightarrow H = 1.66$

[5]

**ANSWER 2:**

**a)** [synthesis of taught material]
The cell needs to be a 1st generation cell in order to exhibit gain. Also, we need 2 cells for a 1 cycle delay. Therefore:




The widths M, N are such that NM=C

The Nyquist criterion states that $\frac{1}{2\pi\tau} > 2f_B$.

[10]

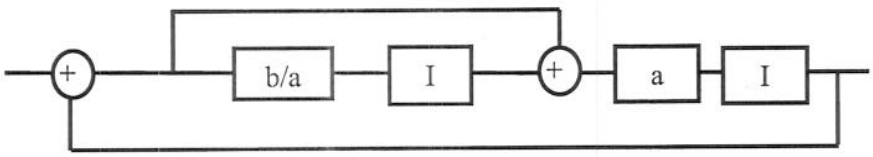
b) [taught example]
An integrator has a transfer function:
$H(z) = \frac{1}{1-z^{-1}}$. This can be implemented as


D is the cell from part (a) with gain=1

[5]

c) [computed example]
write $H(z) = \frac{1}{1-az^{-1}-bz^{-2}} = \frac{1}{1-az^{-1}\left(1+bz^{-1}/a\right)}$

Which can be implemented as:




[5]

**ANSWER 3:**

a) [computed example]
From the translinear principle,
$I_1 I_3 / A_1 A_3 = I_2 I_4 / A_2 A_4 \Rightarrow (I_{B1} + I_{IN}) I_{B2} / A_1 A_3 = (I_T - I_{B2})(I_{B3} - I_{OUT}) / A_2 A_4 \Rightarrow$
$(A_2 A_4 / A_1 A_3)(I_{IN} I_{B2} + I_{B1} I_{B2}) + I_{B3}(I_{B2} + I_T) = (I_T - I_{B2}) I_{OUT}$
This is an affine relation. To make it linear we must choose $I_{B1} = I_{B2} = 0$.
In this case,

$$\underbrace{(A_2 A_4 / A_1 A_3)}_{\gamma} I_{IN} I_{B2} = (I_T - I_{B2}) I_{OUT} \Rightarrow \frac{I_{OUT}}{I_{IN}} = \frac{1}{\gamma \frac{I_T}{I_{B2}} - 1} = G \Rightarrow \frac{I_T}{I_{B2}} = \frac{G+1}{\gamma G} \Rightarrow I_{B2} = \frac{\gamma G}{G+1} I_T$$

[5]

b) [new derivation]
In AC, it is a Bernoulli cell. The capacitor current satisfies:

$$\left.\begin{aligned} &\dot{V}_C = (I_C - i_u)/C, \; i_u = I_T - I_{B2} \\ &I_C = I_S \exp(\beta(V_{in} - V_C)) \;, \beta = 1/V_T \\ &I_{in} = I_S \exp(\beta V_{in}) \Rightarrow \dot{I}_{in} = \beta \dot{V}_{in} I_{in} \end{aligned}\right\} \Rightarrow \dot{I}_C = \beta(\dot{V}_{in} - \dot{V}_C) I_C \Rightarrow$$

$$\dot{I}_C = \beta I_C \left( \frac{\dot{I}_{in}}{\beta I_{in}} - \frac{I_C - i_u}{C} \right) \Rightarrow \dot{I}_C - I_C \left( \frac{\dot{I}_{in}}{I_{in}} + \frac{i_u}{V_T C} \right) + \frac{I_C^2}{C V_T} = 0$$

This equation in the capacitor current can be solved by letting:
$X = 1/I_C$
So that the equation becomes:

$$\dot{I}_C - I_C \left( \frac{\dot{I}_{in}}{I_{in}} + \frac{i_u}{V_T C} \right) + \frac{I_C^2}{C V_T} = 0 \Rightarrow -\frac{\dot{X}}{X^2} - \frac{1}{X} \left( \frac{\dot{I}_{in}}{I_{in}} + \frac{i_u}{V_T C} \right) + \frac{1}{X^2} \frac{1}{C V_T} = 0 \Rightarrow$$

$$\dot{X} + X \left( \frac{\dot{I}_{in}}{I_{in}} + \frac{i_u}{V_T C} \right) - \frac{1}{C V_T} = 0 \Rightarrow \dot{X} I_{in} + X \dot{I}_{in} + X I_{in} \frac{i_u}{C V_T} - \frac{I_{in}}{C V_T} = 0$$

let $Y = X I_{in}$ then $\dot{Y} + \omega_0 Y = \frac{I_{in}}{i_u} \omega_0$

Then Y is an LPF applied on the input current scaled by the bias current, with a pole at

$$\omega_0 = \frac{i_u}{V_T C}$$

We can now write for the output current:
$I_{out} = I_S \exp(\beta(V_{BE3} + V_C)) = I_{B2} \exp(\beta V_C) = I_S I_{in} X = I_S Y$, so that the output is indeed proportional to Y.

[15]

**ANSWER 4:**

a) [taught]

CC is device with 3 terminals, a non inverting voltage input, an inverting current input and a current output. A CC needs additional supplies since it cannot conserve power.

A CFOA is a CC + an impedance and a voltage follower.

CCI:
$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

CCII±
$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

CCII∞±:
$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \lim_{\varepsilon \to \infty} \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1/\varepsilon & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

CCIII:
$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

[10]

b) [new example]

Each op-amp can be replaced by a CCII∞−, x the inverting input, x the output and y the non-inverting input. All other components remain the same, the overall output becomes current input, and the overall input becomes current output.

[10]

**ANSWER 5:**

a) [taught]

The slew rate can be extremely large because $\max\left|\frac{dV}{dt}\right| = \max|i_x|C$. Since $i_x$ is an input it is unlimited. This applies also to Figure 5.1, the slew rate is only limited by the power handling of the transistors.

[3]

b) [taught]

No capacitor can be connected to the inverting or output terminals, as it increases the Q of feedback amplifiers and can cause instability.

[3]

c) [taught]

The diodes reduce offset by introducing both npn and pnp BE junctions in all signal paths. It follows that D1 and D4 are NPN and D2 and D3 are PNP. The diodes decrease dynamic range and increase the required supply and consequently power dissipation.

[3]

d) [taught]

$$Z_T = \frac{-1}{sC}$$

[2]

e) [computed example]

$$g_m = \frac{\partial I_{out}}{\partial V_+}.$$

$$v_{BE,T3} = v_{BE,D3} \Rightarrow v_{BE,T3} = v_{BE,D3} = v_+ / 2 \Rightarrow$$

$$g_m = \frac{\partial i_x}{\partial v_+} = \frac{1}{2}\frac{\partial i_x}{\partial v_{BE,T3}} = \frac{1}{2}\frac{I_0}{V_{TH}}$$

The open loop voltage gain is then

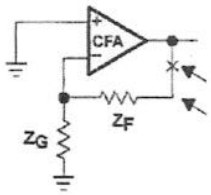
$$G = Z_T g_m = \frac{1}{2}\frac{I_0}{V_{TH} sC}$$

The unity gain frequency is when

$$G = 1 = \frac{1}{2}\frac{I_0}{V_{TH} sC} \Rightarrow \omega = \frac{1}{2}\frac{I_0}{V_{TH} C} = \frac{1}{2}\frac{100\mu A}{25mV\,4pF} = 500\text{Mrad/s}$$

[3]

f) [taught]




$$\left.\begin{aligned} V_{out} &= Z_T I_- \\ I_- &= \frac{V_- - V_{out}}{R_F} + \frac{V_-}{R_G} = V_+\left(\frac{1}{R_F}+\frac{1}{R_G}\right) - \frac{V_{OUT}}{R_F} \end{aligned}\right\} \Rightarrow V_{out} = Z_T I_- = \frac{1}{sC}\left(V_+\left(\frac{1}{R_F}+\frac{1}{R_G}\right) - \frac{V_{OUT}}{R_F}\right) \Rightarrow$$

$$V_{OUT}\left(1+\frac{1}{sCR_F}\right) = \frac{1}{sC}V_+\left(\frac{1}{R_F}+\frac{1}{R_G}\right) \Rightarrow \frac{V_{OUT}}{V_+} = \frac{1+\frac{R_F}{R_G}}{1+sCR_F}$$

The pole is always at $\omega_p = \frac{1}{CR_F}$ and the DC gain is $1+\frac{R_F}{R_G}$

[3]

f) [computed example]

$\omega_p = \frac{1}{CR_F} = 630 Mrad/s \Rightarrow R_F = 530\Omega$. This value is too small, indeed smaller than the input impedance at x.

[3]

**ANSWER 6:**

a) [taught example]
This is a 2 quadrant square circuit:

$$(1+X)^2 I_0^2 = I_3 I_7$$
$$(1-X)^2 I_0^2 = I_4 I_7$$
$$I_4 + I_3 = 2I_0$$
$$\Rightarrow 2I_0 I_7 = 2I_0^2\left(1+X^2\right) \Rightarrow I_7 = I_0\left(1+X^2\right) \Rightarrow$$
$$-I_{out} = I_7 - I_0 = I_0 X^2$$

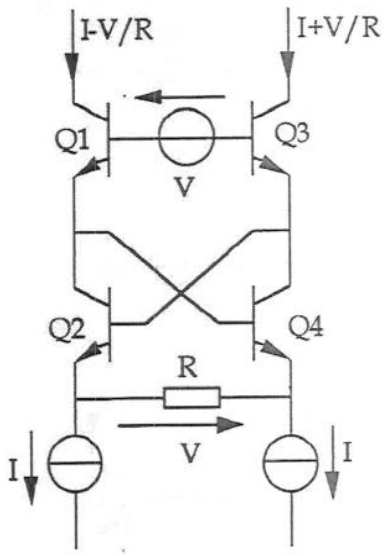
[5]

b) [taught example]
This is a geometric mean, or square root circuit:

$$I_x + I_y = I_z^2$$

[5]

c) [taught]
The Caprio Quad:




[5]

d) [new theory]
An RMS circuit can be designed by placing a current mode integrator (eg a Bernoulli cell) between these two circuits, and driving the whole thing with a Caprio Quad. The pole frequency needs to be much lower than the signal frequency.

[5]