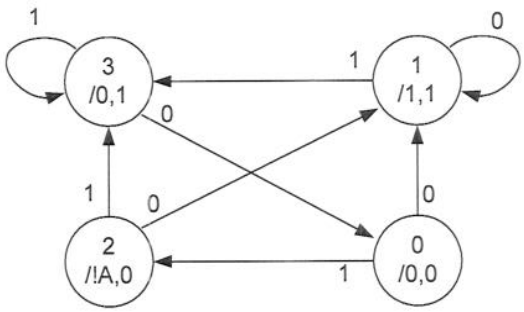
Master - June 2008

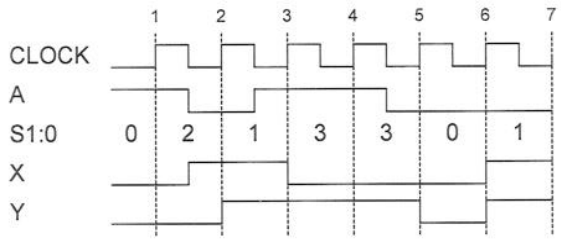
2008 E2.1/ISE2.2 Solutions

Key to letters on mark scheme: B=Bookwork, C=New computed example, A=Analysis of new circuit, D=design of new circuit

1. (a)



[5A]



[3A]

(b) The setup equation is:

$t_p + t_d + t_s < T \quad \Rightarrow \quad 2+23+11 < T \quad \Rightarrow \quad T > 36$

The hold time equation is:

$t_h < t_p + t_d \quad \Rightarrow \quad 5 < 2+7 \quad \Rightarrow \quad 5 < 9\,[\text{OK}]$

[5C]

Hence $T > 36$ ns $\Rightarrow$ $f < 27.8$ MHz [3C]

(c) (i) $I_2 = 1/20k = 50\,\mu$A. It is independent of the switch position because both sides of the switch are at ground potential: a true ground in one case and a virtual earth in the other. [4A]

(ii) The current into the op-amp summing junction is 75 µA. Thus $V_{OUT} = -75\times10^{-6}\times20\times10^{3} = -1.5$ V [4A]

(d) (i) The unfactorized expression has a propagation delay of 3 gates: one to generate G*n* and P*n*, one to form the AND product terms and one to OR them together. The factorized expression has a delay of 5 gates since P0, $P0 \cdot CI$, $G0 + P0 \cdot CI$, $P1 \cdot (G0 + P0 \cdot CI)$ and C1 must be formed in sequence. [4A]

(ii) The expression is [4B]

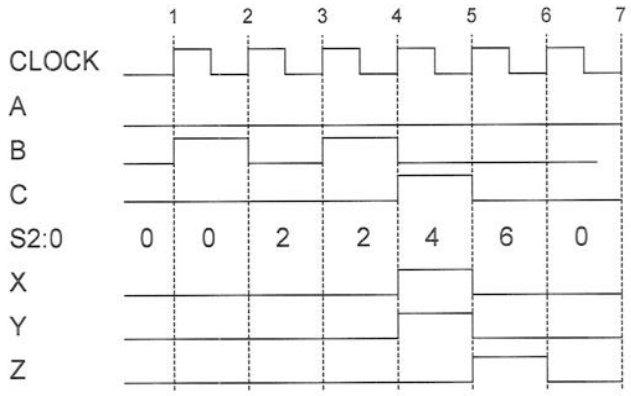
$$C2 = G2 + P2 \cdot G1 + P2 \cdot P1 \cdot G0 + P2 \cdot P1 \cdot P0 \cdot CI$$

and the propagation delay in this form remains 3 gates.

(e) (i) The smallest value is when X4:0 = 0 which gives 160. The largest value is when X4:0 = 1 which is 160+31=191. Thus the range is 160 to 191. [8A]

(ii) There are two ranges according to whether X7 = 0 or 1. If X7 = 0, the smallest value is 00100000 = 32 and the largest is 01011111 = 95. If X7 = 1, we just add 128 to these values. Thus the ranges are 32 to 95 and 160 to 223.

2. (a) The timing diagram is:



[7A]

[3A]

(b) You insert 90p but receive 30p in change: 10p from state 4 and 20p from state 6.

Hence the cost of a chocolate bar is 60p.

(c) Expressions for the output signals (where digits represent states) are:

$$X = C\cdot(1+2+3+4+5)+B\cdot(4+5)+A\cdot 5$$
$$= C\cdot((S2\oplus S1)+S0)+S2\cdot(A\cdot S0+B\cdot\overline{S1})$$
$$= C\cdot\overline{S2}\cdot(S1+S0)+S2\cdot\overline{S1}\cdot(A\cdot S0+B+C)$$

[5D]

$$Y = C\cdot(2+4)+B\cdot 5$$
$$= C\cdot\overline{S0}\cdot(S2\oplus S1)+B\cdot S2\cdot S0$$

[4D]

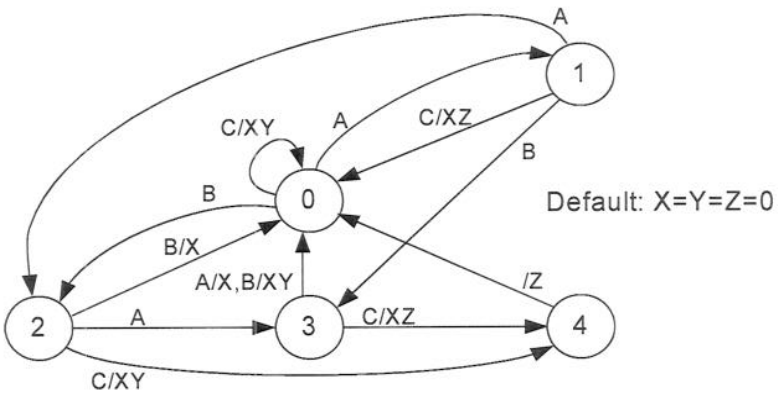
$$Z = C\cdot(3+5)+6$$
$$= C\cdot S0\cdot(S2+S1)+S2\cdot S1$$

[3D]

These expressions assume that state 7 never arises.

(d) The easiest way to modify the state diagram is to just assume an initial credit of 20p and leave everything else the same. Thus all branches that used to go to state 0 now go to state 2. We then subtract 2 from each state number to give the following:

[8D]



3. (a) In the timing digram, EN goes high whenever $q=3$ (i.e. when n is a multiple of 4). The values of y and z change on the next CLOCK rising edge.

n	1	2	3	4	5	6	7	8	9	10	11	12	13
w	6	−1	7	6	−2	6	7	5	−1	−4	−3	−1	0
Q1:0	0	1	2	3	0	1	2	3	0	1	2	3	0
EN				⎍				⎍				⎍	
x	0	6	5	12	18	16	22	29	34	33	29	26	25
y	0	0	0	0	12	12	12	12	29	29	29	29	26
z	0	0	0	0	12	12	12	12	17	17	17	17	−3

[14A]

(b) The worst case delay path is Y to D to Z.
This gives $10+18+5 \le T \;\Rightarrow\; T \ge 33 \;\Rightarrow\; f \le 30.3\,\text{MHz}$ [4A]

(c) We can show the $x(k)$ expression by induction since $x(k)=x(k-1)+w(k-1)$ and the proposition is true for $k=1$ since the sum is empty. A less formal but logical argument will also be accepted.

From part (a), we see that $y(4m)$ was stored at the end of cycle $4m-4$ (which was the last time EN was high). Thus $y(4m)=x(4m-4)$ which is the required result. [6A]

(d) From the timing diagram, we see that:

$$z(4m) = x(4m-4) - y(4m-4) = x(4m-4) - x(4m-8)$$
$$= \sum_{n=4m-8}^{4m-5} w(n) = \sum_{r=1}^{4} w(4m-4-r) = \sum_{k=1}^{4} w(4m-9+k)$$

[6A]

For $m=3$, $z(12)=w(4)+w(5)+w(6)+w(7)=6-2+6+7=17$. This agrees with the answer in part (a).

4. (a) p counts the number of high inputs and the truth table is given by:

ABCDE	p	ABCDE	p
00000	000=0	11111	101=5
10000	001=1	01111	100=4
11000	010=2	00111	011=3
11100	011=3	00011	010=2
11110	100=4	00001	001=1

[12A]

(b) Since Z<Y, the upper comparator outputs will go high in preference and so only the rightmost column in the above table is possible together with the case 00000. This gives the following table:

X	X<–4	–4<X<–3	–3<X<–2	–2<X<–1	–1<X<0	X>0
p	0	1	2	3	4	5
fl(X)	<–4	–4	–3	–2	–1	0

[6A]

From the table we see that $p = 5 + \text{floor}(X)$ is valid for –5≤X<1,

(c) Since Y<Z, only the leftmost column in the above table is possible together with the case 11111. This gives the following table:

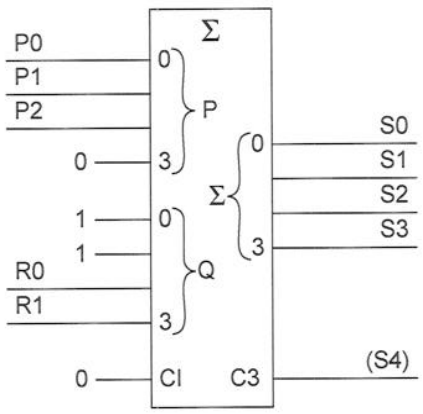
X	X<0	0<X<1	1<X<2	2<X<3	3<X<4	X>4
p	0	1	2	3	4	5
fl(X)	<0	0	1	2	3	4

[6A]

From the table we see that $p = 1 + \text{floor}(X)$ is valid for –1≤X<5,

(d) We may generate $4r+3$ by shifting r left by two bits and setting the two LSBs to 1. This gives the circuit below and we can use C3 as the fifth output bit, S4:

[6D]



s can range from 3 to 20, so we need 5 bits to represent it as an unsigned number. Although this was not part of the question, the converter output is taken as S3:0 interpreted as a signed 4-bit number which has the value $s-16$ when $r \geq 1$ and s when $r = 0$ for $-8 < X < +8$.