EE4-17
EE9-AO4

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2018

MSc and EEE PART IV: MEng and ACGI

HIGH PERFORMANCE ANALOGUE ELECTRONICS

Thursday, 17 May 10:00 am

Time allowed: 3:00 hours

Corrected copy

There are FOUR questions on this paper.

Answer ALL questions.

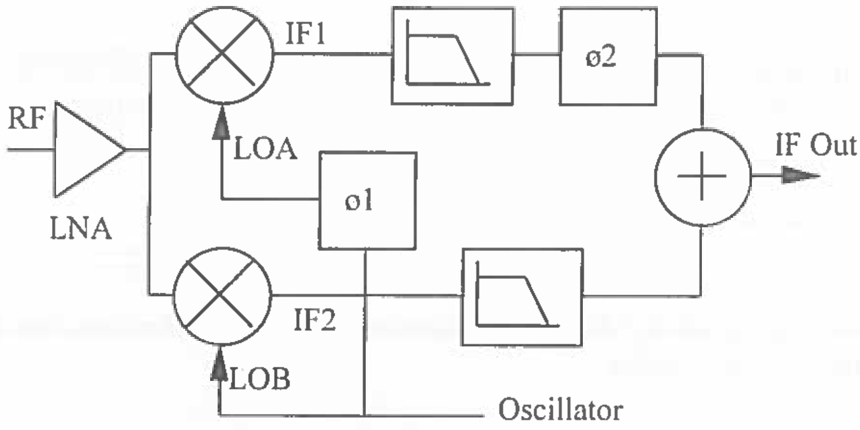
All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s) :	E. Rodriguez-Villegas
	Second Marker(s) :	A.S. Holmes

The Questions

1. (a) The receiver below has been designed with $\phi 1 = 47^{\circ}$. Derive a value for $\phi 2$ which would guarantee image rejection.



[5]

(b) Explain the role of a filter at the output of a local oscillator prior to a mixer. What type of filter would it be?

[5]

(c) In a receiver, a bandpass filter is used to remove image signals located in a 12.3MHz to 12.8MHz band. What is the bandwidth of the RF signal of interest, if the local oscillator frequency is 10.7MHz?

[5]

(d) In a receiver, what are the advantages and disadvantages of having a high gain in the front-end low noise amplifier (LNA)?

[5]

2. (a) Explain why having a differential configuration can be beneficial when designing transconductors.

[2]

(b) In a differential pair with degeneration and resistors as load and biasing, draw all the different noise sources and briefly explain which noises they correspond to.

[4]

(c) Without carrying out any analysis, explain which would be the dominant noise sources for the differential pair in (b).

[4]

(d) What would be the advantages and disadvantages of removing the degeneration in the differential pair?

[4]

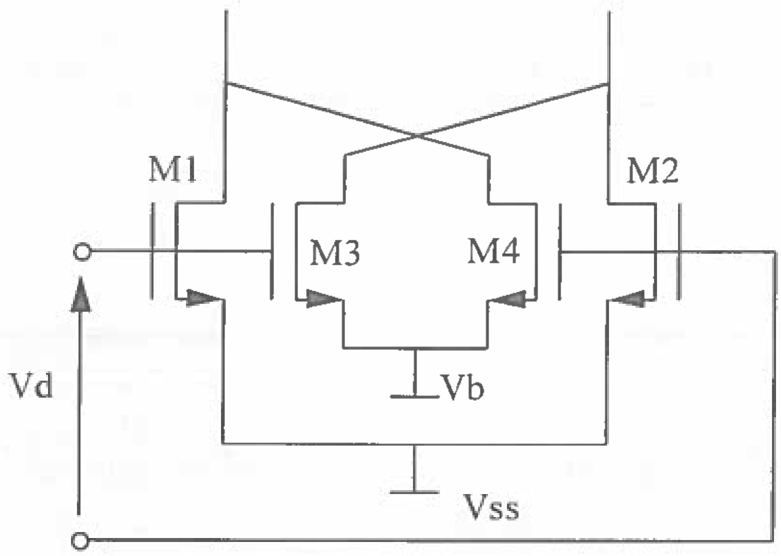
(e) A system is formed by a cascade of two blocks. The first block has an input referred white noise of $1\mu V$, integrated in a 0 to 100Hz bandwidth. The second block has an output referred white noise density of $4(\mu V)^2/Hz$. The power gain of the first block is 0.1. The power gain of the second block is 10. The input noise power from the source is $4(\mu V)^2$ in a 10KHz to 20KHz bandwidth. What is the minimum input signal in a 10kHz to 20kHz bandwidth that the system can process whilst being above the noise floor at the output?

[4]

(f) As a designer, what do you think could have been done differently to improve the noise performance of the previous system?

[2]

3. (a) In the circuit below, the large signal transconductance is 100μA/V and the values of β, V_T and Vss are $200\mu A/V^2$, 0.5V, and 1V, respectively. What is the value of Vb?



[8]

(b) As a designer, you observe that the value of the Total Harmonic Distortion, for the circuit in (a), increases for the following operating point: Vg1=1.8V, Vg2=1.9V. What is the most likely explanation for this? **Note:** Vg stands for voltage at the gate.

[3]

(c) Can the circuit above be used as a mixer? If so, explain how.

[3]

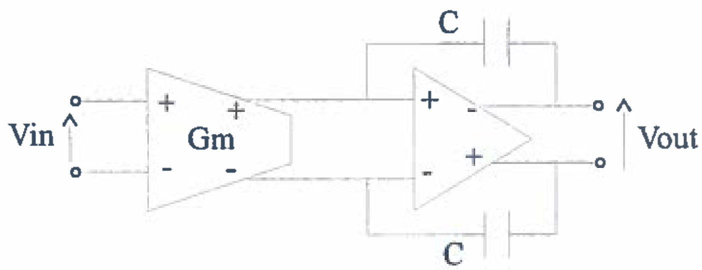
(d) Would the equivalent input noise of the circuit above be larger or smaller than the equivalent input noise of a simple differential pair? Briefly justify your answer.

[3]

(e) Would the linearity of the circuit above be larger or smaller than the linearity of a simple differential pair? Briefly justify your answer.

[3]

4. (a) What type of circuit is the one below? Give an expression for the transfer function.



[4]

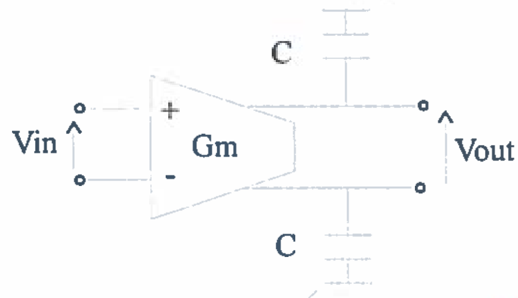
(b) What type of circuits do the following transfer functions correspond to?

$$H(s) = \frac{K\omega o^2}{s^2 + (\omega o/Q)s + \omega o^2} \qquad H(s) = \frac{Ks^2}{s^2 + (\omega o/Q)s + \omega o^2}$$

$$H(s) = \frac{K(\omega o/Q)s}{s^2 + (\omega o/Q)s + \omega o^2} \qquad H(s) = \frac{K(s^2 + \omega z^2)}{s^2 + (\omega o / Q)s + \omega o^2}$$

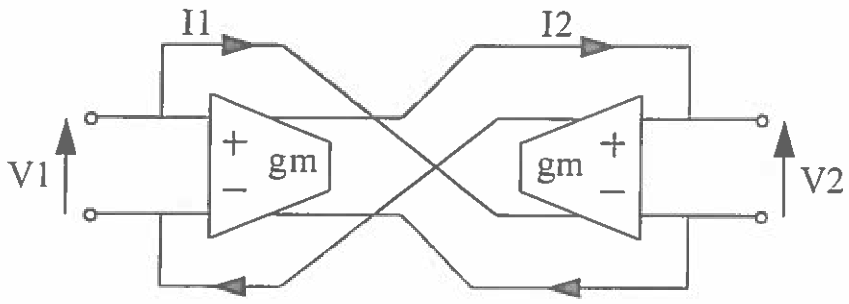
[4]

(c) What are the advantages and disadvantages of the two circuits below? Can you propose an alternative configuration which would not have any of the disadvantages you mentioned?



[4]

(d) Explain how the following circuit simulates an inductor.



[4]

(e) Find an equivalent circuit for an LC ladder, formed by two resistors of values 1Ω, three capacitors of value 2pF, and two inductors of value 1nH, which does not require inductors.

[4]