IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2007

EEE/ISE PART I: MEng, BEng and ACGI

ANALOGUE ELECTRONICS 1

Corrected Copy
None

Monday, 4 June 10:00 am

Time allowed: 2:00 hours

There are FOUR questions on this paper.

Q1 is compulsory.
Answer Q1 and any two of questions 2-4.
Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s) :	A.S. Holmes, A.S. Holmes
	Second Marker(s) :	S. Lucyszyn, S. Lucyszyn

1. **This question is compulsory**. You should attempt all six parts. State clearly any assumptions made in your calculations.

   a) For the circuit in Figure 1.1, determine the operating mode of the MOSFET and the value of the voltage V.

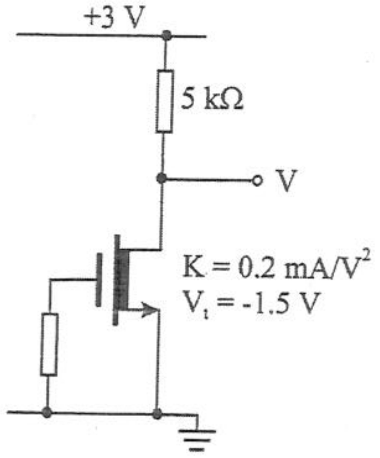


Figure 1.1

[6]

   b) For the circuit in Figure 1.2, determine the operating modes of both transistors and the value of the current I.

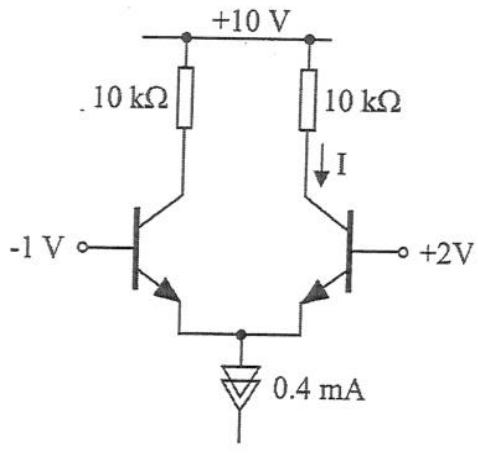


Figure 1.2

[6]

   c) A grounded common emitter amplifier is constructed using a BJT with an Early voltage of 90 V. If the load resistance in the collector circuit is 10 kΩ, and the transistor is biased at a collector current of 0.5 mA, what is the small-signal voltage gain of the circuit? [6]

Question 1 continues on the next page...

d) Figure 1.3 shows an enhancement mode MOSFET connected as a 2-terminal component. Sketch the I-V characteristic of this device for $V \geq 0$, marking on your graph any boundaries between different operating modes.

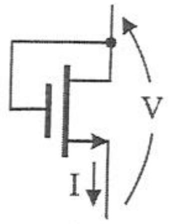


Figure 1.3 [6]

e) The voltage V_{IN} in Figure 1.4 changes to +5V at time $t = 0$, after having been held at zero for a long time. Calculate the time T taken for the output voltage V_{OUT} to fall to 5% of its initial value, and sketch the time variation of V_{OUT} from just before $t = 0$ to time $t = 2T$.

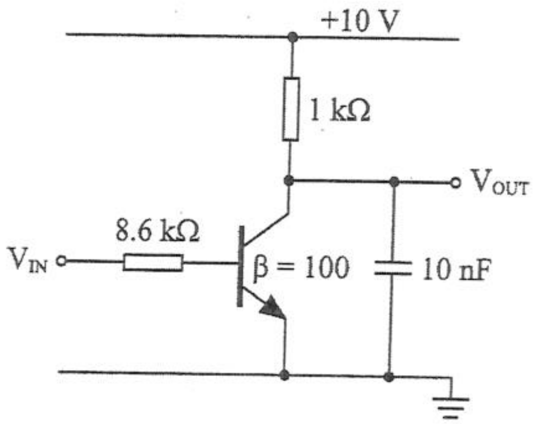


Figure 1.4 [10]

f) The characteristic equation for a Colpitts oscillator is of the form:

$$s^3 L C_1 C_2 + \frac{s^2 L C_2}{R} + s(C_1 + C_2) + \left(g_m + \frac{1}{R}\right) = 0$$

where L, C_1 and C_2 are the reactive components, R represents the circuit losses, and g_m is the usual transistor parameter. By assuming an appropriate form for the complex frequency, s, derive an expression for the oscillation frequency. Also determine the minimum transconductance required for oscillation to occur. [6]

2. a) Determine the collector bias current and quiescent output voltage for the amplifier in Figure 2.1, stating clearly any assumptions you make. Your calculation should take into account the base current of the transistor. [8]

b) Draw a small-signal equivalent circuit for the amplifier, assuming the bypass capacitor is effectively short-circuit, and hence determine the small-signal macromodel parameters (input resistance, output resistance and voltage gain) in the mid-band. [12]

c) Two amplifiers similar to that in Figure 2.1 are cascaded and inserted between a signal source and a load, as shown in Figure 2.2. Determine the overall voltage gain v_L/v_S for this arrangement at frequencies for which all the coupling capacitors are effectively short-circuit. [10]

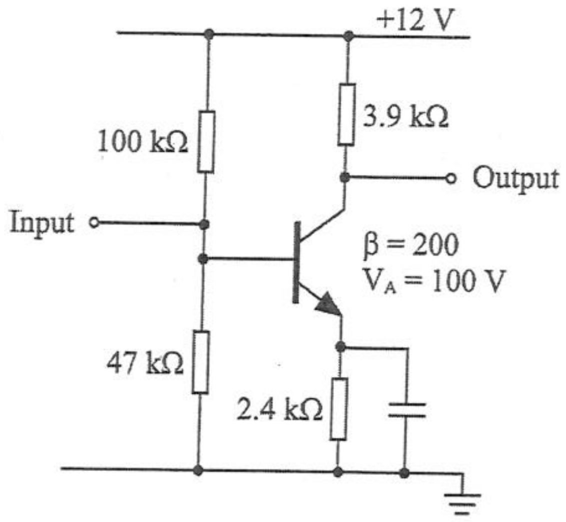


Figure 2.1

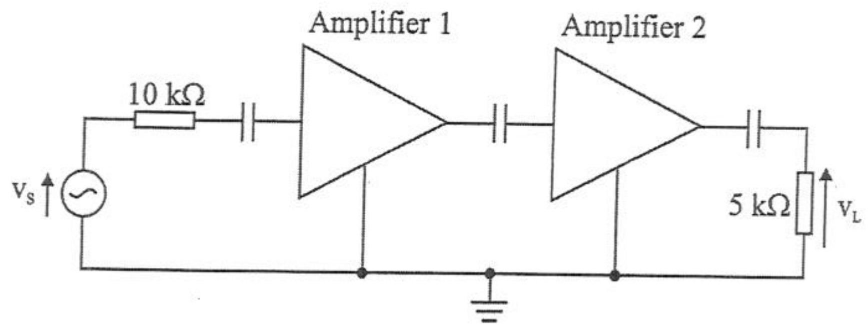


Figure 2.2

3. Figure 3.1 shows an NMOS amplifier employing two enhancement mode MOSFETs.

a) Neglecting the current in the resistor R_F, and assuming both transistors are active, show that the output voltage V_{OUT} may be expressed as:

$$V_{OUT} = V_{DD} - V_{t2} - \sqrt{\frac{K_1}{K_2}} \cdot (V_{G1} - V_{t1})$$

where K and V_t denote the usual MOSFET parameters, V_G denotes gate voltage, and subscripts 1 and 2 refer to Q1 and Q2 respectively. [10]

b) Determine the range of output voltages over which both transistors will remain in the active region, and choose the value of R_F so that the quiescent output voltage lies exactly at the middle of this range. [12]

c) Using the equation in part a), or otherwise, calculate the voltage gain of the amplifier in the mid-band where the input capacitor is effectively short-circuit. Would you expect this amplifier to show linear behaviour for large signals? Explain your answer. [8]

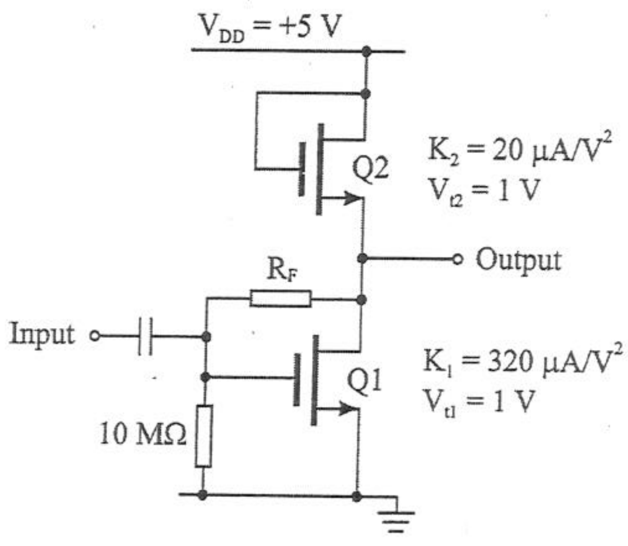


Figure 3.1

4. a) Sketch the circuit diagram for a Class B push-pull output stage. What are the main drawbacks of this configuration as a voltage follower? [10]

b) Figure 4.1 shows one possible configuration for a Class AB output stage. In this circuit, Q2 and Q4 are matched, as are Q1 and Q3. All transistors have $\beta = 50$.

Explain the role of Q1 and Q3. Also, by considering just the upper half of the circuit and neglecting base currents, show that, when Vout = 0, the currents I_1 and I_2 are related as follows:

$$I_2 \exp(I_2 R / V_T) = N I_1$$

where $N = I_{S2}/I_{S1}$ is the ratio of the saturation currents of Q2 and Q1, and $V_T = 25$ mV. If $I_{S1} = 0.25$ pA and $I_{S2} = 5$ pA, what value of R will give a quiescent current of 10 mA in the output transistors? [15]

c) Calculate the base-emitter voltage of Q2 when the output stage is delivering 100 mA into the load. In this calculation you should assume that Q4 is carrying negligible current. Also calculate the base-emitter voltages of Q1, Q3 and Q4 under these conditions, and hence verify that the assumption you made about Q4 is justified. [5]

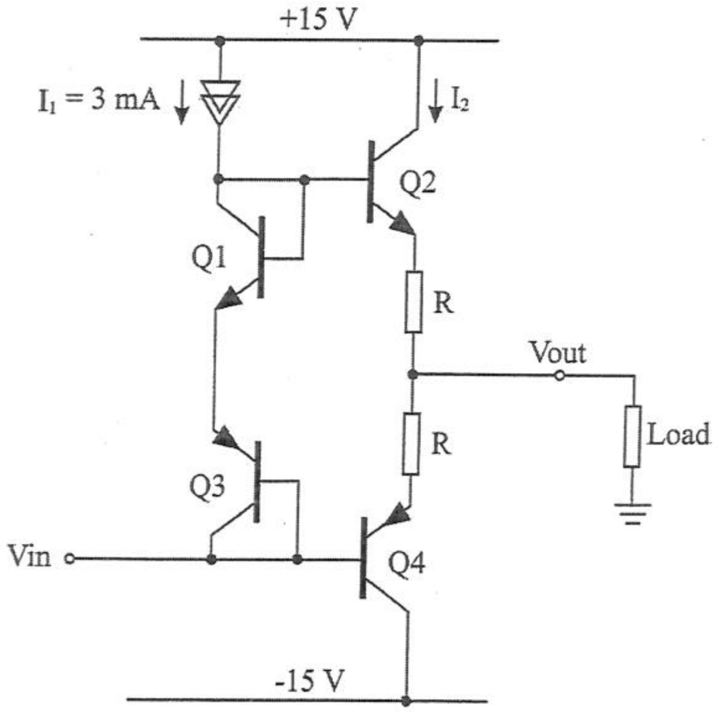


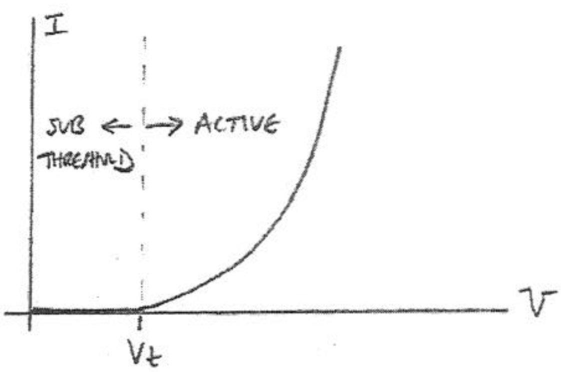
Figure 4.1

1 a) $I_G = 0$, so $V_{GS} = 0$ and (Depletion) MOSFET is conducting
If active then $I_D = K(0 - V_t)^2 = 0.2 \times (1.5)^2 = 0.45\,mA$
This would imply $V = 3 - 0.45 \times 5 = 0.75\,V$
But this inconsistent with active mode since $0.75 < (0 - -1.5)$
$\Rightarrow$ MOSFET must be in <u>TRIODE</u>
Now $I_D = 0.2\left[2\cdot(1.5)\cdot V - V^2\right] = \frac{3-V}{5}$
$\Rightarrow 3V - V^2 = 3 - V \Rightarrow V^2 - 4V + 3 = 0$
$\Rightarrow (V-1)(V-3) = 0$. $V=3$ rejected, so $\underline{V = 1V}$ [6]

b) Differential i/p voltage (3V) is $\gg V_T$ so can assume RH transistor is carrying all the tail current.
$V_E = \max\{2, -1\} - 0.7 = 1.3\,V$
$\Rightarrow$ For LH transistor $V_{BE} = -2.3\,V$, $V_{CB} = +11V \Rightarrow$ <u>LH CUT-OFF</u>.
RH transistor has $I_E = 0.4\,mA$, so $\underline{I = 0.4\,mA}$ if active (neglecting I_B). This implies $V_C = 10 - 0.4 \times 10 = 6V$
which is $> V_B$ so active assumption OK. $\Rightarrow$ <u>RH ACTIVE</u> [6]

c) Small-signal voltage gain for grounded C.E. amp
is $A_v = -g_m(R_C // r_o)$. (standard result)
$g_m = I_C/V_T = 0.5\,mA/25\,mV = 0.02\,S$
$r_o = V_A/I_C = 90V/0.5\,mA = 180\,K$; $R_C = 10k$
$\Rightarrow A_v = -0.02 \times (180k // 10k) = \underline{-189}$ [6]

d) $I_G = 0$, so $I = I_D$. Also, $V_{GS} = V_{DS} = V$ so
(Enhancement) MOSFET is active provided $V > V_t$
So $I = 0$ for $V \le V_t$
$I = K(V - V_t)^2$ for $V > V_t$

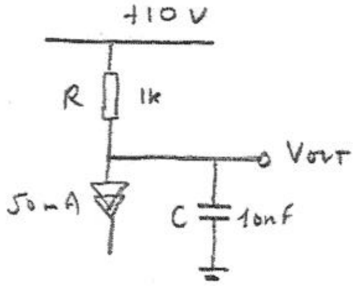


[6]

1 e) Before I/P step, cct has reached steady state with $V_{OUT} = 10V$
Capacitor voltage is continuous so $V_{OUT}\big|_{t=0^+} = +10V$
$\Rightarrow$ At $t=0^+$ transistor is ACTIVE with

$I_B = (5-0.7)/8.6k = 500\mu A$; $I_C = 100 \times 500\mu A = 50mA$

Equivalent cct is :



If transistor remained active then new S.S. would be

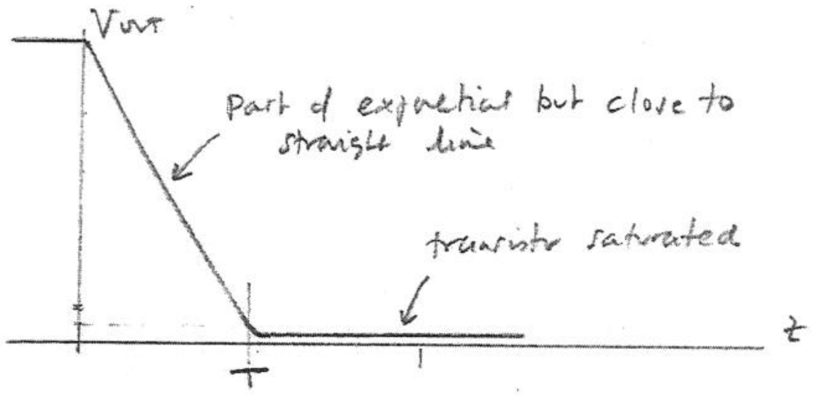
$V_{OUT} = 10 - 50 \times 1 = -40V$

$\Rightarrow$ Using standard result, time variation of V_{OUT} while transistor remains active is :

$$V_{OUT} = -40 + (10 - -40)\,e^{-t/\tau}$$
$$= -40 + 50\,e^{-t/\tau} \qquad \tau = RC = 10\,\mu sec$$

Time taken for V_{OUT} to fall to 5% of +10V is given by: $0.5 = -40 + 50\,e^{-T/\tau}$

or $T = \tau \ln[50/40.5] = \underline{\underline{2.11\ \mu sec}}$



[10]

f) For stable oscillation, characteristic equation must have solution for which $s = j\omega$, where ω is the oscillation frequency. Substituting this form for s gives

$$-j\omega^3 LC_1C_2 - \frac{\omega^2 LC_2}{R} + j\omega(C_1+C_2) + \left(g_m + \frac{1}{R}\right) = 0$$

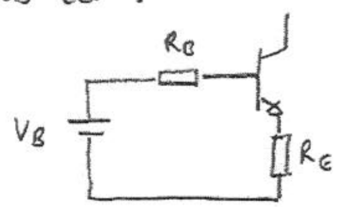
Imag. part $\Rightarrow$ $\omega^2 = \dfrac{C_1+C_2}{LC_1C_2}$ or $f = \dfrac{1}{2\pi}\sqrt{\dfrac{C_1+C_2}{LC_1C_2}}$ Hz

Real part : $\Rightarrow$ $\dfrac{(C_1+C_2)}{LC_1C_2} \cdot \dfrac{LC_2}{R} = g_m + \dfrac{1}{R}$ or $g_m = \dfrac{C_2}{C_1R}$

This is the minimum g_m for oscillation

[6]

2 a) Bias cct :



where $V_B = \frac{47}{47+100} \times 12 = 3.837\ V$

and $R_B = 100k \,\|\, 47k = 31.97\,k$

KVL : $I_E R_E + V_{BE} + I_B R_B = V_B$

$$\Rightarrow \quad I_E = \frac{V_B - V_{BE}}{R_E + R_B/_{1+\beta}}$$

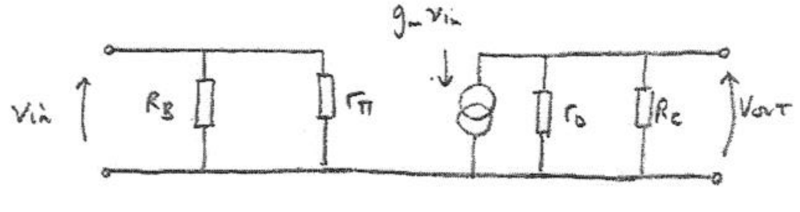
Assuming $V_{BE} = 0.7 \Rightarrow I_E = 1.226\ mA$

$$I_c = \alpha I_E = \frac{200}{201} \times 1.226 = \underline{\underline{1.22\ mA}}$$

$$V_{out} = 12 - 1.22 \times 3.9 = \underline{\underline{7.24\ V}}$$

[8]

b) SSEC :



$g_m = I_c/_{V_T} = 48.8\ mS$

$r_\pi = \beta/g_m = 4.098\ k\Omega$

$r_o = \frac{V_A}{I_c} = 81.97\ k\Omega$

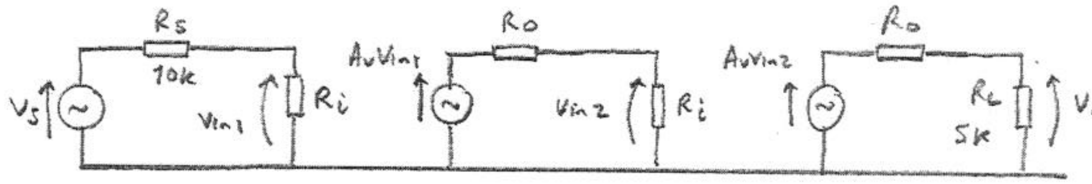
$$R_i = R_B \| r_\pi = 31.97k \,\|\, 4.098k = \underline{\underline{3.63\ k\Omega}}$$

$$R_o = R_C \| r_o = 3.9k \,\|\, 81.97k = \underline{\underline{3.72\ k\Omega}}$$

$$A_v = -g_m R_o = \underline{\underline{-182}}$$

[12]

c) Overall SSEC with s/c caps :



$$V_L = \frac{R_L}{R_L + R_o} \cdot A_v v_{in2} = \frac{R_L}{R_L + R_o} \cdot A_v \cdot \frac{R_i}{R_i + R_o} \cdot A_v \cdot \frac{R_i}{R_i + R_S} \cdot V_S$$

$\Rightarrow$ Overall gain is

$$\frac{V_L}{V_S} = A_v^2 \cdot \frac{R_L}{R_L + R_o} \cdot \frac{R_i}{R_i + R_o} \cdot \frac{R_i}{R_i + R_S}$$

$$= (-182)^2 \cdot \frac{5}{5 + 3.72} \cdot \frac{3.63}{3.63 + 3.72} \cdot \frac{3.63}{3.63 + 10} = \underline{\underline{+2498}}$$

[10]

3 a) Assuming both transistors are active :

$$I_{D1} = K_1 (V_{G1} - V_{t1})^2 \quad ; \quad I_{D2} = K_2 (V_{DD} - V_{OUT} - V_{t2})^2$$

if current in R_F can be neglected, then $I_{D1} = I_{D2}$

$$\Rightarrow \quad K_1 (V_{G1} - V_{t1})^2 = K_2 (V_{DD} - V_{OUT} - V_{t2})^2$$

taking +ve $\sqrt{\ }$ (both active) $\Rightarrow \sqrt{\frac{K_1}{K_2}} (V_{G1} - V_{t1}) = V_{DD} - V_{OUT} - V_{t2}$

$\Rightarrow$ required result after rearrangement [10]

b) Q2 is DG-connected $\Rightarrow$ active provided $V_{GS} > V_t$

Requires $V_{DD} - V_{OUT} \geq V_{t2}$ or $V_{OUT} \leq V_{DD} - V_{t2}$

$V_{OUT} \leq 4V$

Q1 active provided $V_{OUT} \geq V_{G1} - V_{t1}$

Can get lower limit by substituting $V_{OUT} = V_{G1} - V_{t1}$ into part a) equation $\Rightarrow$

$$V_{OUT} = \frac{V_{DD} - V_{t2}}{1 + \sqrt{K_1/K_2}} = \frac{4}{5} = 0.8V$$

So, range is $\underline{\underline{0.8V \leq V_{OUT} \leq 4V}}$

Middle of range is $+2.4V$, which corresponds to a V_{G1} of

$$\frac{5 - 1 - 2.4}{4} + 1 = 1.4\ V$$

(rearranging part a) eqn)

But at DC $\quad V_{G1} = \frac{10M}{10M + R_F} \times V_{OUT}$

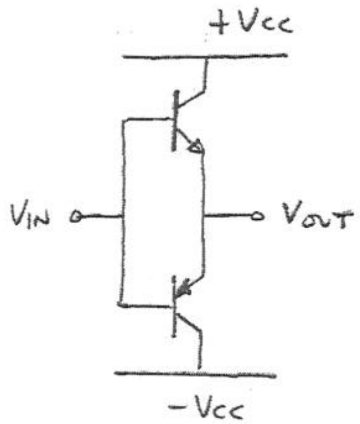
$$\Rightarrow \frac{R_F}{10M} = \frac{2.4}{1.4} - 1 = 0.714 \quad \Rightarrow \underline{\underline{R_F = 7.14\ M\Omega}}$$ [12]

c) Can get gain simply by differentiating part a) eqn

ie $\quad A_V = \frac{\partial V_{OUT}}{\partial V_{IN}} = \frac{\partial V_{OUT}}{\partial V_{G1}} = -\sqrt{\frac{K_1}{K_2}} = \underline{\underline{-4}}$

<u>Yes</u>, amplifier is linear for large signals because large-signal i/p - o/p relationship is linear in V_{G1}. [8]

4 a)



Main drawbacks as voltage follower are cross-over distortion and level shift (that is different for +ve and -ve signals).

[10]

b) Q1 and Q3 provide a bias voltage between the bases of Q2 and Q4, ensuring that at least one of them is conducting at all times.

When $V_{OUT} = 0$, $V_{E1} = 0$ also because of symmetry. KVL for Q1, Q2 and R then gives:

$$V_{BE1} = V_{BE2} + I_2 R$$

$$\Rightarrow \quad V_T \ln\left(\frac{I_1}{I_{S1}}\right) = V_T \ln\left(\frac{I_2}{I_{S2}}\right) + I_2 R$$

$$\Rightarrow \quad \frac{I_1}{I_{S1}} = \frac{I_2}{I_{S2}} \cdot \exp\left(\frac{I_2 R}{V_T}\right) \quad \text{or} \quad N I_1 = I_2 \exp\left(\frac{I_2 R}{V_T}\right)$$

as req.

Putting $N = \frac{5}{0.25} = 20$, $I_1 = 3$ mA, $I_2 = 10$ mA $\Rightarrow$ $\underline{\underline{R = 4.48\ \Omega}}$ [15]

c) $I_{E2} = 100$ mA $\Rightarrow$ $I_{C2} = 98$ mA ; $I_{B2} = 1.96$ mA

$I_{C2} = I_{S2} \exp\left(\frac{V_{BE2}}{V_T}\right)$ $\Rightarrow$ $V_{BE2} = V_T \ln\left(\frac{I_{C2}}{I_{S2}}\right) = \underline{\underline{592 \text{ mV}}}$

if $I_{B2} = 1.96$ mA, then $I_{E1} = 3 - 1.96 = 1.04$ mA

and $I_{C1} = 1.02$ mA $\Rightarrow$ $V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right) = 553$ mV $= V_{EB3}$

Now, working anti-clockwise around loop starting from V_{OUT} we get:

$$\begin{aligned} V_{B4} &= V_{OUT} + I_{LOAD} R + V_{BE2} - V_{BE1} - V_{EB3} \\ &= V_{OUT} + 448 \text{ mV} + 592 \text{ mV} - 553 \text{ mV} - 553 \text{ mV} \\ &= V_{OUT} - 66 \text{ mV} \end{aligned}$$

So, with no current in lower "R", we have $V_{BE4} = -66$ mV and I_{E4} is negligible $\Rightarrow$ assumption was justified. [5]