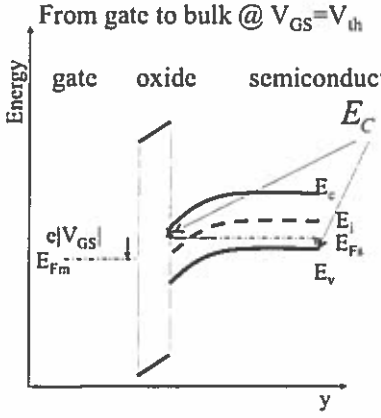
EE3-11

AED exam answers - 2015

1. a) [bookwork] [4]

From gate to bulk @ $V_{GS}=V_{th}$



b) [bookwork.] [4]

Charge balance equation (charge neutrality):

$$Q_G + Q_I + Q_{depl} = 0$$

Q_G is the charge on the gate, is positive for nMOS

Q_I is the charge in the inversion layer underneath the oxide, is negative for nMOS

Q_{depl} is the depletion charge, are fixed ionised acceptor atoms in the substrate, negative in nMOS

Voltage balance equation:

$$V_{GS} = V_{ox} + V_s$$

V_{GS} is the voltage on the gate, is positive for nMOS

V_{ox} is the voltage drop across the oxide, is positive for nMOS

V_s is the voltage drop across the semiconductor near the junction, is positive in nMOS. Is equal to the sum of the voltage drop across the inversion layer and the voltage drop across the depletion layer.

c) [bookwork.] [4]

$V_s = 2\,\phi_F$ – definition of threshold voltage $\phi_F = E_i - E_F$ in the substrate

$n_s = N_A = n_i \exp(\phi_F/V_T)$ – NA is doping density in substrate, V_T is thermal voltage and n_i is the intrinsic carrier concentration.

d) [application of overall knowledge on optimisation techniques] [4]

i) The use of high-k dielectric HfO_2 with metal gate
The use of elevated source and drain contacts
The use of SiC in contacts to impose local tensile strain in the Si channel
The use of SOI (silicon on insulator substrate technology). [4]

ii) In order of i).

- Allows to increase the gate capacitance due to higher dielectric constant while preventing increased leakage current.
- Reduces the source and drain contact resistance associated to the shallow implants in the Si body and thus maintains high g_m (tranconductance).
- Tensile strain in the channel increases the mobility of the electrons and thus the speed of the carriers in the channel
- SOI insulates the substrate from the device layers. More specifically for speed is that the depletion regions underneath the ohmic contacts no longer exist which reduces parasitic capacitances. [4]

e) no doping in the channel of the HEMT (modulation doping). [1]

2. a) [bookwork]

i)

A: JFET

B: MESFET [2]

ii) JFET = pn diode thus built-in voltage is given by (see formulae sheet):

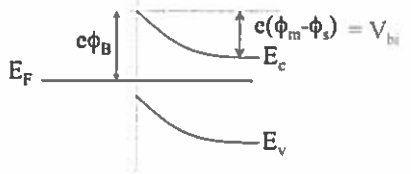
$V_{bi} = V_T \ln(N_A N_D/n_i^2)$

$V_{bi} = 0.026$ [V] $\ln(10^{20}\, 10^{17}/(1.79\, 10^6)^2)$

$V_{bi} = 1.47$ eV

MESFET: gate is Schottky contact

The energy band diagram illustrates the built-in voltage:



ϕ_s is the workfunction of the doped GaAs channel: $\phi_s = \chi_s + (E_c - E_F)$ with χ_s the electron affinity. Constants can be found in the constants list.

From formulae list: $n = N_C \exp[(E_F - E_c)/kT]$

Thus $E_F - E_c = kT \ln(N_C/n) = kT \ln(N_C/N_D) = 0.026 \ln(4.7\, 10^{17}/10^{17}) = 0.04$ eV

$\phi_s = \chi_s + (E_c - E_F) = 4.1$ eV $+ 0.04$ eV $= 4.14$ eV

$V_{bi} = \phi_m - \phi_s = 4.6 - 4.14 = 0.46$ eV

This calculation shows that the potential barrier at the p+n junction in the JFET is much larger than that of the metal-semiconductor contact is the MESFET. Since the leakage current is controlled by the height of the potential barrier, leakage in the highest barrier structure will be lowest, thus for the JFET. [4]

b) [Bookwork]

i)

One sided depletion width d_n: [5]

$$d_n = \sqrt{\frac{2\varepsilon(V_{bi} - V_r)}{q}\frac{1}{N_D}}$$

$$V_{bi} = e\left(\phi_m - \phi_{Si}\right)$$ [2]

V_r is the reverse bias current magnitude which is $V_{GS} - V_y(y)$. y is transport direction.

At pinch off $V_{GS} = V_p$ and V_{DS} is given to be = 0. Note: a_m is the metallurgic junction.

$$d_n(y) = \sqrt{\frac{2\varepsilon\left(V_{bi} - (V_{GS} - V(y))\right)}{eN_D}}$$

$$d_n = a_m = \sqrt{\frac{2\varepsilon\left(V_{bi} - V_p\right)}{eN_D}}$$

$$V_p = V_{bi} - \frac{eN_D a_m^2}{2\varepsilon} = V_{bi} - V_{p0}$$ [3]

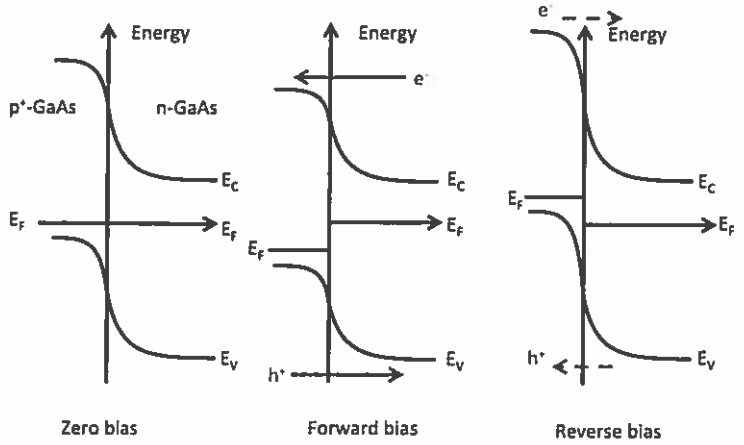
ii) Calculate the threshold voltage, V_{th} for the JFET. [4]

$V_{th} = V_p$

$V_{th} = 0.46$ V $- (1.6\, 10^{-19}\, 10^{17}\, (200\, 10^{-7})^2)/(2\, 13\, 8.85\, 10^{-14}) = -2.32$ V

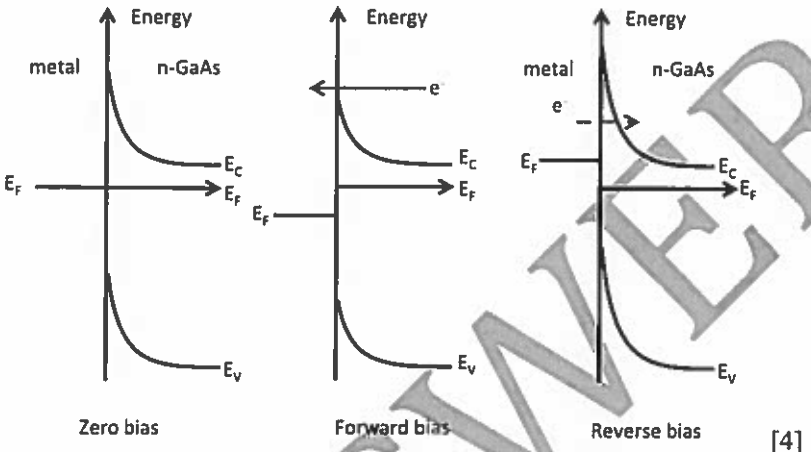
c) [Application of knowledge on bipolar and unipolar devices.]

i) JFET [8]



[4]

MESFET



[4]

ii) MESFET has highest switching speed because it is governed by majority carrier injection rather than minority carrier injections. MESFET gate currents are determined by majority carrier thermionic emission across the barrier (see above). Thus in reverse bias no current flows from GaAs into gate. In pn diode switching is delayed by minority carrier storage. [2]

3. HEMT

a) [bookwork but need to remember $n=n_i$ for intrinsic material] [5]

Workfunction is calculated via:

$\phi_s = \chi_s + (E_c - E_F) = \chi_s + kT \ln(N_C/n)$

for undoped materials $n = n_i$ and for doped materials $n = n_D$.

Parameters from formulae list (for x=0.3 in $Al_{0.3}Ga_{0.7}As$):

$n_{i\,GaAs} = 1.79 \times 10^6$ cm^{-3}

$n_{i\,InAs} = 1 \times 10^{15}$ cm^{-3}

$n_{i\,AlGaAs} = 2.1 \times 10^3$ cm^{-3}

$\chi_{GaAs} = 4.1$ eV

$\chi_{InAs} = 4.9$ eV

$\chi_{AlGaAs} = 4.07 - 1.1 \times 0.3 = 3.74$ eV

$N_{C\,GaAs} = 4.7 \times 10^{17}$ cm^{-3}

$N_{C\,InAs} = 8.7 \times 10^{16}$ cm^{-3}

$N_{C\,AlGaAs} = 2.5 \cdot 10^{19} \times (0.063 + 0.083 \times 0.3)^{3/2}$ cm^{-3} $= 6.72\ 10^{17}$ cm^{-3}

InAs

$\phi_{InAs} = 4.9 + 0.026 \ln(8.7 \times 10^{16}/10^{15}) = 5.02$ eV

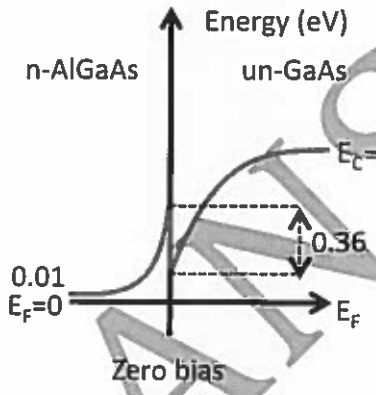
GaAs

$\phi_{GaAs} = 4.1 + 0.026 \ln(4.7 \times 10^{17}/1.79 \times 10^6) = 4.78$ eV

AlGaAs

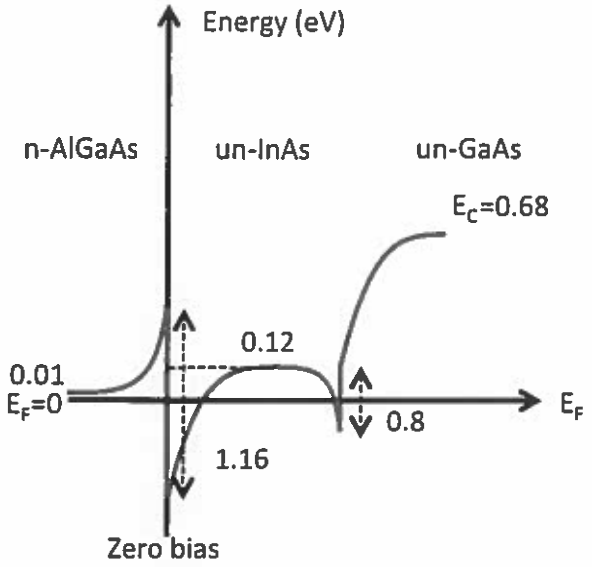
$\phi_{AlGaAs} = 3.74 + 0.026 \ln(6.72 \times 10^{17}/5 \times 10^{17}) = 3.75$ eV

b) [bookwork] Conduction band offset between AlGaAs and GaAs using the electron affinity rule: $\Delta E_c = 3.74 - 4.1 = -0.36$ eV. The negative sign is important as it states that from the E_c in AlGaAs we need to go downwards to reach the E_c of GaAs. [5]



Note that these band diagrams are sketches since we do not know the magnitude of the band bending in each region around the junction as we have not solve the schrodinger equations.

c) [application of heterojunction energy band diagrams] Conduction band offset between AlGaAs and InAs using the electron affinity rule: $\Delta E_c = 3.74 - 4.9 = -1.16$ eV. Conduction band offset between InAs and GaAs using the electron affinity rule: $\Delta E_c = 4.9 - 4.1 = +0.8$ eV. [5]

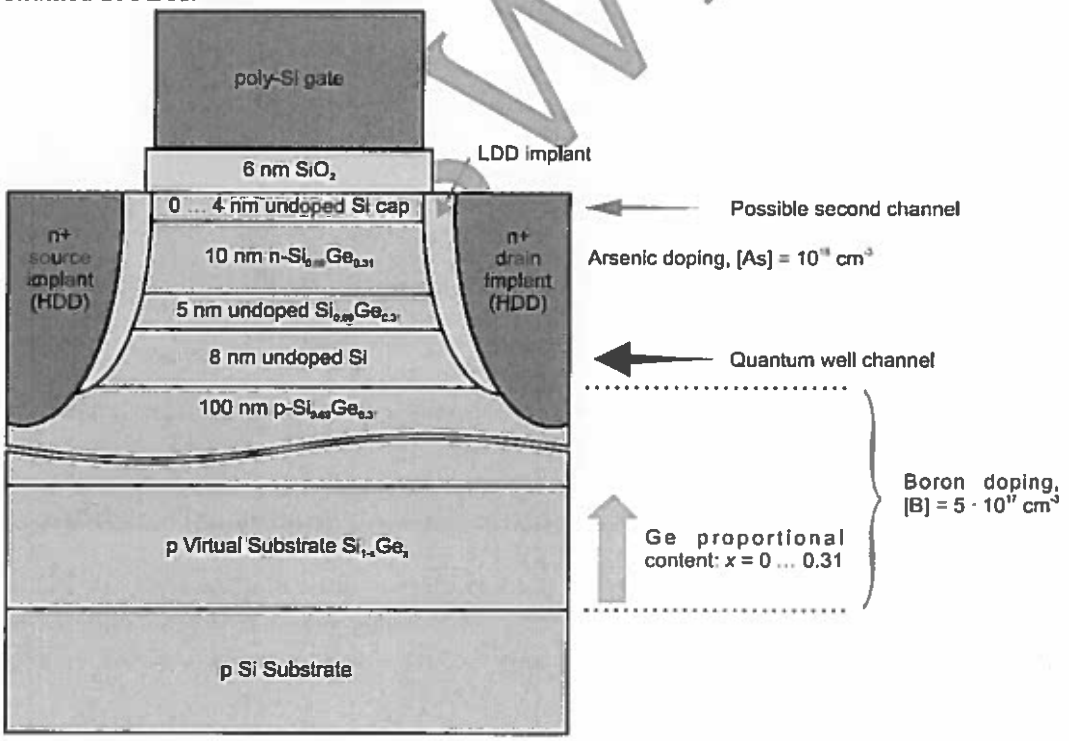


d)

i) (b). Note that $V_{th} < 0$ for HEMTs. (c) will have a deeper quantum well thus more e- available at $V_{GS} = 0$ thus V_{th} must be more negative to pull E_F under E_c of InAs channel. Therefore (b) has the highest V_{th} (closest to 0V) [3]

ii) (c) electron mobility in InAs higher than in GaAs [2]

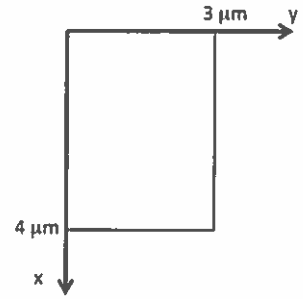
e) bookwork but students must make the connection between the HEMT and globally strained Si FETs.



4. Application of TCAD knowledge.

a)

i) [2]



ii) t_{ox} = 0.01 µm. [2]

iii) This command ensures that the remeshing definition in refine box is applied to the structure. [1]

iv) [5]

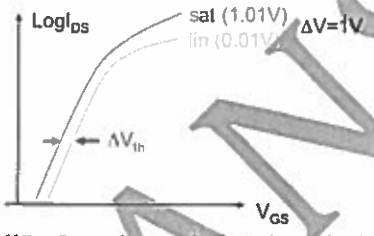
```
14 mask name=source_drain_mask left=1.25 right=1.75
15 mask name=gate_mask          left=1.25 right=1.75 negative
23 refinebox min={-0.02 1.2} max={0.01 1.8} xrefine=0.005
yrefine = 0.005
31 contact name=gate box Oxide xlo=-0.02 xhi=-0.01 ylo=1.25
yhi=1.75
Note: if the dimensions of the Si bulk are also reduced and
different command lines adapted accordingly then the
simulations will be faster.
```

b)

$$DIBL = \frac{\left|V_{th}^{lin} - V_{th}^{sat}\right|}{\left(V_{DS}^{sat} - V_{DS}^{lin}\right)}\left(\frac{mV}{V}\right)$$

i) [2]

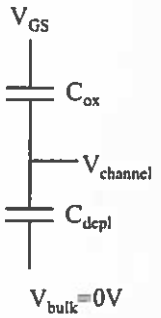
ii) Must be the transfer characteristics. [3]



iii) In order to derive the sub-threshold swing SS, we need to see the equivalence between the BJT and the MOSFET in weak inversion. The potential in the channel of the weakly inverted MOSFET is equivalent to V_{EB} in the BJT. The channel potential is determined by the voltage divider C_{ox} and C_{depl}. [5]

The output current in a BJT has the form:

$$I_C = I_S \exp\left(\frac{V_{EB}}{V_T}\right)$$



In analogy for the MOSFET, V_{EB} is the voltage in the channel, $V_{channel}$ as a result of the applied V_{GS}, given by the capacitive divider:

$$V_{EB} \rightarrow V_{channel} = \frac{C_{ox}}{C_{ox} + C_d} V_{GS}$$

Thus, the weak inversion current takes to form:

$$I_{DS} = I_S \exp\left(\frac{C_{ox}}{C_{ox} + C_d}\frac{V_{GS}}{V_T}\right)$$

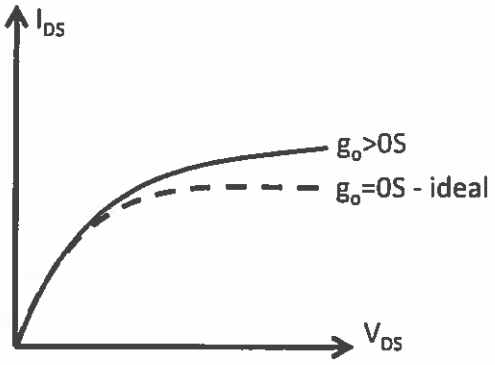
The sub-threshold slope is then given by:

$$S = \frac{dV_{GS}}{d\log(I_{DS})} \approx \frac{kT}{q}\ln(10)\left(1+\frac{C_d}{C_{ox}}\right)$$

iv) [2]

The minimum possible value that can be obtained is when $C_{ox} >> C_D$ (thin gate oxide) at room temperature: $S_{min} = 26\ mV \times 2.3 = 60 mV/dec$.
Difference is $72 - 60 = 12\ mV/dec$

v) [3]



5.

a) [bookwork] The thickness of the Si film must be smaller than the maximum depletion width. The maximum depletion width is when threshold is reached, thus surface potential $V_s = 2\,\phi_F$. Take depletion width equation from equation sheet and simplify for a 1-sided junction, set $V_{bi} = 0$ and replace the reverse bias voltage by $2\,\phi_F$. N_B is the doping of the body. [4]

$$t_{Si} \le W_{depl}, \text{ where } W_{depl} = \sqrt{\frac{2\varepsilon_s(2\phi_F)}{qN_B}}$$

b)

i) [bookwork] [4]

$$V_{GS}^{appl} = V_{GS}^{FET} + R_S I_{DS}$$

$$\frac{dV_{GS}^{appl}}{dI_{DS}} = \frac{dV_{GS}^{FET}}{dI_{DS}} + R_S$$

$$\frac{1}{g_m^{extr}} = \frac{1}{g_m^{intr}} + R_S$$

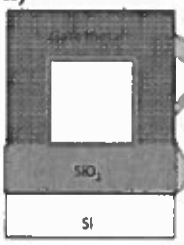
$$g_m^{extr} = \frac{g_m^{intr}}{1 + R_S g_m^{intr}}$$

ii) [application of MOSFET knowledge] The channel in UTB MOSFETs is very thin and thus the carriers see an oxide surface at both sides of the channel, the top one is the gate oxide, the bottom one is the BOX. Oxide surface are rough and cause scattering, reducing the mobility. [2]

c) [bookwork]

i) Note: only two gates – those at the sides of the fin. [3]

ii) The Si channel is now gated at 3 sides and the fin is more square. [3]



iii) Tigate structure allows the dimensions of the fin to be relaxed (less thin). [2]

d) [new topic].

i) Independent gate operation can be implemented in finFETs by removing the metal gate connect at the top of the fin (see picture below). Now there are two disconnected gate contacts that can be biased separately. [3]

ii) One gate contact can control the threshold voltage, whilst the other gate is used for the signal. The energy band diagram is drawn under the assumption that there is no work function difference between fin and gate metal. This illustrates that gate 2 depletes the channel and thus controls the threshold voltage cfr V_{BS}. [4]