EE4-17
EE9-AO4

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2017

MSc and EEE PART IV: MEng and ACGI

Corrected copy

HIGH PERFORMANCE ANALOGUE ELECTRONICS

Monday, 15 May 10:00 am

Time allowed: 3:00 hours

There are FOUR questions on this paper.

Answer ALL questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible
First Marker(s) : E. Rodriguez-Villegas
Second Marker(s) : P. Georgiou

The Questions

1. (a) In a system formed by a cascade of circuit blocks, which ones are the most and least critical ones in terms of noise, and why?

[4]

(b) A system is formed by two cascaded circuit blocks. The first one has a noise factor of 4 and a power gain of 0.9. The second one has a noise factor of 5 and a power gain of 1. Which one of the two blocks is more critical in terms of noise and why?

[4]

(c) Draw a noise-equivalent small signal model for a MOS transistor. Name and give expressions for all the noise sources in the strong inversion saturation region.

[3]

(d) Draw a common-source NMOS stage with a voltage source impedance.

[3]

(e) Calculate an expression for the noise of the circuit you drew in part (d). Assume the gate to source leakage current is not negligible.

[3]

(f) As a designer, what would you do to improve the noise performance of the circuit you drew in part (d)?

[3]

2. (a) Explain why, as a designer, for certain applications you would choose a differential configuration as opposed to a single ended one.

[3]

(b) Briefly explain at least one disadvantage of having a fully differential configuration, as opposed to a single ended one.

[2]

(c) Which one of the following statements is correct and why?

A- The input transistor dominates the noise in a given circuit. In order to improve this, the circuit could be made differential, since with ideal matching, the noise from the two inputs would cancel out.

B- The input transistor dominates the noise in a given circuit. Making the circuit differential will only make worse the noise performance.

[3]

<u>The circuit of Figure 1 relates to the subsequent sections of this question.</u>

The circuit in Figure 1 has been designed on a technology with threshold voltage values equal to 0.6V for NMOS transistors. The block is intended to be used in an application with input voltages ranging from 0.75V to 0.9V. The total harmonic distortion must be under 0.5%. A transient simulation is run, followed by Fourier analysis. This shows that the second order harmonic is 10dB (power) lower than the first order one.

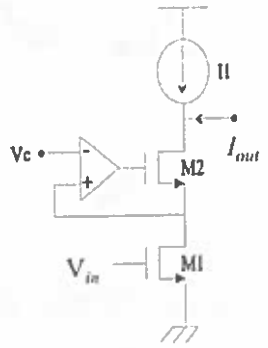

Figure 1

(d) Does this design meet the specifications? If the answer is no, what specification is not met?

[3]

(f) As a designer what would you be inclined to do to improve the Total Harmonic Distortion?

[3]

(g) Provide an expression for the output current in the circuit in Figure 1, assuming the transistors are biased in a region that minimizes distortion.

[3]

(h) When simulating an early version of the circuit in Figure 1, the simulator shows a square wave pulse signal at the output, swinging between the rails (0 and VDD). This is despite the fact that the input is a very small sinusoidal signal. Is your circuit working? If the answer is no explain why, and what would you be inclined to do as a designer.

[3]

3. (a) Name the type of filters the following transfer functions correspond to:

$$H1 = \frac{K\omega o^2}{s^2 + (\omega o/Q)s + \omega o^2}$$

$$H2 = \frac{Ks^2}{s^2 + (\omega o/Q)s + \omega o^2}$$

$$H3 = \frac{K(\omega o/Q)s}{s^2 + (\omega o/Q)s + \omega o^2}$$

$$H4 = \frac{K(s^2 + \omega z^2)}{s^2 + (\omega o / Q)s + \omega o^2}$$

[4]

(b) What is the functionality of the two circuit blocks in Figure 2. Give expressions for the transfer functions.

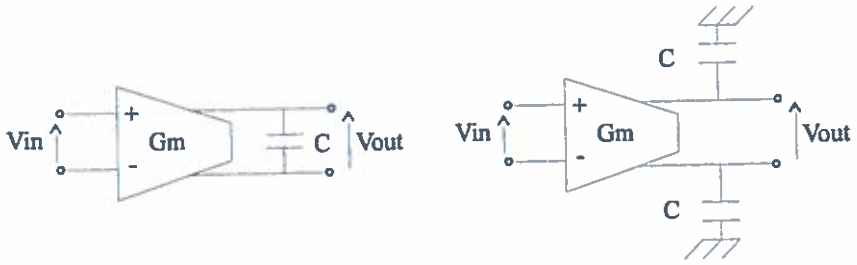

Figure 2

[4]

(c) Mention one advantage and one disadvantage for each of the circuits in Figure.

[4]

(d) Use integrators to implement the flow diagram in Figure 3.

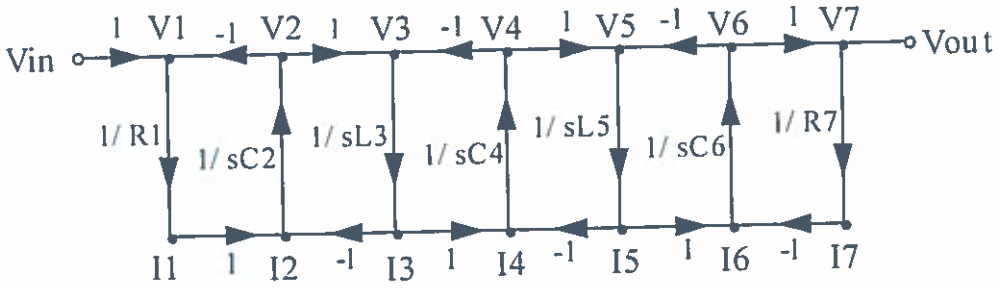

Figure 3

[4]

(e) Draw and LC ladder that functionally behaves as the circuit you drew in (d).

[4]

4. (a) Briefly explain the problem of the image in superheterodyne receivers.

[4]

(b) What receiver specification parameter would you be trying to improve by placing a low pass filter at the output of the local oscillator?

[4]

(c) Draw a mixer. Briefly explain advantages and disadvantages of the circuit you drew.

[4]

(d) The signal coming from a transducer is band limited to 1kHz, by a second order low pass. What is the minimum frequency this signal should be sampled at? Briefly explain why.

[4]

(e) The circuit designed in (a) is found to consume too much power in a new application. However, in this application the signal of interest is only from 30Hz to 200Hz. Since the sampling frequency of the A/D converter is programmable, the system designers decide to reduce this to 500Hz. But when testing the system, it is found that the output signal shows a significant amount of additional distortion. What did the system designers fail to consider when reducing the sampling frequency?

[4]