E4.20
AC3
ISE4.19

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2007

MSc and EEE/ISE PART IV: MEng and ACGI

INTRODUCTION TO DIGITAL INTEGRATED CIRCUIT DESIGN

Friday, 27 April 2:30 pm

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

Corrected copy

Q 6

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung
Second Marker(s) : C. Bouganis

Information for Invigilators:

Students may bring any written or printed aids into the examination.

Information for Candidates:

Students may need red, green, blue, yellow and black coloured pens.

1. a) *Figure 1.1* (see the colour supplementary sheet) shows the layout of an n-well CMOS circuit *P* with four terminals: `in[0]`, `on[t]`, `on[f]` and `out`. Extract and draw the transistor-level schematic diagram of this circuit. Note that `vdd` and `gnd` are routed on the metal 2 layer.

[4 marks]

b) *Figure 1.2* (see the colour supplementary sheet) shows the layout of an n-well CMOS circuit *Q* with four terminals: `c[1]`, `c[2]`, `sin` and `sout`. Extract and draw the transistor-level schematic diagram of this circuit.

[6 marks]

c) Assuming that the transistor connected to the terminal `sin` for the circuit *Q* in *Figure 1.2* is of size $20\lambda \times 2\lambda$, find the size of all transistors for the circuit.

[3 marks]

d) For the layout shown in *Figure 1.1*, draw the vertical cross section along the line `AA'`. Label your diagram indicating the n-well region and the different types and levels of doping (e.g. p^-, n^+ etc).

[7 marks]

2. *Figure 2.1* shows part of an address decoder circuit for a CMOS memory chip. T1 and T6 are strong and weak transistors respectively when compared with the pull-down transistors T2-T5. The signals `addr[5:0]` forms the 6-bit row address of a memory array.

   a) Explain how this circuit works including the purpose of transistor `T6`.

   [2 marks]

   b) Design the predecoder circuit so that the output signal `Y` drives the `word_line` high for the row address $2D_{16}$.

   [4 marks]

   c) Given that the timing diagram for the input signals `addr_clock` and `addr[5:0]` are as shown in *Figure 2.2*, draw the timing diagram for the signals at X and Y. Label your timing diagram with the following four possible signal states: driven low (DL), driven high (DH), charged low (CL) and charged high (CH).

   [4 marks]

   d) Design the layout of the decoder circuit shown in *Figure 2.1* (including that for your predecoder design) in the form of symbolic layout or stick diagram.

   [10 marks]

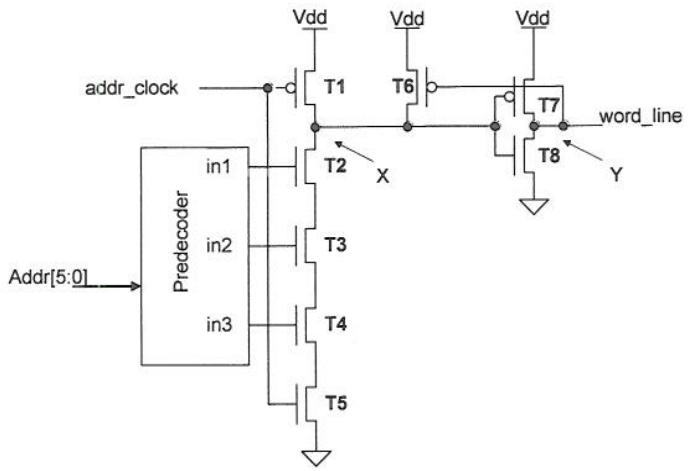


Figure 2.1

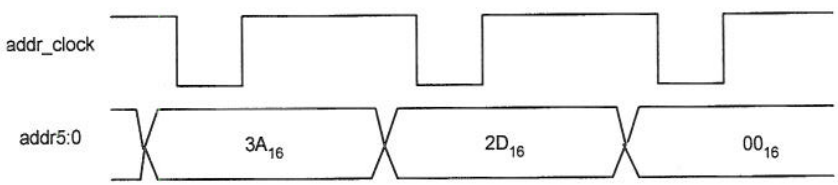


Figure 2.2

3. a) Explain the principle of a precharged circuit and briefly discuss its advantages and disadvantages.

[4 marks]

b) a_i , a_{i+1} and b_i , b_{i+1} are the ith and (i+1)th bits of the binary numbers A and B respectively. *Figure 3.1* shows a 2-bit binary adder using a precharge circuit to add the ith and (i+1)th bits of A and B together. c_{i-1} is the carry input to the ith bit from the adder adding the lower bits together. The signal CLK is the precharge clock. Suppose:

$$x_i = a_i \oplus b_i$$
$$g_i = a_i \bullet b_i$$
$$\hat{g}_i = \overline{a_i} \bullet \overline{b_i}$$

By deriving the Boolean equation for T, V in terms of : g_i, c_{i-1} and x_i and x_{i+1} during the evaluate phase of the clock, show that:

$T = \overline{c_i}$, the complement of ith bit carry output,

$V = \overline{s_i}$, the complement of the ith bit sum output,

[8 marks]

c) Design the layout of the circuit shown in *Figure 3.1* in the form of symbolic layout or stick diagram. Label your layout by marking all the transistors and signal nodes.

[8 marks]

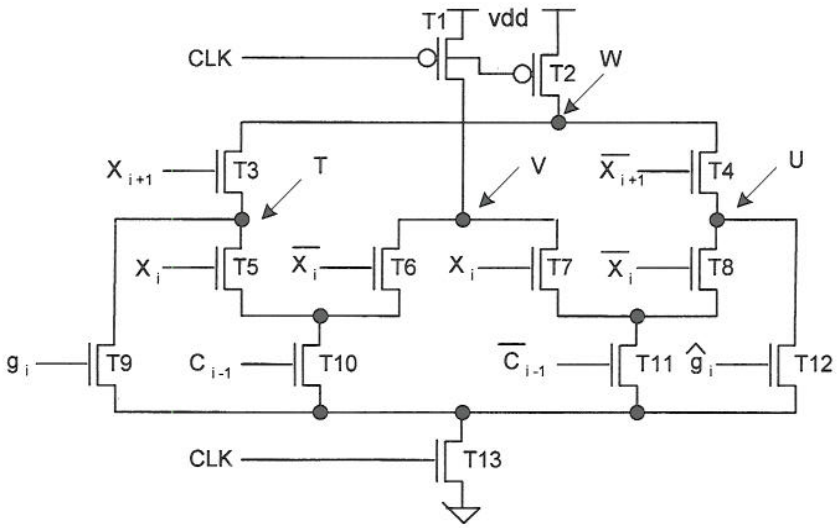


Figure 3.1

4. a) *Figure 4.1* shows the gate-level circuit diagram of a finite state machine with one primary input `IN` and one observable primary output `OUT`. Find a sequence of inputs that will detect a stuck-at-0 (S-A-0) fault on the $\overline{Q}$ output of the upper flip-flop. Assume the existence of a master reset which initially resets all D flip-flops to 0.

[7 marks]

b) Draw the state diagram for this circuit. Hence or otherwise, explain how a S-A-0 fault on the output of gate 1 can be detected.

[7 marks]

c) Describe scan-path design. Explain how the scan-path technique could help in testing the two faults in (a) and (b).

[6 marks]

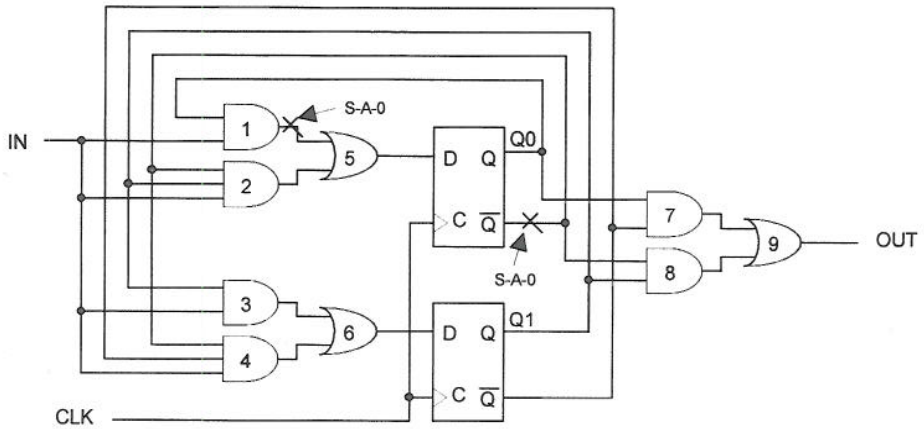


Figure 4.1

5. *Figure .5.1* shows part of the driver and switching circuit of a digital to analogue converter. Transistors T1 to T4 form the differential driver for the current steering switches T5 and T6. The sizes of the transistors are: T1 and T2, 1.5µ (W) x 2.0µ (L); T3 and T4, 3.0µ x 2.0µ; T5 and T6, 20.0µ x 0.25µ. The outputs I_{out} and $\overline{I_{out}}$ are expected to be connected to external resistors. The inputs D and $\overline{D}$ are complementary signals.

   a) Explain how the differential driver circuit works and the expected effect of using only N-channel transistors T1-T4 for the differential driver circuit.

   [6 marks]

   b) What are the important criteria when designing the layout of such a circuit for a mixed signal design? Design a good layout for T1 to T6 that would be suitable for use in a DAC circuit. Your layout design should have roughly the correct transistor dimensions. Label your layout design by marking all the transistors and signal terminals. (There is no need to design the layout for the current source S1.)

   [14 marks]

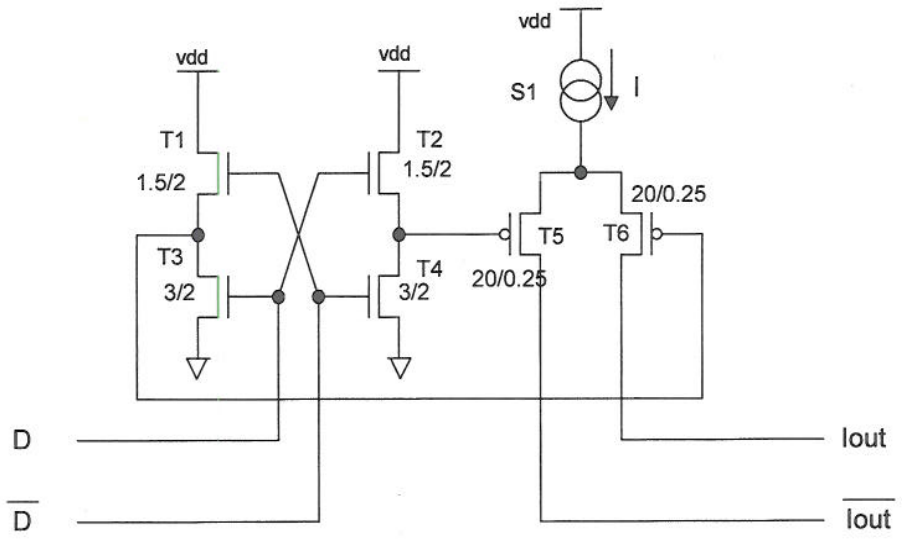


Figure 5.1

6. a) A thirteen-stage ring oscillator is used to calibrate the speed of a CMOS fabrication process. The inverters used in the ring oscillator are all minimum size with p and n transistor widths of 0.3 μm and 0.15 μm respectively. Two complementary outputs are connected to output pads: *clk* and *clkbar*. Each output pad is presenting a load of 6 minimum size inverters. The measured oscillation frequency is 400MHz.

Using the Method of Logic Effort, or otherwise, estimate the delay of a minimum size inverter driving an identical inverter.

[6 marks]

b) *Figure 6.1* shows the circuit for a two phase non-overlapping clock generator. All the inverters are minimum size, and all the transistors used in the NAND gate have a width of 0.3 μm.

By considering the delay from A to B and assuming that both Φ1 and Φ2 outputs are loaded with identical loads, estimate the time between Φ1 going low and Φ2 going high.

[9 marks]

c) For the circuit shown in *Figure 6.2*, find test vectors that can locate stuck-at faults at nodes P and Q.

[5 marks]

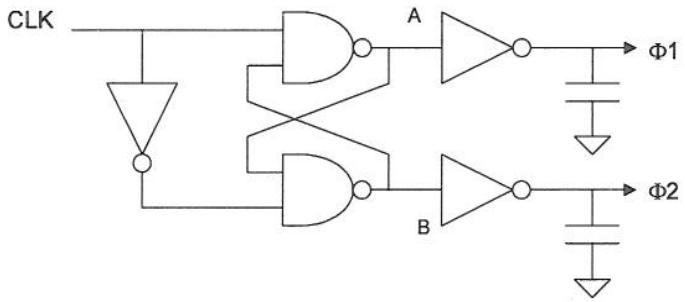
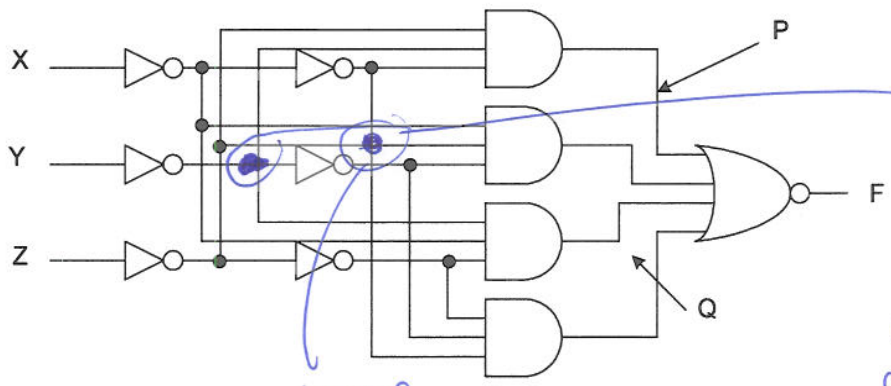


Figure 6.1



announced at 4.20 and at about 4.35 on level 6

ignore

Figure 6.2

Colour Supplementary Sheet

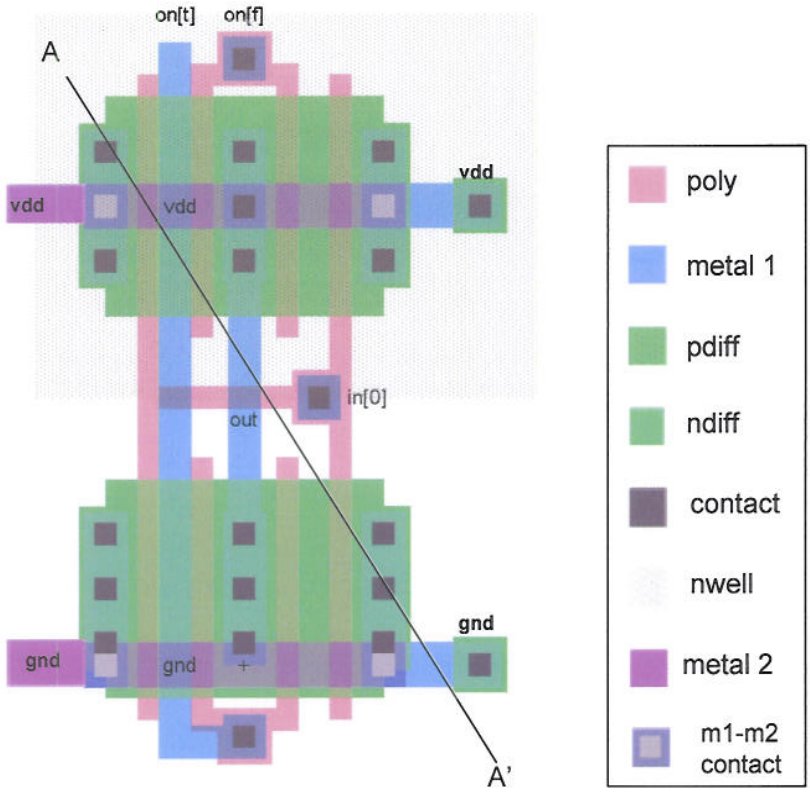


Figure 1.1 Layout of full-custom cell P for Question 1

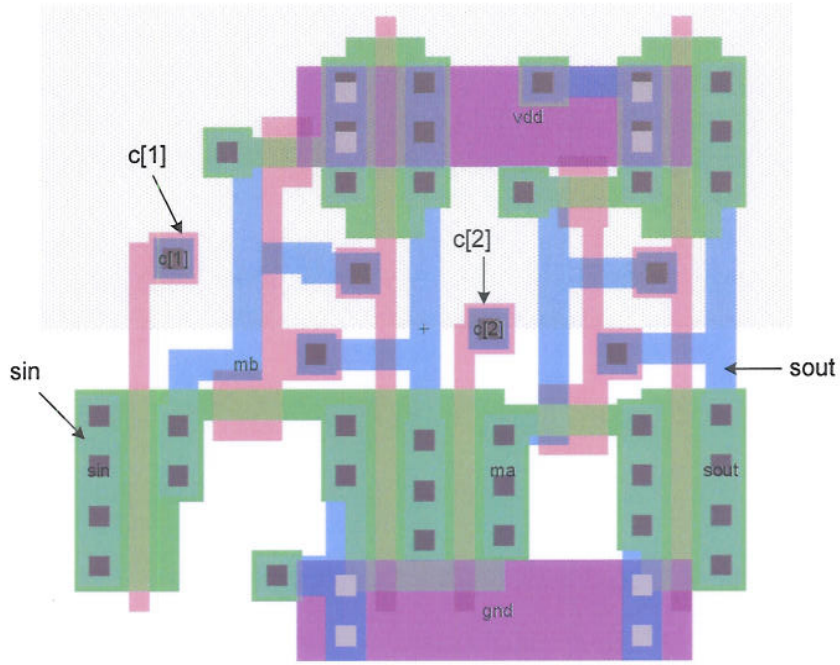


Figure 1.2 Layout of full-custom cell Q for Question 1

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UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
M.Eng. and A.C.G.I. EXAMINATIONS 2007

PART IV

INTRODUCTION TO DIGITAL IC DESIGN

SOLUTIONS

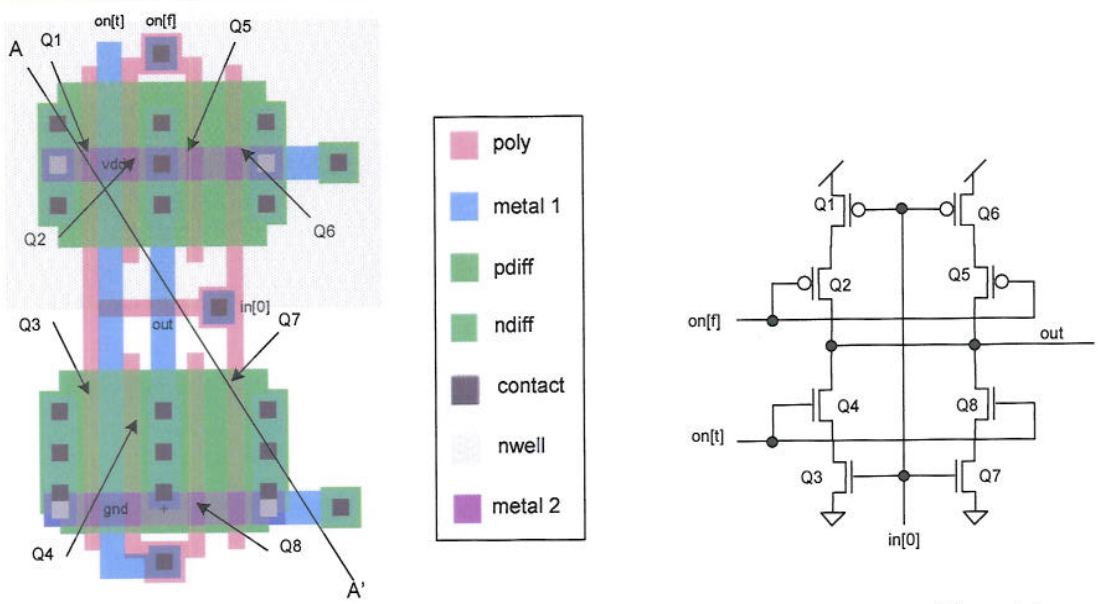
This is an open-book examination.

You may need red, green, blue, yellow and black coloured pens.

First Marker: *Peter Cheung*
Second Marker: *Christos Bouganis*

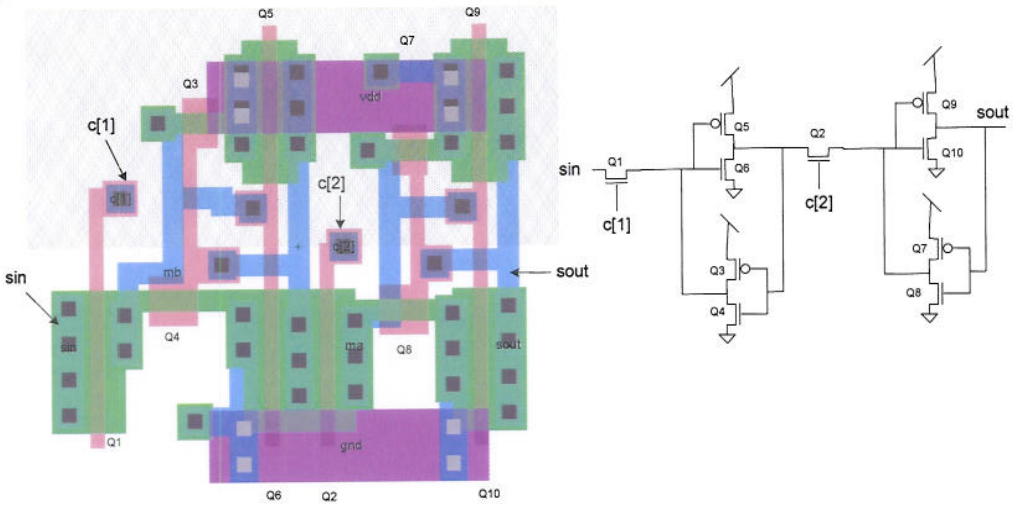
Solution to Question 1

a) This question tests student's ability to understand a full custom layout. Both P & Q are from a JTAG design library.



[4 marks]

b)

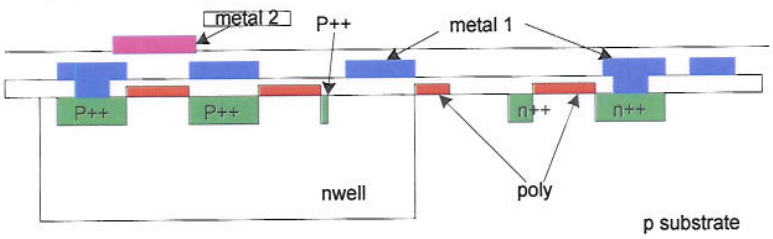


[6 marks]

c) Q1 = Q2 = 20 x 2; Q3 = Q7 = 3 x 5; Q4 = Q8 = 3 x 7; Q5=Q6=Q9=Q10 = 20 x 2.

[3 marks]

d) This part of the question tests student's ability to relate the layout to the physical process and different layers on the chip.



[7 marks]

Solution to Question 2

a) The addr_clock signal precharge the decoder circuit node X. The predecoder provides decoding for each pair of address bits (e.g. addr0 & addr1, addr2 & addr3, addr4 & addr5), which are then ANDed together. T6 provides weak feedback to ensure that this circuit is static (i.e. in the absence of an address clock, a high level in X is maintained).

[2 marks]

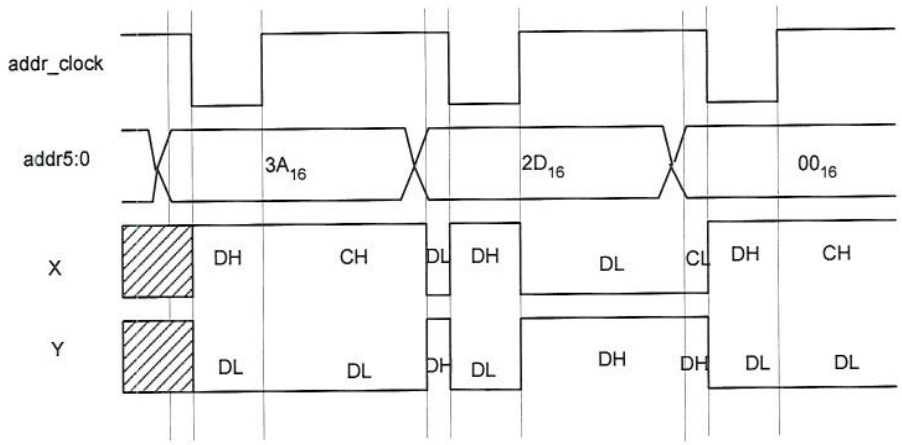
b)

0x2D = 101101B. One possible solution is:

in1 = addr0 & !addr1
in2 = addr2 & addr3
in3 = !addr4 & addr5

[4 marks]

c)



[4 marks]

d)

The layout depends on student's design.

[10 marks]

Solution to Question 3

(a)

In precharged circuits, output and intermediate nodes are charged to either a high or low logic level on one phase of the clock signal. On the other phase of the clock (the evaluate phase), the transistor tree (either n-tree or p-tree) evaluate the logic function. The advantages of this type of circuits are: 1) it is guaranteed that there are no direct path from VDD to GND even during transient; 2) unlike normal CMOS designs, only half the number of transistors are needed; 3) it is generally faster than having both active p-tree and n-tree. The disadvantage is that you need a clock and therefore can incur extra latency.

[4 marks]

(b)

The principle here is very similar to Manchester carry adder. x_i is essentially the propagate signal p_i. Therefore

$$\overline{T} = g_i + p_i \bullet c_{i-1}$$

which is effectively the next stage carry c_i.

$$\overline{V} = c_{i-1} \bullet \overline{x_i} + \overline{c_{i-1}} \bullet x_i$$

Therefore it is really

$$\overline{V} = x_i \oplus c_{i-1} = a_i \oplus b_i \oplus c_{i-1}$$

which is the sum of the ith bit.

[8 marks]

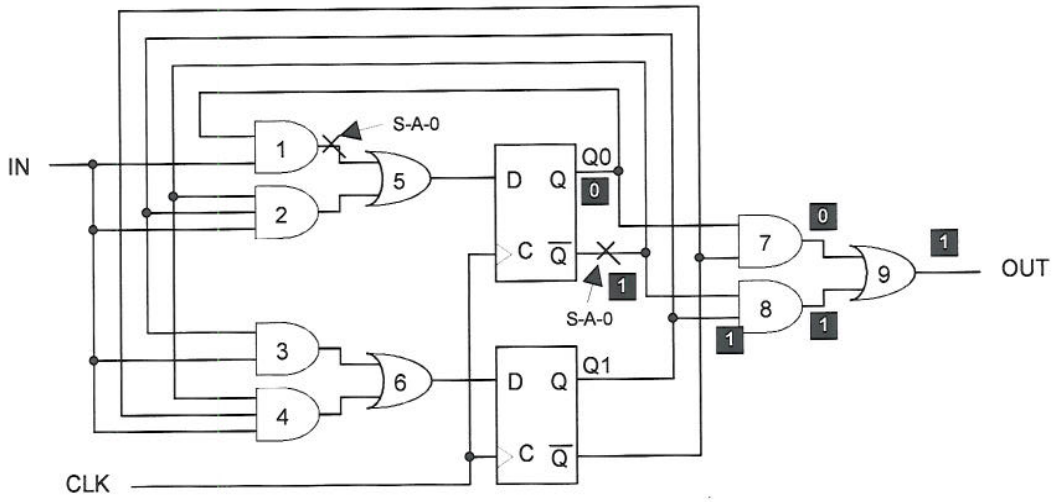
d)

The layout depends on student's design.

[8 marks]

Solution to Question 4

a)

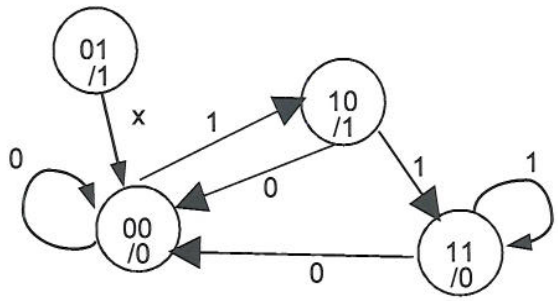


A fault on 1st input to gate 4 is the same as a fault on the Qbar output (/Q0) of the top latch. To test for a S-A-0 fault, we must force /Q1 to 1. For this to be observable at the output, Q1=1 and Q0=0. Assume that the FFs are reset to 0 initially, we must force the state machine to sequence to this state. To do this:

in = (1 1) and out=1 if no fault, otherwise faulty.

[7 marks]

b)



A S-A-0 fault at output of gate 1 can be tested by the following:

In order to force this node to be a 1, the machine must be in state Q1:Q0=1:1. This is possible as 1:1 is a valid state. Then keeping IN=1 and clock again will result in:

Q1:Q0 = 1:0, OUT = 1 if S-A-0 fault on gate 1
Q1:Q0 = 1:1, OUT = 0 if no fault on gate 1

[7 marks]

c) Students are expected to explain what is scan-path design. With scan-path latches, the test in (a) is trivial to generate. We simply strobe in the pattern Q0=0 and Q1=1, and observe the output. For S-A-0 fault in 1, we simply force the latches to 1:1 and IN=1, and clock the latches once, then strobe the data out serially.

[6 marks]

Solution to Question 5

a) The differential driver circuit is effectively a cross-coupled RS flip-flop. Assuming D=0, T2 and T3 are OFF, T1 and T4 are ON. Therefore T5 is conducting and T6 is not conducting. When D goes from 0 to 1, T1 and T4 turn OFF and T2 and T3 turn ON, and the steering switches will reverse. Using n-channel only devices provides two effects:

1. output swing is reduced by Vt, therefore reducing the switching coupling to the output terminals.
2. Pull-down will work faster than pull-up, therefore ensuring that the steering switches are "make-before-break".

(This part of the question is actually quite hard).

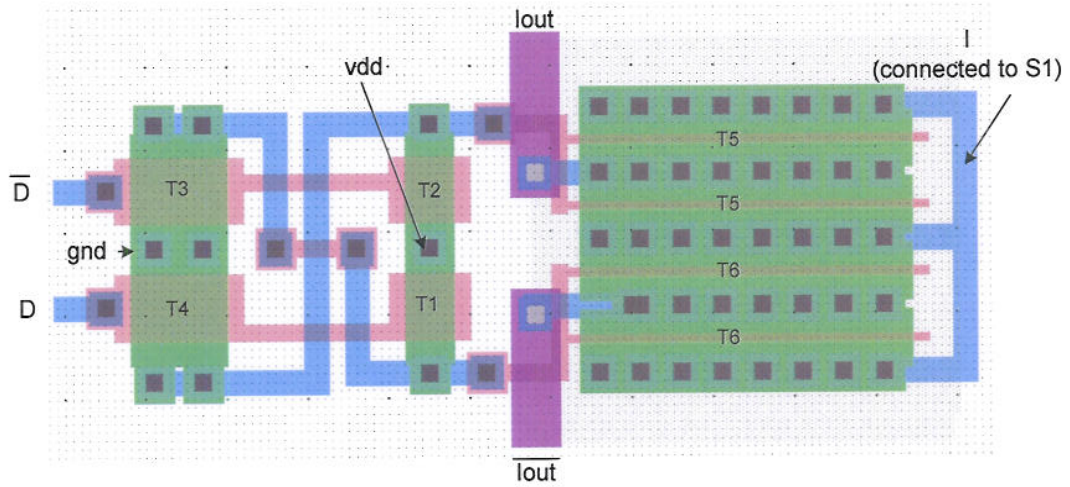
[6 marks]

b)

i) Isolate as much digital switching noise as possible.
ii) Maintain symmetry of signals everywhere.
iii) Avoid unnecessary overlaps of signals.
iv) Guard rings.

[4 marks]

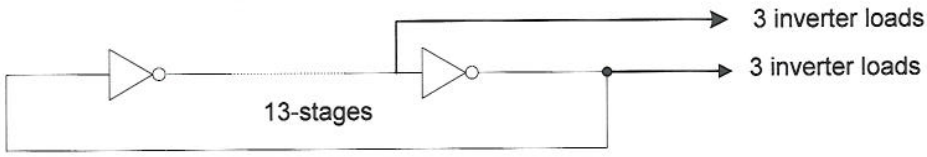
Here is one possible layout from a real layout of such a circuit. Note the symmetry of the layout and the folder T5 and T6.



[10 marks]

Solution to Question 6

a) This question is based on a method developed by Ivan Sutherland for estimating delay & size of transistors in a CMOS circuit known as the Method of Logic Effort.



Since oscillation frequency is 400MHz, the loop delay of the ring oscillator is around 1.25ns.

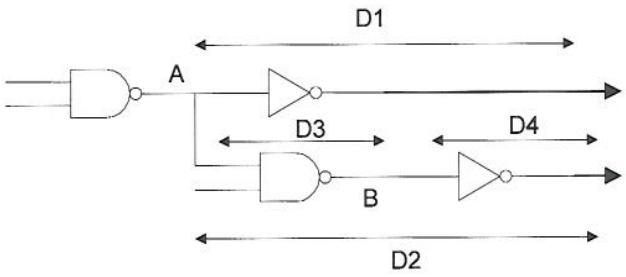
Note that it does not matter where clk and clkbar are taken out to output pads, the logical efforts round the loop remains the same. The load seen round the loop is still 13+6+6 = 25 unit delay.

Total delay round loop = 1.25 ns $\approx 25 * \tau_{inv}$

Therefore $\tau_{inv} = 50$ ps.

[6 marks]

b)



Non-overlap = D2 - D1. D2 = D3+D4. Since D1 = D4 (since both drive the same load), there non-overlap is simply D3.

Assuming parasitic delay for inverter $\approx 0.6\ \tau_{inv}$

D3 = logical effort x electrical effort + parasitic delay

$= \tau_{inv} * [(4/3) \times (1+4/3) / (4/3) + 2\text{x } 0.6]$

$\approx 3.53 * \tau_{inv}$

≈ 176.5 ps.

[9 marks]

c)

P s-a-0: (1 0 0 0) for x, y, z and F
P s-a-1: (0 0 0 1) for x, y, z and F

Q s-a-0: (0 0 1 0) for x, y, z and F
Q s-a-1: (0 0 0 1) for x, y, z and F

[5 marks]