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AC3
ISE4.19

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2010

MSc and EEE/ISE PART IV: MEng and ACGI

INTRODUCTION TO DIGITAL INTEGRATED CIRCUIT DESIGN

Friday, 7 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung
Second Marker(s) : C. Bouganis

Information for Invigilators:

Students may bring any written or printed aids into the examination.

Information for Candidates:

Students may need red, green, blue, yellow and black coloured pens.

1. a) *Figure 1.1* (see the colour supplementary sheet) shows the layout of an n-well CMOS circuit with five terminals: `A`, `B`, `C`, `X` and `Y`. Extract and draw the transistor-level schematic diagram for this circuit. Note that the supply signals are labelled as `Vdd` and `Gnd`.

   Given that the transistor labelled T1 is of size $16\lambda \times 2\lambda$, label all transistors in this circuit with their sizes.

   [8 marks]

   b) What function does this circuit perform? Provide a brief description on how this circuit works.

   [4 marks]

   c) For the layout shown in *Figure 1.1*, draw the vertical cross section along the lines `PP'` and `QQ'`. Label your diagram indicating the n-well region and the different types and levels of doping (e.g. p^-, n^+ etc).

   [8 marks]

2. a) In light of the experience you gained from the design project, describe the proper procedure for designing a full-custom integrated circuit. Highlight any lessons you learned from the design project.

   [8 marks]

   b) *If you worked on the digital biquad filter chip:*

   (i) Draw a diagram showing the hierarchy of the cells used in your design.
   (ii) Describe the control timing for the biquad filter clearly showing the number of clock cycles required to compute one output value.
   (iii) Explain what special action needs to be taken during the last clock cycle in computing an output value.

   If you worked on the media filter chip:

   (i) Draw the floorplan of the chip showing the relationship between various modules, showing their approximate size.
   (ii) Explain the test method used in order to verify the correctness of your design.
   (iii) Describe your personal contributions to the project.

   [12 marks]

3. a) Discuss briefly the advantages and disadvantages of the following three logic design styles:

   (i) Static CMOS logic
   (ii) Pre-charged CMOS logic
   (iii) Complementary pass-transistor logic

   [6 marks]

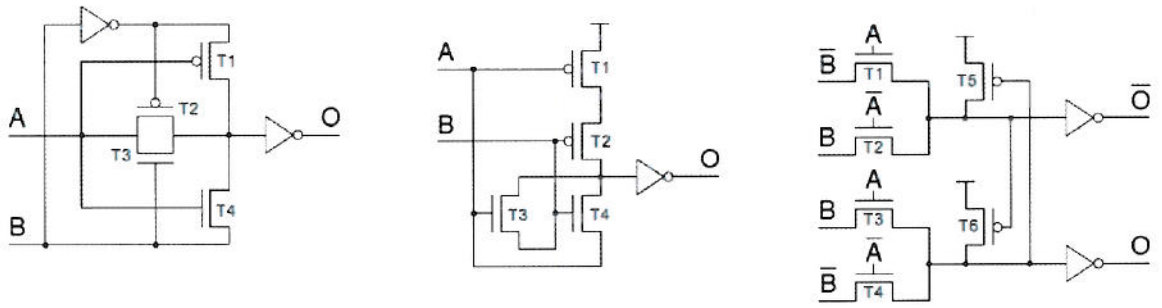
   b) Figure 3.1 (a), (b) and (c) shows three different ways of implementing the same 2-input logic function.

   (i) Determine the Boolean relation between output O and inputs A and B.
   (ii) Briefly explain how each circuit works.
   (iii) Compare and contrast these three different methods of implementation with each other and with the conventional CMOS logic style.

   [8 marks]

   c) Design the layout of all three circuits in the form of stick diagrams.

   [6 marks]



(a) (b) (c)

Figure 3.1

4. a) Explain and compare the following four flip-flop clocking strategies:
   i) Non-overlapping two phase clocking
   ii) True single-phase clocking
   iii) Pulse-triggered clocking
   iv) Double-edge triggered clocking

[6 marks]

b) Figure 4.1 shows a high-speed flip-flop circuit used in a processor chip. With the help of timing diagrams, explain how this circuit works. What are the advantages and disadvantages of such a flip-flop circuit?

[7 marks]

c) Figure 4.2 shows the design of a double-edge triggered flip-flop. With the help of timing diagrams or otherwise, explain how this circuit works. What are the advantages and disadvantages of such a flip-flop circuit?

[7 marks]

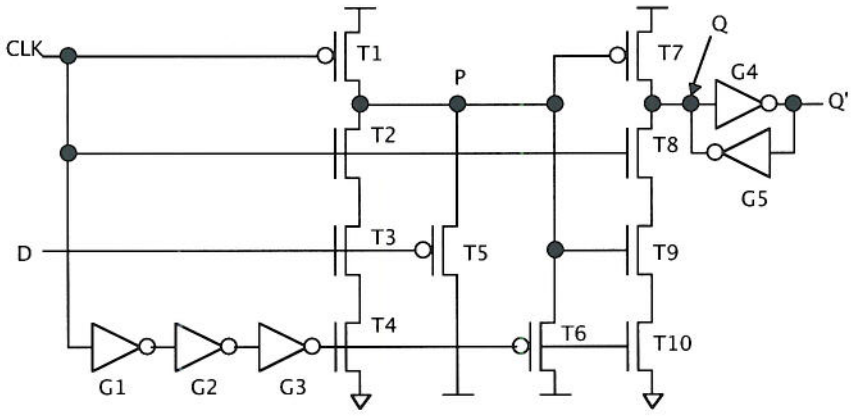


Figure 4.1

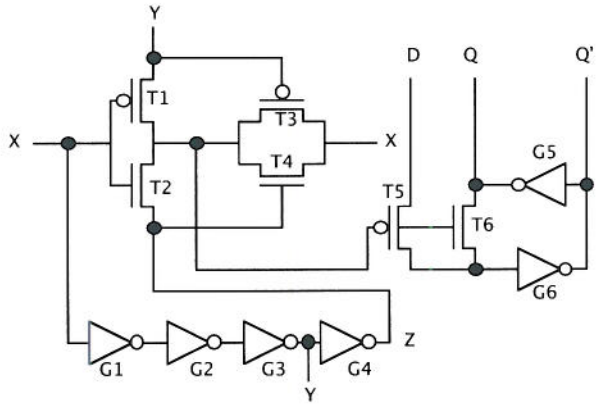


Figure 4.2

5. a) Figure 5.1 shows the gate level circuit diagram for a four-state sequential circuit with one primary input *IN* and one observable primary output *OUT*. Find a sequence of inputs that will detect a stuck-at-0 (S-A-0) fault on the $\overline{Q}$ output of the upper flip-flop. Assume the existence of a master reset, which initially resets all D flip-flops to 0.

[8 marks]

b) Draw the state diagram for this circuit. Explain why a S-A-0 fault on the output of gate 1 is hard to test.

[5 marks]

c) What is a scan-path design? Explain how the scan-path technique could help in testing the two faults in (a) and (b).

[7 marks]

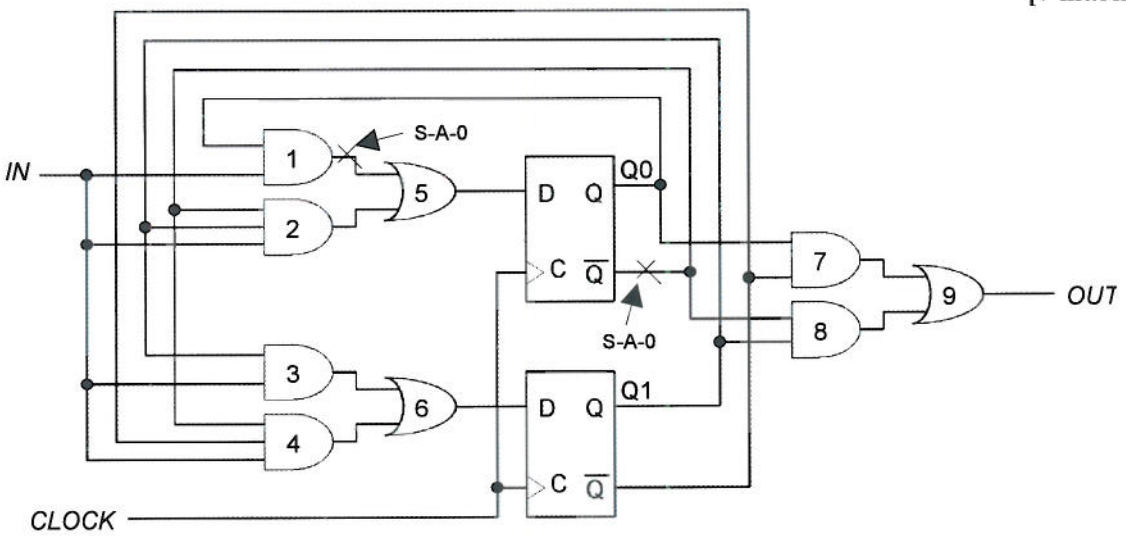


Figure 5.1

6. A bit-serial adder circuit takes two inputs *A* and *B* as serial data with least significant bit first, and produces the sum output serially on each clock cycle, also with least significant bit first. Figure 7 shows a functional block diagram of the bit-serial adder along with its timing diagram. A synchronisation signal *LSB* is normally low but goes high when the least significant bits of *A* and *B* are applied. The clock signal *CLK* determines the bit period of the bit-serial data. All signal transitions occur on or shortly after the rising edge of *CLK*.

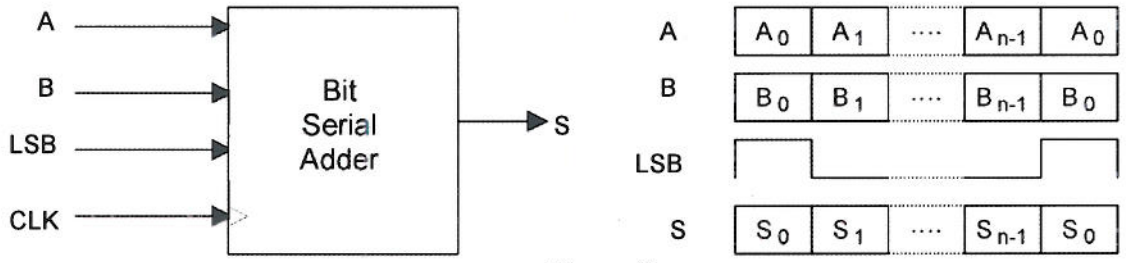


Figure 7

Design a transistor-level circuit to implement this bit-serial adder.

[20 marks]

Colour Supplementary Sheet

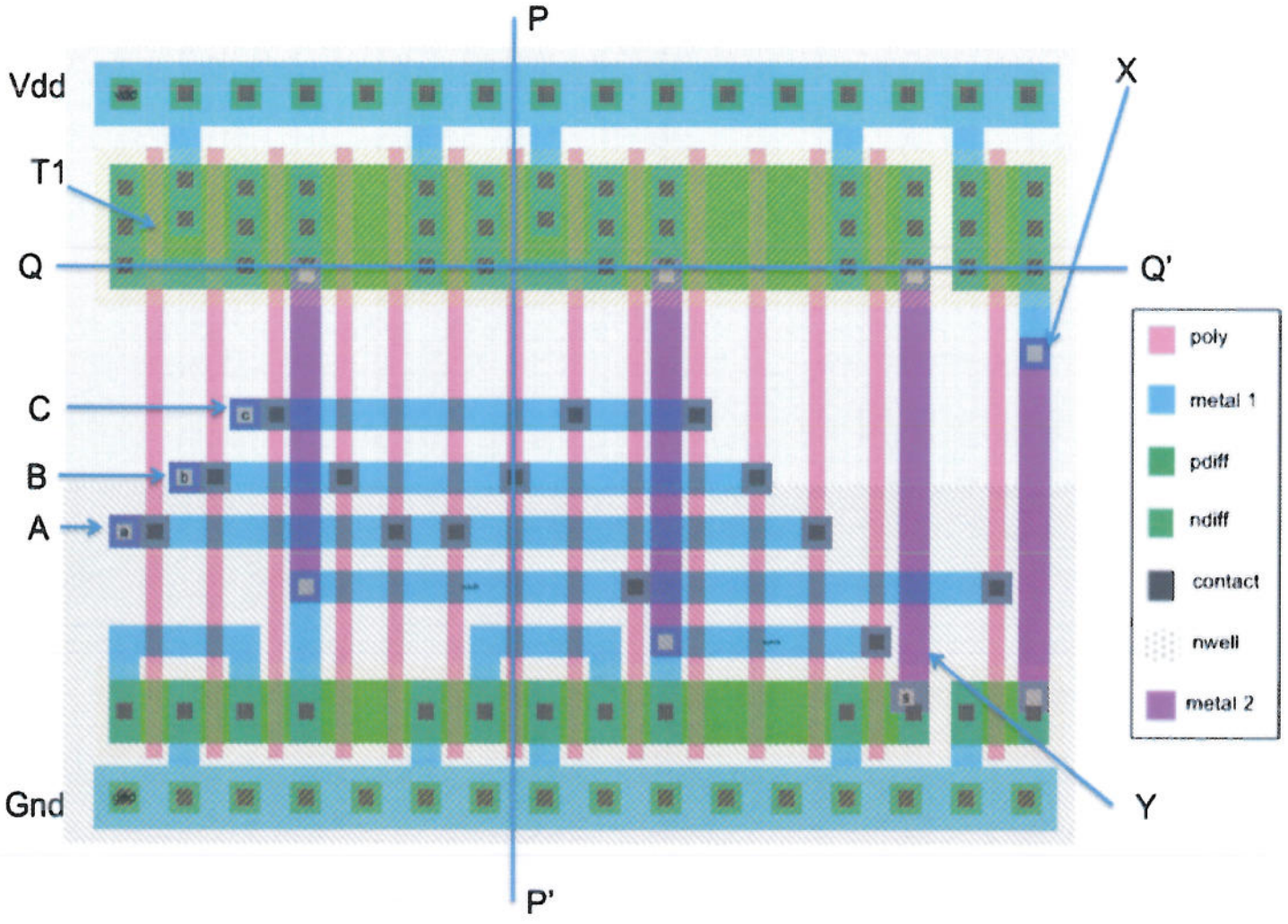


Figure 1.1 Layout of full-custom cell for Question 1

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PART IV

INTRODUCTION TO DIGITAL IC DESIGN

SOLUTIONS

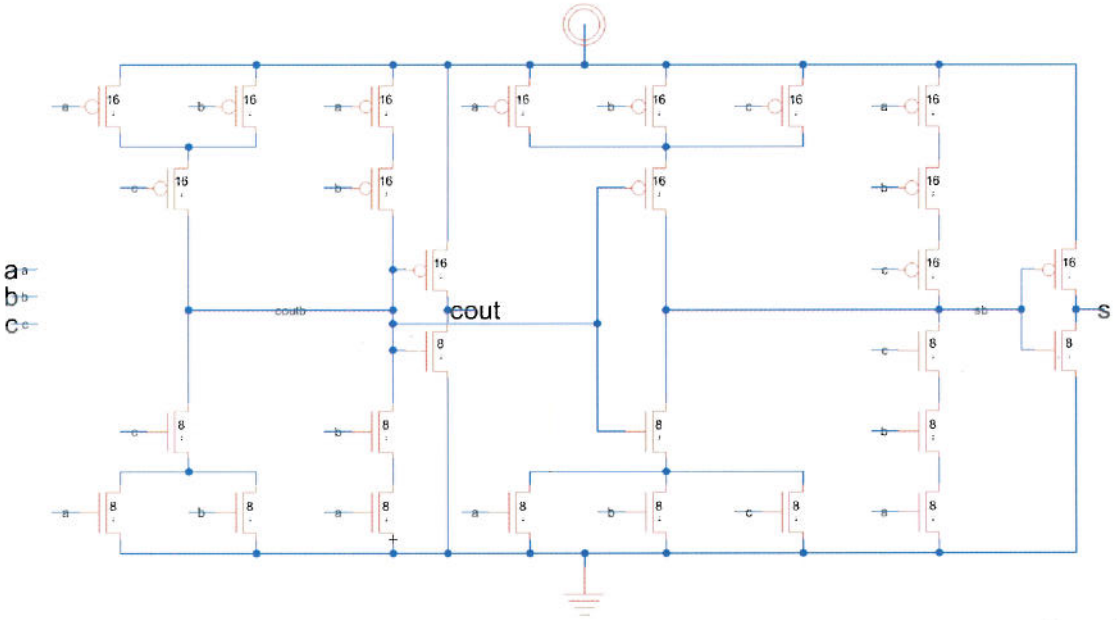
This is an open-book examination.

You may need red, green, blue, yellow and black coloured pens.

First Marker: *Peter Cheung*
Second Marker: *Christos Bouganis*

Solution to Question 1

a) This question tests student's ability to understand a full custom layout. The extracted circuit should be:



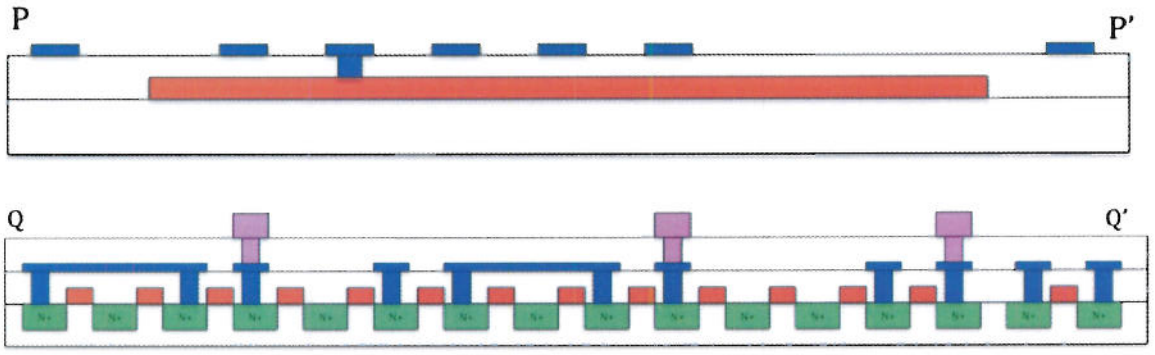
[8 marks]

b) This circuit implements symmetrical full adder. A, B and C are the three adder inputs. X is the carry output and Y is the sum output.

[4 marks]

c) This part of the question tests student's ability to relate the layout to the physical process and different layers on the chip.

[8 marks]



Important points to note:

- No diffusion underneath the poly gates
- Poly to M2 needs to go through M1 layer

Solution to Question 2

Each student was involved in a group design project during the course. Since they were learning while doing the project, a number of mistakes were made. The question is intended to test how much each student learned through this experience.

a) The following are some of the points expected to be discussed in student's answer.

- Clarify specification of the project right from the start, avoid changing spec during design.
- Adhere to top down design approach as much as possible. Model chip behaviourally to verify chip function.
- Careful floorplanning early on for the entire chip.
- For cell based designs (such as the media filter chip), define cell boundary, size and terminal locations early.
- Use auto-place and route tools if available (not available with Electric tools).
- Consider test right at the beginning of the design. Design a good test vector set, and use it for retrospective verification each time a change is made to the circuit (regressive testing).
- Maximize regularity and minimize different types of cell designs.
- From floorplan obtain the most complex cell and pitch-match as much as possible.
- Hierarchical design, both simulation and layout. But avoid excess use of hierarchy.
- Verify layout from simulation if necessary.

[8 marks]

b) This part of the answer provides an opportunity for each student to demonstrate their individual contribution to the project and show their understanding. The answers will depend on which project was chosen. I expect a student who did not really put that much effort into this project will not be able to provide good answers to this part.

[12 marks]

Solution to Question 3

This question tests students understanding of different logic design styles. The material from this question is derived by the paper: "Low-Power Logic Styles: CMOS versus Pass-Transistor Logic", Reto Zimmermann and Wolfgang Fichtner, IEEE Trans. on Solid-State Circuits, 31 (7), 1997.

a)

i) Static CMOS logic:
+ simple to design; always restoring logic level; relatively immune to variation to vdd and other factors
- can be slow; not low power; can be larger than need to be

ii) Pre-charged CMOS logic;
+ smaller than static CMOS; can be fast
- Need a clock; susceptible to noise and other variability problems

iii) Complementary pass-transistor logic
+ can be very fast; small, particularly for exclusive gates
- needs double the transistor counts; would not scale to smaller geometry due to threshold voltage drop

[6 marks]

b)

i) O = A XOR B

ii) (a) is a straight forward pass-transistor XOR implementation. (b) is another pass-transistor implementation of XOR (known as the Wang's XOR). Note when A and B are high, how T3 and T4 pull the output to '1' not '0'! (c) is Yano's complementary pass transistor (CPL) XOR, as covered in lectures.

Students are expected to demonstrate the correct function at O by examining the four combinations of A and B.

iii) Conventional pass-transistor XOR is very commonly used. Simple and generally works well. Compared to CMOS, it is a lot smaller, but may have charge-sharing problem – can be difficult to simulate correctly using SPICE or timing simulators.

Wang's XOR is smaller than all the others, but this circuit is quite slow (no real pull-down inside XOR) and does not scale to smaller geometry.

CPL is very fast and low power. It is large and can scale to smaller geometry.

All these circuits have lower dynamic power than conventional CMOS.

[8 marks]

c) Layout design depends on individual student. I expect good layout with sensible and clearly defined terminals.

[6 marks]

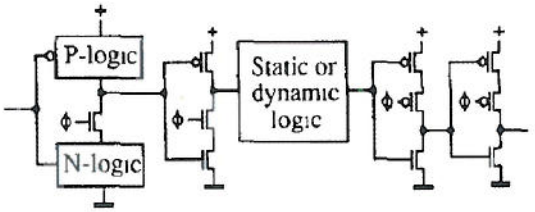
Solution to Question 4

This question test students' understanding of clocked circuits and flip-flops. Part b) of this question is derived from the paper: "Circuit Techniques in a 266-MHz MMX-Enable Processor" by Draper et al, IEEE JSSC, 32 (11) 1997. Part c) is derived from the paper: "A Single Latch, High Speed Double-Edge Triggered Flip-Flop", TA Johnson, IS Kourtev, Proceedings of the 8th IEEE International Conference on Electronics, Circuits and Systems, 2001.

a)

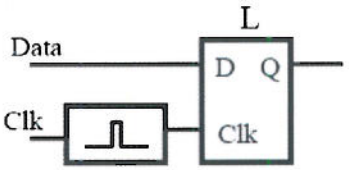
i) Conventional two clock signals, phi_1 and phi_2, where neither clock signals is ever high together, hence "non-overlap". Can be very slow and need to route many clock signals. Suffer from clock skew problem, which need to be compensated by increasing the non-overlap period, which makes circuit even slower. Old method, not used in modern IC designs.

ii) TSPC use only one clock signal. Example of this circuit from notes is (originally proposed by Yuan and Svensson in "High-Speed CMOS Circuit Techniques", IEEE JSSC 24(1) 1989):



This method is immune to clock skew and only need to route a single clock. Can combine latching with logic function (see notes and/or paper). Used extensively in fast processor designs.

iii) Generate pulse from clock edge, than use transparent latch triggered by the pulse. Idea (from notes):



Also used in fast processor designs, this latch is also immune to clock skew problem. Also pulse designed can reduce timing problem and race problems, but increases hold time requirement.

iv) A double-edge trigger flip-flop uses a pulse detector on both rising and falling edge, and register data on both edges of the clock. (Sometimes this is called double pumping in double date rate (DDR) circuits.) Its advantage is to have higher data rate with a lower clock signal. The disadvantage is that it could be a more complex circuit than pulse-trigger FF.

[6 marks]

b)

This is also known as an Edge-Trigger Latch (ETL). It employs a precharged node, P, and a clock-derived, integrated one-shot which provides a transparency period. During this period, the data is sampled into the latch. The transparency period, defined by inverter chain G1–G3 is typically about 250 ps in this design, and provides an attractive attribute of level-sensitive

latches: data can arrive at the latch even after the assertion of the clock. This attribute allows for time-borrowing or slack passing, or alternatively, can be thought of as minimizing the effects of clock uncertainty on cycle time. The transparency period, though advantageous, causes an increase in the hold time, requiring a detailed hold timing analysis to avoid a timing failure.

[7 marks]

c)

This is also known as a double-edge triggered FF (DETFF).

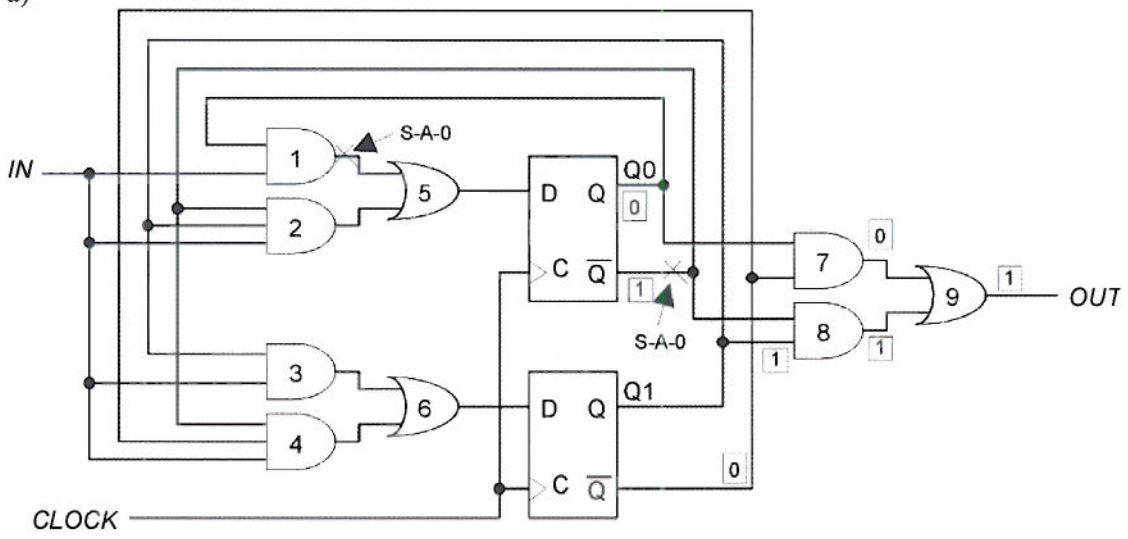
The clock drivers G1 to G4 is essentially a delay line for the clock signal CLK

X. If each inverter G1 through G4 is assumed to introduce a delay ti, then the signals Y and Z are delayed from the clock signal X by 3τ and $4\ \tau$ respectively. The clock driver is used to provide these delayed clock signals to the exclusive-or (XOR) gate consisting of the transistors T1 through T4. Had the signals X, Y, and Z not been delayed at all, the output of the XOR gate would have been a constant logic one (1). Because of the 3τ delay between the signals X and Y, however, there is a short period of time after each clock signal transition where X=Y (Y has not changed yet). During this short period of time the XOR gate outputs a logic zero thereby turning on T5 and cutting off T6. The latch at the right will be temporarily transparent and the input D will have a direct path to the output Q.

[7 marks]

Solution to Question 5

a)

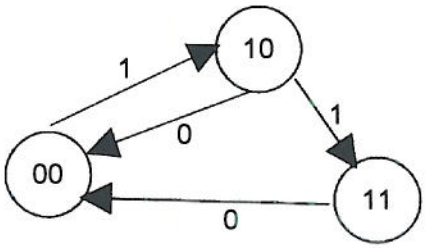


A fault on 1st input to gate 4 is the same as a fault on the Qbar output (/Q0) of the top latch. To test for a S-A-0 fault, we must force /Q1 to 1. For this to be observable at the output, Q1=1 and Q0=0. Assume that the FFs are reset to 0 initially, we must force the state machine to sequence to this state. To do this

in = (1 1) and out=1 if no fault, otherwise fault.

[8 marks]

b)



A S-A-0 fault at output of gate 1 would be hard to test because:

1) In order to force this node to be a 1, the machine must be in state Q1:Q0=1:1. There is no direct path to this state.
2) Even when this state is reached, the fault must be propagated to Q0. Unfortunately with Q1:Q0=1:1, this fault is masked by the lower input to gate 7.

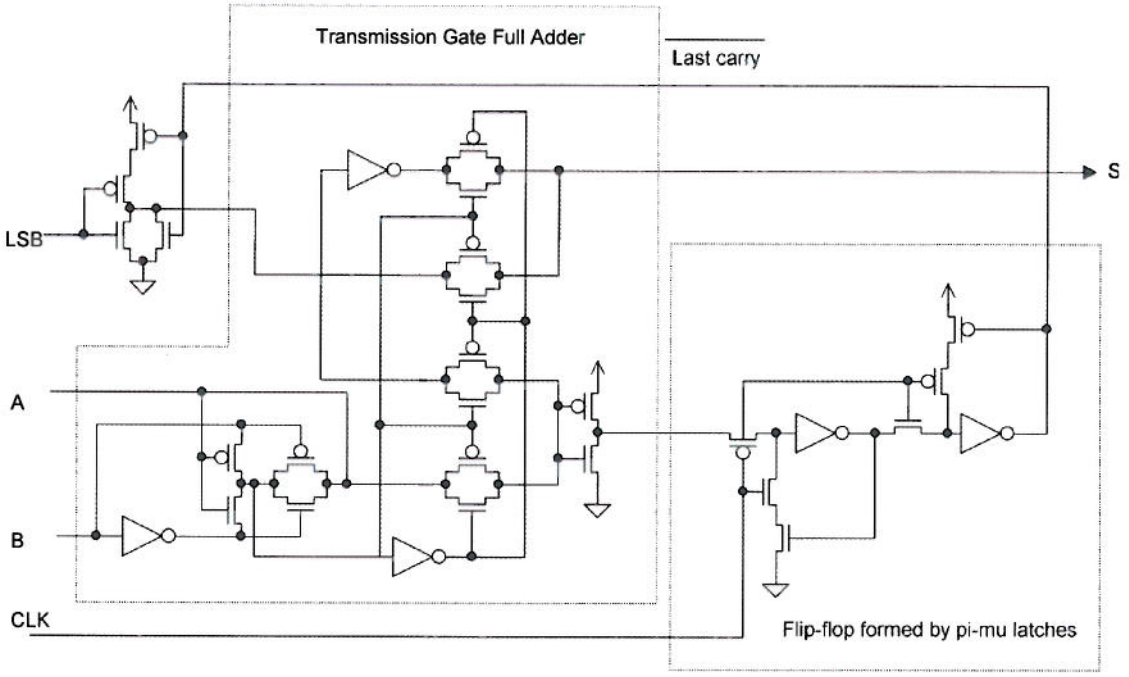
[5 marks]

c) Students are expected to explain what is scan-path design. With scan-path latches, the test in (a) is trivial to generate. We simply strobe in the pattern Q0=0 and Q1=1, and observe the output. For S-A-0 fault in 1, we simply force the latches to 1:1 and IN=1, and clock the latches once, then strobe the data out serially.

[7 marks]

Solution to Question 6

The solution would depend on student's design. Here is a possible solution:



[20 marks]