IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2018

EEE/EIE PART I: MEng, BEng and ACGI

DIGITAL ELECTRONICS 1

Corrected copy

Monday, 11 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 each carry 30%.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : Z. Durrani
Second Marker(s) : C. Bouganis

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least-significant bit of a bus signal is labelled as bit 0, and the most-significant bit with the highest integer number. Therefore the signal X[7:0] is an eight-bit bus with X7 being the MSB and X0 the LSB.

In questions involving circuit design, you may use any standard digital circuits not explicitly forbidden by the question, provided that you specify fully their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

Question 1

1. a) (i) Prove using Boolean algebra:

$$A + \overline{A}B = A + B$$

[4]

(ii) Simplify the following expression using Boolean algebra.

$$\overline{A}BC + \overline{AB + AC}$$

[4]

b) Consider the following Boolean function:

$$f(A,B,C,D) = \prod(0,4,9,10,12)$$

with Don't Cares at 3, 5, 6, 7, 13, 14, and 15

(i) Using a Karnaugh Map, minimise this function in SOP format.

[4]

(ii) Using a Karnaugh Map, minimise this function in POS format.

[3]

c) Show how a 5-input NOR gate can be implemented using two multiplexers, each having two select inputs. You may assume that inverters are available to you.

[5]

d) Complete the missing entries, which are not shaded in the following table. No marks will be awarded for this question unless you show how the solution is derived.

[6]

Decimal	Hexadecimal	Signed binary (8 bits wide)	Octal
256			?
-15		?	
	?		625

The question continues on the next page.

e) Draw the Moore state diagram for the circuit of Figure 1.1. Your diagram should consider all possible values of Q0, Q1 and Q2 in the circuit.

[6]

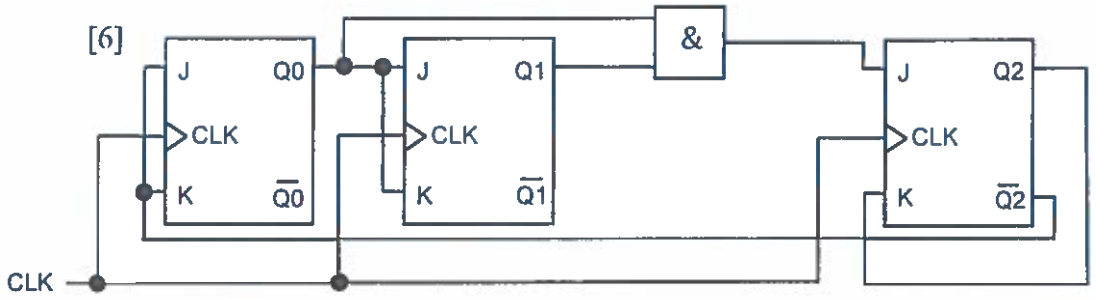

Figure 1.1

[6]

f) Figure 1.2 shows a clocked SR flip-flop:

i) Sketch the state diagram for this flip-flop.

[4]

ii) Hence, derive characteristic Boolean equations for next states Q^+ and $\overline{Q^+}$.

[4]

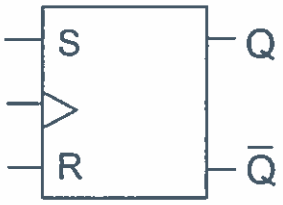

Figure 1.2

Question 2

2. a) Consider an odd parity generator, where a parity bit P is generated for four input bits A, B, C, and D. If all inputs are low, P shows a high value.

(i) Draw the truth table for this device, and hence find the SOP Boolean expression for P.

[4]

(ii) By using Boolean algebra, show that it is possible to transform the Boolean expression in (i) into an expression using only three two-input XNOR gates.

[6]

b) (i) Draw the timing diagram for the signals Y, Q0, Q1, Q2 and Q3 in the circuit below. Assume that the initial values of Q0, Q1, Q2 and Q3 are logic 0, and that any unconnected inputs in the clocked devices default to logic 1. The input Y is a 50% duty cycle square wave.

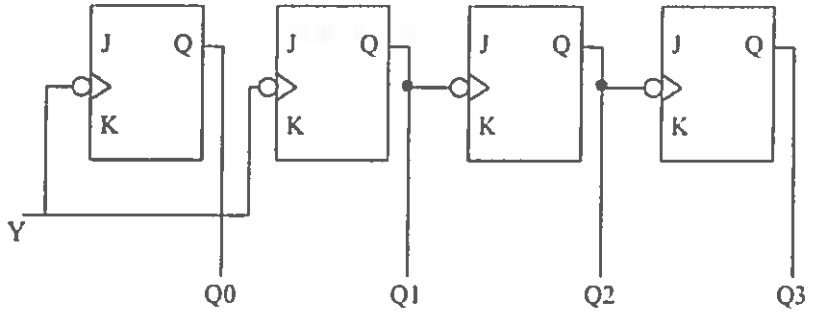

Figure 2.1

[4]

(ii) Show how the circuit of Fig. 2.1 can be used to generate the signal Z from the signal Y in the timing diagram shown in Fig. 2.2. If you use any additional gates and inverters, the number used should be kept to a minimum. Assume that Q0, Q1, Q2 and Q3 are initially at logic 0.

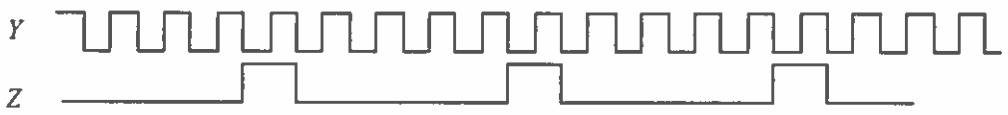

Figure 2.2

[6]

The question continues on the next page.

c) A 5× multiplier circuit is shown in Figure 2.3, where a signed (two's complement) binary input A[3:0] is multiplied by 5, to produce an N bit output, Z[N-1:0]. The circuit is to be designed based on shifts and additions of A[3:0].

(i) Find the minimum value of N required by this circuit. No marks will be awarded for this question unless you show how the solution is derived.

[4]

(ii) Hence, design and draw the circuit diagram of the 5× multiplier, using sign extension of A, four full-adders (FAs) and one half-adder (HA).

[6]

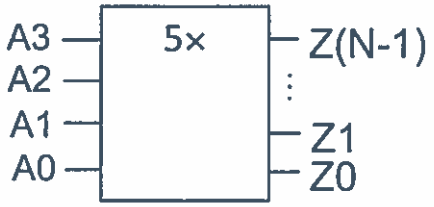

Figure 2.3

Question 3

3. Figure 3.1 shows a synchronous, up/down, 3-bit grey code counter implemented as a finite state machine (FSM). The counter counts up for input $UP / \overline{DN} = 1$ and counts down otherwise.

   a) Draw the Moore state diagram for the FSM.

   [8]

   b) Draw the state transition table for the FSM.

   [8]

   c) The FSM is to be implemented using D-type flip-flops and a combinational logic circuit. Determine minimal Boolean expressions necessary for this implementation.

   [10]

   d) Show how the FSM is to be connected using a block diagram. This should show the D-type flip-flops and interconnections but does not need to show the gate-level circuit.

   [4]

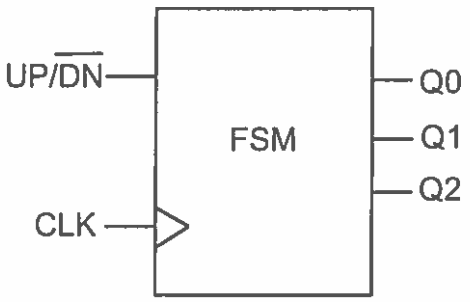

Figure 3.1

[THE END]