IMPERIAL COLLEGE LONDON

B.Eng, M.Eng and ACGI Examinations 2017
Part 1

Biomedical Engineering

BE1-HEE1 Electrical Engineering 1

Tuesday, 00 May 2017 **10.00-12.00**
Duration: 120 min

The paper has 4 questions.
Answer all 4 questions.
Each question is worth 100 marks.

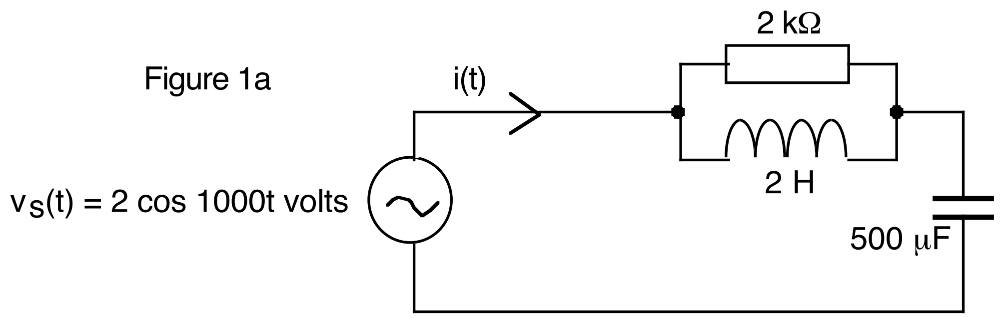
Marks for questions and parts of questions are shown next to the question. The marks for questions (and parts thereof) are indicative, and they may be slightly moderated at the discretion of the Examiner.

1

(a) The circuit of Figure 1a contains a sinusoidal voltage source of radian frequency 1000 and having a peak-to-peak amplitude of 4 volts.

Beginning with a phasor representing the voltage across the resistor, develop a dimensioned sketch of a phasor diagram showing all voltages and currents in the circuit. In this way find the amplitude of the sinusoidal current i(t) and its phase relation to the voltage $v_S(t)$ [30]

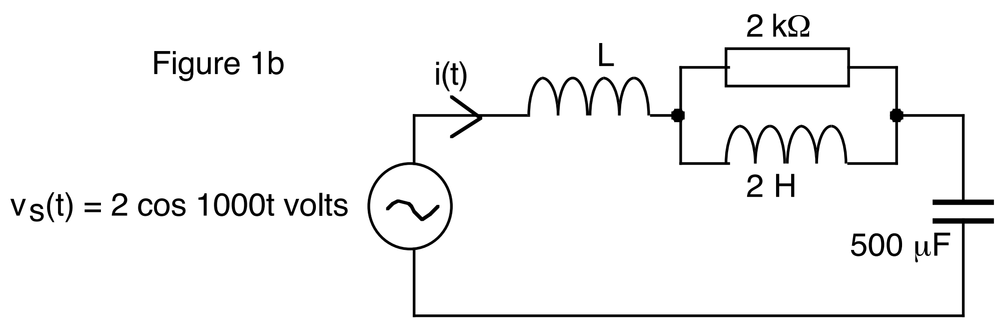
Figure 1a



(b) The circuit of Figure 1b is the same as that in Figure 1a except for an inductor L connected as shown.

By modifying the phasor diagram derived for the circuit of Figure 1a find the value of the inductor L that will ensure that vs(t) and i(t) are in phase. [45]

Figure 1b



(c) Based on the representation of voltages and currents by complex voltages and currents, and assuming the value of L found in part (b), calculate the impedance seen by the voltage source and check that it is commensurate with the condition that $v_S(t)$ and i(t) are in phase. [25]

2

(a) Draw the circuit diagram of an opamp-based logarithmic amplifier. It should contain one diode, one opamp and one resistor. Indicate clearly on your diagram the input and output voltages V_{in} and V_{out} respectivly. [15]

(b) For the circuit you have proposed in part (a) derive an expression relating V_{out} to V_{in}. [20]

Assuming that the resistor has a value of 1 kΩ , that the thermal voltage V_T = 25 mV and that the diode's reverse saturation current I_R = 1 pA, calculate the value of the output voltage V_{out} for V_{in} = 5 volts. [10]

(c) The circuit within the grey box in Figure 2 is designed to provide, across the load resistor R, an essentially constant voltage V of approximately 5 volts. It contains a 5 volt Zener diode.

If R = 60 ohms, what is the approximate value of V ? [10]

If R = 40 ohms, what is the approximate value of V ? [15]

What is the smallest approximate value of R for which V is maintained at approximately 5 volts? [15]

If the resistor R is disconnected (i.e., its value set to infinity) how much power is dissipated by the Zener diode? [15]

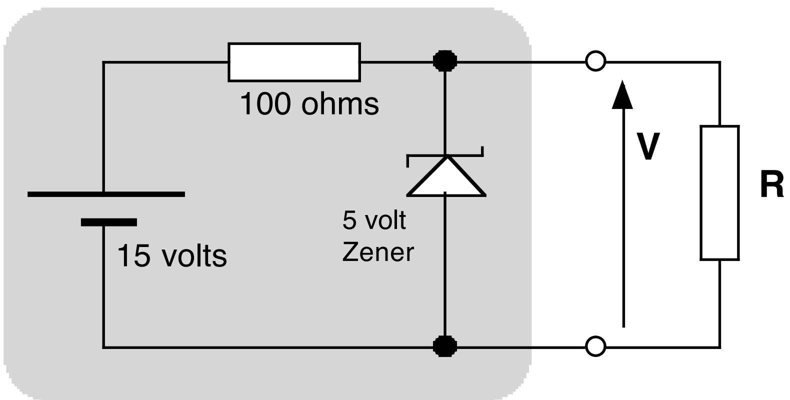


Figure 2

3

(a) Calculate the indicated voltage (**V**) or current (**I**) in each of the circuits (a) to (c) in Figure 3. .

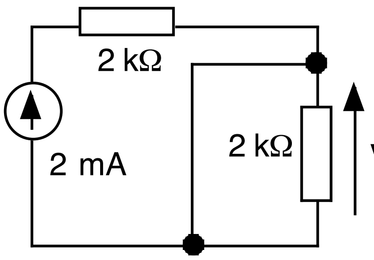


Figure 3a

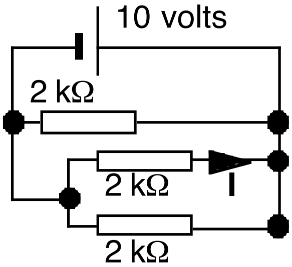


Figure 3b

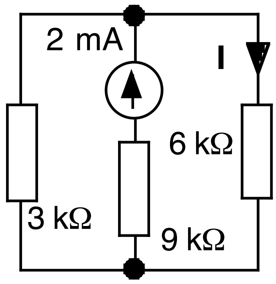


Figure 3c

[5]

[5]

[15]

(b) Use the Superposition Principle to find the voltage V in the circuits of Figures 3d and 3e

[25]

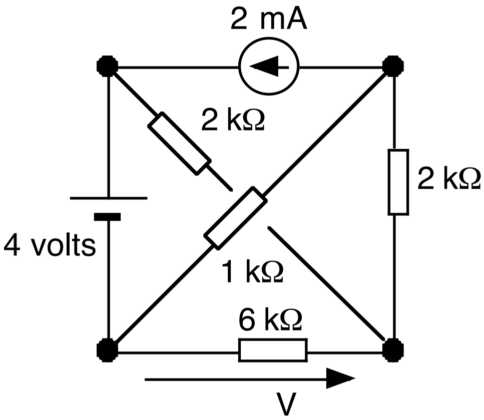


Figure 3d

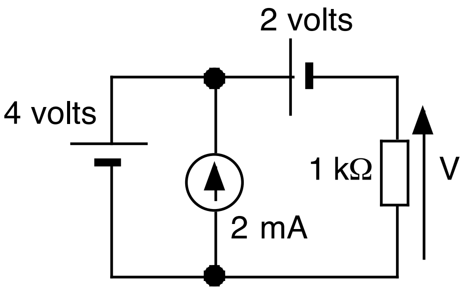


Figure 3e

[10]

(c) The circuit of Figure 3f contains a voltage-controlled current source. For this circuit, and for the voltage reference node indicated on the diagram, write down, *but do not solve*, the nodal voltage equations. In your answer redrawn the circuit diagram and identify clearly the voltages appearing in the nodal voltage equations.

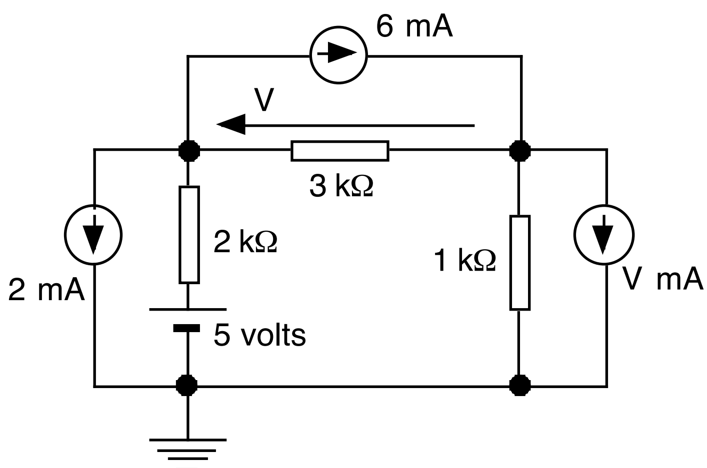


Figure 3f

[40]

4 All the opamps in this question can be assumed ideal and with output saturation voltages of +10 volts and -10 volts.

(a) Calculate the indicated voltage (V) in each of the four circuits A, B, C and D in Figure 4a

[5]

[5]

[15]

[20]

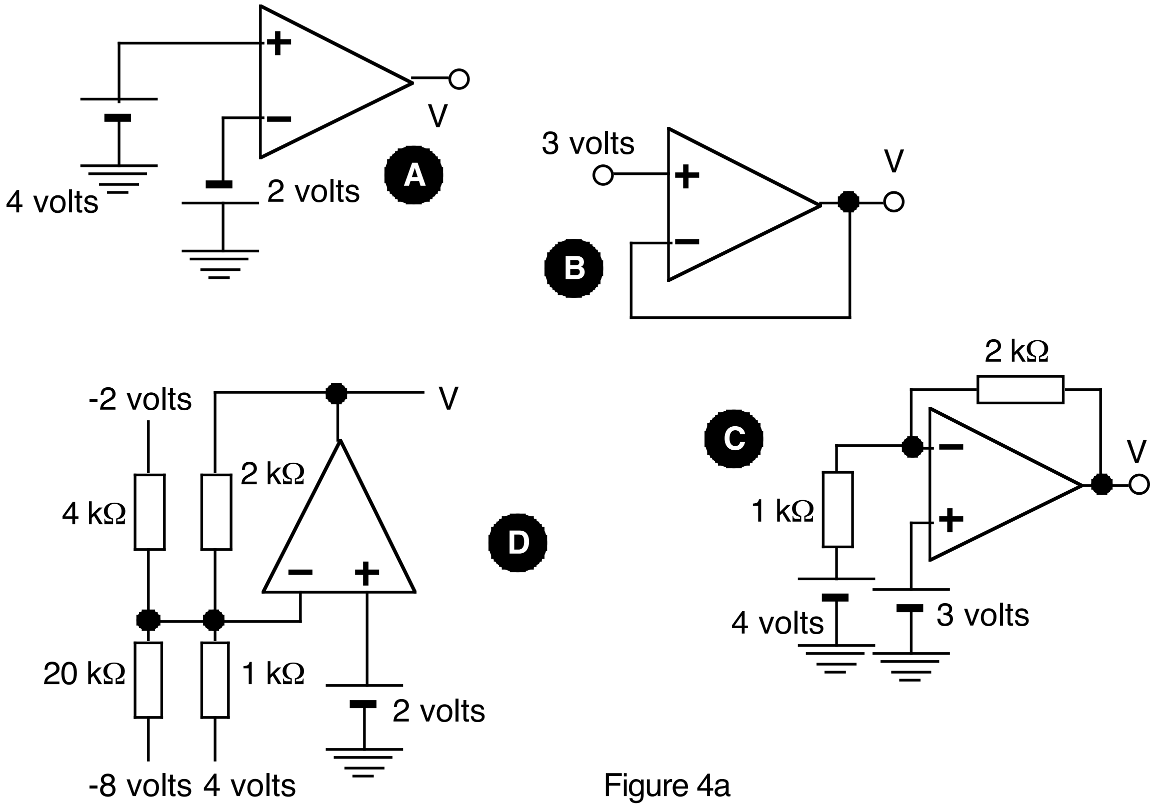


Figure 4a

(b) In the circuit of Figure 4b the voltage V varies between -3 and +3 volts. Provide a dimensioned sketch of the variation of the current I with the voltage V. [20]

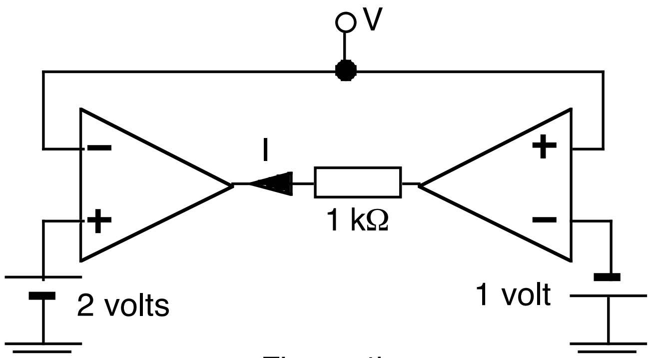
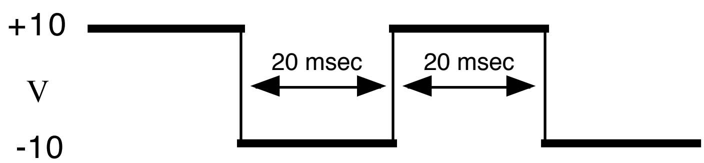


Figure 4b

(c) Using only opamps, resistors and a capacitor, design a circuit employing an integrator and a trigger circuit connected in cascade that will generate a continuous voltage V having the waveform shown in Figure 4c

[35]

Figure 4c



Answer 4

Denote the voltage between the inputs of an op amp by V_I

(a) A $V_I = 4 - -2 = 6$ volts so $V = +10$ volts

B is a voltage follower so $V = 3$ volts

C If linear operation $V_I = 0$ so V^+ and $V^- = 3$ volts. Therefore current through 1 kΩ is $(4-3)/1 = 1$ mA. This current flows through the 2 kΩ resistor, creating a voltage of 2 volts. Applying KVL we get $V + 2 + V_I - 3 = 0$ so $V = 1$ volt, well within the saturation levels, hence $V_I = 0$ confirmed.

D If $V_I = 0$ $V^- = 2$ volts. So currents which add to flow in the 2kΩ resistor are: $(4-2)/1$, $-(2--8)20$ and $(2--2)/4$ so current in 2kΩ is 0.5 mA. This current passes through the 2kΩ resistor creating a voltage of 1 volt. Applying KVL we find $V + 1 + V_I - 2$ so $V = 1$ volt. Assumption about $V_I = 0$ justified.

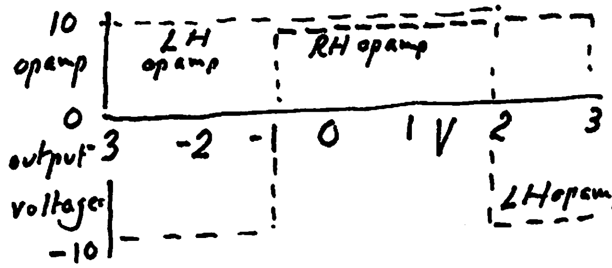
(b) LH opamp output voltage is 10^v for $V < 2$ volts (transition at 2 volts). Otherwise -10^v

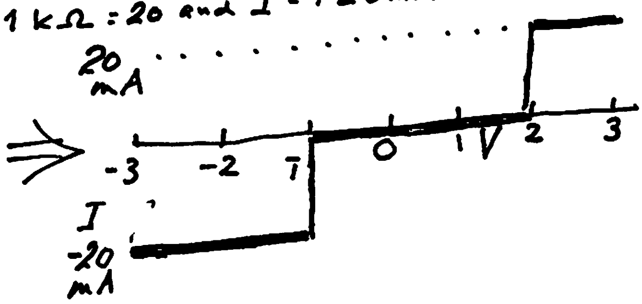
RH opamp output voltage is 10^v for $V > -1$ volt (transition at -1 volt). Otherwise -10^v

Thus for $V = -3$ to -1^v voltage across 1 kΩ = 20 and $I = -20$ mA

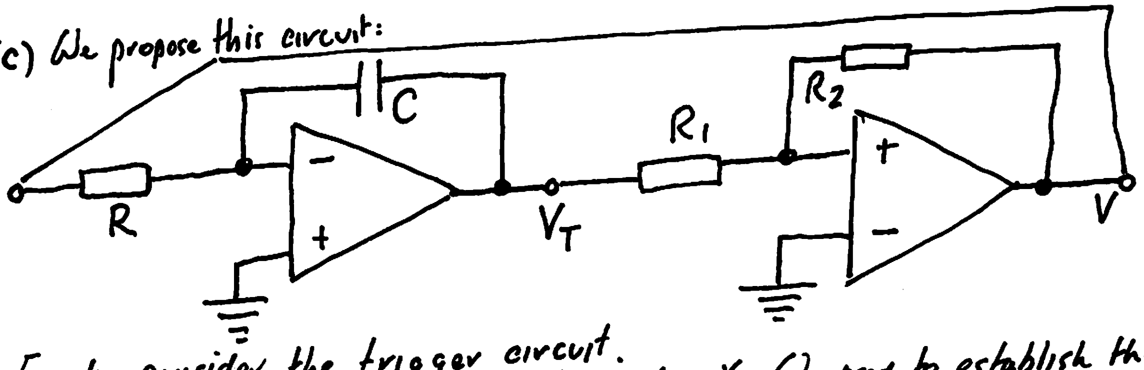
for $V = -1$ to $+2^v$ voltage across 1 kΩ = 0 and $I = 0$ mA

for $V = 2$ to 3^v voltage across 1 kΩ = 20 and $I = +20$ mA

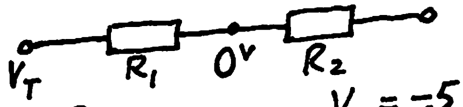




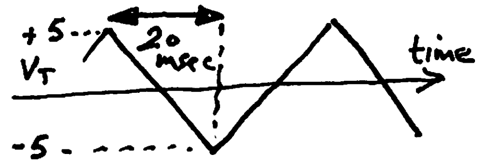
(c) We propose this circuit:



First, consider the trigger circuit. We assume that the opamp saturates at $\pm 10^v$. We need to establish the threshold values of V_T that will cause transition. The model for $V = +10^v$ is shown on the right, from which we calculate that the threshold is $V_T = -10 R_1/R_2$. We arbitrarily choose $R_2 = 1$ kΩ, $R_1 = 5$ kΩ giving $V_T = -5$ volts. The threshold for transition from $V = -10^v$ to $+10^v$ will be $V_T = +5$ volts.



The waveform of V_T will be as shown on right



As V_T decreases, $\frac{dv}{dt} = \frac{10^v}{20.10^{-3}}$. This will be related to the capacitor for which $i = C\frac{dv}{dt}$ so

$i = 10/R = C.10^v/20.10^{-3}$ so that

$RC = 0.02$. Arbitrarily we choose $R = 10$ kΩ, $C = 2\mu F$.

Answer 3

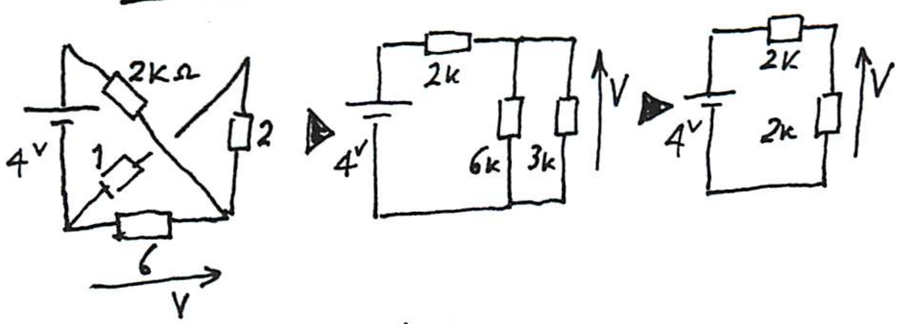
(a) Figure 3a $V = 0$ across the short circuit

Figure 3b $I = 10^{v}/2\,k\Omega = 5\,mA$

Figure 3c The $9\,k\Omega$ is redundant and can be replaced by a short-circuit. The parallel connection of $3\,k\Omega$ and $6\,k\Omega$ is equivalent to $2\,k\Omega$. The voltage across each is $(2\,mA) \times 2\,k\Omega = 4$ volts. So the current through the $6\,k\Omega$ resistor is $4/6$ mA

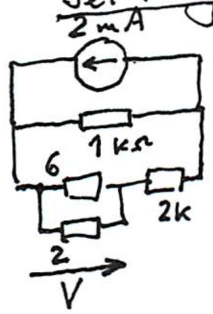
(b) Figure 3d
Two circuits must be analysed.

Set current source to zero



So $V = 2$ volts due to voltage source

Set voltage source to zero

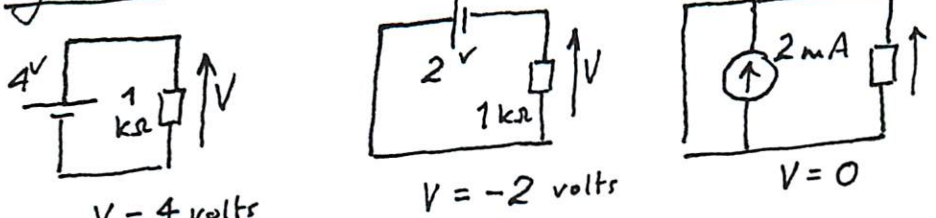


$6\,k\Omega$ and $2\,k\Omega$ in parallel are equivalent to $1.5\,k\Omega$ which, in series with $2\,k\Omega$, provides a resistance of $3.5\,k\Omega$ in parallel with $1\,k\Omega$ such that the current source feeds into ~~the~~ $3.5/4.5\,k\Omega$ generating a voltage of $7/4.5$ volts. The voltage V (across the $6\,k\Omega$) is a fraction of this, namely

$$V = -(7/4.5)\,(1.5/3.5) = \frac{7 \cdot 1.5}{4.5 \cdot 3.5} = \frac{-3}{4.5} \text{ volts.}$$

So by superposition the actual value of $2 - \dfrac{3}{4.5} = \dfrac{18-6}{9} = \dfrac{12}{9} = \dfrac{4}{3}$ volts.

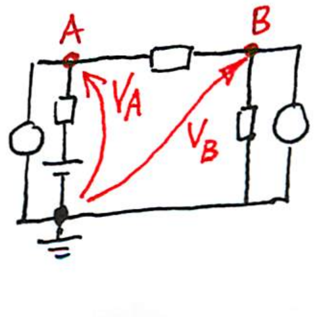
Figure 3e There are 3 circuits to be analysed:



$V = 4$ volts $\quad V = -2$ volts $\quad V = 0$

By superposition $V = 2$ volts.

(c) See circuit at right



KCL at A (IN) $\quad -2 + (5 - V_A)/2 + (V_B - V_A)/3 - 6 = 0$

KCL at B (IN) $\quad 6 + (V_A - V_B)/3 - V_B/1 - (V_A - V_B) = 0$

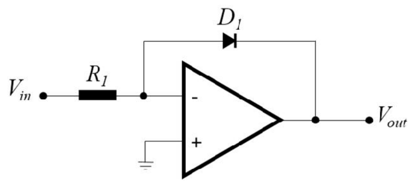
which can be rearranged as:

$$V_A\left(-\tfrac{1}{2} - \tfrac{1}{3}\right) + V_B/3 = 8 - 10 = -2$$

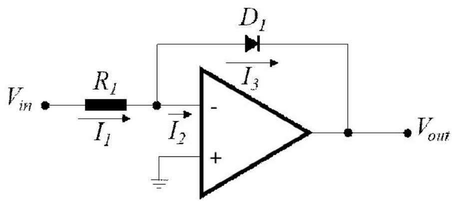
$$V_A\left(\tfrac{1}{3} - 1\right) + V_B\left(-\tfrac{1}{3} - 1 + 1\right) = -6$$

Answer 2

(a) Below is the schematic of the circuit:



(b) Let us label the currents running through the circuit:



Using Kirchhoff's Current Law,

$$I_1 = I_2 + I_3$$

For an ideal Op-amp, the input current is zero and the negative input terminal has the same potential as the positive input terminal which is in this case also zero (*i.e.* virtual ground). If we replace the currents for their corresponding voltages, we get

$$\frac{V_{in} - 0}{R_1} = I_R(e^{\frac{0-V_{out}}{V_T}} - 1)$$

$$\frac{V_{in}}{I_R R_1} = (e^{\frac{-V_{out}}{V_T}} - 1)$$

$$\frac{V_{in}}{I_R R_1} + 1 = e^{\frac{-V_{out}}{V_T}}$$

Typically $\frac{V_{in}}{I_R R_1}$ >>1, hence the above expression can be written as $\frac{V_{in}}{I_R R_1} = e^{\frac{-V_{out}}{V_T}}$

The final expression is: $V_{out} = -ln\left(\frac{V_{in}}{I_R R_1}\right) V_T$

For $V_{in} = 5V$ and the other values stated above in the question, $V_{out} =$ -0.56 V

(c) If the voltage V is approximately 5 volts, a current of 100 mA flows through the 100 Ω resistor. If R = 60 Ω, the current through R = 5/0.06 = 83 mA. This is less than 100 mA so current flows in the Zener and V= 5 volts if R = 40 Ω the current through R would be 5/0.04=125 mA. This exceeds the current available through the 100 Ω resistor so no current flows in the Zener and the circuit becomes a voltage divider with V=40/(40+100)x15 =4.28 volts.

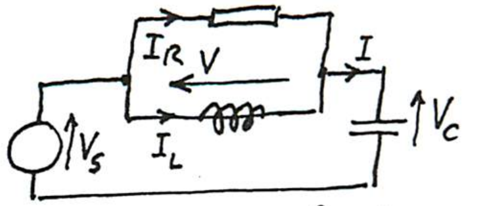
Smallest value of R to maintain V=5volts occurs when the 100mA through the 100 Ω resistor flows entirely through R so that 5 volts =100mA * R, i.e. R=50 Ω. When R is disconnected 100 mA flows in the Zener, so the power dissipated is (5 volts)*(100mA) = 500 mW.

Answer 1

EE1 Exam 2017

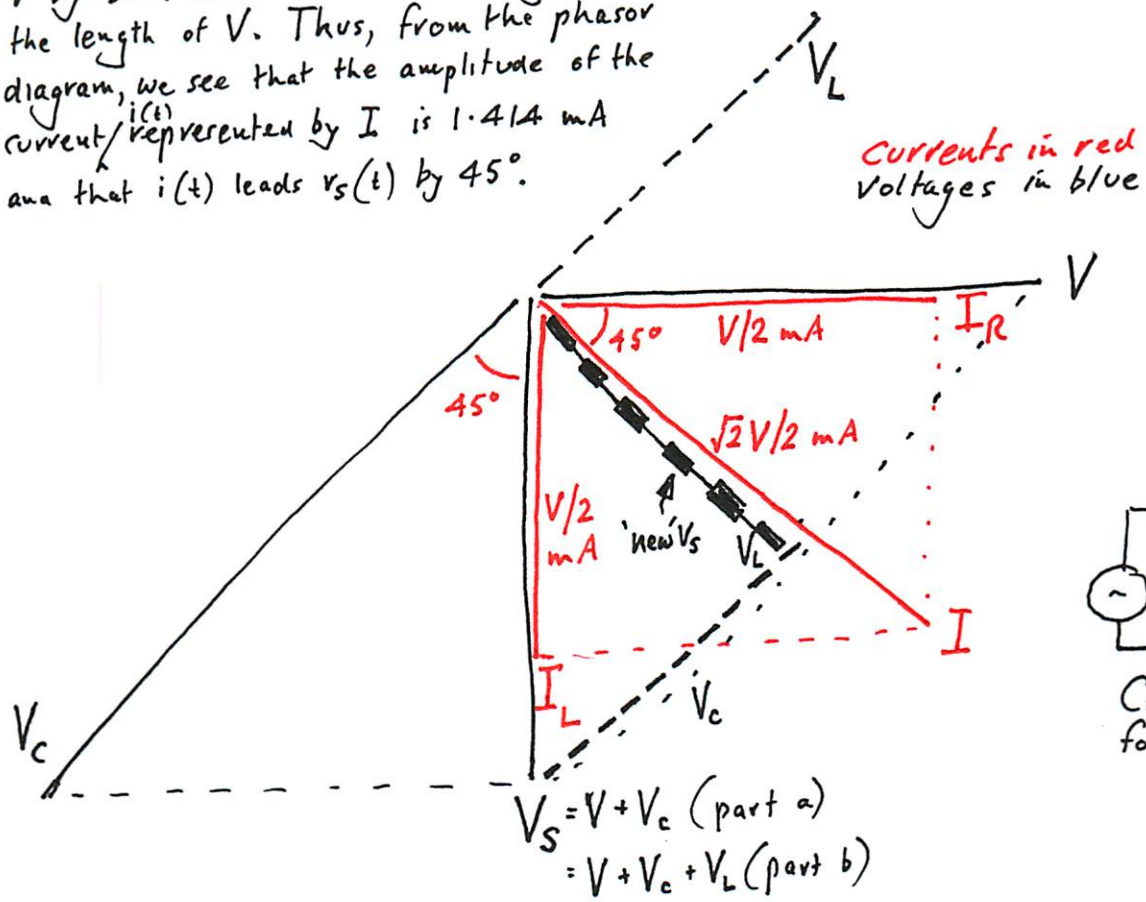
(a) We first calculate the V~I relation for phasors for the inductor and capacitor:

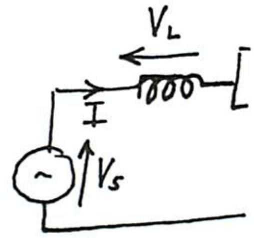
$$\omega L = 2\ \text{k}\Omega, \quad \frac{1}{\omega C} = 2\ \text{k}\Omega$$



Reference sketch for phasors.

Starting with the phasor V (see phasor diagram below) the phasor current I_R is in phase with V and of length $V/2$ mA. I_L lags V by 90° and is also of length $V/2$ mA. The phasor current I (sum of I_R and I_L) lags V by 45° and is of length $\sqrt{2}\times V/2$ mA. I flows in the capacitor so V_c lags I by 90° and is of length $[\sqrt{2}V/2]\times 2\text{k}\Omega = \sqrt{2}V$ volts. Applying KVL ($V_s = V + V_c$) we find that V_s is in phase with I_L and lags V by 90°. We know that the length of V_s represents 2 volts and so also, therefore, does the length of V. Thus, from the phasor diagram, we see that the amplitude of the current $i(t)$ represented by I is 1·414 mA and that $i(t)$ leads $v_s(t)$ by 45°.





Circuit modification for part (b)

(b) With the addition of the inductor L, that part of the phasor diagram involving V, I_R, I_L, I and V_c remains unchanged. The current I now flows additionally through L creating a voltage V_L leading I by 90°. The source voltage V_s is now, by KVL, $V + V_c + V_L$. This 'new' V_s (see ▬ ▬ ▬ in diagram) can, by the suitable choice of L (and hence V_L) ~~by a~~ be adjusted to be in phase with I, so that $i(t)$ and $v_s(t)$ are in phase. That critical value of V_L (– – – in diagram) corresponds to a voltage phasor of length $\sqrt{2}V/2$. Hence $\omega L = (\sqrt{2}V/2) \div (\sqrt{2}V/2) = 1\ \text{k}\Omega$. So $L = 1$ H.

(c) Using the complex representation of voltages and currents, the impedance Z of the circuit connected to the voltage source is:

$$Z = j\omega L + \frac{1}{\frac{1}{2} + \frac{1}{2j}} + \frac{1}{j\omega C}$$ which, substituting for C and L, gives $Z = 2 + j0\ \text{k}\Omega$

Since the imaginary part of Z is zero, $v_s(t)$ and $i(t)$ are in phase, confirming the choice of L.