EE3-11
EE9-AO8

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2014-15

MSc and EEE PART III/IV: MEng, BEng and ACGI

Corrected Copy

ADVANCED ELECTRONIC DEVICES

Monday, 8 December 9:00 am

Time allowed: 3:00 hours

There are FIVE questions on this paper.

Answer Question One and THREE other questions.

All questions carry equal marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : K. Fobelets
Second Marker(s) : S. Lucyszyn

Special instructions for invigilators

Q1 is compulsory

Special instructions for students

Q1 is compulsory.
Do not use red nor green ink.

Constants

permittivity of free space:	$\varepsilon_o = 8.85 \times 10^{-12}$ F/m
permeability of free space:	$\mu_o = 4\pi \times 10^{-7}$ H/m
intrinsic carrier concentration in Si:	$n_{i\,Si} = 1.45 \times 10^{10}$ cm^{-3} at $T = 300$K
intrinsic carrier concentration in GaAs:	$n_{i\,GaAs} = 1.79 \times 10^{6}$ cm^{-3} at $T = 300$K
intrinsic carrier concentration in AlAs:	$n_{i\,AlAs} = 40$ cm^{-3} at $T = 300$K
intrinsic carrier concentration in InAs:	$n_{i\,InAs} = 1 \times 10^{15}$ cm^{-3} at $T = 300$K
dielectric constant of SiO_2:	$\varepsilon_{ox} = 4$
dielectric constant of Si:	$\varepsilon_{Si} = 12$
dielectric constant of GaAs:	$\varepsilon_{GaAs} = 13$
dielectric constant of AlAs:	$\varepsilon_{AlAs} = 10$
dielectric constant of InAs:	$\varepsilon_{InAs} = 15$
electron affinity of Si	$\chi_{Si} = 4.05$ eV
electron affinity of GaAs	$\chi_{GaAs} = 4.1$ eV
electron affinity of AlAs	$\chi_{AlAs} = 3.6$ eV
electron affinity of InAs	$\chi_{InAs} = 4.9$ eV
band gap of Si:	$E_{G\,Si} = 1.12$ eV
band gap of GaAs:	$E_{G\,GaAs} = 1.42$ eV
band gap of AlAs:	$E_{G\,AlAs} = 2.2$ eV
band gap of InAs:	$E_{G\,InAs} = 0.36$ eV
effective density of states of Si:	$N_{C\,Si} = 2.8 \times 10^{19}$ cm^{-3}
	$N_{V\,Si} = 1.04 \times 10^{19}$ cm^{-3}
effective density of states of GaAs:	$N_{C\,GaAs} = 4.7 \times 10^{17}$ cm^{-3}
	$N_{V\,GaAs} = 9.0 \times 10^{18}$ cm^{-3}
effective density of states of AlAs:	$N_{C\,AlAs} = 1.5 \times 10^{19}$ cm^{-3}
	$N_{V\,AlAs} = 1.7 \times 10^{19}$ cm^{-3}
effective density of states of InAs:	$N_{C\,InAs} = 8.7 \times 10^{16}$ cm^{-3}
	$N_{V\,InAs} = 6.6 \times 10^{18}$ cm^{-3}
thermal voltage:	$kT/e = 0.026$V at $T = 300$K
charge of an electron:	$e = 1.6 \times 10^{-19}$ C (1 eV)

Table 0: Workfunction of metals

metal	ϕ (eV)
Al	4.08
Ni	5.01
Ti	4.33
W	4.6

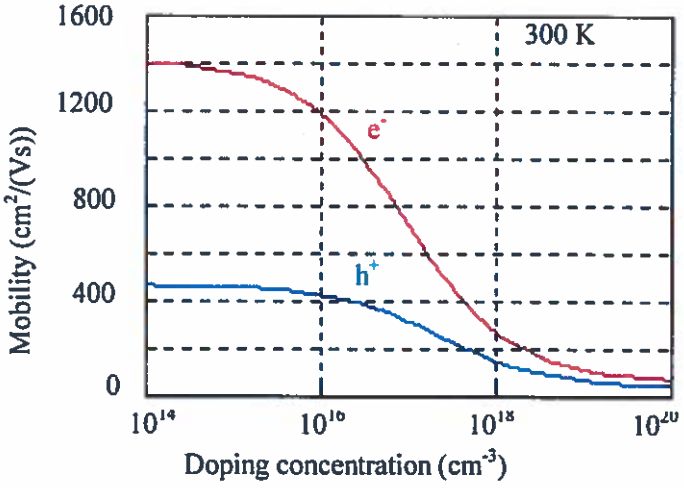

Figure 0: Electron and hole mobility in Si as a function of doping concentration.

Formulae

$$p = N_v e^{(E_v - E_F)/kT}$$
$$n = N_c e^{(E_F - E_c)/kT}$$

Carrier density – Fermi-Dirac statistics

$$J_n(x) = e\mu_n n(x)E(x) + eD_n \frac{dn(x)}{dx}$$
$$J_p(x) = e\mu_p p(x)E(x) - eD_p \frac{dp(x)}{dx}$$

Drift – diffusion current density equations for electrons, J_n and holes, J_p

$$I_{DS} = \frac{\mu C_{ox} W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right)$$

Strong inversion MOSFET current

$$V_{th} = \phi_m - \phi_s + 2\times\phi_F + \gamma\times\sqrt{2\times\phi_F}$$

Threshold voltage

$$\phi_F = \frac{kT}{e}\ln\left(\frac{N_A}{n_i}\right)$$

Fermi potential (difference between intrinsic and Fermi level)

$$\gamma = \frac{\sqrt{2e\varepsilon_s N_A}}{C_{ox}}$$

Body effect coefficient

$$J = \frac{eD_n n_p}{L_n}\left(e^{\frac{eV}{kT}} - 1\right) + \frac{eD_p p_n}{L_p}\left(e^{\frac{eV}{kT}} - 1\right)$$

Diode current density

$$V_{bi} = \frac{kT}{e}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Built-in voltage pn diode

$$W_{depl}(V) = \left[\frac{2\varepsilon(V_{bi} - V)}{e}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]^{1/2}$$

Depletion width in pn diode

$$S = \frac{dV_{GS}}{dLog(I_{DS})}$$

Sub-threshold swing

$$c = c_0 \exp\left(\frac{eV}{kT}\right) \text{ with } \begin{cases} c = p_n \text{ or } n_p \\ c_0 \text{ bulk minority carrier concentration} \end{cases}$$

Minority carrier injection under bias V

$$\delta c = \Delta c \exp\left(\frac{-x}{L}\right) \text{ with } \begin{cases} \delta c = \delta p_n \text{ or } \delta n_p \\ \Delta c \text{ the excess carrier concentration} \\ \text{at the edge of the depletion region} \end{cases}$$

Excess carrier concentration as a function of distance

$$L = \sqrt{D\tau}$$

Diffusion length

$$D = \frac{kT}{e}\mu$$

Einstein relation

1. *Compulsory question.*

a) For a p-type Si resistor.

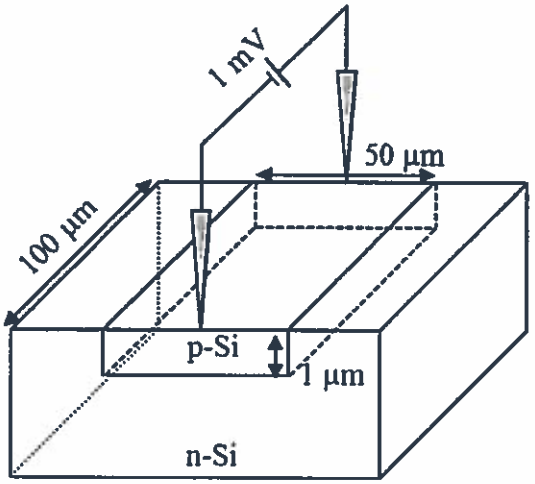

Figure 1.1: The geometry of a diffused p-type region in an n-Si substrate. The probe needles form Ohmic contacts and are shown as grey triangles.

In figure 1.1 a p-type volume has been defined within an n-Si substrate. The doping concentration of the substrate is $N_D = 10^{14}$ cm^{-3} and of the diffused layer is $N_A = 10^{18}$ cm^{-3}. Two Ohmic contacts are made at the edges of the diffused layer with probe needles.

i) Calculate the current through this system when $V = 1$ mV and the contacts have a resistance of 1 Ω each. [4]

ii) Sketch the energy band diagram, including E_F, E_c, E_v and E_G, between the two contacts through the p-Si region when a voltage of 1 mV is applied. Include the influence of the contacts. Ensure all relative magnitudes in energy are correct. [5]

b) For a depletion mode n-channel GaAs MESFET

i) Sketch the energy band diagram, including E_F, E_c, E_v and E_G, from the gate into the bulk when no bias voltages are applied. [4]

ii) Calculate the value of the gate voltage that needs to be applied to fully deplete the channel when $V_{DS} = V_{BS} = 0$ V and the metallurgic channel depth is, $a_m = 200$ nm. The channel doping density is 10^{17} cm^{-3}. The gate metal is tungsten (W) and the gate surface is fully passivated. [5]

c) For a depletion mode AlGaAs/GaAs n-channel HEMT

i) Sketch the energy band diagram, including E_F, E_c, E_v and E_G, from the gate into the bulk when no bias voltages are applied. [5]

ii) Explain why the electron mobility in an n-HEMT is higher than in an n-MESFET. [2]

2. *Velocity saturation in short channel Si MOSFETs.*

The drift velocity-field relationship is given by:

$$|v_d| = |v_d^{\max}| \frac{\left(\frac{|E_x|}{|E_c|}\right)}{\left(1+\frac{|E_x|}{|E_c|}\right)} \quad (1)$$

with v_d the drift velocity, $v_d^{\max}$ the maximum velocity, E_x the electric field in the x direction and E_c the critical value of the electric field.

a) Plot the following:

i) The drift velocity-field curve for $0 \leq E_x \leq 5 \times E_c$. [2]

ii) Add the asymptotes in the low and high electric field region. [2]

iii) Derive an expression for E_c based on the asymptotes. [2]

b) Derive the source-drain current in the:

i) linear region. [8]

ii) saturation region. [3]

for the case velocity saturation occurs. The current can be expressed as:
$I_{DS} = -W\, Q_I(x) |v_d(x)|$. $Q_I(x)$ is the inversion charge per area in strong inversion.
Relate E_x to $V_{CB}(x)$, the potential difference between channel and bulk. All other short channel effects can be neglected in these derivations.

c) Plot the output characteristics, I_{DS}-V_{DS} for an nMOS for $-V_{DD} < V_{DS} < V_{DD}$ with $V_{DD} > V_{GS} - V_{th}$ and $V_{GS} > V_{th}$.

i) For a long channel nMOS that saturates at pinch-off. [3]

ii) For a short channel nMOS that saturates due to velocity saturation. [3]

iii) Give the relationship, (<, >, =), between the saturation currents and voltages in i) and ii). [2]

3. *The use of SiGe in existing semiconductor device technology.*

a) Sketch the energy band diagram (E_c, E_v, E_F, E_G) at zero bias of a completely unstrained n-Si – p-$Si_{1-x}Ge_x$ diode. The material parameters are: $N_D = 10^{-3} \times N_A$. The $Si_{1-x}Ge_x$ is linearly graded from $x_{Ge} = 0$ at the junction to $x_{Ge} = 0.85$ at the end, L_{SiGe} of the SiGe layer. The length of the layers, L_{Si} and L_{SiGe} are longer than the minority carriers diffusion length.
The bandgap of unstrained $Si_{1-x}Ge_x$ is given by:
$$E_G(x_{Ge}) = 1.12 - 0.41 \times x_{Ge}$$
The following relationship is valid for unstrained p-$Si_{1-x}Ge_x$:
$\chi(x_{Ge}) + E_G(x_{Ge}) =$ constant for $0 \le x_{Ge} \le 0.85$, with $\chi(x_{Ge})$ the Ge concentration dependent electron affinity. [10]

b) Indicate the direction of the internal electric field on the sketch in a). [5]

c) Derive the expression of the minority carrier current density in both the Si as well as the $Si_{1-x}Ge_x$ region if a forward bias, V_a is applied across the diode in a). The mathematical expressions should be written as a function of material parameters: N_A, N_D, D_p, D_n, x and V_a. You should assume that V_a drops across the junction depletion region only. [10]

4. *The influence of the access resistance in MOSFETs.*

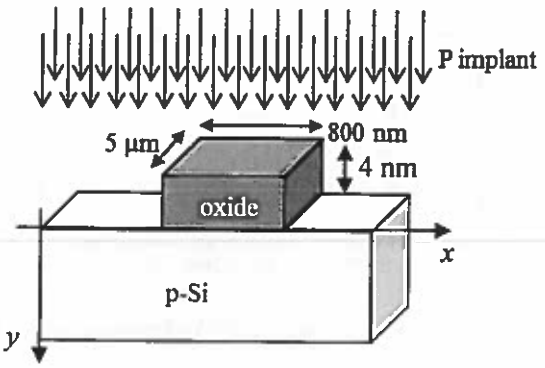

Figure 4.1: Source and drain doping self-aligned to the gate oxide. The dimension of the gate is given. Source and drain implants are symmetric.

After doping implantation and annealing, the junction depth is t_j and the diffusion in the lateral direction, x is $t_j/4$ for both HDD and LDD.
For the HDD, $N_D = 10^{20}$ cm^{-3} and $t_j = 400$ nm.
For the LDD, $N_D = 10^{18}$ cm^{-3} and $t_j = 100$ nm.
In the bulk, $N_A = 5\ 10^{17}$ cm^{-3}.

a) Sketch the 2D (x-y) material cross section of the source implant of the MOSFET of figure 4.1 for two doping techniques (each followed by an anneal step).

   i) Using HDD self-aligned to the gate oxide. [5]

   ii) Using LDD and HDD with side wall spacer technology. The spacer width is 150 nm (in the x direction). [6]

   Indicate the values of the transverse and lateral dimensions of the doping regions. The implanted volumes can be considered rectangular in all directions.

b) Calculate the current, I_{DS} when $V_{DS} = 0.1$ V, $V_{GS} = 1$ V and $V_{th} = 0.4$ V. The influence of the depletion regions and short channel effects can be neglected. Hint: when expressions become complicated, substitute parameters by their numerical values.

   i) For the self-aligned HDD implant with a total parasitic resistance, $R_{tot} = 1.24\ \Omega$. [6]

   ii) For the side wall spacer technique with LDD and HDD regions and a total parasitic resistance, $R_{tot} = 24.68\ \Omega$. [6]

c) Give two advantages of side wall spacer technology. [2]

5. *n-channel enhancement mode Si finFET.*

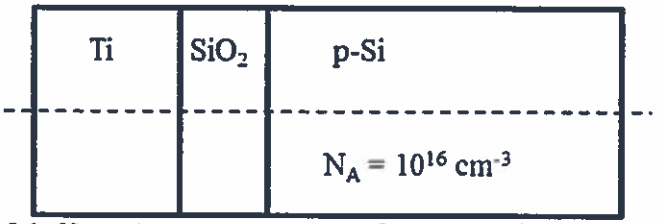

Figure 5.1: Heterojunction consisting of titanium, silicon dioxide and p-Si.

a) Sketch the energy band diagram (E_c, E_v, E_F, E_G) of the heterojunction in figure 5.1 along the dashed line. [5]

b) Calculate the depletion width into the p-Si layer in a) when no voltage is applied and 1/5th of the contact potential difference is dropped across the oxide layer. [5]

c) Sketch a 3D tri-gate finFET on SOI without explicitly drawing the source and drain. Indicate where source and drain should occur with arrows only. The thickness of the oxide that wraps the fin underneath the Ti gate, is constant. The width, height and length of the fin are: $H = 300$ nm, $W = 200$ nm, and $L = 400$ nm. [5]

d) Sketch the energy band diagram (E_c, E_v, E_F, E_G) of this tri-gate finFET through the fin, perpendicular to the source-drain direction. No bias is applied. [5]

e) Calculate the total current, I_{DS} through finFET of c) when a gate voltage is applied that creates inversion charge of $Q_I = 5\times 10^{-7}$ cm^{-2}. $V_{DS} = 1$ mV and no velocity saturation effects occur. The mobility in the channel reduces by a factor of 2 due to interface roughness scattering. You can ignore any edge effects. [5]