ANSWERS - E4-16 & EE9-AC6 - ANALOGUE SIGNAL PROCESSING -2017

1.

a. Compare Voltage and Current mode domains as regards to dynamic range, processing, signal distribution and speed.

- Voltage mode dynamic range is limited by supply voltage whereas current mode dynamic range is limited by how much current can be sourced or sinked in a current mirror leading to larger dynamic range. [1 point]
- Current mode can lead to easier signal processing since addition of signals required just summing through Kirchoffs current law. [1 point]
- In voltage mode one wire can feed many nodes whereas in current mode one wire serves one node and current mirrors are needed to copy currents. [1 point]
- Current mode operation leads to higher speed of operation since capacitive nodes can be charged instantaneously. [1 point]

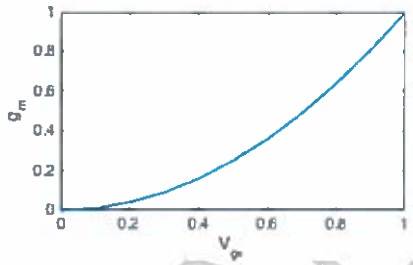
[4]

b. The equation for the drain current of new type of cubic transistor is shown below K and I_0 are constants and all other terms have their usual meaning.

$$I_D = KI_O(V_{GS} - V_t)^3$$

i) Derive the transconductance of the device and sketch its relationship with the transistors gate voltage.

Transconductance: $\frac{dI_D}{dV_{GS}} = 3KI_O(V_{GS} - V_t)^2$ [2 points]



[2 points]

[4]

ii) Derive the transconductance efficiency of the device, stating your answer only in terms of I_D, I_0 and K.

Tranconductance efficiency: $\frac{g_m}{I_D} = 3KI_0\left(\frac{I_D}{I_O}\right)^{3/2}$ [2 points]

[2]

iii) The cubic transistor is to be used in a switched current memory cell shown in Figure 1.1. Explain one reason why such a transistor would have worse performance when compared with a standard MOSFET operating with a square law characteristic.

The effects of charge injection on the floating gate would be squared when it appears on the output current as its transconductance has a square law dependency on the input voltage.

[2]

c. For the cascade of amplifiers shown in Figure 1.2, derive the output referred noise and explain what factors can be optimized to improve the signal to noise ratio.

MOS Noise: $$v_n^2 = \frac{K_w}{I_D^p} \cdot \Delta f + \frac{K_f}{A} \cdot \ln\left(\frac{f_h}{f_l}\right)$$

Distributed gain: $$G_i = \prod_{k=1}^{k=Nf} g_k$$

Total output Noise: $$v_{no}^2 = \sum_{i=1}^{i=Nf} v_{ni}^2 G_i^2$$

Final Equation: $$v_{no}^2 = \sum_{i=1}^{i=Nf} v_{ni}^2 G_i^2 = \sum_{i=1}^{i=Nf} \left(n_i \frac{K_w}{(I_i / n_i)^p} \cdot \Delta f + n_i \frac{K_f}{(A_i / n_i)} \cdot \ln\left(\frac{f_h}{f_l}\right) \right) G_i^2$$ [6 points]

- Increasing Power and Area reduce the noise
- If we are willing to compute slowly (Δf and fh/fl are both small) then we can keep output noise low without consuming a lot of power. [2 points]

2.

a. State and derive the translinear principle (TLP) for a loop of MOS transistors working in weak inversion. Give all assumptions you make.

[bookwork]

In a closed loop containing an even number of forward biased junctions, arranged so that there are an equal number of clockwise facing and counterclockwise facing polarities, the product of the current densities in the clockwise direction is equal to the product of the current densities in the counterclockwise direction.

[2 points for definition]

Number of Clockwise Junctions (Voltage Rises)=Number of Anticlockwise Junctions (Voltage drops)

$$\sum_{n\in CW} V_n = \sum_{n\in CCW} V_n$$

$$V_n = nU_T \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right)$$

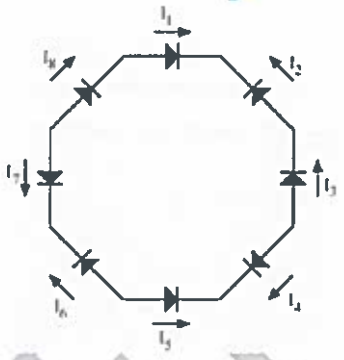
$$\sum_{n\in CW} nU_T \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right) = \sum_{n\in CCW} nU_T \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right)$$

$$\sum_{n\in CW} \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right) = \sum_{n\in CCW} \ln\left(\frac{I_n}{\lambda_n I_{DO}}\right)$$

$$\prod_{n\in CW} \frac{I_n}{\lambda_n I_{DO}} = \prod_{n\in CCW} \frac{I_n}{\lambda_n I_{DO}}$$

$$\prod_{n\in CW} \frac{I_n}{\lambda_n} = I_{DO}^{CW-CCW} \prod_{n\in CCW} \frac{I_n}{\lambda_n}$$

$$\prod_{n\in CW} \frac{I_n}{\lambda_n} = \prod_{n\in CCW} \frac{I_n}{\lambda_n}$$



Assumptions: Temperature and saturation currents are all the same.

[3 points for derivation]

[5]

b. Show how short channel effects in MOS transistors operating in weak inversion, lead to multiplicative errors in output currents of translinear circuits.

- Short channel effects of MOS transistors induce an Error due to early effect/channel length modulation

$$I_{DS(wi)} = \lambda \cdot I_{D0} \exp\left(\frac{V_{GS}}{nU_t}\right)\left(1-\exp\left(\frac{-V_{DS}}{U_t}\right)\right) = \lambda \cdot \gamma \cdot I_{D0} \exp\left(\frac{V_{GS}}{nU_t}\right)$$ [2]

- Appear like an area mismatch

$$\prod_{n\in CW} \frac{I_n}{\lambda_n \gamma_n} = \prod_{n\in CCW} \frac{I_n}{\lambda_n \gamma_n}$$ [2]

[4]

c. Figure 2.1 shows a translinear circuit.

i. Derive the transfer function I_{out} of this circuit using the translinear principle. You may assume that currents I_1 and I_3 are input currents and I_2 and I_4 are a static bias'.

Translinear Loop: $I_{Q1}.I_{Q2}.I_{Q3}.I_{Q4}.I_{Q5}=I_{Q6}.I_{Q7}.I_{Q8}.I_{Q9}.I_{Q10}$ [Total 2 points]

Also $I_{Q1}=I_{Q2}=I_{out}-I_2$, $I_{Q4}=I_{Q5}=I_{out}$, $I_{Q6}=I_{Q7}=I_2$, $I_{Q10}=I_{Q9}=I_4$

Substituting yields:

$I_{out}=I_4\sqrt{(I_3/I_1)}$ [Total 3 points]

[5]

ii. Write down an expression for the output current I_{out} when I_{in}= Asin(ωt) and I_1 and I_3 are given as:

$$I_3 = \left|\frac{dI_{in}}{dt}\right|, \qquad I_1 = \left|\int I_{in}\, dt\right|$$

$I_3 = \left|\frac{dI_{in}}{dt}\right| = A\omega cos(\omega t)$, [1]

$I_1 = |\int I_{in}\, dt| = \frac{A}{\omega}\cos(\omega t)$ [1]

$I_{out}=I_4 \times \omega$ [2]

[4]

iii. What is the function of this circuit when the inputs are applied as in 2.b.ii ?

The circuit monitors the frequency of the input [Total 2 points]

[2]

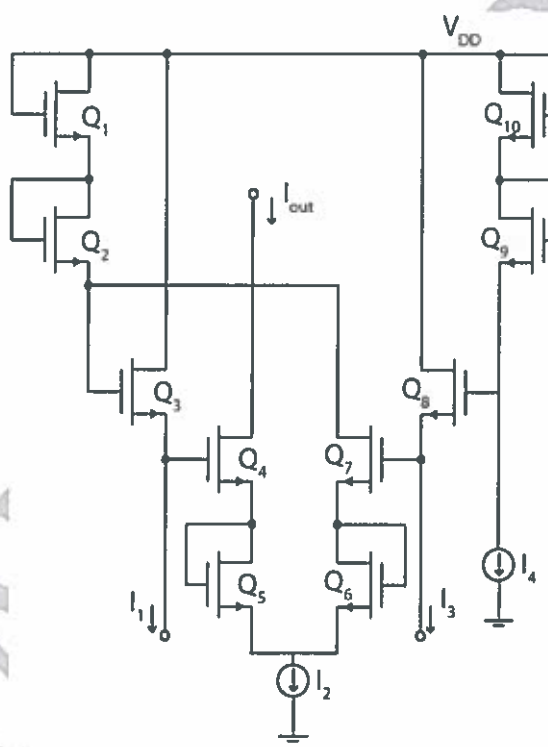


Figure 2.1

3. The transfer function of a second order topology has been decomposed into the following state-space equations:

$$\dot{X_1} = -\left(\frac{\omega_0}{2Q}\right)X_1 - \omega_0\left(1 - \frac{1}{4Q^2}\right)X_2 + \omega_0 U$$
$$\dot{X_2} = -\left(\frac{\omega_0}{2Q}\right)X_2 + \omega_0 X_1$$
$$Y_1 = X_1$$
$$Y_2 = X_2$$

whereby Y_1 and Y_2 are the outputs and X_1 and X_2 are the state-variables and U is the input.

a. Show that the output Y_1 can be used to implement a second order lowpass transfer function and the output Y_2 can be used to implement a "two-pole one-zero" second order transfer function.

New derivation:

$$\left[s + \frac{\omega_0}{2Q}\right]X_1(s) - \omega_0\left(1 - \frac{1}{4Q^2}\right)X_2(s) = \omega_0 U$$
$$-\omega_0 X_1(s) + \left[s + \frac{\omega_0}{2Q}\right]X_2(s) = \omega_0 U(s)$$

Substituting for $X_2(s)$ (2 points)

$$\frac{Y_1(s)}{U(s)} = \frac{X_1(s)}{U(s)} = \frac{\omega_0^2}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}, \textit{low pass response}$$

Substituting for $X_1(s)$ (2 points)

$$\frac{Y_2(s)}{U(s)} = \frac{X_2(s)}{U(s)} = \frac{\omega_0\left(s + \frac{\omega_0}{2Q}\right)}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}, \textit{two pole , one zero response}$$

[4]

b. By using the mappings below, show how these state space equations can be mapped to non-linear log-domain design equations. State any assumptions you make.

$$X_1 = I_1 \exp\left(\frac{V_1}{nU_t}\right) \qquad X_2 = I_2 \exp\left(\frac{V_2}{nU_t}\right) \qquad U = I_U \exp\left(\frac{V_U}{nU_t}\right)$$

New derivation from Theory:

$$\frac{I_1}{nU_t}\exp\left(\frac{V_1}{nU_t}\right)\dot{V_1} = -\left(\frac{\omega_0}{2Q}\right)I_1 \exp\left(\frac{V_1}{nU_t}\right) - \omega_0\left(1 - \frac{1}{4Q^2}\right)I_2 \exp\left(\frac{V_2}{nU_t}\right) + \omega_0 I_u \exp\left(\frac{V_u}{nU_t}\right)$$
$$\frac{I_2}{nU_t}\exp\left(\frac{V_2}{nU_t}\right)\dot{V_2} = -\left(\frac{\omega_0}{2Q}\right)I_2 \exp\left(\frac{V_2}{nU_t}\right) + \omega_0 I_1 \exp\left(\frac{V_1}{nU_t}\right)$$

$$C\dot{V_1} = -CnU_t\left(\frac{\omega_0}{2Q}\right) - CnU_t\omega_0\left(1 - \frac{1}{4Q^2}\right)\frac{I_2}{I_1}\exp\left(\frac{V_2 - V_1}{nU_t}\right) + CnU_t\omega_0\frac{I_u}{I_1}\exp\left(\frac{V_u - V_1}{nU_t}\right)$$
$$C\dot{V_2} = -CnU_t\left(\frac{\omega_0}{2Q}\right) + CnU_t\omega_0\frac{I_1}{I_2}\exp\left(\frac{V_1 - V_2}{nU_t}\right)$$

Let C1=C2=C and define: $I_\omega = CnU_t\omega_0$

A suitable mapping:

$$I_1 = I_2 = I_\omega$$
$$I_U = I_0$$

Final Equations:

$$C\dot{V}_1 = -\left(\frac{I_\omega}{2Q}\right) - I_\omega\left(1 - \frac{1}{4Q^2}\right)\exp\left(\frac{V_2 - V_1}{nU_t}\right) + I_o \exp\left(\frac{V_u - V_1}{nU_t}\right)$$

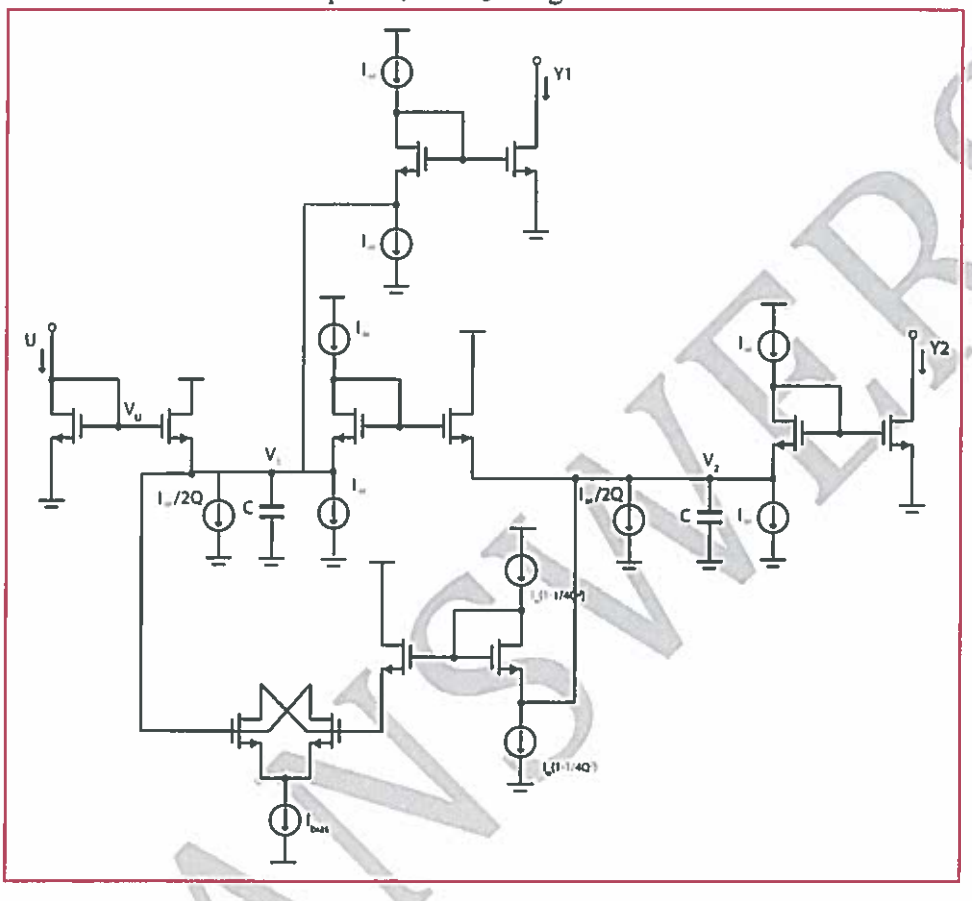
$$C\dot{V}_2 = -\left(\frac{I_\omega}{2Q}\right) + I_\omega \exp\left(\frac{V_1 - V_2}{nU_t}\right)$$

$$Y_1 = I_\omega \exp\left(\frac{V_1}{nU_t}\right)$$

$$Y_2 = I_\omega \exp\left(\frac{V_2}{nU_t}\right)$$

[6]

c. With these log-domain design equations, sketch a schematic of the final log domain topology which realises the two outputs Y_1 and Y_2 using weak inversion MOS transistors.



[10]

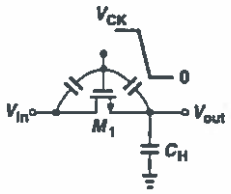
4. Figure 4.1 shows a NMOS sampling switch to be used in the switched capacitor circuit. The width and length of transistor M1 are (W/L)=50/2. This switch causes an error in Vout when it closes.

a. State 4 phenomena which could cause an error in V_{out} with equations descibing each case.

- Charge injection: When a MOSFET is conducting, there is a charge in the inversion layer defined by $Q_{ch} = WLC_{ox}(V_{GS} - V_{th})$. When the MOSFET turns off this charge must escape through the source and drain terminals of the device. When the charge is deposited on the hold capacitor it causes a change, ΔVout in output voltage giving (assuming an equal split):

  $\Delta V_{out} = \frac{Q_{ch}}{2C_H} = \frac{WLC_{ox}(V_{DD}-V_{in}-V_{th})}{2C_H}$ [2]

- Clock Feedthrough: The MOSFET gate source/drain overlap capacitances couple clock transition changes on the hold capacitor causing a change in the output voltage:



  $\Delta V_{out} = \frac{V_{CK}WC_{ov}}{WC_{ov}+C_H}$ where C_{ov} is the overlap capacitance. [2]

- Sampled Noise: A resistor charging a capacitor gives rise to KT/C noise. $v_n = \sqrt{KT/C}$ [2]
- Leakage Current: It will discharge the holding capacitor and thus introduce additional error according to: $\Delta V = \frac{I_{leak}T_H}{C_H}$ [2]

[8]

b. Show with the aid of a graph how the error induced by the most significant of these phenomena causes non-ideal gain and offset.

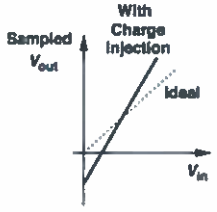
Channel Charge Injection

- Precision is affected.
- Assume all charge is deposited on hold capacitor then:

$$V_{out} \approx V_{in} - \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{C_H},$$

$$V_{out} = V_{in}(1 + \frac{WLC_{ox}}{C_H}) - \frac{WLC_{ox}}{C_H}(V_{DD} - V_{TH}).$$

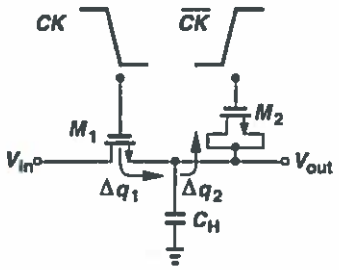
- Causes a non unity gain equal to $1+WLC_{ox}/C_H$
- Causes a constant offset voltage $-WLC_{ox}(V_{DD}-V_{TH})/C_H$



[4]

c. Design a method which cancels out two of these phenomena stating assumptions and showing calculations where necessary.

Including a dummy transistor can remove both charge injection and clock feed-through:



Charge injection from M1 is absorbed to create the channel of M2. For this to occur $\Delta q_1 = \Delta q_2$ where

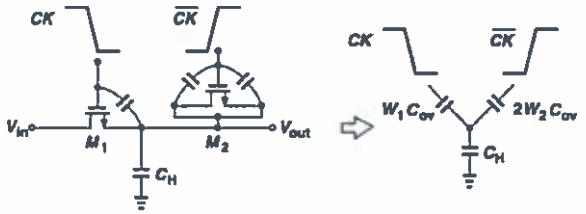
$\Delta q_1 = \frac{W_1 L_1 C_{ox}}{2}(V_{CK} - V_{in} - V_{TH1})$.

and

$$\Delta q_2 = W_2 L_2 C_{ox}(V_{CK} - V_{in} - V_{TH2})$$

Therefore we can choose W_2=0.5W_1, L_2=L_1 to ensure Δq_1=Δq_2 and compensate for charge injection. [2]

Because W_2=0.5W_1 clock feedthrough also gets suppressed:



- Total charge in V_{out} is zero since

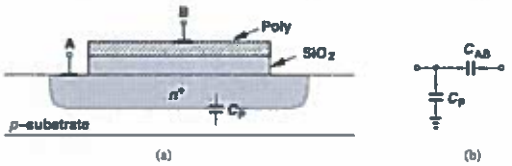
$$-V_{CK}\frac{W_1C_{ov}}{W_1C_{ov}+C_H+2W_2C_{ov}}+V_{CK}\frac{2W_2C_{ov}}{W_1C_{ov}+C_H+2W_2C_{ov}}=0.$$

[2]

[4]

d. What is the advantage of bottom plate sampling of a the capacitor in the circuit Figure 4.2 and state how this should be connected so as not to degrade the circuits speed and precision.

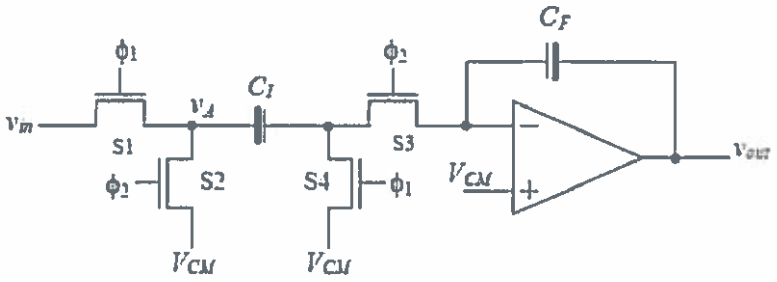
Capacitors implemented in CMOS have a top polysilicon later and a bottom plate, which is a heavily doped n+ region. Therefore the bottom plate has a parasitic junction capacitance, Cp, to the substrate which is usually about 10-20% the oxide capacitance:



(a) Monolithic capacitor structure, (b) circuit model of (a) including parasitic capacitance to the substrate.

Since the input capacitance of the opamp affects speed and precision in SC circuits, it needs to be well defined. Therefore we always connect the top plate to the input of the opamp, and therefore at the high impedance node, and the bottom plate at a low impedance node, which in this design is the input and output. This mimises the effect of the parasitic but also avoids injection of substrate noise. [2]

In this design:



[2]

[4]

5.

[4]

a. Figure 4.1 shows a conventional second-generation positive current conveyor, CCII+.

i. Explain its operation principle and describe how impedances at each of its three ports, X, Y, Z, differ from a standard operational amplifier.

[bookwork]

- Current-voltage characteristics
  $V_X=V_Y$, $I_Z=\pm I_X$, $I_Y=0$
  $Z_Y \rightarrow \infty$, $Z_X \rightarrow 0$, $Z_Z \rightarrow \infty$ [2]
- Voltage-follower between Y-input and X-output
- Current-follower between X-input and Z-output [1]

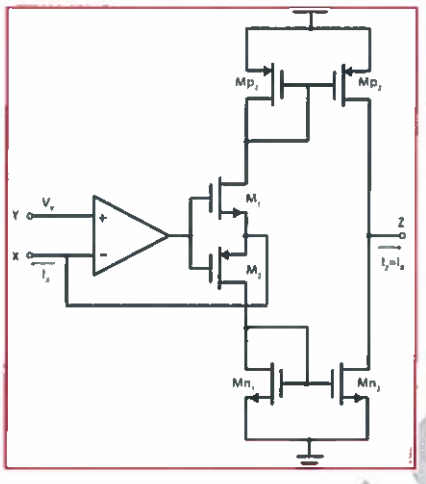
Plus a comparison with Op-amp terminals [1]

[4]

ii. Draw the circuit of a CMOS implementation of a bi-directional CCII+.

Application of taught circuits

Schematic:

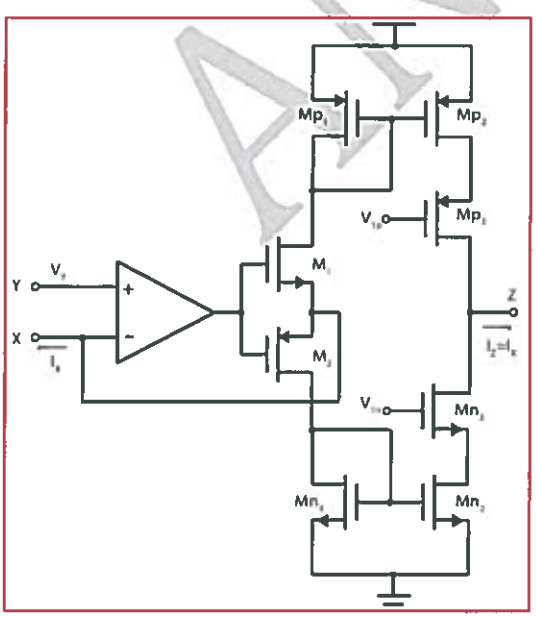


[3]

iii. Propose a method to increase its output impedance.

Cascoding the output will increase the output impedance at the expense of dynamic range.

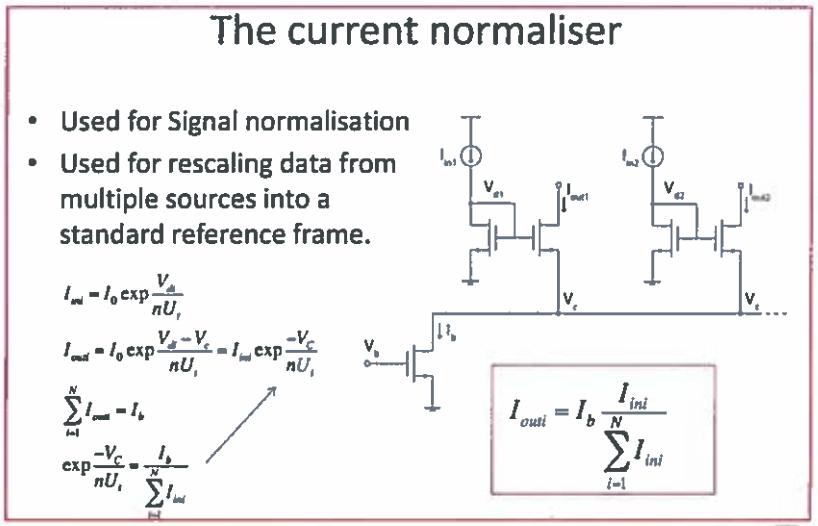
[2]



b. Figure 5.2 shows the circuit for a current normalizer. Derive the transfer function for the generalized current I_{out_i} where i indicate the selected output branch from the circuit.

[4]

Book work:



c. Figure 5.3 shows a circuit which is used as a variable OTA. Using your results from part b. or otherwise derive an equation for the output current I_j as a function of the differential input voltage (E_j-V). You may assume all transistors are operating in weak inversion.

Derivation of new Theory:

For differential pair on the right:

$$I_1 - I_2 = I_{at} \tanh\left(\frac{E_j - V}{2nU_t}\right) = I_0 \exp\left(\frac{v_{d1}}{Ut}\right) - I_0 \exp\left(\frac{v_{d2}}{Ut}\right)$$

For differential pair on the left:

$$I_j = I_3 - I_4 = I_0 \exp\left(\frac{v_{d1} - v_c}{nUt}\right) - I_0 \exp\left(\frac{v_{d2} - v_c}{nUt}\right)$$

$$I_j = \left(I_0 \exp\left(\frac{v_{d1}}{nUt}\right) - I_0 \exp\left(\frac{v_{d2}}{nUt}\right)\right) \exp\left(\frac{-v_c}{nUt}\right)$$

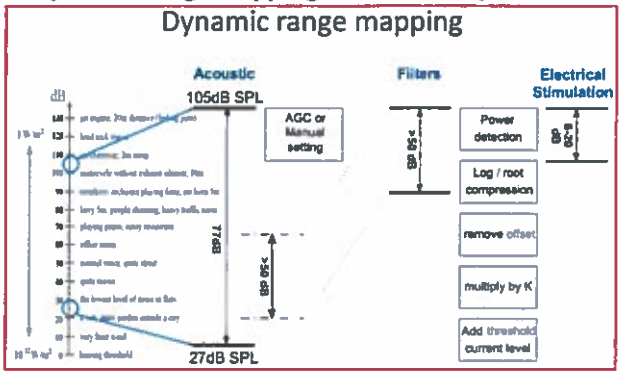
$$I_j = \left(I_0 \exp\left(\frac{v_{d1}}{nUt}\right) - I_0 \exp\left(\frac{v_{d2}}{nUt}\right)\right) \frac{I_{st}}{I_{at}}$$

$$I_j = I_{at} \tanh\left(\frac{E_j - V}{2nU_t}\right) \exp\left(\frac{1}{n}\right) \frac{I_{st}}{I_{at}}$$

[Total 6 points]

6. Figure 6.1 shows the block diagram of a cochlear prosthesis.

a. Explain the concept of dynamic range mapping used in this system and why it is beneficial.

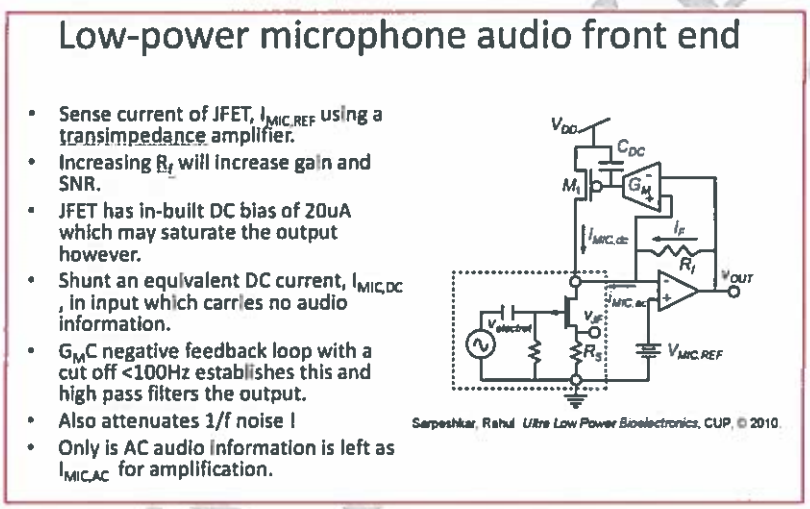


- Dynamic range mapping reduces dynamic range for processing.
- Therefore enables low-power operation for the rest of the analogue processing due to more relaxed dynamic range requirement.
- The instantaneous dynamic range of speech is less than 60db.
- Compress 80dB from AFE to 60 dB in AGC.

[5]

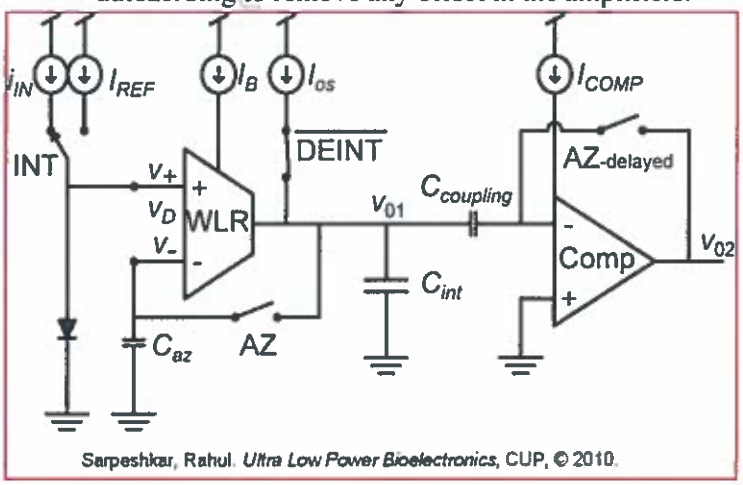
b. Sketch the schematic of a suitable low-power Analogue Front End (AFE) which is suitable for audio frequencies and explain it's operation.

[5]



c.

i) Sketch the schematic of a suitable logarithmic analogue to digital converter which also uses autozeroing to remove any offset in the amplifiers.

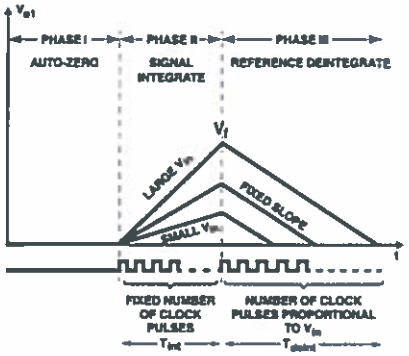


[5]

ii) Explain its operation showing timing diagrams and equations where necessary.

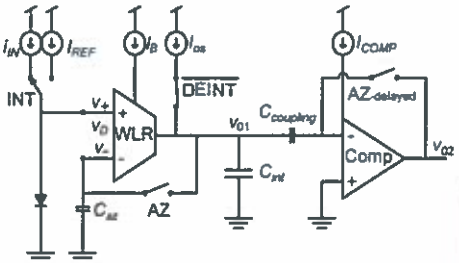
Micropower log-ADC

- Uses a dual slope algorithm.
- Exploits successive integration /de-integration strategy.
- On integration charge capacitor C_{int} with a current proportional to input.
- Then discharge on de-integration phase with a fixed current I_{os}.
- Count time it takes for I_{os} to discharge C_{int}.
- Evaluated by counting clock cycles in a counter.



Operation – Three phases

- **Phase I:** V_+ is tied to I_{REF} and switch AZ is closed, so the offset of the WLR is stored on C_{AZ} and the offset of the comparator is stored on $C_{coupling}$. I_{OS} ensures V_- has a negative offset for de-integration phase.
- **Phase 2:** AZ is opened, and V_+ is switched to I_{IN}, which causes the WLR to charge up C_{int} with a current I_{int} proportional to the log(I_{in}), for a fixed time T_{int}. $I_{int}=g_m(V_D)$ where $V_D=V_+-V_-$
- **Phase 3:** V_+ is switched to I_{REF}(while AZ stays open), and I_{OS} is disconnected, which causes the WLR to discharge C_{int} back down to ground, with a fixed current $I_{deint}=g_m(V_D)$, because V_D will now be negative.
- The time it takes to discharge, T_{deint} is then counted with a digital counter.
- Since T_{deint} is a result of the ratio of two currents, any temperature dependence cancels out !



$$V_f = \frac{I_{int}}{C_{int}} \times T_{int} \quad (I \rightarrow V \text{ transformation})$$

$$T_{deint} = \frac{V_f}{I_{deint}/C_{int}} \quad (V \rightarrow t \text{ transformation})$$

$$= \frac{I_{int}}{I_{deint}} \times T_{int}.$$

[Total 5 points]