IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2017

EEE/EIE PART I: MEng, BEng and ACGI

DIGITAL ELECTRONICS 1

Corrected copy

Thursday, 8 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 each carry 30%.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : Z. Durrani
Second Marker(s) : K. Fobelets

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least-significant bit of a bus signal is labelled as bit 0, and the most-significant bit with the highest integer number. Therefore the signal X[7:0] is an eight-bit bus with X7 being the MSB and X0 the LSB.

In questions involving circuit design, you may use any standard digital circuits not explicitly forbidden by the question, provided that you specify fully their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

Question 1

1. a) (i) Simplify the following Boolean expression using De Morgan's theorem and/or Boolean algebra.

$$\overline{AB\overline{C} + AC + A\overline{B}C}$$

[4]

(ii) Expand $\overline{\overline{A + B} + C}$ in canonical SOP form.

[4]

b) Using a Karnaugh map, find minimal SOP and POS expressions for:

$$f(A,B,C,D) = \sum 0,2,4,6,7,10,13,14$$

with 'don't cares' at 1 and 15

[6]

c) Express the following bit pattern as a hexadecimal number.

1 1 0 1 1 0 1 1 1 1 1 1 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0

assuming the pattern represents:

(i) an unsigned number.

(ii) a signed number in 2s compliment form.

[4]

d) Complete the missing entries, which are not shaded in the following table. No marks will be awarded for this question unless you show how the solution is derived.

[6]

Decimal	Hexadecimal	Signed binary (8 bits wide)	Unsigned binary
4.6875			?
-39		?	
	DA2F		?

e) Write down the truth table for the full adder.

[4]

The question continues on the next page.

f) For the circuit of Figure 1.1, determine the Boolean functions g and f.

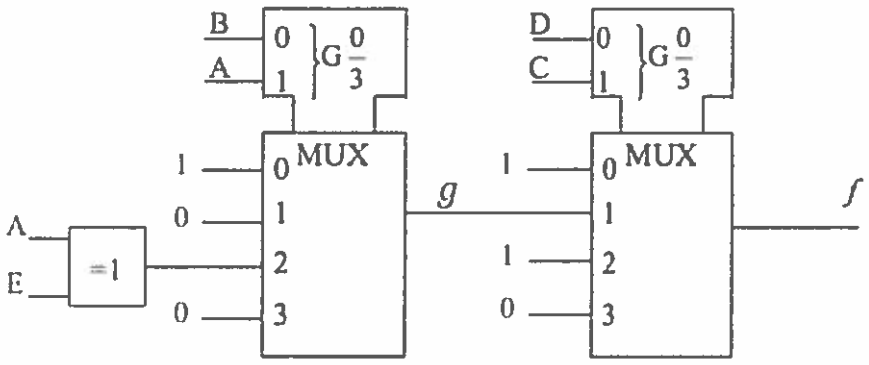

Figure 1.1

[8]

g) Sketch the gate-level circuit diagram for a 4-bit even parity generator.

[4]

Question 2

2. a) Figure 2.1 shows a finite state machine (FSM) implemented with a ROM that contains four 4-bit numbers. The ROM address signals are A[1:0] and the ROM data signals are D[3:0]. The D inputs of two flip flops are connected to the ROM data lines D1 and D0 as shown. The upper two data bits from the ROM D[3:2] form output signals F and G respectively. The outputs of the flip flops, Q0 and Q1, are connected to the address signals A0 and A1 of the ROM respectively. The contents of the ROM are shown in the table in Figure 2.2. The flip flops are initially in a reset state (i.e. Q0 = Q1 = '0').

(i) Draw a diagram showing the state and output values for the FSM.

[6]

(ii) Sketch the waveforms for the output signals F and G for at least 4 cycles of the clock.

[6]

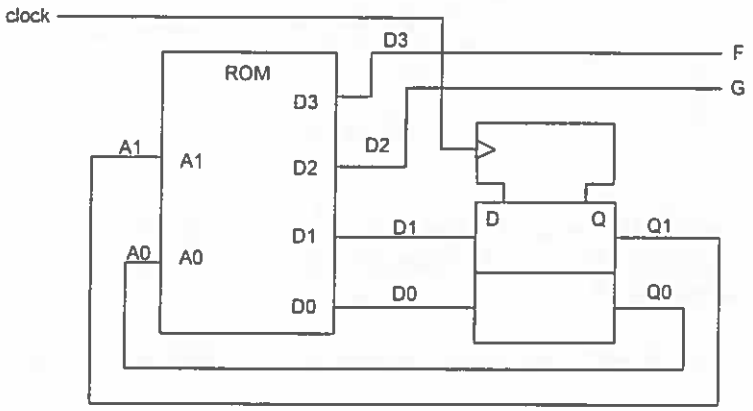

Figure 2.1

Address A[1:0]	ROM Data D[3:0]
0	0011
1	1000
2	0101
3	1110

Figure 2.2

The question continues on the next page.

b) The timing diagram of Figure 2.3 shows waveforms applied to the circuit shown in Figure 2.4. Sketch waveforms for S, R and Q. Assume that initially Q = 0.

[6]

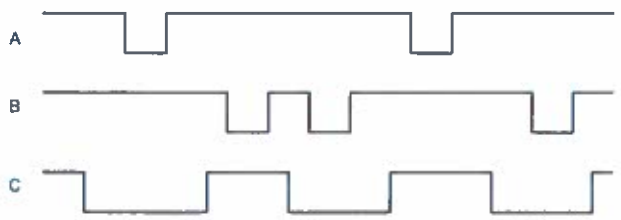

Figure 2.3

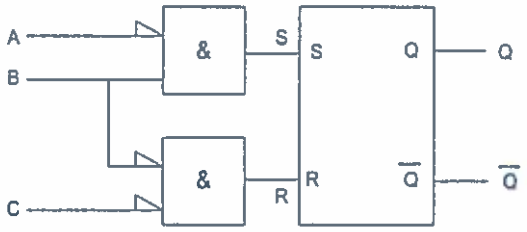

Figure 2.4

c) Figure 2.5 shows the circuit diagram (Fig. 2.5(i)) and symbol (Fig. 2.5(ii)) for a device known as a transmission gate, with output Q. The device uses two field-effect transistors (FETs) and an inverter.

(i) Write down the truth table for the transmission gate. State any assumptions you make.

[6]

(ii)Figure 2.5(iii) shows a circuit which uses transmission gates and additional inverters, with output Z. Write down the truth table for this circuit. What device does the circuit emulate?

[6]

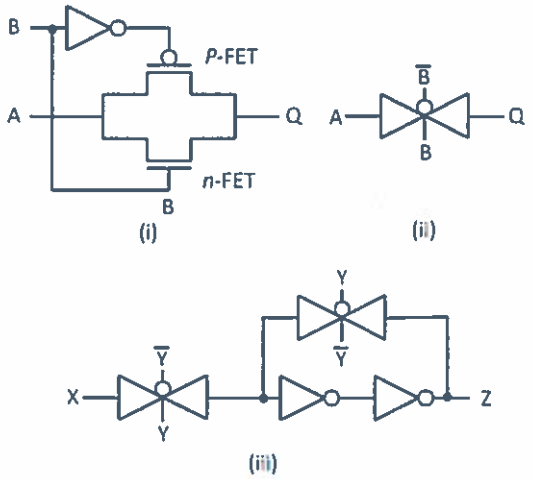

Figure 2.5

Question 3

3. Figure 3.1 shows a synchronous counter implemented using a finite state machine (FSM), which counts the sequence 1, 2, 4, 7, 5, 1 .... You may ignore unused states.

   a) Draw the Moore state diagram for the FSM.

   [5]

   b) Draw the state transition table for the FSM.

   [5]

   c) The FSM is to be implemented using J-K flip-flops and a combinational logic circuit. Determine the Boolean expressions necessary for this implementation.

   [15]

   d) Sketch a minimal circuit diagram for your design. This should show the J-K flip-flops, the gate-level circuit diagram for the combinational logic circuit, and indicate any connections.

   [5]

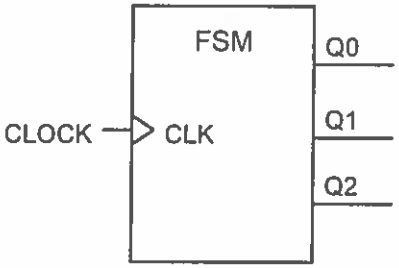

Figure 3.1

[THE END]