E1.4 SOLUTIONS

Solution 1

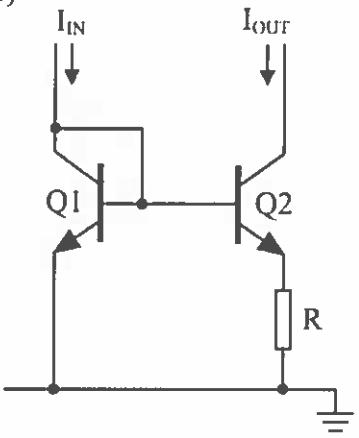
a) Assuming V_{DD} is sufficiently large for the MOSFET to be active, the drain current will be $I_D = K(V_{GS} - V_t)^2 = K(-V_S - V_t)^2$. The same current flows in the source resistor Rs, so we also have $V_S = I_D R_S$. Combining these equations we find V_S satisfies:

$$V_S^2 + (2V_t - 1/KR_S)V_S + V_t^2 = 0 \quad \text{or} \quad 4V_S^2 - 13V_S + 9 = 0$$

The roots are $V_S = 1$ V, 9/4 V, and we can reject the latter because it implies a sub-threshold value for V_{GS}. With $V_S = 1$ V, we have $(V_{GS} - V_t) = 0.5$ V and $I_D = K(0.5)^2 = 0.05$ mA.

At the minimum V_{DD}, the MOSFET will be at pinch-off, with $V_{DS} = 0.5$ V. The drain voltage will be $V_D = V_S + V_{DS} = 1.5$ V, and the supply voltage will be $V_{DD} = V_D + I_D R_D$. With $V_D = 1.5$ V, $I_D = 0.05$ mA and $R_D = 56$ kΩ, this gives $\mathbf{V_{DD} = 4.3\ V}$. [6]

b)



Ignoring base current, KVL in the loop including R and the EBJs gives:

$$V_{BE1} = V_{BE2} + I_{OUT}R$$

Using the reduced Ebers-Moll eqn we can express the V_{BE}s in terms of the input and output currents:

$$V_T \ln(I_{IN}/I_S) = V_T \ln(I_{OUT}/I_S) + I_{OUT}R$$

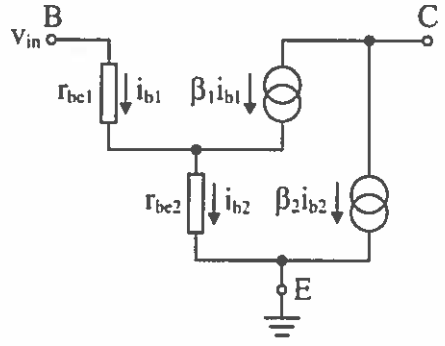
Cleaning this up gives:

$$V_T \ln(I_{IN}/I_{OUT}) = I_{OUT}R \quad \text{or} \quad \mathbf{I_{IN} = I_{OUT}\exp(I_{OUT}R/V_T)}$$

Rearranging the above equation, the value of R is given by $R = V_T \ln(I_{IN}/I_{OUT})/I_{OUT}$. With $I_{IN} = 100$ μA, $I_{OUT} = 10$ μA, $V_T = 25$ mV, this gives $\mathbf{R = 5.76\ k\Omega}$. [6]

c)

SSEC (helpful but not req'd):



The (signal) base-emitter voltages of the two transistors are:

$$v_{be1} = i_{b1}r_{be1} \quad ; \quad v_{be2} = i_{b2}r_{be2}$$

and the sum of these is the input voltage at the B terminal, i.e. $v_{be1} + v_{be2} = v_{in}$.

From the SSEC we can see that $i_{b2} = (1 + \beta_1)i_{b1}$. The quiescent base currents also satisfy $I_{B2} = (1 + \beta_1)I_{B1}$, so $r_{be2} = V_T/I_{B2} = r_{be1}/(1 + \beta_1)$. It follows that $i_{b2}r_{be2} = i_{b1}r_{be1}$ and hence that $v_{be2} = v_{be1} = v_{in}/2$ as required.

[5]

The total collector current is $i_c = g_{m1}v_{be1} + g_{m2}v_{be2} = (g_{m1} + g_{m2})v_{in}/2 = (I_{C1} + I_{C2})v_{in}/(2V_T)$. But $I_{C1} + I_{C2}$ is the total collector bias current, so $i_c = I_C v_{in}/(2V_T)$, and the transconductance is $g_m = i_c/v_{in} = I_C/(2V_T)$ which is half that of a BJT. [3]

d) Both MOSFETs are enhancement mode and diode-connected, and $V_{DD} > V_{tN} + |V_{tP}|$ so we know both devices are active. We can therefore write:

$$I_D = K_N(V - V_{tN})^2 = K_P(V - 3 - V_{tP})^2$$

Taking the –ve square root (to ensure opposite polarity devices are both above threshold), and rearranging, we obtain:

$$V = [3 + V_{tP} + \sqrt{(K_N/K_P)}V_{tN}]/[1 + \sqrt{(K_N/K_P)}] = [2 + \sqrt{(5/2)}]/[1 + \sqrt{(5/2)}] \Rightarrow \mathbf{V = 1.39\ V.}$$ [6]

e) With Class B, there is a dead-band at low signal levels where neither transistor is conducting (conduction angle < 180°), and this gives rise to cross-over distortion. The advantage is that the power consumption is low (~zero under quiescent conditions).

With Class AB, the transistors are biased so that there is a small overlap in the conduction (conduction angle > 180°), with both transistors conducting at low signal levels. The cross-over distortion is significantly reduced, but the power consumption is higher.

Class A has both transistors conducting at all times (conduction angle = 360°) so there is no cross-over distortion; however, the power consumption is very high. [6]

f) For $t < 0$, the transistor is conducting, with $I_B = (5 - 0.7)/220k = 19.5\ \mu A$. The circuit is in steady state, so the capacitor carries no current and, since $\beta I_B > V_{CC}/R_C$ (3.91 mA > 2.5 mA), we know the transistor is saturated. We therefore have $V_{OUT} = V_{CAP} = 0.2$ V at $t = 0^-$.

The transistor switches off at $t = 0$, and the capacitor starts to charge up via the two series resistors. The new steady-state value for V_{CAP} is +5 V, so the trajectory for V_{CAP} is:

$$V_{CAP} = 5 + (0.2 - 5)\exp(-t/\tau) = 5 - (4.8)\exp(-t/\tau)$$

where $\tau = (1k + 2k)\times 5n = 15\ \mu s$ is the time constant. Since $V_{OUT} = (2V_{CAP} + V_{CC})/3$, the corresponding trajectory for V_{OUT} is:

$$V_{OUT} = 5 - (3.2)\exp(-t/\tau)$$

V_A is the value of V_{OUT} at $t = 0^+$ which is $\mathbf{V_A = 1.8\ V}$.

V_B is the value of V_{OUT} at $t = 20\ \mu s$ which is $\mathbf{V_B = 5 - (3.2)\ exp(-20/15) = 4.16\ V}$. [5]

From the graph it is clear that when the transistor is switched on again at $t = 20\ \mu s$ it is initially in active mode. In this case, the value of V_{OUT} at $t = 20^+\ \mu s$ will be that of a Thévenin source with o/c voltage 4.16 V and source resistance 1k//2k = 667 Ω loaded by a current of $\beta I_B = 3.91$ mA. So, $\mathbf{V_C = 4.16 - 3.91m \times 667 = 1.55\ V}$. [3]

Solution 2

a) With the configuration shown, the quiescent emitter current is set by the bias current source, so we can write:

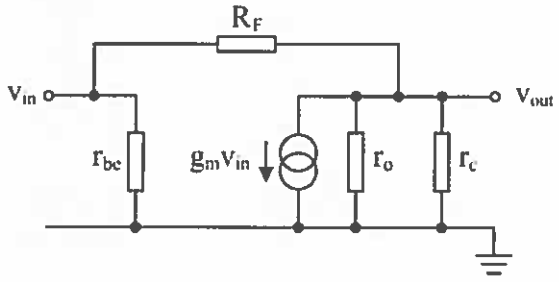
$$I_E = (1 + \beta)I_B = (1 + \beta)(V_{OUT} - V_{BE})/R_F = I_{BIAS} \Rightarrow R_F = (1 + \beta)(V_{OUT} - V_{BE})/I_{BIAS}$$

With $V_{OUT} = 4$ V, $I_{BIAS} = 1$ mA (neglecting r_c), $\beta = 200$, and assuming $V_{BE} \approx 0.7$ V, this gives **$R_F = 663$ kΩ.** [4]

Rearranging the above equation gives $V_{OUT} = R_F I_{BIAS}/(1 + \beta) + V_{BE}$. With $\beta = 300$ this gives **$V_{OUT} = 2.90$ V**, and with $\beta = 100$ it gives **$V_{OUT} = 7.26$ V.** [2]

The sensitivity of V_{OUT} to β variation could be reduced by adding a resistor between the base and ground, chosen so that it carries a current comparable to or larger than I_B. [2]

b) SSEC:



Applying KCL at the output node:

$g_m v_{in} + v_{out}/r_o + v_{out}/r_c + (v_{out} - v_{in})/R_F = 0$

$\Rightarrow A_v = v_{out}/v_{in} = -(g_m - 1/R_F)(r_o//r_c//R_F)$

Putting $g_m = I_C/V_T = 40$ mS, $r_c = 120$ kΩ

$r_o = V_A/I_C = 100$ kΩ $\Rightarrow$ **$A_v = -2016$.**

[6 (SSEC) + 3]

Applying KCL at the input node, the input current is:

$$i_{in} = v_{in}/r_{be} + (v_{in} - v_{out})/R_F = v_{in}[1/r_{be} + (1 - A_v)/R_F]$$

The input resistance is therefore $R_{in} = v_{in}/i_{in} = r_{be}//[R_F/(1 - A_v)]$. With $r_{be} = \beta/g_m = 5$ kΩ and $R_F/(1 - A_v) = 663\text{k}/2017 = 329$ Ω gives **$R_{in} = (5\text{k}//329) = 309$ Ω.** [3]

c) At signal frequencies, where the capacitor has negligible impedance, the feedback resistor in the original SSEC is replaced by shunt resistors of $R_F/2$ at the input and output. The voltage gain and input resistance will now be given by:

$$\mathbf{A_v = -g_m(r_o//r_c//R_F/2) = -0.04 \times 46.8\text{k} = -1872}$$

$$\mathbf{R_{in} = r_{be}//(R_F/2) = 4.96\ k\Omega}$$

The input resistance has increased from 309 Ω to ~5 kΩ. [6]

d) With the modified feedback network in place, the input resistance is dominated by the base-emitter resistance of the transistor. This can be increased by adding an emitter follower before the amplifying transistor or by converting the amplifying transistor to a Darlington pair. [Other solutions are also acceptable, e.g. source follower.] [4]

Solution 3

a) Since Q3 & Q4 are matched, we know $I_{D3} = I_{D4} = I$, so we can determine the gate/drain voltage of Q3 from:

$$I = K(V_{G3} + 10 - V_t)^2 \quad \Rightarrow \quad V_{G3} = -10 + V_t + \sqrt{(I/K)}$$

where we have taken the +ve square root to ensure Q3, Q4 are above threshold. With $I = 0.25$ mA, $K = 0.5$ mA/V^2, $V_t = 1$ V, this gives $V_{G3} = -9 + 1/\sqrt{2} = -8.3$ V. We then obtain the value of R_{BIAS} as $\mathbf{R_{BIAS} = -V_{G3}/I = 8.3\ k\Omega}$. [4]

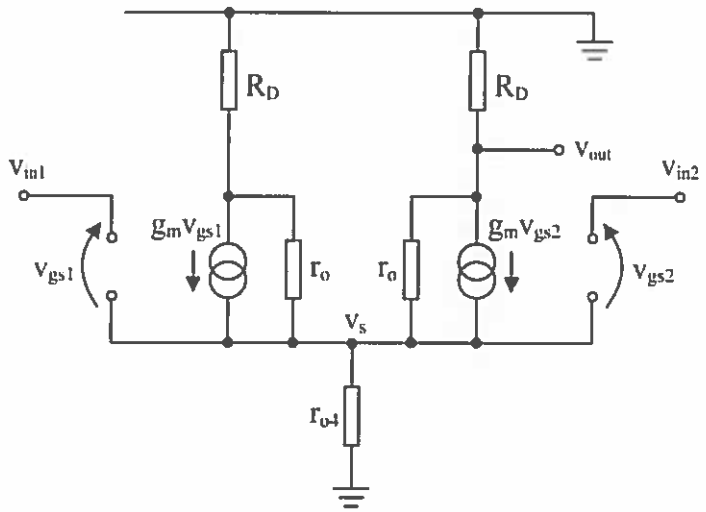
Under quiescent conditions, with $V_{IN1} = V_{IN2}$, we have $I_{D1} = I_{D2} = I/2 = 0.125$ mA. For a quiescent output voltage of +5 V we require $\mathbf{R_D = (10 - 5)/0.125m = 40\ k\Omega}$. [2]

Under quiescent conditions Q1 and Q2 have $V_{GS} = V_t + \sqrt{(I/2K)} = 1.5$ V. The voltage at the drain of Q4 is $V_{D4} = V_{IN} - V_{GS}$ so, when $V_{IN} = 0$ we have $\mathbf{V_{D4} = -1.5\ V}$. [2]

b) Upper limit: Q2 will remain active while $V_{D2} \geq V_{IN2} - V_t$ (and similarly for Q2). For the CMVR calculation we assume $V_{IN1} = V_{IN2} = V_{IN}$, in which case $V_{D2} = 5$ V while Q2 remains active, and the above inequality becomes $\mathbf{V_{IN} \leq 6\ V}$. [3]

Lower limit: Q4 will remain active while $V_{D4} \geq V_{G4} - V_t$. From part a) we know that $V_{G4} = (-9 + 1/\sqrt{2})$ V, so the above inequality becomes $V_{D4} \geq (-10 + 1/\sqrt{2})$. We also know from part a) that Q1 and Q2 have $V_{GS} = 1.5$ V, so the corresponding inequality for V_{IN} is $V_{IN} \geq (-8.5 + 1/\sqrt{2})$ V or $\mathbf{V_{IN} \geq -7.8\ V}$. [3]

c) SSEC:



From the symmetry of the circuit, when a purely differential voltage is applied there will be zero signal voltage at the source of Q1,Q2, i.e. $v_s = 0$ when $v_{in1} = -v_{in2} = v_{d/2}$. We can therefore analyse the RH half-circuit as a CE amplifier. Applying KCL at the output, the output voltage is obtained as:

$$v_{out} = g_m(R_D//r_o)v_d/2$$

$$\Rightarrow \quad \mathbf{A_d = v_{out}/v_d = g_m(R_D//r_o)/2}$$

[6 (SSEC) + 3]

Q2 has $I_D = 0.125$ mA, so $g_m = 2\sqrt{(KI_D)} = 0.5$ mA/V, $r_o = V_A/I_D = 800$ kΩ, giving $\mathbf{A_d = 9.5}$. [3]

d) The maximum gain will be achieved when the current mirror is used to couple Q1's drain current across to the output side. This will give a 2× enhancement of the gain. Also, R_D will be replaced by r_o in the gain expression, so we will have $A_d = 2 \times g_m(r_o//r_o)/2 = g_m r_o/2$.

With $g_m = 0.5$ mA/V and $r_o = 800$ kΩ this gives $\mathbf{A_d = 200}$. [4]