V CA

EE4-20
EE9AC3

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2012

MSc and EEE/ISE PART IV: MEng and ACGI

Corrected Copy

CMOS INTEGRATED CIRCUIT DESIGN AND TECHNOLOGY

Monday, 21 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks.

This is an OPEN BOOK examination.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : T. Constandinou
Second Marker(s) : C. Mehring

Information for Invigilators:

Students may bring any written or printed aids to the examination.

Information for Candidates:

Students may need a ruler and coloured pens (red, green, blue and black).

1. a) Discuss briefly the advantages and disadvantages of the following three logic design styles:

(i) Static logic;
(ii) Domino logic;
(iii) NP logic.

[6 marks]

b) Design a complex static logic gate that implements the following Boolean function in the form of a transistor-level schematic diagram.

$$X = \overline{A \cdot B + C \cdot (D + E)}.$$

[6 marks]

c) Design a full custom layout for this circuit as a symbolic or stick diagram. Assume all NMOS devices are 5/1 and PMOS devices are 10/1 (drawn dimensions).

[8 marks]

d) Using the digital model parameters given below in Table 1.1 for a short-channel (50nm) CMOS technology, estimate the worst-case delay through the gate when driving a 100 fF load capacitance based on the device dimensions specified in part (c).

[5 marks]

Table 1.1

Technology	R_n	R_p	**Scale factor**	$C_{ox} = C'_{ox} WL \cdot (scale)^2$
50 nm (short-channel)	$\frac{34k}{W}$	$\frac{68k}{W}$	50 nm	$(62.5\ aF) \cdot WL$

Where R_n and R_p are the effective switching resistances of the NMOS and PMOS devices respectively (units Ω), C_{ox} is the Gate-Oxide Capacitance (units fF) and W and L are the MOSFET channel width and length (units μm), i.e. drawn dimensions.

2. A full-custom layout design is shown below in Figure 2.1 for an integrated circuit implemented in a commercially available 0.18μm 1P6M CMOS technology (only 2 metal layers).

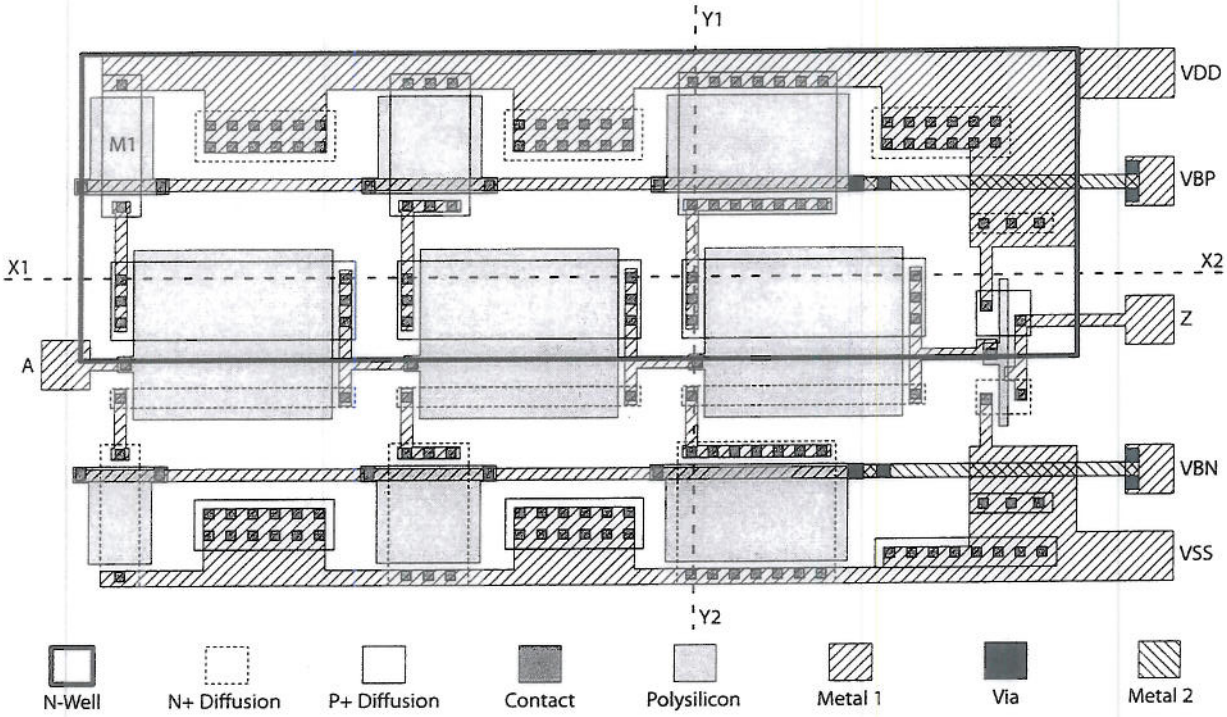


Figure 2.1

a) Extract and draw the transistor-level circuit schematic for this design.

Given that the transistor labelled M1 is of size W/L = (0.8μm/1.7μm), label all transistors in this circuit with their sizes.

[10 marks]

b) What function does this circuit perform? Provide a brief description on how this circuit works.

[5 marks]

c) Draw the vertical cross-sections along the lines X1-X2 and Y1-Y2. Label your diagrams indicating the n-well region and the different structures (eg. Metal1, Metal2), types and levels of doping (eg. P+, N+, etc).

[10 marks]

3. *This question relates to your design project (the SAR ADC or Image Sensor):*

a) In light of the experience you gained from the design project, describe the proper procedure for designing a full-custom integrated circuit. Highlight any lessons you learned from the design project.

[6 marks]

b) Discuss the impact of *process variation* and *device mismatch* on your design. Explain how you have engineered your solution to be robust to these through the design process.

[6 marks]

c) Draw a floorplan of the chip showing the relationship between the various modules and their approximate size. Describe how this would scale with technology, e.g. If you migrated your design from a 0.18μm to a 45nm CMOS technology.

[8 marks]

d) Describe your personal contributions to the project.

[5 marks]

4. You are required to design a 4Mbit DRAM in a 0.18μm CMOS technology based on the *open array* architecture using trench capacitor structures.

a) Draw the top-level system architecture identifying the main blocks and features.

[6 marks]

b) Using the technology data (Table 4.1) and design rules (Figure 4.2) given below, draw the layout of the *DRAM memory bit* using a *trench capacitor* as the storage element using minimum spacing rules. This cell should tessellate (i.e. self-connect if patterned in a large array). What is the silicon area required per bit of memory?

[6 marks]

c) Based on your answers to (a) and (b), calculate the *bitline* capacitance considering all the parasitic capacitances.

[10 marks]

d) Determine the minimum specification of sense amplifier minimum sense voltage given that the RAM will operate from a 1.8V supply.

[3 marks]

Table 4.1

Capacitance Type	Capacitance per unit length or area
Polysilicon to Polysilicon capacitance (lateral)	0.1 fF/μm (at 0.24μm spacing)
Polysilicon to Substrate capacitance – gate oxide (vertical)	9.0 fF/μm^2
Polysilicon to Substrate capacitance – field oxide (vertical)	0.2 fF/μm^2
Polysilicon to Metal 1 capacitance (vertical)	0.2 fF/μm^2
Metal 1 to Metal 1 capacitance (lateral)	0.2 fF/μm (at 0.24μm spacing)
Metal 1 to Substrate capacitance (vertical)	0.1 fF/μm^2
Diffusion contact (drain/source) capacitance (to substrate)	0.5 fF (per contact)
Trench capacitance	10 fF (per contact)

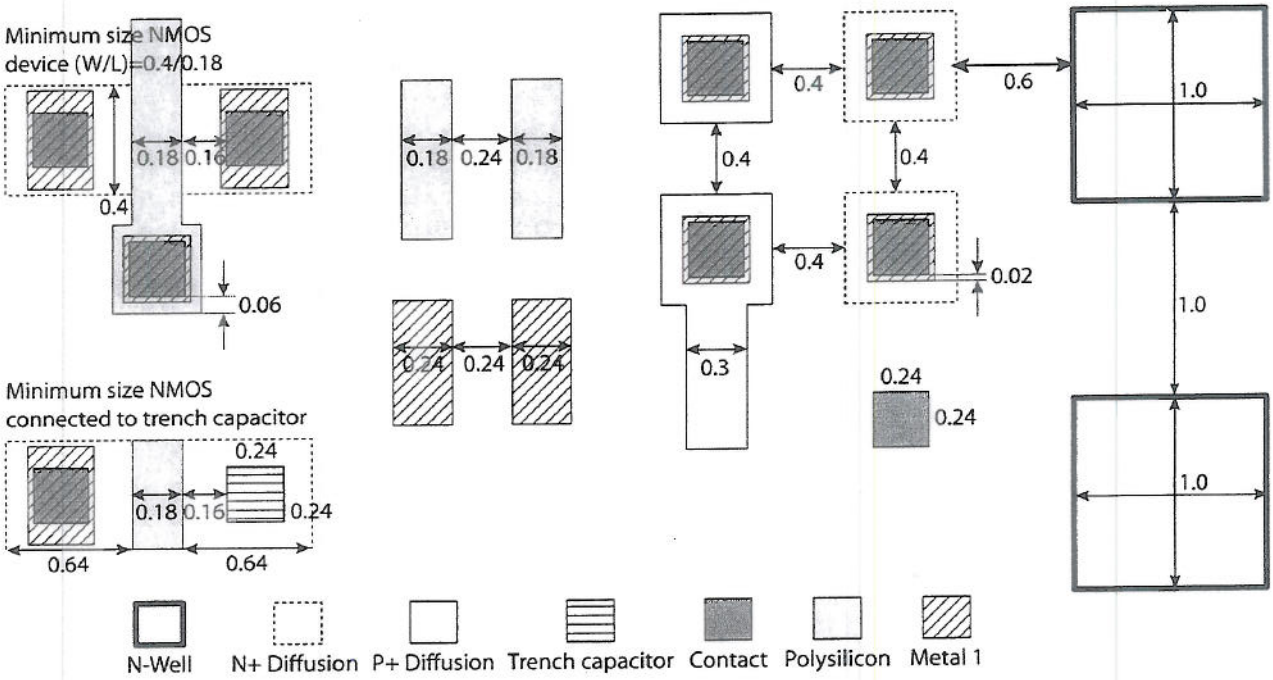


Figure 4.2

5. The *pixel* and *column* circuits to an *Active Pixel Sensor (APS)*-based image sensor designed in a 0.18μm CMOS technology are shown below in Figure 5.1.

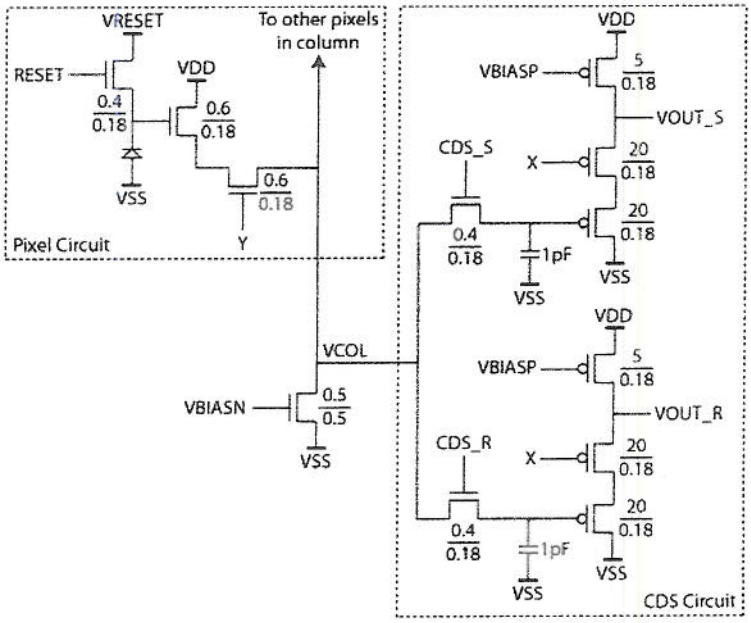


Figure 5.1

a) Describe how the circuit operates using a timing diagram, showing the signals RESET, VCOL, Y, X, CDS_R, CDS_S, VOUT_R, VOUT_S (and any other relevant node voltages) during illumination.

[10 marks]

b) Explain the meaning of Fixed Pattern Noise (FPN), where it originates from and how Correlated Double-Sampling (CDS) can be used to significantly reduce this.

[5 marks]

c) Sketch the layout and cross-section of two different pn-junction-based photodiode topologies that can be used in the circuit above and describe the advantages and disadvantages of each topology.

[5 marks]

d) The circuit shown below in Figure 5.2 shows a new type of pixel circuit reported recently in a research publication. Describe how you believe this circuit operates. What are the potential benefits and drawbacks of such a topology compared to that shown above?

[5 marks]

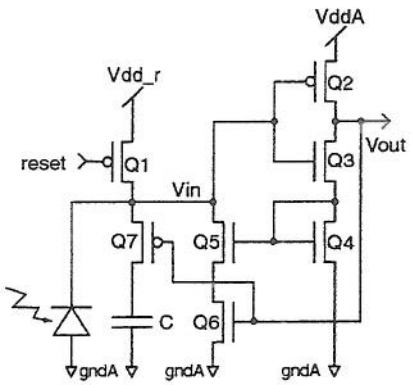


Figure 5.2

6. The *Address Event Representation (AER)* protocol is used to communicate asynchronous events from multiple independent *senders* using a high-speed (asynchronous) digital bus and a handshake (i.e. request and acknowledge signals). The idea is that when a sender wants to transmit an event, it sends an asynchronous pulse to the AER system. The input of the AER system has one latch per input, such that an input pulse from any sender will set the latch of that channel. If the bus is idle, the address of this sender is asserted onto the bus (via an address encoder) and the AER system outputs an AER_REQ signal. After the receiving device reads the bus value, it returns an AER_ACK signal back to the AER system to release the bus (by resetting the input latch).

a) A challenge in such asynchronous, event-based systems is dealing with collisions, i.e. when two senders wish to output an event at the same time. To resolve such a condition, an *arbiter* circuit can be used (shown below in Figure 6.1). Explain how this circuit operates and how it can be extended to take any number of inputs.

[7 marks]

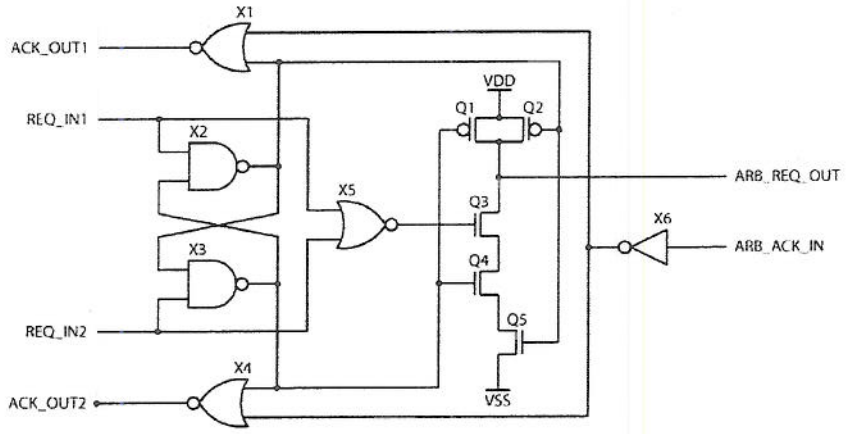


Figure 6.1

b) Considering an 8-input AER system, sketch a system architecture showing the 13 external I/O connections (8 sender inputs, a 3-bit AER bus, AER_REQ and AER_ACK) and the internal organisation. Draw a timing diagram to demonstrate the system operation given two of the senders (eg. channels 5 and 8) each signal a single event.

[10 marks]

c) To realise the address encoder (eg. 8-input to 3-bit word) in an AER system, a *wired-OR* topology is often used. Describe how this can be implemented (using a diagram if necessary) and outline the design considerations that need to be taken into account to achieve high speed.

[5 marks]

d) The layout to a device often used in implementing *wired-OR* address encoders is shown below in Figure 6.2. Describe the device and explain how this could be used to improve the performance the address encoder.

[3 marks]

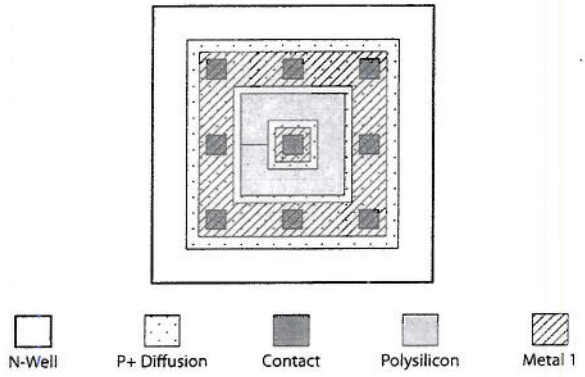


Figure 6.2

E4-20
E9AC3

IMPERIAL COLLEGE LONDON

Page 1/10

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2012

MSc and EEE PART IV: MEng and ACGI

CMOS INTEGRATED CIRCUIT DESIGN AND TECHNOLOGY (SOLUTIONS)

Monday, 21 May 10:00 am

Time allowed: 3 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

OPEN BOOK EXAM.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s):	T.G. Constandinou
	Second Marker(s):	C. Mehring

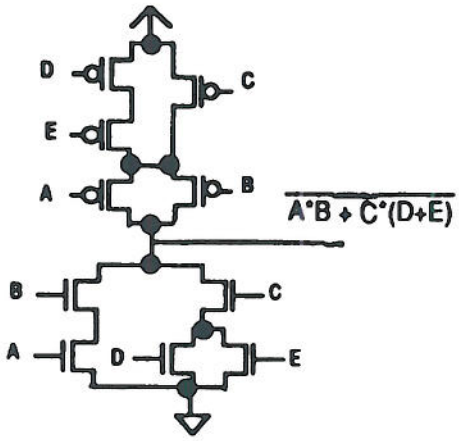
bookwork / new example

1. (a) (i) *Static logic* in CMOS realizes combinatorial circuits using an equal number of NMOS and PMOS devices such that for any given input combination, the output is always being asserted. Dynamic logic is distinguished from this by exploiting temporary storage of information in stray and gate capacitances. Dynamic logic circuits are usually faster than static counterparts, and require less surface area, but are more difficult to design, and have higher power dissipation. Dynamic logic gates also require a clock signal in its implementation of combinational logic circuits. Domino and NP logic are types of dynamic logic.

1. (a) (ii) *Domino logic* overcomes a common problem in dynamic logic when cascading gates such as to ensure the states are maintained between clock cycles. Domino logic solves this by inserting an inverter between logic stages. Features of domino logic: (1) They have smaller areas than conventional CMOS logic (as does all Dynamic Logic), (2) Parasitic capacitances are smaller so that higher operating speeds are possible, (3) Operation is free of glitches as each gate can make only one transition, (4) Only non-inverting structures are possible because of the presence of inverting buffer, (5) Charge distribution may be a problem.

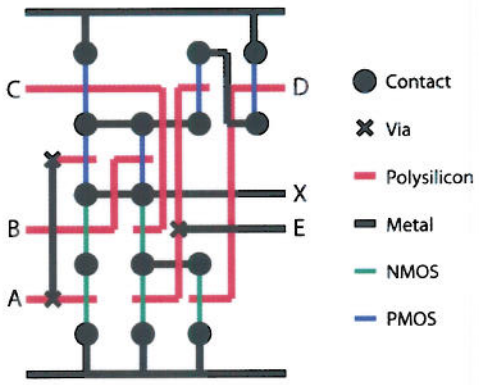
1. (a) (iii) A natural evolution of the domino logic is the *NP (or zipper) logic*. This implements the logic functions using alternating NMOS/PMOS pre-charge/pre-discharge transistors as well as also alternating the logic function realization using either NMOS or PMOS devices. This logic has a lower area occupancy, since there is no need of a static inverter, but has also a lower speed, given by the presence of PMOS transistors.

1. (b)



[6 marks]

1. (c)



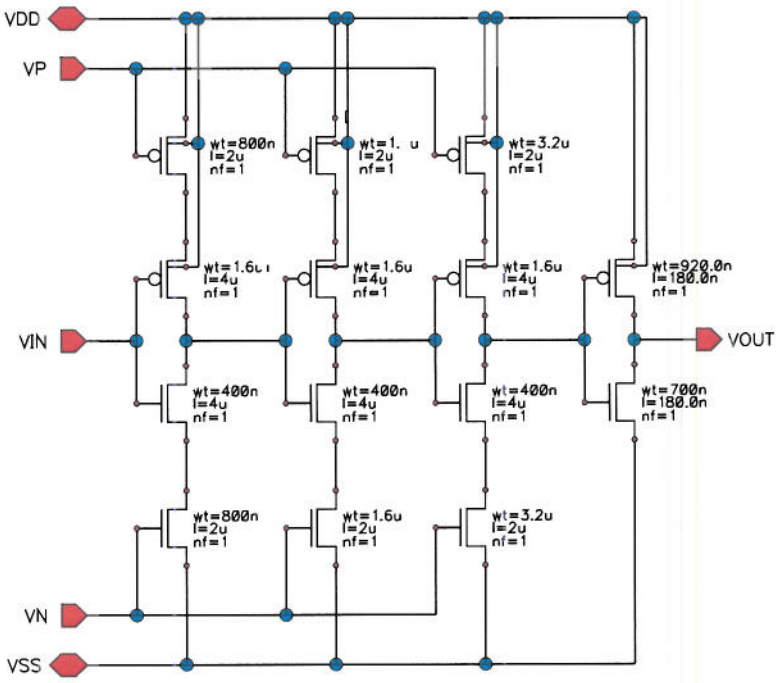
[8 marks]

1. (d) C_{OXN}=5(62.5aF)=0.31fF, C_{OXP}=10(62.5aF)=0.63fF. Therefore output capacitance is approximately, $C_{OUT}=C_{LOAD}$=100fF (gate capacitance negligible compared to load). Worst-case delay is when: $\bar{A}$, B, C, $\bar{D}$ and $\bar{E}$ (i.e. 3 PMOS devices are ON and in series). Therefore, $R_{out}=3R_p$=3(68K/10)=20.4K. t_{PLH}=0.7(20.4K)(100fF) = 1.43ns.

[5 marks]

new example / new theoretical application 3

2. (a) Circuit schematic shown below:



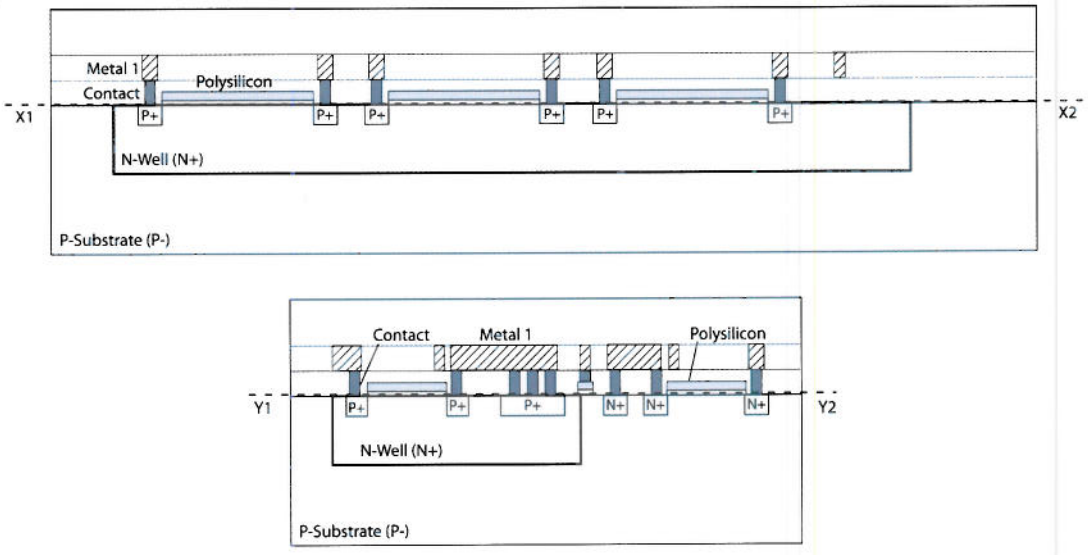
Marking scheme: 3 marks for correctly identifying there are 14 devices (7 NMOS and 7 PMOS), 4 marks for correct connectivity, 3 marks for W/L – allowing for some margin of error (+/-20%).

[10 marks]

2. (b) This is a current-starved inverter chain with the currents being limited at a ratio of 1:2:4. This circuit can be used to avoid excessive short-circuit currents when digital (or analogue) inputs have long rise/fall times, i.e. aren't sharp. Each inverter stage progressively "sharpens" the signal such that the final inverter connects directly to the supply to provide a x1 drive strength, sharp transition. However it should be noted that the first three inverter stages have long MOSFET devices and therefore the propagation delay is likely to be significant. This circuit has therefore obviously been optimized for power (and not speed).

[5 marks]

2. (c)



[10 marks]

bookwork / new example

3. (a) Should discuss generic mixed-signal design flow, starting from defining specifications, architecture, sub-block specs, implementation, etc. Expected to include examples of personal/project-specific lessons learnt demonstrating general competence in full-custom IC design. Also project/time management issues could be identified, with a post-analysis- i.e. what would you do differently knowing what you do now.

[6 marks]

3. (b) The answer should demonstrate a general understanding of device mismatch in analogue design and process variation mostly for digital. Project-specific examples necessary: For converter, mismatch effects the capacitor array matching (charge redistribution) or resistive. Also mismatch may impact offset to inverter/buffer amplifier. For imager, mismatch affects FPN and thus a requirement for the CDS circuit. If implementing column-level CDS, SF devices should be sized such as to minimize column-level mismatch. To give an example analysis or calculation with some numbers demonstrating competence/understanding to Vth/Id referred mismatch.

Marking as follows: [2] for general, [2] for specific examples related to project, [2] for detailed analysis and/or numerical example.

[6 marks]

3. (c) Floorplan should show good hierarchy, organisation and general engineering practice. Marks will be deducted if not detailed enough or badly drawn/annotated. Area estimate should show good understanding of routing overhead and be based on solid assumptions (stating them). Technology scaling needs to discuss impact of digital/analogue in 45nm, how will performance scale - eg. power supply will reduce, SNR will reduce, power will reduce, digital area will scale, etc.

Marking as follows: [4] for floorplan illstration, [2] for area estimate and [2] for technology scaling.

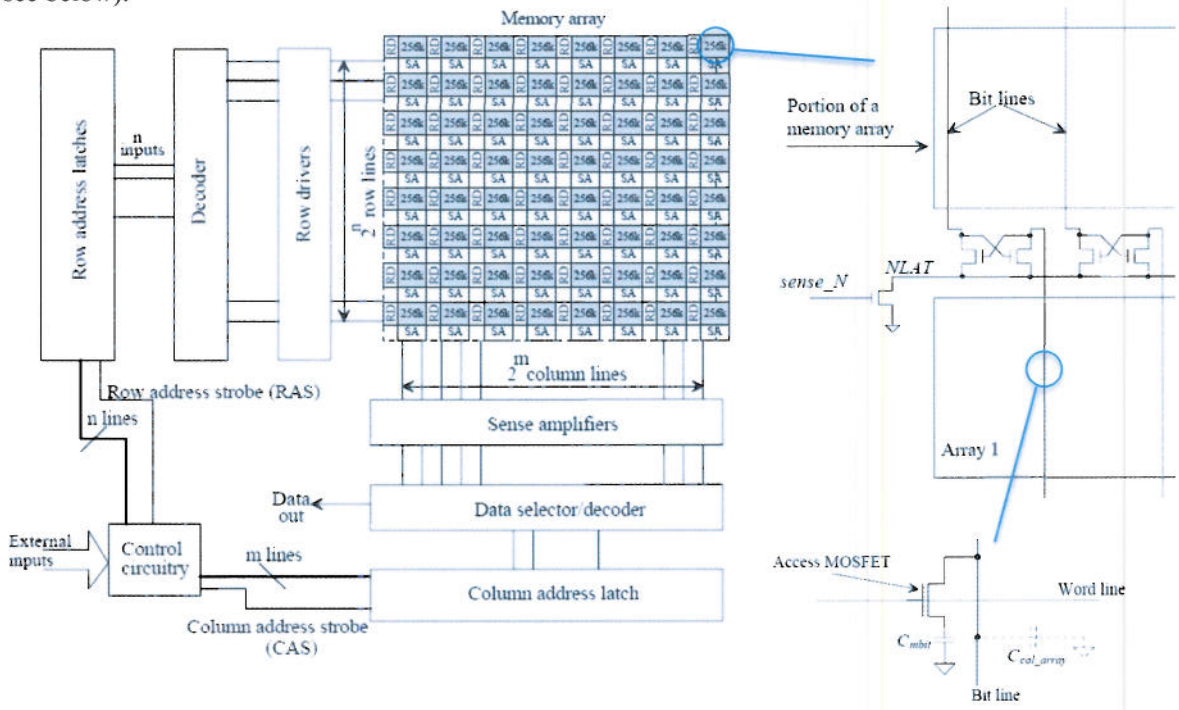
[8 marks]

3. (d) Personal contributions expected to be more than a list of sub-blocks (or simple tasks). Should describe in some detail what was implemented and/or the process and how this impacted the end-design. Eg. Was the main power-saving due to the digital logic block one group member implemented or due to good system architecture.

[5 marks]

Calculation for new example

4. (a) Answer here is not unique – should demonstrate an understanding to the challenges in implementing large RAM arrays – i.e. low level RAM should be organised in 256kbit arrays, with a 4x4 matrix of these. Top-level architecture should be based on Figures from chapter 16 adapted (eg. see below).

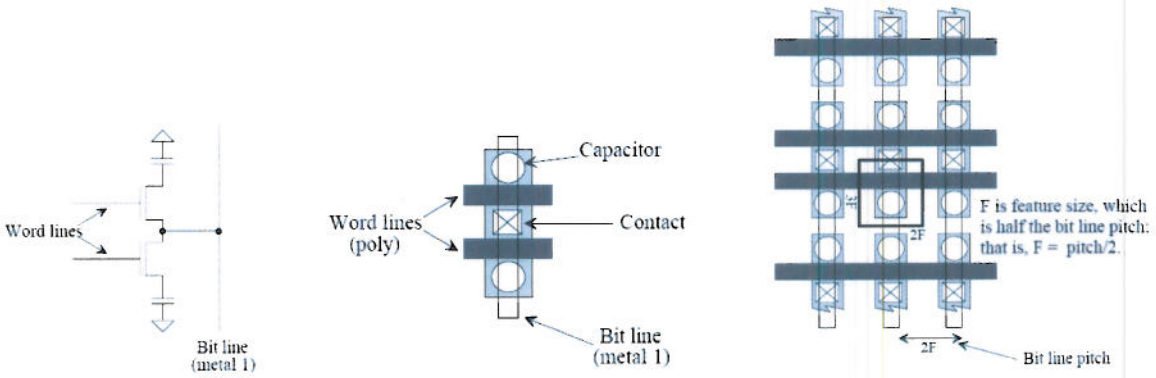


Marking as follows: 1 mark for using a two-tier hierarchy, 3 marks for low-level array and 2 marks for correctly describing how these will be linked together.

[6 marks]

4. (b) Based on Fig. 16.19 – using technology parameters (design rules) given:

[6 marks]



Width of Mbit cell = 0.4μm (width of minimum NMOS device) + 2 x 0.2μm (minimum spacing between NMOS devices – ½ each side) = 0.8μm

Length of Mbit cell = 1.46μm (length of minimum NMOS device) – 0.12μm (shared S/D contact) - 0.16μm (spacing between contacts not needed - shared S/D contact) + 0.2μm (½ minimum spacing between NMOS devices on side of trench capacitor) = 1.38μm

Mbit area = 1.38μm x 0.8μm = 1.104μm^2

4. (c) To calculate the bitline capacitance need to first calculate the total parasitic capacitance between metal 1 bitline and ground (i.e. all other adjacent nodes). Then bitline capacitance = N (number of wordlines = 512) * (metal parasitic capacitance per bit + drain contact capacitance).

Total parasitic capacitance per bit = v + h (vertical + horizontal parasitics)

Vertical parasitic capacitance per bit = a + b (= v)

a = (total metal 1 area (per Mbit) – ½ contact area – poly area) * (capacitance between Metal 1 to substrate)
= [(1.38μm * 0.24μm) – (0.24μm * 0.12μm) – (0.4μm * 0.18μm)] * 0.1fF/μm = 23aF
b = (poly area * capacitance between Metal 1 + poly 1)
= (0.4μm * 0.18μm) * 0.2fF/μm = 14.4aF
v = 23 + 14.4 = 37.4aF

Horizontal parasitic capacitance per bit (= h)
= 1.38 * 0.2 * 0.24/(0.8-0.24) = 118.3aF

Total parasitic capacitance per bit = v + h
= 37.4aF + 118aF = 155.4aF.

Bitline capacitance = 512 * (155.4aF + 0.5fF) = 335.6fF

[10 marks]

4. (d) Charge stored on one trench capacitor = Q = Cbit*Vdd = 10fF * 1.8 = 18fC.

[1]

Voltage change when storage capacitor connected to the bitline = Q/(Cbit+Cbitline) = 18fC/(335.6fF+10fF)=52.1mV.

[1]

Assuming ½ the charge leaks, the sense amplifier should be able to send 26mV.

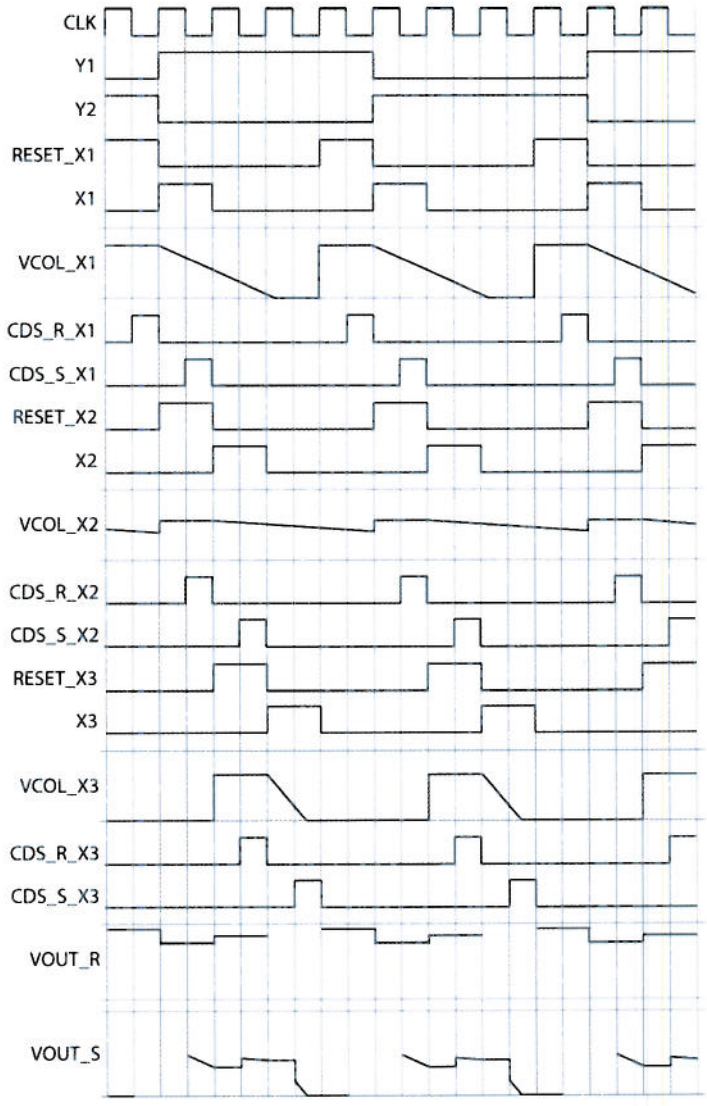
[1]

[3 marks]

New theory Calculation for new example

5. (a) The pixel circuit is a standard 3T active pixel sensor topology. It operates as follows: (1) the reset transistor is closed to reset the pixel and charge the storage node up to a reset voltage, (2) the reset transistor is the open to allow the capture to begin, (3) the photocurrent discharges the storage node, (4) the source follower buffers the storage node voltage to the bottom of the array. All pixels within a column share a current sink device and CDS circuit.

The CDS circuit consists of two track-and-hold circuits, to sample each column after the reset phase and after the sampling phase. In turn, each column's SAMPLE and RESET signals are sequenced to a global SAMPLE and RESET line, which feed the difference amplifier. A detailed timing diagram for a 4x4 array is shown below:



Assuming the input image is not changing and all pixels in column 1 are moderately illuminated, all pixels in column 2 are weakly illuminated and all pixels in column 3 are strongly illuminated (causing pixel saturation). Column 4 operation not illustrated. Also note the reset offset voltage of VCOL_X1-3 indicating mismatch in source followers. Operation of CDS is to sample this offset (see VOUT_R).

[10 marks]

5. (b) FPN is a static spatial "noise" that exists in an image sensor due to device mismatch mainly in the source follower devices. For example, if the image sensor is illuminated with a uniform light intensity, FPN can be observed as a random variation of captured levels. CDS is one popular approach to overcome this by taking two samples, one after resetting and one after sampling. By taking the difference between these any offset in the start (reset) value due to the VTH mismatch of the source

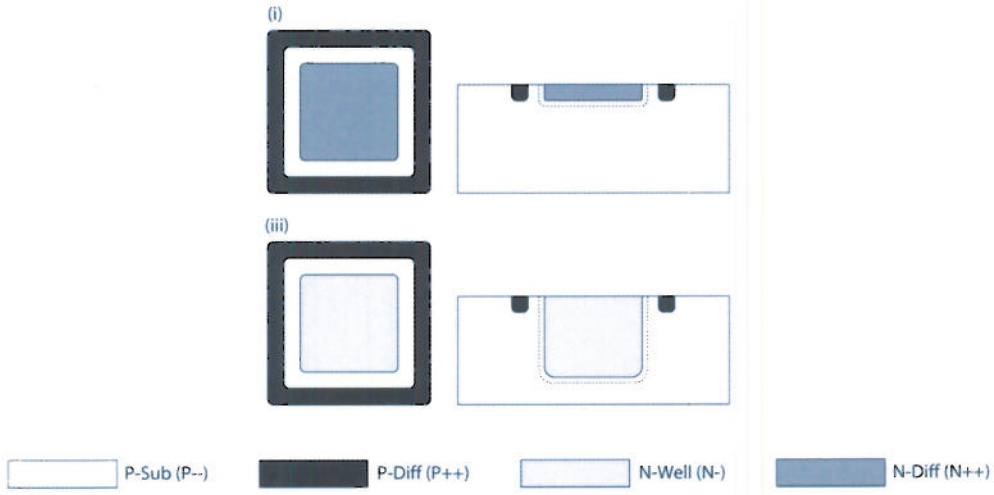
follower devices is removed. Also, see answer to part (a) – timing diagram for an illustration as to how this operates. Note the source followers in the output of the CDS circuit can use large devices to reduce any further mismatch (i.e. from column to column).

[5 marks]

5. (c) Shown below are: (i) a N+ diffusion/p-substrate and (iii) n-well/p-substrate photodiodes.

The N+ diffusion/p-substrate photodiode is generally preferable for smaller pixel size, higher pitch and/or fill factor but generally exhibit lower responsivity/quantum efficiency (due to high doping concentration). This type of diode also exhibits better short wavelength (i.e. blue/green) response due to shallower junction geometry.

The N-well/p-substrate photodiode has better responsivity/quantum efficiency (due to lower doping concentration). This diode also exhibits better long wavelength (i.e. red) response due to deeper junction geometry. A general disadvantage of well-based photodiodes is large well-to-well spacing rules, thus pitch/pixel size becomes compromised.



[5 marks]

5. (d) This shows a digital pixel circuit (i.e. the output voltage is a digital logic level), where the pixel intensity is proportional to the timing between the reset input of the output transition. The circuit operates as follows: (1) the reset transistor (Q1) is closed. This brings Vin up to Vdd_r which ensures Vout is LOW. This closes Q7 which charges capacitor C to VDD_r. (2) when the reset input is removed (Q1 open), the photocurrent starts to discharge capacitor C until Vin approaches the switch point of inverter Q2/Q3. As the short-circuit current begins to rise, positive feedback provided through current mirror Q4/Q5 discharges the capacitor completely (bringing down voltage Vin), such that the inverter switches to a HIGH logic level. The positive feedback massively reduces the power consumption. One advantage of such a pixel is the possibility of achieving a very high dynamic range, since the light intensity is converted to a timestamp. Also, this pixel is event-based and prioritises pixels with high intensities over those with low intensities. This could be extremely useful if the input scene is mostly dark with the region of interest having a higher intensity as the dark pixels can easily be discarded. In a traditional frame-based imager all pixels need to be sampled, irrespective of their value- thus an event-based imager can also reduce the output data bandwidth.

[5 marks]

New theory/new theoretical application

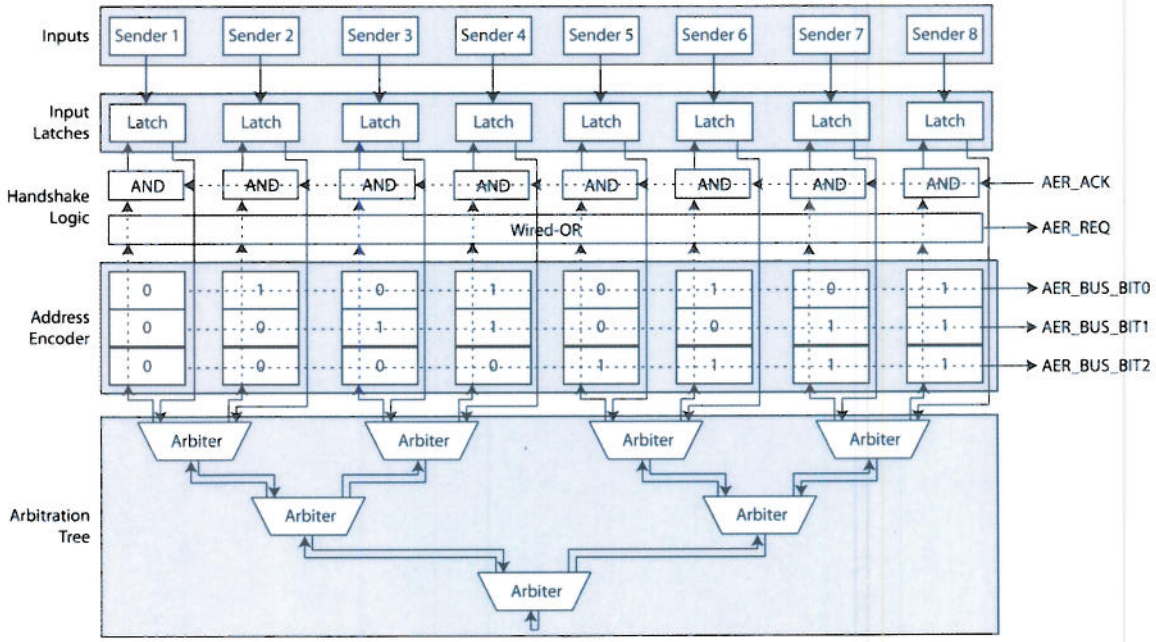
6. (a) An arbiter circuit is useful when needing to select which input arrives first (i.e. which rising edge occurs first). This is often used in asynchronous circuit design. This can be easily extended by building a binary arbitration tree out of arbiter elements. The arbitration tree has the task to select one of many requests, facilitated through a binary tree hierarchy. The arbiter cell operates on a single input pair, i.e. by selecting one of two outputs, resolving contention by using a high gain positive feedback element.

The arbiter circuit that has been given operates as follows:

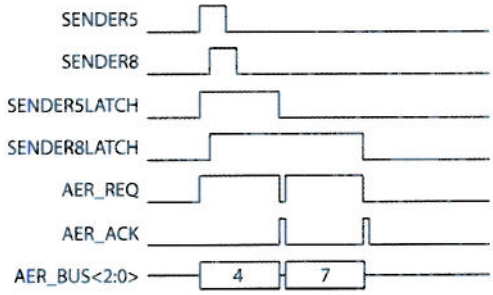
- If REQ_IN1 and/or REQ_IN2 is asserted, ARB_REQ_OUT is asserted to a higher arbitration level (logic OR operation).
- If either REQ_IN1 or REQ_IN2 is asserted, the RS flip-flop (X2, X3) is steered accordingly and on the arbiter receiving an ARB_ACK_IN signal from a higher level, it signals an ARB_OUTX to the requesting branch.
- If neither REQ_IN1 nor REQ_IN2 are asserted the RS flip-flop enters an undefined state, however this doesn't effect the operation since it will not pass an ARB_REQ_OUT signal to a higher level.
- If both REQ_IN1 and REQ_IN2 are asserted, the RS flip-flop selects the last asserted and on receiving an ARB_ACK_IN signal from a higher level, it signals an ACK_OUTX to the selected branch.

[7 marks]

6. (b) A possible system architecture is shown below showing the 8 inputs (top) and I/O signals (right).



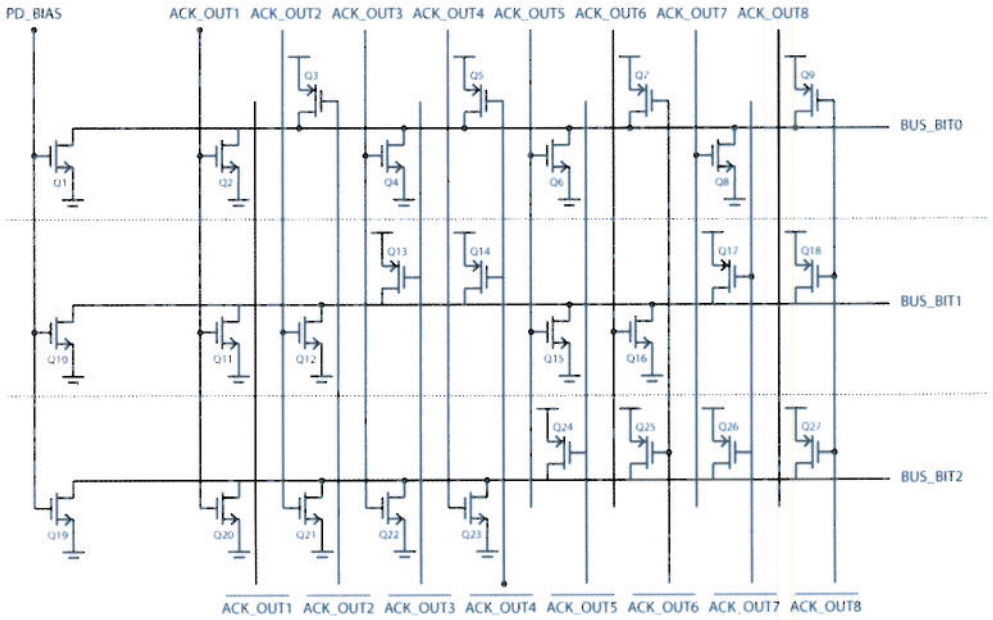
A timing diagram showing sender 5 signalling an event momentarily before sender 8 also signalling.



[10 marks]

10/10

6. (c) To realise the address encoder (eg. 8-input to 3-bit word) in an AER system, a *wired-OR* topology is often used. This uses one NMOS transistor per input, with all drains connected together and to a PMOS pull-up (current source). If any of the NMOS inputs are HIGH, it will pull the output LOW- and if all the inputs are LOW, the PMOS pull-up will pull the output high. In designing a wired-OR it is crucial to minimise the capacitance on the output node, by keeping all transistor sizes small (but strong enough to be able to pull the entire bus down when active) and as close together as possible (reduce interconnect parasitics). Also the PMOS pull-up needs to be able to source enough current, otherwise the low-to-high transition time will be slew-limited. An example 8-input wired OR configuration is showed below (using NMOS pull-down and PMOS drive transistors – note that the NMOS encoder devices are "optional"- can be used if both low-to-high and high-to-low transition times need to be fast).



[5 marks]

6. (d) This is an annular MOSFET (i.e. circular). The source contact is around the edge (perimeter), with the drain in the middle, and the gate in a ring. The field (VDS) is therefore radial. The advantage of using this device is a relatively large W/L can be achieved whilst keeping the drain capacitance (middle contact) to a minimum. Since the source will be connected to a power supply, its capacitance does not degrade performance.

[3 marks]