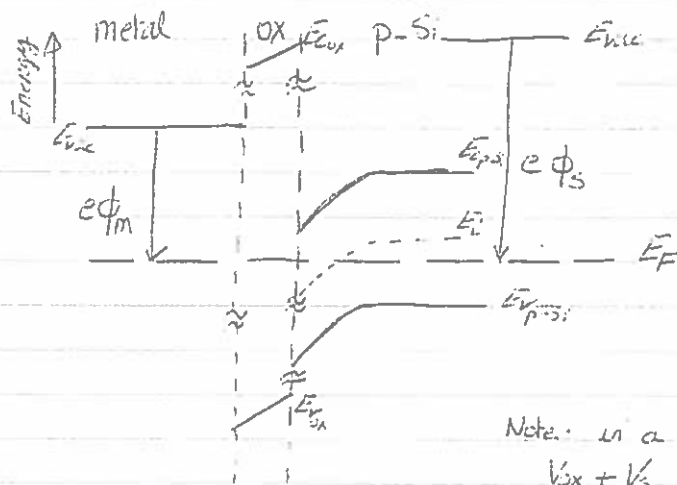


Q1
a)

[5]

Note: in a very good sketch
 $V_{ox} + V_s = e(\phi_s - \phi_m)$

b) 4) $V_s = \phi_F \Rightarrow n_s = N_A \exp\left(\frac{-\phi_F}{V_T}\right) \quad (1)$

onset of
depletion
[1]

$$\begin{aligned} n &= N_c \exp\left(-\frac{(E_c - E_F)}{kT}\right) \\ n_i &= N_c \exp\left(-\frac{(E_c - E_i)}{kT}\right) \end{aligned} \quad [2]$$

$$\Rightarrow \frac{n}{n_i} = \exp\left(\frac{-E_c + E_F + E_i - E_c}{kT}\right)$$

$$n = n_i \exp\left(\frac{E_F - E_i}{kT}\right) = n_i \exp\left(\frac{\phi_F}{kT}\right)$$

$$\Rightarrow p = p_i \exp\left(-\frac{(E_F - E_i)}{kT}\right) = p_i \exp\left(\frac{\phi_F}{kT}\right)$$

$$N_A = n_i \exp\left(\frac{\phi_F}{kT}\right) \quad (2)$$

(2) in (1): $n_s = n_i \exp\left(\frac{\phi_F}{kT}\right) \exp\left(-\frac{\phi_F}{kT}\right) = n_i \quad (i.i')$

$V_s < \phi_F$: depletion $V_s > \phi_F$: weak inversion.

②

$$V_s = 2\phi_F \Rightarrow n_s = N_A \exp(0) = N_A \quad \text{ii)} \quad [1]$$

ii) is the definition of threshold
[1]

$$\begin{aligned} \rightarrow V_s < 2\phi_F & \text{ weak inversion.} \\ V_s > 2\phi_F & \text{ moderate inversion.} \end{aligned}$$

Note: both $V_s = \phi_F$ & $V_s = 2\phi_F$ define the boundary between two operation regimes.

c) ideal long channel MOSFET in strong inversion:

$$I_{D_s} = \frac{\mu C_{ox} W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$\text{linear region: } I_{D_s} = \frac{\mu C_{ox} W}{L} (V_{GS} - V_{th}) V_{DS}$$

$$\text{threshold } V_{GS} = V_{th} \Rightarrow I_{D_s} = 0$$

in I_{D_s} equation:

$$0 = 2.85 \cdot 10^{-13} V_{th} - 4.425 \cdot 10^{-13}$$

$$V_{th} = \frac{4.425}{2.85} V = 0.5 \quad [1]$$

$$\text{Saturation } I_{D_s} = \frac{\mu C_{ox} W}{2L} (V_{GS} - V_{th})^2 = K V_{GS}^2 - 2K V_{th} V_{GS} + V_{th}^2 K$$

$$\text{Threshold } V_{GS} = V_{th} \Rightarrow I_{D_s} = 0$$

In I_{D_s} equation:

$$0 = 4.425 \cdot 10^{-11} V_{th}^2 - 3.9825 \cdot 10^{-11} V_{th} + \frac{8.960625}{2} \cdot 10^{-12}$$

$$0 = 4.425 V_{th}^2 - 3.9825 V_{th} + 0.8960625$$

$$V_{th} = \frac{+3.9825 \pm \sqrt{(3.9825)^2 - 4 \times 4.425 \times 0.8960625}}{2 \times 4.425}$$

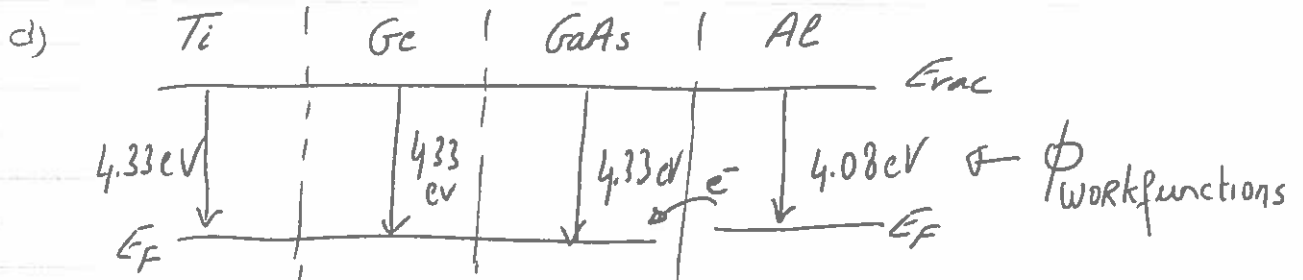
$$= 0.45V$$

[2]

③

$$DIBL = \frac{\left| \frac{V_{th}^{lin} - V_{th}^{sat}}{V_{DS}^{lin} - V_{DS}^{sat}} \right|}{|0.01 - 1|} = \frac{0.5 - 0.45}{0.01 - 1} = 0.051 \frac{V}{V} \quad [1]$$

$$= 51 \frac{mV}{V}$$



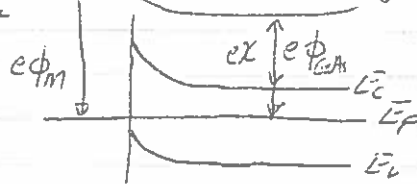
$E_G^{Ge} = 0.66 eV$
 $\Delta E_C = 4 - 4.1 = 0.1 eV$
 $E_G^{GaAs} = 1.42 eV$
 $\Delta E_V = \Delta E_G - \Delta E_C = 0.66 eV$

[5]

e) i) $\mu_1 = \mu_2 < \mu_3$ OR $\mu_3 > \mu_2 = \mu_1$ [3]

ii) $N_{sat2} < N_{sat3} < N_{sat1}$ OR $N_{sat1} > N_{sat3} > N_{sat2}$ [2]

f) n-type MISFET needs Schottky contact



$\phi_{GaAs} < \phi_{Ti}$ for Schottky contact

$$\phi_{GaAs} = \chi_{GaAs} + \frac{(E_C - E_F)}{e}$$

$N_D = 10^{15} cm^{-3} \rightarrow$ very low

[5]

(4)

$$\phi_{\text{GaAs}} = 4.1 \text{ eV} + 0.156 \text{ eV} \approx 4.26 \text{ eV}$$

$$n = N_c \exp\left(\frac{-(E_c - E_F)}{kT}\right)$$

$$\begin{aligned} E_c - E_F &= kT \ln\left(\frac{N_c}{n}\right) \\ &= 0.026 \ln\left(\frac{4.7 \times 10^{17}}{10^{15}}\right) = 0.156 \text{ eV} \end{aligned}$$

N_c will be the best theoretical choices because this gives the largest $V_{bi} = \phi_m - \phi_{\text{GaAs}}$.

g)
$$I_{O_G}^{\text{MESFET}} > I_{O_G}^{\text{JFET}}$$

The gate of a MESFET is determined by a Schottky barrier, that of a JFET by a pn-junction.

The leakage current through the gate is related to the barrier height.

Due to interface charges & traps in a metal/semiconductor contact the barrier height in a MESFET is lower than in a JFET.

$$\Rightarrow I_{O_G}^{\text{MESFET}} > I_{O_G}^{\text{JFET}}.$$

[5]

h) i) finFET

[1]

- ii)
- a) gate
 - b) buried oxide layer
 - c) gate oxide
 - d) Si substrate.

[4]

(5)

(2) a) Small drain voltage = linear (triode) region

[8]

W_{max} = maximum depletion width from gate = @ threshold
 $\rightarrow W_{max} = W_{dep} (V_s = 2\phi_F)$

formula sheet: * $W_{dep} = \left[\frac{2\epsilon_s \epsilon_0 (V_m - V)}{e N_A} \frac{1}{N_A} \right]^{1/2}$ for 1-sided junction

$V_m = 0$: only consider V_s and anyway $\phi_m = \phi_{p,n}$

$$W_{max} = \sqrt{\frac{2 \epsilon_s \epsilon_0}{e N_A} \frac{kT}{e} \ln\left(\frac{N_A}{N_D}\right)}$$

$$W_{max} = \sqrt{\frac{2 \times 2.85 \times 10^{-14} \text{ F/cm} \times 12 \times 0.026 \text{ eV} \ln\left(\frac{10^{16}}{1.45 \times 10^{10}}\right)}{1.6 \times 10^{-19} \text{ C} \times 10^{16} \text{ cm}^{-3}}} = 3.05 \times 10^{-5} \text{ cm}$$

$$* W_{DB} = \sqrt{\frac{2 \epsilon_s \epsilon_0 (V_{bi} + 0.026)}{e N_A}} \quad \text{assume depletion region extends in the lower doping side only.}$$

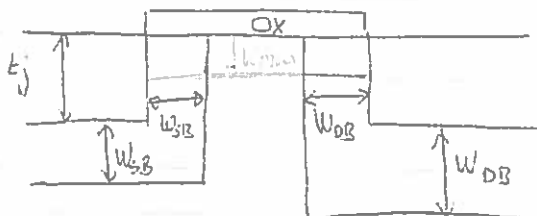
$$V_{bi} = \frac{kT}{e} \ln\left(\frac{N_A N_D}{n_i^2}\right) = 0.026 \ln\left(\frac{10^{16} \times 10^{20}}{(1.45 \times 10^{10})^2}\right) = 0.94 \text{ V}$$

$$W_{DB} = \sqrt{\frac{2 \times 2.85 \times 10^{-14} \text{ F/cm} \times 12 \times (0.94 + 0.026)}{1.6 \times 10^{-19} \text{ C} \times 10^{16} \text{ cm}^{-3}}} = 3.93 \times 10^{-5} \text{ cm}$$

* W_{SB} + same assumption as for W_{DB} and $V_s = 0 \text{ V}$

$$W_{SB} = \sqrt{\frac{2 \times 2.85 \times 10^{-14} \text{ F/cm} \times 12 \times 0.94}{1.6 \times 10^{-19} \text{ C} \times 10^{16} \text{ cm}^{-3}}} = 3.53 \times 10^{-5} \text{ cm}$$

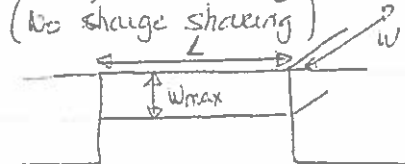
b)



[4]

6

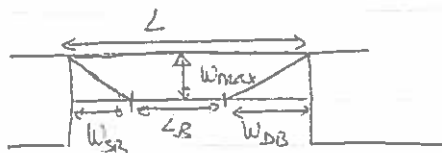
c) Q_G (charge controlled by gate when no charge sharing)



[8]

$$Q_G = \frac{-e N_A W_{max} L W}{L W} : \text{ (charge per gate area)}$$

Q_{GCS} (charge controlled by gate with charge sharing)



$$\text{area trapezium : } \left(\frac{L + L_b}{2} \right) \cdot W_{max}$$

$$Q_{GCS} = -e N_A W_{max} \left(\frac{L + L_b}{2} \right) W$$

$$= \frac{-e N_A W_{max}}{L W} \left(\frac{L + (L - W_{sb} - W_{db})}{2} W \right)$$

charge per gate area.

$$\text{charge lost : } \Delta Q = Q_G - Q_{GCS}$$

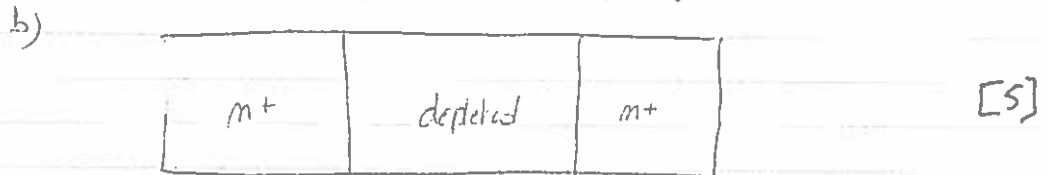
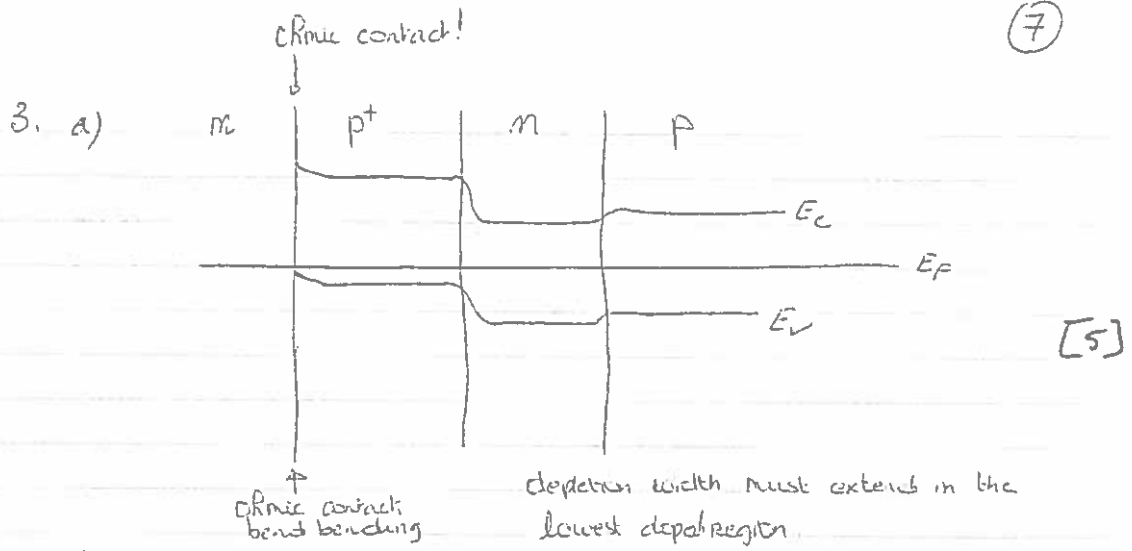
$$= \frac{-e N_A W_{max} W}{L W} \left(L - \left(\frac{2L - W_{sb} - W_{db}}{2} \right) \right)$$

$$= \frac{-e N_A W_{max} W}{L W} \left(\frac{2L - 2L + W_{sb} + W_{db}}{2} \right)$$

$$= \frac{-e N_A W_{max} W}{L W} \left(\frac{W_{sb} + W_{db}}{2} \right)$$

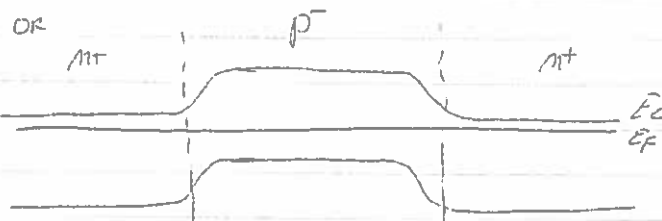
$$\Delta V_{th} = \frac{-e N_A W_{max}}{2 C_{ox} L} (W_{sb} + W_{db})$$

(7)



Note, in the MOSFET part of the course, we have seen that depleted means that the electron concentration $\leq n_i$

\Rightarrow possibilities



(8)

- c) Pinch-off occurs when the channel is depleted, \neq
 Since it is stated that the differences in doping concentration need to be taken into account, the depletion extending from the p-type region & that from the bulk both need to be taken into account.

Depletion from bulk

[10]

 W_B

$$\begin{array}{l} \text{channel } N_D = 10^{17} \text{ cm}^{-3} \\ \text{bulk } N_A = 5 \times 10^{17} \text{ cm}^{-3} \end{array} \left\{ \begin{array}{l} \text{only } 5\times \text{ different} \\ \Rightarrow \text{have to take both into account} \end{array} \right.$$

In formulae sheet
$$W = \sqrt{\frac{2\epsilon_0\epsilon_s (V_0 - V)}{e} \left(\frac{1}{N_A} + \frac{1}{N_D} \right)}$$

we only need W_p

we know that $w_n + w_p = W$ (1)

charge neutrality $w_n N_D = w_p N_A$ (2)

(2) $w_n = w_p \frac{N_A}{N_D}$ (3)

(3) in (1) $w_p \left(\frac{N_A}{N_D} + 1 \right) = W$

$$w_p \left(\frac{N_A + N_D}{N_D} \right) = W$$

$$V_B = 0 \rightarrow w_p = \sqrt{\frac{2\epsilon_0\epsilon_s (V_B)}{e} \left(\frac{N_A + N_D}{N_A N_D} \right) \left(\frac{N_D}{N_A + N_D} \right)}$$

$$w_p = W_{Bp} = \sqrt{\frac{2\epsilon_0\epsilon_s V_{Bp}}{e} \left(\frac{N_D}{N_A (N_A + N_D)} \right)}$$

Depletion from gate (p')

gate p' : 10^{20} cm^{-3}

channel n : 10^{17} cm^{-3}

since $N_A^+ \gg N_D^-$
 assume $w_{p+} \ll w_{n-}$
 \Rightarrow 1-sided junction.

$$W \approx W_{p'} = \sqrt{\frac{2\epsilon_0\epsilon_s (V_{Gp} - V_{Dp})}{e N_D}}$$

@ $V_{Gp} = V_p$ $t_n - W_{Bp} - W_{p'} = 0$

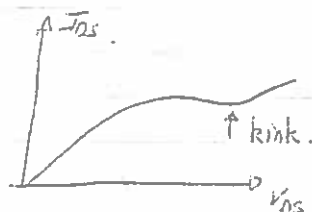
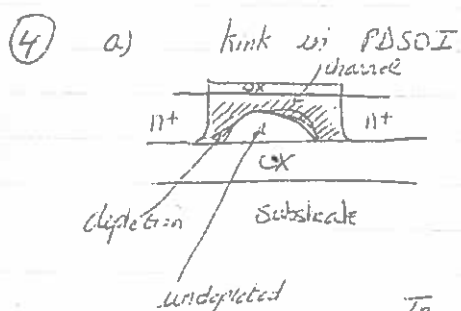
$$W_{p'} = t_n - W_{Bp}$$

9

$$\sqrt{\frac{2\epsilon_0\epsilon_{si}(V_{G_s}-V_P)}{eN_D}} = t_n - \sqrt{\frac{2\epsilon_0\epsilon_{si}V_{D_B}}{e}\left(\frac{N_D}{N_{A_S}(N_{A_S}+N_D)}\right)}$$

$$\frac{2\epsilon_0\epsilon_{si}(V_{G_s}-V_P)}{eN_D} = \left(t_n - \sqrt{\frac{2\epsilon_0\epsilon_{si}V_{D_B}}{e}\left(\frac{N_D}{N_{A_S}(N_{A_S}+N_D)}\right)}\right)^2$$

$$V_P = \frac{2\epsilon_0\epsilon_{si}V_{G_s}}{eN_D} + \left(\sqrt{\frac{2\epsilon_0\epsilon_{si}V_{D_B}}{e}\left(\frac{N_D}{N_{A_S}(N_{A_S}+N_D)}\right)} - t_n\right)^2$$



[5]

In PDSOI, the depletion region from the gate does not reach the BOX \rightarrow there is a region of undepleted Si. When the voltage V_{D_S} increases, impact ionisation occurs @ drain creating e^-h^+ pairs. e^- get extracted in D but h^+ build up in the undepleted region. This causes a change in charge in that region \rightarrow then change in Q_{dep} and thus a change in $\Delta V_{th} = \frac{\Delta Q_{dep}}{C_{ox}}$. $V_{th} \uparrow \Rightarrow (V_{D_S} - V_{th}) \downarrow \Rightarrow I_{D_S} \downarrow \rightarrow$ kink Cox

- b) advantages: (*) isolation between nMOS & pMOS removes latch-up [5]
(take 3 out of) (*) fewer processing steps needed

(10)

- (*) Reduce substrate leakage \Rightarrow lower power consumption.
- (*) Higher packing density
- (*) Smaller parasitic capacitance \Rightarrow higher speed

disadvantages

- (take 2 out of 3)
- (*) Completely surrounded by oxide \Rightarrow heating problem
 - (*) SOI substrate more expensive
 - (*) Transients: minority carrier ^{recombination} supply only available via ^{generation} processes

c) for fully depleted SOI t_c needs to be depleted
 @ $V_{GS} = 0V \Rightarrow$ the depletion region from the gate $d_G = t_c$. This depletion region can only be formed by the potential difference between $n-Si$ & ~~gate~~ gate contact.

from formulae list:

$$W_{depl} = \left[\frac{2\epsilon(V_{bi} - V)}{e} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) \right]^{1/2}$$

One-sided junction \Rightarrow
 $V_{GS} = 0V$

[10]

$$W_{depl} = \left[\frac{2\epsilon V_{bi}}{e N_A} \right]^{1/2}$$

the maximum width of t_c is when $V_{th} = 0V$
 thus $t_c \leq W_{depl}(V_{th} = 0V)$

V_{th} from formulae list:

$$V_{th} = \phi_m - \phi_s + 2\phi_F + \gamma \sqrt{2\phi_F}$$

$$\gamma = \frac{\sqrt{2e\epsilon N_A}}{C_{ox}}$$

(11)

$$V_{th} = 0 = \phi_m - \phi_s - 2\phi_F + \gamma \sqrt{2\phi_F}$$

$$\Rightarrow \phi_m = \phi_s - 2\phi_F + \gamma \sqrt{2\phi_F}$$

$$V_{bi} \text{ or } W_{depl} = ?$$

$$V_{bi} = 2\phi_F \quad \text{when max depletion region occurs.}$$

$$t_c^{\max} = \sqrt{\frac{2\epsilon_s 2\phi_F}{eN_A}} \quad \text{with } \phi_F = V_T \ln\left(\frac{N_A}{n_i}\right)$$

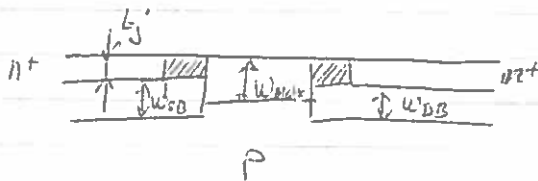
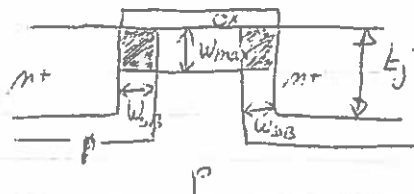
$$\Rightarrow t_{c\max}^2 = \frac{4\epsilon_s \phi_F}{eN_A}$$

$$\phi_F = \frac{eN_A t_{c\max}^2}{4\epsilon_s}$$

$$\phi_m = \phi_s - \frac{eN_A t_{c\max}^2}{2\epsilon_s \epsilon_0} - \gamma \sqrt{\frac{eN_A t_{c\max}^2}{2\epsilon_s \epsilon_0}}$$

$$\hookrightarrow \phi_m^{\min} = \text{minimum value of } \phi_m$$

(5)



$V_{bi} = 0 \quad V_{bi} = V_{th}$
 w_{max} : max gate induced depletion width

w_{sb}/w_{db} : S/D depletion width

area of shared charge

✓

[5]

area of shared charge

t_j

all other parameters same.

b) $t_j \downarrow \Rightarrow$ contact resistance \uparrow
 $\Rightarrow R_s \uparrow$ (Source resistance)

$$g.m = \frac{dI_{ds}}{dV_{gs}} \quad \text{or} \quad \frac{1}{g_m} = \frac{dV_{gs}}{dI_{ds}}$$

$$V_{GS}^{ext} = V_{GS}^{int} + R_S I_{Dc} \quad \text{assume } \begin{cases} I_G = 0 \\ I_{Dc} = I_{Dsat} \end{cases}$$

$$\frac{-1}{g.m^{ext}} = \frac{dV_{as}^{ext}}{dI_{Ds}}$$

$$= \frac{d(V_{GS}^{int} + R_S I_{DS})}{dI_{DS}} = \frac{dV_{GS}^{int}}{dI_{DS}} + R_S$$

$$\frac{1}{g_m^{\text{ext}}} = \frac{1}{g_m^{\text{int}}} + R_s$$

[81]

$$\frac{1}{g_m^{\text{ext}}} = \frac{1 + R_s g_m^{\text{int}}}{g_m^{\text{int}}}$$

$$g_m^{ext} = \frac{g_m^{int}}{1 + R_s g_m^{int}}$$

ext: externally & manual gm

int : internally " " (without R_5 parasite)

c)

(13)

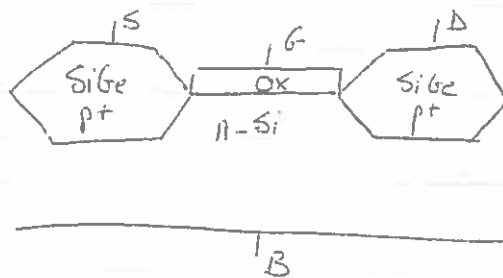
c) i) elevated source-drain technology.

[2]

ii) SiGe has a larger lattice constant than Si, then when the Si channel is surrounded by SiGe (e.g. in the source & drain areas) it puts Si under compressive strain increasing hole mobility (for pMOS).

[2]

iii)



[3]