

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2012

EEE PART IV: MEng and ACGI

Corrected Copy

Q5 SP

FACTS AND POWER ELECTRONICS

Tuesday, 8 May 2:30 pm

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks.

Please use a separate answer book for Sections A and B.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : T.C. Green, B.C. Pal
 Second Marker(s) : B.C. Pal, T.C. Green

[4-49]

Information for Candidates

Charge on the electron: $1.6 \times 10^{-19} \text{ C}$
Boltzmann's Constant: $1.38 \times 10^{-23} \text{ m}^2 \text{ kg s}^{-2}$

Section A

1.

a)

- i) Together, the matrices T and T_R given below, can perform the DQ transformation in which a balanced positive-sequence three-phase voltage set is converted to a simpler representation. Explain how the matrices shown achieve that. [3]

$$T = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad T_R = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 0 \\ -\sin(\omega t) & \cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

- ii) For each of the signals u_1 , u_2 and u_3 , describe the expected form of transformed signals when the matrices T and T_R are applied. [4]

$$u_1 = \begin{bmatrix} U_1 \cos(\omega t + \frac{\pi}{6}) \\ U_1 \cos(\omega t + \frac{2\pi}{3} + \frac{\pi}{6}) \\ U_1 \cos(\omega t - \frac{2\pi}{3} + \frac{\pi}{6}) \end{bmatrix} \quad u_2 = \begin{bmatrix} U_0 + U_2 \cos(\omega t) \\ U_0 + U_2 \cos(\omega t - \frac{2\pi}{3}) \\ U_0 + U_2 \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \quad u_3 = \begin{bmatrix} U_1 \cos(\omega t + 30^\circ) \\ U_1 \cos(\omega t - 90^\circ) \\ U_1 \cos(\omega t + 150^\circ) \end{bmatrix}$$

- iii) Describe how the DQ transform is applied to the control of a power converter. [3]

- b) Figure 1.1 shows an inverter arranged to export power from a DC-link to which a PV array has been attached. The inverter is to be operated under closed-loop current control in DQ form.

- i) Explain why a phase-locked loop, PLL would be needed and describe a suitable form of PLL. [3]

- ii) Describe how the reference values of the D- and Q-axis currents should be formed in this application. [4]

- iii) Sketch the format of the current control system including feed-forward terms for the inductive voltage drop. [3]

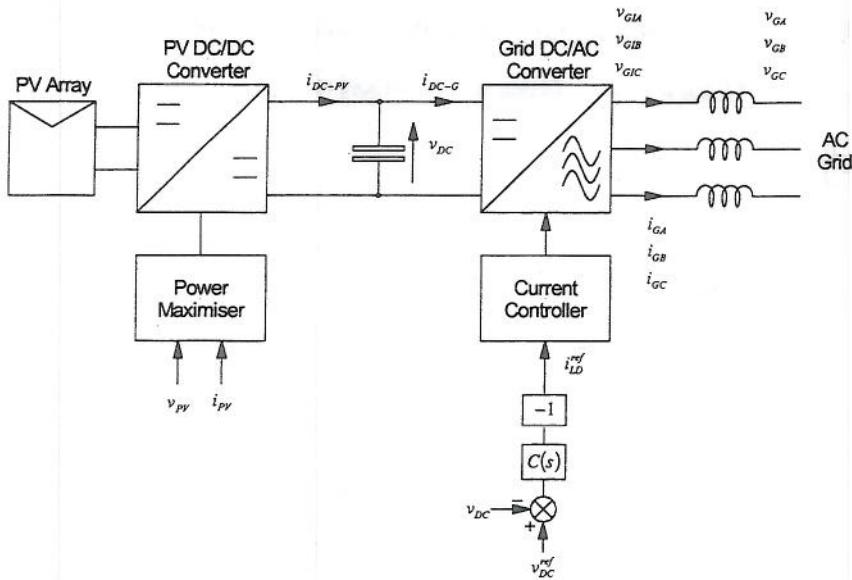


Figure 1.1, A Grid connected inverter acting as an interface for a PV Array

2.

- a) Explain why multilevel converters are used for very high power converters. [4]
- (b) Figure 2.1 shows an example of the modular multi-level converter (MMC).

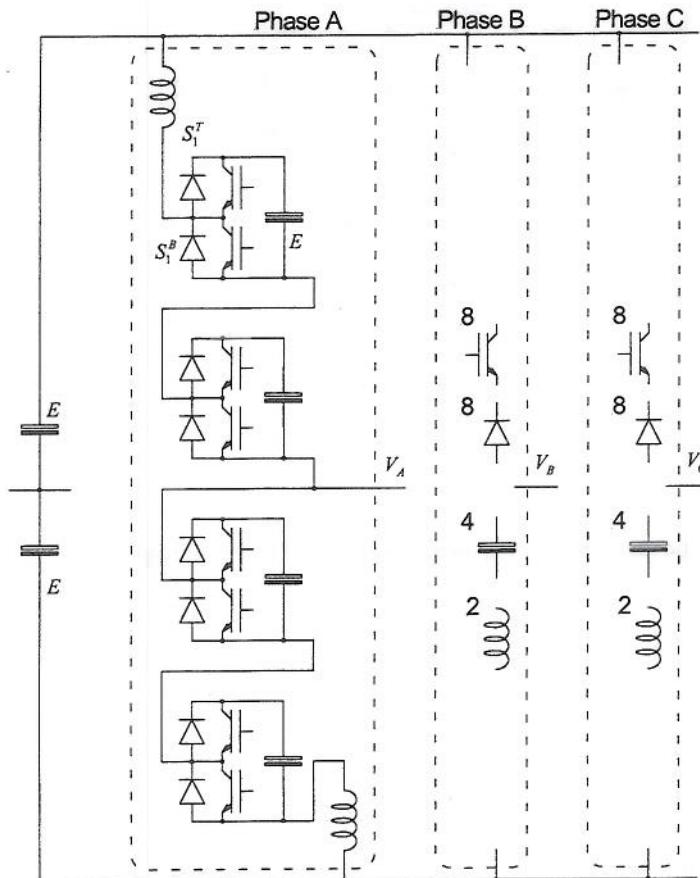


Figure 2.1, an example MMC

- i) Explain the operation of the MMC in terms of how the AC voltages are synthesized and the current paths that need to be established [5]
- ii) Show that the energy exchange with the cells of one arm is given by the equation below and describe the condition that ensures the energy exchange is zero. [7]

$$E_{Arm} = \frac{1}{3}V_{DC+}I_{DC}T - \frac{1}{2}V_{Ph}I_{Ph}T$$

- iii) Explain the advantages of the MMC over other topologies of multi-level converter. [4]

3.

- a) Compare and contrast the three common power semiconductor switching devices: thyristors, IGBTs and MOSFETs. In your answer, discuss the different properties of each, their approximate ratings and the features of each device. [6]
- b) Explain why it is not possible to make a single power semiconductor device block an arbitrarily large voltage or conduct and arbitrarily large current. [3]
- c) A thyristor valve, shown in figure 3.1, is subjected to high rates of change of voltage in V_{valve} . Explain why this valve may fail and describe a simple solution to prevent failure under such circumstances. [3]

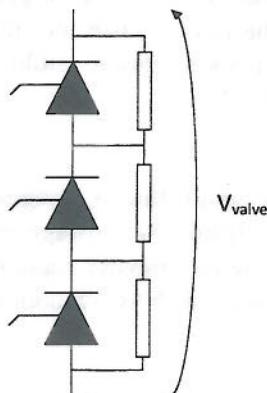


Figure 3.1 Series thyristor valve

- d) It is proposed that a diode valve capable of conducting 14 kA is made from 8 diodes capable of conducting 2 kA each. Due to non-identical thermal mounting of the devices, the temperature range expected in the devices under operation is expected to be between 320 and 340 K. The devices can be assumed to have a reverse saturation current of $1 \times 10^{-11} \text{ A}$ and obey the Shockley equation.
- Show that under worst-case conditions, the voltage across the diodes with no sharing network present is approximately 0.944 V and show that forced current sharing using resistors is necessary. [2]
 - Hence, calculate the smallest value of resistors in the sharing network that enable all devices to operate within specification and comment on whether physical sharing resistors need to be added. [3]
- e) Explain the relative merits of *normally-on* (*i.e.* on with zero gate-source voltage) versus *normally-off* (*i.e.* off with zero gate-source voltage) power semiconductor switches in the context of Silicon carbide MOSFETs and JFETs. [3]

Section B

4.

- a)
- i) What is meant by 'natural impedance' or 'surge impedance' in AC Power transmission line? [3]
 - ii) Explain the importance of the concept of the surge impedance loading of an AC power transmission. [4]
 - iii) A 230 kV double-circuit AC transmission line was built 30 years ago with twin conductors per-phase. To accommodate the growth in demand and generation in the system, the twin conductors are being replaced with quad conductors of similar individual geometry. What impact will this re-engineering have on the natural impedance of the line and consequently on the power transfer capacity? [3]
 - iv) Instead of opting for quad conductor arrangement, the utility also had an option to reinsulate the line to raise the transmission voltage to 345 kV level. What impact such option could have had on the power transfer capacity of the line? [3]
- b) A 100-mile long, 230 kV double-circuit line is designed to carry 300 MW. The receiving end of the line suffers from low voltage problem when the line is overloaded. It is decided to increase the transfer capacity of the line to 450 MW. Explain what would be the best choice of FACTS controller solve this problem. [4]
- c) What are the factors influencing the maximum thermal limit in AC power line? [3]

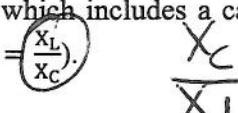
[4-49]

5.

a)

- i) Describe what is meant by a '*loop flow*' in a power transmission system? [3]
- ii) How can '*loop flow*' be controlled? Explain your answer with a simple example of a meshed system. [5]

b) A long (greater than 200 mile) 345 kV AC transmission circuit, shown in Fig 5.1 transfers a power of 350 MW. A wind farm of 100 turbines with a capacity of 2 MW each is planned close to the sending end of the line. The transmission operator is planning a controllable series compensator to help transfer the additional power from wind farm through existing line.

- i) Derive the power (both real and reactive) versus angle relationship of a transmission line which includes a capacitor in terms of the degree of compensation ($k_c = \frac{X_L}{X_C}$).  [6]
- ii) Determine the degree of compensation required to transfer the power from the wind farm (when it is producing at full capacity) while maintaining the steady-state power transfer margin at the same level as the uncompensated case. Assume 1.0 p.u. voltage at the sending and receiving ends. The line impedance is 0.2 p.u and is purely reactive. The base power is 100 MVA. [6]

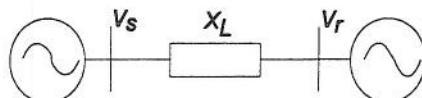


Fig 5.1: A simple interconnected power system model

- 6.
- a) Briefly describe the function of a static VAr compensator (SVC) with the help of a sketch of circuit and the V - I characteristic. [7]
 - b) How is SVC modelled in each of the following:
 - i) power flow studies [4]
 - ii) small-signal stability studies [5]
 - c) A steel plant has a large induction furnace to melt raw materials used to produce steel. The power demand of the induction furnace behaves as a fluctuating load leading to fast voltage variation at the supply substation. This affects other loads connected to the substation. The plant also has several important loads that cannot tolerate transient voltage dips. Describe how a suitable FACTS controller would be chosen to solve this problem. [4]

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[4-49]

Information for Candidates

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Section A

1.

(a)

- (i) Together, the matrices T and T_R given below, can perform the DQ transformation in which a balanced positive-sequence three-phase voltage set is converted to a simpler representation. Explain how the matrices shown achieve that. [3]

$$T = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \quad T_R = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 0 \\ -\sin(\omega t) & \cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

[Book work]

The third row in T has equal terms and identifies the common-mode (zero-sequence component). The first and second rows are trigonometric factors that resolve three vectors at 120° to two vectors at 90° .

T_R leaves the zero-sequence term unaltered but applies a backward rotation at ωt to the remaining terms. Thus, positive sequence signals are transformed to stationary signals which express amplitude as the combination of the two terms and angles as their ratio but have no regular time varying component.

[3 marks]

- (ii) For each of the signals u_1 , u_2 and u_3 , describe the expected form of transformed signals when the matrices T and T_R are applied. [3]

$$u_1 = \begin{bmatrix} U_1 \cos(\omega t + \frac{\pi}{6}) \\ U_1 \cos(\omega t + \frac{2\pi}{3} + \frac{\pi}{6}) \\ U_1 \cos(\omega t - \frac{2\pi}{3} + \frac{\pi}{6}) \end{bmatrix} \quad u_2 = \begin{bmatrix} U_0 + U_2 \cos(\omega t) \\ U_0 + U_2 \cos(\omega t - \frac{2\pi}{3}) \\ U_0 + U_2 \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \quad u_3 = \begin{bmatrix} U_1 \cos(\omega t + 30^\circ) \\ U_1 \cos(\omega t - 90^\circ) \\ U_1 \cos(\omega t + 150^\circ) \end{bmatrix}$$

[Interpretation]

u_1 is a negative sequence term offset by $+\pi/6$. It will transform to double frequency oscillatory terms (backward rotational transformed backward again).

[1 mark]

u_2 has a DC zero-sequence term that will appear in the third element of the transformed vector and a sportive sequence term with no phase offset which will appear in the first term of the transformed vector (the second term will be zero).

[2 marks]

u_3 is positive sequence voltage with an offset of 30° . $U_1 \cos(30^\circ)$ is the first term; $U_1 \sin(30^\circ)$ is the second term and the third tem is zero.

[1 mark]

- (iii) Describe how the DQ transform is applied to the control of a power converter. [3]

[Bookwork]

The design approach is:

- Transform plant model equations by applying T and T_R .
- Design controller for DQ model

Then in operation

- Apply reference signals in DQ form
- Convert feedback signals to DQ form
- Apply error in DQ form to controllers
- Convert output of controller from DQ form to abc form and apply that to the physical plant.

[3 marks]

- (b) Figure 1.1 shows an inverter arranged to export power from a DC-link to which a PV array has been attached. The inverter is to be operated under closed-loop current control in DQ form.
- (i) Explain why a phase-locked loop, PLL would be needed and describe a suitable form of PLL.

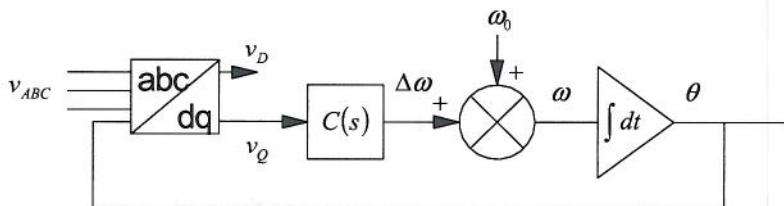
[3]

[Book work]

A PLL is needed because in this application the AC frequency is externally set by the grid but is not strictly constant. Thus the frequency, and more particularly the instantaneous phase angle, must be measured so that the DQ axis rotation matches the grid frequency.

[1 mark]

A PLL can be formed with an oscillator that is an integrator for converting frequency to angle (mod 2π) and a phase comparator that is a DQ transform block. When locked, the Q -axis voltage will be zero and any Q -axis voltage that appears is treated as the phase error as shown in the diagram below



[2 marks]

- (ii) Describe how the reference values of the D - and Q -axis currents should be formed in this application.

[4]

[Interpretation of notes]

In this application there is no call for reactive power and so the Q -axis current demand can be set to zero. It could be set otherwise if operation at power factors other than unity was required.

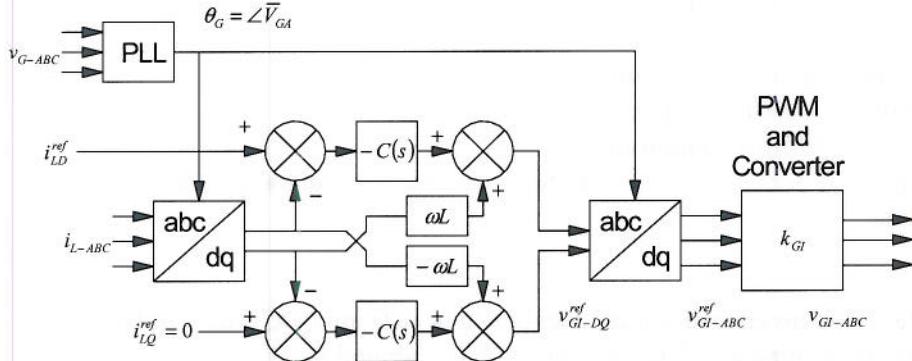
[1 mark]

The real power exported from the DC link is determined by the power supplied by the PV array minus any power losses. If the power balance on the DC link is set incorrectly then the DC link voltage will rise or fall and threaten correct operation. A convenient way to set the D -axis current demand is on the basis of the error between the measured DC-link value and a reference value. This ensures that sufficient real power is exported to hold the link voltage constant.

[3 marks]

- (iii) Sketch the format of the current control system including feed-forward terms for the inductive voltage drop. [3]

[Book work]



[3 marks]

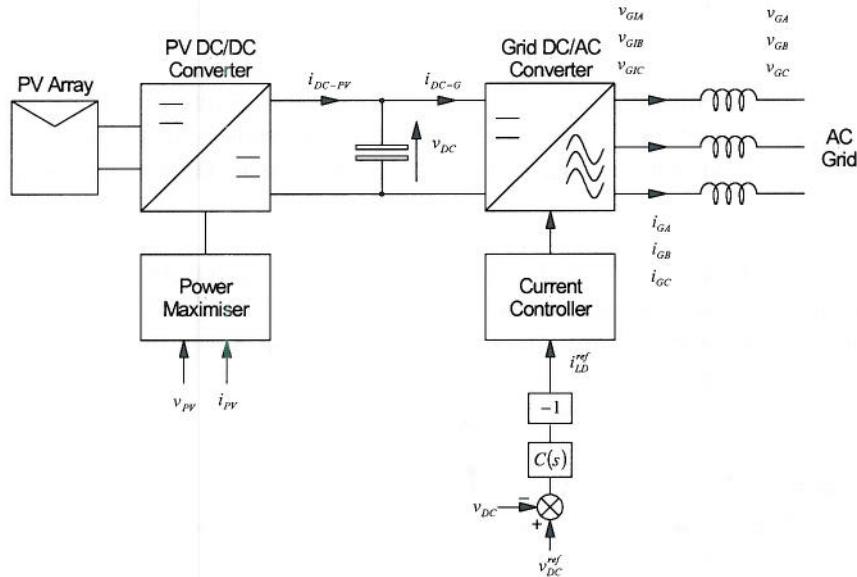


Figure 1.1, A Grid connected inverter acting as an interface for a PV Array

2.

- (a) Explain why multilevel converters are used for very high power converters. [4]

[Interpretation]

Very high power implies raising the system voltage (and keeping the current roughly similar) and system voltages well in excess of a typical junction breakdown voltage are needed. If “valves” of many transistors in series are used then all must be switched together to perform 2-level PWM and high switching losses result. If the transistors are used in multi-level format then only one (or two) are switched to make each level transition. With a high number of levels, “staircase” waveform close to a sine-wave can be synthesised in which each transistor only switches at line frequency and the switching losses are low.

[2 mark for staircase versus PWM; 2 marks for argument on switching loss]

- (b) Figure 2.1 shows an example of the modular multi-level converter (MMC).

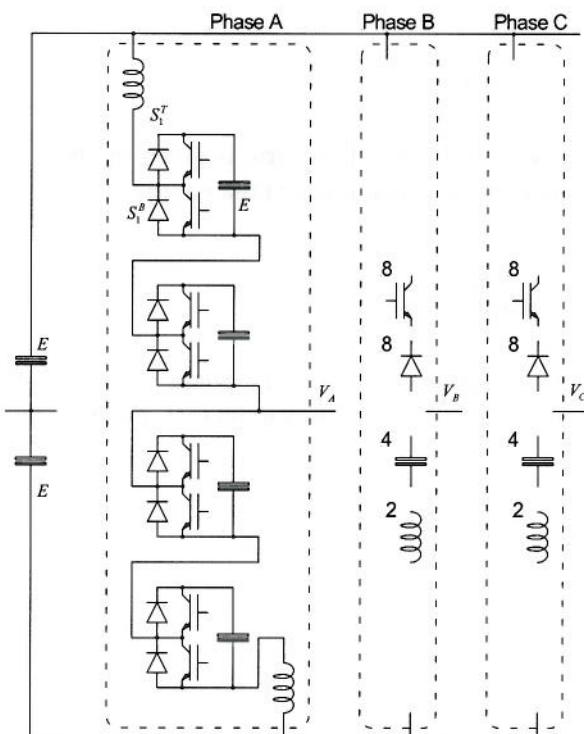


Figure 2.1, an example MMC

- (ii) Explain the operation of the MMC in terms of how the AC voltages are synthesized and the current paths that need to be established [5]

[Interpretation]

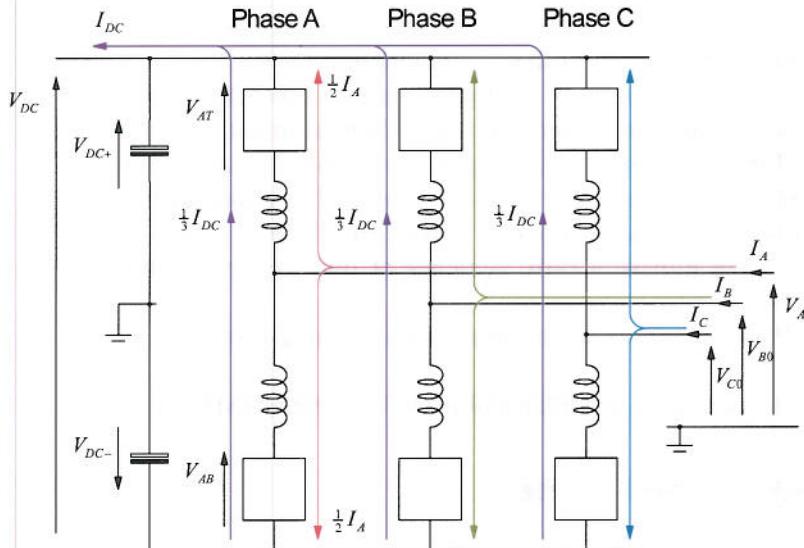
Cell voltages in each arm must be sufficient for the arm to support the full DC-link voltage. The two arms of each phase can then act like elements of a potential divider, the two arm voltages must sum to the DC-link voltage but the split can be varied so that the AC terminal can be placed at a number of levels between the DC-rails. Each

time one top cell switches on to inject its cell voltage, a bottom cell is switched off (to remove its) and the AC voltage moves down one step.

[3 marks]

Each AC phase current is split equally between the upper and lower arms. The DC current is split equally between each phase as shown in the diagram below.

[2 marks]



- (iii) Show that the energy exchange with the cells of one arm is given by the equation below and describe the condition that ensures the energy exchange is zero.

[7]

$$E_{Arm} = \frac{1}{3}V_{DC+}I_{DC}T - \frac{1}{2}V_{Ph}I_{Ph}T$$

[Book work]

The voltage required of the cell stack is the difference between the phase voltage and the DC bus voltage (if we ignore the small voltage over the arm inductor). For the top arm of phase A, the voltage is:

$$\begin{aligned} v_{AT} &= V_{DC+} - v_A \\ &= V_{DC+} - \hat{V} \cos(\omega t) \end{aligned}$$

The current through top arm of phase A is:

$$\begin{aligned} i_{AT} &= \frac{1}{3}I_{DC} + \frac{1}{2}i_A \\ &= \frac{1}{3}I_{DC} + \frac{1}{2}\hat{I} \cos(\omega t) \end{aligned}$$

The power exchanged with this arm is:

[4-49]

$$\begin{aligned}
 p_{AT} &= v_{AT} i_{AT} = (V_{DC+} - \hat{V} \cos(\omega t)) (\frac{1}{3} I_{DC} + \frac{1}{2} \hat{I} \cos(\omega t)) \\
 &= \frac{1}{3} V_{DC+} I_{DC} - \frac{1}{2} \hat{V} \cos(\omega t) \hat{I} \cos(\omega t) \\
 &\quad + \frac{1}{2} V_{DC+} \hat{I} \cos(\omega t) - \hat{V} \cos(\omega t) \frac{1}{3} I_{DC}
 \end{aligned}$$

The net energy exchange is found by integrating over the cycle (noting that sinusoidal terms integrate to zero but \cos^2 integrates to a non-zero result):

$$\begin{aligned}
 E_{AT} &= \int_{-\frac{1}{2}T}^{\frac{1}{2}T} p_{AT} dt \\
 &= \int_{-\frac{1}{2}T}^{\frac{1}{2}T} \left(\frac{1}{3} V_{DC+} I_{DC} - \frac{1}{2} \hat{V} \cos(\omega t) \hat{I} \cos(\omega t) \right) dt \\
 &= \frac{1}{3} V_{DC+} I_{DC} T - \frac{1}{2} \frac{1}{2} \hat{V} \hat{I} T \\
 &= \frac{1}{3} V_{DC+} I_{DC} T - \frac{1}{2} V_{Ph} I_{Ph} T
 \end{aligned}$$

[4 marks]

If we also assume that the positive and negative bus voltages are half the total DC-link voltage then we obtain.

$$E_{AT} = \frac{1}{3} \frac{1}{2} V_{DC} I_{DC} T - \frac{1}{2} V_{Ph} I_{Ph} T$$

Comparing this with the overall power balance for the converter, we can see that when the DC current is chosen as:

$$I_{DC} = 3 \frac{V_{Ph}}{V_{DC}} I_{Ph} \cos(\phi)$$

then the net energy exchange with the module stacks is zero.

[3 marks]

- (iv) Explain the advantages of the MMC over other topologies of multi-level converter.

[4]

[Book work]

The MMC is modular in the sense that the numbers principal components (transistors, diodes, and cell capacitors) all scale linearly with the number of levels chosen. For the diode-clamped design the number of diodes scales quadratically and for the flying capacitor design the number of capacitors scales quadratically. For these designs the complexity grows with number of levels and makes them impractically for a high number of levels. Further, transistors are associated with particular levels so building in redundancy is expensive. In the MMC, any cell can perform any duty and so a small number of additional cells can be added to provide useful redundancy. The chain cell converter shares the linear scaling and redundancy features of the MMC but can only provide reactive power in its simple form and providing real power flow adds great complexity.

The MMC has twice as many transistors (for a given number of levels) in comparison to the other topologies but the penalty in conduction power loss is less than a factor of two.

[2 marks for scaling discussion; 1 mark for redundancy; 1 mark for any other correct point]

3.

- a) Compare and contrast the three common power semiconductor switching devices: thyristors, IGBTs and MOSFETs. In your answer, discuss the different properties of each, their approximate ratings and the features of each device. [6]

[bookwork]

The main distinction between these devices is in the power level they are suited to and the effect that the design for a given power level has on functionality

[1]

At low power levels, it is possible to use minority carrier devices, ie MOSFETs. These are fast to switch, require almost no power to control and can be switched off and on at will. IGBTs are similar from an end user perspective, but switch slower as they are minority carrier devices (hence they are slow to turn off), but can still be turned on and off by a gate signal. The thyristor is the slowest of all the devices but is available up to much higher power ratings. The main problem with it is that the standard thyristor cannot be switched off (although there are variants such as the GTO that can be – again with the trade off that the changes needed to allow turn off reduce the on-state conduction capability).

[4]

The approximate ratings (for Silicon devices) are:

MOSFET - typically used up to 300 V and 100 A but can be obtained up to 1kV(at low current) and 1kA (at low voltage)

IGBT - typically used at up to a few kV and about 2 kA

Thyristor – up to around 12 kV and 5 kA.

(Award marks for sensible numbers here – they do not have to match exactly)

[1]

- b) Explain why it is not possible to make a single power semiconductor device block an arbitrarily large voltage or conduct an arbitrarily large current. [3]

[bookwork with some interpretation]

In order to make a device capable of conducting more current it must be increased in area, and to conduct more voltage it must be increased in length. As voltage blocking capability is increased, the cross sectional area must also increase to keep the power dissipation per unit area constant. Thus, a device capable of blocking an arbitrarily large voltage or conducting an arbitrarily large current must be of an arbitrary size. This means there are several issues:

- The finite defect rate in clean room processes means that as devices get larger, the device yield will reduce.
- The larger a device, the more problems will be encountered with uneven current flow, generation of hot spots, leading to differential thermal expansion and device failure.

[3]

- c) A thyristor valve, shown in figure 3.1, is subjected to high rates of change of voltage in V_{valve} . Explain why this valve may fail and describe a simple solution to prevent failure under such circumstances. [3]

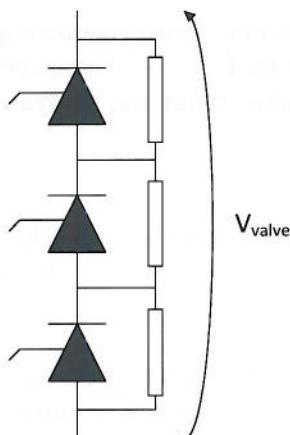


Figure 3.1 Series thyristor valve

[bookwork]

The leakage currents in the devices have some variation and so the voltage across blocking devices in steady state is forced by the resistors. However, these resistors do not allow voltages to share quickly – and thus not during a voltage transient. Voltages will not share equally when V_{valve} changes rapidly if there is a mismatch in device reverse recovery charge (which there will be...) and so we must place a capacitor sharing network in parallel with the resistors to ensure sharing occurs in the transient case.

- d) It is proposed that a diode valve capable of conducting 14 kA is made from 8 diodes capable of conducting 2 kA each. Due to non-identical thermal mounting of the devices, the temperature range expected in the devices under operation is expected to be between 320 and 340 K. The devices can be assumed to have a reverse saturation current of 1×10^{-11} A and obey the Shockley equation.
- i) Show that under worst-case conditions, the voltage across the diodes with no sharing network present is approximately 0.944 V and show that forced current sharing using resistors is not necessary. [2]

[calculation]

The devices each obey the equation:

$$I = I_s \exp\left(\frac{V_d}{kT/q}\right)$$

The worst case scenario is if all devices operate with the lowest current per given voltage (hottest) except one which operates with the largest current per volt

(coolest), as this forces the most current through the device with lowest slope resistance (coolest).

For T=320 K, the current through a device is:

$$I = 1 \times 10^{-11} \exp(V_d * 36.2319)$$

And for T=340 K the current through a device is:

$$I = 1 \times 10^{-11} \exp(V_d * 34.1006)$$

Thus, for 8 devices we have a worst case condition of 7 hot devices and 1 cold device:

$$I_{\text{total}} = 1 \times 10^{-11} \exp(V_d * 36.2319) + 7 * 1 \times 10^{-11} \exp(V_d * 34.1006) = 14000$$

This cannot be solved analytically but we can show that under these conditions the voltage is 0.944 V.

This gives a worst case current in the coolest device of 7.14 kA, which is well outside the operating envelope of the device, so a forced current share network is needed.

- ii) Hence, calculate the smallest value of resistors in the sharing network that enable all devices to operate within specification and comment on whether physical sharing resistors need to be added. [3]

[calculation]

The smallest resistor value under worst case occurs when the coolest diode is conducting exactly 2 kA. To do this, it requires a voltage of:

$$V_{dc} = 0.9088 \text{ V.}$$

The hottest diodes thus take equal current of $(14-2)/7=1.714 \text{ kA}$, which requires a voltage of $V_{dh}=0.9611$

Thus, we have:

$$V_{dh} + 2000 * R = V_{dc} + 1714 * R$$

Giving $R=0.18 \text{ m}\Omega$.

This is small enough that diode contact resistance and wiring resistance makes physical resistors unnecessary.

- e) Explain the relative merits of *normally-on* (*i.e.* on with zero gate-source voltage) versus *normally-off* (*i.e.* off with zero gate-source voltage) power semiconductor switches in the context of Silicon carbide MOSFETs and JFETs. [3]

[Interpretation]

Several companies are now producing power devices made from Silicon Carbide, such as SiC MOSFETs from Cree and Si JFETs from SemiSouth. The Cree MOSFETs are normally-off and SemiSouth produce both normally-on and normally-off versions of their JFETs. The normally off JFETs have slightly lower performance than the normally-on devices. SemiSouth believe that normally-off is favoured in a power device (pushing this as a feature). However, the advantage or disadvantage of normally-on or off aspect of a device depends on the failure mode of the gate drive. It is not necessarily more likely that a gate drive will fail with its output low instead of high and so a normally-off device is not guaranteed to be open circuit if the gate drive circuit fails.

[3]

Section B

4.

a)

- i) What is meant by ‘natural impedance’ or ‘surge impedance’ in AC Power transmission line?

[3]

[book work]

For high voltage transmission line, the shunt conductance (G) and series resistance (R) are negligible compared to series reactance and shunt susceptance. The characteristic impedance of a transmission line with loss neglected is purely real and is known as natural impedance. The expression for natural impedance is $Z_0 = \sqrt{\frac{L}{C}}$. This impedance in high voltage power line influences the impact of lightning and switching surges. Because of this, it is also known as surge impedances.

- ii) Explain the importance of the concept of the surge impedance loading of an AC power transmission.

[4]

[interpretation]

The power delivered by a transmission line when it is terminated by its surge impedance is known as surge impedance loading (SIL) and is expressed as:

$$SIL = \frac{V_0^2}{\sqrt{\frac{L}{C}}}$$

V_0 is normal rated voltage of the line. When receiving end power is equal to the SIL, the magnitude of the voltage along the entire length remains equal. The current is in phase with the voltage at any point. The amount of reactive power generated by the shunt capacitance per unit length is exactly absorbed by the line inductance per unit length of the line. When loading is more than SIL, the voltage drops along the line reaching lowest at the receiving end. Another way to look at this is the line capacitance produces less reactive power than the line inductance absorbs because of larger line current. This means the line needs more reactive power (capacitive). The other situation is when loading is less than SIL. The receiving end voltage rises above sending end voltage. This is a situation when more capacitive reactive power is generated than can be absorbed by the series inductance.

So receiving end loading as percentage of SIL is a good information to suggest how much compensation of what nature is needed to maintain a good voltage profile along the line.

- iii) A 230 kV double-circuit AC transmission line was built 30 years ago with twin conductors per-phase. To accommodate the growth in demand and generation in the system, the twin conductors are being replaced with quad conductors of similar individual geometry. What impact will this re-engineering have on the natural impedance of the line and consequently on the power transfer capacity?

[3]

[interpretation with some mental calculation]

The quad conductor arrangement will reduce the self inductance of the line resulting in lower surge impedance. The power transfer capacity will increase. The overall surge impedance loading (SIL) will increase by 40%.

- iv) Instead of opting for quad conductor arrangement, the utility also had an option to reinsulate the line to raise the transmission voltage to 345 kV level. What impact such option could have had on the power transfer capacity of the line? [3]

[interpretation with some mental calculation]

The re-insulation of the system to raise the voltage to 345 kV level will increase the per phase ground capacitance almost in the proportion of $345/230 = 1.5$ (approximately). This will reduce the surge impedance. The SIL will go up by $2.25 \times 1.25 = 3$ times. The power transfer capacity of the line will go up by 3 folds.

- b) A 100-mile long, 230 kV double-circuit line is designed to carry 300 MW. The receiving end of the line suffers from low voltage problem when the line is overloaded. It is decided to increase the transfer capacity of the line to 450 MW. Explain what would be the best choice of FACTS controller solve this problem. [4]

[interpretation]

The option is to go for is a shunt voltage support device such as SVC or STATCOM. Since the receiving end has voltage drop problem, an SVC in the middle is more cost effective and will address fast voltage instability problem. The STATCOM option is technically more effective and will offer faster dynamic voltage control but economically SVC is very attractive as STATCOM is expensive. The SVC will offer reasonably fast voltage support and lift the power transfer capacity of the line.

- c) What are the factors influencing the maximum thermal limit in AC power line? [3]

[interpretation with some element of practical understanding]

The reduction in mechanical strength of the conductor at high temperature caused by high loading is a consideration. The minimum statutory ground clearance (due to sag) is also important consideration. The seasonal variation of ambient temperature influences the conductor thermal limit significantly.

5

a)

- i) Describe what is meant by a '*loop flow*' in a power transmission system? [3]

[book work with some interpretation]

Loop flows are parallel power flows in a multi-line interconnected power systems, as a consequence of basic circuit laws which defines current flows by the impedance rather than the current capacity of the lines. They can result in overloaded lines with thermal and voltage level problems. They influence the steady state power flow limits.

- ii) How can '*loop flow*' be controlled? Explain your answer with a simple example of a meshed system. [5]

[book work with some examples, illustrations and interpretation]

Impedance compensation and or phase compensation are used to control the loop flow. To further understand the free flow of power, a very simple meshed system is considered in Fig A.5. The lines AB, BC, AC have continuous ratings of 1000 MW, 1250 MW and 2000 MW.

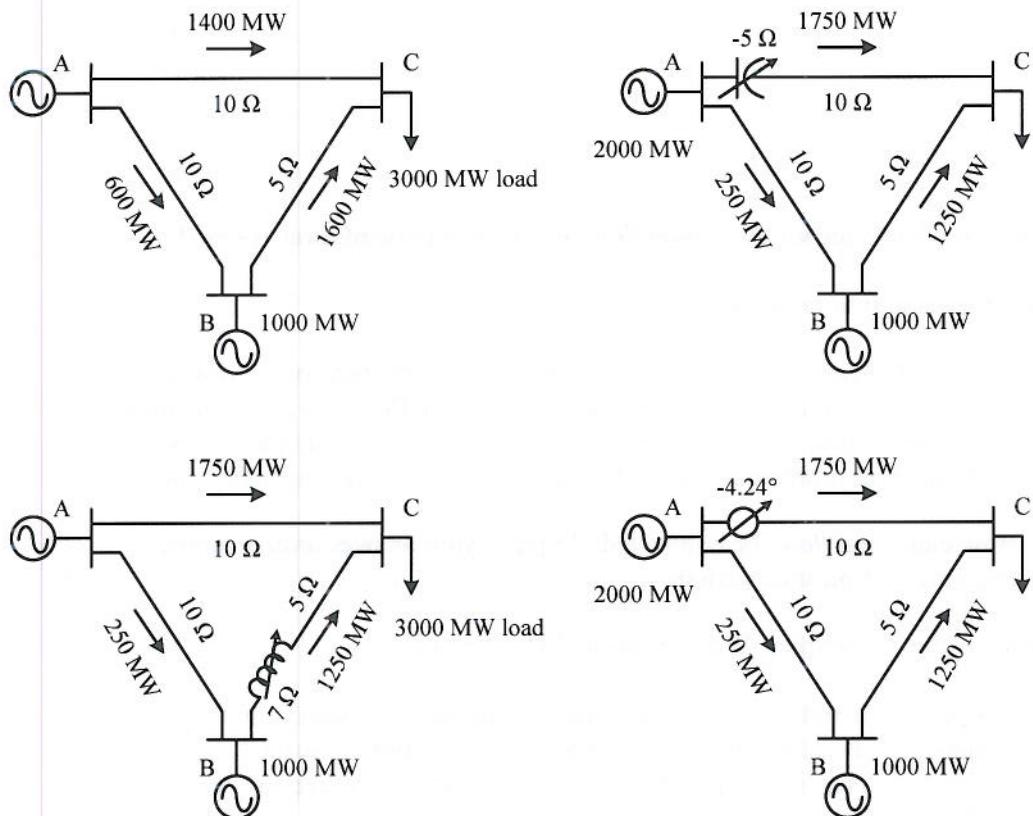


Figure A.5 Power flow in a mesh network: (a) system diagram; (b) system diagram with Thyristor-Controlled Series Capacitor in line AC; (c) system diagram with Thyristor-Controlled Series Reactor in line BC; (d) system diagram with Thyristor-Controlled Phase Angle Regulator in line AC : Understanding FACTS N G Hingorani and L Gyugyi , IEEE Press 2000

For the impedance shown in the diagram, three lines would be carrying 600, 1600, 1400 MW, respectively. Such situation overloads line BC (loaded to 1600 MW for its continuous rating of 1250 MW and therefore the generation would have to be decreased at B and increased at A, in order to meet the load without overloading line BC. Power, in short, flows in accordance with transmission line series impedance, dominantly inductive, that bear no direct relationship to transmission ownership, contracts, thermal limits, or transmission losses.

It will be interesting to see the impact of adding a $-5\ \Omega$ series capacitor in section AC. This would result in a new line flow pattern 250, 1250, 1750 in AB, BC and AC respectively. This means if this series capacitor is adjustable, other power flow pattern can also be realised so the total loss will be reduced. Addition of series inductor (reactor) in one of the lines would also provide the option of power flow control in the steady state. Thyristor controlled phase angle regulator can be inserted in one of the lines to serve the same purpose of realising various level of power flows.

- b) A long (greater than 200 mile) 345 kV AC transmission circuit, shown in Fig 5.1 transfers a power of 350 MW. A wind farm of 100 turbines with a capacity of 2 MW each is planned close to the sending end of the line. The transmission

operator is planning a controllable series compensator to help transfer the additional power from wind farm through existing line.

- i) Derive the power versus angle relationship (both real and reactive) of a transmission line which includes a capacitor in terms of the degree of compensation ($k_c = \frac{X_L}{X_C}$). [6]

[book work with derivation]

The series capacitor works by increasing the voltage across the transmission line that is a function of line current. This happens as part of the inductive voltage drop in the line is compensated by the capacitive drop. The conventional view is that the series capacitor cancels a portion of the series reactance and thereby reducing the effective transfer reactance. An interesting physical view is that in order to increase the current through the line, increased voltage has to be impressed across the physical line, this can be accomplished by adding series connected circuit element (passive or active) that would provide a voltage in phase opposition to the voltage prevalent across the series line reactance. A simple capacitor can be used to do this but a synchronous voltage source can also do the job in much controlled way.

The technology has matured from fixed capacitor (FC) to controllable one. In FC, fixed value of capacitance is connected in series with the line. The module is achieved through large number of units. The amount of series compensation is expressed as percentage of total line reactance. Typically it varies from 10-70 %. The percentage of compensation is defined as $k*100\%$, where k is degree of compensation. The effective transmission reactance is given by

$$X_{eff} = X_L - X_c ; k = \frac{X_c}{X_L}$$

' k ' is known as the degree of series compensation.

The power flow between two ends of a line as shown in the diagram of Fig 5.1 can be derived from the first principle. Complex power injected from sending end with a series capacitor (X_c)

$$S = P + jQ = V_s I_s^*$$

$$I_s = \frac{V_s e^{j\delta} - V_r e^{j0}}{j(X_L - X_c)}$$

[2]

Upon necessary workout and simplification the expression for power are given as:

$$P = \frac{V_s V_r}{(1 - k) X_L} \sin \delta \quad [2]$$

$$Q = \frac{V_s V_r}{(1 - k) X_L} \cos \delta - \frac{V_s^2}{(1 - k) X_L}$$

[2]

- ii) Determine the degree of compensation required to transfer the power from the wind farm (when it is producing at full capacity) while maintaining the steady-state power transfer margin at the same level as the uncompensated case. Assume 1.0 p.u. voltage at the sending and receiving ends. The line

impedance is 0.2 p.u and is purely reactive. The base power is 100 MVA. [6]

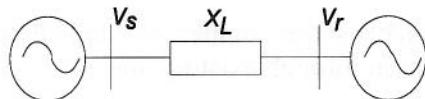


Fig 5.1: A simple interconnected power system model

[numerical problem with calculation]

Uncompensated case:

$$\begin{aligned} P &= \frac{V_s V_r}{X_L} \sin\delta \\ 3.5 &= \frac{1.0 \times 1.0}{0.2} \sin\delta \\ \delta &= 45 \text{ deg} \end{aligned}$$

With compensation:

The degree of compensation (k) can be computed from

$$P = \frac{V_s V_r}{X_L(1 - k)} \sin\delta$$

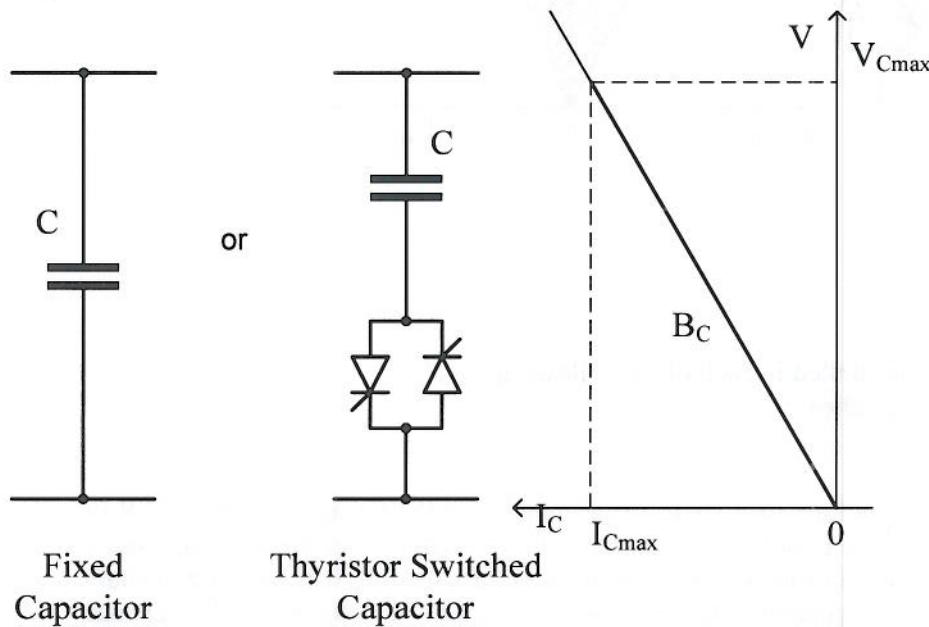
With $P = 5.5$, and keep stability limit to 45 degree, with both end voltages at 1.0 p.u, the required k will be 0.366. The range of compensation required will be 0 to 40%.

6.

- a) Briefly describe the function of a static VAr compensator (SVC) with the help of a sketch of circuit and the V - I characteristic. [7]

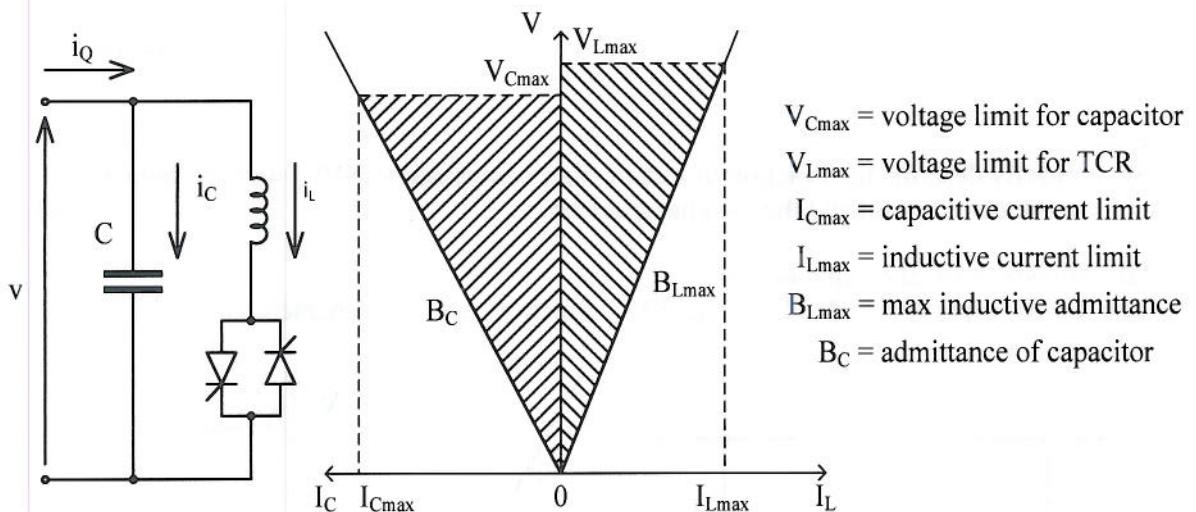
[Bit of book work and explanation]

The Fixed capacitor and TCR type SVC function and V-I characteristics are as follows:



Based on the choice of capacitor, two standard topologies for var source can be realized: One comprises of fixed capacitor and thyristor control reactor (FC+TCR). The other one is thyristor switched capacitor and thyristor control reactor (TSC+TCR) type.

Fig next shows arrangement for FC+TCR with its associated V-I area. It can be seen that the var generator can be made to work anywhere in the hatched area through proper control within the limits of voltages and currents.



- b) How is SVC modelled in each of the following:
i) power flow studies

[4]

[book work]

A commonly used topology of a static var compensator (SVC), is either FC+TCR or TSC+TCR comprises a parallel combination of a thyristor controlled reactor and a fixed or switched capacitor as we have learnt in the last section. It is basically a shunt connected static var generator/absorber whose output is adjusted to exchange capacitive or inductive current so as to maintain or control specific parameters of the electrical power system, typically bus voltage. The reactive power injection of a SVC connected to bus k is given by

$$Q_k = V_k^2 B_{svc}$$

$B_{svc} = B_C - B_L$; the symbols B_C and B_L are the respective susceptances of the fixed capacitor and the thyristor controlled reactor. It is also important to note that SVC does not exchange real power with the system.

- ii) small-signal stability studies

[5]

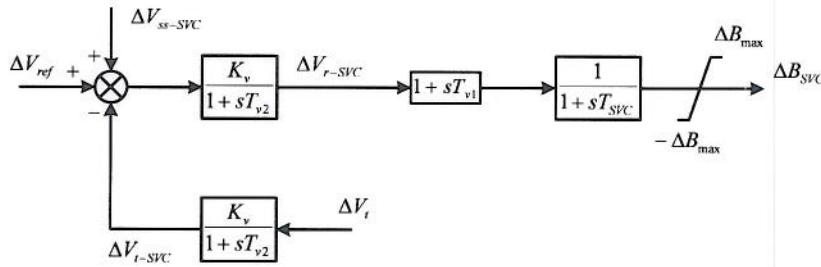
[book work]

The small-signal dynamic model of an SVC is given in Figure below. ΔB_{svc} is defined as $\Delta B_C - \Delta B_L$. The differential equations from this block diagram can easily be derived as

$$\begin{aligned} \frac{d}{dt} \Delta B_{svc} &= \frac{1}{T_{svc}} \left[-\Delta B_{svc} + \left(1 - \frac{T_{v1}}{T_{v2}}\right) \Delta V_{r-svc} - \frac{K_v T_{v1}}{T_{v2}} \Delta V_{t-svc} \right] \\ &\quad + \frac{K_v T_{v1}}{T_{v2} T_{svc}} [\Delta V_{ss-svc} + \Delta V_{ref}] \\ \frac{d}{dt} \Delta V_{r-svc} &= \frac{1}{T_{v2}} \left[-\Delta V_{r-svc} - K_v \Delta V_{t-svc} + K_v V_{ref} + K_v V_{ss-svc} \right] \end{aligned}$$

[4-49]

$$\frac{d}{dt} \Delta V_{t-SVC} = \frac{1}{T_m} [\Delta V_t - \Delta V_{t-SVC}]$$



SVC Dynamic Model

- c) A steel plant has a large induction furnace to melt raw materials used to produce steel. The power demand of the induction furnace behaves as a fluctuating load leading to fast voltage variation at the supply substation. This affects other loads connected to the substation. The plant also has several important loads that cannot tolerate transient voltage dips. Describe how a suitable FACTS controller would be chosen to solve this problem.

[4]

[Interpretation]

The option here has to be between SVC and STATCOM. The SVC is a cheaper option, but STATCOM can support voltage and reactive power requirement of the plant during network voltage drop. Besides the furnace loads, the plant will have various other voltage sensitive load such as variable speed drive motor. The low voltage leads to their shutting down thus affecting the plant productivity. SVC at low voltage situation acts as capacitor and as such cannot support the voltage as much STATCOM will do. The speed of response of STACOM is about 5-10 times faster than that of SVC, which is very important for the sensitive loads to stay on during depressed voltage situation. Thus STATCOM will be able to offer better power quality at the substation.

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