Paper Number(s): **E2.1**
ISE2.2

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2001

EEE/ISE PART II: M.Eng., B.Eng. and ACGI

DIGITAL ELECTRONICS II

Monday, 11 June 2:00 pm

There are FIVE questions on this paper.

Answer THREE questions.

Time allowed: 2:00 hours

Examiners: Brookes,D.M. and Clarke,T.J.W.

Notation: *Unless explicitly indicated otherwise, digital circuits throughout this paper are drawn with their inputs on the left and their outputs on the right. The notation X2:0 denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0. Signals labelled with identical names are connected together. Logical negation is indicated by an exclamation mark: i.e.* !X *denotes the logical inversion of* X.

1. *Figure 1* shows the state diagram of a synchronous state machine having two inputs, X and Y and one output, Z. Transitions from a state to itself have been omitted. The symbol "?" denotes "don't care".

   (a) Construct the state table for the state machine including both the next state and the value of the output, Z. [4]

   (b) Complete the timing diagram of *Figure 2* by showing the sequence of states that the state machine follows and the waveform of the output signal. [5]

   (c) Explain what is meant by saying that two states are "equivalent". [3]

   (d) Showing your reasoning clearly, determine which states are equivalent and hence show that it is possible to reduce the number of states to four by merging equivalent states. [4]

   (e) Draw a state diagram for the reduced state machine. [4]

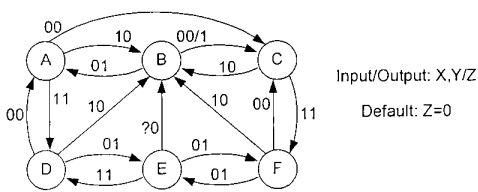


Figure 1

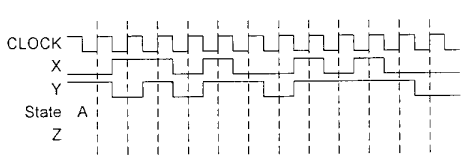


Figure 2

2. *Figure 3* shows a circuit containing four flipflops and two exclusive-or gates. The circuit has two independent clock signals, C and D, which may have different frequencies. The input signal, U, consists of pulses that last exactly one cycle of C and whose transitions occur slightly after the rising edge of C.

   (a) Complete the timing diagram, showing the waveforms of V, W, X, Y and Z. [6]

   (b) If the clock signals C and D have periods c and d respectively and an arbitrary phase relationship, determine the maximum and minimum time delay between the rising edge of U and the rising edge of the corresponding output pulse at Z. You may neglect propagation delays and setup times. [5]

   (c) Determine, as a function of c and d, the minimum interval between successive rising edges of U that will ensure that each input pulse results in a distinct output pulse at Z. [5]

   (d) Giving your reasons fully, say which of the signals V, W, X, Y and Z are likely to contain glitches and explain the circumstances under which they may occur. [4]

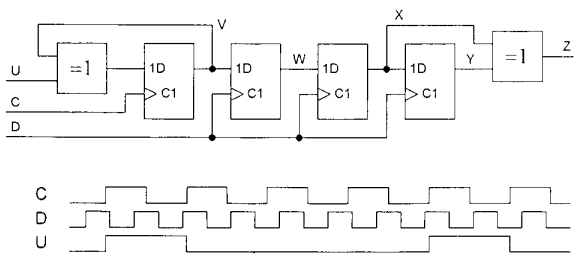


Figure 3

3. *Figure 4* shows the circuit of a transmission gate consisting of two enhancement transistors and two logic gates. The figure also shows an abbreviated symbol used to represent the circuit.

The n-channel and p-channel transistor characteristics in the triode region are given by:

$$I_{D_1} = K\left(2V_{DS}\left(V_{G_1S} - V_{T_1}\right) - V_{DS}^2\right) \quad \text{and} \quad I_{D_2} = -K\left(2V_{DS}\left(V_{G_2S} - V_{T_2}\right) - V_{DS}^2\right)$$

For both transistors, the source is connected to OUT and the drain to IN. The logic gate output voltages are 0 and 5 volts and the signals IN and OUT lie in the range 0 to 5 volts.

(a) Derive a simplified expression for the overall conductance of the transmission gate when both transistors are in the triode region of operation. [6]

(b) *Figure 5* shows a circuit constructed from four transmission gates and an inverter. Derive Boolean expressions for the outputs, X and Y, and describe the function of the circuit. [4]

(c) Design a circuit using only NAND gates and inverters that performs the same function as the circuit of *Figure 5*. [5]

(d) Estimate the number of transistors required for the transmission gate implementation and for the NAND gate implementation of the circuit. You may assume that the control signal buffers within the transmission gates are shared wherever possible. [5]

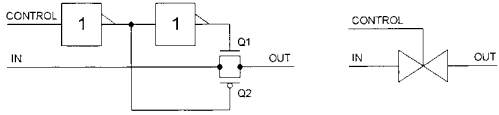


Figure 4

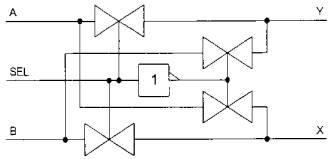


Figure 5

4. (a) Show that adding 1 onto an unsigned binary number can be performed by inverting each bit for which all the lower significance bits are 1. [4]

(b) *Figure 6* shows an n-bit incrementing block that adds 1 to the input number x whenever INC0 is high. It contains XOR gates, 2-input AND gates and a single $(n+1)$-bit AND gate.

If the propagation delay of all gates is 1 unit, determine the delay to each of the changing outputs when INC0 changes from 0 to 1 for each of the following circumstances:

(i) $Xi = 0$ for all i

(ii) $Xi = 1$ for all i [5]

(ii) $Xi = 1$ for $i<(n-1)$ and $X(n-1) = 0$

(c) *Figure 7* shows a 16-bit incrementer formed by cascading four of the incrementing blocks of *Figure 6* of sizes 5, 4, 4 and 3-bits respectively. The INCn output of each stage is connected to the INC0 input of the next higher stage. Determine the worst-case delay from X0 to each of Y4, Y8, Y12 and Y15 and specify the circumstances in which each worst case arises. [5]

(d) Determine the maximum size of incrementer that can be formed by cascading the incrementing blocks of *Figure 6* such that the worst-case delay from X0 to any Yi does not exceed 5 units. State the number of blocks required and the size of each block. [6]

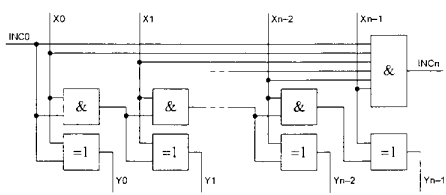


Figure 6

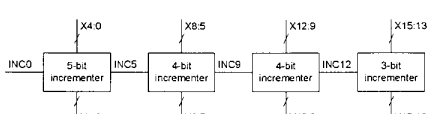


Figure 7

5. (a) *Figure 8* shows an R-2R ladder network that forms part of a 12-bit Digital-to-Analog converter. Show that, providing certain conditions are met, $I_k = 2^{k-12} I_T$. State the conditions needed for this to be true and give an expression for I_B. [4]

(b) In *Figure 9*, the ladder is used to form a Digital-to-Analog converter. The value of R is 10kΩ and a voltage V_{IN} of 2.048 V is applied to the input of the ladder. The current mirror reverses the direction of I_P. You may assume that the voltage V_M is zero.

The switches are controlled by a 12-bit unsigned binary number x which lies in the range 0 to 4095. The ladder output current I_k is sent to I_P or I_Q according to whether the k^{th} bit of x is 1 or 0 respectively. Determine expressions for I_P and I_Q and hence for V_{out} in terms of the number x. [6]

(c) If the 2R resistor that carries I_{11} is 0.1% too large, determine the resultant error in V_{out} when x is equal to (i) 0, (ii) 2048, (iii) 4095. [6]

Determine the % accuracy required of this resistor to ensure that the maximum error in V_{out} does not exceed ½ LSB.

(d) Explain why, in some applications, it is necessary to follow a Digital-to-Analog converter with a Sample/Hold circuit. [4]

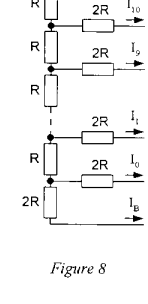


Figure 8

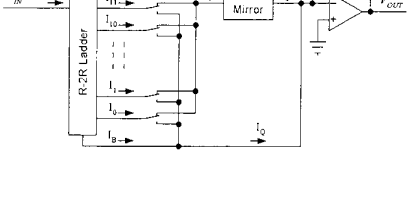


Figure 9

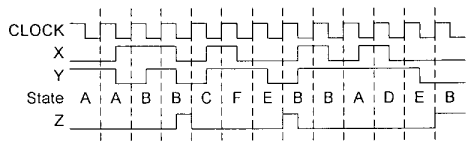
2000 E2.1/ISE2.2 Solutions

1. (a) From the specification in the question we get the following state table (default Z=0):

State/Z	X,Y			
	00	01	10	11
A	C	A	B	D
B	C/1	A	B	B
C	C	C	B	F
D	A	E	B	D
E	B	F	B	D
F	C	E	B	F

[4]

(b)



[5]

(c) Two states, A and B, are equivalent if, regardless of the input signal sequence, it makes no difference to the output waveform whether the state machine's initial state is A or B. [3]

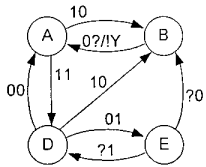
(d) (i) 0-equivalent states must have the same output under all circumstances. We therefore have two subsets: A=C=D=E=F and B. B cannot be equivalent to any other state since it has a different output when XY=01.

(ii) 1-equivalent states must be 0-equivalent and have 0-equivalent next states. Since all states are 0-equivalent except for B, we need to check for branches to B that occur in some states but not others. The only time this happens is in state E when XY=00. Therefore our 1-equivalent subsets are: A=C=D=F, E and B.

(iii) 2-equivalent states must be 1-equivalent and have 1-equivalent next states. We note that A and D are not 2-equivalent since they branch to A and E respectively when XY=01. For the same reason A and F are not 2-equivalent. Thus we get: A=C, D=F, E and B.

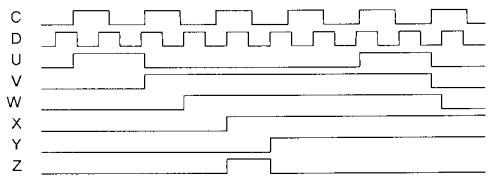
(iv) 3-equivalent states must be 2-equivalent and have 2-equivalent next states. We get exactly the same subsets as before and these subsets are therefore equivalent. [4]

(c) We can draw the reduced state diagram (labelling AC and DF as A and D respectively):



[4]

2. (a)



[6]

(b) The sequence of events and their times is: $U\uparrow=0$, $V\uparrow=c$, $W\uparrow=c\leftrightarrow c+d$, $Z\uparrow=c+d\leftrightarrow c+2d$. [5]

(c) We require the time delay between successive rising edges of Z to be at least $2d$. If the time delay between successive rising edges of U is x, then we require the shortest delay from the second rising edge to be at least $2d$ greater than the longest delay from the first rising edge. Algebraically, this gives:

$$x + c + d > c + 4d \quad \Rightarrow \quad x > 3d$$ [5]

It is also necessary that x is a multiple of c and at least $2c$.

(d) W is likely to contain glitches if the clock frequencies are not in an exact ratio. They will occur if a rising edge of C causes V to change within the setup/hold window of the flipflop that generates W. [4]

Z is likely to contain glitches if W changes on successive cycles.

3. (a) The total current is given by

$$I_{D_1} + I_{D_2} = 2KV_{DS}\left(\left(V_{G_1S} - V_{T_1} - \tfrac{1}{2}V_{DS}\right) - \left(V_{G_2S} - V_{T_2} - \tfrac{1}{2}V_{DS}\right)\right)$$

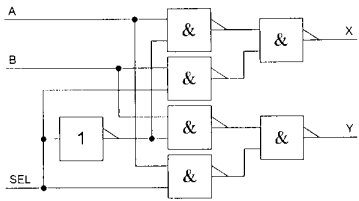
Hence the conductance is

$$\frac{I_{D_1} + I_{D_2}}{V_{DS}} = 2K\left(V_{G_1G_2} - V_{T_1} + V_{T_2}\right) = 2K\left(5 - V_{T_1} + V_{T_2}\right) \qquad [6]$$

(b) X = A·!SEL + B·SEL and Y = A·SEL + B·!SEL

The circuit acts as a changeover switch. If SEL = 0, it connects A to X and B to Y whereas if SEL = 1, the connections are reversed. [4]

(c)



[5]

(d) The transmission gate implementation requires 8 switch transistors and 4 transistors for the two inverters that form a non-inverting buffer. All the FET gate signals can be derived from these two inverters. Thus the total number of transistors is 12.

The NAND gate implementation requires 2 transistors for each gate input. This gives a total of 26 transistors. [5]

4. (a) If 1 is added onto the LSB of a number, the LSB will be inverted and a carry out will be generated from the LSB column iff the original LSB was equal to 1. This process will be repeated for successive higher order bits until we reach a bit position with a 0 in the original number. This bit will be inverted but will not generate a carry out into the next stage so all higher bits will be left unchanged. [4]

(b) (i) Only Y0 changes and the delay is 1 unit.

(ii) All outputs change. The delay to output Yi is i+1 units. The delay to INCn is 1 unit.

(iii) All outputs change except INCn. The delay to output Yi is i+1 units. [5]

(c) The delays involved in the path from Y0 to Y15 are:

Y0 to INC5	1 unit
INC5 to INC 9	1 unit
INC9 to INC12	1 unit
INC12 to Y15	3 units

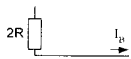
This gives a total delay of 6 units. This delay will arise iff X14:0 all equal 1.

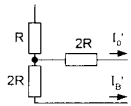
Following a similar argument, the worst case delay from Y0 to Y4 is 5 units (iff Y3:0=1), from Y0 to Y8 is 5 units (iff Y7:0 = 1) and from Y0 to Y12 is 6 units (iff Y11:0 = 1). [5]

(d) The maximum size of incrementer is 15 bits formed by cascading blocks of sizes 5, 4, 3, 2 and 1. [6]

5. (a) We assume that all the ladder outputs are held at a potential of 0 volts and use induction on the ladder order.

Suppose that for a ladder of order n we have $I_k = 2^{k-n} I_T$ and $I_B = 2^{-n} I_T$. We can form a ladder of order $n+1$ by re-labelling I_k as I_{k+1}' and by replacing the lowest 2R resistor by a network of 3 resistors:





Both networks have an impedance of 2R to ground and the substitution will therefore not affect any of the other currents. In addition we must have $I_o' = I_B' = \frac{1}{2} I_B$ since both 2R resistors have the same voltage across them. Thus we have $I_{k+1}' = I_k = 2^{(k+1)-(n+1)} I_T$ and $I_o' = I_B' = \frac{1}{2} I_B = 2^{-(n+1)} I_T$. [4]

(b) The entire ladder is equivalent to a resistor R to ground and so $I_T = V_{IN} / R = 204.8\,\mu A$. The current $I_P = xI_0 = 2^{-12} xI_T$ and $I_Q = I_T - I_P$.

The op-amp output is given by

$$\begin{aligned} V_{OUT} &= -5R(I_Q - I_P) = 5R(2I_P - I_T) \\ &= 5RI_T(2 \times 2^{-12} \times x - 1) \\ &= 5 \times 2^{-12} V_T (x - 2048) \\ &= 5(x - 2048)\,\text{mV} \end{aligned}$$ [6]

(c) If the resistor carrying I_{11} is 0.1% too large, then I_{11} will be reduced by 0.1%. For x<2048, this will cause IP to decrease and IQ to increase. Thus VOUT will change by $-2 \times 0.5\% \times V_{IN} = -20.48$ mV. For x ≥2048 V_{OUT} will change by +20.48 mV. Thus the answers are (i) –20.48 mV, (ii) –20.48 mV and (iii) +20.48 mV.

To restrict changes to ½LSB = 2.5 mV, the resistor accuracy must be [6]

$0.1\% \times 2.5 / 20.48 = 0.0122\%$.

(d) When several input bits change together, the switches will not switch exactly at the same time. This means that the current into the op-amp may contain a glitch which may be coupled to the output. In some applications, even a brief glitch is damaging: an example of this is the video DAC in a display. The glitch can be avoided by using a sample/hold circuit to disconnect the DAC output while it is changing. [4]