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E2.1

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2004

EEE/ISE PART II: MEng, BEng and ACGI

DIGITAL ELECTRONICS 2

Friday, 11 June 2:00 pm

Time allowed: 2:00 hours

There are FIVE questions on this paper.

Answer THREE questions.

All questions carry equal marks

Corrected Copy

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : D.M. Brookes

Second Marker(s) : T.J.W. Clarke

Notation:

> *Unless explicitly indicated otherwise, digital circuits throughout this paper are drawn with their inputs on the left and their outputs on the right. The notation X2:0 denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0. The numerical value of the number X2:0 is given by x.*

1. *Figure 1.1* shows the circuit for a successive approximation Analog-to-Digital converter having an input voltage V and a twos-complement signed 8-bit output $X7{:}0$ in the range -128 to $+127$. One LSB of the converter is equal to 0.2 V and input voltages in the range ±0.1 V are converted to the value 0.

   (a) If the input voltage V equals -10.45 V, determine the value of the output $X7{:}0$. [3]

   (b) Give the sequence of values taken at $X7{:}0$ during the process of converting an input voltage of -10.45 V and give the corresponding voltages at W. [11]

   (c) The aperture of the sampling switch is 50 ns and the propagation delays of the D/A converter and comparator are 100 ns and 60 ns respectively. Neglecting any propagation delays in the control logic, calculate the minimum time to convert an input voltage. You may assume that $X7{:}0$ is set to the correct initial value before the conversion process begins. [3]

   (d) If the comparator input current lies in the range ±2 μA, calculate the minimum value of C to ensure that the capacitor voltage changes by no more than ½ LSB during the conversion time found in part (c). [3]

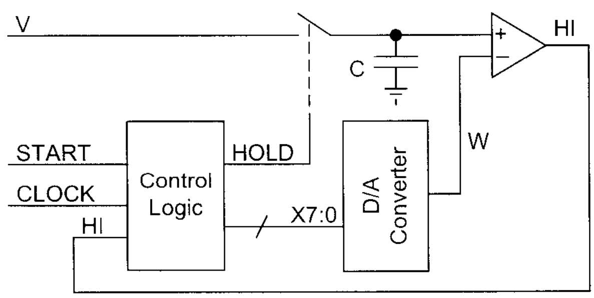

Figure 1.1

2. The state of a synchronous state machine is represented by a 3-bit number *Q2:0*. It has two inputs, *A* and *B*, and two outputs *X* and *Y*. The state table shown in *Table 2.1* gives the next sta are synchronized with the clock.

(a) Draw a state diagram for the state machine using the relative positions of the states shown in *Figure 2.1*. Your diagram should indicate the state transitions and the output signals. Transitions from a state to itself should be omitted. [8]

(b) If inputs *A* and *B* have the waveforms shown in *Figure 2.2*, determine the state sequence and the waveforms of *X* and *Y*. The clock rising edges are indicated by vertical lines and the state machine is initially in state 0. [6]

(c) Determine Boolean expressions for *D2*, *D1*, *D0*, *X* and *Y* that are as simple as possible. [6]

D2:0/X,Y		A,B 00	01	11	10
Q2:0	0	0	1		6
	1	0	1	3	
	2	0/1,0		7/1,0	6/1,0
	3		1	3	2
	4	0/0,1	1/0,1		6/0,1
	5	4	5	7	
	6	0		7	6
	7		5	7	6

Table 2.1

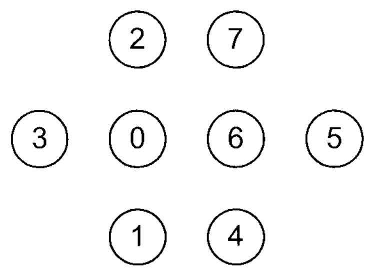

Figure 2.1

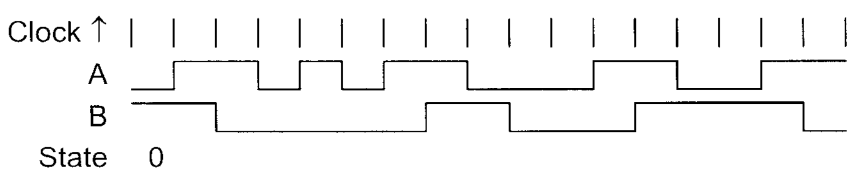

Figure 2.2

3. In a binary data transmission scheme, each transmitted bit occupies a bitcell having a duration of 1 μs. For a logical 0, the transmitted signal is low throughout the bitcell whereas for a logical 1, a short pulse is transmitted at the start of the bitcell. In order to prevent long intervals without any transmitted pulses, the transmitter inserts an additional bitcell containing a pulse whenever four consecutive zero bits have been transmitted. *Figure 3.1* illustrates the transmission of the bit sequence 11100000101 in which the inserted bitcell is marked with *. The frequency of CLOCK is 8 MHz.

(a) The output signal, *D*, of the transmitter is connected to the receiver circuit of *Figure 3.2* which consists of a 6-bit counter and four gates. On each rising edge of *CLOCK* the counter increments unless *D* is high in which case it resets to 0. All pulses on *D* last for exactly one *CLOCK* cycle with signal transitions occurring slightly after the *CLOCK* rising edge.

Draw a timing diagram showing the data sequence of *Figure 3.1* and the resultant waveforms of *D, V, W, X* and *Y*. On your diagram, show the decimal value of *Q5:0* during each output pulse on *X* or *Y*. Do not attempt to show the waveform of *CLOCK* on your diagram. [10]

(b) Modify the circuit so that output pulses are suppressed for the bitcell that immediately follows a sequence of four consecutive 0 bits. You may use any standard logic elements provided you fully specify their operation. [10]

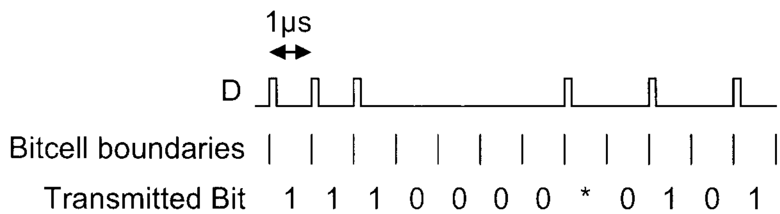

Figure 3.1

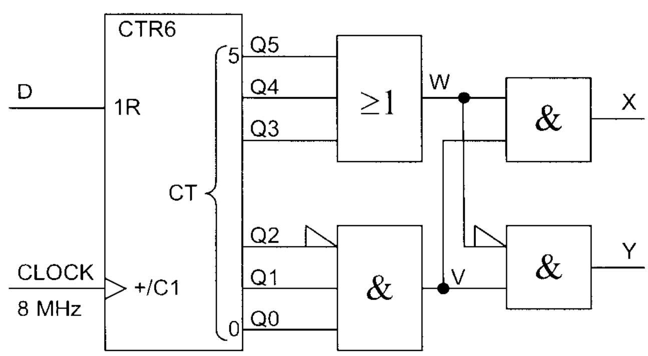

Figure 3.2

4. In this question, *P3:0*, *Q*, *R2:0*, *D3:0* and *Y7:0* all represent unsigned binary numbers whose numerical values are given respectively by *p*, *q*, *r*, *d* and *y*.

(a) The input to the "DIV" logic module shown in *Figure 4.1* is a number *p* in the range 0 to 9. The module outputs are the 1-bit quotient, *q*, and the 3-bit remainder, *r*, that result from dividing *p* by 5. Thus if $p = 7$, the circuit will give $q = 1$ and $r = 2$.

Determine a Boolean expression for *Q* and hence show how the whole module may be formed using a 3-bit adder and appropriate gates. [5]

(b) *Figure 4.2* shows a circuit that combines the "DIV" module of part (a) with a 4-bit register and an 8-bit shift register whose outputs shift in the direction *Y0*→*Y1*→...→*Y7*. If p_n and y_n represents the values of *p* and *y* after the n^{th} clock pulse, give algebraic expressions for p_{n+1} and y_{n+1} in terms of p_n and y_n for each of the four cases [6]

(i) $p_n < 5$ and $y_n < 128$

(ii) $p_n \geq 5$ and $y_n < 128$

(iii) $p_n < 5$ and $y_n \geq 128$

(iv) $p_n \geq 5$ and $y_n \geq 128$.

(c) If $p_0 = 0$ and $y_0 = 215_{10} = 11010111_2$, determine the values of p_n and y_n for $n = 1,\ldots,8$. [6]

(d) Given that $p_0 = 0$, explain the relationship of p_8 and y_8 to the number y_0. Determine the maximum possible value of y_8 and say what value of y_0 will result in it. [3]

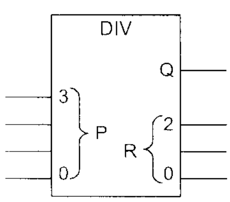

Figure 4.1

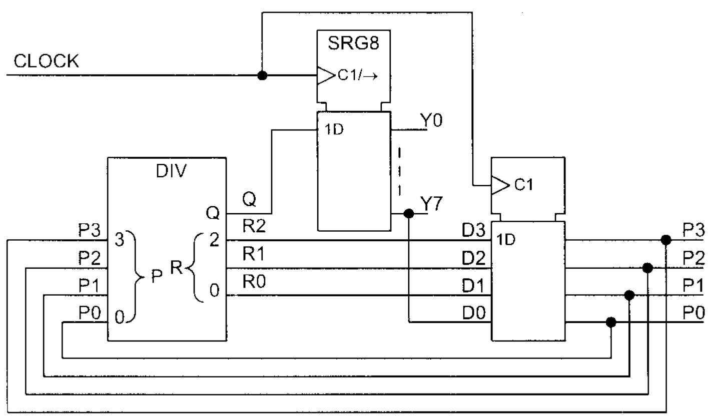

Figure 4.2

5. *Figure 5.1* shows two 1-bit full adder modules, labelled ΣE and ΣO, which can be cascaded to form an n-bit adder with the two modules used respectively for the even and odd numbered bit positions. Thus a ΣE module is used for bit 0, the least significant bit. The propagation delays, in gate delays, of the two modules are

ΣE	S	!CO
P,Q	3	1
CI	3	1

ΣO	S	CO
P,Q	5	2
!CI	4	1

(a) If n modules are cascaded to form an n-bit adder as described above, calculate for both even and odd n the worst-case delays from any input to (i) any S output and (ii) any CO or $!CO$ output. [5]

(b) In *Figure 5.2* the two n-bit adders have the same P and Q inputs but their CI inputs are fixed at 0 and 1 respectively. Using a multiplexer, the input signal CIN is used to select between the outputs of the adders.

(i) Show that the combined circuit acts as a single n-bit adder.

(ii) Design the circuitry for the part of the multiplexer that generates the $COUT$ output.

(iii) Using the propagation delays from part (a) above and assuming that n is even, calculate the four propagation delays for the circuit from each of CIN and P_0 to each of $COUT$ and S_{n-1}. [9]

(c) If we denote by An and Bn the n-bit adders of part (a) and of Figure 5.2 respectively, determine the worst-case propagation delay from any P input to the S_{63} output for each of the 64-bit adders using (i) a single $A64$ adder and (ii) an $A32$ adder followed by a $B32$ adder. [6]

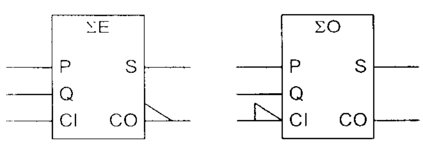

Figure 5.1

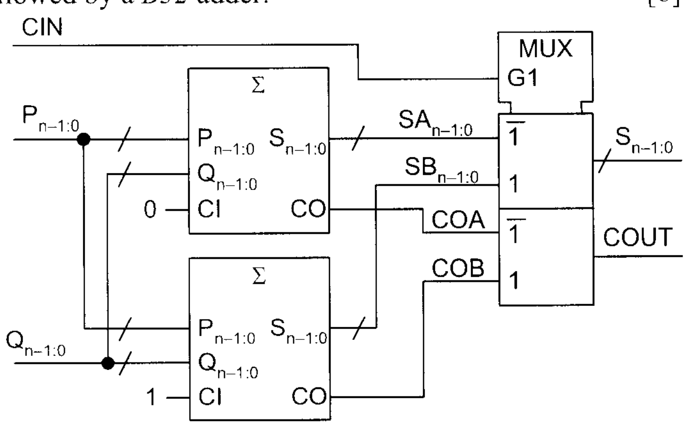

Figure 5.2

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[E2.1, ISE2.2]

1 (a) $x = \text{round}(V/0.2) = \text{round}(-52.25) = -52 = 11001100$ [3]

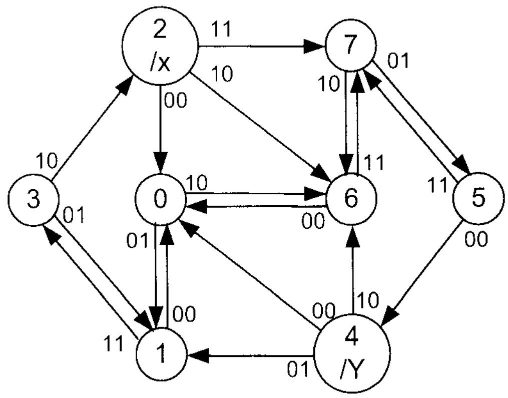
(b) The voltage W must be the lower threshold of the corresponding input interval and is therefore $w = 0.2x - 0.1$. The sequence is as follows: [11]

Clock	Step	X	X (binary)	W
0	128	0	0000 0000	-0.1
1	64	-64	1100 0000	-12.9
2	32	-32	1110 0000	-6.5
3	16	-48	1101 0000	-9.7
4	8	-56	1100 1000	-11.3
5	4	-52	1100 1100	-10.5
6	2	-50	1100 1110	-10.1
7	1	-51	1100 1101	-10.3
8	0.5	-52	1100 1100	-10.5

(c) If we assume that X7:0 is set to 0 before the conversion starts, then we don't have to wait for the 100 ns the first time around. The minimum conversion time is therefore $50 + 60 + 7 \times 160 = 1.23\ \mu s$. [3]

(d) $C = \dfrac{I \times \Delta t}{\Delta V} = \dfrac{2\ \mu A \times (1.23 - 0.05)\ \mu s}{0.1V} = 23.6\ pF$ [3]

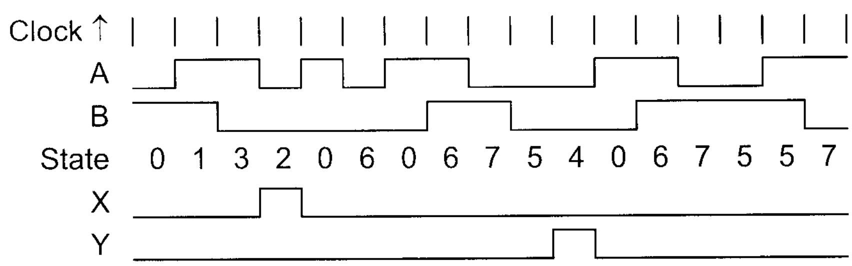
2. (a) The state diagram is:



Inputs: A,B

Default: X=Y=0 [8]

(b) The timing diagram is:



[6]

(c) These are all straightforward except for D2 for which we need a Karnaugh map and find the two groups of 8 shaded below:

D2		A,B				
		00	01	11	10	
Q2:0	0	0	0		1	← A·!Q0
	1	0	0	0		
	3		0	0	0	
	2	0		1	1	
	6	0		1	1	
	7		1	1	1	← Q2·Q0
	5	1	1	1		
	4	0	0		1	

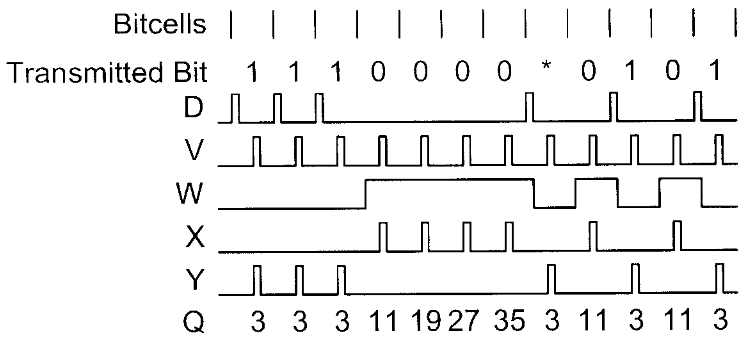
D2=Q2.Q0 + A.!Q0

D1=A
X=!Q2.Q1.!Q0

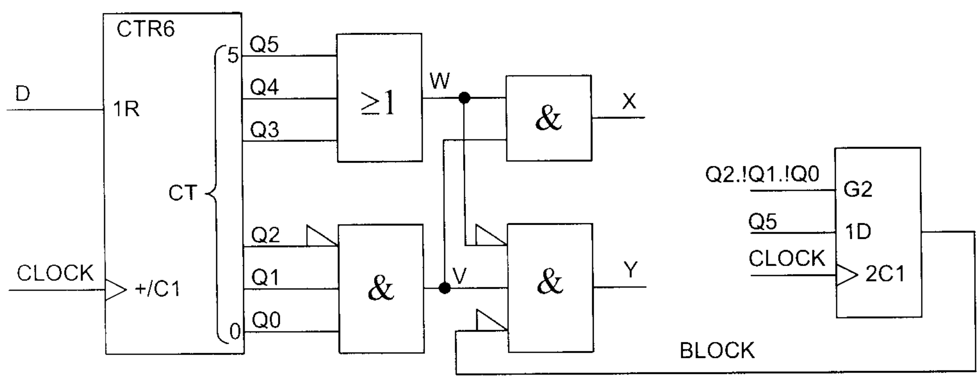
D0=B
Y=Q2.!Q1.!Q0

[6]

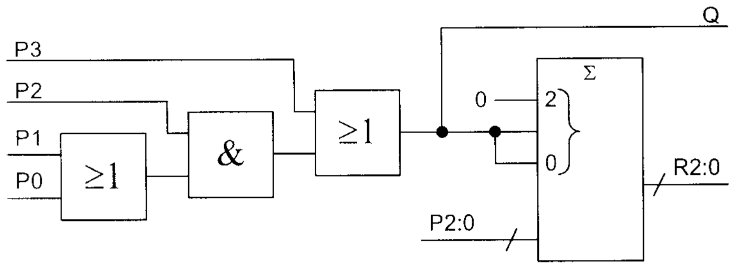
3. (a) Because of the AND-gate, pulses on X or Y can only occur when Q2:0 = 011_2 which means that that Q5:0=3+8k for some integer k. The falling edges of W occur when the counter resets to zero which is immediately at the end of the input pulses. Pulses on V occur midway between the input pulses. In the timing diagram below, Q is the value of Q5:0. [10]



(b) We need to remember that we have had four consecutive zeros and then suppress the next pulse. The easiest way to do this is to use a flipflop with a clock enable input to remember the value of Q5 at the last pulse: [10]



4. (a) Q=$(p \ge 5)$=P3 + P2.(P1+P0) and whenever Q=1, we need to subtract 5 (= add 3 modulo 8) from P to give R. hence:



[5]

(b) $y_{n+1} = 2y_n + q_n - 256(y_n \ge 128) = 2y_n + (p_n \ge 5) - 256(y_n \ge 128)$ and
$p_{n+1} = 2r_n + (y_n \ge 128) = 2p_n - 10(p_n \ge 5) + (y_n \ge 128)$

Hence we get:

(i) $p<5, y<128$ $\quad y_{n+1} = 2y_n$ and $p_{n+1} = 2p_n$

(ii) $p \ge 5, y<128$ $\quad y_{n+1} = 2y_n + 1$ and $p_{n+1} = 2p_n - 10$

(iii) $p<5, y \ge 128$ $\quad y_{n+1} = 2y_n - 256$ and $p_{n+1} = 2p_n + 1$

(iv) $p \ge 5, y \ge 128$ $\quad y_{n+1} = 2y_n - 255$ and $p_{n+1} = 2p_n - 9$ [6]

(c) Using the above expressions, we can generate the following table: [6]

clock	*y*	*y* (binary)	*p*	*q*	*r*	*d*
0	215	1101 0111	0	0	0	1
1	174	1010 1110	1	0	1	3
2	92	0101 1100	3	0	3	6
3	184	1011 1000	6	1	1	3
4	113	0111 0001	3	0	3	6
5	226	1110 0010	6	1	1	3
6	197	1100 0101	3	0	3	7
7	138	1000 1010	7	1	2	5
8	21	0001 0101	5	1	0	0

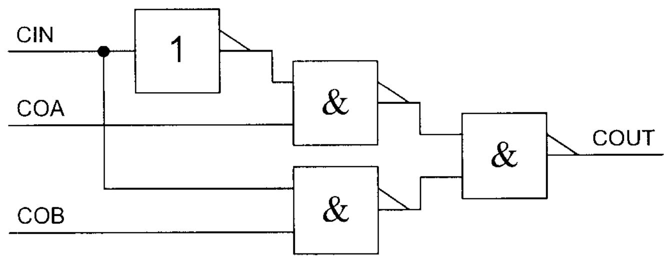
(d) The numbers y_8 and p_8 are the quotient and remainder after dividing y_0 by 10. The maximum possible value of y_0 is 255 which will result in $y_8 = 25$ and $p_8 = 5$. This is therefore the maximum value of y_8. [3]

5. (a) We get one delay from each stage except the last which has more: [5]

	S	CO/!CO
n even	n+3	n
n odd	n+2	n

(b) (i) If CIN=0 then the outputs come from the top adder which has CI=0. Similarly for CIN=1. [2]

(ii) This is a standard multiplexer: [3]



(iii) The multiplexer adds 2 onto the delays from P but reduces the delay from CIN to only 3 (independent of n). [4]

	S	COUT
CIN	3	3
P0	n+5	n+2

(c) (i) $P0 \to S63 = 67$ [2]

(ii) $\max(P0 \to C31 \to S63,\ P32 \to S63)$
$= \max(32+3,\ 32+5) = \max(35,37) = 37$ [4]