EE4-17
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IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2012

MSc and EEE PART IV: MEng and ACGI

Corrected Copy

HIGH PERFORMANCE ANALOGUE ELECTRONICS

Thursday, 17 May 10:00 am

Time allowed: 3:00 hours

There are FOUR questions on this paper.

Answer ALL questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : E. Rodriguez-Villegas
Second Marker(s) : P. Georgiou

The Questions

1.

(a) Explain briefly the main advantage of a direct conversion receiver with respect to a superheterodyne one.

[5]

(b) A receiver system can tolerate -60 dBμ of received noise power. The equivalent input noise of the receiver system, as quoted by the manufacturers, is -90 dBm. What is the noise figure of the receiver?

[5]

(c) The receiver architecture in Figure 1.1 receives the following RF signal:

$$RF=A\cos(At+\varnothing_A)+B\cos(Bt+\varnothing_B)$$

where the first term represents the signal of interest, and the second one the image. Derive an equation describing IFOut if the reciever is used with $\phi1=\phi2=90^{o}$. Is this the right way of designing the receiver?

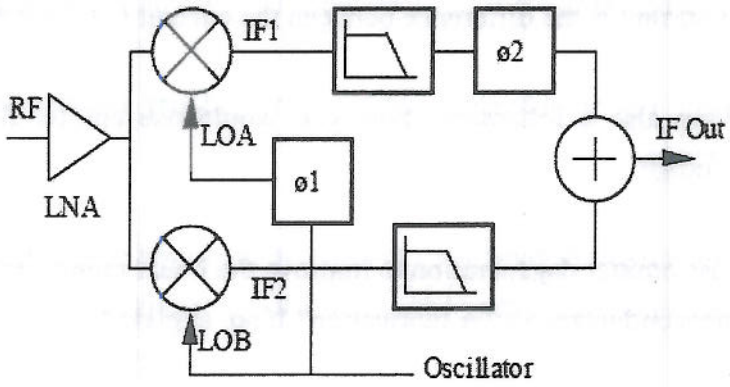

Figure 1.1.

[6]

(d) In a subsampling receiver, the received signal of interest is centred at 10 MHz and has a bandwidth of 250 kHz. Which one of the following frequencies would you choose for subsampling and why: 600 kHz or 100 kHz?

[4]

2. For the circuit in Figure 2.1, where A=20, and the transistors are operating in the active region:

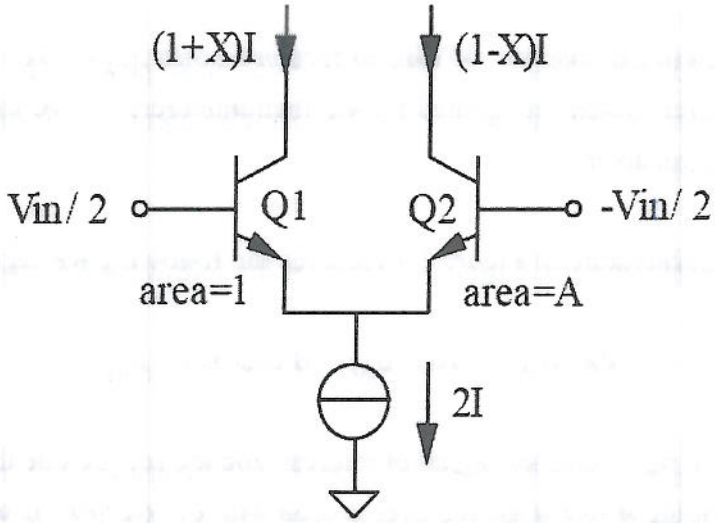

Figure 2.1

(a) At what value of the input voltage (V_{in}) does the maximum of the transconductance occur if the output current is the difference between the current in both branches?

[4]

(b) Explain, drawing also a schematic, how you would use emitter degeneration to improve the linear range.

[3]

(c) If you were to use emitter degeneration to improve the linear range, could you modify the value of the transconductance after fabrication? If so, explain how.

[3]

(d)Explain, drawing also a schematic, which other strategy you could use to increase the circuit linear range.

[4]

(e) What is the value of the transconductance in the circuit you proposed in (d)?

[3]

(f) How could you modify the value of the transconductance after fabrication for the circuit you proposed in (d)?

[3]

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3.

(a) Give one advantage of the LC-ladder approach for implementing continuous-time filters. Give one reason why passive LC-ladder filters are generally unsuitable for implementing fully-integrated on-chip filters.

[2]

(b) Figure 3.1 shows a doubly terminated LC-ladder filter. For this circuit:

i) Does it provide a high-pass, low-pass, band-pass or band-stop response? Explain your answer.

[2]

ii) If the voltage across component x is Vx and the current through it ix, write down the nodal equations for the filter. Hence show that the filter can be represented by the scaled signal flow graph of Figure 3.2.

[5]

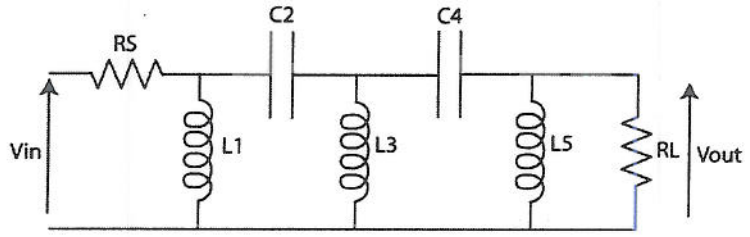

Figure 3.1.

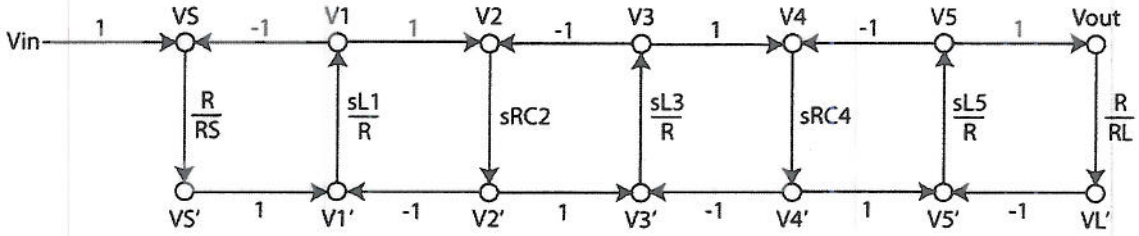

Figure 3.2.

(c) Briefly explain how inductors to be integrated on-chip can be implemented using active components.

[2]

(d) Figures 3.3 and 3.4 show circuits containing floating capacitors.

i) Why is it preferable to avoid the use of floating capacitors in high frequency integrated circuit applications?

[2]

ii) How could the circuit in Figure 3.3 be modified to eliminate the floating capacitor?

[2]

ii) Draw a signal flow graph to show how the circuit in Figure 3.4 can be modified to eliminate the floating capacitor.

[5]

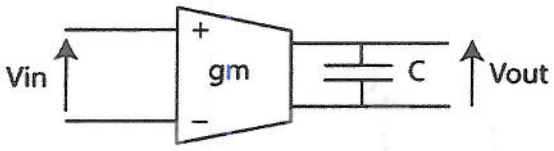

Figure 3.3.

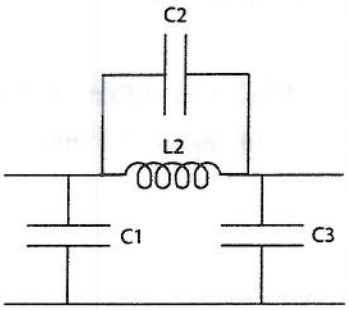

Figure 3.4.

4.

(a) For the circuit in Figure 4.1:

i) If *Iout* = *Ic1* – *Ic2*, *Vt* is the thermal voltage and *Va* is small show that

$$Iout = \frac{IqVa}{2Vt}$$

(*Hint:* $\tanh(x) = \frac{e^x - e^{-x}}{e^x + e^{-x}}$.)

[5]

ii) If the input referred noise density is 50 nV/√Hz what is the output referred current noise density?

[2]

iii) Draw a modified version of Figure 4.1 which can be used as a multiplier which has both inputs as voltages. Briefly explain how your circuit works.

[3]

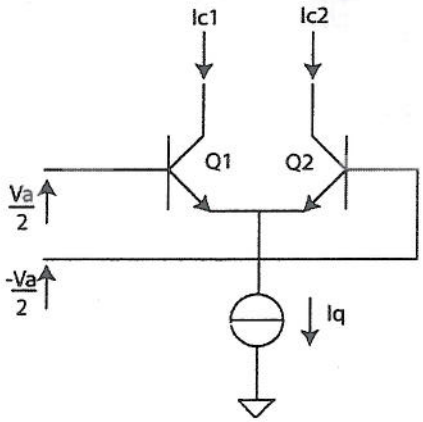

Figure 4.1.

(b) A multiplier is used to multiply two signals such that:

$Vout = V1 \times V2$, where $V1 = A1\sin(2\pi f_1 t)$ and $V2 = A2\sin(2\pi f_2 t)$.

The multiplier is followed by a first order filter with transfer function

$$H(jf) = \frac{1}{1 + \frac{jf}{f_c}}$$

where f_c is the filter cut-off frequency.

i) Draw an active filter topology that implements a first order $H(jf)$ transfer function.

[1]

ii) For a certain input the multiplier *Vout* has frequency components at 10 kHz and 5.01 MHz. The filter then attenuates the 5.01 MHz output component by 34 dB. What is the cut-off frequency of the filter? Give your answer to the nearest kHz. How much has the 10 kHz component been attenuated by?

[3]

iii) The multiplier alone has output referred noise which is white and of value 24 nV/√Hz. The filter alone has input referred noise which is white and of value 7 nV/√Hz. When the two are cascaded, what it is the equivalent noise density present at the input to the filter?

[1]

iv) What is the total noise voltage at the output of the filter? (*Hint: Use* $\frac{f}{f_c} = \tan\theta$ *and an appropriate trigonometric identity.*)

[5]

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1.

(a) (Theory)

In a direct conversion receiver, a single local oscillator is used whose frequency is equal to the RF carrier frequency, and thus the IF = 0 Hz. No bandpass filtering is required as the signal is converted directly to baseband. In addition, there is no image signal, thus no image filtering is needed. All signal filtering is at baseband frequencies, and therefore can be performed on-chip. This means that a single-chip receiver is feasible using direct conversion. In a superheterodyne receiver it is difficult to have good image rejection since in order to achieve this either a very high order filter is needed or the IF would need to be high. However, if the IF was high a very high (to the point of impractical) Q filter would be required for channel selection.

(b) (New computed example)

Noise factor= (Psys+Pni)/Pni(dB)

Noise figure is noise factor in dB.

In Watts Psys=10^{-12}, Pni=10^{-12}. (Psys+Pni)(dBm)=-87. NF=3dB

(c) (Application of theory)

Local oscillator :

LOA = 2 cos (Lt - ø1) LOB = 2 cos Lt

RF signal :

A cos (At + øA) + B cos(B t + øB)

where A = (L - IF) is the wanted signal, and B = (L + IF) is the image.

After mixing { Recall 2cosXcosY = cos(X-Y) + cos(X+Y) and cos(-X)=cos(X) }

o IF1 = 2A cos (At + øA) cos (Lt - ø1) + 2B cos (B t + øB) cos (Lt - ø1)

= A cos ((L- A)t - ø1 - øA) + A cos ((L+ A)t - ø1 + øA)

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+ B cos ((B- L)t + øB + ø1) + B cos ((B+ L)t + øB - ø1)

o IF2 = 2A cos (At + øA) cos Lt + 2B cos (Bt + øB) cos Lt

= A cos ((L - A)t - øA) + A cos ((L + A)t + øA)+ B cos ((B- L)t + øB) + B cos ((B+ L)t + øB)

Lowpass filter removes sum components:

o IF1 = A cos ((L- A)t - øA- ø1) + B cos ((B- L)t + øB + ø1)

= A cos (IFt - øA- ø1) + B cos (IFt + øB + ø1)

o IF2 = A cos ((L - A)t - øA) + B cos ((B- L)t + øB)

= A cos (IFt - øA) + B cos (IFt + øB)

After phase shift - ø2:

o IF1 = A cos (IFt - øA- ø1 - ø2) + B cos (IFt + øB + ø1 - ø2)

o IF2 = A cos (IFt - øA) + B cos (IFt + øB)

Adding signals IF1 and IF2 :

IFOut = 2Bcos (IFt-øB)

It is not the right way of designing the receiver because the information it keeps is the one of the image, not the one of the signal of interest. It should have been designed with ϕ_1=90^o and ϕ_2=-90^o

(d) (Application of theory)

600kHz. At 100kHz there would be aliasing, since the signal would repeat in the frequency spectrum every 100kHz, and the bandwidth is 250kHz:

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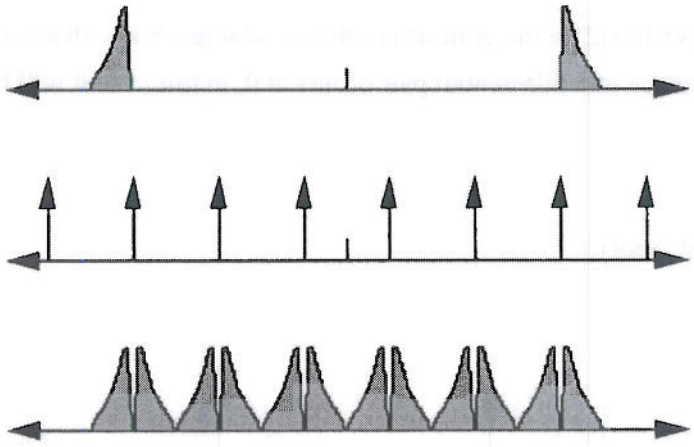
Subsampling Receivers

A bandpass signal centred on fo is sampled at a rate fo/m (i.e. well below the Nyquist rate). Provided that the sampling rate is slightly greater than twice the bandwidth of the RF signal, then aliasing will not occur.



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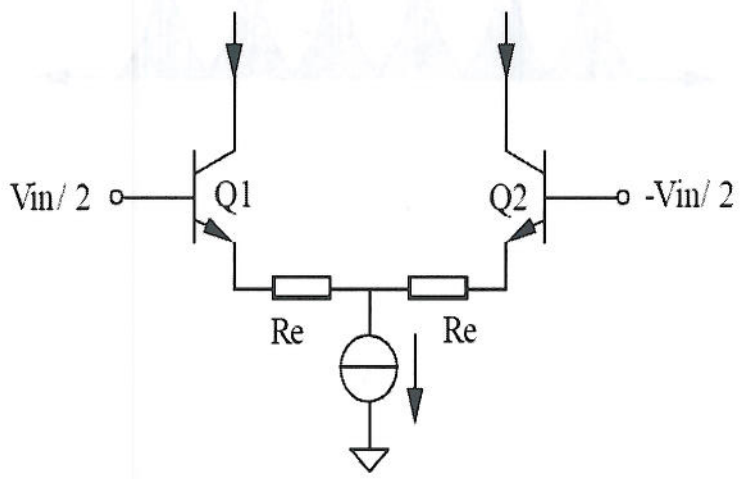
2.

(a) (Application of theory)

After analysing the circuit:

Iout=2Itanh(Vin/2Vt-lnA/2) ie the same as in a differential pair but with an offset. Since the maximum of the transconductance in a differential pair occurs at 0, in this case it will be at around 78mV.

(b) (Application of theory)



$$\begin{aligned} Vin &= Vbe1 + ReIc1 - Vbe2 - ReIc2 \\ &= Ic1(re1 + Re) - Ic2(re2 + Re) \end{aligned}$$

where the values of re1 and re2 depend on the instantaneous value of Vin. If Re >> re1, re2 then the non-linear variation of gm with Vin is swamped:

$$Vin = Ic1Re - Ic2Re = (Ic1 - Ic2)\,Re$$

if $Iout = (Ic1 - Ic2)$; $Iout/Vin = 1/Re$

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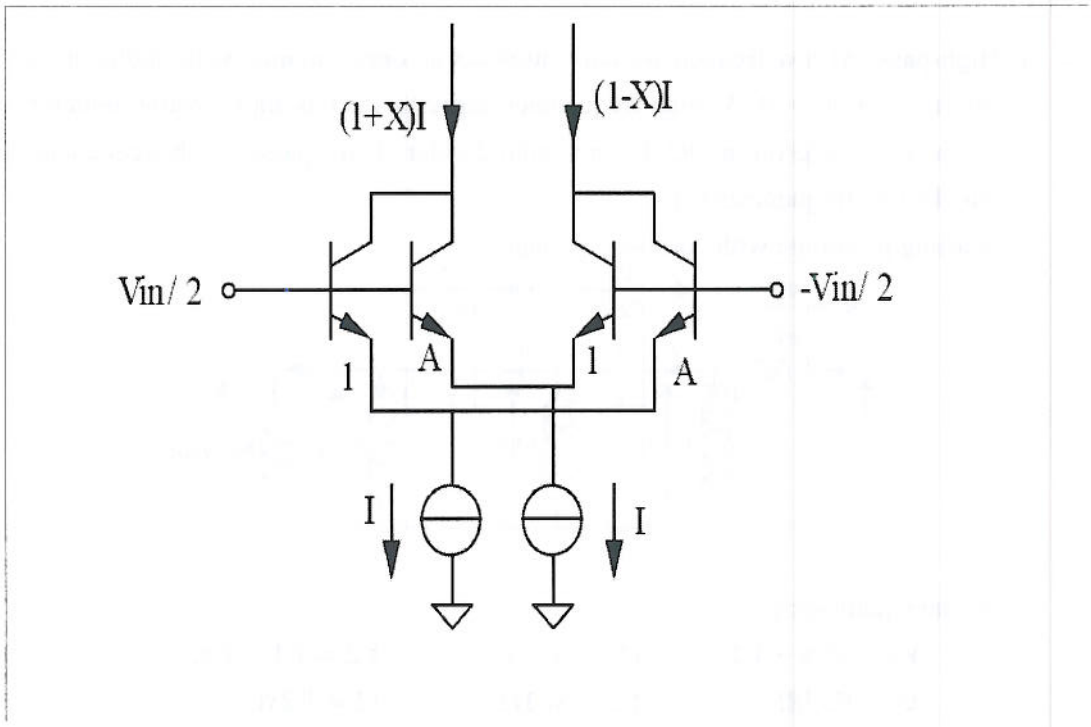
(c) (Application of theory)

If degeneration is implemented with passive resistors no.

(d) (Theory)

If several 'offset' differential pairs are connected in parallel, then the combined dynamic range will be extended. The area scaling must be carefully designed to ensure linearity of the combined response.



(e) (Application of theory)

After calculations, or by realising it is equivalent to the sum of the transconductance of two differential pairs with offset:

$I/Vt[\text{sech}^2(Vin/2Vt-\ln A/2)+\text{sech}^2(Vin/2Vt+\ln A/2)]$

(f) (Application of theory)

With the bias current

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3. Theory.

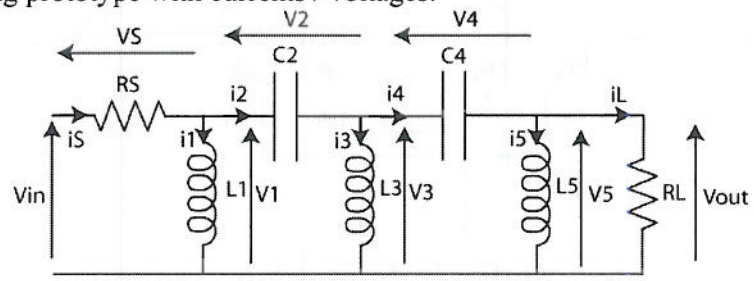
(a) Low sensitivity to component tolerances. OR. Insensitive to parasitic capacitances (grounded capacitors can be pre-distorted out to absorb stray capacitances to ground) [1].

Inductors are difficult to implement on chip (low value, low Q). OR. Capacitors are small in value. Both limit tuning capabilities [1].

(b) Application of theory.

i) High-pass. At low frequencies capacitors act as open circuits while inductors act as shorts, so Vout = 0. At high frequencies capacitors act as shorts while inductors are open, so Vout given by RS/RL potential divider. Thus, passes high frequencies and blocks low frequencies [2].

ii) Starting prototype with currents / voltages:



Nodal equations: [2]

$VS = Vin - V1;$ $\quad i1 = iS - i2;$ $\quad V2 = V1 - V3;$

$iS = VS/RS;$ $\quad V1 = sL1i1;$ $\quad i2 = V2sC2;$

$i3 = i2 - i4;$ $\quad V4 = V3 - V5;$ $\quad i5 = i4 - iL;$

$V3 = sL3i3;$ $\quad i4 = V4sC4;$ $\quad V5 = sL5i5;$

$Vout = V5;$

$iL = Vout/RL;$

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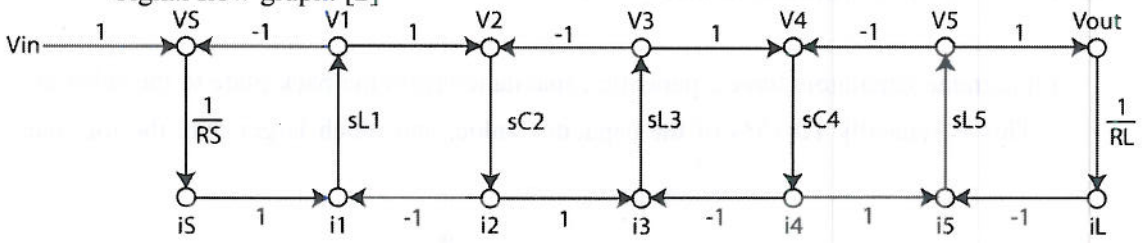
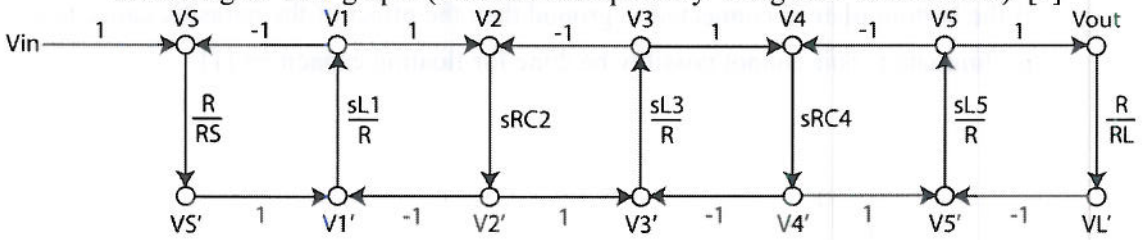
Signal flow graph: [2]



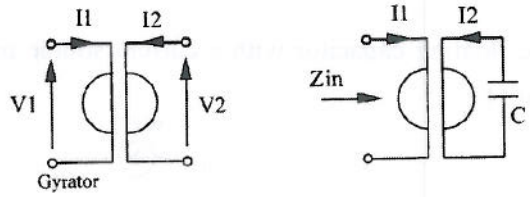
Scaled signal flow graph: (Currents multiplied by 'imagined' resistance R): [1]



(c) Theory.

Use a gyrator [1].

General case gyrator [1]:



$I1 = G\,V2 \qquad I2 = -G\,V1$

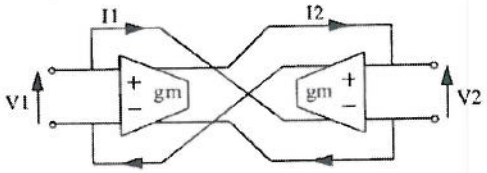
(G = 'gyration conductance')

To simulate an inductor, connect a capacitor across port 2:

$$V1 = -\frac{I2}{G} = \frac{C}{G}\frac{dV2}{dt} = \left(\frac{C}{G^2}\right)\frac{dI1}{dt} = L\frac{dI1}{dt}$$

Inductor value is tuneable by varying G.

OR. Specific circuit [1]: e.g.



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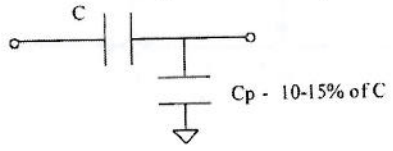
(d) Theory (i, ii). Application of theory (iii).

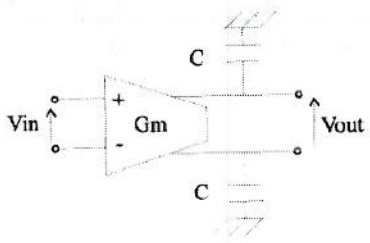
i) Integrated capacitors have a parasitic capacitance from the back plate to the substrate. This is typically 10-15% of the capacitor value, and much larger than the top plate



parasitic capacitance [1].

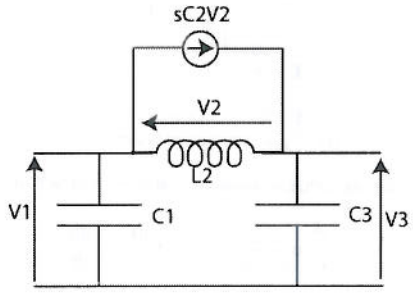
If the bottom plate is connected to ground then the effect of the parasitic capacitance is eliminated. This cannot possibly be done for floating capacitors [1].

ii)



. gm and C values must be correct. [2]

iii) Replace floating capacitor with a current source providing the same current as the capacitor [1]:



Split current source in two such that the KCL equations at nodes 1 and 3 are maintained [1]:

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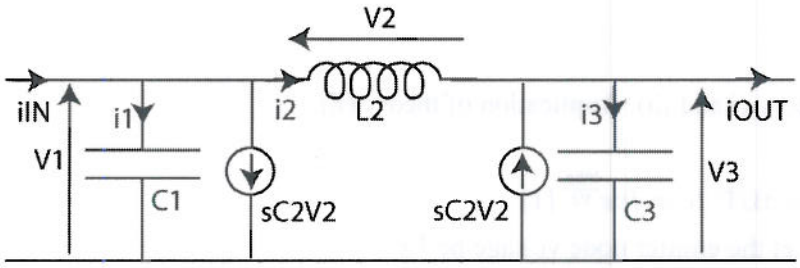
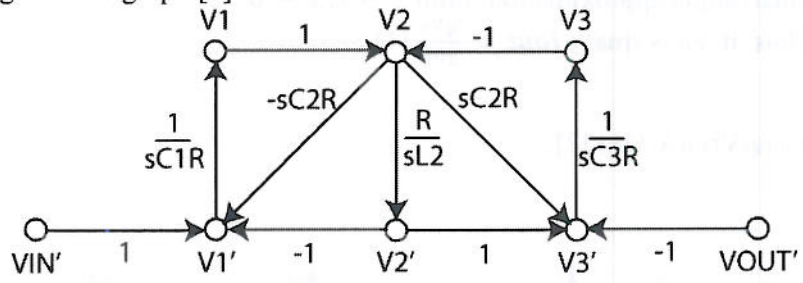


Nodal equations [1]:

$$i1 = iIN - i2 - sC2V2; \qquad V2 = V1 - V3;$$
$$V1 = i1/sC1; \qquad i2 = V2/sL2;$$

$$i3 = i2 + sC2V2 - iOUT;$$
$$V3 = i3/sC3;$$

Scaled signal flow graph [2]:



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4.

(a) Theory (i and iii). Application of theory (ii).

i) For BJT: $Ic = Ise^{\frac{Vbe}{Vt}}$ [1].

Let the emitter node voltage be Vx.

Thus $Ic1 = Is1e^{\frac{Va/2-Vx}{Vt}}$ and $Ic2 = Is2e^{\frac{-Va/2-Vx}{Vt}}$.

Assume the transistors are matched so $Is1 = Is2 = Is$.

Therefore $Iout = Ic1 - Ic2 = Is(e^{\frac{\frac{Va}{2}-Vx}{Vt}} - e^{\frac{\frac{-Va}{2}-Vx}{Vt}}) = Ise^{\frac{-Vx}{Vt}}(e^{\frac{\frac{Va}{2}}{Vt}} - e^{\frac{\frac{-Va}{2}}{Vt}})$ [1].

For the constant current source: $Iq = Ic1 + Ic2 = Ise^{\frac{-Vx}{Vt}}(e^{\frac{\frac{Va}{2}}{Vt}} + e^{\frac{\frac{-Va}{2}}{Vt}})$ [1].

Combining these: $\frac{Iout}{Iq} = \frac{e^{\frac{\frac{Va}{2}}{Vt}} - e^{\frac{\frac{-Va}{2}}{Vt}}}{e^{\frac{\frac{Va}{2}}{Vt}} + e^{\frac{\frac{-Va}{2}}{Vt}}}$.

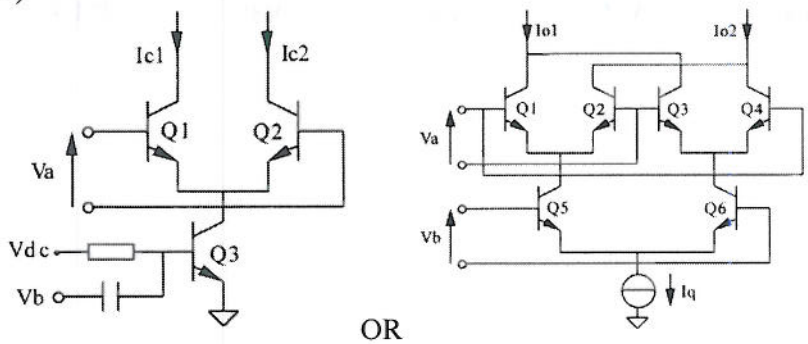
Using hint: $Iout = Iq \tanh(\frac{Va}{2Vt})$ [1].

Small angle approximation: $\tanh x \to x, x \to 0$.

Thus, if Va is small: $Iout = \frac{IqVa}{2Vt}$ [1].

ii) 25(Iq/Vt) nA/√Hz [2].

iii)



OR [2]

In both cases the Iq current source of Figure 4.1 is replaced by a transconductor (either a single transistor or differential pair). The required Iq is therefore generated by a voltage to current conversion. [1]

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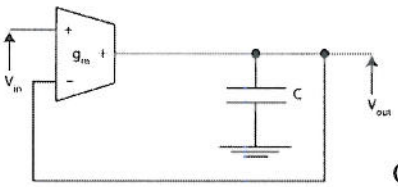
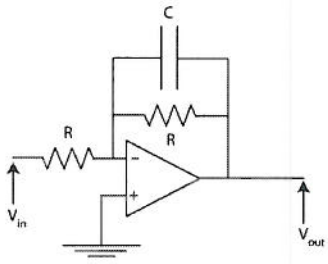
(b) Application of theory.

i)



OR.



(Note this second topology has 180 phase shift compared to the given transfer function) [1].

ii) First order filter has 20 dB attenuation per decade. 34 dB/20 dB = 1.7 decades. $10^{1.7}$ = 50.11 frequency span. Thus cut-off = 5.01 M/50.11 = 100 kHz [2].
~0 dB (is 1 decade below cut-off). Precise answer is 0.04 dB [1].

iii) Noise sources add as squares: $\sqrt{(7^2+24^2)}$ = 25 nV/√Hz [1].

iv)

$$T(f) = \frac{1}{1 + jf/fp}$$

To evaluate the equivalent noise bandwidth, we evaluate the total mean square noise power after filtering:

$$P(vno) = vn^2 \int_0^\infty |T(f)|^2 \, df = vn^2 NBW \qquad [1]$$

Thus $$NBW = \int_0^\infty \left| \frac{1}{1 + jf/fp} \right|^2 df$$

Substitute $f/fp = \tan\theta$ thus $df = fp \sec^2\theta \, d\theta$

$$NBW = \int_0^\infty \frac{1}{1+(f/fp)^2} df = \int_0^{\pi/2} \frac{1}{1+\tan^2\theta} fp \sec^2\theta \, d\theta = \int_0^{\pi/2} fp \, d\theta = fp\frac{\pi}{2} \qquad [2]$$

vn = 25 nV/√Hz so $vn^2 = 6.25 \times 10^{-16}$ V²/Hz.
Output noise power = π/2*fc*vn^2 = 98×10^{-12} V² [1].
Output noise voltage is 9.9 μVrms. [1]