Paper Number(s): **E3.11**
E4.42
AS4

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2002

MSc and EEE PART III/IV: M.Eng., B.Eng. and ACGI

ADVANCED ELECTRONIC DEVICES

Tuesday, 7 May 10:00 am

There are FIVE questions on this paper.

Answer THREE questions.

Corrected Copy

Time allowed: 3:00 hours

Examiners responsible:

First Marker(s): Fobelets,K.

Second Marker(s): Juhasz,C.

Special instructions for invigilators: None

Information for candidates:

$$V_{bi} = \frac{kT}{e}\ln\frac{N_A N_D}{n_i^2}$$

$$W_n = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{e}(V_0 - V)\frac{N_A}{N_A N_D + N_D^2}}$$

$$W_p = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{e}(V_0 - V)\frac{N_D}{N_A N_D + N_A^2}}$$

$$n = N_C \exp\left[\frac{-(E_C - E_F)}{kT}\right]$$

$$p = N_V \exp\left[\frac{(E_V - E_F)}{kT}\right]$$

$$D = \frac{\mu kT}{e}$$

$$\frac{dE}{dz} = \frac{e}{\varepsilon_0\varepsilon_r}(N_D + p - N_A - n)$$

Schottky contact current density :

$$J_{sch} = \frac{4\pi e m^* k^2 T^2}{h^3}\exp\left(\frac{-e\Phi_b}{kT}\right)\left[\exp\left(\frac{eV}{kT}\right) - 1\right]$$

pn diode current density :

$$J_{pn} = \left[\frac{eD_n n_{p_0}}{L_n} + \frac{eD_p p_{n_0}}{L_p}\right]\left[\exp\left(\frac{eV}{kT}\right) - 1\right]$$

e	=	$1.602\ 10^{-19}$ C
h	=	$6.626\ 10^{-34}$ Js
n_i	=	$1.45\ 10^{10}$ cm^{-3} for Si at 300K
n_i	=	$1.79\ 10^{6}$ cm^{-3} for GaAs at 300K
kT/q	=	0.026 V at 300 K
ε_0	=	$8.854\ 10^{-12}$ F/m
m_0	=	$0.911\ 10^{-30}$ kg
N_{CSi}	=	$2.8\ 10^{19}$ cm^{-3}
N_{VSi}	=	$1.04\ 10^{19}$ cm^{-3}
N_{CGaAs}	=	$4.7\ 10^{17}$ cm^{-3}
N_{VGaAs}	=	$7\ 10^{18}$ cm^{-3}
$\varepsilon_r^{SiO_2}$	=	4
ε_r^{Si}	=	11.7
ε_r^{GaAs}	=	13.1

$m_{nSi} = 0.19$
$m_{hSi} = 0.49$

E_G	=	1.42 eV for GaAs at 300K
E_G	=	2.18 eV for AlAs at 300K
E_G	=	1.12 eV for Si at 300K
E_G	=	0.66 eV for Ge at 300K

Element	Work function Φ_m (V)
Au	5.1
W	4.55

Element	Electron affinity, χ (V)
Si	4.01
GaAs	4.07
AlAs	3.5

1. Heterojunctions

i) Sketch the ideal energy-band diagram of the pn-heterojunction formed by p-GaAs – n-$Al_{0.3}Ga_{0.7}As$ in thermal equilibrium and without external bias. Include E_c, E_v, E_f, E_g, ΔE_c and ΔE_v
Indicate the depletion width in the p (z_p) and the n-doped (z_n) regions. [8]

ii) Is it possible to design a pn-homojunction with a non-symmetry in the conduction and valence band offset? Give a brief reason for your answer. [2]

iii) Derive the expression for the depletion width in the n- and the p-doped region of the p-GaAs – n-$Al_{0.3}Ga_{0.7}As$ heterojunction of part i). The Poisson equation is given on page1. [10]

2. Gating JFET ↔ MESFET

The parameters of the ideal n-channel Si JFET and MESFET used in this question are:

Si MESFET: W as gate metal
$N_D = 10^{16}$ cm^{-3}.

Si JFET: $N_A = 10^{18}$ cm^{-3}, $N_D = 10^{16}$ cm^{-3},
$D_p = 10$ cm^2/s, $D_n = 25$ cm^2/s,
$L_p = 10^{-3}$ cm, $L_n = 1.5\ 10^{-3}$ cm.

All calculations to be carried out at T=300K.

i) Calculate the built-in voltage V_{bi} for the a) JFET and b) MESFET. [5]

ii) Compare the gate leakage current (reverse bias) of the MESFET gate to that of the JFET. [5]

iii) Compare the turn-on voltage for a forward bias current density of 10 A/cm^2 for both MESFET and JFET. [4]

iv) Based on the results calculated in i), ii) and iii), answer the following questions:

a) which FET has the highest input resistance in reverse bias and why? [2]

b) which FET shows the highest switching speed? [2]

c) sketch on the same graph the gate current - gate-source voltage characteristics for the JFET and MESFET. [2]

3. biCMOS

i) Discuss briefly what is meant by biCMOS technology and why it is used in communication systems like mobile phones. [6]

ii) In which device of biCMOS technology was SiGe introduced. Give at least two reasons for introducing SiGe and discuss the performance improvement it yields compared to a) GaAs technology and b) pure Si technology. [8]

iii) Out diffusion of boron doping during the high thermal processing steps is a problem in SiGe biCMOS technology. Give two reasons why diffusion of boron doping degrades the performance of the device and give a way to minimise this out diffusion. [6]

4. FET ↔ HBT

i) Draw the intrinsic small signal equivalent circuit of a FET for frequencies lower than 1 GHz and give the physical interpretation for each component. [5]

ii) Draw the intrinsic hybrid π small signal equivalent circuit of a Bipolar Transistor (BT) for frequencies lower than 1 GHz and give the physical interpretation for each component. [5]

iii) Derive the expression for the channel transit time τ_t for a n-channel GaAs FET at low electric field and the base transit time τ_b for a npn GaAs BT (no material gradients in the base). [5]

iv) Calculate the cut-off frequency f_T of the FET and BT in iii) based on τ_t and τ_b respectively, at room temperature, and given the following parameters: [2]

FET: gate length $L_g = 0.5\ \mu m$
gate width $W_g = 50\ \mu m$
e^- mobility $\mu_n = 2000\ cm^2/Vs$
h^+ mobility $\mu_h = 500\ cm^2/Vs$
electric field $E = 1000\ V/cm$

BT: base width $W_b = 0.5\ \mu m$
base collector depletion width $W_{bc} = 2\ \mu m$
electron diffusion constant $D_n = 52\ cm^2/s$
hole diffusion constant $D_h = 13\ cm^2/s$
$V_{BE} = 0.6V$

v) Explain briefly why the cut-off frequency calculated in iv) for both the FET and BT is too high compared to the performance of real devices. [3]

5. General questions

a) Given the conduction band diagram of a GaAs HEMT from gate to bulk (see figure 5.1), draw the density of states in the quantum well for this structure. [2]

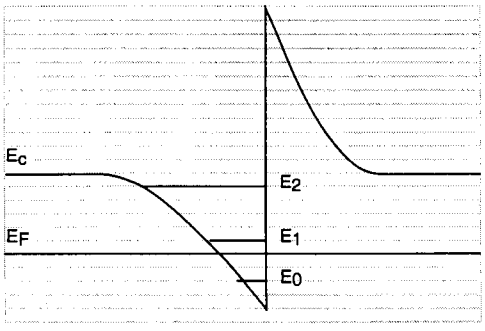

Figure 5.1: Conduction band diagram of HEMT.

b) Why is the region immediately underneath the gate metal of a JFET highly doped? [2]

c) Sketch the energy band diagram (include E_c, E_v, E_f, E_g) from gate to channel of a p-channel MESFET at V_{GS}=0V. Give the condition on the work function difference for good gate action. [2]

d) Why is the mobility of the electrons in the channel of a GaAs/AlGaAs HEMT higher than in a GaAs MESFET with the same geometry and carrier density in the channel? [2]

e) Emitter current crowding is important in power bipolar transistors. How can the un-homogeneous emitter current density be avoided by using processing techniques? [2]

f) Why is the input noise current for a FET very small? [2]

g) How can the base transit time in a Si/SiGe HBT be improved and give the reason for the improvement. [2]

h) Can a gunn diode be made in Si? Give the explanation for your answer. [2]

i) Fig. 2 gives the current-voltage characteristics of a GaAs/AlGaAs resonant tunnelling diode. Sketch the energy band diagram corresponding to the bias points A, B and C of figure 5.2. Include E_c, E_v, E_f, E_g, ΔE_c and ΔE_v

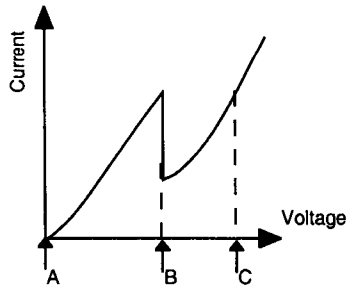

Figure 5.2: Current-voltage characteristics of RTD

j) Give a reason for the use of biCMOS technology. [1]

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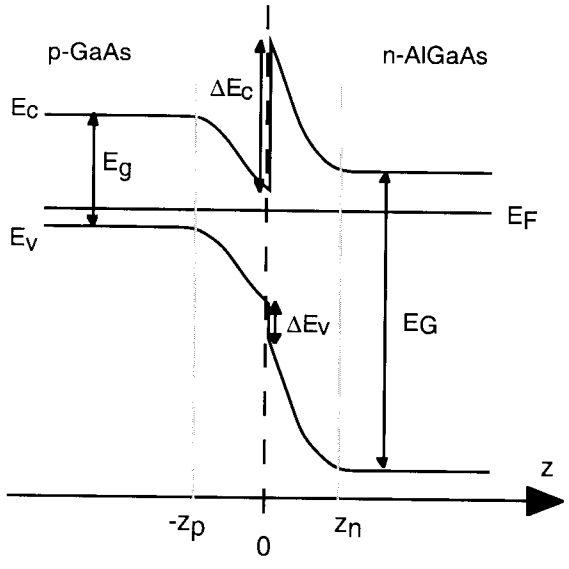
Model answers and Mark Schemes First Examiner: Dr. K. Fobelets

Paper Code: E3.11 Second Examiner: Dr. C.Juhasz

Question Number etc. in left margin Mark allocation in right margin

Q1 Heterojunctions

i) [8]



ii) no, since a difference in band gap of the two materials forming the junction is needed. [2]

iii) [10]

Poisson equation : $\frac{dE}{dz} = \frac{e}{\varepsilon_0 \varepsilon_r}(p - n - N_A + N_D)$

$$\begin{cases} (1)\ \frac{dE}{dz} = 0 & z < -z_p \\ (2)\ \frac{dE}{dz} = \frac{-N_A e}{\varepsilon_0 \varepsilon_{GaAs}} & -z_p < z < 0 \\ (3)\ \frac{dE}{dz} = \frac{N_D e}{\varepsilon_0 \varepsilon_{AlGaAs}} & 0 < z < z_n \\ (4)\ \frac{dE}{dz} = 0 & z > z_n \end{cases}$$

$E = -\frac{dV}{dz}$ (5)

(5) in (2) : $\frac{d^2V}{dz^2} = \frac{N_A e}{\varepsilon_0 \varepsilon_{GaAs}}$ $-z_p < z < 0$

Integrate : $\frac{dV}{dz} = \frac{N_A e}{\varepsilon_0 \varepsilon_{GaAs}} z + C_1$

@ $z = -z_p$ $\frac{dV}{dz} = 0 \Rightarrow C_1 = \frac{N_A e}{\varepsilon_0 \varepsilon_{GaAs}} z_p$

thus : $\frac{dV}{dz} = \frac{N_A e}{\varepsilon_0 \varepsilon_{GaAs}}(z + z_p)$

Integrate : $V = \frac{N_A e}{\varepsilon_0 \varepsilon_{GaAs}}(z + z_p)^2 + C_2$

@ $z = -z_p$ $\quad V(-z_p) = V(-\infty)$ (continuity) $\Rightarrow \quad C_2 = V(-\infty)$

thus solution : $V(z) = \frac{N_A e}{2\varepsilon_0 \varepsilon_{GaAs}}(z + z_p)^2 + V(-\infty) \qquad -z_p < z < 0$

(5) in (3) : $\frac{d^2V}{dz^2} = \frac{-N_D e}{\varepsilon_0 \varepsilon_{AlGaAs}} \qquad 0 < z < z_n$

identical to above : $V(z) = \frac{-N_D e}{2\varepsilon_0 \varepsilon_{AlGaAs}}(z - z_n)^2 + V(+\infty) \qquad 0 < z < z_n$

Continuity in $z = 0$:

1) $\varepsilon_{GaAs} E(z \to -0) = \varepsilon_{AlGaAs} E(z \to +0)$

gives : $\frac{N_A e}{\varepsilon_0} z_p = \frac{N_D e}{\varepsilon_0} z_n$ or $N_A z_p = N_D z_n$ (6)

2) $V(z \to -0) = V(z \to +0)$

gives : $\frac{N_A e}{2\varepsilon_0 \varepsilon_{GaAs}}(z_p)^2 + V(-\infty) = \frac{-N_D e}{2\varepsilon_0 \varepsilon_{AlGaAs}}(z_n)^2 + V(+\infty)$

$V_{bi} = V(+\infty) - V(-\infty) = \frac{N_A e}{2\varepsilon_0 \varepsilon_{GaAs}}(z_p)^2 + \frac{N_D e}{2\varepsilon_0 \varepsilon_{AlGaAs}}(z_n)^2$ (7)

(6) $\to z_p^2 = \left(\frac{N_D}{N_A} z_n\right)^2$

in (7) : $V_{bi} = \frac{N_A e}{2\varepsilon_0 \varepsilon_{GaAs}}\left(\frac{N_D}{N_A} z_n\right)^2 + \frac{N_D e}{2\varepsilon_0 \varepsilon_{AlGaAs}}(z_n)^2$

$V_{bi} = \frac{e}{2\varepsilon_0 \varepsilon_{GaAs}} \frac{N_D^2}{N_A}(z_n)^2 + \frac{N_D e}{2\varepsilon_0 \varepsilon_{AlGaAs}}(z_n)^2 = \frac{e}{2\varepsilon_0}\left(\frac{1}{N_A \varepsilon_{GaAs}} + \frac{1}{N_D \varepsilon_{AlGaAs}}\right) N_D^2 z_n^2$

$z_n = \sqrt{\frac{2V_{bi} N_A \varepsilon_0 \varepsilon_{GaAs} \varepsilon_{AlGaAs}}{e N_D (N_A \varepsilon_{GaAs} + N_D \varepsilon_{AlGaAs})}}$

(6) $\to z_n^2 = \left(\frac{N_A}{N_D} z_p\right)^2$

in (7) : $V_{bi} = \frac{N_A e}{2\varepsilon_0 \varepsilon_{GaAs}}(z_p)^2 + \frac{N_D e}{2\varepsilon_0 \varepsilon_{AlGaAs}}\left(\frac{N_A}{N_D} z_p\right)^2$

$V_{bi} = \frac{e}{2\varepsilon_0}\left(\frac{1}{N_A \varepsilon_{GaAs}} + \frac{1}{N_D \varepsilon_{AlGaAs}}\right) N_A^2 z_p^2$

$z_p = \sqrt{\frac{2V_{bi} N_D \varepsilon_0 \varepsilon_{GaAs} \varepsilon_{AlGaAs}}{e N_A (N_A \varepsilon_{GaAs} + N_D \varepsilon_{AlGaAs})}}$

$W = z_p + z_n$

Q2 Gating JFET ↔ MESFET

i) a) JFET [5]

pn-junctions control gating in JFETs, the built-in voltage V_{bi} expression is given in the formulae sheet.

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) = 0.026\ln\left(\frac{10^{18}10^{16}}{\left(1.45\,10^{10}\right)^2}\right) = 0.819V$$

b) MESFET

Schottky contact controls gating in MESFETs. The Schottky barrier and the doping density in the semiconductor determine the built-in voltage.

$$\text{Schottky barrier}: \phi_b = \left(\phi_m - \chi\right)$$

$$\text{Built-in voltage}: V_{bi} = \phi_b - \frac{\left(E_c - E_f\right)}{q}$$

$$\text{Maxwell-Boltzman}: n = N_C \exp\left[\frac{-\left(E_c - E_f\right)}{kT}\right] \Rightarrow -\left(E_c - E_f\right) = kT\ln\left(\frac{n}{N_C}\right)$$

$$V_{bi} = \phi_b + \frac{kT}{q}\ln\left(\frac{n}{N_C}\right) = 4.55 - 4.01 + 0.026\ln\left(\frac{10^{16}}{2.8\,10^{19}}\right) = 0.334V$$

ii)The gate leakage currents are the reverse bias currents in the gate diodes. [5]

See current density equations on formulae sheet.

The exponential term in both current expressions is negligible in reverse bias.

a) JFET

$$J_{pn_{rev}} = -\left[\frac{eD_n n_{p_0}}{L_n} + \frac{eD_p p_{n_0}}{L_p}\right]$$

$$n_{p_0} = \frac{n_i^2}{p_{p_0}} = \frac{n_i^2}{N_A} = \frac{\left(1.45\,10^{10}\right)^2}{10^{18}} = 2.103\,10^2\ cm^{-3} \quad \text{minority carrier expression}$$

$$p_{n_0} = \frac{n_i^2}{n_{n_0}} = \frac{n_i^2}{N_D} = \frac{\left(1.45\,10^{10}\right)^2}{10^{16}} = 2.103\,10^4\ cm^{-3} \quad \text{minority carrier expression}$$

$$J_{pn_{rev}} = -\left[\frac{1.602\,10^{-19}\ 25\ 2.103\,10^2}{1.5\,10^{-3}} + \frac{1.602\,10^{-19}\ 10\ 2.103\,10^4}{10^{-3}}\right] = -\left(5.615\,10^{-13} + 3.369\,10^{-11}\right) = -3.425\,10^{-11}\,A/cm^2$$

b) MESFET

The gate leakage currents in MESFETs are much larger than the gate leakage currents in JFETs.

$$J_{sch_{rev}} = -\frac{4\pi e m^* k^2 T^2}{h^3}\exp\left(\frac{-e\Phi_b}{kT}\right) = -\frac{4\pi e^3 m^* \left(kT/e\right)^2}{h^3}\exp\left(\frac{-e\Phi_b}{kT}\right)$$

$$J_{sch_{rev}} = -\frac{4\pi\left(1.602\,10^{-19}\right)^3\ 0.19\ 0.911\,10^{-30}\ (0.026)^2}{\left(6.626\,10^{-34}\right)^3}\exp\left(-\frac{(4.55-4.01)}{0.026}\right)$$

$$J_{sch_{rev}} = -19.85\ A/m^2 = -19.85\,10^{-4}\ A/cm^2$$

iii) The turn-on voltage is the voltage at which the gate starts conducting. This means that the –1 term in the current expressions is negligible. (see reverse bias current values in ii) [4]

JFET:

$$J_{pn} = J_{pn_{rev}}\left[\exp\left(\frac{eV_{on}}{kT}\right)\right]$$

$$V_{on} = \frac{kT}{q}\ln\left(\frac{J_{pn}}{J_{pn_{rev}}}\right)$$

$$V_{on} = 0.026\ln\left(\frac{10}{3.425\,10^{-11}}\right) = 0.686V$$

MESFET:

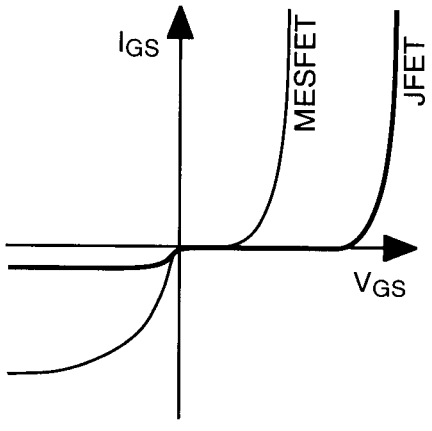
$$J_{sch} = J_{sch_{rev}}\left[\exp\left(\frac{eV_{on}}{kT}\right)\right]$$

$$V_{on} = \frac{kT}{q}\ln\left(\frac{J_{sch}}{J_{sch_{rev}}}\right)$$

$$V_{on} = 0.026\ln\left(\frac{10}{19.85\,10^{-4}}\right) = 0.22V$$

The turn-on voltage of the MESFET is lower than the turn-on voltage of the JFET.

iv) a) the JFET because the reverse bias current through the gate is lowest. [6]
b) MESFET
c)



Q3 biCMOS

Essential information is underlined.
i) biCMOS technology is a processing technology which allows to monolithically integrate bipolar transistors with Si CMOS. The reason for this integration in communication applications is the need for an integration of the digital and analogue part, the need for low power and low noise performance, and the need for compact portable circuits. The digital part is performed by Si CMOS which has low power and low noise characteristics. However the analogue part needs to operate at much higher frequencies, therefore bipolar transistors are more useful. [6]

ii) SiGe was introduced in the base region of the bipolar transistor. The use of SiGe in the base of the bipolar transistor has several advantages.

a) Compared to GaAs technology

Currently GaAs is/was used for the rf analogue circuits, however the use of III-V materials inhibits an easy and cheap integration of the Si CMOS digital part with the analogue circuits. The noise performance of Si-based materials is better than that of III-V materials. The low frequency noise of SiGe HBTs is better than GaAs due to the existence of a native oxide for Si. The thermal conductivity of SiGe is better than that of GaAs important for power transistors.

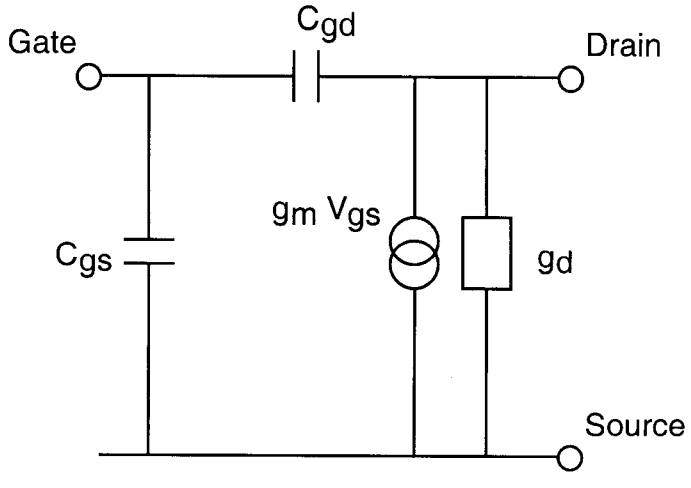
b) Compared to Si technology

Introducing SiGe in the base of the bipolar transistor improves the emitter efficiency and the current gain of the transistor. This is due to the band gap difference which results in a valence band discontinuity which acts as a potential barrier for holes flowing from base to emitter. This reduces hole current, improving γ. The bandgap difference between base and emitter occurs in an exponential term in the current gain β. This gain improvement allows for an increased base doping (which decreases the emitter efficiency) generating a lower base resistance and thus higher operation frequency. [8]

c) During the high thermal steps for e.g. anneal of doping implantation damage, boron doping in the base layer of the bipolar transistor diffuses into the emitter and collector region. This out-diffusion of p-type doing atoms increases the effective base width, which allows for more recombination current to occur in the base (degrades the emitter efficiency). More over in the case of a SiGe base, a part of the increased base which is Si will be at the emitter side and thus the barrier for hole current from the base to the emitter is not existent at that point which will reduce the gain of the transistor. The lack of Ge at the collector side of the HBTs in biCMOS technology (only the base is SiGe in SiGe biCMOS technology) introduces a barrier for the electrons which reduces the collector current and degrades the Early voltage of the device.

Small amounts of C are included in the base (SiGeC) region of the tansistors and have shown reduced out diffusion of B atoms from the base. [6]

Q4 FET ↔ HBT



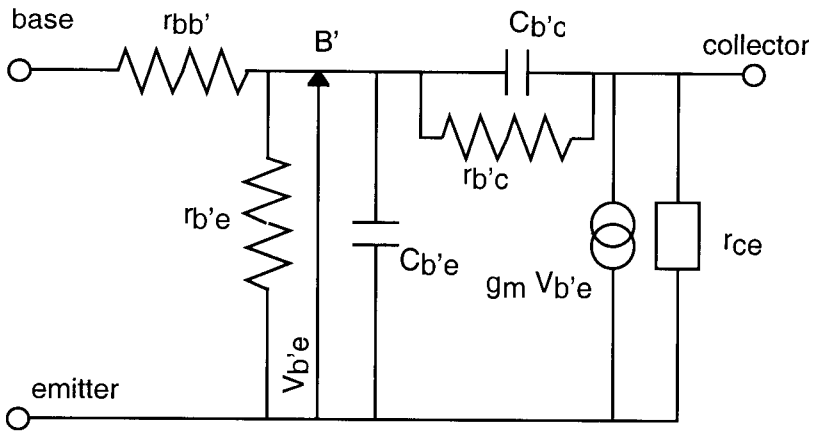
i) [5]

C_{gd} : gate drain capacitance, is the variation of the charge under the gate as a function of the drain voltage

C_{gs} : gate source capacitance, is the variation of the charge under the gate as a function of the source voltage

g_m V_{gs}: current source, current through the channel controlled by the gate. g_m is the transconductance, is a measure for the control of the gate on the channel.

g_d: output conductance, a finite output conductance is due to gate length modulation.



ii)
$r_{bb'}$: base spreading resistance, gives rise to a voltage drop due to emitter current crowding
$C_{b'e}$: emitter-base junction capacitance (diffusion + depletion capacitance)
$r_{b'e}$: emitter-base junction diffusion resistance
$C_{b'c}$: collector-base junction capacitance (diffusion + depletion capacitance)
$r_{b'c}$: collector-base junction diffusion resistance (large)
$g_m V_{gs}$: current source, collector current dependent on the internal base-emitter voltage. r_{ce}: output resistance primarily due to the early effect. [5]

iii) n-channel FET [5]
$\tau_t = L/v = L/\mu E$
With L: channel length, m: mobility and E: electric field.

npn BT:
Charge in base of npn (electrons):

$$Q_b = \frac{en'_p W}{2} \quad (n''_p << n'_p)$$

$$Q_b = \frac{en_{p_0} e^{\frac{eV_{be}}{kT}} W}{2}$$

Electron current injected into base from emitter:

$$I_e = \frac{eD_n n_{p_0}}{W} e^{\frac{eV_{be}}{kT}}$$

$$e^{\frac{eV_{be}}{kT}} = \frac{I_e W}{eD_n n_{p_0}}$$

into Q_b

$$Q_b = \frac{en_{p_0} I_e W^2}{2eD_n n_{p_0}} = \frac{I_e W^2}{2D_n}$$

The base transit time is determined by the emitter-base diffusion capacitance:

$$C_{be_{diff}} = \frac{dQ_b}{dV_{be}}$$

$$C_{be_{diff}} = \frac{W^2}{2D_n} \frac{dI_e}{dV_{be}} = \frac{W^2}{2r_e D_n}$$

Hence the charging time becomes:

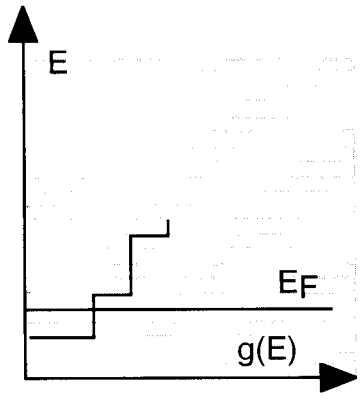
$$\tau_b = C_{be_{diff}} r_e = \frac{W^2}{2D_n}$$

iv) FET: $f_T = 1/\tau_t = \mu E/L = 2000\ 1000/(0.5\ 10^{-4}) = 4\ 10^{10}$ Hz = 40 GHz [2]
BT: $f_T = 1/\tau_b = 2\ D_n/W^2 = 2\ 52//(0.5\ 10^{-4})^2 = 4.16\ 10^{10}$ Hz = 41.6 GHz

v) FET: the intrinsic and extrinsic capacitance and resistance values of the FET are ignored in the cut-off frequency calculation based on channel transit time.
BT: In the calculation of the cut-off frequency the complete emitter-collector delay has to be taken into account, meaning that in the calculations of iv) the collector depletion transit time, collector capacitance charging time, emitter capacitance charging time have been ignored. Further reductions in f_T will be due to external parasitics. [3]

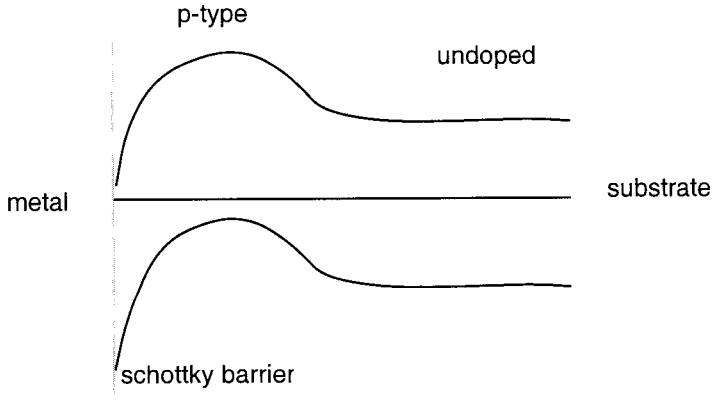
Q5 general questions

i) [2]



ii) The gate needs to control the conduction in the channel, therefore the depletion variation caused by the gate should mainly happen in the channel region. When the region under the gate is highly doped and the channel lightly doped the depletion width will extend in the least doped area thus mainly in the channel. [2]

iii)



Condition on work function difference for good schottky barrier on p-type material is:

$\phi_{semiconductor} > \phi_{metal}$

(then transfer of electrons from the metal to the semiconductor will happen, making the semiconductor more n-type near junction and creating a barrier for holes)

[2]

iv) Because in HEMTs modulation doping is being used, which means that the doping layer is separated from the channel layer, reducing impurity scattering and thus increasing the mobility of the carriers in the undoped channel. [2]

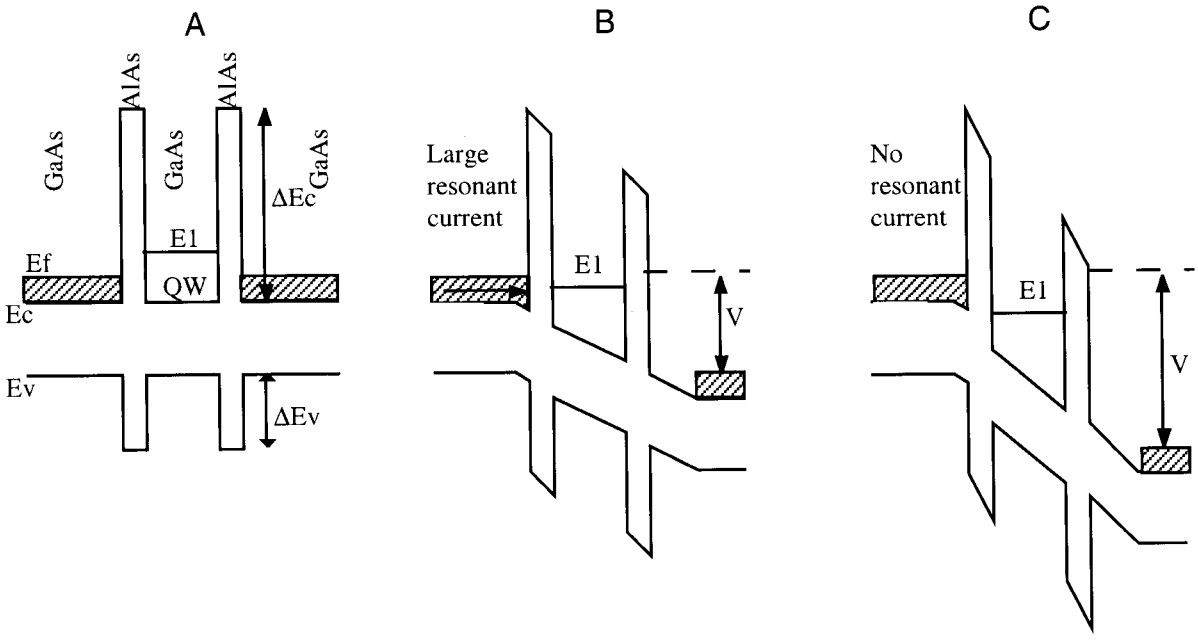
v) By the use of an interdigitated transistor structure such that the emitter contacts are only occupying the width of the emitter current crowding. [2]

vi) Because the input noise current for a FET is determined by the gate leakage current which is normally very small. [2]

vii) When using a grading in Ge (from high at the emitter side to low at the collector side) in the base τ_b can be improved because the gradient causes an internal electric field in the base which enhances the diffusion by a drift term [2]

viii) No, because the gunn effect is caused by the special character of the band diagram of GaAs. Scattering of electrons from the Γ into the L band causes a negative differential velocity curve of GaAs on which the gunn effect is based. This feature is absent in Si. [2]

ix) [3]



x) Integration of digital (FET) and analogue rf electronics (Bipolar) for optimum speed (bipolar) and power consumption (FET) for hybrid designs, generally used in mobile communication systems. [1]