Paper Number(s): **E1.1**

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2002

EEE/ISE PART I: M.Eng., B.Eng. and ACGI

ANALYSIS OF CIRCUITS

Wednesday, 5 June 10:00 am

There are FIVE questions on this paper.

Answer THREE questions.

Time allowed: 2:00 hours

Examiners responsible:

First Marker(s): Spence,R.

Second Marker(s): Weiss,G.

Corrected copy

Special Information for Invigilators	NIL
Information for Candidates	Supplementary sheet for Q1 is provided This sheet needs to be tied into the answer booklet

1. The voltage waveform shown below in Figure 1a, and reproduced on a separate sheet, is applied to the input terminal A of the circuit shown in Figure 1b. The light grid is provided to enable you to read off voltage values where necessary. The opamp can be considered ideal, with output limiting occurring at +/- 12 Volts. Under the assumption that the voltage at the output terminal B is at 12 volts immediately after t = 0, determine the waveform of the voltage at terminal B, from t = 0 to t =180 ms, *and plot it on the separate sheet.* Be sure to tie that sheet inside your answer book. [10]

At t = 30 ms the voltage at point B is connected to the input terminal D of the circuit shown in Figure 1c. Under the assumption that, at time t = 30 mS, the voltage across the capacitor C is zero, provide a dimensioned sketch, on the separate sheet provided, of the waveform of the voltage at point E up to t =150 ms. [10]

Explain all your answers.

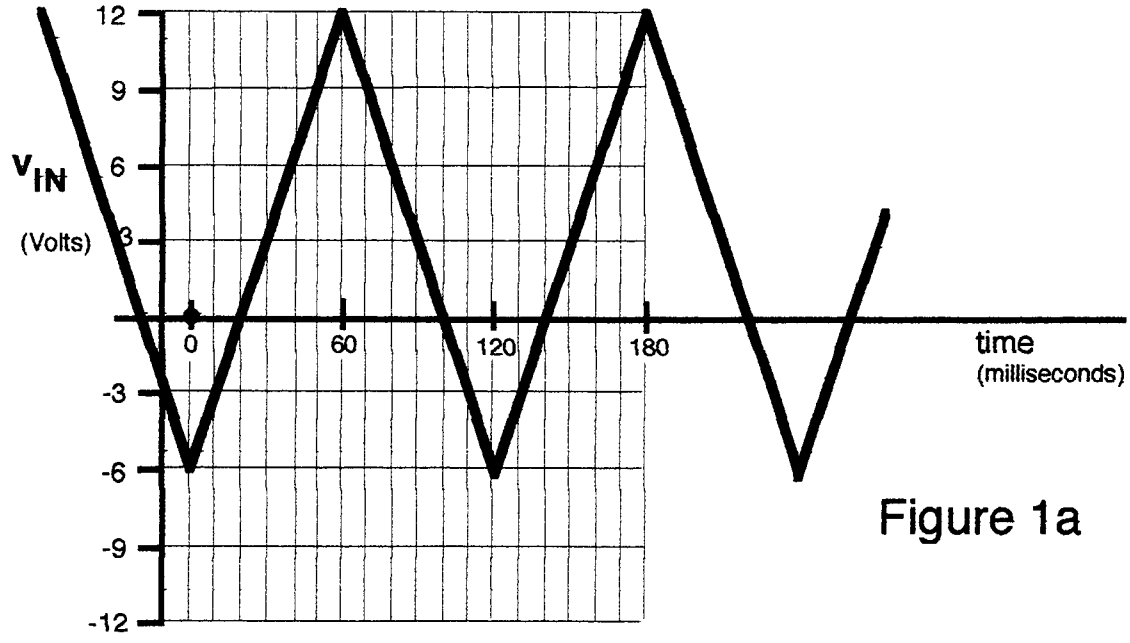


Figure 1a

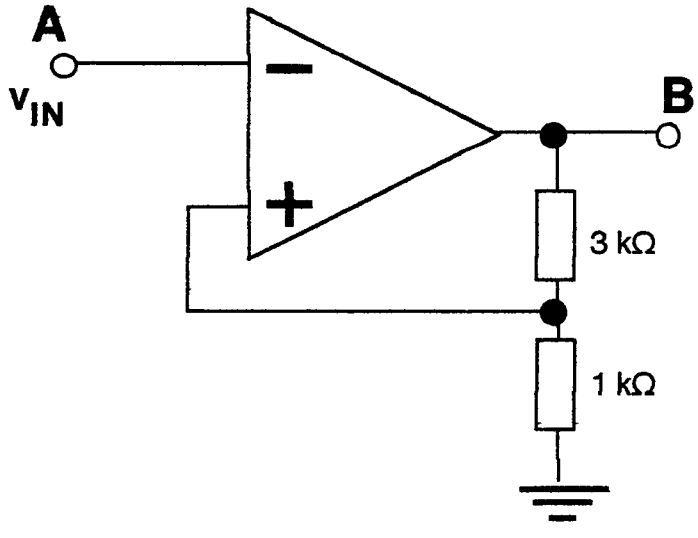


Figure 1b

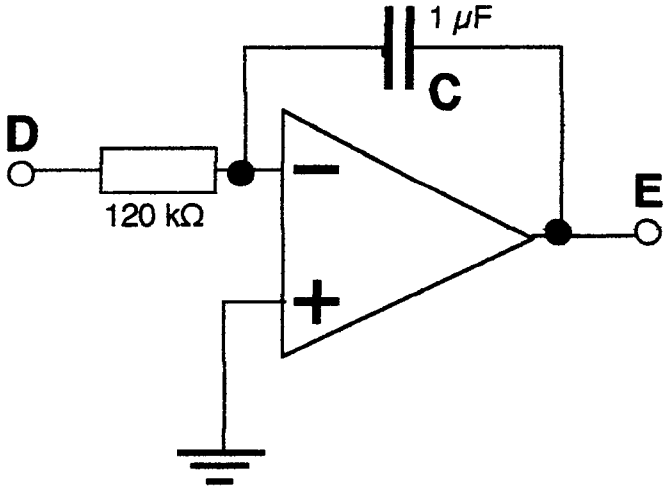


Figure 1c

2. (a) The circuit of Figure 2 contains two sinusoidal voltage sources described by the complex voltage V_S. These sources are identical in both magnitude and phase. By analysing the circuit determine the frequency at which the ratio V^*/ V_S is real. [6]

(b) For this frequency

(i) sketch the phasor diagram for the RC circuit and separately for the LR circuit, and [4]
(ii) combine the two phasor diagrams, taking into account the fact that the phasor V_S appears in both. [4]
Show that this latter phasor diagram is compatible with the fact that V^*/V_S is real. [4]

(c) What is the magnitude of V^* at this frequency if the value of R is now chosen to be $(L/C)^{0.5}$? . [2]

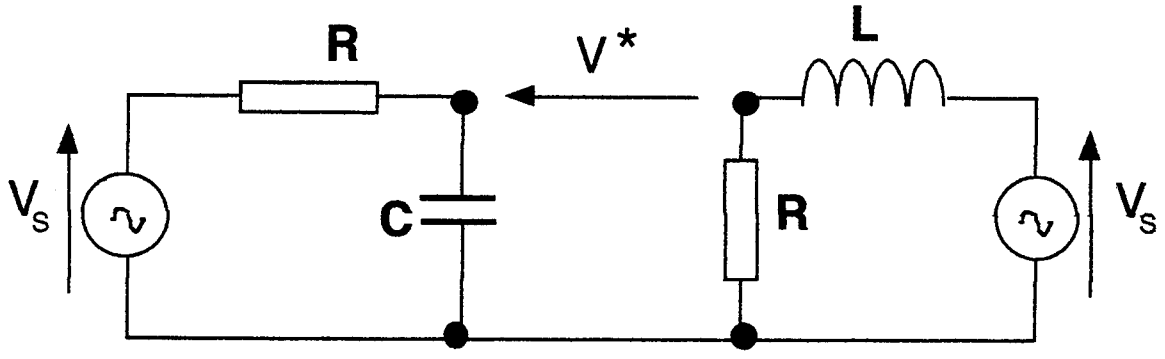


Figure 2

3. For the circuit of Figure 3, calculate the value of the current I by two methods:
(a) by using the Superposition Principle, and [10]
(b) by first replacing all except the 5 Ω resistor by a Thevenin Equivalent Circuit. [10]

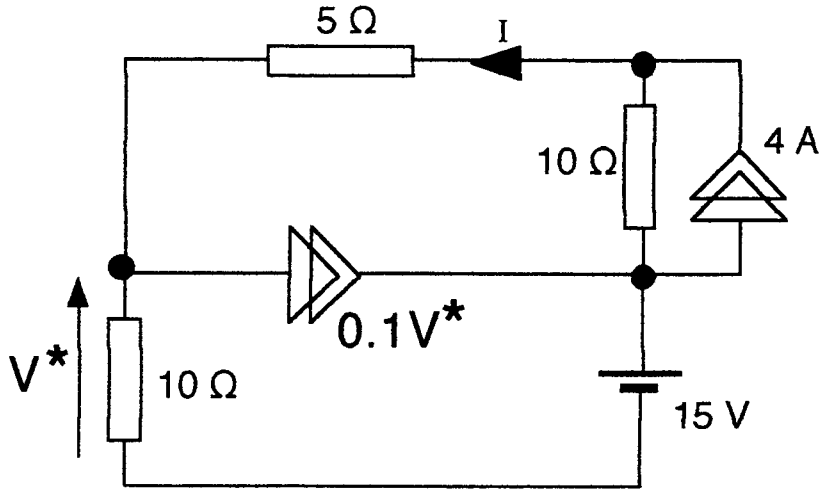


Figure 3

4. The circuit of Figure 4a is designed to supply an essentially constant voltage of 5 V to the resistive load R. The small-signal internal resistance of the Zener diode when operating as intended is 20 Ω.

(a) By making appropriate assumptions, calculate the maximum and minimum values of R to ensure that (i) the voltage V remains at essentially 5 V, and (ii) that the curent through the Zener diode does not exceed 9 mA. [6]

(b) For R = 1000 Ω calculate the change in load voltage V resulting from a 1% change in the supply voltage whose nominal value is 15 V. [4]

(c) The same Zener diode is now employed in the circuit of Figure 4b, again in order to supply an essentially constant voltage of 5 V to the resistive load R. For R = 1000 Ω, calculate the change in load voltage V resulting from a 1% change in the supply voltage whose nominal value is 15 V. In your analysis the transistor may be replaced by the equivalent circuit shown in Figure 4c, with g = 200 mA/volt. For this circuit the Zener diode current is allowed to exceed 9 mA. [6]

With regard to the variation in load voltage due to a variation in the supply voltage, does the circuit of Figure 4b offer any significant advantage? What advantage is achieved by the introduction of the transistor in the circuit of Figure 4b? [4]

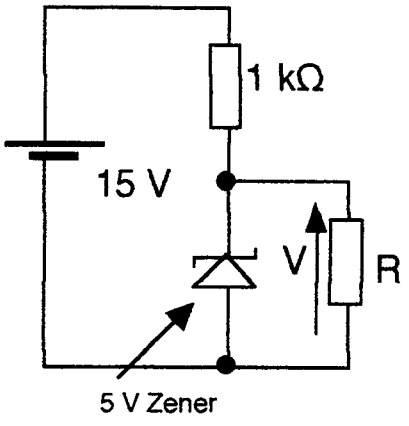


Figure 4a

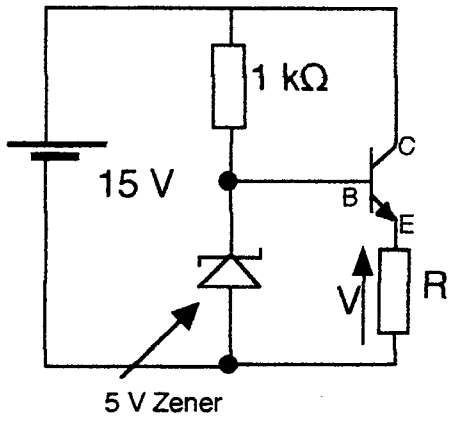


Figure 4b

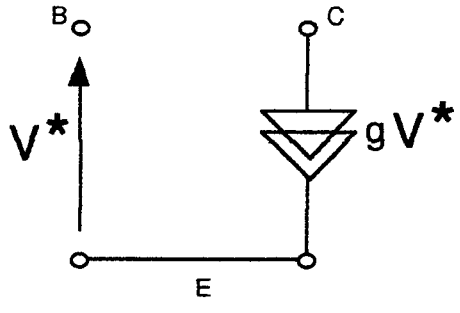


Figure 4c

5. Each of the two circuits shown in Figure 5a,b contains a sinusoidal voltage source of frequency ω described by a complex voltage V_S , and generates an output voltage V_O.

(a) For each circuit derive an expression for the voltage ratio V_O/V_S. Hence provide a dimensioned sketch, for each circuit, of the asymptotes of the relation between the magnitude of V_O/V_S and the radian frequency ω, using logarithmic axes. [6]

(b) The circuit of Figure 5c is designed to act as a filter. The opamps may be assumed to be ideal.

There is a 'mid-band' range of frequencies for which the capacitor and inductor have negligible effect on the magnitude of the voltage gain V_Y/V_X. For that range of frequencies calculate the value of $|V_Y/V_X|$. [2]

Using the results of part (a), provide a dimensioned sketch of the asymptotes of the relation between $|V_Y/V_X|$ and the radian frequency ω. [12]

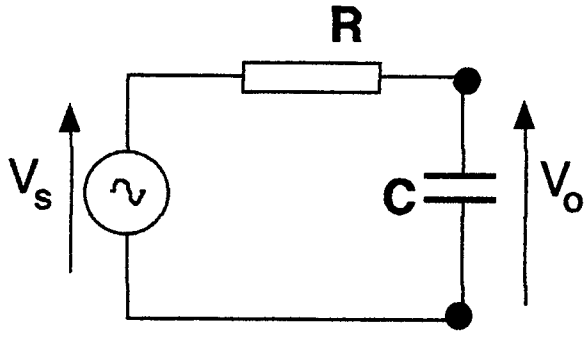


Figure 5a

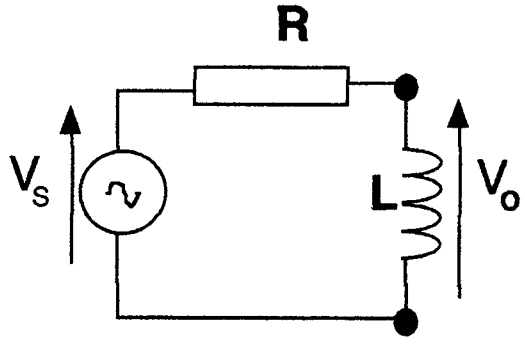


Figure 5b

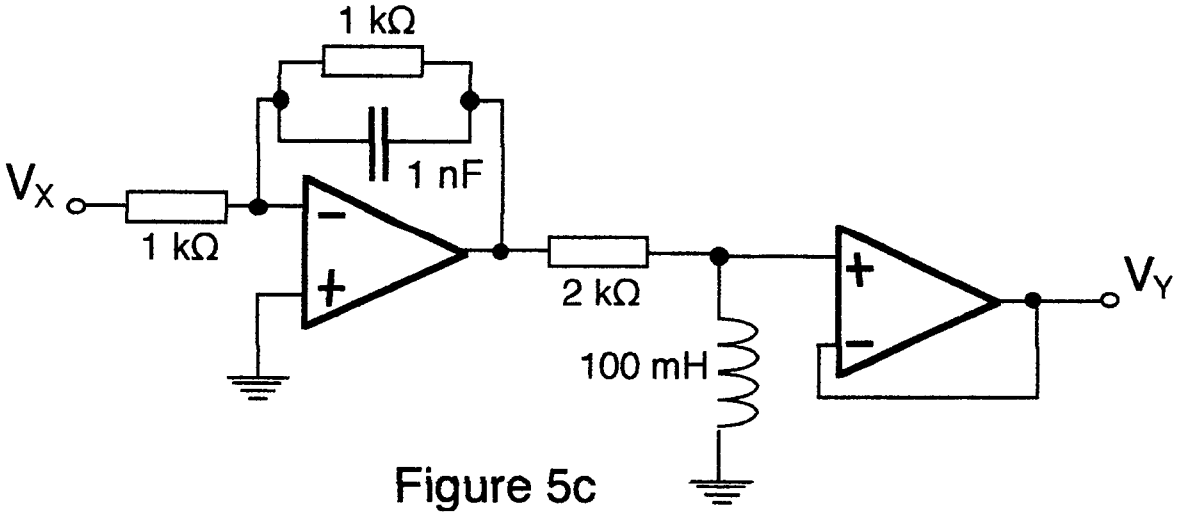
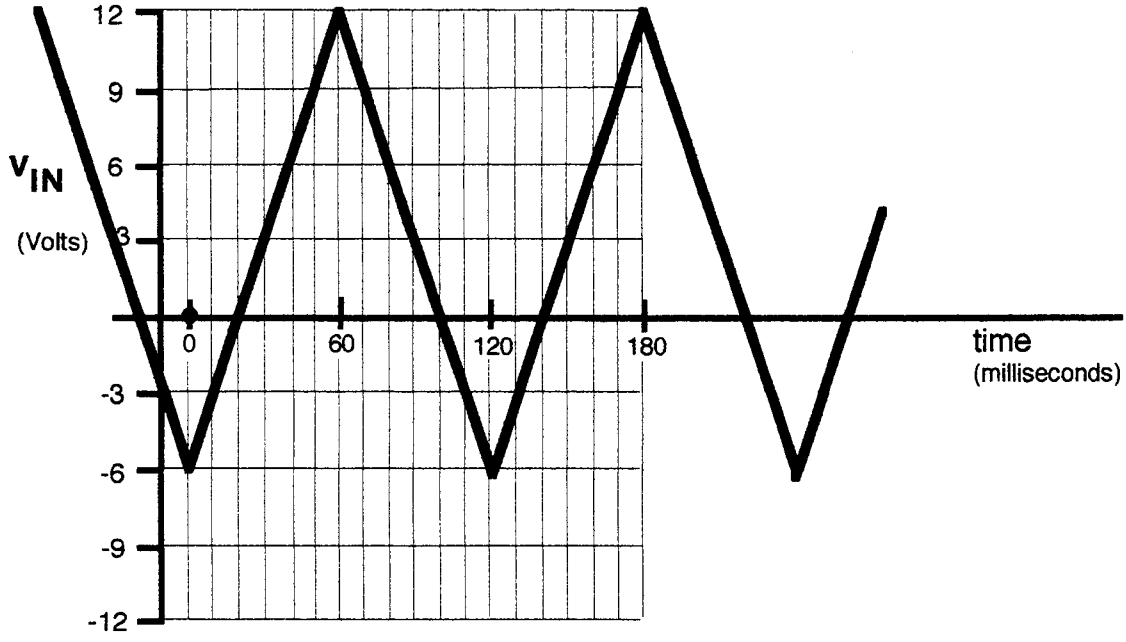
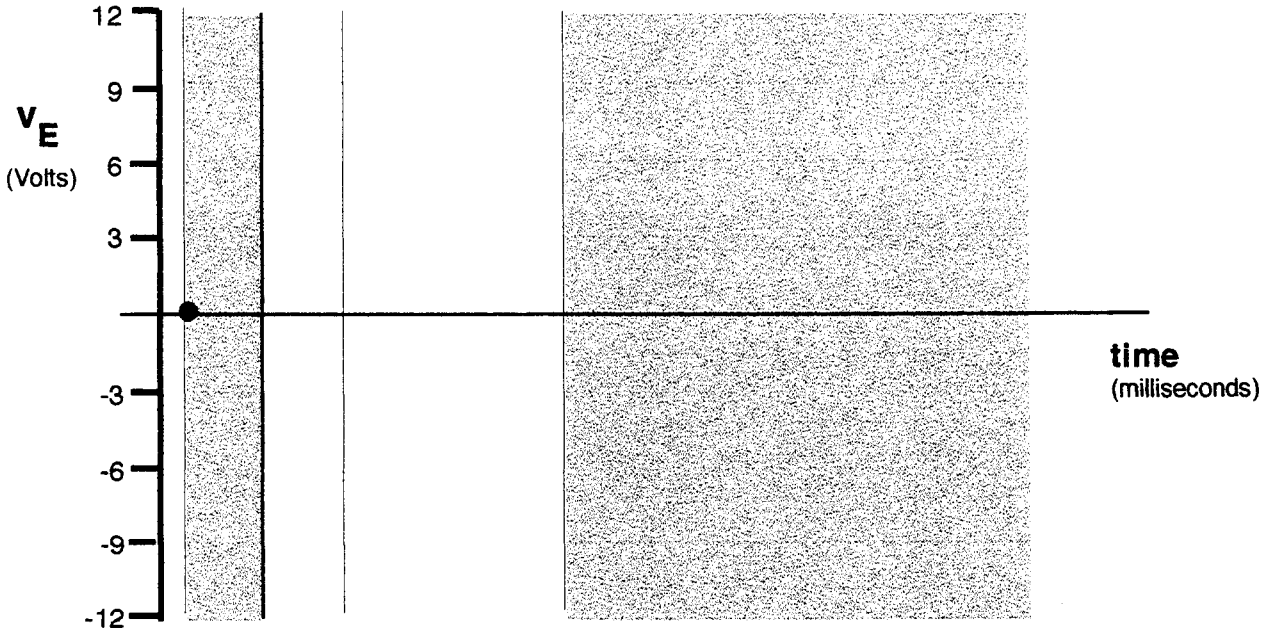


Figure 5c

EE 1.1 exam 2002 Supplementary sheet for question 1. To be tied into answer sheet.





SOLUTIONS - E1.1

Answer 1 ANALYSIS of CIRCUITS 2002

The circuit of Figure 1b is a Schmitt Trigger.

If V_B is initially at 12 V, $v_+ = 3^v$ and v_I is positive ($v_I = v_+ - v_-$)
v_I will become negative, and V_B change to -12^v, when V_{IN} increases above 3^v. This occurs at $t = 30$ mS.
Now $v_+ = -3^v$, so v_I will become positive, and V_B changes to $+12^v$, when v_{IN} falls below -3^v. This occurs at $t = 110$ mS.
See waveform sketch for V_B on attached sheet.

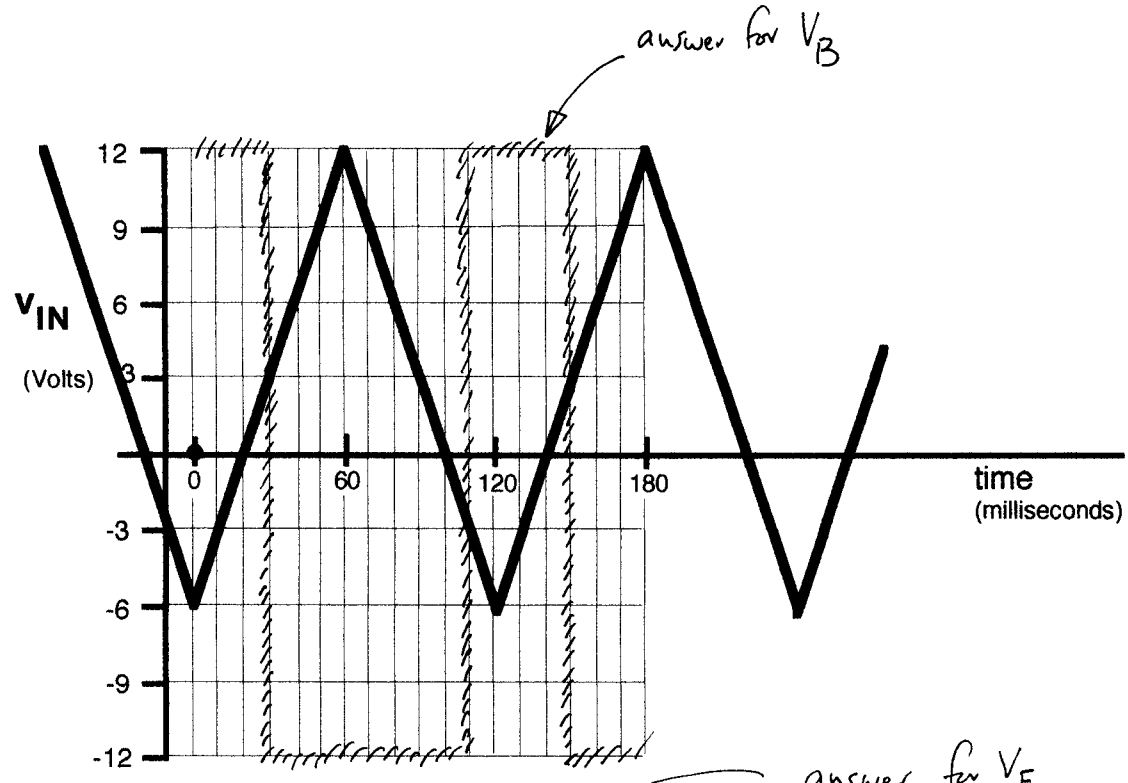
At $t = 30$ mS, application of V_B at -12^v to terminal D causes (assuming a virtual short circuit between the input terminals) a current of $12/120 = 0.1$ mA to flow out of the capacitor until $t = 110$ mS.
The resulting change in capacitor voltage, and hence V_E, can be derived from:

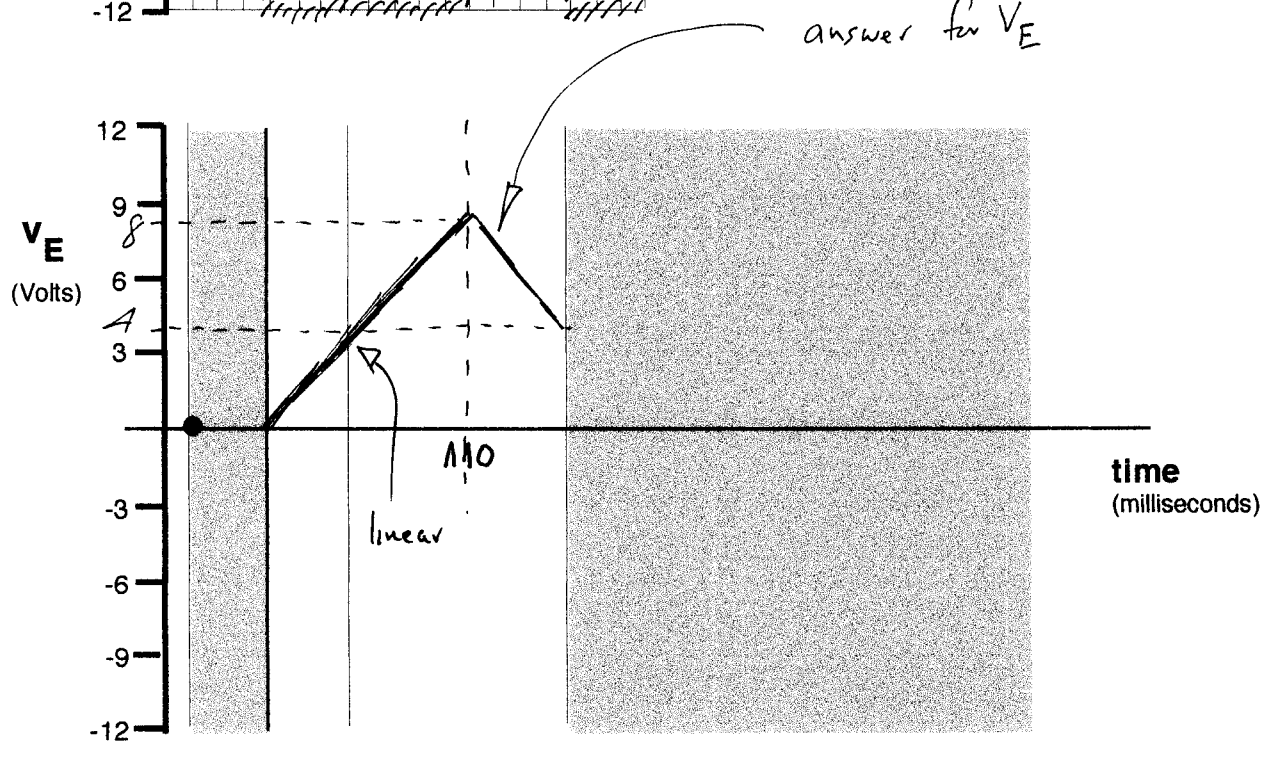
$$i = C \frac{dv_E}{dt}$$

Since $i = 0.1$ mA, $C = 10^{-6}$ F and $dt = 80$ mS, the change in V_E is 8 volts. (see waveform sketch on supplementary sheet)

When V_B changes to $+12^v$ the capacitor charging current has the same magnitude but opposite direction, and remains constant for 40 mS.
The consequent decrease in V_E is therefore 4^v (see waveform sketch)

EE 1.1 exam 2002 Supplementary sheet for question 1. To be tied into answer sheet.





Answer 2

Let V_C be the complex capacitor voltage and V_R the voltage across the right-hand resistor such that $V^* = V_C - V_R$

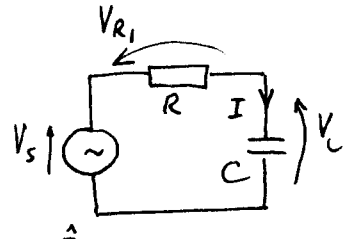
By "potential divider" action,

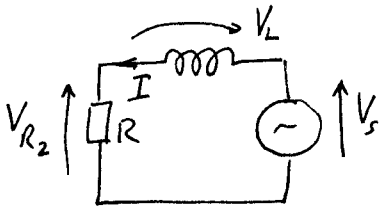
$$V_C = \left[\frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}}\right] V_S \qquad \text{and} \qquad V_R = \left[\frac{R}{R + j\omega L}\right] V_S$$

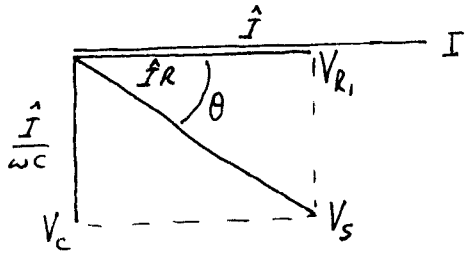
so that $$V^* = V_C - V_R = V_S\left[\frac{1}{1 + j\omega CR} - \frac{R}{R + j\omega L}\right] = \left[\frac{j\omega(L - R^2C)}{R(1 - \omega^2 LC) + j\omega(L + R^2C)}\right] V_S$$

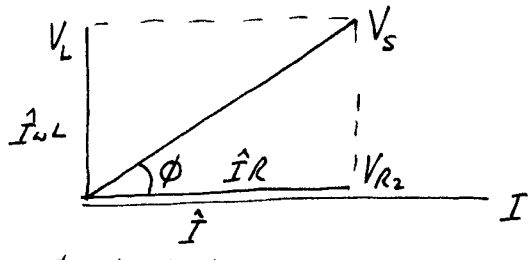
Therefore $\frac{V^*}{V_S}$ is real when $\omega^2 LC = 1$, that is, when $\omega = \frac{1}{\sqrt{LC}}$. When $R = \sqrt{L/C}$, $V^* = 0$

Phasor diagrams



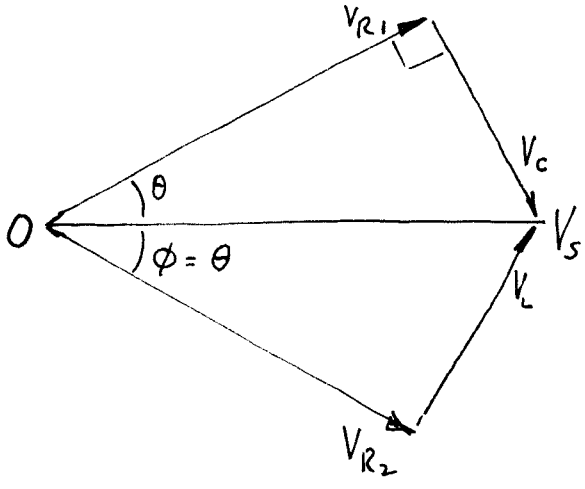




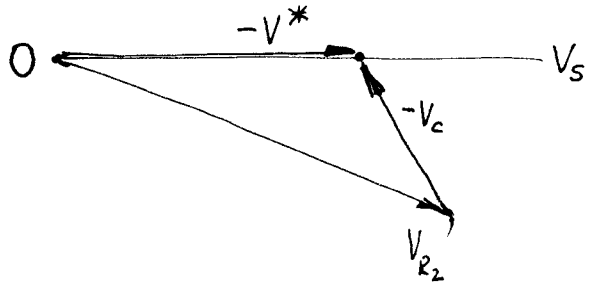


$$\theta = \tan^{-1}\frac{1}{\omega CR} \qquad \phi = \tan^{-1}\frac{\omega L}{R}$$

but since $\omega L = \frac{1}{\omega L}$, $\theta = \phi$ so the combined phasor diagram, in which V_S is common, is as shown below (left).

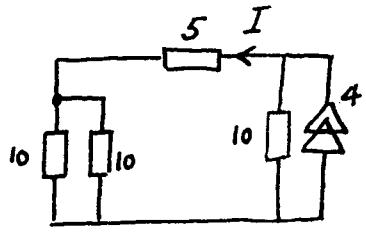


From the diagram on the left we see that $V^* = V_C - V_{R_2}$ is either 0° or 180° out of phase with V_S (see below)



Answer 3

Superposition To find current I due to the 4A source:

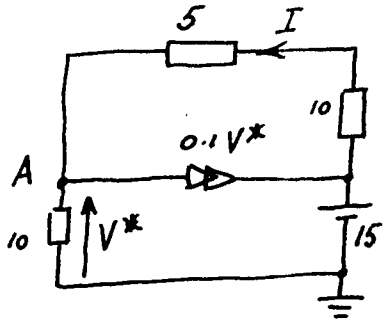


So 4A divides equally between two branches and

$I = 2$ A

because VCCS acts as a 10Ω resistor

To find current I due to 15V source:



Assume reference (earth, as shown) and apply KCL at node A:

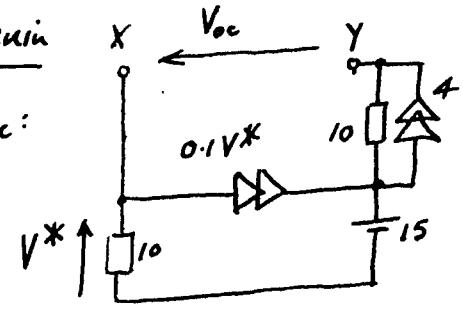
$$\frac{V_A - 15}{15} + 0.1V_A + \frac{V_A}{10} = 0 \quad \text{i.e.,} \quad V_A\left[\frac{1}{15} + \frac{1}{5}\right] = 1 \quad \text{or} \quad V_A = \frac{15}{4}$$

$$\text{So } I = \frac{(15 - 15/4)}{15} = 0.75 \text{ A}$$

By Superposition, $I = 2 + 0.75 = 2.75$ A

By Thevenin

To find V_{oc}:



Voltage across right-hand 10Ω = 40 V

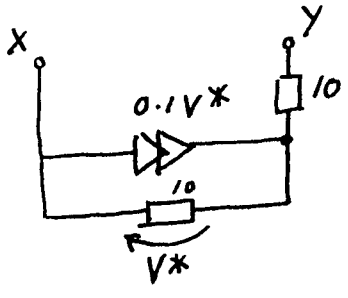
Voltage across voltage source = 15 V

To find voltage (V^*) apply KCL at X

$$\frac{V^*}{10} + 0.1V^* = 0 \quad \text{so} \quad V^* = 0$$

By KVL $V_{oc} = 40 + 15 + 0 = 55$ V

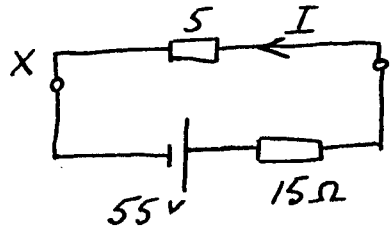
To find R_o set independent sources to zero



Because VCCS is equivalent to 10Ω,

$R_o = 10 + 5 = 15\,\Omega$

Thevenin Equivalent Circuit with 5Ω reconnected:



By Ohms Law,

$$I = \frac{55}{20} = 2.75 \text{ A}$$

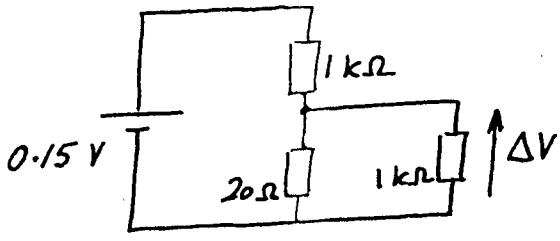
Answer 4

Assume that a current of 1 mA is needed to ensure that the Zener is in the breakdown region.

If the voltage V is 5 volts, the current through the 1 kΩ resistor is 10 mA. If a minimum of 1 mA must flow in the diode, a maximum of 9 mA is available to flow in R. In this case, minimum $R = 5^V/9\,mA = 555\,\Omega$

If the maximum current of 9 mA flows in the diode, 1 mA flows in the load, so that maximum $R = 5^V/1\,mA = 5\,k\Omega$.

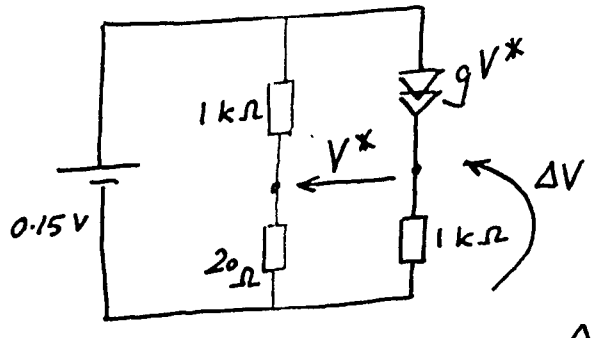
Small-change model of circuit of Figure 4a (for 1% increase in 15 V)



To good approximation,

$$\Delta V = \frac{20}{1020}\,0.15 = 2.94\ mV$$

Small-change model of circuit of Figure 4b (for 1% increase in 15 V)



Voltage across $20\,\Omega = \frac{20}{1020}\,0.15 = 2.94\ mV$

$$V^* = 2.94\ mV - \Delta V \quad \text{——— (1)}$$

$$\Delta V = gV^*R \quad \text{——— (2)}$$

Combine (1) and (2) to eliminate V^*:

$$\frac{\Delta V}{gR} = 2.94\,mV - \Delta V$$

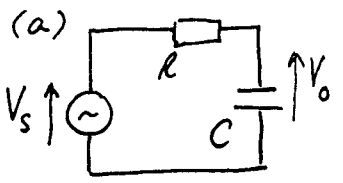
$$\text{so } \Delta V\left[1 + \frac{1}{200.1}\right] = 2.94\ mV \qquad \text{so } \Delta V = 2.93\ mV$$

With regard to the variation in load voltage due to a variation in the supply voltage, the circuit of Figure 4b offers no significant advantage.

The introduction of the transistor allows a variable load current to be taken without significantly changing the Zener diode current. Thus, the maximum load current is not directly limited by the maximum Zener current.

Answer 5

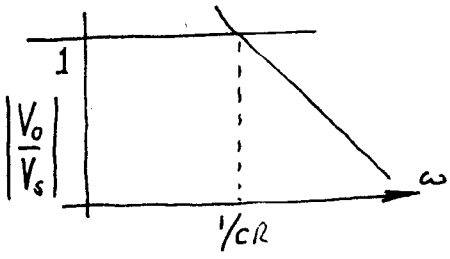
(a)

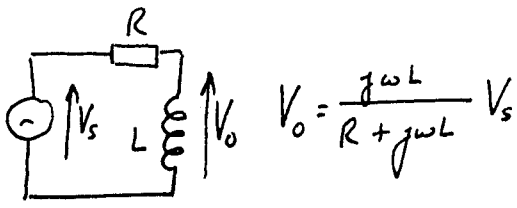


$$V_0 = \left[\frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}}\right] V_s$$

so $$\frac{V_0}{V_s} = \frac{1}{1 + j\omega CR} \qquad \text{——— (1)}$$

Assuming log axes:

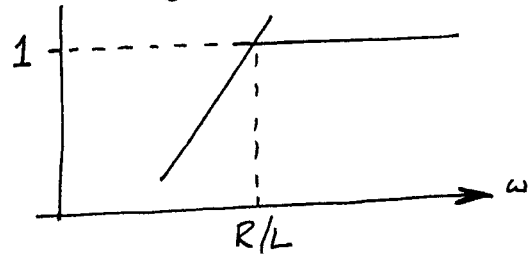




$$V_0 = \frac{j\omega L}{R + j\omega L} V_s$$

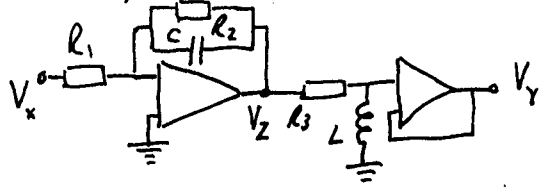
so $$\frac{V_0}{V_s} = \frac{1}{1 - jR/\omega L} \qquad \text{——— (2)}$$

Assuming log axes



(b) For the circuit of figure 5c, see designation of components as shown here:

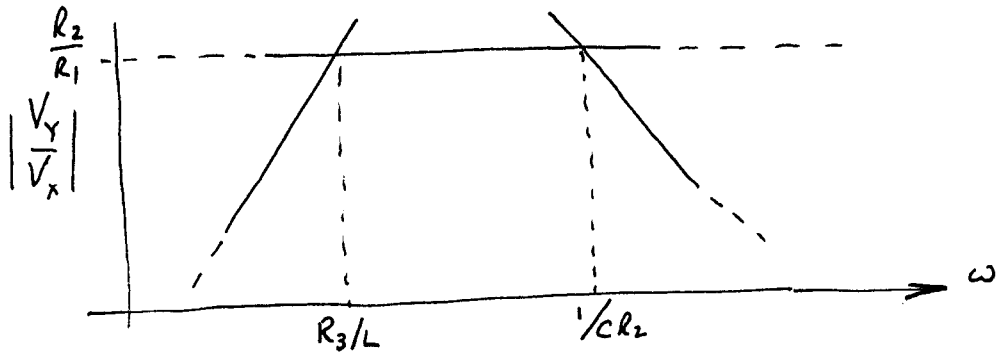
$$\frac{V_Z}{V_X} = -\left[\frac{\frac{1}{1/R_2 + j\omega C}}{R_1}\right] = -\frac{R_2}{R_1}\left[\frac{1}{1 + j\omega CR_2}\right]$$



and, from (2) above

$$\frac{V_Y}{V_Z} = \frac{1}{1 - jR_3/\omega L}$$

The asymptotes of $\left|\frac{V_Y}{V_X}\right| = \left|\frac{V_Y}{V_Z} \times \frac{V_Z}{V_X}\right|$ can be deduced from the asymptotes shown above:



where $R_2/R_1 = \#\ 1$

$$\frac{R_3}{L} = \frac{2 \cdot 10^3}{100 \cdot 10^{-3}} = 2 \times 10^4 \text{ radians per sec}$$

and $$\frac{1}{CR_2} = \frac{1}{1 \cdot 10^{-9} \cdot 10^3} = 10^6 \text{ radians per sec.}$$