A=analysis, D=design, C=calculated solution using taught theory, B=bookwork
NB - marking will be 1 mark for every 2% indicated on question paper (max 50 marks) so marks here are half of marks on question paper.

Solution to Question 1

36 minutes for the question => 9 minutes each part

a)
i) 1074.75
ii) 270F
iii) 112
iv) -1
v) 1023
[1 mark each, except iv & v 1 mark if both right]

[4C]

b)
seee eeee emmm mmmm mmmm mmmm mmmm mmmm

(i) s=0, e=158, m=0 => exp=31, mant=1 => 2^{31}=2147483648 **[2 marks]**
(ii) s=1,e=125,m= 10001....=>exp=2^{-2}, mant=1.001 =>-1.125/4=0.2812 **[2 marks]**

Unsigned exponent => 31 bit unsigned comparison can be used onfloating point, and combine with sign bit **[2 marks]**

[6C/A]

c)

R0=2
R1=4
R2=2-32=-30
R3=6
R4=0

Timing:
0: 0-3
4: 1-4
8: 2-6
C: 4-7

[4A]

d)
(i) -28*x
(ii)
RSB R1, R0, R0 lsl 3; R1 := R0*7
RSB R1, R1, R1 lsl 4; R1 := R1*15
(iii)
floor((2^{31}-1)/105) = 20452225 **(allow approximations)**

[6A/D]

Solution to Question 2

27 minutes for the question

This tests ability to understand low-level operation of ARM assembler instructions

For each part, deduct 1 mark for each column wrong down to minimum of 0 marks, except in allow consequent errors in memory write data. Assume mem[] = mem_{32}[]. Ignore entries in n/a columns

	r0	r1	r2	r3	r4	NZCV	Memory
a)	-2	3	&100 256	1	-3 &FFFFFFFD	1000	mem_{32}[&104] = 3 260
b)	&10B 267	1	&01020304 16909060	1	n/a	n/a	mem_8[&1] = 1
c)	&FC 252	$2^{31}+2^8$ &80000100 2147483904	2^9 &200 512	$2^{10}+1$ &401 1025	&01000000 2^{24} 16777216	0011	Mem_{32}[&100]=&401

[5A+5A+5A]

Solution to Question 3

27 minutes for the question

This questions tests understanding of the operation of different types of direct-mapped caches.

a)

each line has two words

i	tag	index	word sel	type
1	0	0	0	M
2	0	0	1	H
3	0	1	0	M
4	0	1	1	H
5	1	0	0	M

14,18,14,10, c, 8, 4, 0, 4, 8, c
H, M,H, H, M,H, M,H, H,H,H,

[5A]

b)

i	tag	index	word sel	type
1	0	0	0	M
2	0	1	0	M
3	0	2	0	M
4	0	3	0	M
5	1	0	0	M

M,M,H,H,H,M,M,M,H,H,H

[5A]

c)

1 R0,R4
2 none
3 R8, RC
4 none
5 W0,W4, R10,R14
6 none
7 none
8 none
9 W10,W14,R0,R4

[5A]

Solution to Question 4

This question tests whether the student understands the ARM conditional instructions and pipeline, and implications for code timing.

27 minutes for the question

```
TEST
        CMP R1, R0
        CMPEQ R3, R2
        BEQ T1
        RSB R5, R4, #0
        B T2
T1
        MOV R5, R4
T2
```

a)
if (R1=R0) and (R3=R2) then R5 := R4 else R5 := -R4

Either the BEQ branch is executed or the B branch is taken. The taken branch has execution time 4 cycles, all other instructions one cycle.

[4A]

b)

```
TEST
        CMP R1, R0
        CMPEQ R3, R2
        BEQ T1
        RSBNE R5, R4, #0
        MOVEQ R5, R4
```

[4D]

c) F=Fetch, D=Decode, E=execute

1F	1D	1E						
	2F	2D	2E					
		3F	3D	3E				
			4F (aborted)	S	S	4F	4D	4E

[4B]

d)
100MHz * 1/(1+BPL) = 100/(1+0.25*0.4*5)=66.6MHz. Must assume branch latency = pipeline length

[3C]