UNIVERSITY OF LONDON

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 1996

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER 1.6

HARDWARE

Friday, May 17th 1996, 2.00 - 3.30

Answer THREE questions

For admin. only: paper contains
4 questions
2 pages (excluding cover page)

a. A half adder circuit is defined by the following truth table:

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Write down the boolean equation for the truth table, and draw the corresponding circuit.

b. Show how two half adders can be combined to form a full adder, using a minimum of gates.

c. Draw a block diagram to show how full and half adders can be connected up to make a circuit that adds two n-bit registers producing a carry

d. Explain how an eight bit multiplier can be broken down into four four bit multipliers with some additional adding circuitry.

e. Use the idea described in part d to design a two bit multiplier circuit.

2. Flip Flops

a. Using two nand gates draw a circuit for the R-S flip flop. Explain in what respect it is a non deterministic circuit.

b. A D-type latch has inputs D and LATCH and outputs Q and Q'. When LATCH=1 the value of Q follows the value D, but when LATCH=0 the value of Q does not change. Show how a D type latch can be constructed from an R-S flip flop by adding two more nand gates and an invertor.

c. Explain what is meant by an edge triggered circuit, and why edge triggering is preferred to simple latch circuits such as the one you designed in part b.

d. Show how the edge triggered D-type flip flop can be made up from two D type latch circuits and an invertor gate.

e. Draw the finite state machine diagram for the edge triggered D type flip flop.

3. Multiplexers and decoders

a. A two-to-one multiplexer has three inputs named IN1, IN2, and SELECT, and the output is named OUT. Show the two possible 3-input, one-output truth tables for the multiplexer if you know that the inputs have been named according to common practice.

b. With the addition of at most one inverter to the above multiplexer, build three separate two-input one output circuits, each one providing the following logical functions:

(i) AND
(ii) OR
(iii) XOR

c. A one-to-two demultiplexer with enable has two inputs named INPUT and ENABLE, and two outputs named OUT1 and OUT2. Again show the possible two-input, two-output truth tables for this device assuming that the inputs have been named according to common practice.

4. Sequential Circuit Design

A counter is to work in two modes determined by a single bit input as follows:
When the input is 1 the counter outputs states 0, 3, 0, 3, 0, 3, etc.
When the input is 0 the counter outputs 0, 2, 1, 0, 2, 1, 0, etc.

a. Draw the transition diagram of a finite state machine that corresponds to the specification.

b. Compile a state transition table in the following format for an implementation of this circuit using two flip flops:

Input	State(t_n)	State(t_{n+1})	Q1	Q0	D1	D0
0						
0						
0						
0						
1						
1						
1						
1						

c. Draw Karnaugh maps for D0 and D1, determine the minimum form of the state sequencing logic and draw the complete circuit diagram for the counter.

The three parts carry, respectively, 25% 25% 50% of the marks.

End of paper