E1.4 SOLUTIONS

Question 1

a) Since the MOSFET is at pinch-off we know we can use the active mode drain current equation. So, we have $I_D = K(V_{GS} - V_t)^2 = 0.5$ mA. With $K = 2$ mA/V^2 and $V_t = -1.5$ V this gives $V_{GS} = -1.5 \pm 0.5$ V. Taking the positive sign (to ensure n-ch MOSFET above threshold), we find $V_{GS} = -1$ V, and since $V_G = 0$ this implies $V_S = 1$ V. The source resistance can now be obtained as $\mathbf{R_S = V_S/I_D = 2\ k\Omega}$.

The device is at pinch-off so $V_{DS} = V_{GS} - V_t = 0.5$ V. So $V_D = 1.5$ V, and $R_D = (V_{CC} - V_D)/I_D$ gives $\mathbf{R_D = 7\ k\Omega}$. [6]

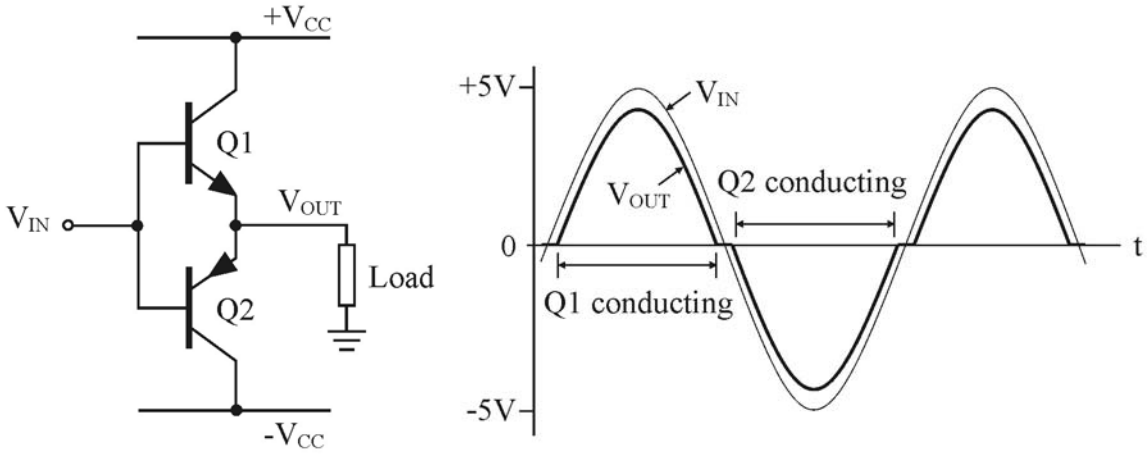
b) According to the resistance reflection rule, the output resistance is given by:

$$R_o = R_S/(1 + \beta) + r_e$$

With $R_S = 10$ kΩ, $r_e = V_T/I_E = 25$ mV/10 mA = 2.5 Ω, and $\beta = 100$, this gives $\mathbf{R_o = 101.5\ \Omega}$.

(NB this is very quick if the student knows reflection rule; otherwise the result will need to be derived by small-signal analysis) [6]

c) Class B push-pull output stage: Output waveform with 10 Vpp input:



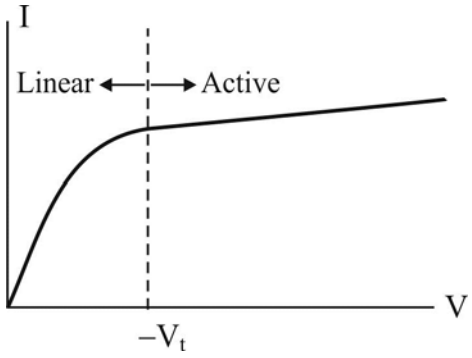
[3 + 3]

When V_{IN} is positive, Q1 conducts and acts as an emitter follower, so the output follows the input but dropped down by $V_{BE} \sim 0.7$ V. Conversely, when V_{IN} is negative, Q2 acts as the emitter follower and the output is raised above the input by $V_{BE} \sim 0.7$ V. However, when the input voltage is near zero, neither transistor conducts and the output goes to zero. This leads to distortion in the output waveform around the zero-crossing points, as shown. [2]

d) Assuming the small-signal approximation is adequate (as suggested by the question), and using the standard result for the small-signal differential gain, we have $V = g_m R_D v_d$, where v_d is the differential input voltage. The quiescent current is 0.5 mA, so $g_m = 2\sqrt{(KI_D)} = 1$ mA/V, and with $v_d = 200$ mV and $R_D = 10$ kΩ we obtain **V = 2 V**.

(NB to use the above method students need to see that the gain result they know from BJT differential amplifiers applies equally well to a MOSFET diff pair. If they don't see this they can still obtain an answer by solving large signal equations, but this will take longer.) [6]

e) The MOSFET has $V_{GS} = 0$, so the I-V curve (with $I = I_D$ and $V = V_{DS}$) is just the output curve at zero gate-source voltage. An n-channel device will be active if $V \geq -V_t$ and linear when $V < -V_t$ (nb reverse inequalities for p-ch device). Sketch for n-channel device is:



[6]

f) Rise time: assuming transistor has been on for a long time, it will be saturated and the output voltage will be $V_{OUT} \sim 0.2$ V. If it switches off at t = 0, the new steady state will be $V_{OUT} = +5$ V. The trajectory of V_{OUT} will therefore be:

$$V_{OUT} = 5 + (0.2 - 5)\exp(-t/\tau)$$

where $\tau = RC = 1$ μs is the time constant.

Putting $V_{OUT} = 0.5$ V, the time to 10% is $t_{10} = \tau\ln(4.8/4.5)$. Similarly, the time to 90% is $t_{90} = \tau\ln(4.8/0.5)$. The rise time is therefore $\mathbf{t_r = t_{90} - t_{10} = \tau ln(4.5/0.5) = 2.2\ \mu s}$.

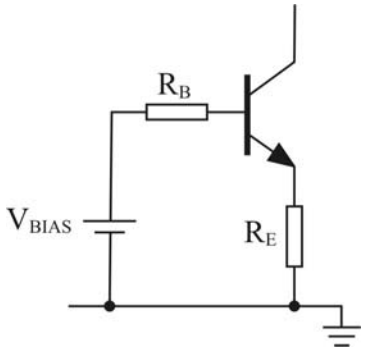
Fall time: assuming the transistor has been off for a long time, the output voltage will be $V_{OUT} = +5$ V. If it switches on at t = 0, it will initially be active with $I_C = 43$ mA assuming $V_{BE} = 0.7$ V. The new steady state (that would be reached if transistor remained active) is $V_{OUT} = 5 - 0.043 \times 1k = -38$ V. The initial trajectory of V_{OUT} will therefore be:

$$V_{OUT} = -38 + (5 - -38)\exp(-t/\tau)$$

The time to 90% is $t_{90} = \tau\ln(43/42.5)$, and the time to 10% is $t_{10} = \tau\ln(43/38.5)$, so the fall time is $\mathbf{t_f = t_{10} - t_{90} = \tau ln(42.5/38.5) = 99\ ns}$, (Linear ramp approximation giving $t_f = 93$ ns also acceptable.) [8]

Question 2

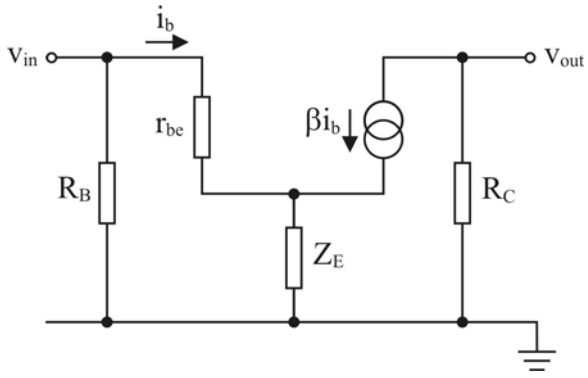
a) Replacing input resistor network by Thévenin equivalent, bias circuit reduces to:



$V_{BIAS} = 10\times33/(33 + 150) = 1.803$ V
$R_B = 33k//150k = 27.0k$
KVL then gives: $I_ER_E + V_{BE} + I_BR_B = V_{BIAS}$
$\Rightarrow\ I_E = (V_{BIAS} - V_{BE})/[R_E + R_B/(1 + b)]$
Assuming $V_{BE} = 0.7$ V,
$I_E = (1.803 - 0.7)/(2.2k + 27k/201) = 0.473$ mA
$I_C = aI_E = 200\times473/201 =$ **0.470 mA**
$V_{OUT} = 10 - 0.47\times10 =$ **5.30 V**

[6 + 2]

b) SSEC:



KVL on input side:

$$i_br_{be} + (1+\beta)i_bZ_E = v_{in}$$

KVL on output side:

$$-\beta i_bR_C = v_{out}$$

$\Rightarrow A_v = v_{out}/v_{in} = -\beta R_C/[r_{be} + (1 + \beta)Z_E]$
Using $r_e = r_{be}/(1 + \beta)$ this reduces to

$$A_v = -\alpha R_C/(r_e + Z_E)$$

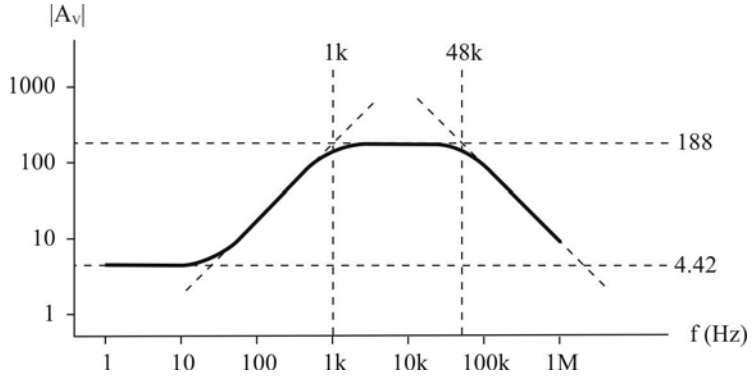
$r_e = V_T/I_E = 25m/0.473m = 52.9\ \Omega$

In mid-band, where $Z_E \to 0$, $A_v = -\alpha R_C/r_e =$ **–188**

At low frequency, where $Z_E \to 2.2\ k\Omega$, $A_v = -\alpha R_C/(r_e + Z_E) =$ **–4.42** [6 (SSEC) + 3 + 3]

c) At low end of mid-band, $Z_E \approx 1/j\omega C_E$ and a HP filter is formed with r_e. The cut-off frequency is therefore given by $\omega_c r_e C_E = 1$ or $f_c = 1/(2\pi r_e C_E)$. With $r_e = 52.9\ \Omega$, for a cut-off at 1 kHz we require $C_E = 1/(2\pi r_e f_c) = 1/(2\pi\times52.9\times1k) =$ **3.0 μF**

Load capacitor C_L and output resistor R_C form a LP filter with cut-off frequency $f_c = 1/(2\pi R_C C_L) = 1/(2\pi\times10k\times330p) =$ **48 kHz**



[4 + 2 + 4]

Question 3

a) The role of the 10 MΩ is to set the operating point by forcing the condition $V_{G1} = V_{OUT}$ at DC. [2]

Both MOSFETs have $V_{GD} \leq 0$ and hence are active if above threshold. The drain current expressions are therefore:

$$I_{D1} = K_1(V_{OUT} - V_{t1})^2 \quad ; \quad I_{D2} = K_2[(V_{DD} - V_{OUT})/2 - V_{t2}]^2$$

No current flows in the 10 MΩ, and if we also neglect the current in the 1 MΩ resistors the drain currents must be equal:

$$K_1(V_{OUT} - V_{t1})^2 = K_2[(V_{DD} - V_{OUT})/2 - V_{t2}]^2$$

Taking the positive square root (to ensure both devices are above threshold) gives:

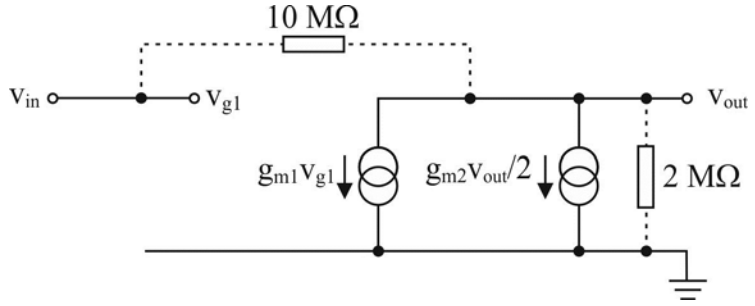
$$2\sqrt{(K_1/K_2)}(V_{OUT} - V_{t1}) = V_{DD} - V_{OUT} - 2V_{t2}$$

from which the required result follows. [6]

With $\sqrt{(K_1/K_2)} = 2$, $V_{DD} = 10$ V and $V_{t1} = V_{t2} = 1$ V, we obtain $\mathbf{V_{OUT} = 12/5 = 2.4\ V}$.

Substituting for V_{OUT} in either of the drain current equations gives $\mathbf{I_{D1} = I_{D2} = 0.784\ mA}$. [4]

b) SSEC (omitting MOSFET output resistances):



[6]

Ignoring the resistors (which are carrying negligible current), KCL at the output gives

$$g_{m1}v_{in} + \tfrac{1}{2}g_{m2}v_{out} = 0$$

from which it follows that $\mathbf{A_v = -2g_{m1}/g_{m2} = -2\sqrt{(K_1/K_2)} = -4}$. [4]

The input current is $i_{in} = (v_{in} - v_{out})/10M = v_{in}(1 - A_v)/10M = 5v_{in}/10M$, so the input resistance is $\mathbf{R_{in} = 2\ M\Omega.}$ [2]

c) In the presence of a signal v_{in}, we can write the total output voltage as $V_{out} = (2.4 - 4v_{in})$, while the total input voltage is $V_{in} = 2.4 + v_{in}$. The condition for Q1 to remain active is therefore: $2.4 - 4v_{in} \geq 2.4 + v_{in} - V_{t1}$

We therefore require $v_{in} \leq V_{t1}/5 = 0.2$ V for Q1 to remain active.

Q2 will remain active provided $(V_{DD} - V_{OUT})/2 > V_{t2}$ or $V_{OUT} < 8$ V. The limiting case would correspond to $v_{in} = -1.4$ V.

So, the constraint on Q1 is the limiting factor, and range of input signal amplitudes over which both transistors will remain active is **from 0 to 0.2 V (0.4 V peak-to-peak).** [6]