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Model Answers and Mark Schemes	First Examiner:		Esther Rodriguez-Villegas
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1.

(a) (theory)

Let's assume two normalised single harmonic signals at two different frequencies :
S1= cos(w1t) and S2= cos(w2t).
Mixing is based on the fact that when those two signals are multiplied two new signals are generated at frequencies w1+w2 and w1-w2. Mathematically this is just the result of applying the trigonometric rule:

$$\cos(A)\cos(B) = \frac{\cos(A+B) + \cos(A-B)}{2}$$

The same could although the same could be extrapolated to more complex signals, applying superposition.

(b) (theory)

If we are trying to select one particular frequency channel from the complete RF spectrum we need a bandpass filter to reject any unwanted frequencies. Generally this filter has to be narrowband, and high Q filters are difficult to design at high frequencies. This problem is compounded if the input signal frequency is variable. A tuneable, high Q bandpass filter with a constant bandwidth is now required. A solution for that is to "mix" the signal with another signal generated by an oscillator. In this way the spectrum of the former is maintained but it is shifted in frequency to facilitate channel selection.

(c) (theory)

The local oscillator (provided it is tunable) to facilitate the design of the filter.

(d) (application of theory)

In a superhet receiver, the design of the prefilter is eased if the IF is high, while the design of the IF bandpass filter is eased if the IF is low. The double conversion superhet receiver avoids this conflict. The first IF is high which ensures that the image frequency is well

separated from the wanted signal. The second IF is low, which enables the design of circuits with sharp selectivity and hence good adjacent channel rejection. Besides, If the second local oscillator can be designed such that it tracks any frequency offsets or drift of the first LO, then the effects of these frequency offsets can be minimised.

The disadvantage is that it is a more complicated design, which involves a penalty in terms of area, power, design time, etc...

(e) (theory)

It is a receiver architecture in which a single local oscillator is used whose frequency is equal to the RF carrier frequency, and thus the IF = 0 Hz. No bandpass filtering is required as the signal is converted directly to baseband. In addition, there is no image signal, thus no image filtering is needed. All signal filtering is at baseband frequencies, and therefore can be performed on-chip. This means that a single-chip receiver is feasible using direct conversion.

The main drawback with direct conversion architectures is their susceptibility to LO 're-radiation' which is picked up by the antenna. After mixing, this leads to dc offsets in the receiver, which will directly corrupt any dc information in the signal.

2.

(a) (application of theory)

The transfer function of that system is:

$$\frac{V_{out}}{V_{in}} = \frac{[k_o + k_2\tau_1]}{[s^2\tau_1\tau_2 + sQ\tau_1 + 1]}$$

Therefore it is a second order lowpass filter

(b) (application of theory)

Three integrators and two amplifiers

(c) (application of theory)

There are many solutions possible for this question. Basically any of the transconductors that appear in the lecture notes with a capacitor connected at the input would be a good answer.

(d) (application of theory)

It is an open question, so many answers are possible. Students are expected to comment on area, power, noise and dynamic range.

(e) (new theory)

From the expression of the transfer function obtained in (a), if $k_0=0$ and $k_2 \rightarrow k_2 s$, the new transfer function would be one corresponding to a bandpass filter:

$$\frac{V_{out}}{V_{in}} = \frac{[k_2\tau_1 s]}{[s^2\tau_1\tau_2 + sQ\tau_1 + 1]}$$

This variable mapping can also be done in the block diagram:

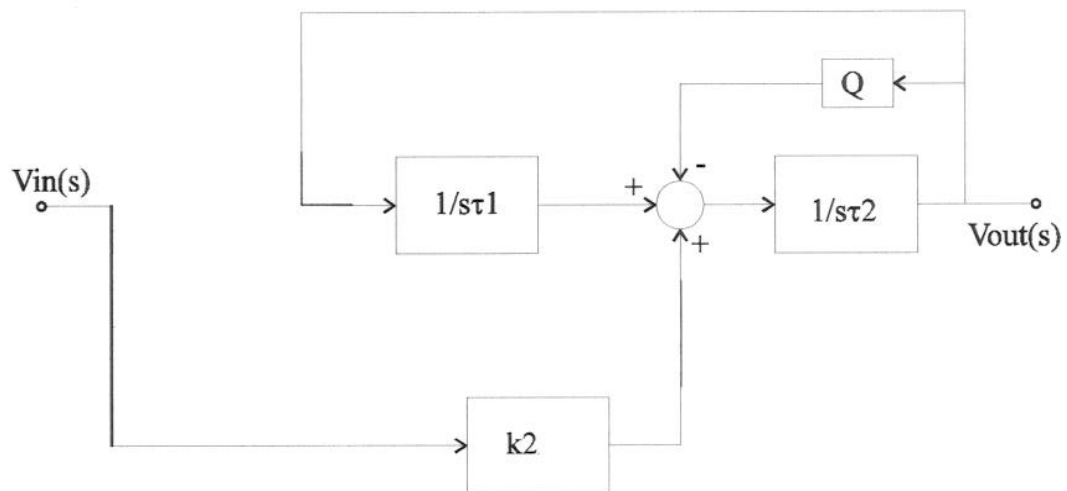| Department of Electrical and Electronic Engineering Examinations 2008 Confidential		
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3.

(a) (new theory)

$$I_{out} = \frac{I_1 - I_2}{2}$$

$$I_1 = \beta\left(\frac{C_i}{C_T}V_{i+} + \frac{C_R}{C_T}V_R - V_T\right)^2$$

$$I_2 = \beta\left(\frac{C_i}{C_T}V_{i-} + \frac{C_R}{C_T}V_R - V_T\right)^2$$

$$I_{out} = \beta\frac{C_i}{C_T}\left(\frac{C_i}{C_T}\frac{(V_{i+} + V_{i-})}{2} + \frac{C_R}{C_T}V_R - V_T\right)(V_{i+} - V_{i-})$$

$$\left(\frac{C_i}{C_T}\frac{(V_{i+} + V_{i-})}{2} + \frac{C_R}{C_T}V_R - V_T\right) = \sqrt{\frac{I_{bias}}{\beta}}$$

$$I_{out} = 0.5\sqrt{\beta I_{bias}}(V_{i+} - V_{i-})$$

(b) (new theory)

$$R_{out} = (g_{ds}^{-1}) = \left(\frac{C_{GD}}{C_T}g_m\right)^{-1} = \left(2\frac{C_{GD}}{C_T}\sqrt{\beta I_{bias}}\right)^{-1}$$

(c) (application of theory)

It is an open question, so more than one answer are possible. The expected one is: adding cascode transistors.

4.

(a) In strong inversion (theory):

Assuming matched transistors in saturation:

$$Vd = Vgs1 - Vgs2 \ = \ \frac{\sqrt{Id1} - \sqrt{Id2}}{\sqrt{\beta}} \qquad\qquad Is = Id1 + Id2$$

Solving these simultaneous equations gives a solution for Id1 and Id2:

$$Id1 = \frac{Is}{2} + \frac{Is}{2}\sqrt{\frac{2\beta Vd^2}{Is} - \frac{\beta^2 Vd^4}{Is^2}} \qquad\qquad Id2 = \frac{Is}{2} - \frac{Is}{2}\sqrt{\frac{2\beta Vd^2}{Is} - \frac{\beta^2 Vd^4}{Is^2}}$$

These expressions are valid if

$$\left(\frac{2\beta Vd^2}{Is} - \frac{\beta^2 Vd^4}{Is^2}\right) \le 1, \ \text{i.e.} \ |Vd| \le \sqrt{Is/\beta}$$

$$Iout = Id1 - Id2$$

$$= \ Is\sqrt{\frac{2\beta Vd^2}{Is} - \frac{\beta^2 Vd^4}{Is^2}} = Vd\sqrt{2\beta Is}\sqrt{1 - \frac{Vd^2\beta}{2Is}}$$

In weak inversion (application of theory):

With identical derivations as for the bipolar differential pair, just substituting Ut by nUt:

$$V_{in} = nU_t\left(\frac{1+X}{1-X}\right) \qquad \text{or} \qquad X = \tanh\left(\frac{V_{in}}{2nU_T}\right)$$

$$I_{out} = I_{d1} - I_{d2} = I_s\tanh\left(\frac{V_{in}}{2nU_t}\right)$$

(b) (application of theory)

Operating at small signal just biasing the differential pair with another MOS transistor and introducing a second input signal through its gate.

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(b) (application of theory)

1-Adding another differential pair in cross coupled configuration

2- Biasing with another differential pair in the bottom

The resulting circuit would be identical to a Gilbert multiplier but with MOS transistors instead on bipolar.

For further improvement, predistorting the signal for the top differential pair and adding resistor degeneration for the bottom.

5.

(a) (theory)

Thermal noise arises because the channel behaves as a resistor. It's the consequence of the thermal fluctuations of carriers. In the strong inversion saturation region:

$$ind^2 = \frac{8kTgm\Delta f}{3}\ A^2$$

Flicker noise is essentially a low-frequency phenomenon exhibited by almost all electronic devices, but its nature is still not properly understood. Flicker noise is associated with a flow of dc current, and in many cases is due to surface traps capturing and releasing electrons in a random fashion.

$$vng^2 = \frac{k_f\Delta f}{CoxWLf}\ V^2$$

Shot noise, which is associated with current flow across a potential barrier such as a p-n junction. In the MOS transistor can occur if there is current leakage at the gate.

$$ing^2 = 2qIg\Delta f\ A^2$$

(b) (theory)
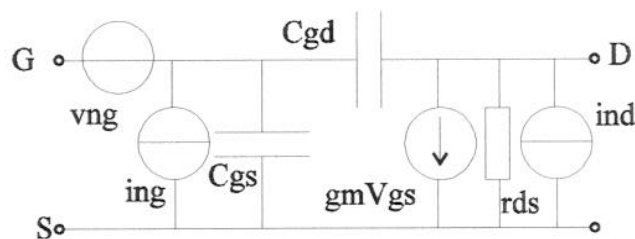
Referring all the noise sources to the input:

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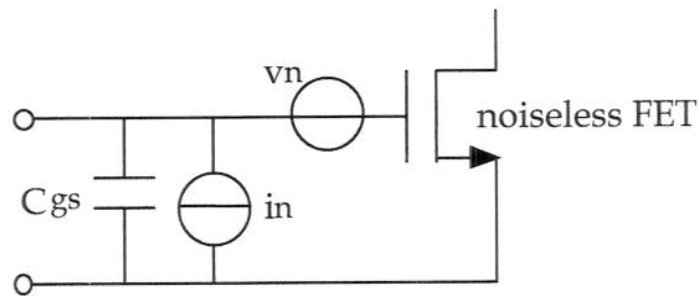
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$$vn^2 = \frac{ind^2}{gm^2} + vng^2 = \frac{8kT}{3gm} + \frac{k_f}{WLCox\, f}\ V^2$$

$$in^2 = ing^2 = 2qIg\Delta f\ A^2$$

(c) (new theory)

$$v_n^2 = \left(\frac{8kT}{3g_m} + \frac{k_f}{WLC_{ox}f}\right)\left(\frac{C_T}{C_i}\right)^2$$

where $C_T \approx \sum_{i=1}^{N} C_i$

(c) (new theory and computed example)

• Considering the first stage alone:

$$F1 = \frac{veq1^2}{vns^2}$$

Thus the equivalent input noise voltage $veq1^2 = F1vns^2$
This equivalent input noise $veq1^2$ consists of the received (source) input noise, plus internal noise $vn1^2$ contributed by the first stage:

$$veq1^2 = vns^2 + vn1^2$$

$$vn1^2 = veq^2 - vns^2 = (F1-1) vns^2$$

• Considering the second stage alone, $vn2^2 = (F2-1)vns^2$

The total power of noise will then be:

$$vnt^2 = \prod_{i=1}^{N} Gi \cdot vns^2 + \prod_{i=1}^{N} Gi \cdot vn1^2 + \prod_{i=2}^{N} Gi \cdot vn2^2 + \ldots + GN \cdot vnN^2 =$$

$$= \prod_{i=1}^{N} Gi \cdot vns^2 + \prod_{i=1}^{N} Gi \cdot (F1-1) \cdot vns^2 + \prod_{i=2}^{N} Gi \cdot (F2-1) \cdot vns^2 + \ldots + GN \cdot (FN-1) \cdot vnN^2$$

$$F = \frac{vnt^2}{\displaystyle\prod_{i=1}^{N} Gi \cdot vns^2} = F1 + \frac{(F1-1)}{G1} + \ldots + \frac{(FN-1)}{\displaystyle\prod_{i=1}^{N} Gi}$$

Applying this equation, the noise factor for that system is 8.35.

6.

(a) (new theory)

$$I = I_s \exp\left(\sum_{i=1}^{N} \frac{C_i}{C_T} \frac{V_i}{nU_T} \right)$$

(b) (new theory)

The current in the input transistors is given by:

$$I_{1,2} = I_s \exp\left(\frac{0.5 V_{i+/-} + 0.5 V_R}{nU_T} \right)$$

And in the common mode sensing branch:

$$I_3 = I_{bias} = I_s \exp\left(\frac{\dfrac{0.5(V_{i+} + V_{i-})}{2} + 0.5 V_R}{nU_T} \right)$$

Resulting in an output current:

$$I_{out} = I_{bias} \sinh\left(\frac{0.5 V_{in}}{2nU_T} \right)$$

(c) (new theory)

MOS could be considered a special case of FGMOS when $\dfrac{C_i}{C_T} = 1$.

$$I_{out} = I_{bias} \sinh\left(\frac{V_{in}}{2nU_T} \right)$$

(d) (new theory)

$$I_{out} = I_{bias}\left[\left(\left(\frac{C_i/C_T}{2nU_T} \right) V_{in} + \frac{1}{3} \left(\frac{C_i/C_T}{2nU_T} \right)^3 V_{in}^3 + \delta(V_{in}) \right) \right]$$

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In a FGMOS transistor C_i/C_T is <1, and this reduces the third order harmonic.

(e) (new theory)

Just adding an extra capacitive input to each input FGMOS transistor.