

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE  
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING  
EXAMINATIONS 2000

EEE PART II: M.Eng., B.Eng. and ACGI

**ANALOGUE ELECTRONICS II**

Tuesday, 6 June 2000, 2:00 pm

There are FIVE questions on this paper.

Answer THREE questions.

All questions carry equal marks.

Time allowed: 2:00 hours

**Corrected Copy**

*corrected*  
*Q5*

Examiners: Prof C. Toumazou, Dr C. Papavassiliou

1. The approximate large signal model of the MOSFET can be represented by

$$I_D = (KW/L)[(V_{GS} - V_T) - (V_{DS}/2)]V_{DS}(1 + \lambda V_{DS}).$$

Under what operating conditions does the MOSFET exhibit a square-law between  $I_D$  and  $V_{GS}$ ? Derive this square law relationship from the above expression.

*Figure 1* shows a single-stage inverting CMOS voltage amplifier. Sketch a typical large signal voltage gain transfer characteristic of the amplifier. Identify clearly on your curve the particular operating mode of each transistor when  $V_{in}$  is increased from 0V to  $V_{DD}$ . In particular identify the region and operating conditions for the highest, linear voltage gain of the amplifier.

Assuming operation in the linear high gain region, calculate the voltage gain of the amplifier of *Figure 1* given that  $V_{bias}$  is 2 volts.

The CMOS process has the following parameters:

NMOS

$$K_N = 20 \mu A/V^2$$

$$\lambda_N = 0.01$$

$$V_{T_N} = 2V$$

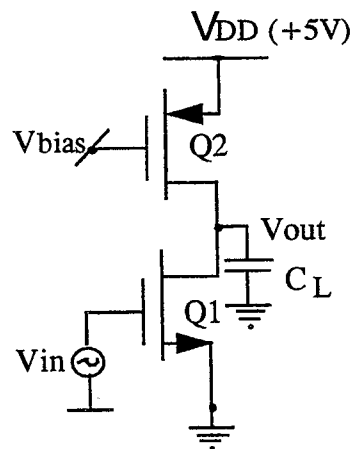
PMOS

$$K_p = 10 \mu A/V^2$$

$$\lambda_p = 0.02$$

$$V_{T_p} = -2V$$

Assume the process has a fixed transistor length  $L = 10 \mu m$  and that the width of the NMOS transistor is  $W_1 = 40 \mu m$ , and for the PMOS transistor  $W_2 = 20 \mu m$ . You may also assume that the DC value of  $V_{in}$  is appropriate for correctly biasing the amplifier.



*Figure 1*

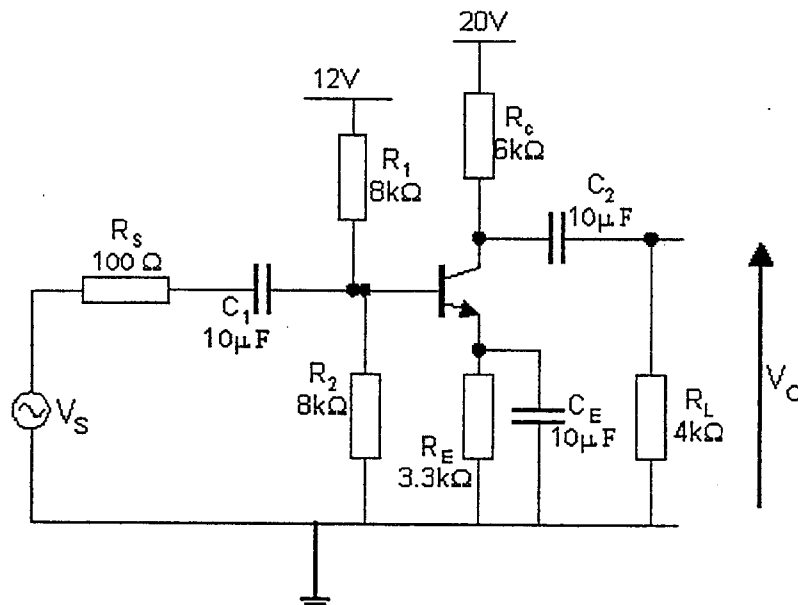
2. The circuit of *Figure 2(a)* is a typical common-emitter amplifier. Sketch and label the small signal high frequency hybrid  $\Pi$  model of the amplifier. Apply Miller's theorem to derive approximate expressions for the amplifier's small signal voltage gain and input -3dB bandwidth. Clearly state any assumptions you make. Assume all a.c. coupling capacitors are short-circuits at the frequency of interest.

Transistor data:

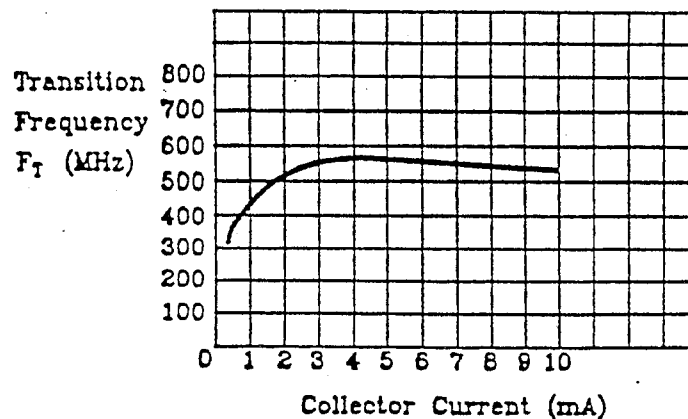
$$\beta = 100 \quad E_a = 100 \text{ V} \quad r_{b'b} = 50 \Omega \quad C_{b'c} = 2 \text{ pF}$$

where  $\beta$  is the current gain (also known as  $h_{fe}$ ),  $E_a$  is the Early voltage,  $r_{b'b}$  is the base spreading resistance and  $C_{b'c}$  is the reverse-biased collector-base junction capacitance.

A graph of transition frequency  $F_T$  versus collector current for the transistor is shown in *Figure 2(b)*. You may assume that the thermal voltage  $V_T$  of the transistor is 26 mV, and  $V_{BE} = 0.6 \text{ V}$ .



*Figure 2 (a)*



*Figure 2(b)*

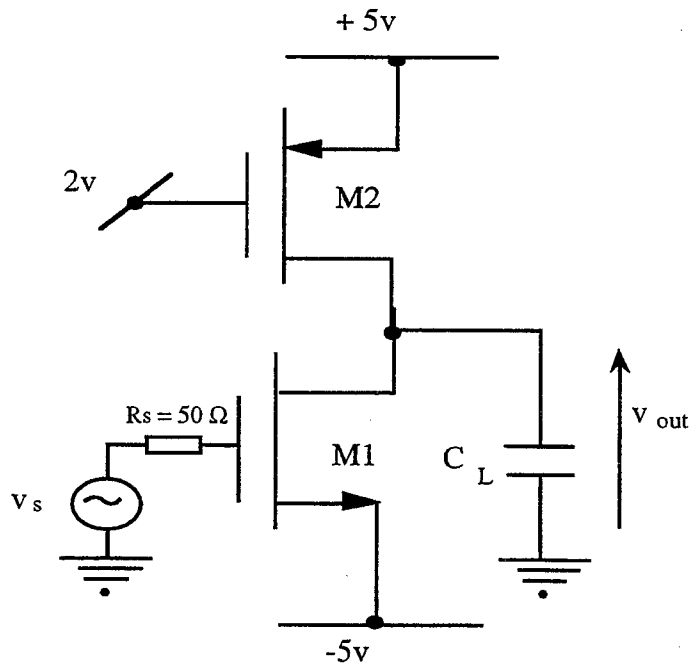
3. *Figure 3(a)* shows a single-stage inverting CMOS voltage amplifier, and *Figure 3(b)* is a corresponding high frequency small signal macromodel of the amplifier.

The CMOS process has the following parameters:

NMOS	PMOS
$K_N = 20 \mu\text{A}/\text{V}^2$	$K_P = 10 \mu\text{A}/\text{V}^2$
$\lambda_N = 0.01$	$\lambda_P = 0.02$
$V_{T_N} = +2\text{V}$	$V_{T_P} = -2\text{V}$
$C_{gd_N} = 0.02 \text{ pF}$	$C_{gd_P} = 0.02 \text{ pF}$
$C_{bd_N} = 0.05 \text{ pF}$	$C_{bd_P} = 0.01 \text{ pF}$

Assume the process has a fixed transistor length  $L = 10 \mu\text{m}$  and that the width for the NMOS transistor is  $W_1 = 50 \mu\text{m}$ , and for the PMOS transistor  $W_2 = 100 \mu\text{m}$ . You may also assume that the d.c. value of  $V_{in}$  is appropriate for correctly biasing transistor  $M_1$ .

By inspection of the amplifier of *Figure 3(a)* calculate values of all the small signal parameters shown in the macromodel of *Figure 3(b)*, and then use the model to calculate the small signal bandwidth of the amplifier. Assume an Oxide Capacitance  $C_{OX} = 3.5 \times 10^{-4} \text{ pF}/\mu\text{m}^2$  and an amplifier load capacitance  $C_L = 0.05 \text{ pF}$ . Assume also that the amplifier approximates a single dominant pole response up to its unity-gain frequency.



*Figure 3(a)*

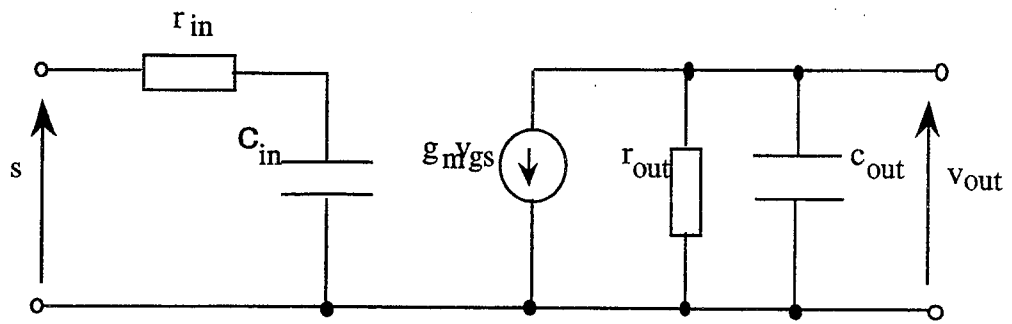
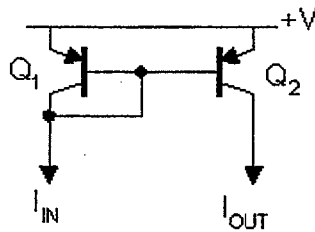


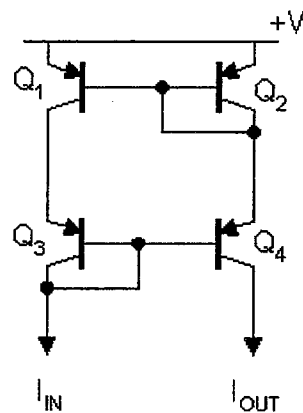
Figure 3(b)

4. *Figure 4* shows two bipolar current-mirrors. Briefly explain the operation of each current-mirror, identifying all sources of error contributing to current transfer inaccuracy.

Assuming identical transistor current gain  $\beta$  for each device, prove that the finite beta error for the current-mirror of *Figure 4(b)* is approximately  $2/\beta^2$  and qualitatively explain how the action of negative feedback increases the output resistance of this current-mirror compared with the current-mirror of *Figure 4(a)*.



*Figure 4(a)*



*Figure 4(b)*

5. Briefly explain what is meant by the following terms when used in analogue circuit design : -

bootstrapping  
cascoding  
phase-margin

Figure 5 shows a single-stage inverting CMOS voltage amplifier. Using simplified models for each FET prove that the output conductance,  $g_{out}$ , of the amplifier operating in saturation is given by

$$g_{out} = [(g_{o1} g_{o2}/g_{m2}) + g_{o3}]$$

stating clearly any assumptions you make.

Calculate the maximum positive and negative output swing of the amplifier. Finally, what is meant by the body effect in CMOS circuits ?

$V_T$  not specified  
Verbal correction  
at  $\approx 3:30$  pm

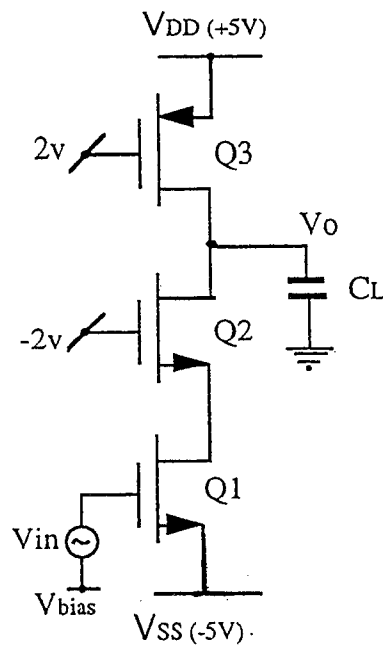
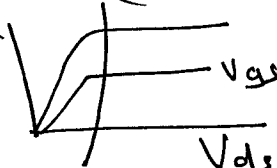
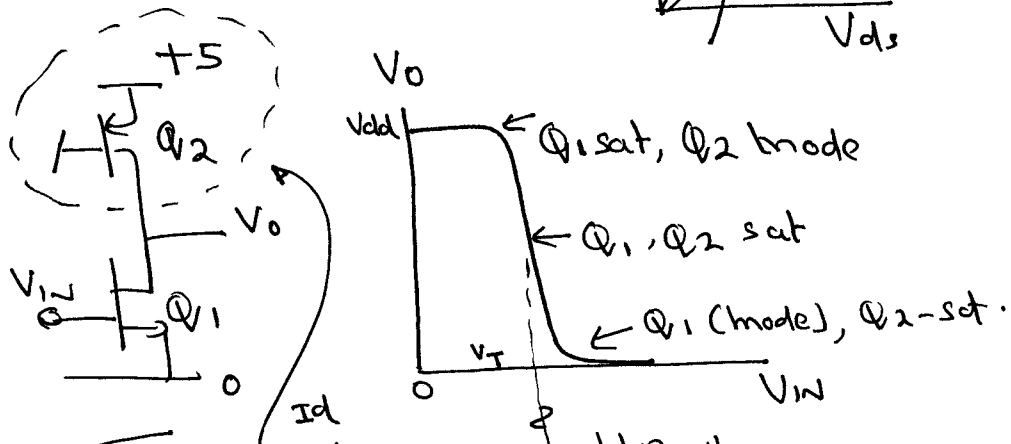


Figure 5

Q1/ Condition for square-law is  $(V_{GS} - V_T)$  curve.

4  $V_{DS} \geq (V_{GS} - V_T)$   $I_d = \frac{k_w}{L} \cdot (V_{GS} - V_T)^2$

6 Load Characteristic  $I_d$   $V_{GS}$   $V_{DS}$  Highest linear gain region. Region for maximum small signal gain.

To calculate voltage Gain  $\Rightarrow$

3  $V_{GS2} = -3V$ ,  $V_T = |a| \Rightarrow I_d = \beta = \frac{k_w}{2L} = 4 \times 10^{-5} A$

$$A = -g_m R_{out} = -g_m / (g_{o1} + g_{o2})$$

4  $= -2\sqrt{\beta I_d} / I_d (\lambda_1 + \lambda_2)$

$$g_{m1} = 4 \times 10^{-4} S$$

$$\therefore A = 4 \times 10^{-4} / (4 \times 10^{-5}) (0.03)$$

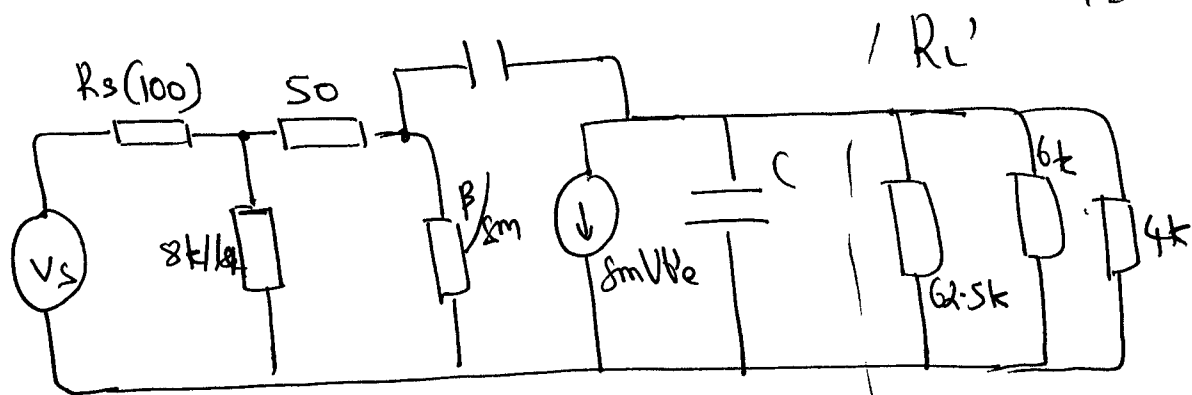
3  $A = -66.66 \times 2 \approx -133$



Q2

 $\frac{I}{12}$ 

4



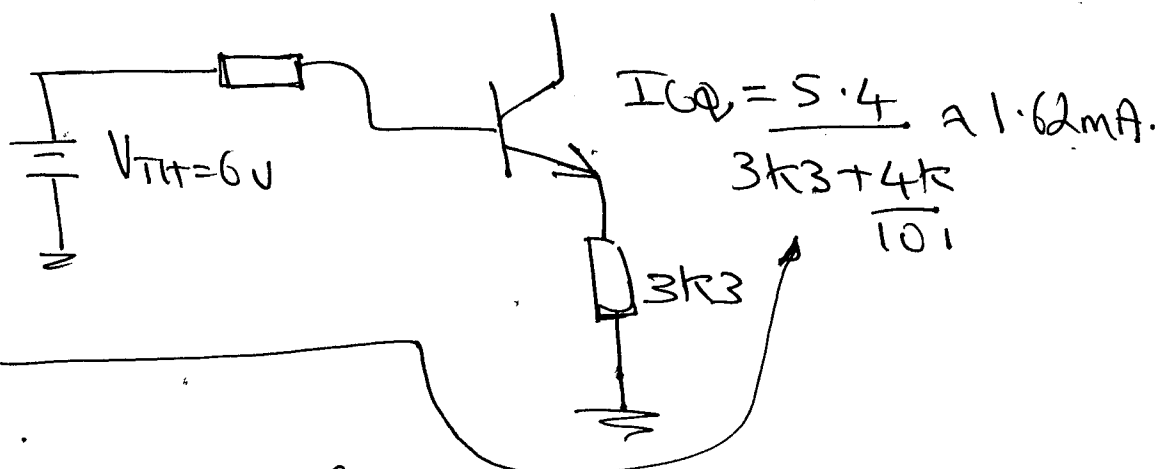
Midband voltage gain

$$V_o/V_s = (V_o/V_{be})(V_{be}/V_s)$$

$$V_o/V_{be} \approx A_m = -g_m R_{L'}$$

To calculate  $I_{CQ}$  from biasing

3



$$\therefore g_m = \frac{1.6}{26}, \quad r_{ce} = \left( \frac{100}{1.6} \right) k$$

$$A_m = \frac{-1.6}{26} \times (62.5 // 6 // 4) k$$

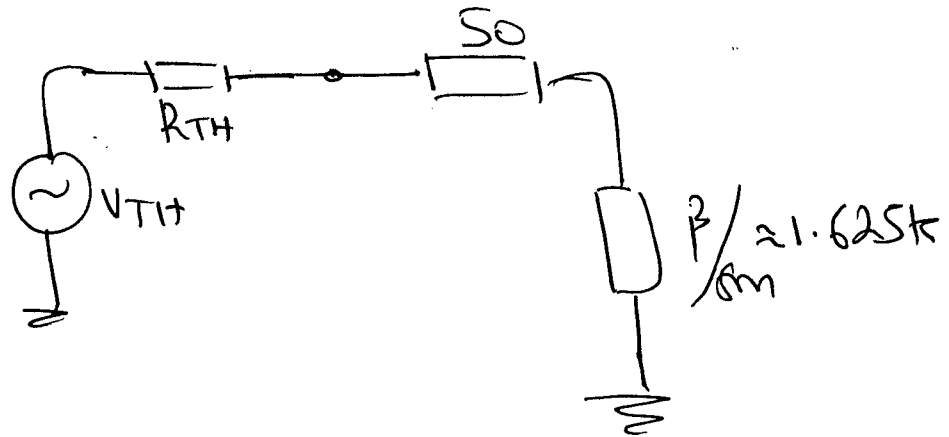
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$A_{m\pm} = -147 \leftarrow$  used to Miller multiply  $C_b'c$  to input and Output.

Q2 (cont)

4/12

Input attenuation



$$V_{TH} = \frac{8k // 8k}{100 + 8k // 8k} \approx 0.975V_s$$

$$R_{TH} = 100 // 4k \approx 97.5k$$

$$\frac{V_{b'e}}{V_{TH}} = \frac{1.625k}{1.625k + 50 + 97.5} \approx 0.916$$

Since  $V_{TH} = 0.975V_s$

$$\frac{V_{b'e}}{V_s} = 0.894 \Rightarrow \frac{V_o}{V_s} \approx -147 \times 0.894$$

②

$$A = -131.5$$

Input -3dB bandwidth  $f_{-3dB} = \frac{1}{2\pi R_{in} C_{in}}$

To calculate  $C_{in}$  require  $C_{b'e}$   
from data sheet spec

$$I_C @ 1.62mA \Rightarrow f_T = 500MHz$$

Q2 cont

$\frac{5}{12}$

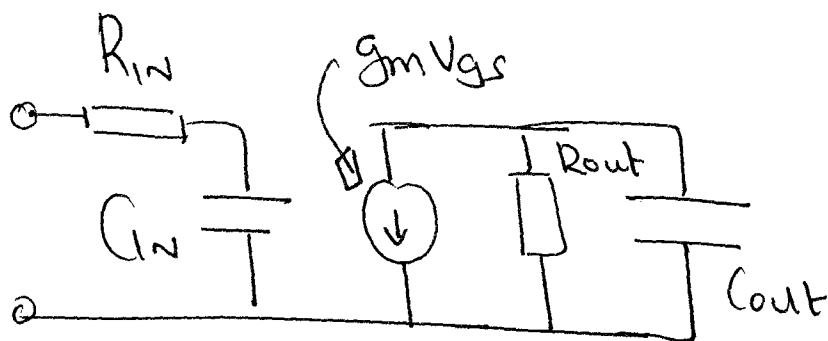
(3) Since  $f_T = \frac{g_m}{2\pi(C_{b'e} + C_{b'c})} \Rightarrow C_{b'e} = 17.6 \text{ pF}$ .

$\therefore C_{in} = [17.6 + (1 + A_m)2] \text{ pF} = 313.6 \text{ pF}$

(3)  $R_i = ((R_{TH} + 50) // 1.625) \text{ k} \approx 135.2 \text{ k}$

$f_{-3dB} = 3.75 \text{ kHz}$

20



Bias current  $I_D = \beta (V_{SS1} - V_T)^2$

$|V_{SS1}| = 3V$ ,  $|V_T| = 2V \Rightarrow I_D = \beta = \frac{k_n}{2L} = 5 \times 10^{-5} A$

$\Gamma_{in} = R_S = 50$ ,  $C_{in} = [C_{gs} + C_{gd1}(1+A)]$

$C_{gs} = \frac{2}{3}WL C_{ox} = \frac{2}{3} [500 \times 10^{-12}] 3.5 \times 10^{-4} \times 10^{-12}$   
 $= 0.12 pF$

$A = -g_m R_{out} = -g_m / (g_{o1} + g_{o2})$   
 $= 2 \sqrt{\beta I_D} / I_D (1 + \lambda V + \lambda_P)$

$\Rightarrow \boxed{g_{m1} = 1 \times 10^{-4}}$

$\therefore A = 1 \times 10^{-4} / (5 \times 10^{-5}) \times 0.03$   
 $= -66.66$

$C_{in} = 0.12 pF + (66.66 \times 0.02) pF$   
 $\approx 1.353 pF$

$R_{out} = 1 / (5 \times 10^{-5} \times 0.03) = 666 k\Omega$

$C_{out} = C_L + C_{db1} + C_{db2} + C_{gd2} + (1 + 1/A) C_{ds1}$   
 $= 0.05 + 0.05 + 0.01 + 0.02 + (1 + 1/6666) 0.02$   
 $\approx 0.15 pF$

f-3dB smaller of

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$f_{p2}$  or  $f_{p1}$

$$f_{p1} = \frac{1}{2\pi R S C_{in}} = 2.35 \text{ GHz}$$

③ —  $f_{p2} = \frac{1}{2\pi R_{out} C_{out}} = \boxed{1.59 \text{ MHz}}$  — ~~xx.~~

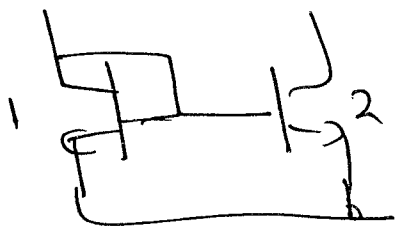
TOTAL

$$\frac{20}{20}$$

Qn 4

## Simple Widlar Mirror

12



$$\frac{I_O}{I_{IN}} = 1 \pm \frac{\Delta V_{be}}{V_T} - \frac{2}{\beta} + \frac{\Delta V_{ce}}{E_a}$$

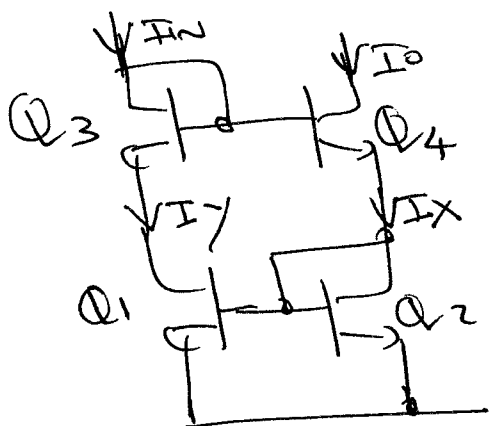
$\sigma_1$  = finite beta error due to base current of  $Q_1$  and  $Q_2$

$\sigma_2$  =  $\Delta V_{be}$  error due to processing mismatches between two transistors

$\sigma_3$  =  $\Delta V_{ce}$  error due to Early Voltage and different operating  $V_{ces}$ .

5

## Improved Widlar Mirror



$\sigma_2$  - same as Widlar.

$\sigma_3$  = reduced to negative feedback.

$\sigma_1$  = reduced through negative feedback.

$Q_4$  forms a negative feedback loop around  $Q_1$  and  $Q_2$  and reduces the finite beta error

Consider first the mechanism for increasing  $R_{out}$ .

Assume collector voltage of  $Q_4$  increases slightly causing  $I_{out}$  to increase due to finite Early voltage of  $Q_4$ . If  $I_{out}$  increases  $E_{2,3}$

5

collector current of  $Q_2$  increases, causing  $V_{be1}$  and  $V_{be2}$  to increase (feedback).

Since  $I_{in}$  is assumed constant then as  $I_{C1}$  increases  $I_{B1}$  must reduce,  $V_{be1}$  reduces,  $I_{C1}$  and hence  $I_{B2}$  reduces (counting the initial increase). Net result is a constant current source.

5

To estimate the reduction in finite beta error,

$$I_X = \left( \frac{\beta+1}{\beta} \right) I_0, \quad I_Y = \left( \frac{\beta}{\beta+2} \right) I_X = \left( \frac{\beta+1}{\beta+2} \right) I_0$$

$$I_{in} = I_Y + \frac{I_0}{\beta} = I_0 \left[ \frac{\beta+1}{\beta+2} + \frac{1}{\beta} \right]$$

$$= I_0 \left[ \frac{\beta(\beta+1) + \beta+2}{\beta(\beta+2)} \right] = I_0 \left[ \frac{\beta^2 + 2\beta + 2}{\beta^2 + 2\beta} \right]$$

$$\approx \boxed{1 - 2/\beta^2}$$

5

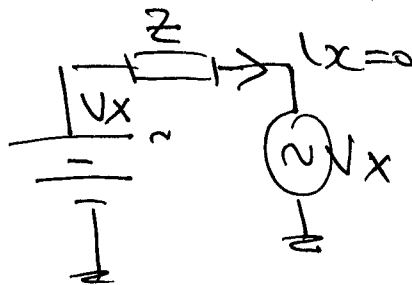
Finite beta error has reduced by a factor of  $\beta^2$ .

Q5

## Boostrapping

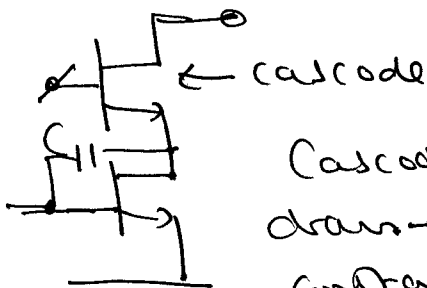
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The term coined for the situation when the two sides of an impedance/admittance are held at the same potential (a.c) so that potential across impedance  $\approx 0$ . Simulates high impedance. As one side moves up by  $\Delta V$  the other side follows hence term bootstrapping.



3

## Cascoding



Cascoding ensures collector-emitter / drain-source voltage almost constant when variations in output swing

$\therefore$  output current stays virtually constant ensuring high output resistance. Also since voltage variation across  $C$  is minimized,  $C$  can charge up a lot faster hence  $dv/dt$  increased and so dominant time constant is reduced. With FET another dominant pole is at the output so the phase margin is improved. With a BJT the dominant pole is at the input, gain-bandwidth product broken since gain of another set by load and transconductance gain.

3

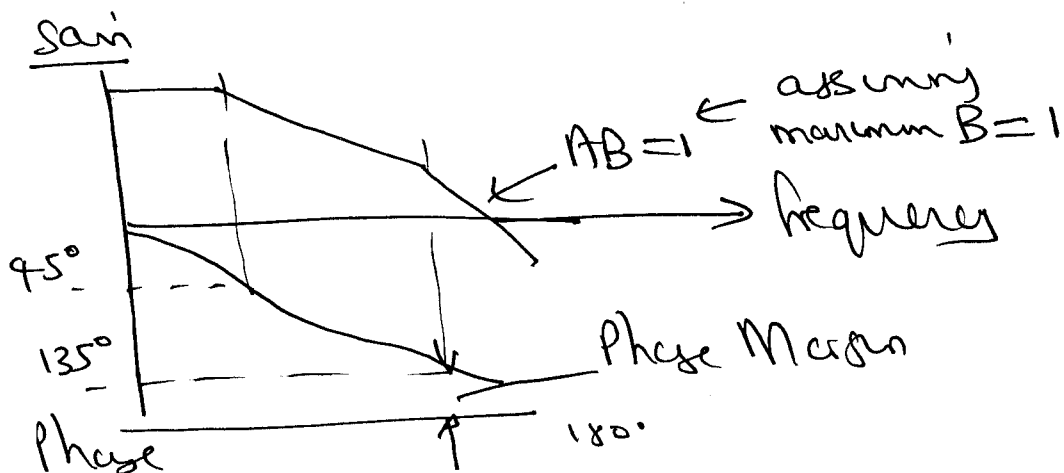


Ans cont

## Phase Margin

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Margin of Safety. Phase difference between phase shift at frequency which causes the loop-gain of the system to be unity at 180 degrees. eg

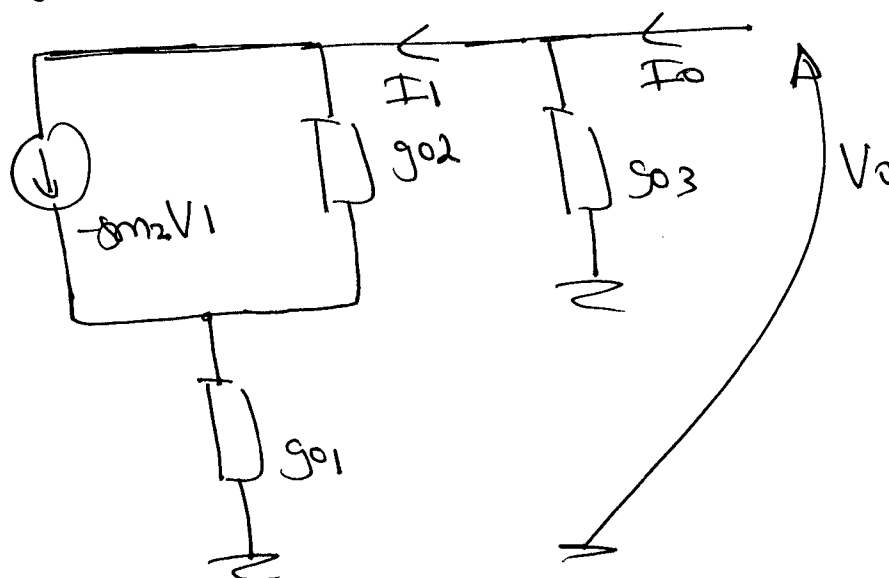


$$\left( \frac{A}{1+AB} \right) \Rightarrow |BA|=1 \quad \angle(AB)=180^\circ$$

Oscillator

③

Equivalent circuit for figure 5



④

$$g_{out} = I_1/V_O + I_2/V_O = I_1/V_O + g_{O3}$$

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Q.5  
cont.

Equations

12  
12

$$I_1 = -g_{m2} V_1 + (V_0 - V_1) g_{o2}$$

$$I_1 = -g_{m2} V_1 + (V_0 g_{o2}) - g_{o2} V_1$$

$$\therefore I_1 \left[ 1 + \left( \frac{g_{m2} + g_{o2}}{g_{o1}} \right) \right] = V_0 g_{o2}$$

Assuming  $g_{m2} \gg g_{o2}$  and  $g_{m1} / g_{o2} \gg 1$

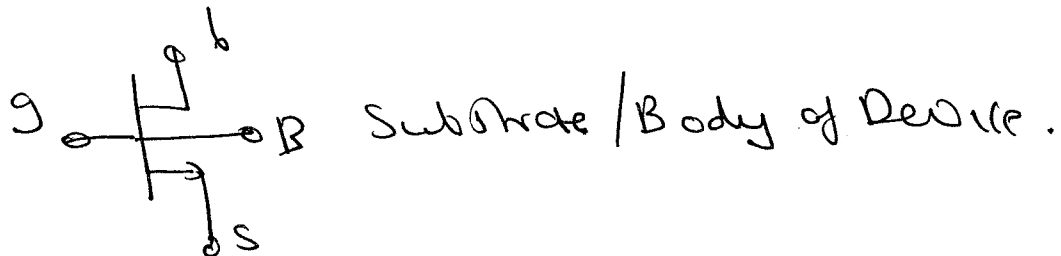
$$\text{Then } I_1 \left( \frac{g_{m2}}{g_{o1}} \right) = V_0 g_{o2}$$

$$\text{OR } \frac{V_0}{I_0} = \frac{g_{m2}}{g_{o2} g_{o1}} \Rightarrow \boxed{g_{out} = \frac{g_{o1} g_{o2}}{g_{m2}} + g_{o3}}$$

④

### Body Effect

The MOSFET is a 4-terminal device



Parasitic junctions (PN) exist between Body and Channel. Substrate should be connected to more negative potential than source.

$V_{BS}$  voltage is generated in  $V_T$  and is referred to as the Body Effect.

$$V_T = V_{T0} + \gamma \left[ \sqrt{V_{BS} + 2\phi_F} - \sqrt{2\phi_F} \right]$$

③

no. 2/20

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E2.2