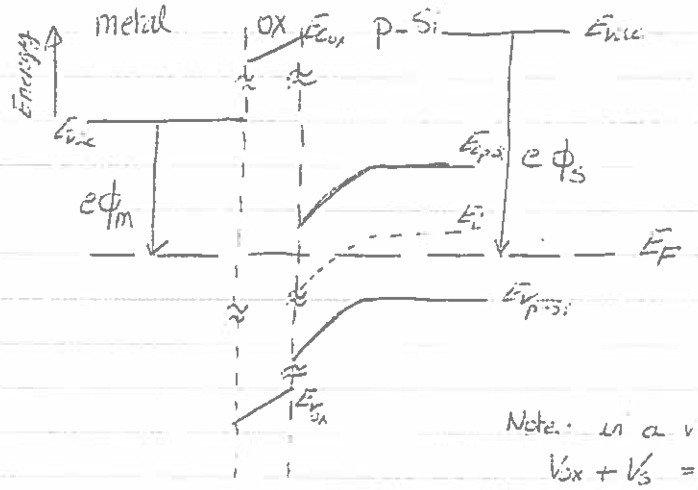
EE3-11

Q1

a)



[5]

Note: in a very good sketch $V_{ox} + V_s = e(\phi_s - \phi_m)$

b) i) $V_s = \phi_F$ onset of depletion [1]

$\Rightarrow \quad n_s = N_A \exp\left(-\frac{\phi_F}{V_T}\right) \qquad (1)$

$n = N_c \exp\left(-\frac{(E_c - E_F)}{kT}\right)$ [2]

$n_i = N_c \exp\left(-\frac{(E_c - E_i)}{kT}\right)$

$\Rightarrow \quad \frac{n}{n_i} = \exp\left(\frac{-E_c + E_F + E_c - E_i}{kT}\right)$

$n = n_i \exp\left(\frac{E_F - E_i}{kT}\right) = n_i \exp\left(-\frac{\phi_F}{kT}\right)$

$\Rightarrow \quad p = p_i \exp\left(-\frac{(E_F - E_i)}{kT}\right) = p_i \exp\left(\frac{\phi_F}{kT}\right)$

$N_A = n_i \exp\left(\frac{\phi_F}{kT}\right) \qquad (2)$

(2) in (1) : $\quad n_s = n_i \exp\left(\frac{\phi_F}{kT}\right) \exp\left(-\frac{\phi_F}{kT}\right) = n_i$ $\qquad$ ii)

$V_s < \phi_F$: depletion $\qquad V_s > \phi_F$: weak inversion.

$V_S = 2\phi_F \Rightarrow n_S = N_A \exp(0) = N_A$ iii) [1]

ii) is the definition of threshold [1]

$\Rightarrow$ $V_S < 2\phi_F$ weak inversion.
$V_S > 2\phi_F$ moderate inversion.

Note: both $V_S = \phi_F$ & $V_S = 2\phi_F$ define the boundary between two operation Regimes.

c) ideal long channel MOSFET in strong inversion

$$I_{DS} = \frac{\mu C_{ox} W}{L}\left((V_{GS} - V_{tn})V_{DS} - \frac{V_{DS}^2}{2}\right)$$

linear region: $I_{DS} = \frac{\mu C_{ox} W}{L}(V_{GS} - V_{tn})V_{DS}$

threshold $V_{GS} = V_{tn} \Rightarrow I_{DS} = 0$

in I_{DS} equation:

$$0 = 2.85\ 10^{-13}\ V_{th} - 4.425\ 10^{-13}$$

$$V_{th} = \frac{4.425}{2.85}\ V = 0.5 \quad [2]$$

Saturation $I_{DS} = \frac{\mu C_{ox} W}{2L}(V_{GS} - V_{tn})^2 = K V_{GS}^2 - 2KV_{tn}V_{GS} + V_{tn}^2 K$

threshold $V_{GS} = V_{tn} \Rightarrow I_{DS} = 0$

In I_{DS} equation:

$$0 = 4.425\ 10^{-11}\ V_{th}^2 - 3.9825\ 10^{-11}\ V_{th} + 8.960625\ 10^{-12}$$

$$0 = 4.425\ V_{th}^2 - 3.9825\ V_{th} + 0.8960625$$

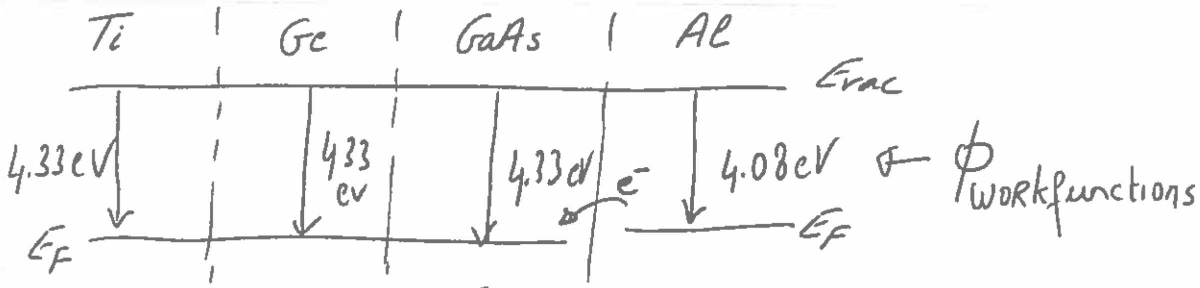
$$V_{th} = \frac{+3.9825 \pm \sqrt{(3.9825)^2 - 4 \times 4.425 \times 0.8960625}}{2 \times 4.425}$$

$$= 0.45V \quad [2]$$

$$DIBL = \left|\frac{V_{th}^{lin} - V_{th}^{sat}}{V_{DS}^{lin} - V_{DS}^{sat}}\right| = \frac{0.5 - 0.\cancel{45}}{|0.01 - 1|} = 0.051 \ \frac{V}{V}$$ [1]

$$= 51 \ \frac{mV}{V}$$

d)



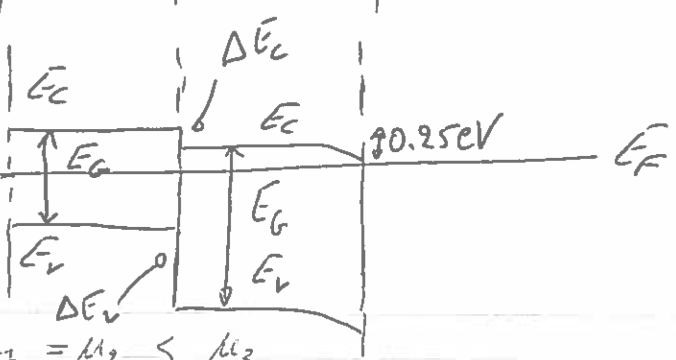
$E_G^{Ge} = 0.66eV$

$\Delta E_C = 4 - 4.1 = 0.1eV$

$E_G^{GaAs} = 1.42eV$

$\Delta E_V = \Delta E_G - \Delta E_V$

$= 0.66eV$



[5]

e) i) $\mu_1 = \mu_2 < \mu_3$

OR $\mu_3 > \mu_2 = \mu_1$ [3]

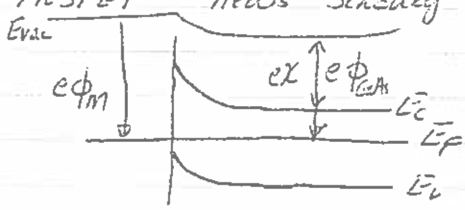
ii)

$v_{sat_2} < v_{sat_3} < v_{sat_1}$

OR

$v_{sat_1} > v_{sat_3} > v_{sat_2}$ [2]

f) n-type MESFET needs Schottky contact



$\phi_{GaAs} < \phi_m$ for Schottky contact

[5]

$\phi_{GaAs} = \chi_{GaAs} + \frac{(E_C - E_F)}{e}$ $\qquad N_D = 10^{15} cm^{-3} \rightarrow$ very low

$$\phi_{GaAs} = 4.1\ eV + 0.156\ eV \cong 4.26\ eV$$

$$n = N_c \exp\left(\frac{-(E_c - E_F)}{kT}\right)$$

$$E_c - E_F = kT \ln\left(\frac{N_c}{n}\right)$$

$$= 0.026 \ln\left(\frac{4.7\ 10^{17}}{10^{15}}\right) = 0.156\ eV$$

Ni will be the best theoretical choices because this gives the largest $V_{bi} = \phi_m - \phi_{GaAs}$.

g) $I_{0_G}^{MESFET} > I_{0_G}^{JFET}$

the gate of a MESFET is determined by a Schottky barrier, that of a JFET by a pn-junction.

the leakage current through the gate is related to this barrier height.
Due to interface charges & traps in a metal/semiconductor contact the barrier height in a MESFET is lower than in a JFET

$$\Rightarrow I_{G_0}^{MESFET} > I_{G_0}^{JFET}.$$

[5]

h) i) finFET [1]

ii) a) gate
b) buried oxide layer
c) gate oxide
d) Si substrate.

[4]

(2) a) Small drain voltage = linear (triode) Region [8]

W_{max} = maximum depletion width from gate = @ threshold

$\rightarrow W_{max} = W_{depl}(V_s = 2\phi_F)$

formulae sheet: * $W_{depl} = \left[\frac{2\varepsilon_0\varepsilon_{si}(V_{bi} - V)}{e}\frac{1}{N_A}\right]^{1/2}$ for 1-sided junction

$V_{bi} = 0$: only consider V_s and anyway $\phi_m = \phi_{p\,si}$

$$W_{max} = \sqrt{\frac{2\,\varepsilon_0\,\varepsilon_s\,2}{e\,N_A}\frac{kT}{e}\ln\left(\frac{N_A}{n_i}\right)}$$

$$W_{max} = \sqrt{\frac{4\times 8.85\,10^{-14}\frac{F}{cm}\,12\,0.026}{1.6\,10^{-19}\,C\,\,10^{16}cm^{3}}\ln\left(\frac{10^{16}}{1.45\,10^{10}}\right)} = 3.05\,10^{-5}\,cm$$

* $W_{DB} = \sqrt{\frac{2\varepsilon_0\varepsilon_{si}(V_{bi} + 0.26)}{e\,N_A}}$ assume depletion region extends in the lowest doping side only.

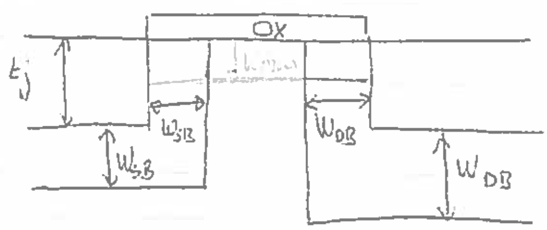
$$V_{bi} = \frac{kT}{e}\ln\left(\frac{N_A N_D}{n_i^2}\right) = 0.026\ln\left(\frac{10^{16}\,10^{20}}{(1.45\,10^{10})^2}\right) = 0.94\,V$$

$$W_{DB} = \sqrt{\frac{2\,8.85\,10^{-14}\,12\,(0.94+0.26)}{1.6\,10^{-19}\,10^{16}}} = 3.99\,10^{-5}\,cm$$

* W_{SB} : same assumption as for W_{DB} and $V_s = 0\,V$

$$W_{SB} = \sqrt{\frac{2\times 8.85\,10^{-14}\,12\,0.94}{1.6\,10^{-19}\,10^{16}}} = 3.53\,10^{-5}\,cm$$

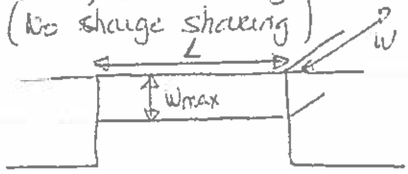
b)



[4]

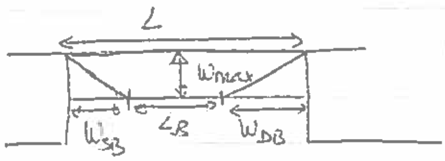
c) Q_G (No charge sharing) Charge controlled by gate when

[8]



$$Q_G = \frac{-e N_A W_{max} L W}{L W} \quad : \quad (\text{charge per gate area})$$

Q_{GCS} (with charge sharing) charge controlled by gate



area trapezium : $\left(\frac{L+L_B}{2}\right) \cdot W_{max}$

$$Q_{GCS} = -e N_A W_{max} \left(\frac{L+L_B}{2}\right) W$$

$$= \frac{-e N_A W_{max}}{L W} \left(\frac{L + (L - W_{SB} - W_{DB})}{2} W \right)$$

charge per gate area.

charge lost : $\Delta Q = Q_G - Q_{GCS}$

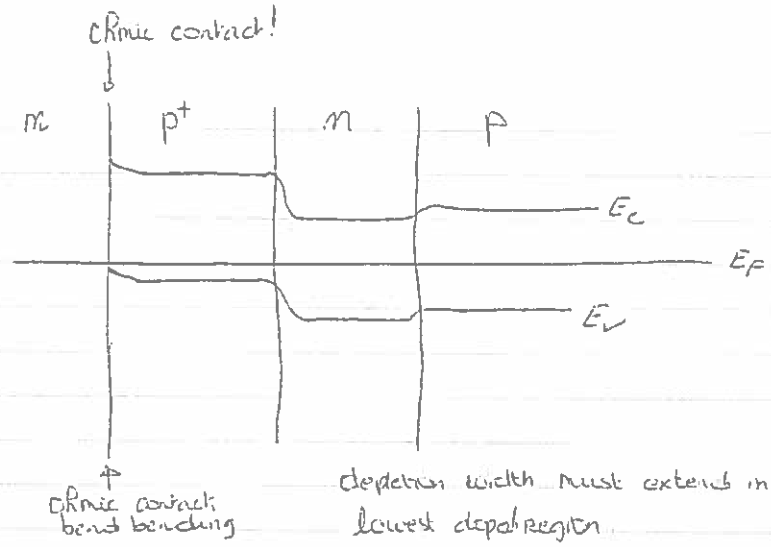
$$= \frac{-e N_A W_{max} W}{L W} \left(L - \left(\frac{2L - W_{SB} - W_{DB}}{2} \right) \right)$$

$$= \frac{-e N_A W_{max} W}{L W} \left(\frac{2L - 2L + W_{SB} + W_{DB}}{2} \right)$$

$$= \frac{-e N_A W_{max} W}{L W} \left(\frac{W_{SB} + W_{DB}}{2} \right)$$

$$\Delta V_{th} = \frac{-e N_A W_{max} (W_{SB} + W_{DB})}{2 C_{ox} L}$$

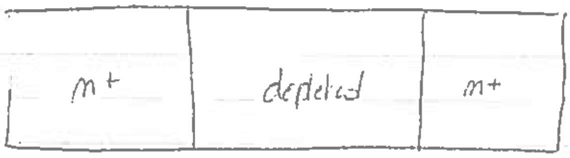
3. a)



[5]

depletion width must extend in the lowest depol region

b)

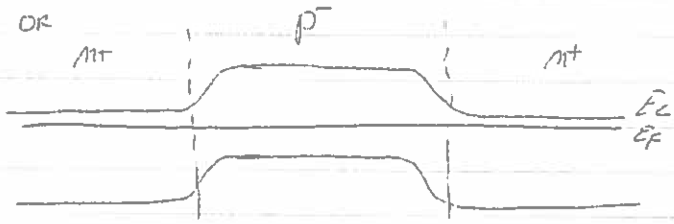


[5]

Note, in the MOSFET part of the course, we have seen that depleted means that the electron concentration $\leq n_i$

$\Rightarrow$ possibilities

OR



c) Pinch-off occurs when the channel is depleted,
Since it is stated that the differences in doping concentration need to be taken into account, the depletion extending from the p⁺type region & that from the bulk both need to be taken into account.

[10]

Depletion from bulk

W_B

channel $N_D = 10^{17}\ cm^{-3}$
bulk $N_A = 5 \cdot 10^{17}\ cm^{-3}$

$\Big\}$ only 5x different $\Rightarrow$ have to take both into account

In formulae sheet $\quad W = \sqrt{\dfrac{2\varepsilon_0\varepsilon_{si}(V_0 - V)}{e}\left(\dfrac{1}{N_A} + \dfrac{1}{N_D}\right)}$

we only need W_p
we know that $\quad w_n + w_p = W \qquad (1)$
charge neutrality $\quad W_n N_D = W_p N_A \qquad (2)$

$$(2) \quad W_n = W_p \frac{N_A}{N_D} \qquad (3)$$

$$(3) \text{ in } (1) \quad W_p\left(\frac{N_A}{N_D} + 1\right) = W$$

$$W_p\left(\frac{N_A + N_D}{N_D}\right) = W$$

$$V_B = 0 \longrightarrow \quad W_p = \sqrt{\frac{2\varepsilon_0\varepsilon_s}{e}(V_B)\left(\frac{N_A + N_D}{N_A N_D}\right)}\left(\frac{N_D}{N_A + N_D}\right)$$

$$W_p = W_{B_p} = \sqrt{\frac{2\varepsilon_0\varepsilon_s}{e} V_{0_B}\left(\frac{N_D}{N_A(N_A + N_D)}\right)}$$

Depletion from gate (p^+)

gate p^+ : $10^{20}\ cm^{-3}$
channel n : $10^{17}\ cm^{-3}$

$\Big\}$ since $N_A \gg N_D$ assume $w_{p+} \ll w_{n-}$ $\Rightarrow$ 1-sided junction

$$W \cong W_{p_G} = \sqrt{\frac{2\varepsilon_0\varepsilon_{si}(V_{0_G} - V_G)}{e N_D}}$$

@ $V_{GS} = V_P \qquad t_n - W_{B_p} - W_{p_G} = 0$

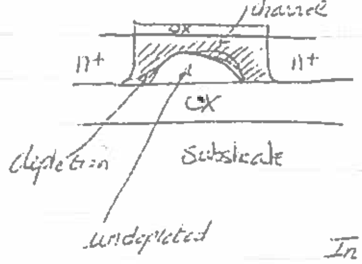
$$W_{p_G} = t_n - W_{B_p}$$

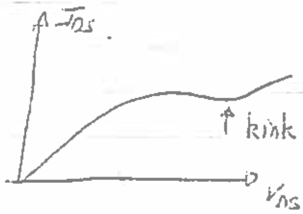
$$\sqrt{\frac{2\varepsilon_0\varepsilon_{Si}(V_{D_G}-V_P)}{e N_D}} = t_n - \sqrt{\frac{2\varepsilon_0\varepsilon_S}{e} V_{D_B}\left(\frac{N_D}{N_{A_B}(N_{A_B}+N_D)}\right)}$$

$$\frac{2\varepsilon_0\varepsilon_{Si}(V_{D_G}-V_P)}{e N_D} = \left(t_n - \sqrt{\frac{2\varepsilon_0\varepsilon_S}{e} V_{D_B}\left(\frac{N_D}{N_{A_B}(N_{A_B}+N_D)}\right)}\right)^2$$

$$V_P = \frac{2\varepsilon_0\varepsilon_{Si}V_{D_G}}{e N_D} + \left(\sqrt{\frac{2\varepsilon_0\varepsilon_{Si}}{e} V_{D_B}\left(\frac{N_D}{N_{A_B}(N_{A_B}+N_D)}\right)} - t_n\right)^2$$

4) a) kink in PDSOI





[5]

In PDSOI, the depletion region from the gate does not reach the BOX → there is a region of <u>undepleted Si</u>. When the voltage V_{DS} increases, <u>impact ionisation</u> occurs @ drain creating e^-h^+ pairs. e^- get extracted in D but <u>h^+ build up</u> in the undepleted region. This causes a change in charge in that region → then change in Q_{depl} and thus a <u>change in ΔV_{th}</u> $= \frac{\Delta Q_{depl}}{C_{ox}}$
$V_{th}\uparrow \Rightarrow (V_{GS}-V_{th})\downarrow \Rightarrow I_{DS}\downarrow$ → kink

b) advantages : (*) isolation between nMOS & pMOS removes latch-up [5]
(take 3 out of) (*) fewer processing steps needed

(*) Reduce substrate leakage => lower power consumption.
(*) higher packing density
(*) smaller parasitic capacitances => higher speed

disadvantages

(take 2 out of)

(*) Completely surrounded by oxide => heating problem
(*) SOI substrate more expensive
(*) transients : minority carrier ~~supply~~ creation only available via recombination / generation processes

c) for fully depleted SOI t_c needs to be depleted @ $V_{GS} = 0V$ => the depletion region from the gate $d_G = t_c$. This depletion region can only be formed by the workfunction difference between n-Si & ~~metal~~ gate contact.

from formulae list:

$$W_{depl} = \left[\frac{2\varepsilon (V_{bi} - V)}{e} \left(\frac{1}{N_D} + \frac{1}{N_A} \right) \right]^{1/2}$$

{ One-sided junction =>
{ $V_{GS} = 0V$

[10]

$$W_{depl} = \left[\frac{2\varepsilon V_{bi}}{e N_A} \right]^{1/2}$$

the maximum width of t_c is when $V_{th} = 0V$
thus $t_c \leq W_{depl} (V_{th} = 0V)$

V_{th} from formulae list:

$$V_{th} = \phi_m - \phi_S + 2\phi_F + \gamma \sqrt{2\phi_F}$$

$$\gamma = \frac{\sqrt{2 e \varepsilon_S N_A}}{C_{ox}}$$

$V_{th} = 0 = \phi_m - \phi_s + 2\phi_F + \gamma\sqrt{2\phi_F}$

$\Rightarrow \phi_m = \phi_s - 2\phi_F - \gamma\sqrt{2\phi_F}$

V_{bi} in W_{depl} = ?

$V_{bi} = 2\phi_F$ when max depl region occurs.

$$t_c^{max} = \sqrt{\frac{2\varepsilon\, 2\phi_F}{eN_A}} \quad \text{with } \phi_F = V_T \ln\left(\frac{N_A}{n_i}\right)$$

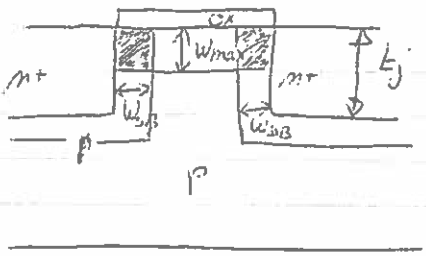
$$\Rightarrow t_{c_{max}}^2 = \frac{4\varepsilon\phi_F}{eN_A}$$

$$\phi_F = \frac{eN_A t_{c_{max}}^2}{4\varepsilon}$$

$$\phi_m = \phi_s - \frac{eN_A t_{c_{max}}^2}{2\varepsilon_0\varepsilon_s} - \gamma\sqrt{\frac{eN_A t_{c_{max}}^2}{2\varepsilon_0\varepsilon_s}}$$

↳ ϕ_m^{min} = minimum value of ϕ_m

(5)



$V_{DS} = 0 \quad V_{GS} = V_{th}$

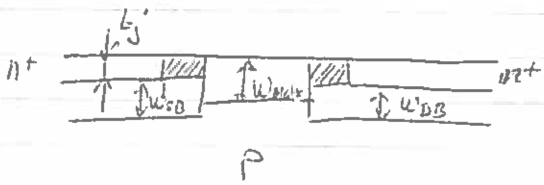
W_{max} : max gate induced depletion width

W_{SB}/W_{DB} : S & D depletion width

area of shared charge

✓

[5]



area of shared charge

t_j ↓

all other parameters same.

b) $t_j \searrow \Rightarrow$ contact resistance $\nearrow$
$\Rightarrow R_S \nearrow$ (source resistance)

$$g_m = \frac{dI_{DS}}{dV_{GS}} \quad \text{or} \quad \frac{1}{g_m} = \frac{dV_{GS}}{dI_{DS}}$$

$$V_{GS}^{ext.} = V_{GS}^{int} + R_S I_{DS} \qquad \text{assume} \begin{cases} I_G = 0 \checkmark \\ I_{bulk} = 0 \checkmark \end{cases}$$

$$\frac{1}{g_m^{ext}} = \frac{dV_{GS}^{ext}}{dI_{DS}}$$

$$= \frac{d\left(V_{GS}^{int} + R_S I_{DS}\right)}{dI_{DS}} = \frac{dV_{GS}^{int}}{dI_{DS}} + R_S$$

$$\frac{1}{g_m^{ext}} = \frac{1}{g_m^{int}} + R_S$$ [8]

$$\frac{1}{g_m^{ext}} = \frac{1 + R_S g_m^{int}}{g_m^{int}}$$

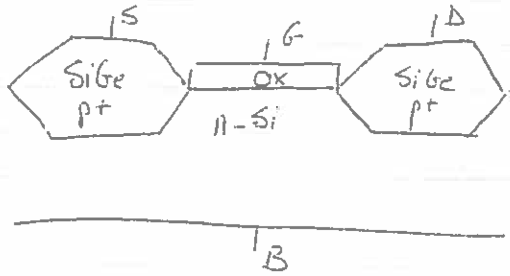
$$g_m^{ext} = \frac{g_m^{int}}{1 + R_S g_m^{int}}$$

ext : externally measured g_m
int : internally " "
(without R_S parasitic)

c)

c) i) elevated source-drain technology. [2]

ii) SiGe has a larger lattice constant than Si, thus when the Si channel is surrounded by SiGe (e.g. in the source & drain areas) it puts Si under compressive strain increasing hole mobility (for pMOS). [2]

iii) 

[3]