IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2011

EEE/ISE PART I: MEng, BEng and ACGI

DIGITAL ELECTRONICS 1

Wednesday, 1 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 each carry 30%.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible   First Marker(s) :   Z. Durrani

                          Second Marker(s) :   E. Shamonina

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Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X[7:0] is an eight bit bus with X7 being the MSB and X0 the LSB.

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

Question 1

1. a) Simplify the following Boolean expressions using De Morgan's theorem and/or Boolean algebra.

    i) $\overline{A}\,\overline{B}\,\overline{C} + \overline{B}C + B\overline{C} + A\overline{B}$

    ii) $\overline{\overline{\overline{\overline{A}BCD}}}$

    [4]

    [4]

    b) Simplify the following Boolean equation, in sum-of-products form, using a Karnaugh map.

    $$f(A,B,C,D) = \Sigma(0,1,2,5,7,8,9,10)$$

    [4]

    c) Simplify the following Boolean equation, in product-of-sums form, using a Karnaugh map.

    $$f = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}CD + \overline{A}\,\overline{B}\,C\overline{D} + BCD + A\overline{C}\,\overline{D} + ACD + ABC$$

    [4]

    d) Figure 1.1 shows the output transitions for a J-K flip-flop.

    (i) Give the values of the inputs J and K necessary to obtain these output transitions.

    [2]

    (ii) Draw the Moore state diagram for the J-K flip-flop.

    [2]

Output transition	J	K
0 → 0		
0 → 1		
1 → 0		
1 → 1		

Figure 1.1

e) Assuming that all numbers are 8 bits wide, and given that the hexadecimal code for the ACSII character 'A' is 41, complete the missing entries which are not shaded in the following table. (No marks will be awarded for this question unless you show how the solution is derived.)

[8]

Binary	Hexadecimal	Unsigned decimal	Signed decimal	ASCII
?		77		?
10100011	?		?	

f) For the circuit shown in Figure 1.2, find the Boolean expressions for the logic functions P and Q.

[6]

MUX

A
B

$G\frac{0}{3}$

1 → 0
0 → 1
1 → 2
D → 3

P

MUX

C

$G\frac{0}{3}$

1 → 0
0 → 1
0 → 2
→ 3

Q
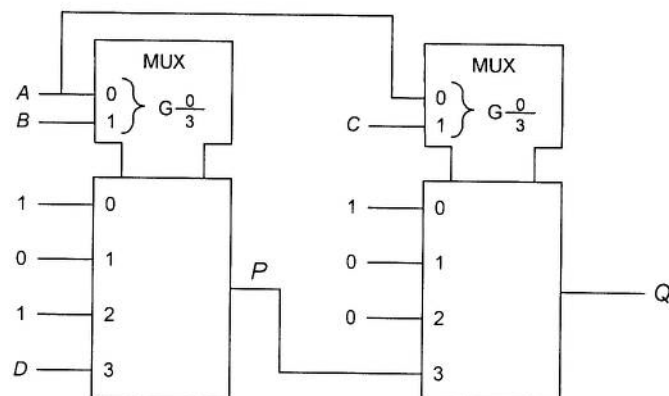
Figure 1.2

g) Figure 1.3 shows a finite state machine (FSM) implemented with a ROM that contains four 4-bit numbers. The ROM address and data lines are A[1:0] and D[3:0] respectively. D[1:0] are connected to the inputs of two D-type flip-flops and D[2] provides the output signals Z. The contents of the ROM are shown in Figure 1.4. The flip-flops are initially in the reset state (Q0 = Q1 = '0').

(i) Draw the Moore state diagram of the FSM.
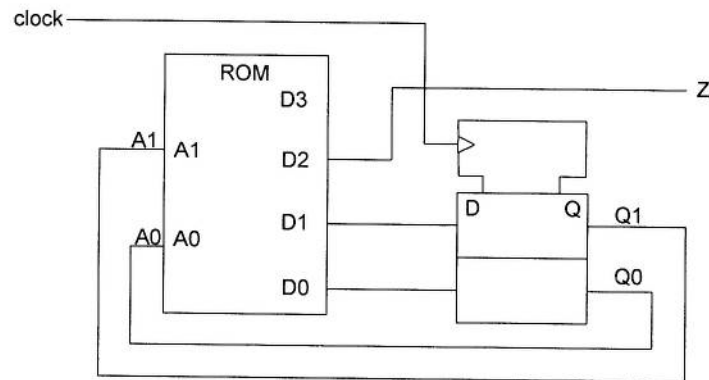
[3]

(ii) Sketch the waveforms for Q0, Q1 and Z for 5 cycles of the clock.

[3]

Figure 1.3

Address	Data
0	2
1	4
2	3
3	1

Figure 1.4

Question 2

2. a) Figure 2.1 shows a J-K flip-flop with an asynchronous clear terminal. By using this flip-flop:

(i) Design an asynchronous binary counter which counts the sequence:
0, 1, 2, …. 9, 0, 1, 2, ….. indefinitely

[6]

(ii) Sketch the timing diagram of your counter for 12 clock periods, starting with the counter at decimal 0, and mark the position of any glitches in the output.
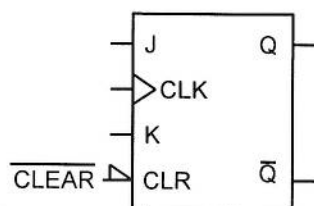
[4]

Figure 2.1

b) The circuit of Figure 2.2 consists of three shift registers, a full-adder, and a D-type flip-flop. For the timing waveforms for the input signals CLOCK and $\overline{\text{LOAD}}$ shown in Figure 2.3, draw the waveforms for P, Q, CIN, Z2, Z1 and Z0. Assume that these functions are initially '0'.
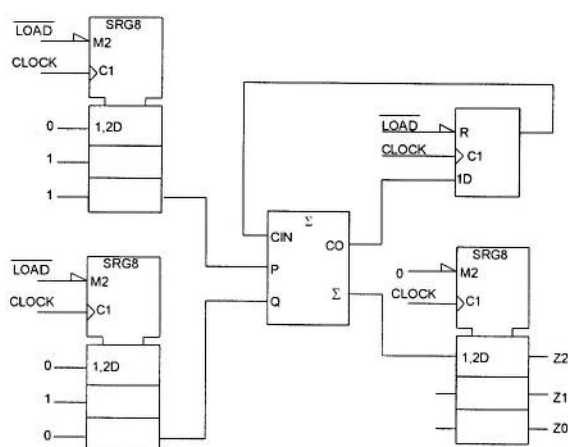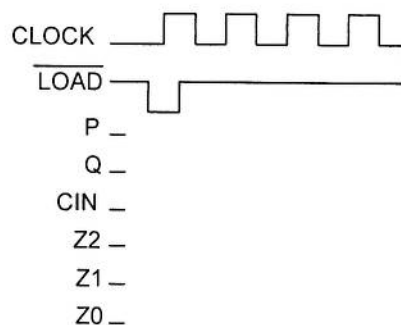
[6]

Figure 2.2

Figure 2.3

c) Figure 2.4 shows a 1-bit full subtractor, with inputs P, Q and B_i, and outputs D and B_o. The circuit performs the binary subtraction $P - Q - B_i$, where P and Q are the bits to be subtracted and B_i is a 'borrow' bit from a previous stage of subtraction. D corresponds to the difference output and B_o indicates if a 'borrow' has been necessary from the following stage.

(i) Write down the truth table for the 1-bit full subtractor.

[8]

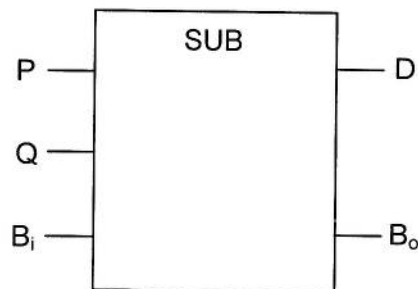(ii) Hence, determine the Boolean expressions for D and B_o.

[6]

Figure 2.4

Question 3

3. Figure 3.1 shows a 7-segment display driven by a finite state machine (FSM). The FSM output signals A, B, C, D, E, F and G are connected to the display inputs and the segments turn-on when the corresponding signal is 'high'. The display is driven such that the sequence $3 \rightarrow 2 \rightarrow 1 \rightarrow 0$ is repeated. The corresponding patterns on the display are shown in Figure 3.2. Here, '1' lies on the right-hand side of the display.

a) Draw the state diagram for the FSM.

[4]

b) Draw the state transition table for the FSM.

[8]

c) The FSM is to be implemented using D-type flip-flops and a combinational logic circuit. Determine the Boolean expressions necessary for this implementation.

[10]

d) Sketch the minimal circuit diagram for your design. This should show the D-type flip-flops, the gate-level circuit diagram for the combinational logic circuit, and any interconnections.
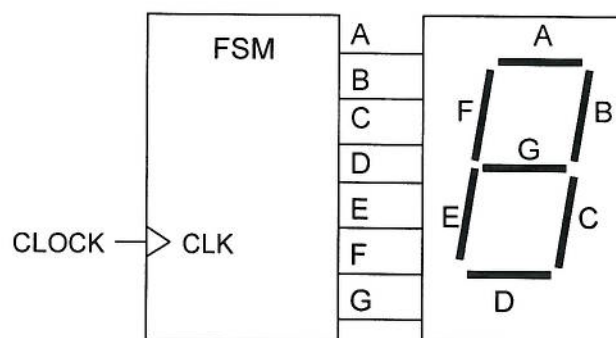
[8]

Figure 3.1

Figure 3.2

[THE END]

E1.2 Digital Electronics 1
Solutions 2011

Answer to Question 1:

a) (i)

$$\overline{A}\,\overline{B}\,\overline{C} + \overline{B}C + B\overline{C} + A\overline{B}$$
$$= \left(\overline{A}\,\overline{C} + A\right)\overline{B} + \overline{B}C + B\overline{C}$$
$$= \left(A + \overline{C}\right)\overline{B} + \overline{B}C + B\overline{C}$$
$$= \overline{B}\,\overline{C} + A\overline{B} + \overline{B}C + B\overline{C}$$
$$= A\overline{B} + \overline{B}\left(C + \overline{C}\right) + B\overline{C}$$
$$= A\overline{B} + \overline{B} + B\overline{C}$$
$$= \overline{B} + B\overline{C} = \overline{B} + \overline{C}$$

[4]

(ii)

$$\overline{\overline{\overline{\overline{A}BCD}}}$$

$$= \overline{\overline{\overline{ABC}}} + \overline{D}$$

$$= (\overline{\overline{A}} + \overline{B})C + \overline{D}$$

$$= AC + \overline{B}C + \overline{D}$$

[4]

b)

$$f(A,B,C,D) = \Sigma(0,1,2,5,7,8,9,10)$$

$$\Rightarrow f = \overline{A}BD + \overline{B}\,\overline{D} + \overline{B}\,\overline{C}$$

[4]

c)

$$f = \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}CD + \overline{A}\overline{B}C\overline{D} + BCD + A\overline{C}\overline{D} + ACD + ABC$$

$$\Rightarrow f = (A + \overline{B} + D)(C + \overline{D})(\overline{A} + B + \overline{C} + D)$$

[4]

d)

(i) Values of the J and K inputs:

Output transition	J	K
$0 \rightarrow 0$	0	X
$0 \rightarrow 1$	1	X
$1 \rightarrow 0$	X	1
$1 \rightarrow 1$	X	0

[2]

(ii) Moore state diagram:
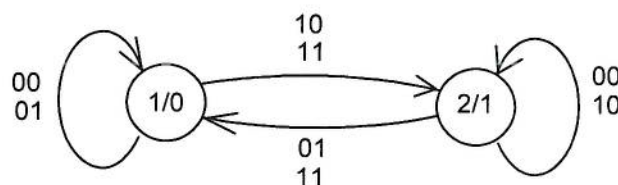
[2]

e)

Binary	Hexadecimal	Unsigned decimal	Signed decimal	ASCII
0100 1101		77		M
1010 0011	A3		-93	

[8]

f)

$$P = \overline{A}\,\overline{B} + A\overline{B} + DAB$$
$$= \overline{B}(A + \overline{A}) + DAB$$
$$= \overline{B} + B(DA)$$
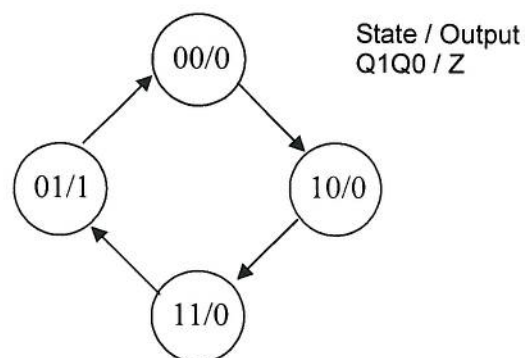$$= \overline{B} + AD$$

$$Q = \overline{A}\,\overline{C} + AC(\overline{B} + AD)$$
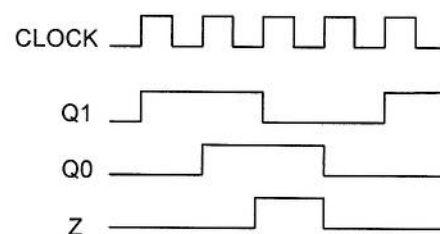$$= \overline{A}\,\overline{C} + AC\overline{B} + ACD$$

[6]

g)

(i) Moore state diagram:

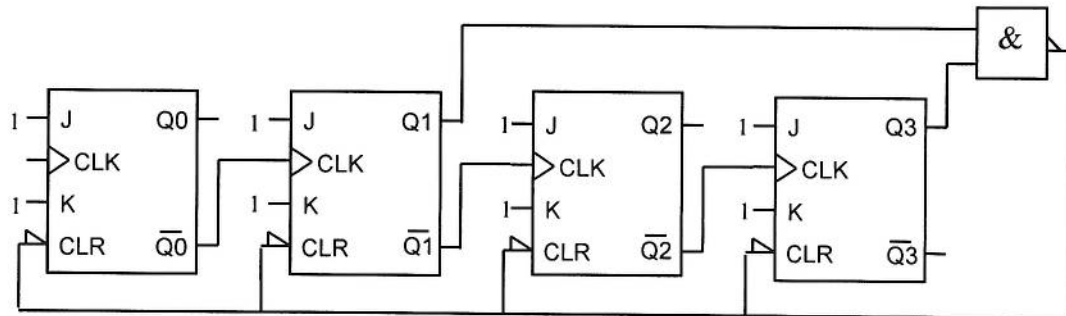State / Output
Q1Q0 / Z

[3]

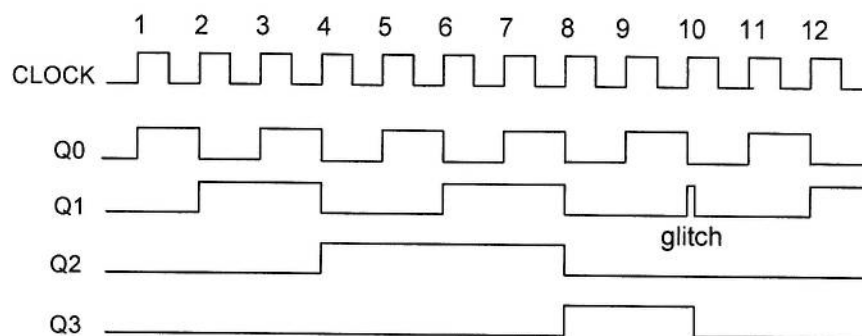(ii) Waveforms for Q0, Q1 and Z:

[3]

Answer to Question 2:

a) (i) The circuit below is an asynchronous 4 bit ripple counter, using J-K flip-flops. The J-K flip-flops 'toggle' with each clock pulse as J=K=1. The counter then counts up from 0 to 9. However, at the next count, the counter output is $(1010)_2$, the 'NAND' gate output becomes 0, and the counter resets to 0.
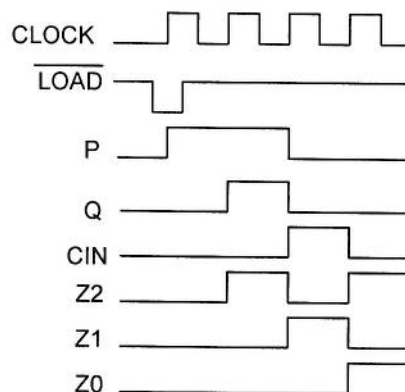

[6]

(ii) Timing waveform of counter:

[4]

b) This is a bit-serial adder. The timing waveforms are as follows:

[6]

c) (i) The operation $P - Q - B_i$ gives the following truth table for the 1-bit full subtractor:

B_i	P	Q	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

[8]

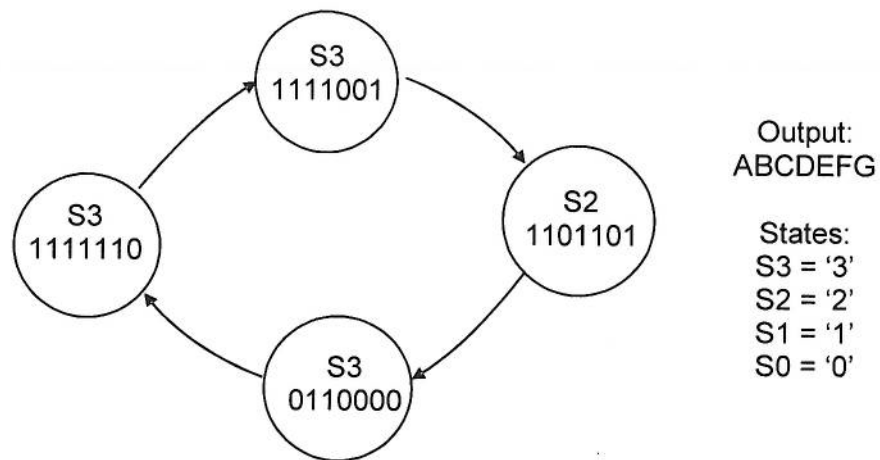(ii) Boolean expressions for D and B_o, using Karnaugh maps:

$$D = \overline{P}\,\overline{Q}B_i + \overline{P}Q\overline{B_i} + PQB_i + P\overline{Q}\,\overline{B_i}$$

$$B_o = \overline{P}Q + \overline{P}B_i + QB_i$$

[6]

Answer to Question 3

a) Moore state diagram:

Output:
ABCDEFG

States:
S3 = '3'
S2 = '2'
S1 = '1'
S0 = '0'

[4]

b) State transition table:

Current state value	Current state							Next state						
	A	B	C	D	E	F	G	A^+	B^+	C^+	D^+	E^+	F^+	G^+
3	1	1	1	1	0	0	1	1	1	0	1	1	0	1
2	1	1	0	1	1	0	1	0	1	1	0	0	0	0
1	0	1	1	0	0	0	0	1	1	1	1	1	1	0
0	1	1	1	1	1	1	0	1	1	1	1	0	0	1

[8]

c) As there are 7 variables, a Karnaugh map approach to obtain simplified Boolean expressions is difficult. However, direct inspection of the state transition table may be used to identify the following Boolean expressions:

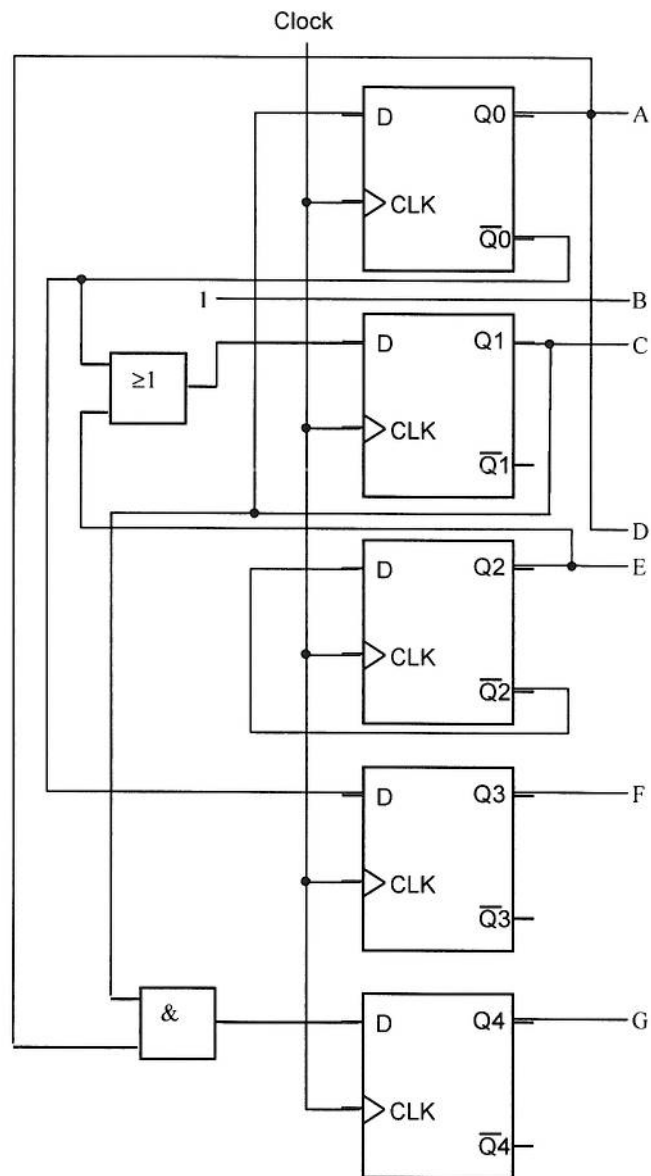$A^+ = C$ $B^+ = 1$ $C^+ = \overline{D} + E$

$D^+ = C$ $E^+ = \overline{E}$ $F^+ = \overline{D}$

$G^+ = AC$

[10]

d) Independent flip-flops for B and D may be eliminated, as B = 1 and D = A. We may also use the inverted outputs of flip-flops, where possible, to eliminate any inverters. The circuit then uses 5 flip-flops, 1 AND gate and one OR gate.

[8]