UNIVERSITY OF LONDON
IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2002

MSc in Computing Science
for Internal Students of the Imperial College of Science, Technology and Medicine

PAPER M2

ARCHITECTURE AND OPERATING SYSTEMS

Friday 26 April 2002, 10:00
Duration: 120 minutes

Answer THREE questions

Paper contains 4 questions
Calculators required

1a Explain the function of the 1-bit Status Flags on the 8086 microprocessor. Describe what conditions are reflected by the C, O, S and Z bits.

b The following hexadecimal digits represent values stored at successive byte locations in the memory of an 8086-based microcomputer.

5678							567F
A7	39	F8	FC	62	FC	64	FC

i) The 16-bit value at location `567A` is a two's complement integer. What is its representation in base 10?

ii) The 16-bit value at location `567C` is an address. What is its representation in base 10?

c The following C function uses Euclid's Algorithm to compute the highest common factor of two positive integers.

```
int hcf(int a, int b) {
    if (a == b)
        return a;
    else
        if (a > b)
            return hcf(a-b, b);
        else
            return hcf(a, b-a);
}
```

Write the equivalent subroutine in 8086 assembler. Your solution should use a stack frame and EQUate statements, preserve the contents of any registers used and include informative comments.

The three parts carry, respectively, 30%, 30%, 40% of the marks.

2a i) Use a sketch to show how two single-bit inputs can be added together by using just an XOR and an AND gate. Why this is called a half adder?

ii) Use another sketch to show how a full adder can be built from a total of five logic gates.

iii) Explain how can a n-bit adder can be built from a series of 1-bit full adders. Why is this called a slow adder?

b i) List the stages of the Basic Machine Cycle.

ii) Explain how the internal structure of the CPU can be utilised to improve performance.

iii) Explain what penalty can occur with this improvement and suggest two possible strategies for avoiding it.

c i) List the elements of the IEEE 754 standard for representation of single-precision floating point numbers, explaining their function and how many bits is used for each. Include how zero and NaNs are represented.

ii) Suggest a suitable (non-IEEE) format for storing floating point numbers including 0.0 that are strictly greater than -1.0 and strictly less than +1.0, using a single 8-bit byte.

iii) What is the largest positive number that can be represented by your format?

iv) What is the smallest positive number that can be represented by your format?

The three parts carry, respectively, 30%, 30%, 40% of the marks.

3a Give an example which shows why testing and setting a lock must be an indivisible operation.

b Two concurrent processes P1 and P2 have a critical region. P1 *increments* the shared integer X by one and P2 *decrements* X by 1. Write pseudocode to protect these critical regions using Semaphores.

Make sure to include data declarations and appropriate initialisations.

c In an operating system with a static multi-level priority ready queue (such as the Simple Kernel), describe two scenarios in which Semaphore operations lead to a context switch between user processes.

d i Illustrate with an example what is meant by *deadlock*?

ii Describe how deadlock is detected.

iii What would be a good policy for choosing which process to terminate once deadlock has been found? If a system did not have deadlock detection facilities how would deadlock manifest itself to the user?

The four parts carry, respectively, 20%, 30%, 20% and 30% of the marks.

4a Carefully distinguish between *processes* and *threads*. How do single-threaded and multi-threaded operating systems differ?

b Suggest two performance benefits that would follow from rewriting an application that runs as a set of communicating single-threaded processes as a multithreaded application.

c Consider a paged virtual memory system with 16K pages that runs on a machine with 32-bit virtual addresses. A 512MB hard disk sector-addressable hard disk with 16K sectors is used as a swap partition. Currently there are 8 processes running on the machine. Now compute the following quantities:

i) How many process page tables are required?

ii) If a process address register (PAR) can be up to 32 bits long, what is the maximum amount of physical memory that can be supported on this machine?

iii) How wide (in bits) should each entry in a process page table be if 64MB physical memory is installed?

d Suppose the scheme is now extended to incorporate segmentation, such that a process can have up to 8 segments, each of which is subdivided into 16KB pages. 32-bit virtual addresses are still used.

i) Draw a diagram to show how a virtual address should be divided into segment number, page number and page offset. Indicate the width (in bits) of each part.

ii) How many page tables and how many segment tables are needed if 3 processes using 8 segments each are currently running.

The four parts carry, respectively, 20%, 10%, 45% and 25% of the marks.