EE1-09b (Operating Systems)

Note to externals

This paper a historic anomaly, an exam for Part b of EE1-09 which delivers 33% of the total module mark. Part A is coursework assessed in Autumn Term.

Therefore it is unique amongst our exams in having only 1/3 of normal weighting and therefore has just one question.



THE ANSWERS

A: Analysis, B: Bookwork, C: Computed Example, D: Design

1. a) i) Describe the 4 distinct categories of data used in the execution of a process, detailing for each category whether it is changed by the process, the operating system, or neither.

[2]

В.

1/2 mark for both category and changer correct (P or O or None). stack-context (P)

attributes (O)

instructions (None)

data (P)

ii) A single process makes transitions in the 7 state model as shown labelled A-D in Figure 1.1. State whether each transition is possible, or impossible. If possible explain what single action would make it happen. The order of the transitions A - D need not be considered.

[2]

A.

A Possible. Process waits on I/O request

B Possible. Process is scheduled

C. Possible. Process is brought back into memory by OS.

D. Impossible. Ready → Waiting, Normal → Suspend depend on different events.

b) i) Describe how preemptive and non-preemptive scheduling are different.

[2]

R

Non-preemptive schduling is carried out only when the current process terminates or waits. Preemptive scheduling may also be carried out when the OS decides another process should run, even though the current process is running.

ii) For the jobs detailed in Figure 1.2, complete two diagrams showing when each job executes for the two cases: Non-preemptive priority scheduling, and shortest remaining job first scheduling.

[4]

A A A A A A A B B B B B B B B B B B B B		Alla.	. 67		- 10			100									
rity		4	1				b., .	0		T1_		-					
A A A A A A A B B B B B B B B B B B B B										1111	1e						
B B B B B B B B B B B B B B B B B B B	Priority		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
C C D non-preemptive priority A A A A B B B B B B B B B B B B B B B	3	Α	Α	Α	Α	Α	Α										
non-preemptive priority a A A A A A A B B B B B B B B B B B B B	1	В						В	В	В	В	В	В				
non-preemptive priority a A A A A A B B B B B B B B B B B B B B	2	C												C	Ç		
a A A A A A A B B B B B B B B B B B B B	4	D														D	
B B B B B B B B B B B B B B B B B B B								non-	pree	empt	ive p	oriori	ity				
B B B B B B B B B B B B B B B B B B B																	
B B B B B B B B B B B B B B B B B B B																	
a C C C a D D	n/a	Α	Α	Α				Α	Α	Α							
a D D	n/a	В									В	В	В	В	В	В	
	n/a	С			С	С											
SRJF	n/a	D					D										
										SRJ	F						

iii) Figure 1.3 shows two execution traces of three non-waiting jobs: A, B and C under two given unknown scheduling methods. Determine whether the scheduling method in each case could be non-preemptive,

ANSWERS

and whether it could be preemptive. For each answer give a reason for impossibility or a scheduling method that could generate the trace.

[2]

Ã.

In trace 1 job A is interrupted by job B before it terminates. Since single jobs are defined not to wait this can only happen with preemption.

in trace 2 every job that starts runs to completion, therefore there is no preemption. However, a scheduling method with preemption could possibly generate this trace. For example, priority scheduling with preemption and A=1, B=2, C=3 will run A then B then C as in trace 2.

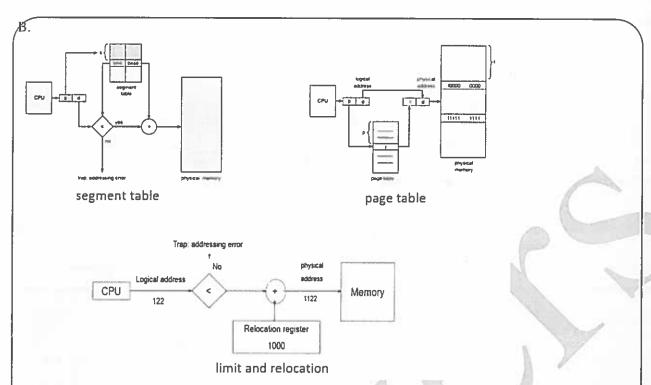
- c) Give one advantage, and one disadvantage, of each of the following methods to implement mutual exclusion.
 - i) Semaphores
 - ii) Interrupt disabling

[2]

3.		
Method	Advantage	Disadvantage
Semaphore	Can implement N bounded mutual exclusion or has low interrupt latency overhead	Slow or complex
Interrupt disable	Fast or simple	Affects all interrupt latency by critical region time

d) Draw diagrams of hardware to implement two distinct logical to physical address translation methods (other than a Translation Look-Aside Buffer) making clear for each how address translation and memory protection are implemented.

[6]



Full marks for any 2 of these solutions. Two marks for the diagram, one for clarifying how memory protection is implemented.

In the case of segment table, and limit and relocation, memory protection is implemented by the comparator and a limoit register as shown.

In the case of a hardware page table, memory protection is implemented by one of:

- limiting the frames available in the page table.
- one or more frames (e.g. those representing os code) are trapped after the page table as invalid
- a special valid bit is used in the page table to indicate whether a given page is valid.

any one of these solutions will be allowed.

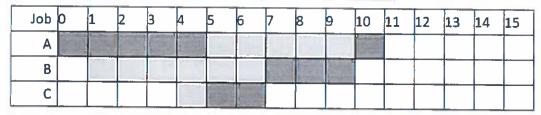
Question 1. has a total of 20 marks.

Transition	From	То
A	Running	Waiting
В	Ready	Running
С	Ready-suspend	Ready
D	Ready	Waiting-suspend

Figure 1.1: State Transitions.

Job	Priority	Arrival time (ms)	Duration (ms			
Α	3	0	5			
В	I	1	6			
С	2	2	2			
D	4	4	I.			

Figure 1.2: Four jobs. B has the highest priority.



Trace 1

Job	0	1	2	3	4	5	6	7	8	9	10	11	12	13	15
Α															
В															
С															-

Trace 2

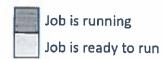


Figure 1.3: Execution traces.