EE4-53
EE9-FPN1-02

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2017

EEE PART IV: MEng and ACGI

Corrected copy

HVDC TECHNOLOGY AND CONTROL

Monday, 8 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer 2 questions from Part A and 2 questions from Part B. Use a separate answer book for each section.

All questions carry equal marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible
First Marker(s) : B. Chaudhuri, M. Merlin
Second Marker(s) : M. Merlin, A.S. Chaudhuri

Part A: Answer any 2 questions out of 3 from this part

1. a) Explain why is it difficult to use LCC technology for realising a sub-sea DC grid such as the one envisaged in the North-sea.

[4]

b) The DC circuit breakers are not necessary to protect a LCC HVDC link against DC-side faults. Justify or rectify this statement describing the steps for DC fault current limiting and interruption.

[5]

c) A standard six-pulse converter bridge is operating with a commutation overlap angle (μ) less than 60°. Answer the following assuming the thyristor valves to be ideal:

i) Considering commutation of current from phase 'a' (valve 1) to phase 'b' (valve 3), show that the voltage of the positive pole is the average of the voltages of the overlapping phases 'a' and 'b'.

[4]

ii) Using the result in part (i) derive an expression for the average reduction in direct voltage due to the commutation overlap in terms of the AC-side voltage, the firing delay (α) and the overlap angle (μ).

[4]

d) Explain why a bipole LCC HVDC link can transmit the same amount of power as an equivalent three-phase AC transmission line using identical conductors and insulators.

[3]

2. a) Explain why 'strong' AC systems are necessary at both ends of a LCC HVDC link for reliable operation.

[5]

b) A monopole LCC HVDC link with six-pulse converters interconnects two separate 400 kV AC systems. The resistance of the DC transmission line is 1.5 Ω. The rectifier end of the link is set to maintain the direct current at 2 kA until the minimum firing angle limit (α_{min}) of 5° is violated. The inverter end is operating with a fixed extinction angle (γ) of 18°. The commutating resistance at either end is 3.0 Ω. The margin current is 15% of the rated current. Calculate the reactive power drawn by the rectifier under the following conditions. Neglect commutation failure, tap changer action, effect of voltage dependent current order limit (VDCOL) and any upper limit on firing angle (α).

i) when rated AC system voltage is maintained at the converter stations at both ends.

[5]

ii) when the rectifier side AC system voltage drops by 20% of the rated value.

[6]

iii) when the inverter side AC system voltage drops by 10% of the rated value resulting in an increase of extinction angle (γ) to 25° to prevent commutation failure while maintaining the rated direct current flow.

[4]

3. a) The control characteristics of the rectifier and inverter of a LCC HVDC link is shown in Figure 3.1 in terms of the direct current (I_d) and DC voltage at the rectifier end (V_{dr}). The commutation resistance at each end in R_c. The DC line resistance is R_L. At both ends, a proportional controller with gain K_p is used to maintain the respective current order. Identify the segments of the control characteristics corresponding to the following control modes and derive an expression for the slope of each segment in terms R_c, R_L and K_p. Comment on the nature of the slope in each case considering $K_p >> R_c > R_L$

i) Rectifier in current control mode.

[3]

ii) Inverter in constant extinction angle control mode.

[3]

iii) Rectifier operating at minimum firing angle (α).

[3]

iv) Inverter in current control mode.

[3]

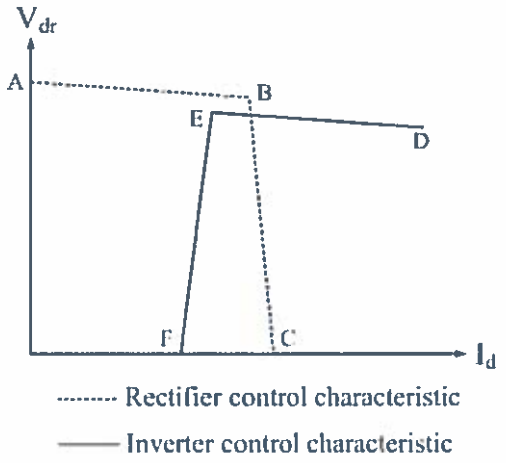

Figure 3.1: Control characteristics for rectifier and inverter

b) What is the role of bridge control and pole control within a converter station of a LCC HVDC link?

[4]

c) Explain why only the inverter end and not the rectifier end of a LCC HVDC link is generally susceptible to commutation failure and spurious turn on of valves due to accidental release of firing pulses.

[4]

Part B: Answer any 2 questions out of 3 from this part

4. For this question, use the symbols, current and voltage directions shown in Figure 4.1.

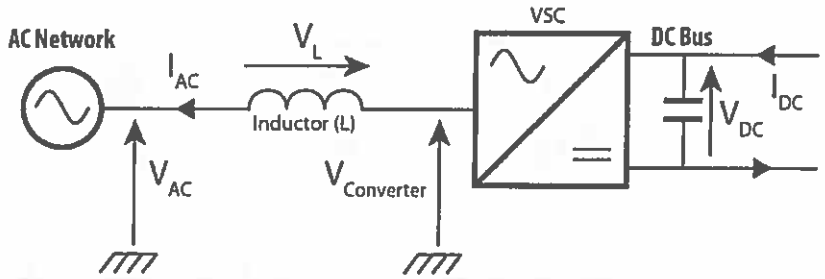

Figure 4.1 – Diagram of a Voltage Source Converter (VSC)

a) What are the properties of VSCs?

[3]

b) Use a phasor diagram and an equation to explain the relationship between the AC grid and converter voltages?

[2]

c) What is the purpose of zero-sequence voltage injection in VSCs?

[3]

d) In the case of a VSC with the following characteristics: ±320kV DC bus voltage, 370kV AC voltage at 50Hz and simple sinusoidal modulation (i.e. no zero-phase sequence voltage injection), calculate the following constraints:

i) Maximum capacitive reactive power when the phase reactor is equal to 150mH?

[3]

ii) Largest possible phase reactor if 350MVAr of capacitive reactive power is required?

[3]

e) For an IGBT with 1.0V initial on-state voltage and 0.6mΩ internal resistance, what are the conduction power losses for the following current waveforms:

i) $I(t) = 1000\,sin\left(2\pi 50\,t + \frac{2\pi}{3}\right) + 600$

[3]

ii) $I(t) = \left|500\,sin\left(2\pi 250\,t - \frac{\pi}{2}\right)\right|$

[3]

5. For this question, use the symbols, current and voltage directions shown in Figure 5.1. The hybrid MMC has part of its stacks consisting of half-bridge submodules (N_{HB}) and full-bridge submodules (N_{FB}). The total number of submodules per stack is $N_{SM} = N_{HB} + N_{FB}$. Please use the same current convention in your answers.

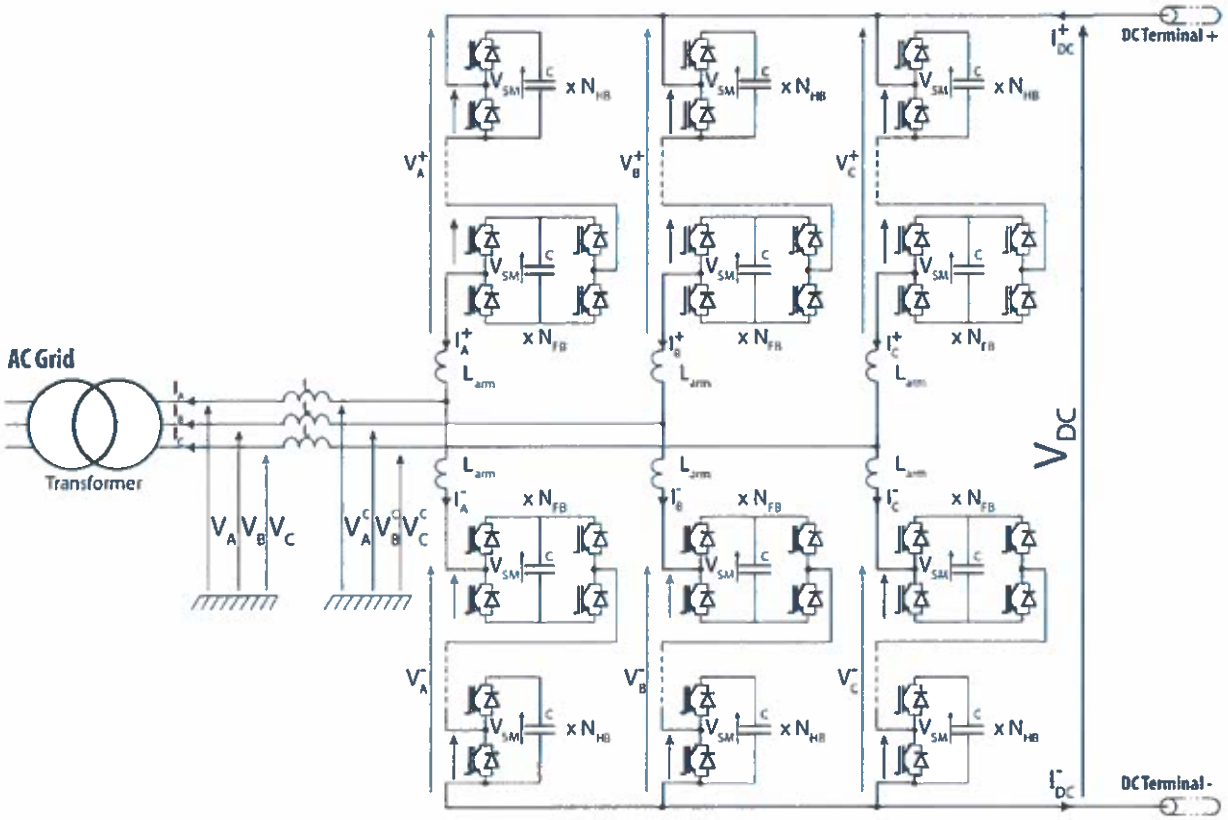

Figure 5.1 – Circuit diagram of a hybrid MMC

a) For a 600 MVA MMC connected to a ±250kV DC bus, calculate the nominal AC line voltage and nominal RMS current magnitudes for the following modulation indexes:

i) 80%.
ii) 100%.
iii) 120%.

[2]

b) For each of the modulation indexes above, calculate the required number of half-bridge and full-bridge SMs per stack, each rated at 3 kV for the following cases. Ignore the voltage drops across the inductors and assume constant SM voltage (i.e. infinite SM capacitance). Also include the resulting number of semiconductor devices in the conduction path:

i) Without DC fault blocking?

[5]

ii) When DC fault blocking is required?

[5]

c) An MMC is inverting power, resulting in 707A RMS AC currents (no reactive power) being injected into the AC grid and 1500A DC current drawn from the DC grid:

i) Write all the six arm current equations based on these AC and DC grid currents.

[2]

ii) To balance its submodule capacitors, the energy management of this MMC requires the following balancing currents:

- Horizontal balancing current in Phase A: 100A
- Horizontal balancing current in Phase B: 200A
- Horizontal balancing current in Phase A: -300A
- Vertical balancing current (RMS) for Phase A only: 354A
- Vertical balancing current (RMS) for Phase B only: 0A
- Vertical balancing current (RMS) for Phase C only: 0A

Calculate the final vertical balancing current equations for each phase to keep the DC current free from any AC components.

[4]

ii) Write the new equations for all six arm current equations using both the AC, DC and balancing currents.

[2]

6. For this question, use the symbols, current and voltage directions shown in in Figure 6.1

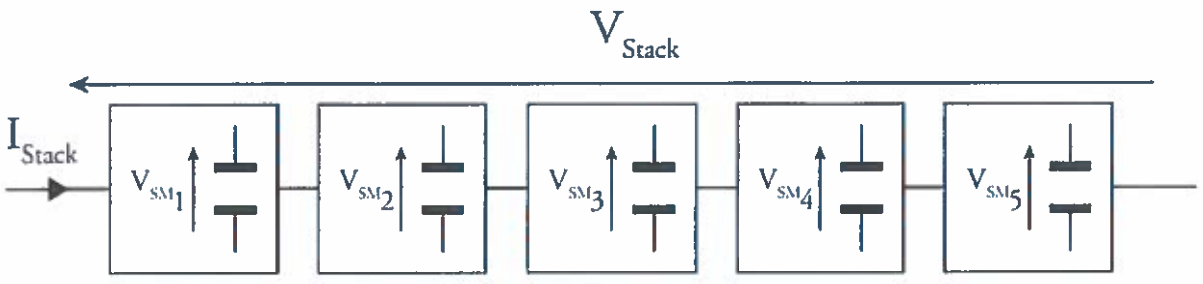

Figure 6.1 – Stack of submodules with pre-charged capacitors

a) Explain the working principles of a stack of submodules, including the operating conditions for stable operation.

[3]

b) A stack of submodules generates a voltage waveform given by:

$$V_{Stack}(t) = 600\sin(\omega t) - 100\sin(3\omega t) + 500$$

For each of the current waveform equations below, state and prove whether the stack will operate stably or not.

i) $I_{Stack}(t) = 10\sin(\omega t) - 6$
ii) $I_{Stack}(t) = 30\sin(\omega t) - 15$
iii) $I_{Stack}(t) = 30\sin\left(\omega t + \frac{\pi}{2}\right)$
iv) $I_{Stack}(t) = 20\sin(\omega t) + 30\sin(3\omega t) - 9$
v) $I_{Stack}(t) = 5\sin(\omega t) + 10\sin(\omega t) - 2$

[5]

c) The operational study of a stack of N_{SM} submodules equipped with a capacitor C_{SM} at the nominal voltage V_{SM} is necessary for the estimation of its maximum ($\overline{\Delta E}$) and minimum ($\underline{\Delta E}$) energy deviations, assuming a maximum submodule voltage deviation of $\pm\Delta V$. Calculate the missing parameters in each case below:

i) Number of submodules,
when $C_{SM} = 1mF, V_{SM} = 3kV, \overline{\Delta E} = 20kJ, \underline{\Delta E} = -5kJ, \Delta V = 10\%$
ii) Submodule capacitance,
when $N_{SM} = 20, V_{SM} = 1kV, \overline{\Delta E} = 15kJ, \underline{\Delta E} = -10kJ, \Delta V = 10\%$
iii) Nominal submodule voltage,
when $N_{SM} = 18,\ C_{SM} = 5mF, \overline{\Delta E} = 5kJ, \underline{\Delta E} = -25kJ, \Delta V = 5\%$
iv) Peak-to-peak energy deviation of the stack,
when $N_{SM} = 16,\ C_{SM} = 3.3mF, V_{SM} = 2kV, \Delta V = 5\%$
v) Desired submodule voltage deviation,
when $N_{SM} = 8,\ C_{SM} = 2mF, V_{SM} = 10kV, \overline{\Delta E} = 50kJ, \underline{\Delta E} = -60kJ$

[5]

d) Explain the concept of submodule rotation.

[3]

[One last question on the other side]

e) Using the representation of a 5-submodule stack in Figure 6.1where each submodule is of a full-bridge type, the measured level of charge of the submodule capacitors is:

$$V_{SM1} = 1.5kV, V_{SM2} = 1.4kV, V_{SM3} = 1.6kV, V_{SM4} = 1.7kV, V_{SM5} = 1.3kV.$$

Indicate the switching state (zero, positive or negative state) of each submodule computed by a rotation algorithm for a certain stack voltage command (choose the solutions which minimize the number of capacitors in the conduction path).

i) The stack voltage command is +4.5kV and the stack current is positive
ii) The stack voltage command is -1.5kV and the stack current is positive
iii) The stack voltage command is +3.0kV and the stack current is negative
iv) The stack voltage command is -6.0kV and the stack current is negative

[4]