EE3-01
EE9-AC1

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2016

MSc and EEE PART III/IV: MEng, BEng.and ACGI

Corrected copy

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Correction @ 9:50am.
Q4 (c)

Monday, 5 December 9:00 am

Time allowed: 3:00 hours

(i) Transistors Q1 & Q2

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : C. Toumazou
Second Marker(s) : P. Georgiou

1. Figure 1 below shows a single stage of a differential amplifier.

(a)

(i) Draw a circuit schematic for the current source I_0 that ensures the differential gain is independent of temperature and power supply variation. Include any start up circuits that may be required.

[9]

(ii) For your design, show that the gain bandwidth product is independent of temperature.

[6]

(b) Draw a circuit schematic of a stable voltage reference that could provide the bias voltage V_s and is independent of temperature variation.

[5]

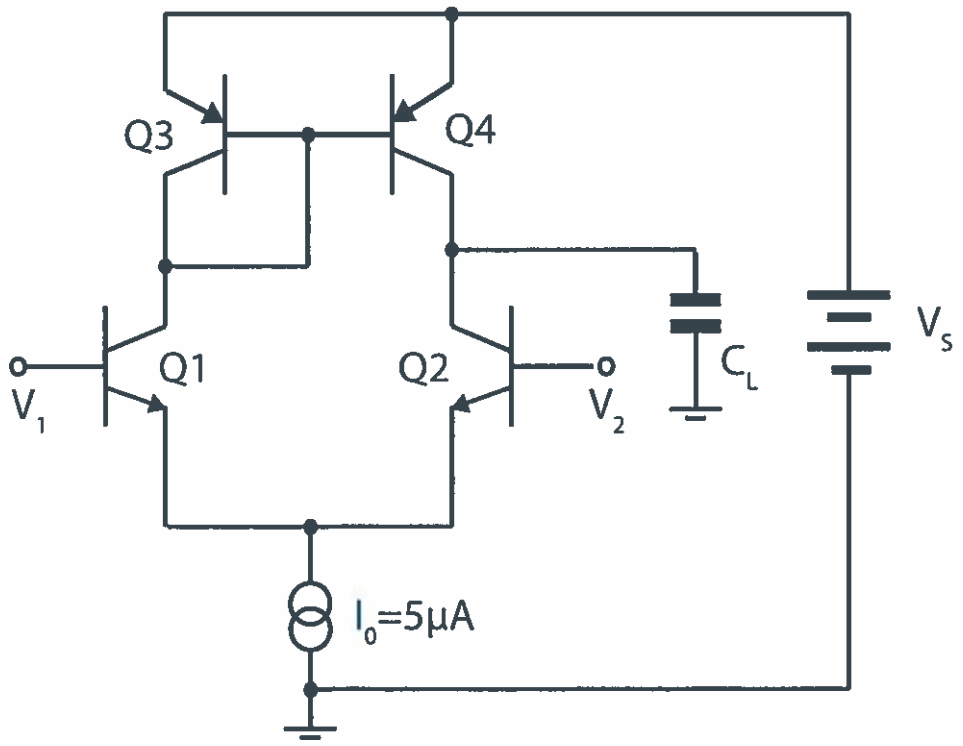

Figure 1.

2. Figure 2 shows a partially-designed two-stage CMOS op-amp required to give a voltage gain of approximately 80 dB, a slew-rate of 5 *V/μs* and a gain-bandwidth product of 3 MHz.

(a) Given that the technology is a fixed 5 μm double metal CMOS process, design the channel widths of transistors Q1, Q2 and Q6 for the op-amp to meet the above performance specifications. Aspect ratios of all other devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below.

[15]

(b) Explain why a resistor in series with the compensation capacitor *C* in Figure 2 can significantly improve the amplifier's phase margin.

[5]

CMOS TRANSISTOR MODEL PARAMETERS

MODEL PARAMETERS	*Kp* ($\mu A/V^2$)	λ (V^{-1})	V_{T0} (V)
PMOS	20	0.03	-0.8
NMOS	30	0.02	1.0

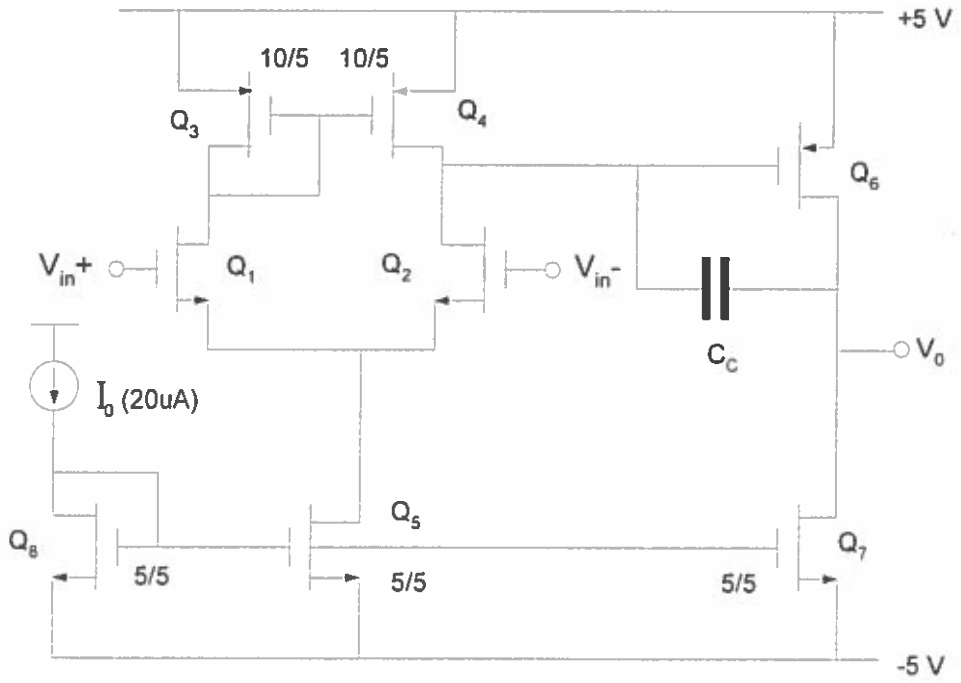

Figure 2

3. (a) Two high-performance analogue-to-digital converters are the current-mode algorithmic converter and the sigma-delta converter. Sketch a typical architecture for ONE of these converter types and explain its principles of operation.

[10]

(b) Assume that the maximum resolution of any sampled-data converter is limited by switch noise (kT/C). Calculate the maximum resolution of a stereo-audio system running at a sample rate of 40 kHz. Assume a MOSFET switch aspect ratio $(W/L) = 1/8$, transconductance parameter $Kp = 20\ \mu A/V^2$ and a device threshold voltage $V_T = 1\ V$. The on voltage of the switch is a $5\ V$ reference (i.e. $V_{GSon} = V_{ref} = 5\ V$). You may also assume that the switch settles in $10\ \tau$ (where τ = time constant) over one period of the clock frequency.

Boltzmanns constant $k = 1.38 \times 10^{-23}\ J/K$ and the ambient temperature is $300\ K$.

[10]

4. Figure 4 shows a differential opamp which is based upon a single-stage fully differential design.

(a) Sketch the circuit diagram of a single-stage fully differential op-amp including common mode feedback.

[6]

(b) Explain the technique used for efficient layout when designing transistor-based amplifiers.

[4]

(c) (i) Transistors Q1 and Q2 of Figure 4 could be considered to form a linear differential resistor. Derive the equation for the linear differential resistance.

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[5]

(ii) Assuming the time constant of the circuit is τ=10ms, calculate the value of feedback capacitor, C, assuming input transistors Q1 and Q2 are operating in the triode region and have W/L=5, K=20uA/V2, Vg=1V, Vt=0.5V and node x is at a common mode of 0 V. You may neglect body effects.

[5]

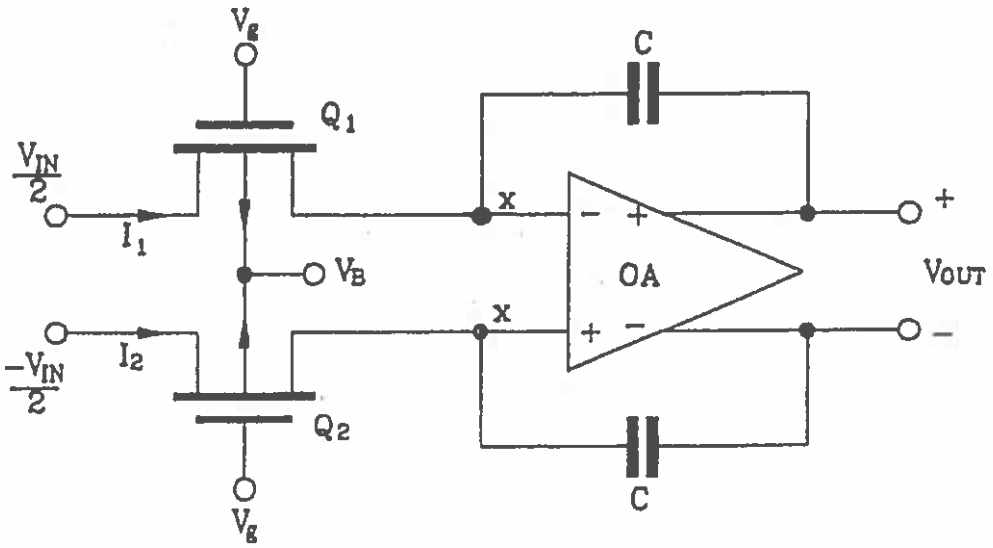

Figure 4.

5.

(a) Sketch the basic design of a 3rd-order Chebyshev low pass switched-capacitor ladder filter using op-amps, capacitors and switches.

[5]

(b) For the circuit in part a. state the equations of the normalised passive component values and draw the equivalent RLC prototype.

[5]

The filter is to have a cut-off frequency of 5kHz. The normalised inductance and capacitance of the ladder filter L2=1.096 and C1=C3=1.596. The values of capacitance in the switched-capacitor filter are 5.08pF for the capacitor based sections and 3.49pF for the inductive sections and all other switched capacitors are 1pF.

(c) i) Calculate the clock frequency required to achieve a cut-off frequency of 5 KHz.

[4]

ii) Show through calculation that the values of capacitance used in the switched-capacitor filter realise the normalised inductance and capacitance values of the original ladder filter.

[6]

6. (a) Sketch the circuit of a VGS multiplier with equations describing its operation. [6]

(b) For the current mirror of Figure 6.1 derive the voltage swing in terms of device threshold voltage V_T, clearly stating any assumptions you make. [7]

(c) Sketch a suitable two transistor and four transistor potential divider voltage reference circuit and show that when VDD=+5V, VSS=-5V and ID=10uA, for an output voltage Vout=0, the four transistor circuit consumes less area than the two transistor one. You may assume $K_P=8\mu A/V^2$, $K_N=17\mu A/V^2$, $V_{TN}=V_{TP}=1V$. [7]

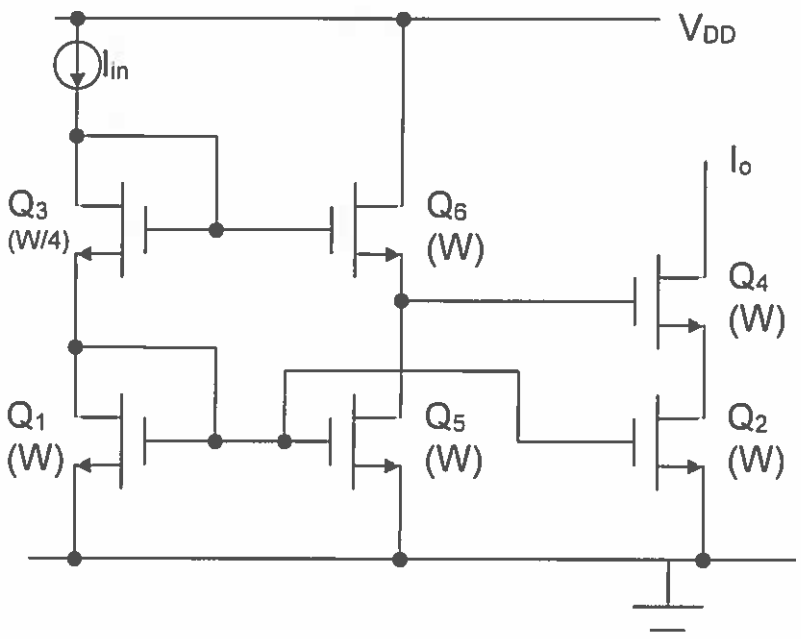

Figure 6.1