UNIVERSITY OF LONDON
IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2002

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER C112

HARDWARE

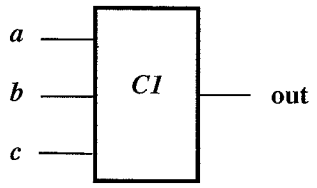
Friday 10 May 2002, 14:00
Duration: 90 minutes
(Reading time 5 minutes)

Answer THREE questions

Paper contains 4 questions
Calculators required

1. Combinational Circuits

a A three-input one-output combinational circuit called *C1* has the following Karnaugh map:



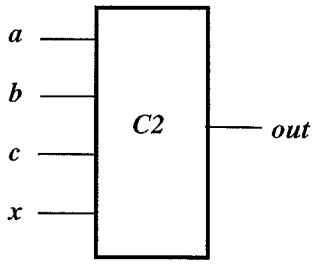
a \ bc	00	01	11	10
0	0	0	1	1
1	1	0	0	1

i) What is its truth table?

ii) Determine the simplest circuit that can be used for *C1* which may contain invertors, two-input AND, OR, NAND or NOR gates.

iii) Find the simplest circuit for *C1* which is built from two-input NAND gates only.

b A four-input one output combinational circuit, *C2* is built with inputs *x, a, b,* and *c*.



When *x=0*, the output of this new circuit is exactly the same as the output of circuit *C1* in terms of inputs *a,b,* and *c*. When *x=1* the output is equal to *b eor a*.

i) Draw the Karnaugh map for this circuit.

ii) Determine the simplest circuit (fewest gates) that can be used for *C2* using invertors, two three or four-input AND, OR, NAND or NOR gates.

iii) In one application the input combinations 000 and 001 for inputs *a,b,c* are never used, and therefore, these can be considered "don't care" inputs. Design a new circuit *C3* for this application.

c Design a two-to-one multiplexer from invertors, two-input AND, OR, NAND and/or NOR gates. Use this multiplexer and your circuit of part a.ii to design a circuit for *C2* using the functional design approach. Compare this circuit to the circuit of part b.ii. Comment on advantages and disadvantages of using the direct and the functional design approach for this example and in general.

The three parts carry, respectively, 30%, 40%, 30% of the marks.

2. Sequential Circuit Design

A counter is to work in four modes determined by two input bits as follows.
When the input is 0 (0,0) the output remains at 0
When the input is 1 (0,1) the counter goes through the sequence 0,3,2,1,0,3,2,1 . .
When the input is 2 (1,0) the counter goes through the sequence 3,1,2,3,1,2 . .
The input (1,1) does not occur.

a Draw the state transition diagram (using the Moore finite machine model) that corresponds to the above specification.

b Compile a state transition table in the following format:

Input		Current State		Next State	
I1	I0	Q1	Q0	D1	D0
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1				
0	1				
0	1				
0	1				
1	0				
1	0				
1	0				
1	0				
1	1				
1	1				
1	1				
1	1				

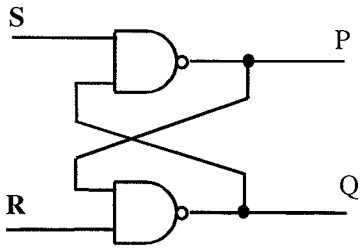
c Draw Karnaugh maps for D0 and D1 and determine the minimum form of the Boolean equations for D0 and D1 to implement the counter.

d Explain what the difference is between the Moore finite state machine and the Mealy finite state machine. For each, give one reason why a designer should choose to use it.

The four parts carry, respectively, 25%,20%,30%,25% of the marks.

3. Registers

a The R-S Flip-flop has the following circuit.



Explain why the flip flop behaviour is sometimes non deterministic.

b Using one R-S flip flop as in part a, and AND gates and invertors, design a D type latch. When the latch input is set to 1 the Q output is the same as D, and when the latch input is 0 the output does not change.

c Show how two D-type latches of the type designed in part b may be connected together, with other gates if required, to form an edge triggered D-Q flip flop.

d A two way multplexer has three inputs A,B and C and one output O. When C=0, the output O is the same as A. When C=1 the output O is the same as B. Design a circuit for this two way multiplexer using only two input NAND gates and invertors.

e Design a four input multiplexer using two-input multiplexers of the kind designed in part d. Label your circuit according to the table:

input (C1, C0)	Output O follows
(0,0)	A
(0,1)	B
(1,0)	C
(1,1)	D

f As part of a hardware design it is necessary to have a register which will carry out four different functions. These are clear, parallel load, hold and rotate left. Draw a labelled diagram showing one stage of this register. You may use any of the components designed above.

The six parts carry, respectively, 15%,15%,15%,15%,15%,25% of the marks.

4. Register Transfers

a Outline briefly the steps that are required to transfer a byte of data from one eight bit register to another. Indicate how the register data lines are connected and how the clock signals are applied.

b The figure overleaf shows part of a simple eight bit processor. Some of the instructions can be executed in one cycle, for example

ADD B,A

in which the contents of register A is replaced by the sum of the contents of A and B. For this particular instruction determine the values that the controller should use for the multiplexer control inputs S0 S1 S2 S3, and the function selectors F0, F1, F2, F3, F4, and indicate which register clocks out of C0 C1 C2 will receive a pulse.

c Some of the instructions will require several clock cycles to execute. For example, the instruction:

MOV B,A

Moves the contents of register B to A, overwriting what was previously in A. Write down the required register transfers to implement this instruction, and determine the values of S0 to S3, F0 to F4 and C0 to C3 for all the necessary cycles.

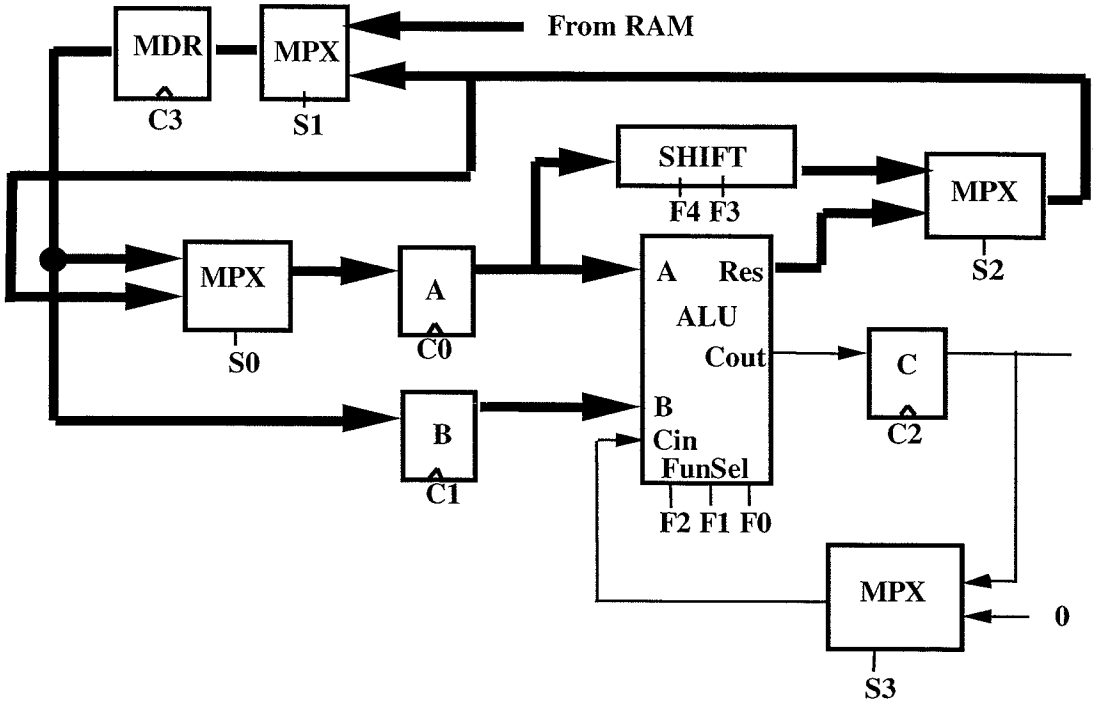
d The instruction:

MOV A,B

Moves the contents of register A to B, overwriting what was previously in B, but preserves the MDR. Write down the required register transfers to implement this instruction, and determine the values of S0 to S3, F0 to F4 and C0 to C3 for all the necessary cycles.

e Explain why register C has been included.

The five parts carry equal marks.



Definitions

Clock gates:

C0 Controls Register A
C1 Controls Register B
C2 Controls the carry store
C3 Controls the Memory Data Register

Multiplexer Selection

S0 Selects the input to register A (0=MDR, 1=Result)
S1 Selects the input to the Memory Data Register (0=RAM,1=ALU/Shifter)
S2 Selects the source of the result (0=ALU Result, 1=Shifter)
S3 Selects the ALU Carry In (0=0, 1=C)

ALU function (F2 F1 F0):

000 0
001 B-A
010 A-B
011 AplusB
100 AeorB
101 A+B
110 A•B
111 -1

Shifter function (F4 F3):

00 No Action
01 Shift Left
10 Logical Shift Right
11 Arithmetic Shift Right