UNIVERSITY OF LONDON
IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2001

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER C112

HARDWARE

Tuesday 15 May 2001, 14:00
Duration: 90 minutes
(Reading time 5 minutes)

Answer THREE questions

Paper contains 4 questions
Calculators not required

1. Sequential Circuit Design

A circuit is to be designed to recognise the sequence 10111 in a synchronous serial input stream. On recognising the sequence, the output is to be set to 1 for one clock pulse only, and overlapping sequences are allowed. Hence an input/output pattern might look like this:

input	0	1	1	0	1	1	1	0	1	1	1	1	0	0	etc.
output	0	0	0	0	0	0	1	0	0	0	1	0	0	0	etc.

a. Draw the state transition diagram that corresponds to the above specification

b. Compile a state transition table in the following format:

Input	This State			Next State		
I	Q3	Q2	Q1	D3	D2	D1
0						
0						
0						
0						
0						
0						
0						
0						
1						
1						
1						
1						
1						
1						
1						
1						

c. Draw Karnaugh maps for D1, D2 and D3 and determine the minimum form of the Boolean equations for D1 and D2 to implement the counter.

d. Design the circuit that will produce the correct output.

The four parts carry, respectively, 25%,20%,30%,25% of the marks.

2. Hardware Arithmetic

a. A full adder has the following truth table:

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Design a combinational circuit for a one bit full adder using *EXCLUSIVE OR* gates if you wish.

b. Show how four of your circuits designed in part a can be connected to make a four bit full adder with both carry in and carry out.

c. Using half adders and inverters design a circuit which generates the 2's complement of a four-bit number.

d. A very simple four bit ALU has just two functions, A plus B and A minus B. It has a single input C where C=0 selects A minus B and C=1 selects A plus B. Design a circuit for this using the components that you designed in parts b and c and any other gates you need.

The four parts carry, respectively, 20%,20%,20%,40% of the marks.

3. Multiplexers and decoders

a. A two-to-one multiplexer has three inputs named IN1, IN2, and SELECT, and the output is named OUT. Show the two possible 3-input, one-output truth tables for the multiplexer if you know that the inputs have been named according to common practice.

b. With the addition of at most one inverter to the above multiplexer, build three separate two-input one output circuits, each one providing the following logical functions:

(i) AND

(ii) OR

(iii) XOR

c. A one-to-two demultiplexer with enable has two-inputs named INPUT and ENABLE, and two outputs named OUT1 and OUT2. Again show the possible two-input, two-output truth tables for this device assuming that the inputs have been named according to common practice.

The three parts carry, respectively, 35%,35%,30% of the marks.

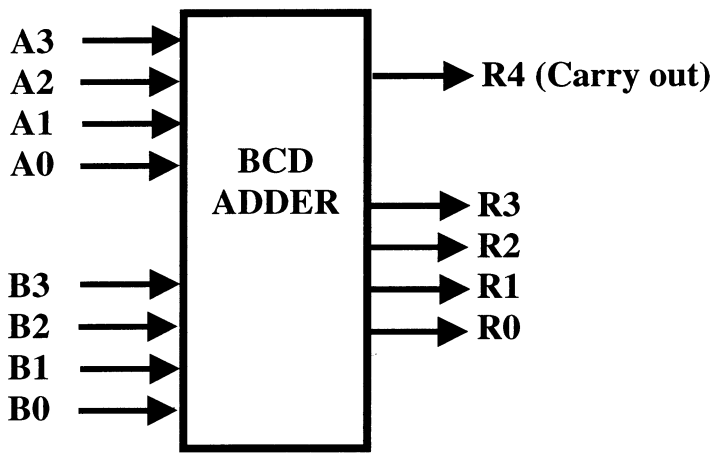
4. Binary Coded Decimal Processing

Binary coded decimal digits are represented by the **excess-3** encoding when the four bits are assigned in the following manner:

BCD digit	B3	B2	B1	B0 (bits)
0	0	0	1	1
1	0	1	0	0
2	0	1	0	1
3	0	1	1	0
4	0	1	1	1
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0

The rest of the bit combinations (**0000, 0001, 0010, 1101, 1110, 1111**) are not used and considered **invalid** BCD digit combinations.

The circuit for the BCD adder of two BCD digits is shown below:



a. Determine the Boolean equation for a four input one output circuit whose output is a **1** when an invalid BCD bit combination is input to it.

b. When a four-bit binary adder is used to add two BCD digits the produced result is not always the correct BCD sum. Show that when the binary adder is used to add two such BCD digits and a carry is not generated (**R4=0**) then a binary subtractor must be used to correct the resulting sum of the two BCD digits.

c. Similarly to part b., show that when two BCD digits are added by a simple binary adder and a carry is generated (**R4=1**), then an additional binary adder must be used to correct the resulting sum of the two BCD digits.

d. Design the BCD adder for two BCD digits defined above (show your work and the final circuit). Assume that only valid BCD digits are used as input.

The four parts carry, respectively, 20%,30%,20%,30% of the marks.