IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2015

EEE/EIE PART I: MEng, BEng and ACGI

DIGITAL ELECTRONICS 1

Corrected Copy

Monday, 1 June 10:00 am

Time allowed: 2:00 hours

There are THREE questions on this paper.

Answer ALL questions.
Q1 carries 40% of the marks. Questions 2 and 3 each carry 30%.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : Z. Durrani
Second Marker(s) : J.V. Pitt

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X[7:0] is an eight bit bus with X7 being the MSB and X0 the LSB.

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

Question 1

1. a) Simplify the following Boolean expressions using De Morgan's theorem and/or Boolean algebra.

i) $\overline{\overline{A}+\overline{\left(A\overline{B}\right)}\overline{C}}$

[4]

ii) $ABC+B\left(A\oplus B\right)$

[4]

b) Simplify the following Boolean equation, in <u>sum-of-products</u> form, using a Karnaugh map.

$$f=\overline{A}\,\overline{B}\left(\overline{C\oplus D}\right)+A\overline{B}\overline{C}\,\overline{D}+ACD+ABD$$

[4]

c) Simplify the following Boolean equation, in <u>product-of-sums</u> form, using a Karnaugh map.

$$f\left(A,B,C,D\right)=\sum\left(2,4,6,8,10,13,14\right)$$

[4]

d) Assuming that all numbers are 16 bits wide, complete the missing entries, which are not shaded in the following table. (No marks will be awarded for this question unless you show how the solution is derived.)

[8]

Decimal	Hexadecimal	Binary	BCD
5153	?		
		0011 0111 1001 1000	?
	1CF	?	
-1101		?	

e) The waveforms for signals P and Q shown in Figure 1.1 are applied to the circuit shown in Figure 1.2. Copy the timing diagram and add waveforms for S, T, U and V. Assume that initially U=0 and V=1.

[8]

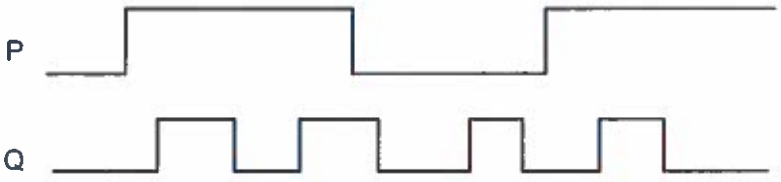

Figure 1.1

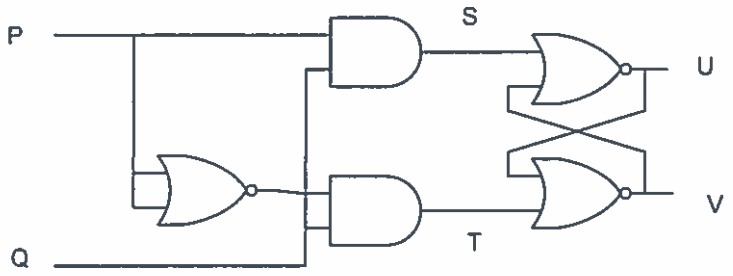

Figure 1.2

f) Sketch the state diagram for the circuit shown in Figure 1.3, where N[2:0] = 011. You may assume that initially, Q[2:0] = 000.

[4]

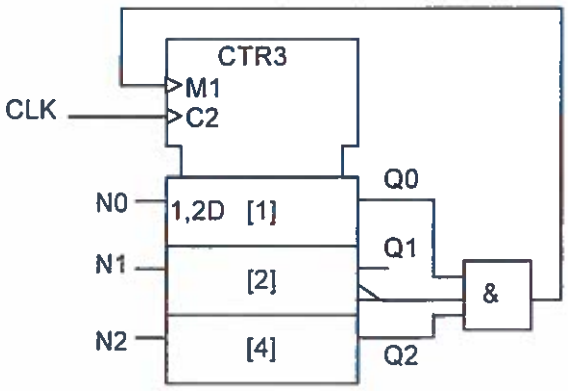

Figure 1.3

g) Draw the truth table for the circuit shown in Figure 1.4.

[4]

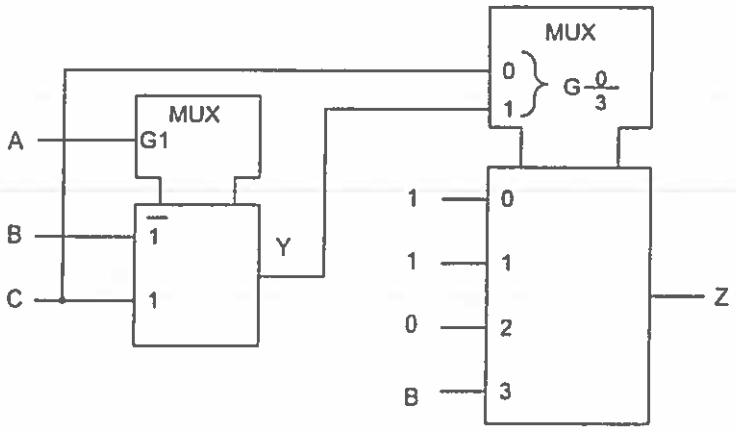

Figure 1.4

Question 2

a) (i) Sketch the LED pattern that would be used on a seven segment LED display to show the hexadecimal character set unambiguously.

[4]

(ii) Hence, using a minimum number of NAND gates and inverters only, design a circuit to control the top horizontal segment of the seven segment hexadecimal display.

[4]

(iii) Modify your design for part (ii) for the case where the hexadecimal characters 5 and 9 never occur. Implement this circuit using NOR gates and inverters only.

[4]

b) Figure 2.1 shows the module COMP, that compares the magnitude of two 4-bit unsigned numbers A[3:0] and B[3:0]. The module produces a logic '1' on outputs H, E and L if A>B, A=B and A<B respectively. Derive Boolean equations for H, E and L. You do not need to simplify your Boolean equations.

[8]

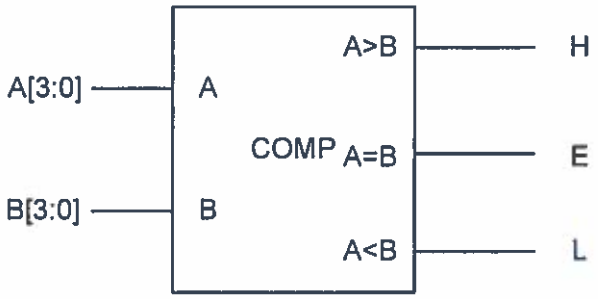

Figure 2.1

c) Show how two of the COMP modules shown in Figure 2.1 can be connected with additional logic gates to perform the comparisons A>B, A=B and A<B for two 8-bit unsigned numbers.

[10]

Question 3

3. Figure 3.1 shows the Mealy state diagram for a finite state machine (FSM) with one input X and one output signal Y.

   a) Draw the state transition table for the FSM.

   [6]

   b) Hence, or otherwise, design a circuit to implement this FSM using two D flip-flops and logic gates. Your design should be in the form of Boolean equations.

   [6]

   c) Determine the minimum number of gates necessary to implement the design of (b).

   [4]

   d) The FSM is to be implemented using a state encoding method known as 'one-hot' encoding, shown in Figure 3.2. In this new method, four D flip-flops and binary code are used to define the states. Re-design the FSM using this new state encoding. Your design should be in the form of Boolean equations.

   [14]

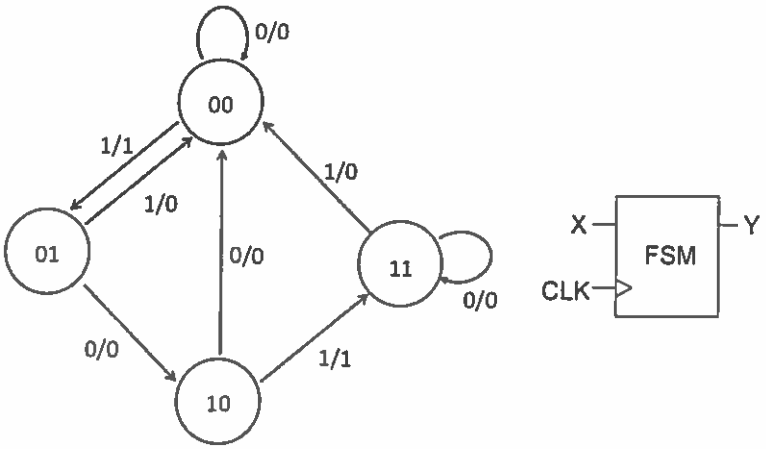

Figure 3.1

Original state encoding	One-hot encoding
00	0001
01	0010
10	0100
11	1000

Figure 3.2

[THE END]