EE3.01 SOLUTIONS

Answers to question 1:

1.a Bookwork
Must Explain
-Bandgap Voltage reference Circuit [2]
-PTAT (proportional to absolute temperature) current generator [2]

b.) Figure 2.a of question is a bandgap voltage reference circuit which has almost zero temperature coefficient, used mainly as stable voltage reference in ICs. For BG reference,

$$-V_{BE1} = V_{BE2} + I_2 R_3 \quad ; \beta \gg 1$$

$$V_{BE1} - V_{BE2} = V_T \ln\left(I_1/I_2\right)$$

$$V_o = V_{BE3} + \left(R_2/R_3\right) V_T \ln\left(I_1/I_2\right) \quad ; V_{BE3} = V_T \ln\left[I_3/I_s\right] \text{ assume room temp}$$

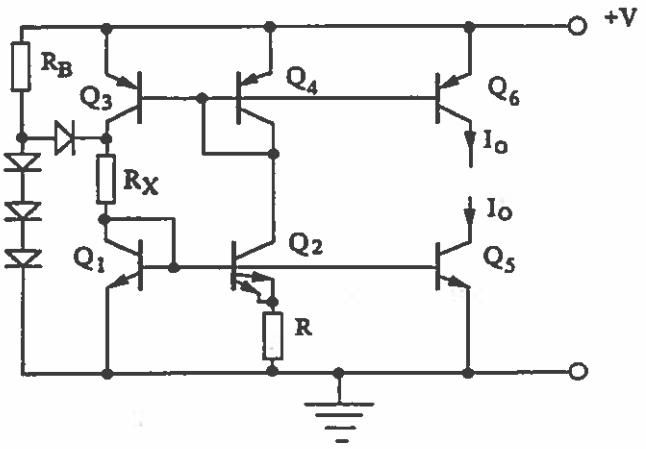
$$For \ \partial V_o/\partial T = 0 \Rightarrow \partial V_{BE3}/\partial T = \frac{V_T}{T}\frac{R_2}{R_3}\ln\left[\frac{I_1}{I_2}\right]$$

$$Since \ \partial V_{BE}/\partial T = -2.5\, mV/^{\circ}C \ and \ \frac{V_T}{T} = \frac{1.38\times10^{-23}}{1.6\times10^{-19}}$$

$$\Rightarrow \left(\frac{R_2}{R_3}\right)\ln\left(\frac{I_1}{I_2}\right) = 29 \Rightarrow V_o = 1.283$$

[7]

c) Self biased PTAT current source with start up circuit.



Drawing of PTAT [5]
Drawing of Startup Circuit [4]

Answers to question 2:

2. a.

$$Av1 = -gm2/(go2+go4)$$

$$(go2+go4) = I_{D2}(\lambda_N + \lambda_p) = 5\times10^{-6}\times0.05 = 2.5\times10^{-7}\Omega^{-1}$$

$$gm2 = 2\sqrt{\beta_2 I_D}$$

$$\beta_2 = \frac{K_N}{2}\left(\frac{W}{L}\right)_2 = 7.5\times10^{-5}A/V$$

$$gm2 = 3.87\times10^{-5}S$$

$$Av1 = -154.9$$

$$Av2 = -gm6/(go7+go6)$$

$$(go7+go6) = I_{D6}(\lambda_N + \lambda_p) = 20\times10^{-6}\times0.05 = 10\times10^{-7}\Omega^{-1}$$

$$gm6 = 2\sqrt{\beta_6 I_{D6}}$$

$$\beta_6 = \frac{K_N}{2}\left(\frac{W}{L}\right)_6 = 1.6\times10^{-4}A/V$$

$$gm6 = 1.13\times10^{-4}S$$

$$Av2 = -113$$

$$A_{total} = Av1\times Av2 = 17503$$

$$G.Bp = gm2/2\pi C_c = 12.32MHz$$

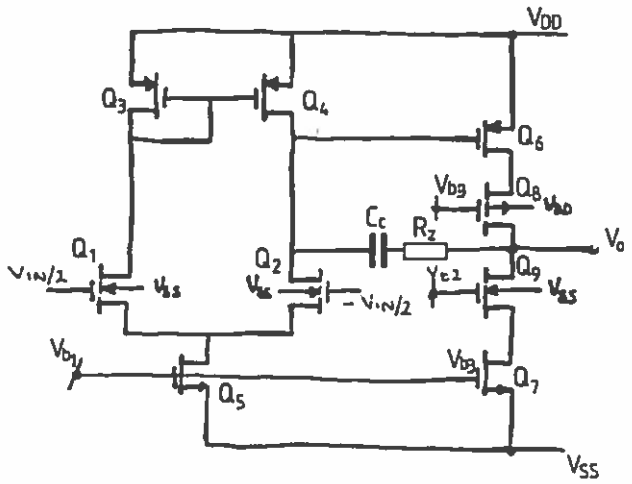
[8]

In a 2-stage opamp the load contributes to the 2nd pole hence reducing load increases stability.
With a single-stage, the load forms the dominant pole hence reducing the load increases bandwidth.

[2]

c.

2. CASCODED OUTPUT



[6]

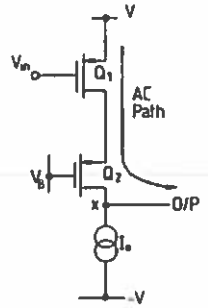
Cascoding output stage increases the output impedance by:

Go=[go6(go8/gm8) +go7(go9/gm9)]
Since Gain of output stage=gm6/[Go]=A_{V2}

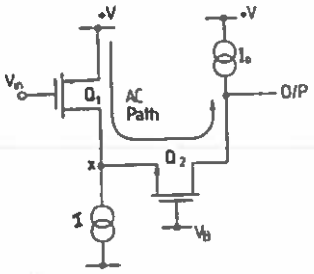
Answers to question 3:

4.a

Concept



Conventional 'stacking' cascode

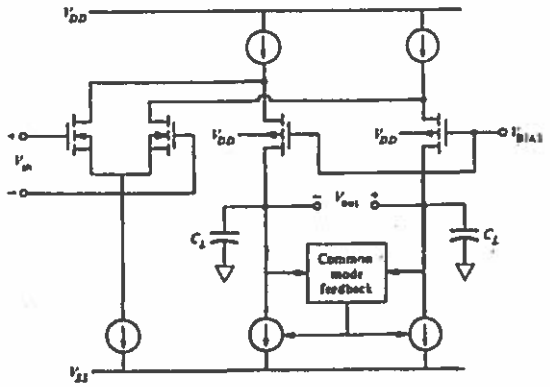


Folded cascode

In the folded cascode we are unstacking the conventional cascode and spreading it out. The AC current path is folded and this allow a reduction in power supply. The conventional cascode requires a 2-stage architecture and since the impedance at (x) is high requires internal compensation. The folded cascode can be used as a single stage architecture, node x is low impedance so the only high impedance node will be at the output.
Gain of the folded cascode Av=gm1/Go.

[4]

b.



[6]

c)

Circuit is a differential continuous time integrator with a balanced double differential linear active transresistor.

$$I_1 = 2\beta[(V_g - V_x - V_T)(V_{in}/2 - V_x) - 1/2(V_{in}/2 - V_x)^2]$$

$$I_2 = 2\beta[(V_g - V_x - V_T)(-V_{in}/2 - V_x) - 1/2(-V_{in}/2 - V_x)^2]$$

$$R = 2V_{in}/(I_1 - I_2)$$

$$R = \frac{1}{\beta(V_g - V_T)}$$

[5]

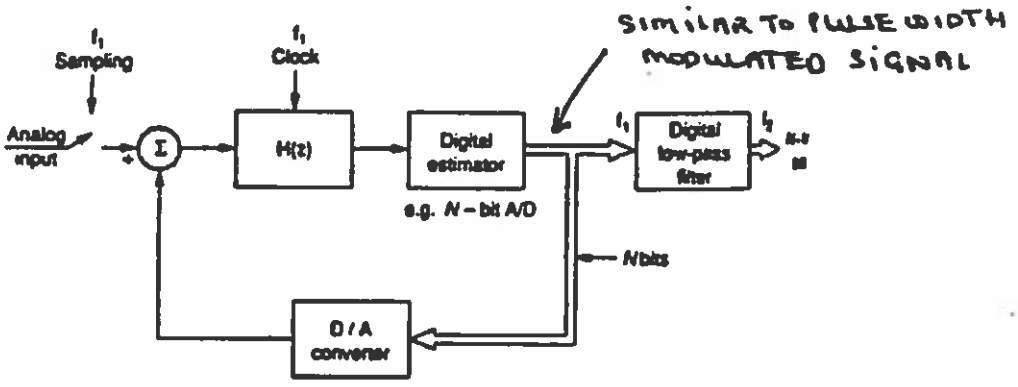
Time constant τ=RC=10ms
R=1/20ux5(1-0.5)=20 KΩ
C=τ/R=10m/20K=5x10^{-7} f

[5]

Answers to question 4:

4.a) Explain sigma delta operation (bookwork).

[5]



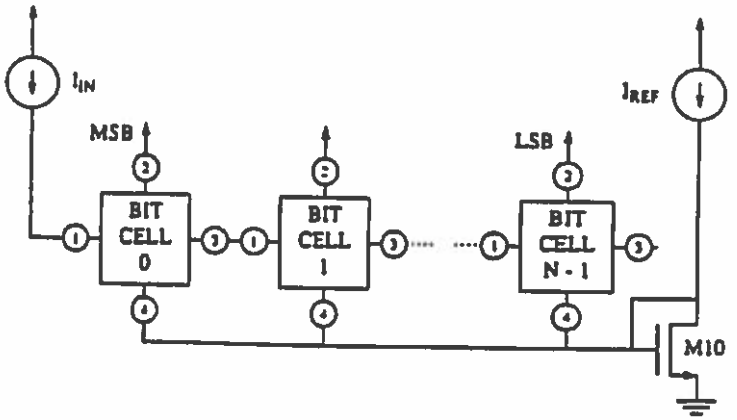
Typical oversampled Σ-Δ (modulator) converter architecture .

[5]

b)(i) Explain how the conversion works (bookwork)

[3]

Draw a cascade of blocks whereby N=8



[4]

c) KT/C noise limits the resolution of a sampled data converter.

DR = 2^N = Vref/Noise= $V_{ref}/\sqrt{(kT.10Rf_C)}$

[3]

Answer to question 5

a)Derivation from notes

Termed "lossy" since only acts as an integrator at high frequency f > f_o

Verify above transfer function?

SOLUTION

$$\Phi_1 \qquad I_{av} = \frac{C_1 V_{IN}}{T}$$

$$\Phi_2 \qquad \frac{-C_1 V_{IN}}{T} = V_O\left[j\omega C_2 + \frac{C_3}{T}\right]$$

Rearranging yields

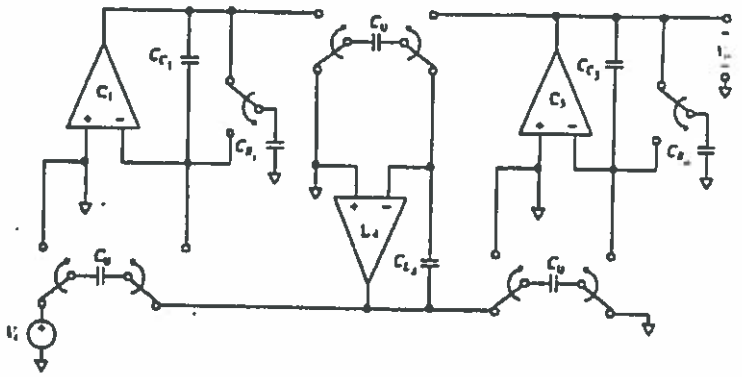
$$\frac{-C_1 V_{IN}}{C_3} = V_O\left[\frac{j\omega C_2 T}{C_3} + 1\right]$$

$$\frac{V_O}{V_{IN}} = -\frac{C_1}{C_3}\frac{1}{\left[1 + \frac{j\omega C_2 T}{C_3}\right]}$$

$$= -\frac{C_1}{C_3}\frac{1}{\left[1 + \frac{jf}{f_o}\right]}$$

Where $$f_o = \frac{1}{2\pi}\frac{C_3}{C_2} f_c$$

b. 3rd-order Chebyshev low pass switched-capacitor ladder filter.



[5]

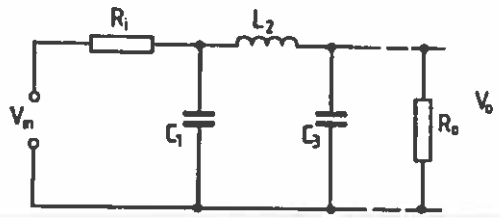
General transformation rules for ladder prototypes:

Inductor: $\frac{f_c L_2}{R_s} = \frac{C_{L2}}{C_u}$

Capacitor: $\frac{C_{c3}}{C_u} = f_c R_s C_3$

Resistor Rs=dummy scalar.

The circuit is equivalent to an RLC prototype



[5]

c. For switched capacitor equivalent:

C_{c1}=Cc3=5.08 pF

C_{L2}=3.49 pF.

C_u=1pF

Assume scaling Rs=Ri=Ro=1Ω

Therefore

L2= CL2/fc= $3.49/100x10^3=3.49x10^{-5}$ H

Normalised 1rad/sec we multiply by $2\pi f_0$

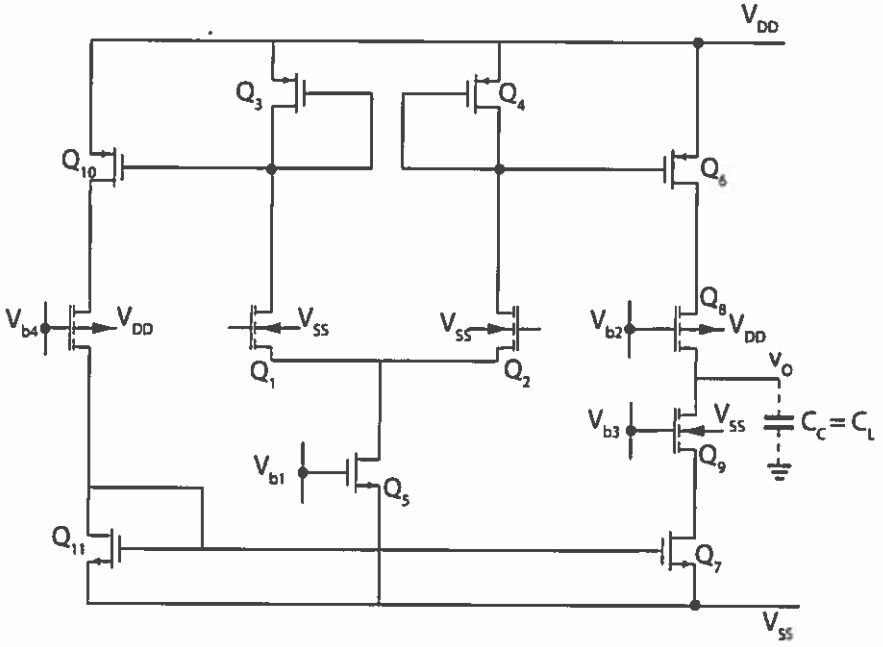
L2=$3.49 x10^{-5}$ x 2π x 5 KHz =1.096 H

C1=C3=Cc3/fc = $5.08/100x10^3$ =$5.08x10^{-5}$ f

Normalised value C1=C3=1.596

Answer to question 6

6. (a) Sketch the circuit of a differential to single ended output high frequency operational amplifier that does not require miller compensation.



[7]

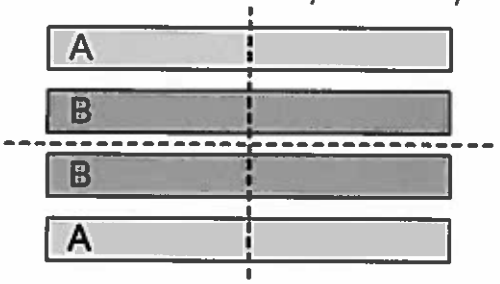
(b) Suggest an enhancement to the circuit in 6.a that would improve the voltage gain of the amplifier and discuss the limitation in doing this.

We can cascade output transistors to increase the output resistance and therefore the gain. This however would limit the output voltage swing.

[3]

(c) When matching transistors special care is taken with the layout. Discuss what is meant by common centroiding when matching two transistors.

Mismatches like λ (the Vds difference), threshold voltage VT and W/L may cause errors in offset and gain. A proper layout may help reduce the effect of such mismatches as well as gradients. Common centroid design splits the transistors over a common centroid or axis of symmetry. For example, the elements A and B in an array may be inter-digitated as in figure below. The input differential pair transistors in the Op-amp are the critical ones for the layout as they affect the offset and gain.



[5]

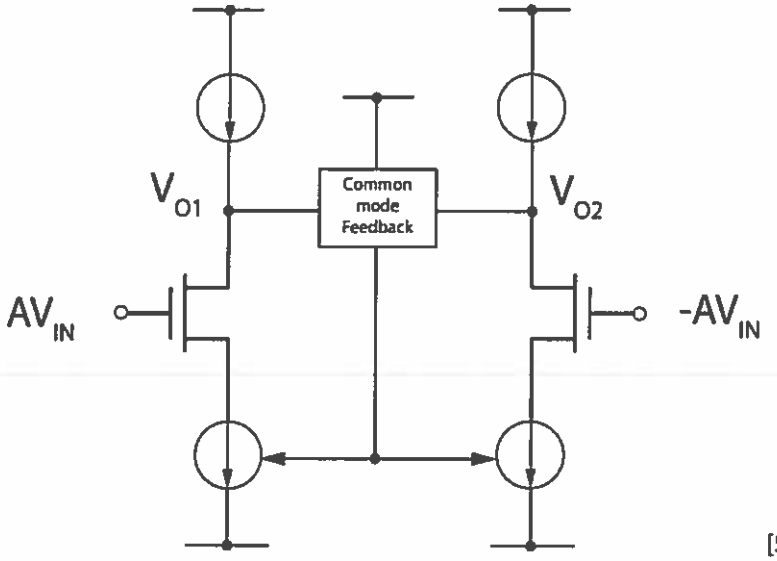
(d) For fully differential output op-amps explain what is meant by common mode feedback.

If an amplifier has a differential output with high gain, the voltages at the outputs are pretty well ill defined and will drift all over the place, usually taking the amplifier out of its high gain region.

We therefore need to sample an output which is "common" to both and stabilise this voltage.

The technique is known as common-mode feedback and we will describe it in slightly more detail when we come on to differential in, differential out, CMOS op-amp architectures.

We will show here how the technique can be used to improve the CMRR of the simple differential amplifier.



[5]