E3.05
ISE3.19

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2005

MSc and EEE/ISE PART III/IV: MEng, BEng and ACGI

Corrected Copy

DIGITAL SYSTEM DESIGN

Wednesday, 4 May 10:00 am

Time allowed: 3:00 hours

There are SEVEN questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : P.Y.K. Cheung
Second Marker(s) : D.M. Brookes

Special instructions for invigilators: None

Information for candidates:

In the figures showing digital circuits, all components have, unless explicitly indicated otherwise, been drawn with their inputs on the left and their outputs on the right. All signals labelled with the same name are connected together. All circuits use positive logic. The least significant bit of a bus signal is labelled as bit 0, and the most significant bit with the highest integer number. Therefore the signal X[7:0] is an eight bit bus with X7 being the MSB and X0 the LSB.

Hexadecimal numbers are prefixed with '$'. For example the decimal number 10 is written as $A.

In questions involving circuit design, you may use any standard digital circuits that are not explicitly forbidden by the question provided that you fully specify their operation.

Marks may be deducted for unnecessarily complex designs unless you are explicitly instructed not to simplify your solution.

1. An 6-tap FIR filter can be described using the difference equation shown in *Equation 1.1*, where y_n is the current output and x_n, x_{n-1}, ..., x_{n-5} are the current and previous five input samples respectively.

$$y_n = 0.25x_n + 1.5x_{n-1} - 0.875x_{n-2} + 0.125x_{n-3} - 0.375x_{n-4} + 0.625x_{n-5} \qquad (1.1)$$

a) Show that *Equation 1.1* can be rewritten as:-

$$y_n = 0.125 \times [(((x_{n-1} - x_{n-2}) \times 2 + (x_{n-1} + x_{n-5})) \times 2 + (x_n - x_{n-4})) \times 2 + (x_{n-2} + x_{n-3} - x_{n-4} + x_{n-5})]$$

[6 marks]

b) Given that all inputs are 8-bit signed integers in 2's complement form and that all inputs are already stored in shift registers, design a circuit to implement this FIR filter using a tree of two-input adders or subtractors. Explain clearly how the adders and subtractors are interconnected in order to ensure that no overflow can occur. Show clearly the width of all the signals in your circuit and the position of the binary point of the output y_n.

[10 marks]

c) The FIR filter in b) is to be implemented on Altera's FLEX10K FPGA with Logic Element (LE) each consisting of a 4-input Lookup Table (LUT) and a register. Assuming that each LE has a worst-case delay of 1ns, and that the register setup time is 1.6ns and clock to output delay is 1.0ns, estimate the highest system clock frequencies achievable using this filter with and without pipelining. State any assumptions made.

[4 marks]

2. The correlation between two 256 × 256 pixel images X and Y can be estimated using sum-of-absolute difference as defined by the following equation:

$$C = \sum_{j=0}^{255} \sum_{i=0}^{255} \left| x_{ij} - y_{ij} \right| \tag{2.1}$$

where x_{ij} and y_{ij} are the 8-bit unsigned intensity value of the pixel at row i and column j of X and Y respectively.

The correlator is to be implemented on an Altera Stratix FPGA which contains Logic Elements (LE), each consisting of a 4-input Lookup Table (LUT) and a register. It also contains three different sizes of block RAMs which can be configured according to *Figure 2.1*. Furthermore, the M512 block is a synchronous memory while the M4K and M-RAM blocks are synchronous dual-port memories.

a) Assuming that X and Y are already stored in memory, design a digital circuit to evaluate the correlation as defined by *Equation 2.1*. The circuit should perform the computation one pixel at a time. You design should show all the building blocks such as memories, adders, counters and multiplexers relating to the datapath. There is no need to show any control circuitry. Do not show the detail gate level circuit.

[12 marks]

b) Estimate the number of LEs and block RAMs needed to implement your design and the number of clock cycles required to complete the computation for each image frame.

[4 marks]

c) A parallel implementation using 256 computation unit is to be employed so that one entire row can be processed in a single clock cycle. Explain how you may use the block RAM efficient to implement such as design.

[4 marks]

M512 RAM Block	M4K RAM Block	M-RAM Block
512 × 1	4K × 1	64K × 8
256 × 2	2K × 2	64K × 9
128 × 4	1K × 4	32K × 16
64 × 8	512 × 8	32K × 18
64 × 9	512 × 9	16K × 32
32 × 16	256 × 16	16K × 36
32 × 18	256 × 18	8K × 64
	128 × 32	8K × 72
	128 × 36	4K × 128
		4K × 144

Figure 2.1

3. Given that x and y are N-bit signed 2's complement numbers and that N is even, a modified Booth encoded multiplier implements the function shown in *Equation 3.1*.

$$y \times x = y \times \sum_{j=0}^{N/2-1} 2^{2j}\left(-2x_{2j+1} + x_{2j} + x_{2j-1}\right) \tag{3.1}$$

where $x_{-1} = 0$, x_i is bit i of the multiplier x for $i \geq 0$, and y is the multiplicand.

Figure 3.1 shows a block diagram of a modified Booth encoded parallel multiplier for N=6 with 3 identical stages. Each stage consists of two modules: the Booth encoder module (BE) and the partial product module (PP). The BE module takes three bits from the multiplier x and performs modified Booth encoding. The PP module calculates $y \times 2^{2j}\left(-2x_{2j+1} + x_{2j} + x_{2j-1}\right)$ for a particular value of j and adds it to the cumulative total.

Figure 3.2 shows the design of the PP module. It consists of six parallel 2-input AND gates, an arithmetic left shifter shown as "<<1", sign-extension blocks depicted as "SX1", a multiplexer and an 8-bit 2's complement adder/subtractor, where the add/subtract control signal S is low for addition and high for subtraction.

a) Draw up the truth table for the three outputs of the BE modules S, D and N, and design the gate level circuit for this module.

[6 marks]

b) Assuming that X = 100001_2 and Y = 001011_2, demonstrate the operation of this multiplier circuit by completing the table of signals of all three PP Modules as shown in *Figure 3.3*. Hence verify that the result produced by the multiplier is correct.

[10 marks]

c) Assume that the delay of any gate, a multiplexer and the clock-to-output delay of a register is 1 ns, and the delay of an k-bit adder is $1.5 \times k$ ns, the setup and hold times of a register are respectively 1ns and 0ns. Determine the worst case delay from any input to any output of the multiplier.

[2 marks]

d) Pipelining can be used between each stage to increase the clock frequency of a system using this multiplier. Estimate the maximum clock frequency that can be used with this pipelined multiplier. State any assumptions made.

[2 marks]

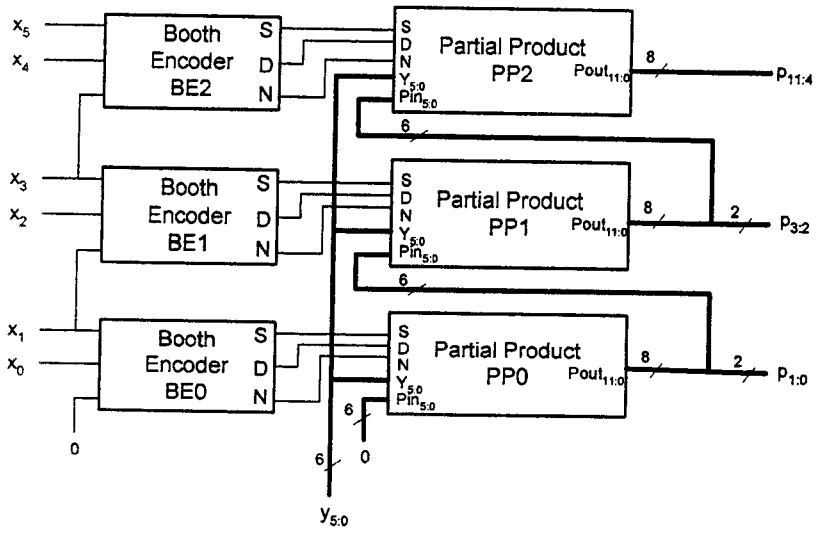

Figure 3.1

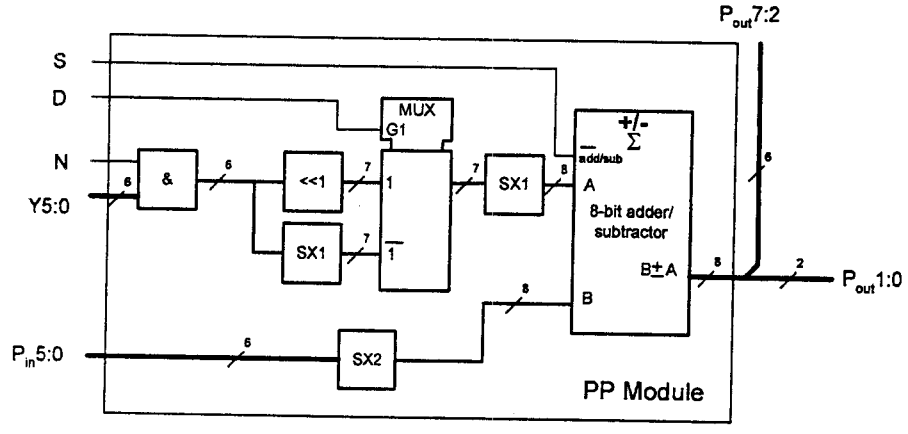

Figure 3.2

	BE0/PP0	BE1/PP1	BE2/PP2
S			
D			
N			
B7:0			
A7:0			
$P_{out}7:0$			

Figure 3.3

4. In a 32-bit microprocessor system shown in *Figure 4.1*, a fast cache memory is used to increase the effective speed of the main memory. The operation of the microprocessor and the memory interface circuit is controlled by the clock signal *CLK*. *Figure 4.2* shows the timing diagram during three different types of memory accesses.

The address bus $A31:2$ becomes valid and the address strobe signal $\overline{AS}$ is asserted in T_0 shortly after the rising edge of CLK. The microprocessor samples the wait signal *WAIT* on the falling edge of CLK the middle of T_1. If $WAIT = 0$, the microprocessor completes the current memory access and proceeds to the next memory operation. However if $WAIT = 1$, the microprocessor inserts a wait cycle and continues to sample *WAIT* on subsequent falling edges of CLK until it becomes 0. During T_0 $\overline{WR}$ is set to low for a write operation and set to high for a read operation.

During a memory read operation, if the data being accessed is stored in cache memory, the cache circuitry asserts *HIT* before the end of T_0 indicating that the data will be available from the cache at the end of T_1. Such a cache read operation takes only 2 clock cycles to complete. However if the data being accessed is not in cache, *HIT* is deasserted before the end of T_0 and data must be read from main memory at the end of T_3. At the same time it is also written to cache by asserting the $\overline{WCACHE}$ signal. Such a main memory read operation takes 4 cycles to complete.

All memory write operations also take 4 cycles to complete at the end of T_3 by asserting $\overline{WMEM}$ and $\overline{WCACHE}$ signals in T_3. Writing to main memory is always accompanied by writing to the cache.

Design, in the form of a state diagram or an ASM chart, a 6 state Moore finite state machine (FSM) that takes as input signals $\overline{AS}$, $\overline{WR}$ and *HIT*, and produces the signals *WAIT*, $\overline{WCACHE}$ and $\overline{WMEM}$.

[20 marks]

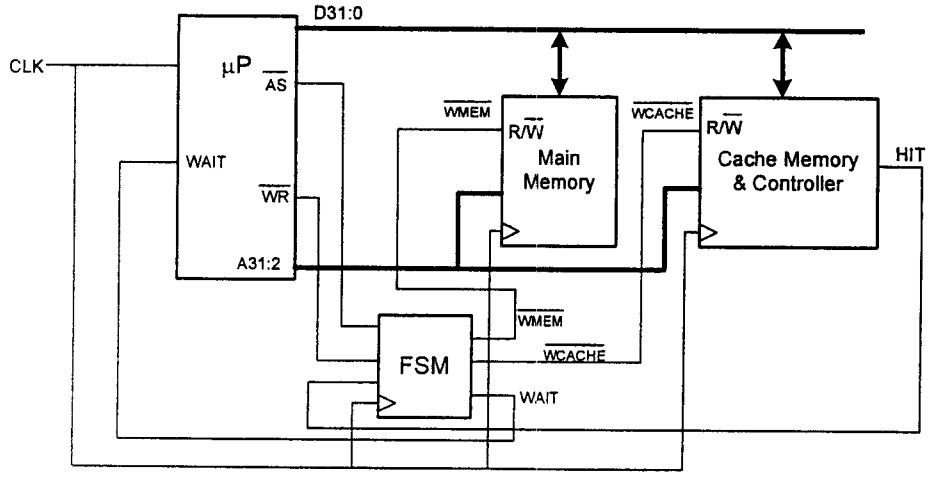

Figure 4.1

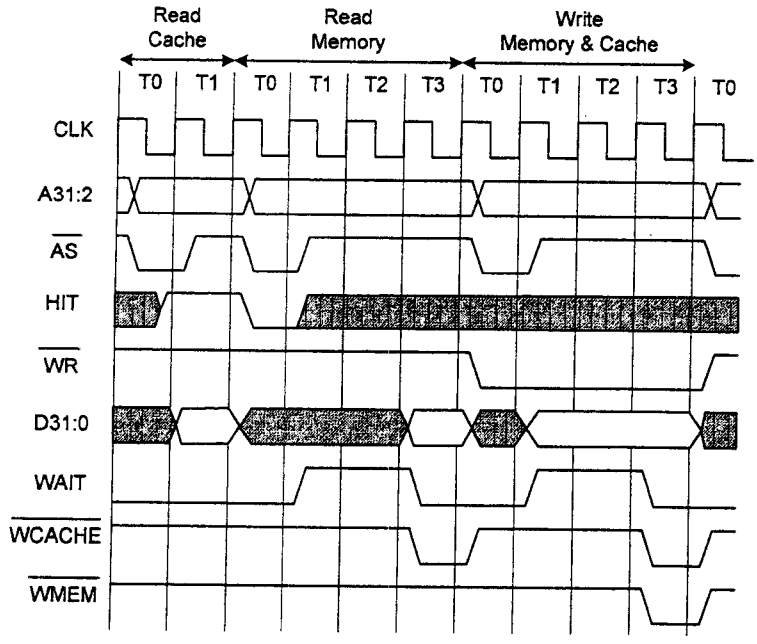
Read Cache
Read Memory
Write Memory & Cache
T0
T1
T0
T1
T2
T3
T0
T1
T2
T3
T0
CLK
A31:2
AS
HIT
WR
D31:0
WAIT
WCACHE
WMEM

Figure 4.2

5. *Figure 5.1* shows the state diagram of a Moore finite state machine (FSM) with 4 inputs and 4 outputs. The FSM is to be implemented using an Altera's FLEX10K FPGA device which contains Logic Elements (LEs) each consisting of a 4-input lookup table (LUT) and a register. It also contains a number of Embedded Array Block (EAB), which can be configured as a 256 × 8 ROM with asynchronous address inputs and registered data outputs.

a) Implement the FSM using one EAB such that the 4 input signals IN3:0 are wired to the least significant bits of the address A[3:0], the 4 output signals OUT3:0 are taken from the least significant bits of the data D[3:0]. Explain why there is no advantage in using one-hot state encoding when implementing the FSM using memory. Determine the content of the EAB.

[10 marks]

b) Re-implement the FSM using only Logic Elements and one-hot state encoding. How many LEs are required to implement the FSM?

[10 marks]

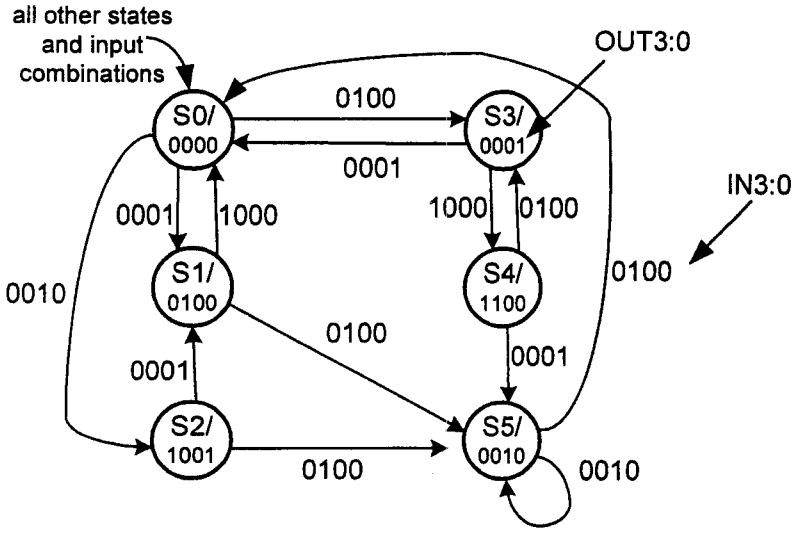

Figure 5.1

6. a) What happens to the output of a digital signal when it goes into metastable state? What are the circumstances under which metastability arises?

[6 marks]

b) *Figure 6.1* shows a circuit to synchronise an asynchronous input A to a synchronous system G. The synchronous system G can operate with a maximum clock frequency of 300 MHz and the input setup time is 2 ns. Flip-flops FF1 and FF2 have a setup time of 2 ns, a hold time of 0 ns, and a clock-to-output delay of 2 ns. Ignoring the possibility of metastability, what is the maximum clock frequency of this circuit?

[2 marks]

c) The mean time between failures (MTBF) of a synchronising flip-flop is given by *Equation 6.1*:

$$MTBF = \frac{e^{t/\tau}}{T_a \times f \times a} \tag{6.1}$$

where t is the maximum duration over which metastability may persist from the time of the clock edge without causing errors, f is the frequency of the clock signal to the synchronizing flip-flop, a is the transition rate of the asynchronous input, and $T_0 = 2\times10^{-11}$ s and $\tau = 0.05$ns for these flip-flops.

Using the maximum clock frequency determined in b), and assuming that the asychronous transition rate is 50MHz, determine the MTBF of FF1.

Explain qualitatively why adding the second flip-flop FF2 improves the overall MTBF of the synchronizer.

[8 marks]

d) *Figure 6.2* shows another synchroniser circuit. Describe with the aid of a timing diagram the relationship between the asynchronous input A and the synchronised output Z.

[4 marks]

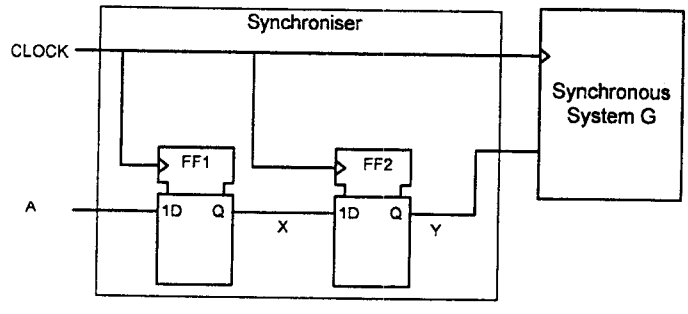

Figure 6.1

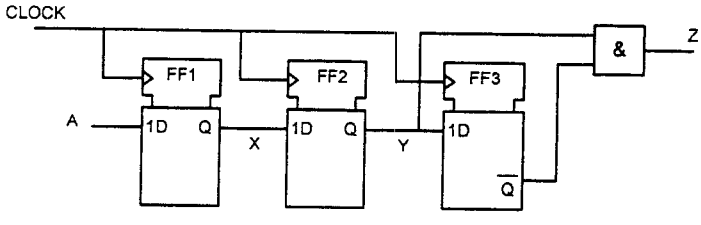

Figure 6.2

7 *Figure 7.1* shows a systolic processing cell consisting of a coefficient register M1, a 2's complement multiplier M2, an adder M3 and two D-type registers M4, M5. The coefficient register is preloaded with a constant value a_i.

Figure 7.2 shows three such cells connected together to form a linear array of 3 cells. An input sample X is supplied on each clock cycle of signal CLK to the P_{in} input of the left-most cell. The array output Y and Z are taken from the A_{out} and P_{out} outputs of the right-most cell respectively. a_3 is a constant value supplied to the A_{in} input of the left-most cell. The constant values stored in each systolic cell, counting from left to right, are a_2, a_1 and a_0 respectively.

a) During clock cycle n, the input and outputs of the array are X(n), Y(n) and Z(n) respectively. Deduce a relationship between the input X at time n–3 and the outputs Y and Z at time n. Draw a timing diagram to illustrate you're answer.

[12 marks]

b) Hence or otherwise, state a general relationship between Y and X for a linear array of M cells.

[4 marks]

c) Assuming that X driven by a D-type register and that the delays of the circuit elements inside the systolic processing cells are: multipliers 10ns, adder 5ns, register (clock to output) 1ns, registers setup time 1ns, register hold time 0ns. What is the maximum operating frequency of such a linear array with M cells?

[4 marks]

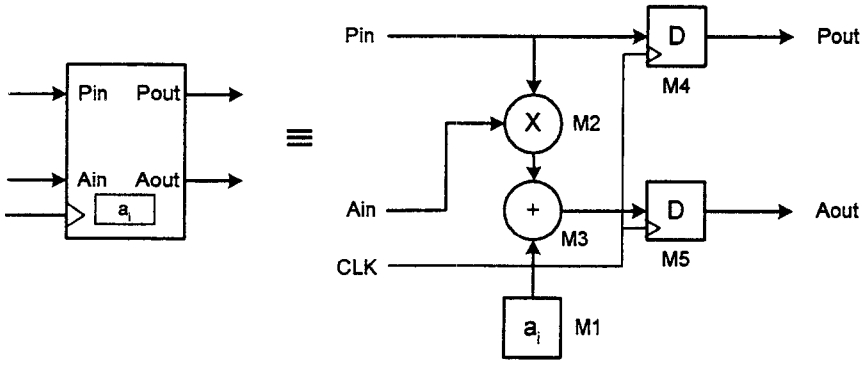

Figure 7.1

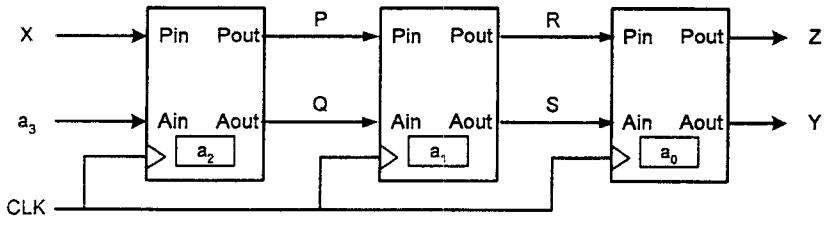

Figure 7.2

[END]

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DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
M.Eng., B.Eng., B.Sc(Eng.) and A.C.G.I. EXAMINATIONS 2005

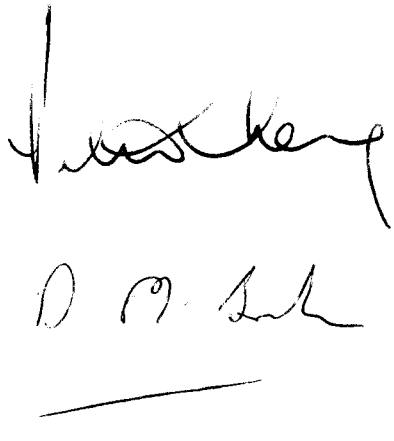
PART III and PART IV

DIGITAL SYSTEM DESIGN

SOLUTIONS

First Marker: *Peter Y. K. Cheung*

Second Marker: *Mike Brookes*



Answer to Question 1

This question tests students' ability to system level circuit which involves arithmetic circuits and to determine the word-length appropriate to such a circuit.

a) The first step is to factorise the equation with 0.125:

$$y_n = 0.125 \times [2x_n + 12x_{n-1} - 7x_{n-2} + x_{n-3} - 3x_{n-4} + 5x_{n-5}]$$
$$= 0.125 \times [2x_n + 12x_{n-1} - 8x_{n-2} + x_{n-2} + x_{n-3} - 3x_{n-4} + 5x_{n-5}]$$

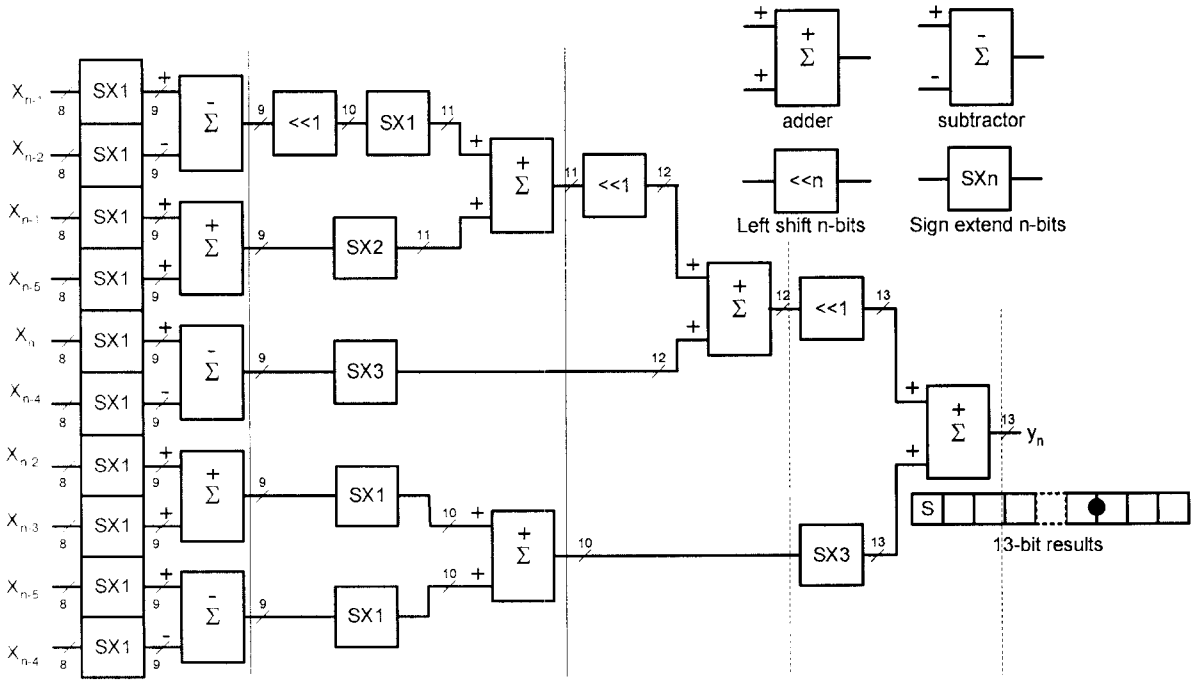
The coefficient for x_{n-2} is written as (-8+1) in order to minimize the number of '1' bit in the multiplication operations.

From this equation, the following table can be drawn up:

Sample	Coeff	Sign	B3	B2	B1	B0
x_n	0.35	+	0	0	1	0
x_{n-1}	1.5	+	1	1	0	0
x_{n-2}	-0.875	-	1	0	0	0
x_{n-3}	0.125	+	0	0	0	1
x_{n-4}	-0.375	-	0	0	1	1
x_{n-5}	0.625	+	0	1	0	1

[6 marks]

b) Note that <<n and SXn modules do not require hardware.



[10 marks]

c) Assuming that routine delay is negligible and that pipeline stages are added as shown at the vertical lines, the worst-case delay is incur by the output adder stage:

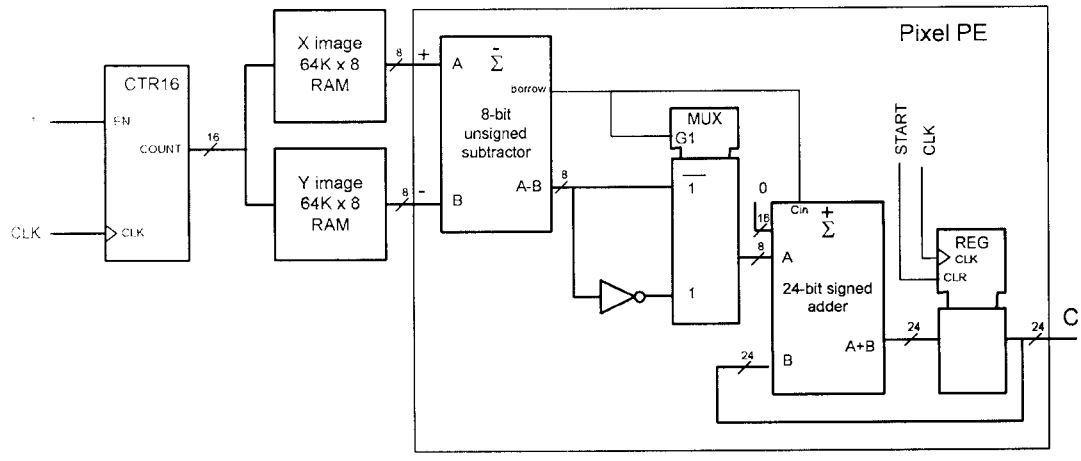
No pipeline: $t_d = (9+11+12+13) \times t_{LUT} = 45ns$. $f_{max} = 22MHz$.

$t_d = 13 \times t_{LUT} + t_{setup} + t_{ck-q} = 15.6ns$. $f_{max} = 64.1MHz$.

[4 marks]

Answer to Question 2

a)



[12 marks]

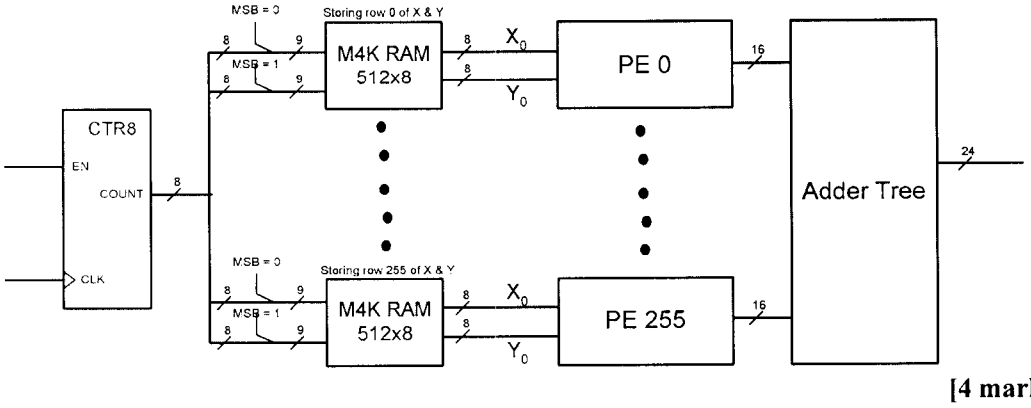
b)

Block	LE	Block
Counter	16	-
Image memory	-	2 x M-RAM
Subtractor	8	-
MUX + inv	8	-
Adder + Reg	24	-
Total	56	2 x M-RAM

Requires 65536 clock cycles.

[4 marks]

c) Best solution is to use 256 x M4K RAM, each storing one row of X and Y. Using the dual-port feature of M4K Block RAM, and by setting MSB of X and Y addresses to be 0 and 1 respectively, both images can be accessed simultaneously without conflict. Design is now (not required for full marks).

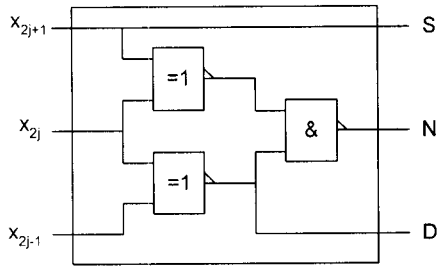


[4 marks]

Answer to Question 3

a)

x_{2j+1}	x_{2j}	x_{2j-1}	S	D	N	Action
0	0	0	0	0	0	0
0	0	1	0	0	1	y
0	1	0	0	0	1	y
0	1	1	0	1	1	2y
1	0	0	1	1	1	-2y
1	0	1	1	0	1	-y
1	1	0	1	0	1	-y
1	1	1	0	0	0	0



[6 marks]

b) Multiplicant (Y) = +11 = 001011 (bin)

Multiplier (X) = -31 = 100001 (bin)

01 (0) - processed by BE0/PP0
000 - processed by BE1/PP1
100 - processed by BE2/PP2

It would be easier if we enumerate all the relevant signals as shown here:

	BE0/PP0	BE1/PP1	BE2/PP2
x_{2j+1}	0	0	1
x_{2j}	1	0	0
x_{2j-1}	0	0	0
$(-2x_{2j+1} + x_{2j} + x_{2j-1})$	×1	×0	×−2
S	0	0	1
D	0	0	1
N	1	0	1
P_{in}5:0	$00	$02	$00
B	$00	$02	$00
A	$0B	$00	$16
P_{out}7:0	$0B	$02	$EA

[10 marks]

c) X -> N delay in BE = 2 ns.
Worst case delay in PP0 is N to Pout = (1+1+1.5x8) ns = 14ns. Therefore, X -> Pout delay = 16 ns.
Worst case delay in PP1&2, Pin to Pout = 12 ns.
Worst case delay from x0 to Pout = 16 + 12 + 12 = 40 ns.

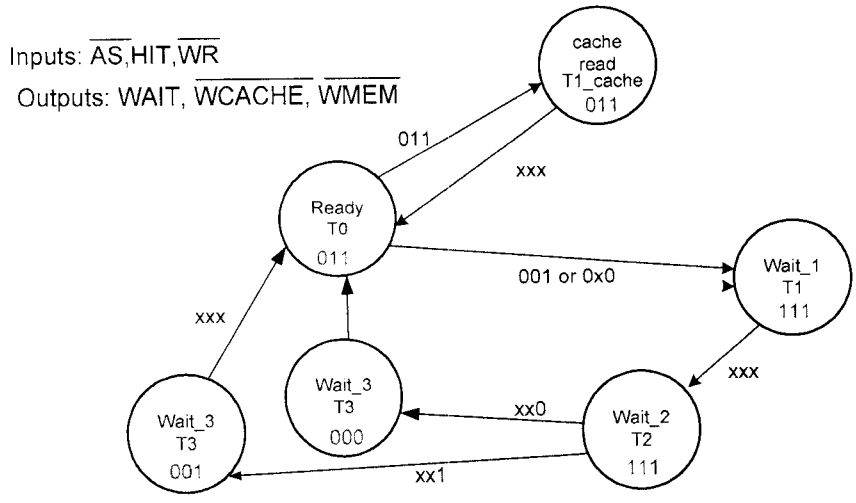
[2 marks]

d) Assumption: register at input and output of multiplier.
Pipeline register inserted between stages, must include setup and clk-> output delay time, then t_{min} (pipelined) = 14 + 1 + 1= 16 ns, f_{max}(pipelined) = 62.5MHz.

[2 marks]

Answer to Question 4

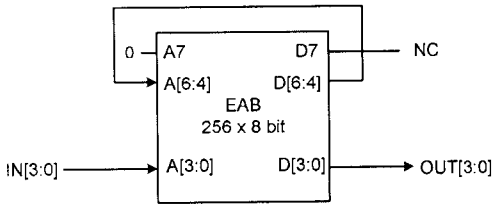
The Moore state machine.



[20 marks]

Answer to Question 5

a) Connect the EAB as shown here. Remember that the output D[7:0] are registered. Therefore contents of ROM must reflect the next state and NEXT OUTPUT.



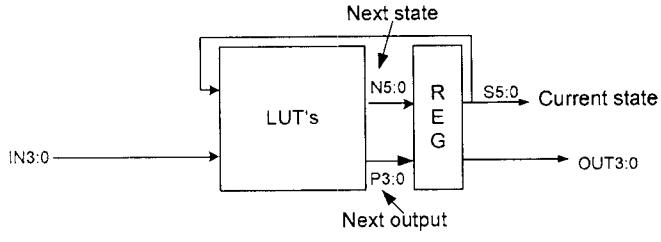
Contents of ROM:

current state A[6:4]	Input A[3:0]	next state D[6:4]	Next output D[3:0]
000	0001	001	0100
000	0010	010	1001
000	0100	011	0001
001	1000	000	0000
001	0100	101	0010
010	0001	001	0100
010	0100	101	0010
011	0001	001	0100
011	1000	100	1100
100	0001	101	0010
100	0100	011	0001
101	0010	101	0010
101	0101	000	0000

D7 of all location contain 0 (could be 1). All other locations contain 00000000. This ensures that ALL illegal state and illegal inputs will force next state to be state 0.

[10 marks]

b) 6 states, therefore 6 FF for one-hot encoding, each representing one state. Assume 000001 for S0, 000010 for S1,….. , 100000 for S5. Note that the inputs are also one-hot! Therefore the next state logic can be written down straight from the state transition table. Must be careful with outputs. To match the EAB implementation, must register the output. Therefore P3:0 are next outputs!



N1 = S0*IN0 + S2*IN0
N2 = S0*IN1
N3 = S0*IN2 + S4*IN2
N4 = S3*IN3
N5 = S1*IN2 + S2*IN2 + S4*IN0 + S5*IN1
N0 = !(N1+N2+N3+N4+N5)

P0 = N2 + N3 = S0*IN1 + S0*IN2 + S4*IN2 (These are next outputs)
P1 = N5 = S1*IN2 + S2*IN2 + S4*IN0 + S5*IN1
P2 = N1 + N4 = S0*IN0 + S2*IN0 + S3*IN3
P3 = N2 + N4 = S0*IN1 + S3*IN3

One LE can implement any arbitrary logic with 4 input variables. Therefore, N1, N2, N3, N4, P0, P3 require only 1 LE. N0, N5, P1 and P2 require 2 LEs. Therefore total number of LE used = 6 + 8 = 14.

[10 marks]

Answer to Question 6

a) When an output of digital circuit is in metastable state, the logic level in undefined and the time for this signal to exit metastable state and acquire either a logic '0' or '1' level is also not known.

Metastability can occur whenever a signal is sampled in a clock domain that is asynchronous to it. It occurs when the transition of this asynchronous signal violate the setup and/or hold time of the flip-flop in the new clock domain.

[6 marks]

b) Synchroniser imposes a maximum of clock period of (2 + 2) ns. Therefore maximum clock frequency is 250MHz, which is lower than maximum frequency that G can operate in.

[2 marks]

c) Since the synchronizer is operating at 250MHz, the available time for metastability to settle is $(t_{period} - t_{setup})$ ns = 2 ns. For FF1:

$$\text{MTBF (2ns)} = \exp(2/0.05) / (2\text{x}10^{-11} \text{ x } 250 \text{ x } 10^{6} \text{ x } 5 \text{ x } 10^{7})$$
$$= 0.94 \text{ x } 10^{38} \text{ sec.}$$

[6 marks]

Adding FF2 provides an additional window over which the signal has a chance to settle. However, the probability of FF2 going into metastability is much harder to calculate because its input X is no longer asynchronous. If the MTBF of FF2 is MTBF2, the overall probability of failure is the produce of the two.

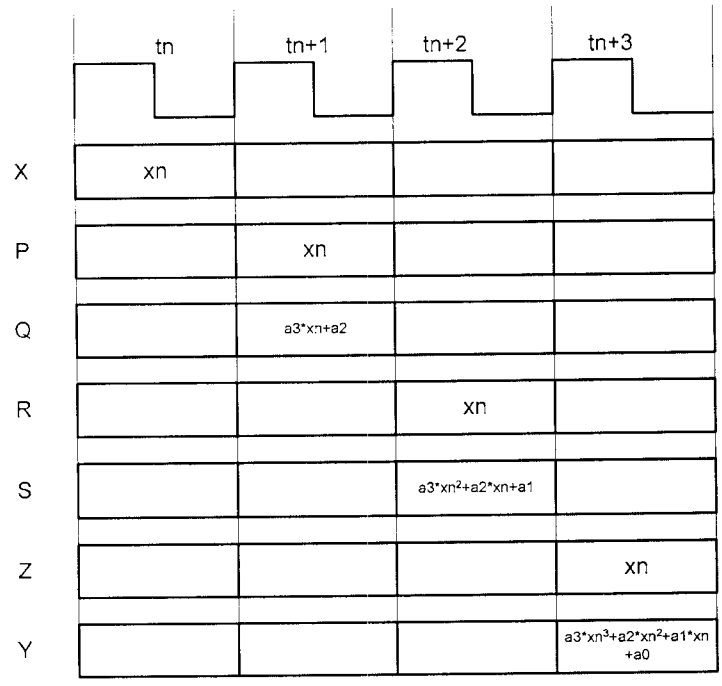
[2 marks]

d) The circuit is an edge-detecting synchroniser which detects a rising edge in A and generate a one clock period positive pulse at Z.

[4 marks]

Answer to Question 7

a)



The relationship is:

$Y_{n+3} = a_3 \times x_n^3 + a_2 \times x_n^2 + a_1 \times x_n + a_0$ (three cycles later)

$Z_{n+3} = x_n$ (three cycles later)

[12 marks]

b) $Y_{n+M} = a_M \times x_n^M + a_{M-1} \times x_n^{M-1} + \ldots + a_2 \times x_n^2 + a_1 \times x_n + a_0$ (M cycles delay)

[4 marks]

c) Worse case delay

Clock → Pin → M2 → M3 → M5setup

= 1 + 10 + 5 +1 ns = 17 ns.

Therefore Max frequency = 58.8 MHz for **any** value of N.

[4 marks]

[END]