TÉCNICO LISBOA

BATCHARGERctr

Datasheet

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Dec 2024

Version 1.0

Revision history

Version	Date	Description
1v0	Dec 2024	First version of charger controller block

Contents

1 General description

The controller block is a digital block located to the left of the power block. It is responsible for setting the appropriate operating mode of the power block and managing the monitors used by the ADC to maximize energy efficiency. Based on the digital words for battery temperature, voltage, and current provided by the ADC, the controller selects the appropriate mode and enables the necessary monitors. The controller halts the process if the temperature becomes dangerously high or low.

2 Block Diagram

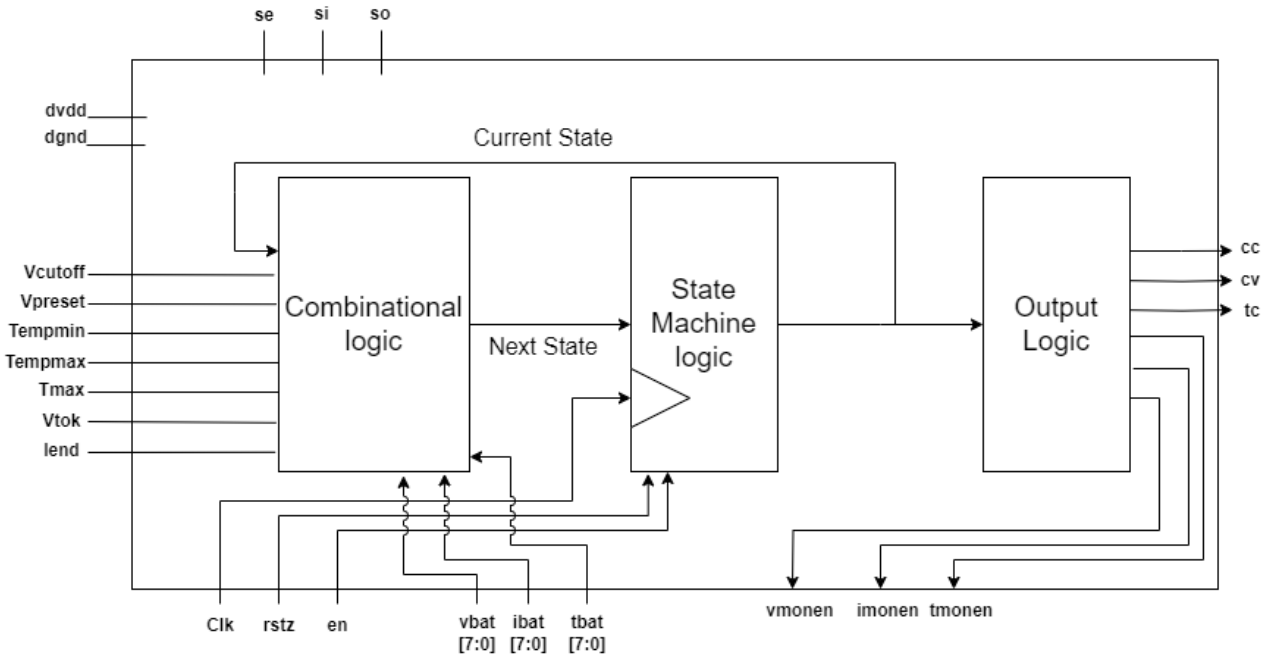

Figure 1: Block Diagram of the controller block

3 Pinning

Pin	Type	Dir	Supply	Description
dvdd	Power	I/O	-	Digital logic supply
dgnd	Power	I/O	dvdd	Digital logic ground
vcutoff [7:0]	Digital	I	dvdd	Voltage threshold for exiting trickle mode (constant from OTP)
vpreset[7:0]	Digital	I	dvdd	Voltage for constant voltage mode (constant from OTP)
tempmin[7:0]	Digital	I	dvdd	Minimum temperature of the charger (constant from OTP)
tempmax[7:0]	Digital	I	dvdd	Maximum temperature of the charger (constant from OTP)
tmax[7:0]	Digital	I	dvdd	Maximum charge time (constant from OTP - units of 255 clock periods).
vtok	Digital	I	dvdd	Signals that voltage and temperature are valid
iend[7:0]	Digital	I	dvdd	Charge current to be use as "end charging" end criteria of the trickle current mode
clk	Digital	I	dvdd	Clock signal. The controller operates with a negedge clock
rstz	Digital	I	dvdd	Reset of the controller. The controller is reseted when rstz=1'b0
en	Digital	I	dvdd	Enable of the controller. It is enable when en=1'b1.
vbat[7:0]	Digital	I	dvdd	Battery voltage from ADC defined as vbat = adc(vref=0.5V, battery_voltage /10)
ibat[7:0]	Digital	I	dvdd	Battery current from ADC defined as ibat = adc(vref=0.5V, battery_current * Rsens); Rsens = 1/C ; C=nominal capacity of battery
tbat[7:0]	Digital	I	dvdd	Battery temperature from ADC defined as tbat = adc(vref=0,5, vadc); vadc = Temp/330 + 20/165
vmonen	Digital	O	dvdd	Enables voltage monitor of the ADC
imonen	Digital	O	dvdd	Enables current monitor of the ADC
tmonen	Digital	O	dvdd	Enables temperature monitor of the ADC
tc	Digital	O	dvdd	Signals the power block to enter trickle current mode
cv	Digital	O	dvdd	Signals the power block to enter contant voltage mode
cc	Digital	O	dvdd	Signals the power block to enter constant current mode
so	Digital	O	dvdd	Scan output
si	Digital	I	dvdd	Scan input
se	Digital	I	dvdd	Scan enable

4 Detailed description

The controller block operates on the negative edge of the clock and functions only when the signals *en*, *vtok*, and *rstz* are active (logic high). This controller has five states and is responsible for selecting the three possible modes of operation (CC, CV, and TC) for the charger's power block. Additionally, it selects which monitors (temperature, voltage, or current) are activated by the ADC. At any given time, only one of the signals *cc*, *cv*, or *tc* can be active. This controller is based on the CC/CV algorithm. In every state, the system checks the temperature to ensure it operates within safe limits and avoids overheating. The flowchart of the system is presented in Fig.2.

4.1 Start and wait states

In the start state, the controller verifies whether it is safe for the charger to operate. It begins by checking the temperature from the ADC to ensure that it is within the safe operating range. If the temperature is too high or too low, the controller transitions to the wait state, where the charger remains idle until the system either cools down or heats up to acceptable levels.

Next, the controller checks the battery voltage. If the voltage is not lower than 4.2V, the battery is already fully charged, and the operation can terminate. If the battery voltage is very low ($V_{bat} \leq V_{cutoff}$), the controller enters the trickle current (TC) mode. Otherwise, it transitions to the constant current (CC) mode. In both the start and wait states, only the temperature and voltage monitors are active, and no mode signals (*cc*, *cv*, or *tc*) are asserted.

4.2 Trickle current state

The trickle current mode is used to recover a battery that is in a deeply discharged state. In this mode, the signal *tc* is asserted (`1'b1`), signaling the power block to charge the battery with a small current. If the system begins to overheat, it transitions to the wait state to allow the system to cool down. Once the battery voltage reaches the cutoff voltage (V_{cutoff}), the controller transitions to the constant current (CC) state, and the signal *tc* is deasserted (`1'b0`). During this mode, only the temperature and voltage monitors are active.

4.3 Constant current state

The constant current mode is typically used during the initial phase of the charging process. In this mode, the signal *cc* is asserted, signaling the power block to charge the battery with a higher current compared to the trickle current mode. As the battery charges, its voltage rises. When the battery voltage reaches the preset voltage (V_{preset}), the controller transitions to the constant voltage (CV) mode. During this mode, only the temperature and voltage monitors are active.

4.4 Constant voltage state

The constant voltage mode is typically used during the final phase of the charging process. In this state, the signal *cv* is asserted, signaling the power block to charge the battery at a

constant voltage of 4.2V while gradually reducing the charging current as the battery approaches full charge. The charging process is terminated when either the charging current drops below the minimum threshold (I_{end}) or the maximum charging time (T_{max}) is reached. At this point, the system transitions to the end state. During the constant voltage mode, only the current monitor is active.

4.5 End state

In the end state, the battery has completed the charging process. However, if the battery becomes discharged over time, the controller will automatically restart the charging process based on the conditions defined in the start state.

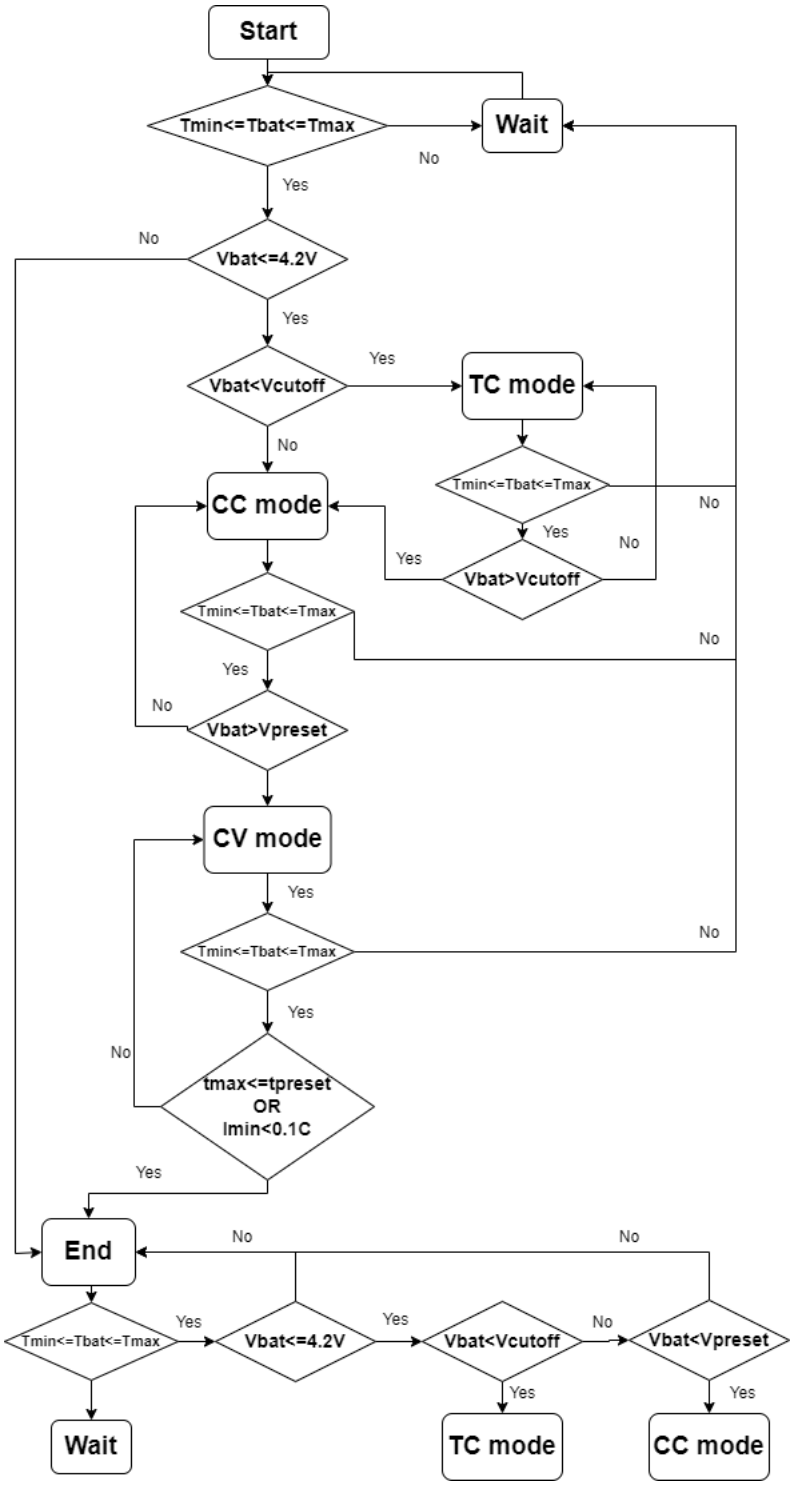

Figure 2: Flow Chart of the controller block

5 Characteristics

Parameter	Min	Typ	Max	Unit
Voltage at pin dvdd	1.8	4.5	5	V
Clock	1	10	-	ns

6 Assembly guidelines

Pin	Recomendation
dvdd	Consider as noisy supply signal
dgnd	Consider as noisy supply signal
vcutoff [7:0]	Digital signal. No special recommendation
vpreset[7:0]	Digital signal. No special recommendation
tempmin[7:0]	Digital signal. No special recommendation
tempmax[7:0]	Digital signal. No special recommendation
tmax[7:0]	Digital signal. No special recommendation
vtok	Digital signal. No special recommendation
iend[7:0]	Digital signal. No special recommendation
clk	Use controlled routing to maintain integrity and minimize jitter
rstz	Digital signal. No special recommendation
en	Digital signal. No special recommendation
vbat[7:0]	Digital signal. No special recommendation
ibat[7:0]	Digital signal. No special recommendation
tbat[7:0]	Digital signal. No special recommendation
vmonen	Digital signal. No special recommendation
imonen	Digital signal. No special recommendation
tmonen	Digital signal. No special recommendation
tc	Digital signal. No special recommendation
cv	Digital signal. No special recommendation
cc	Digital signal. No special recommendation
so	Digital signal. No special recommendation
si	Digital signal. No special recommendation
se	Digital signal. No special recommendation

7 Testing

The scan test can be performed on this controller. The pins *so*, *si*, and *se* are the scan output, the scan input, and the scan enable, respectively.