

Pontifícia Universidade Católica de Minas Gerais



PUC Minas

Relatório III Arquitetura de Computadores

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Professor Romanelli Lodron
Horário Seg - 07:00-08:30

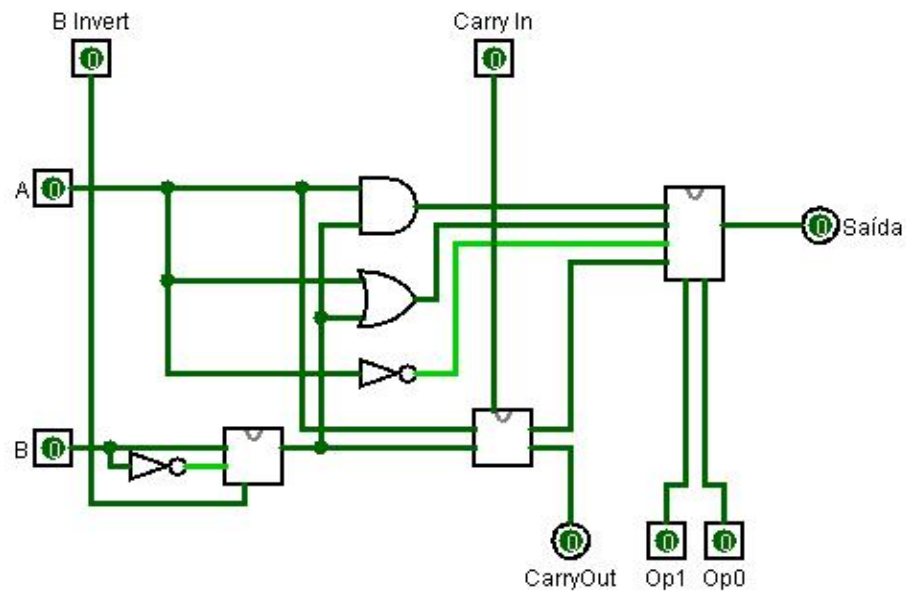
Belo Horizonte, 06 de Março de 2017

Conteúdo

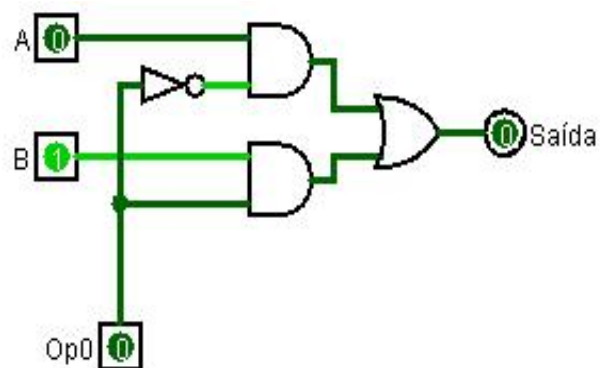
1	Parte I - Estudo da ALU e MUX	1
2	Parte II - Montagem Simulador 97	3

1 Parte I - Estudo da ALU e MUX

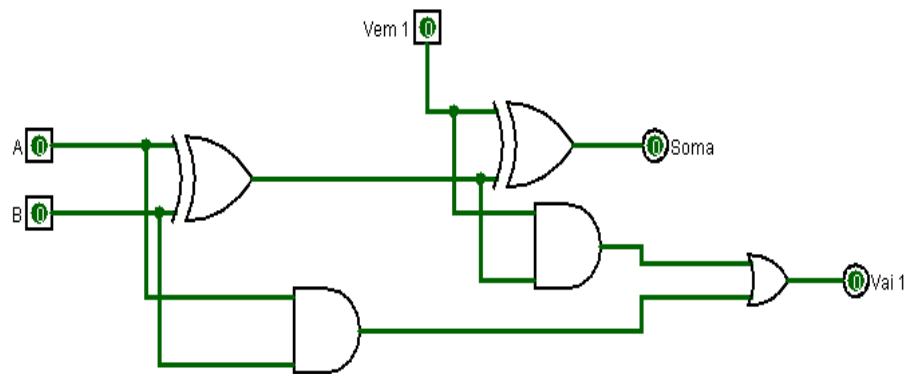
ULA 1bit realizada no Logisim.



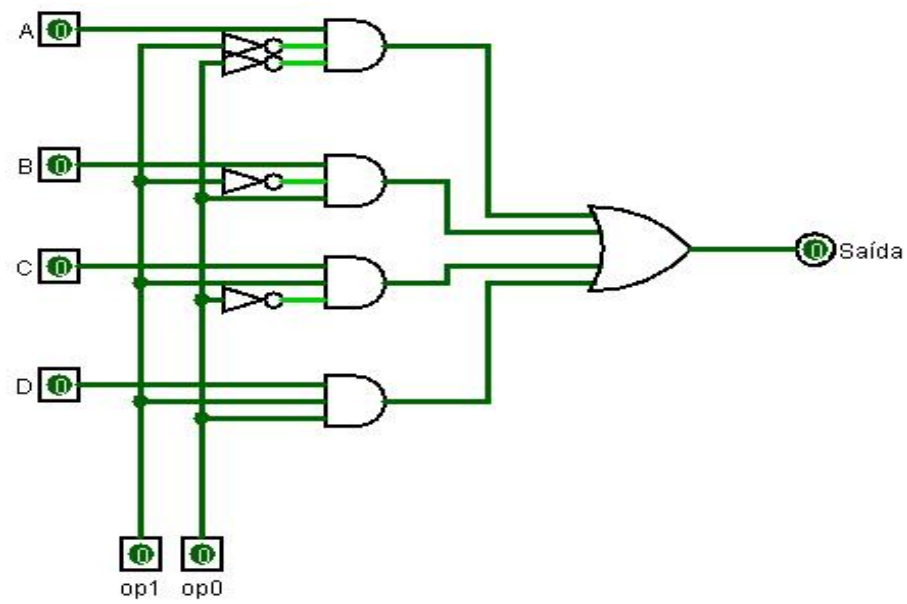
Multiplexador de 1 bit utilizado no BInvert



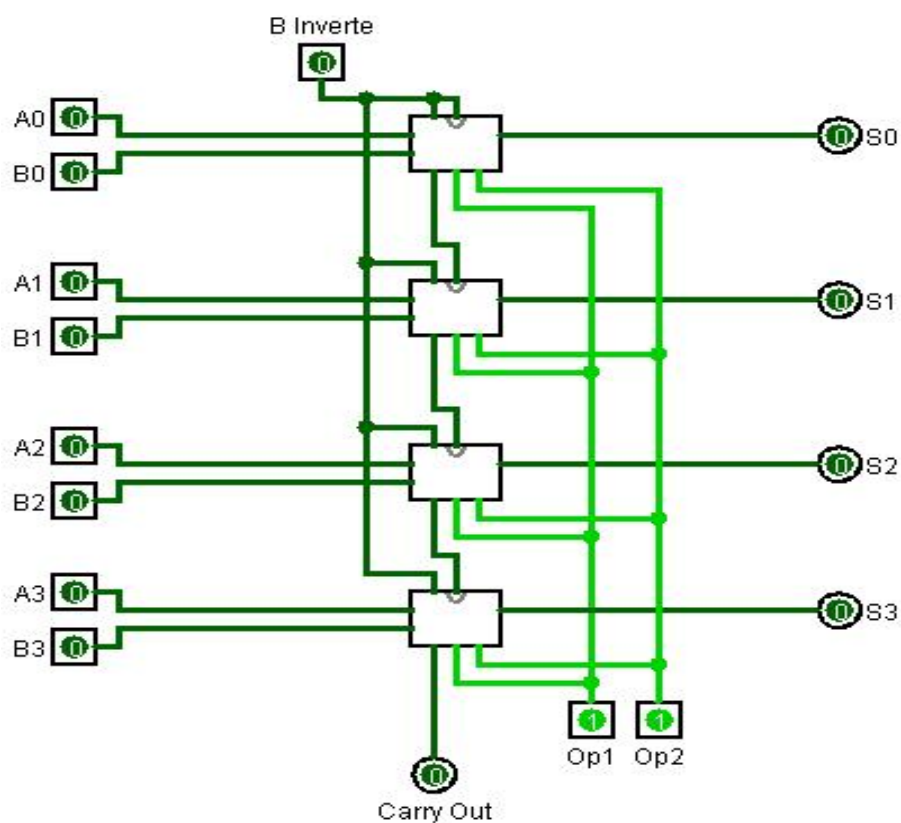
Somador Completo de 1 bit utilizado na ULA



Multiplexador de 2 bits que determinará as operações da ULA



ULA de 4bits realizada no Logisim.



2 Parte II - Montagem Simulador 97

Tabela verdade adotada no projeto da ULA.

A	B	OP1	OP0	S	Saída Real
0	0	0	0	0	0
0	0	0	1	0	
0	0	1	0	1	~OP0
0	0	1	1	0	
0	1	0	0	0	OP0
0	1	0	1	1	
0	1	1	0	1	1
0	1	1	1	1	
1	0	0	0	0	OP0
1	0	0	1	1	
1	0	1	0	0	OP0
1	0	1	1	1	
1	1	0	0	1	1
1	1	0	1	1	
1	1	1	0	0	0
1	1	1	1	0	

Testes Realizados no Simulador 097

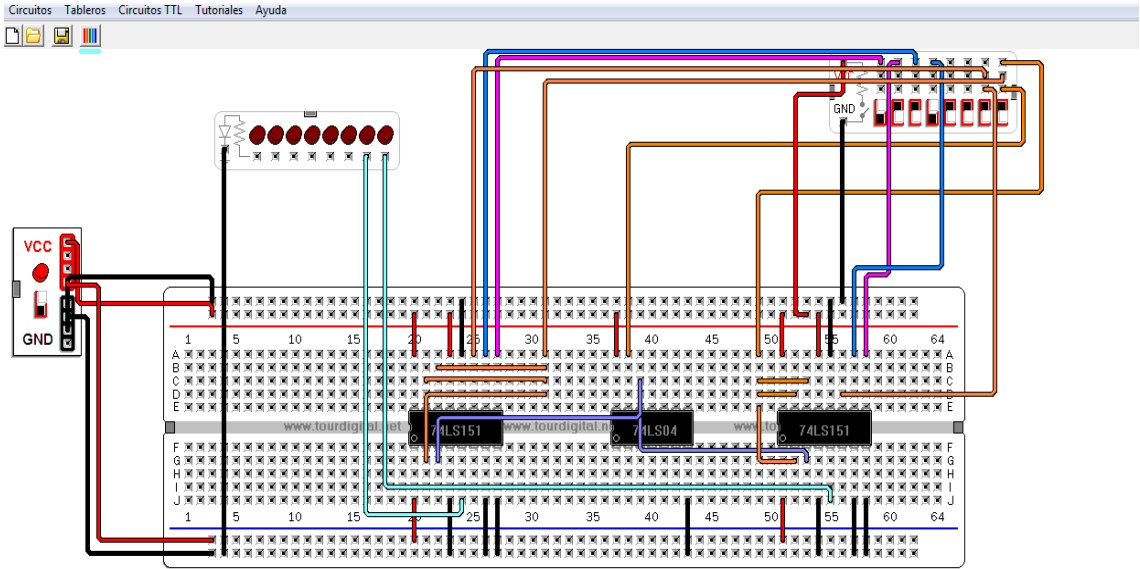


Figura 1: Teste 1 - AND(A,B)

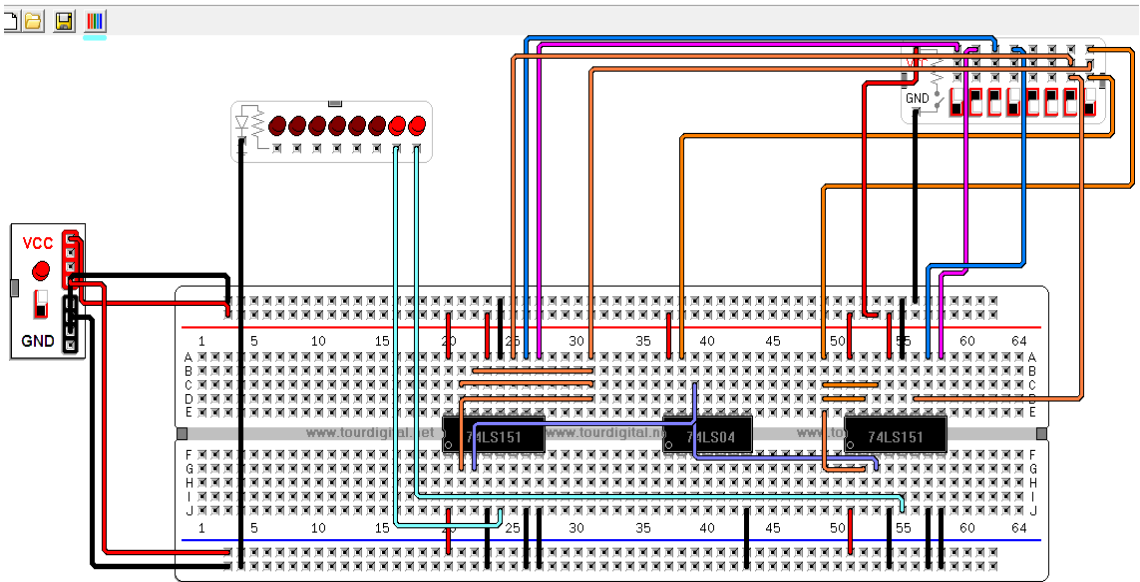


Figura 2: Teste 2 - OR(A,B)

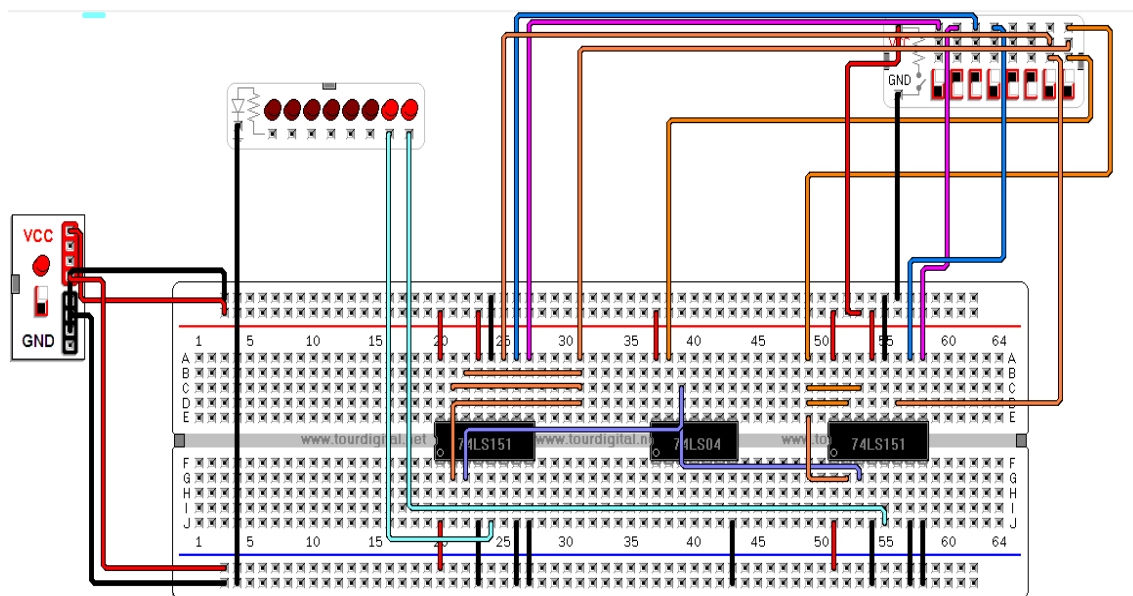


Figura 3: Teste 3 - SOMA(A,B)

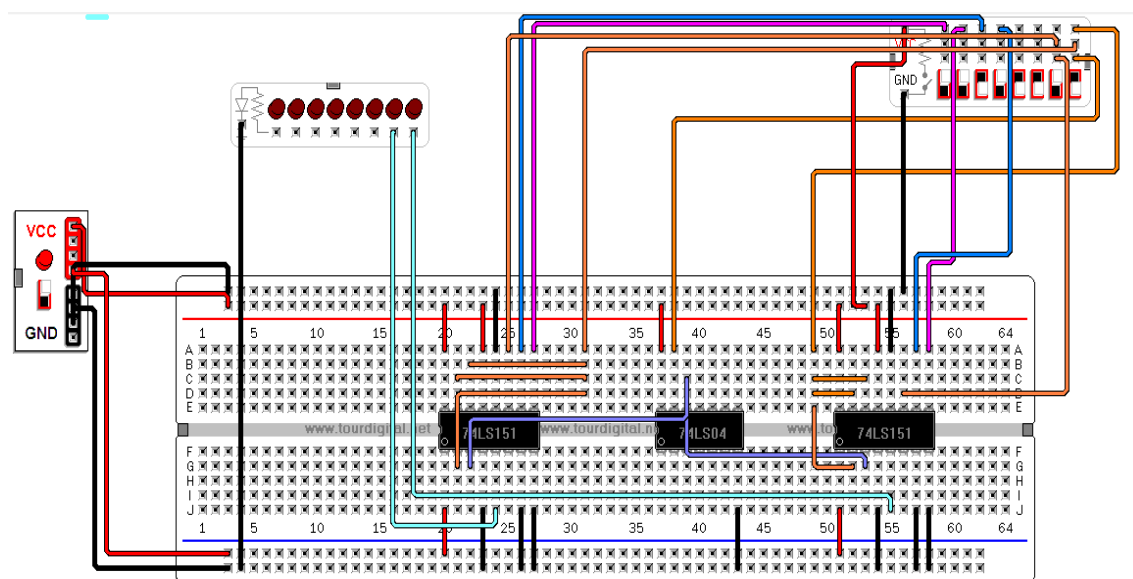


Figura 4: Teste 4 - NOT(A)

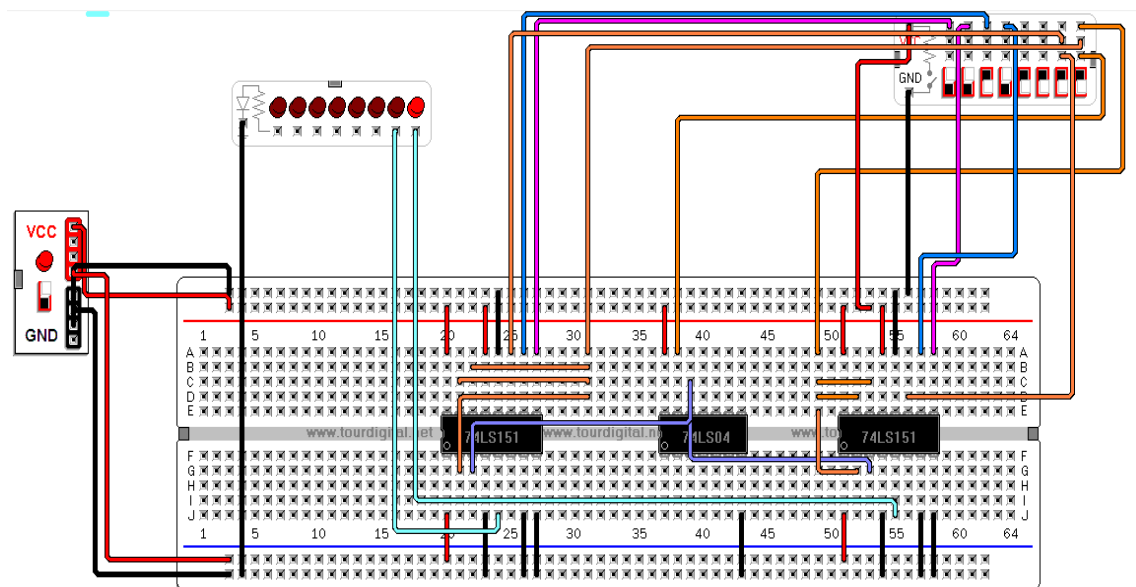


Figura 5: Teste 5 - AND (B,A)

Instrução Realizada	Binário(A,B,Op.Code)	Valor Em Hexa	Resultado em Binário
AND(A,B)	10 01 00	24	00
OR(A,B)	10 01 01	25	11
SOMA(A,B)	10 01 11	27	11
NOT(A)	11 01 10	36	00
AND(B,A)	11 01 00	34	01

Figura 6: Tabela de Execução dos programas de Teste