**体系结构 第六章**

**陈彦帆 2018K8009918002**

1.

2.

1）机械层。接口的外形、尺寸、信号排列、连接线的长度范围等等。

2）电气层。信号描述、电源电压、电平标准、信号质量等等。

3）协议层。信号时序、握手规范、命令格式、出错处理等等。

4）架构层。硬件模型、软件架构等等。

3.

以axi3总线为例：

output [3 :0] arid ,

output [31:0] araddr ,

output [7 :0] arlen ,

output [2 :0] arsize ,

output [1 :0] arburst,

output [1 :0] arlock ,

output [3 :0] arcache,

output [2 :0] arprot ,

output arvalid,

input arready,

input [3 :0] rid ,

input [31:0] rdata ,

input [1 :0] rresp ,

input rlast ,

input rvalid ,

output rready ,

output [3 :0] awid ,

output [31:0] awaddr ,

output [7 :0] awlen ,

output [2 :0] awsize ,

output [1 :0] awburst,

output [1 :0] awlock ,

output [3 :0] awcache,

output [2 :0] awprot ,

output awvalid,

input awready,

output [3 :0] wid ,

output [31:0] wdata ,

output [3 :0] wstrb ,

output wlast ,

output wvalid ,

input wready ,

input [3 :0] bid ,

input [1 :0] bresp ,

input bvalid ,

output bready

总共212条

若加上时钟线和复位线，则为214条。

4.

module apb\_gpio #(

PADDR\_SIZE = 32

)

(

input PRESETn,

input PCLK,

input PSEL,

input PENABLE,

input PADDR,

input PWRITE,

input [PDATA\_SIZE/8-1:0] PSTRB,

input [PDATA\_SIZE -1:0] PWDATA,

output [PDATA\_SIZE -1:0] PRDATA,

output PREADY,

output PSLVERR,

input [PDATA\_SIZE -1:0] gpio\_i,

output [PDATA\_SIZE -1:0] gpio\_o,

);

reg [PADDR\_SIZE -1:0] data\_r;

reg [PADDR\_SIZE -1:0] control\_r;

wire [PADDR\_SIZE -1:0] next\_data;

wire [PADDR\_SIZE -1:0] next\_control;

assign PSLVERR = 1'd0;

assign PREADY = 1'd1;

genvar i

generate for (i=0;i<PDATA\_SIZE/8;i++) begin: data\_gen

assign next\_data[i\*8+7:i\*8] = PSTRB[i] ? PWDATA[i\*8+7:i\*8] : data\_r[i\*8+7:i\*8];

end endgenerate

genvar i

generate for (i=0;i<PDATA\_SIZE/8;i++) begin: control\_gen

assign next\_control[i\*8+7:i\*8] = PSTRB[i] ? PWDATA[i\*8+7:i\*8] : control\_r[i\*8+7:i\*8];

end endgenerate

always @(posedge PCLK)

if(~PRESETn) data\_r <= {PADDR\_SIZE{1'd0}};

else if (PSEL & PENABLE & PWRITE & (PADDR == 1'd0))

data\_r <= next\_data;

always @(posedge PCLK)

if(~PRESETn) data\_r <= {PADDR\_SIZE{1'd0}};

else if (PSEL & PENABLE & PWRITE & (PADDR == 1'd1))

control\_r <= next\_control;

assign PRDATA = PADDR==1'd0 ? data\_r : control\_r;

assign gpio\_o = ~control\_r & data\_r;

endmodule

5. Rank, Bank, Row, Column

6.行地址最多15位，列地址最多11位：

(2^15)\*2^11 \* 2 \* 4 \* 2^3\*64 bit = 32G Byte

行地址\*列地址\*64位\*bank数\*双通道\*片选