ercesiMIPS Lab Manual

A guide to Single Cyclic CPU with 7-9(11) MIPS Instructions

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"SWEET JEZUS WHY!?"

If you're reading this, chances are that either your arms are suffering from anemia in waiting for the TA's to finish helping the 20 people in the room, or you're trying to design in Chisel without any TA's whatsoever, and you just wanna end it all. Fret not! This document serves as a specification for basic explanations of single cyclic MIPS CPU with 7-11 instructions supporting, also a helpful links and forbidden deigning secrets whose names none dare speak.

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1 Overview

The structure of Single cyclic MIPS CPU has been introduced in CS 11007 class lecture.

- **Supported Instructions** includes *sub, add, or, ori, lw, sw, lst, beq, j*, or adding *addi, and, andi* for better programming experience in assembly. All these instructions can be supported without exception detecting (overflow detecting)
- **All instructions work in one cycle.** For the very beginning stage, Single Cyclic CPU model is a great example to explain how CPU works.
- **Consisted of Data Path, Control Unit and Memory Unit.** To illustrate the typical systematic idea of computer, we recommend you design your first CPU with two separated modules, CPath and DPath, in such coding style, both blocks can also be easily verified separately. Additionally, if more complement MIPS ISA is chosen, this structure will be high efficient to be extended.
- **Chisel3 is also recommended.** Chisel is a powerful structural hardware description language, with more efficient expression for block, operation, and IO bundles compared with Verilog. However, the most significant feature of Chisel is that it can express the structure of system without detailed circuits coding. Further more, we prefer Chisel3 instead of Chisel2, which relies on verilator for verilog simulations instead of Synopsys vcs. The difference between these tow versions can be referenced here: `https://github.com/ucb-bar/chisel3/wiki/Chisel3-vs-Chisel2`.

2 Specification

A typical single cyclic CPU core is consisted of Control Unit and Data Path unit. In lecture 10 11, the whole system is illustrated in Fig. 1.

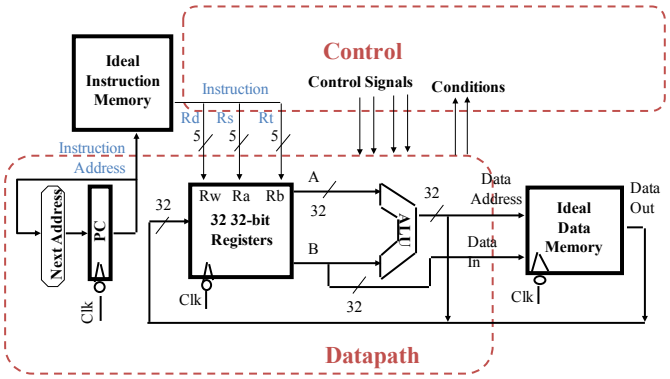

Figure 1: Single Cyclic CPU Block Diagram

Two Module classes are recommended for Control Unit and Data Path Unit respectively, as shown in following Fig. 2. Although the Harvard structure is adopted now to simplify the memory control and initialization, a MIPS adaptive memory model (Princeton Structure) is mandatory in further MIPS program test (for Multi-cyclic CPU Lab). In Fig. 2, almost all signals

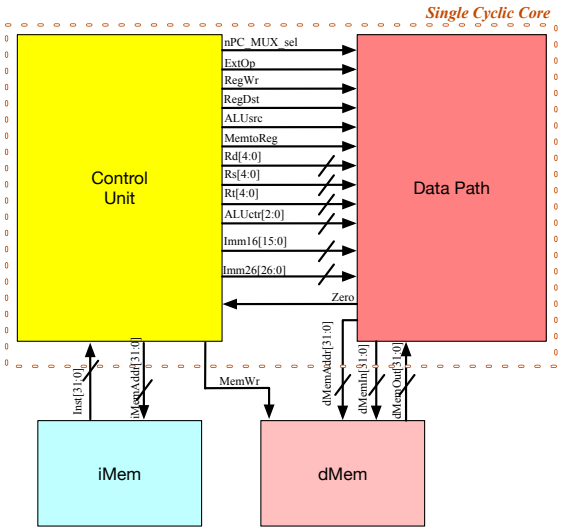

Figure 2: Single Cyclic CPU Block Diagram

can be renamed by your self except those evaluation required singles specified in Section 4.1.

3 Chisel3 101

3.1 Files, Directory and `package`

All designed files should contain `package` definition at the very beginning position for `sbt` interpreting.

```
package SingleCycle
```

If the package name is re-defined by you own, please check all files to revise the package name. Theoretically, the files with correct package definition could be placed anywhere of `src` directory. We preferred `src/main/scala/SingleCycle` for the design files and `src/test/scala/SingleCycle` for the tests files.

3.2 Define Ports

In single cycle ercesiMIPS project, bunches of singles connect Control Unit and Data Path Unit, which are only with different direction in different **Module**. Simply wrap the object in an `Input()` or `Output()` function. A example of `CtltoDatIo` is defined below.

```
class CtltoDatIo extends Bundle()
{
  val nPC_MUX_sel = Output(Bool())
  val RegWr   = Output(Bool())
  val RegDst    = Output(Bool())
  val ExtOp   = Output(Bool())
  val ALUctr    = Output(UInt(2.W))
  val ALUsrc    = Output(Bool())
  val MemtoReg  = Output(Bool())
  val Rd      = Output(UInt(5.W))
  val Rt      = Output(UInt(5.W))
  val Rs      = Output(UInt(5.W))
  val Imm16     = Output(UInt(16.W))
  val Imm26   = Output(UInt(26.W))
}
```

To make the definition efficiently, the signals can be instanced in both modules, as shown below:

```
class CPathIo extends Bundle()
{
  val Inst    = Input(UInt(32.W))
  val resetSignle = Input(Bool())
  val MemWr   = Output(Bool())
  val valid   = Output(Bool())
  val ctl     = new CtltoDatIo()
  val dat     = new DatToCtlIo().flip()
}

class CtlPath extends Module()
{
  val io      = IO(new CPathIo ())
  ...
}
```

```
class DatToCtlIo extends Bundle()
{
  val cmp_out = Output(Bool())
}
class DPathIo extends Bundle()
{
  //val host    = new HTIFIO()
  val imem_addr = Output(UInt(32.W))
  val dmem_addr = Output(UInt(32.W))
  val dmem_datIn  = Output(UInt(32.W))
  val dmem_datOut = Input(UInt(32.W))
  val ctl     = new CtltoDatIo().flip()
  val dat     = new DatToCtlIo()
}

class DatPath extends Module {
  val io = IO(new DPathIo ())
```

```
  ...
}
```

In these examples, the connected IOs in different modules are instanced with `flip()` function for reversing its direction.

3.3 Define a Module

To object the hierarchical mechanism, modules defined in Chisel are described as a type of new **Module** class, shown as below.

```
class DatPath extends Module {
  val io = IO(new DPathIo ())
  // Internal Signal
  val BusA  = Wire(UInt(32.W))
  val BusB  = Wire(UInt(32.W))
  ......
  ......
}
```

In which, a user-defined Data Path module, with module name of DatPath, is defined as a *class* which:

- inherits from Module,
- contains an interface wrapped in an `IO()` function and stored in a port field named io, and
- wires together subcircuits in its constructor.

4 Evaluation Requirement

4.1 Signal Requirement

TBD