ercesiMIPS Lab Manual

A guide to Single Cyclic CPU with 7-9(11) MIPS Instructions

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"SWEET JEZUS WHY!?"

If you're reading this, chances are that either your arms are suffering from anemia in waiting for the TA's to finish helping the 20 people in the room, or you're trying to design in Chisel without any TA's whatsoever, and you just wanna end it all. Fret not! This document serves as a specification for basic explanations of single cyclic MIPS CPU with 7-11 instructions supporting, also a helpful links and forbidden deigning secrets whose names none dare speak.

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1 Overview

The structure of Single cyclic MIPS CPU has been introduced in CS 11007 class lecture.

- **Supported Instructions** includes *sub, add, or, ori, lw, sw, lst, beq, j*, or adding *addi, and, andi* for better programming experience in assembly. All these instructions can be supported without exception detecting (overflow detecting)
- **All instructions work in one cycle.** For the very beginning stage, Single Cyclic CPU model is a great example to explain how CPU works.
- **Consisted of Data Path, Control Unit and Memory Unit.** To illustrate the typical systematic idea of computer, we recommend you design your first CPU with two separated modules, CPath and DPath, in such coding style, both blocks can also be easily verified separately. Additionally, if more complement MIPS ISA is chosen, this structure will be high efficient to be extended.
- **Chisel3 is also recommended.** Chisel is a powerful structural hardware description language, with more efficient expression for block, operation, and IO bundles compared with Verilog. However, the most significant feature of Chisel is that it can express the structure of system without detailed circuits coding. Further more, we prefer Chisel3 instead of Chisel2, which relies on verilator for verilog simulations instead of Synopsys vcs. The difference between these tow versions can be referenced here: https://github.com/ucb-bar/chisel3/wiki/Chisel3-vs-Chisel2.

2 Specification

A typical single cyclic CPU core is consisted of Control Unit and Data Path unit. In lecture 10 11, the whole system is illustrated in Fig. 1.

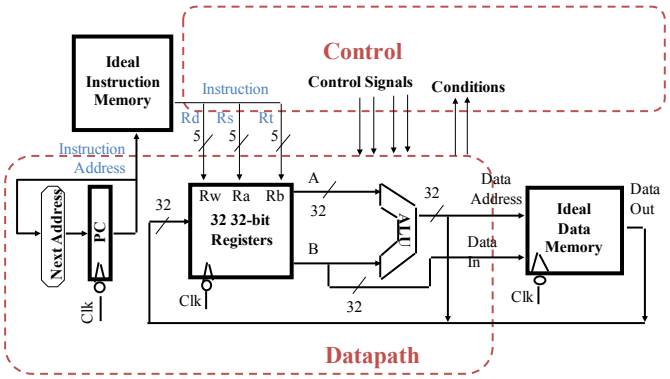

Figure 1: Single Cyclic CPU Block Diagram

Two Module classes are recommended for Control Unit and Data Path Unit respectively, as shown in following Fig. 2. Although the Harvard structure is adopted now to simplify the memory control and initialization, a MIPS adaptive memory model (Princeton Structure) is mandatory in further MIPS program test (for Multi-cyclic CPU Lab).

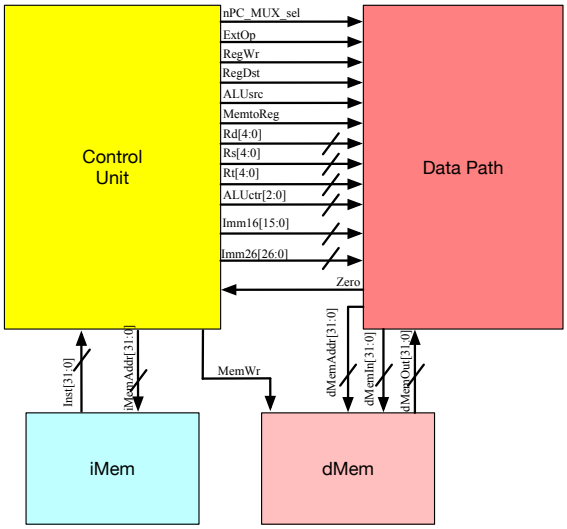

Figure 2: Single Cyclic CPU Block Diagram

3 Chisel3 101

4 Evaluation Requirement

http://www.mbsd.cs.ru.nl/publications/papers/2010/CleanStdEnvAPI.pdf