Datasheet

Total MIPI Display IP Solution

DSI-2 v1.0 Host Controller
DSI-2 v1.0 Device Controller
C-PHY v1.0
D-PHY v1.2 Physical Interface
C-PHY/ D-PHY Combo Physical Interface

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1 Introduction

1.1 About DSI

The MIPI®Alliance the Display Serial Interface (DSI) dates back to 2005. The Display Serial Interface specification defines protocols between a host processor and peripheral devices using a D-PHY physical interface. The DSI-2 specification builds on existing specifications by adopting pixel formats and command set defined in MIPI Alliance Specifications for Display Pixel Interface 2 (DPI-2) and Display Command Set (DCS).

From a system or software point of view, serialization and deserialization operations should be transparent. The most visible, and unavoidable consequence of transformation to serial data and back to parallel is increased latency for transactions that require a response from the peripheral. For example, reading a pixel from the frame buffer on a display module has a higher latency using DSI-2 than DBI. Another fundamental difference is the host processor's inability during a read transaction to throttle the rate or size of returned data.

1.2 Arasan's Contribution to MIPI

Arasan has been a member of MIPI for over ten years. We are active participants in a number of working groups. We work closely with other member customers to ensure compliant implementation of standards based IP.

1.3 Arasan's Total IP Solution

Arasan provides a Total IP Solution, which encompasses all aspects of IP development and integration, including analog and digital IP cores, verification IP, software stacks & drivers, and hardware validation platforms. Benefits of Total IP Solution:

- Seamless integration from PHY to Software
- Assured compliance across all components
- Single point of support
- Easiest acquisition process (one licensing source)
- Lowest overall cost including cost of integration
- Lowest risk for fast time to market

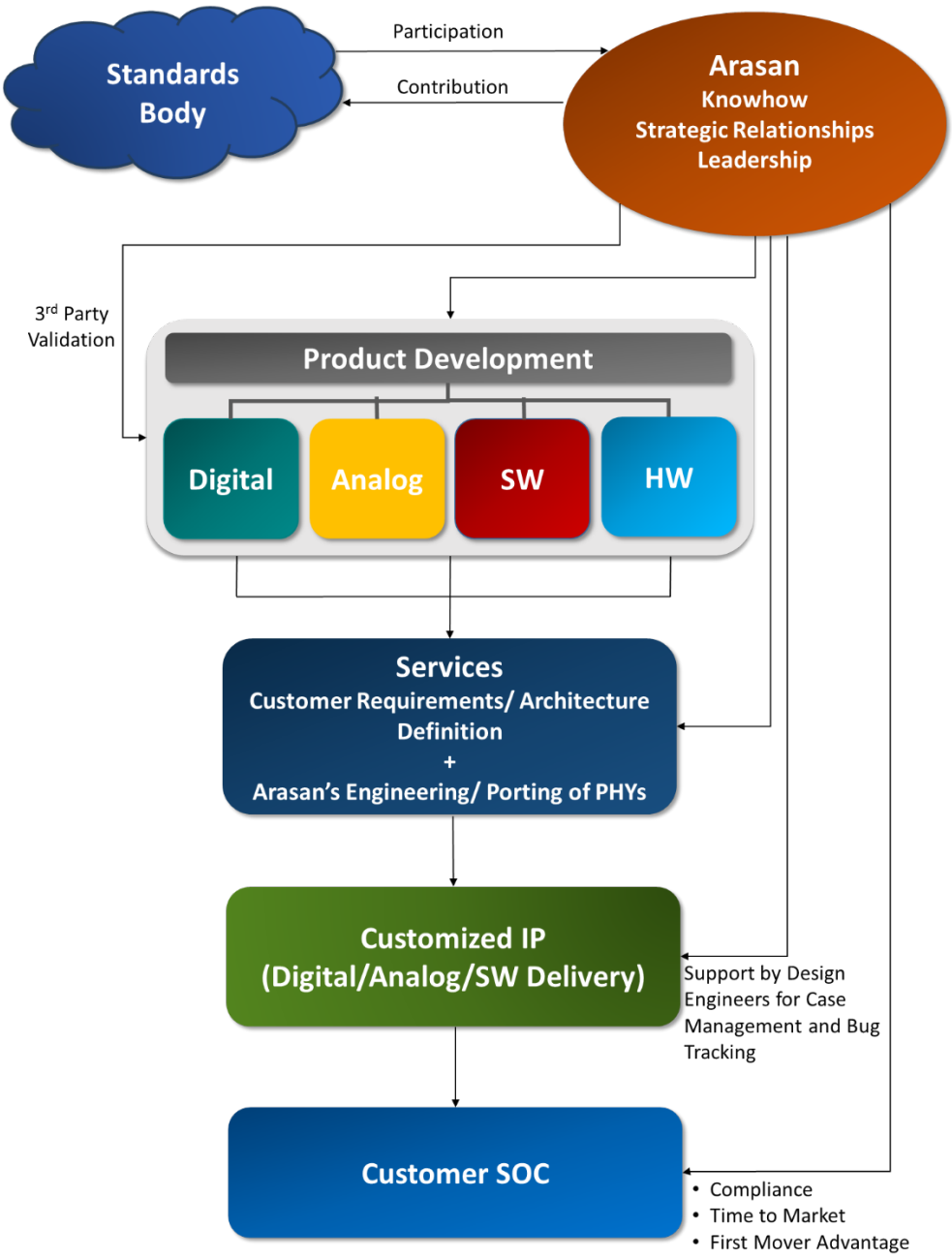

Figure 1: Arasan's Total IP Solution

2 MIPI DSI-2 Host IP

2.1 Overview

Arasan Chip Systems is a leading SOC IP provider of a complete suite of MIPI compliant IP solutions, which consist of IP cores, verification IP, software stacks and drivers, protocol analyzers, hardware platforms for software development and compliance testing, and optional customization services. The MIPI compliant IP cores are interface building blocks that simplify interconnect architectures in mobile platforms. This leads to smaller footprint, greater interoperability between mobile IP, chips and devices from diverse sources, and lower power and EMI.

This document describes the Arasan IP Core that functions as a MIPI DSI-2 Host Controller, which typically resides in a mobile platform's application processor, and communicates over a D-PHY serial link to a DSI-2 Device in the display panel.

2.2 Features

- Compliant with the following MIPI specifications
  - Display Serial Interface (DSI-1) version 1.0
  - Display Pixel Interface (DPI-2) version 2.00
  - Display Bus Interface (DBI-2) version 2.00
  - Display Command Set (DCS) version 1.02
  - D-PHY version 2.0 – approval pending early 2016
  - C-PHY version 1.0
  - Acknowledge packets and trigger messages
  - Programmable error injection in Verification IP and error detection in design IP
- Display Panel Connectivity and video/command processing supports:
  - DPI or DBI, depending on panel or display unit architecture
  - Generic command
  - Generic parallel interface for sending and receiving vendor-specific information to and from the display driver logic in the display module
  - All generic read/writes over DBI/Generic interface
- Video Mode supports:
  - Wide range of display resolution and pixel formats
  - Display resolutions: QQVGA, QCIF, QVGA, CIF,VGA,WVGA, XGA, 1080p, QXGA, QSXGA
  - Burst mode and non-burst transfers over DPI interface

- DBI supports:
  - 8/9/16-bit data transfer in DBI Type B interface
  - All DCS commands

- AHB Interface for register configuration and monitoring using programmed IO

2.3 Architecture

2.3.1 Functional Description

The Arasan DSI-2 Host Controller IP is designed to provide MIPI DSI-2 1.0 compliant high speed serial connectivity for mobile application processors using 1 to 4 D-PHYs depending on bandwidth needs. Serial connectivity to the display module's DSI-2 device is implemented using 1 to 4 D-PHY's (also available from Arasan), depending on display bandwidth needs. This IP connects to the D-PHY's through the PPI interface.

On the application processor side, Arasan's DSI-2 Host Controller provides the choice of DPI or DBI Interface to a graphics controller. A DBI interface provides downstream support of Types 1 to 3 display modules, and the DPI Interface is needed for Types 2 to 4 displays.

Initial configuration of this IP can be done through programmed IO over the AHB bus, however, other bus interfaces can be provided upon request.

2.3.2 Functional Block Diagram

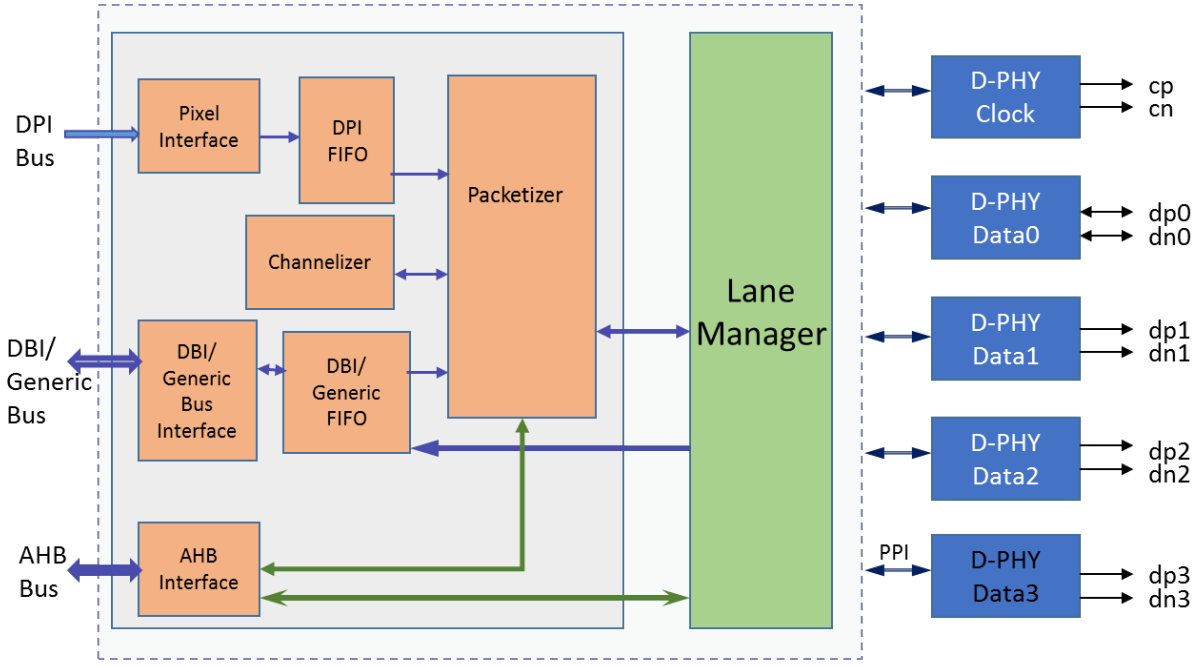

Figure 1: DSI-2 Device (Tx) Functional Block Diagram

2.3.3 Block Diagram Description

2.3.3.1 Lane Manager

This block communicates through a PPI interface with one to four D-PHY data lanes, depending on the bandwidth needs of an application. The Lane Manager block drives the different states in the D-PHY's like ULPS (Ultra-Low Power State), HS (High Speed) and LP (Low Power). It receives the data from the Packetizer module and distributes across the D-PHY data lanes based on the programmed lane count.

It has timers like high speed transmit timeout, low speed reception timers, and turnaround timeout counters to recover itself from fault mode conditions, and device reset timers for recovery from contentions.

In LP mode, this block is responsible for sending and receiving the trigger messages, and receiving the generic/DCS read response data in short or long packet formats. For incoming LP mode packets, this block manages ECC and CRC checking.

2.3.3.2 Channelizer

The Channelizer utilizes the Blanking and Low Power (BLLP) interval during DPI transmits to interleave DBI/Generic transfers during those times. This results in extremely efficient DSI-2 bandwidth utilization.

2.3.3.3 Packetizer

Depending on the packet information registered in the control FIFO in the DBI/Generic Bus Interface, short packets or headers of long packets are generated and transmitted by the Packetizer. For long packets, data from the Data FIFO is appended, the byte length of which is referenced in the control FIFO.

Depending on the signalling in the DPI Interface and the parameters programmed in its registers, either short or long packets are generated and transmitted. ECC is generated and added for short packets and headers of long packets. For long packets, pixels that are gathered in a DPI Data FIFO are appended as payloads of long packets, along with a CRC value calculated by the Packetizer.

2.3.3.4 DPI FIFO and Pixel Interface

A pixel-to-byte converter in the Pixel Interface converts the incoming 16, 18 or 24-bit pixel data to byte format and stores it in DPI FIFO, and notifies the Packetizer. A 2048 x32-bit DPRAM is used for line buffering.

2.3.3.5 DBI/Generic FIFO and Bus Interface

These blocks parses and classify the incoming DCS/generic commands as read and write commands under various categories. The read commands are passed on to the peripherals and read responses are sent back to the DBI interface. Commands that involve a huge data write data transfer are converted into DCS/generic long write commands and sent by the Packetizer to the Lane Manager as packets.

2.3.3.6 AHB Slave Interface

This block allows a processor to configure the IP through programmed IO, and provides for the IP to provide status information to the processor using interrupts.

2.4 Pin Diagram

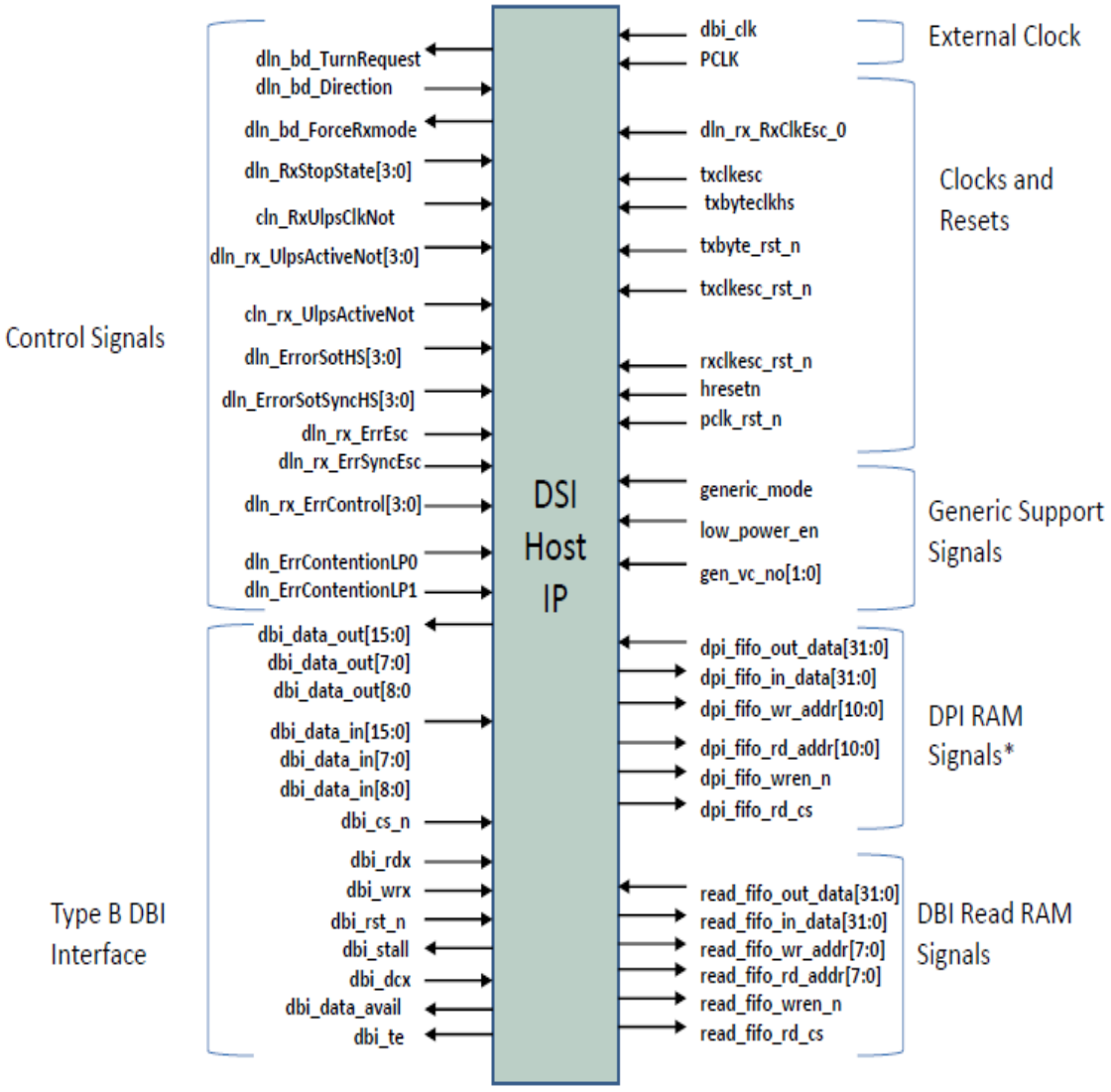

Figure 2: DSI-2 Host Pinout

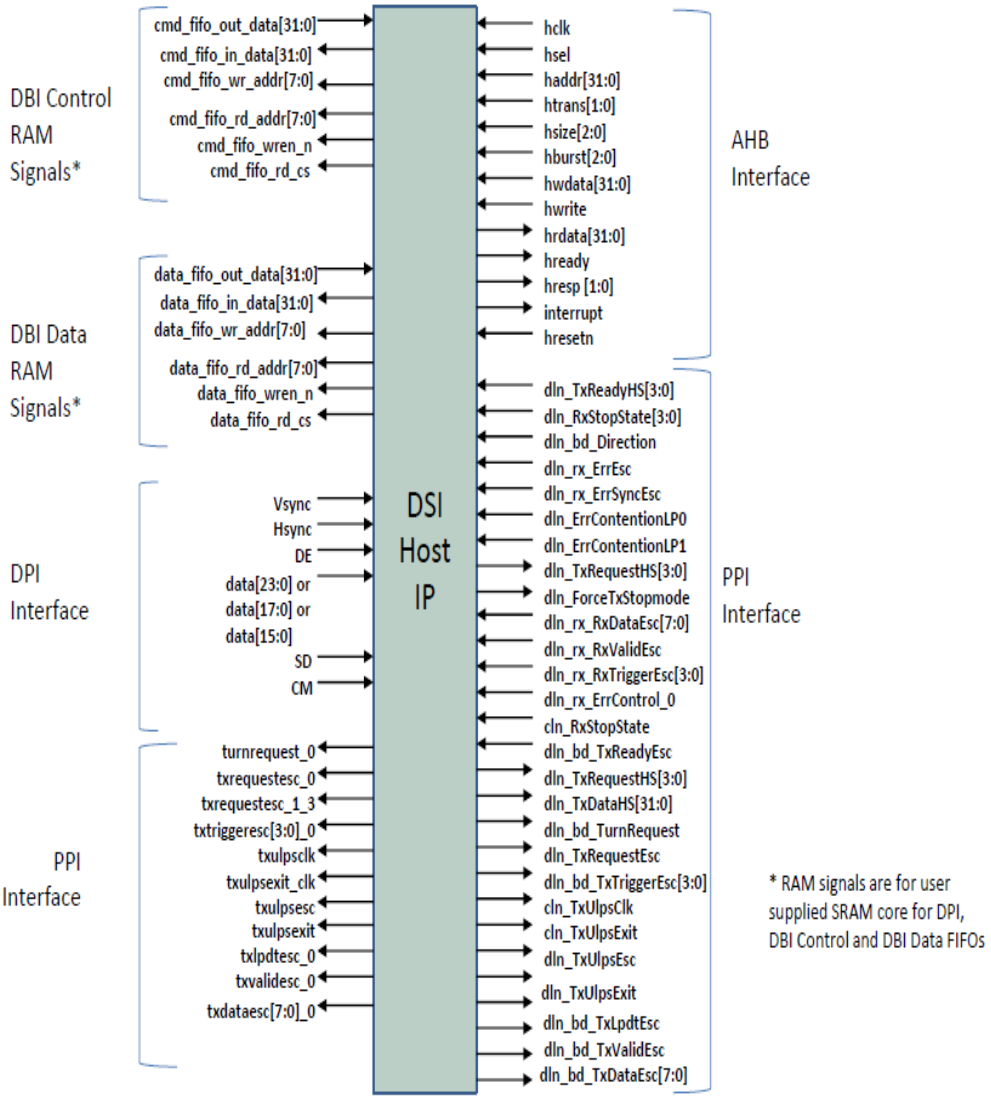

Figure 3: DSI-2 Host Pinout Continued

2.5 SOC Level Integration

2.5.1 IP Deliverables

- Verilog HDL of the IP Core
- User guide
- Gate count estimates available upon request
- Synthesis scripts

2.5.2 Verification Environment

- Comprehensive suite of simulation tests for ease of SOC integration
- Verification components and test files provided
- Verification environment and test suite well documented

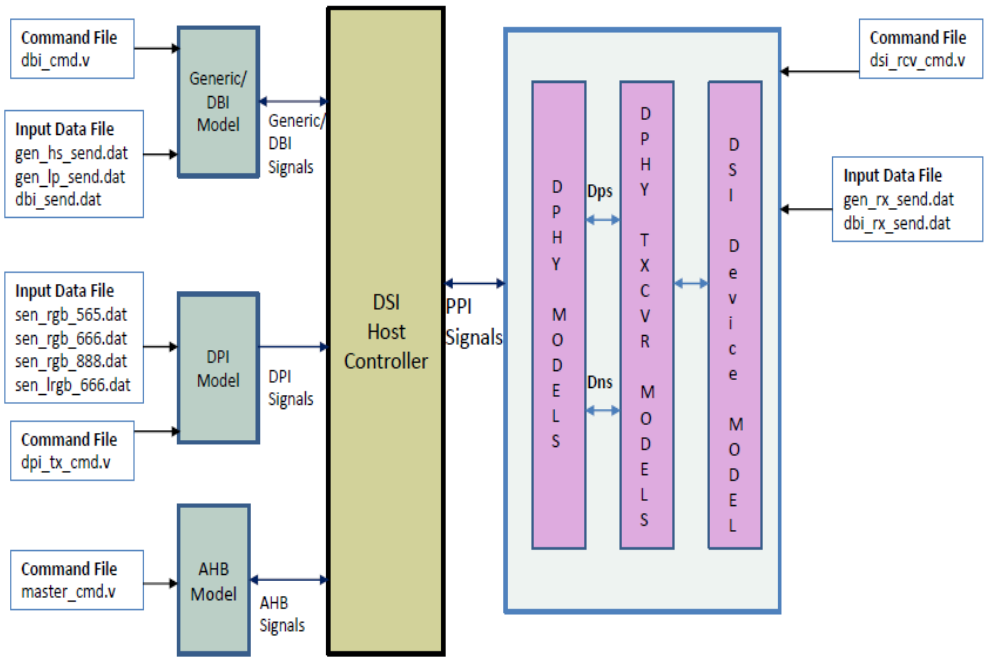

Figure 4: Verification Environment of DSI-2 Host IP

3 MIPI DSI-2 Device IP

3.1 Overview

Arasan Chip Systems is a leading SOC IP provider of a complete suite of MIPI compliant IP solutions, which consist of IP cores, verification IP, software stacks and drivers, protocol analyzers, hardware platforms for software development and compliance testing, and optional customization services. The MIPI compliant IP cores are interface building blocks that simplify interconnect architectures in mobile platforms. This leads to smaller footprint, greater interoperability between mobile IP, chips and devices from diverse sources, and lower power and EMI.

This document describes the Arasan IP Core that functions as a MIPI DSI-2 Device Controller, which typically resides in a mobile platform's display panel, and communicates over a D-PHY serial link to a DSI-2 Host in the applications processor.

3.2 Features

- Compliant with the following MIPI specifications
  - Display Serial Interface (DSI-1) version 1.0
  - Display Pixel Interface (DPI-2) version 2.00
  - Display Bus Interface (DBI-2) version 2.00
  - Display Command Set (DCS) version 1.02
  - D-PHY version 2.0 – approval pending early 2016
  - C-PHY version 1.0
  - Acknowledge packets and trigger messages
  - Programmable error injection in Verification IP and error detection in design IP
- Display Panel Connectivity and video/command processing supports:
  - DPI or DBI, depending on panel or display unit architecture
  - Generic command
  - Generic parallel interface for sending and receiving vendor-specific information to and from the display driver logic in the display module
  - All generic read/writes over DBI/Generic interface
- Video Mode supports:
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  - Display resolutions: QQVGA, QCIF, QVGA, CIF,VGA,WVGA, XGA, 1080p, QXGA, QSXGA
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- DBI supports:
  - 8/9/16-bit data transfer in DBI Type B interface
  - All DCS commands

- AHB Interface for register configuration and monitoring using programmed IO

3.3 Architecture

3.3.1 Functional Description

The Arasan DSI-2 Device Controller IP is designed to provide MIPI DSI-2 1.0 compliant high speed serial connectivity for mobile display modules with Type 1 to 4 architectures. Serial connectivity to the mobile applications processor's DSI-2 host is implemented using 1 to 4 D-PHY's (also available from Arasan), depending on display bandwidth needs. This IP connects to the D-PHY's through the PPI interface.

Display modules consist of display driver logic driving display signals onto a display device or panel. On the display driver side, Arasan's DSI-2 Device Controller provides the DBI Interface for Types 1 to 3 display modules and the DPI Interface for Types 2 to 4 displays.

Initial configuration of this IP can be done through programmed IO over the AHB bus, however, other bus interfaces can be provided upon request.

3.3.2 Functional Block Diagram

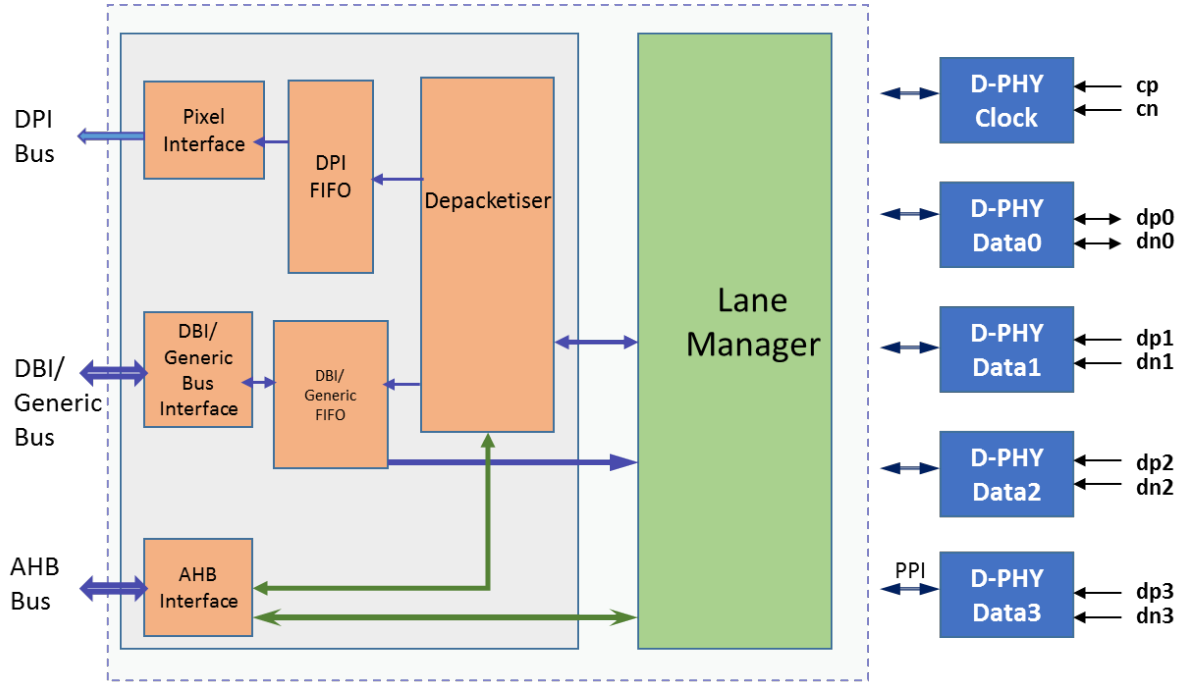

Figure 5: DSI-2 Device (Rx) Functional Block Diagram

3.3.3 Block Description

3.3.3.1 Lane Manager

This block communicates through a PPI interface with one to four D-PHY data lanes, depending on the bandwidth needs of an application. The Lane Manager block detects the different states of the D-PHY's like ULPS (Ultra-Low Power State), HS (High Speed) and LP (Low Power). It collects incoming bytes of data from the D-PHY lanes at every clock edge based on programmed lane count and forwards them to the Depacketizer module. It is also responsible for contention and error detection and response for all incoming packets.

In LP mode, this block is responsible for sending trigger messages, acknowledgment packets and generic/DCS read response data in short or long packet formats. For outgoing LP mode packets, this block manages ECC and CRC generation.

3.3.3.2 Depacketizer

From the DSI-2 data type in the Data Identifier of the incoming packet, the Depacketizer determines whether the incoming packet is short or long. From the incoming long packets, the Depacketizer separates out the header, footer and payload and forwards each of them to the appropriate protocol layer blocks. The checksum value for long packet payloads is calculated and compared with received CRC and entered in the register set for further processing. Short packets and headers for long packets are corrected for 1-bit errors.

3.3.3.3 DPI FIFO and Pixel Interface

This path is selected in video mode and is unidirectional. Display sync event timing information originates as short packets from the DSI-2 host. Upon receiving them, the Pixel Interface converts those to display-related control signals, such as horizontal and vertical sync and blanking intervals. Payload bytes extracted by the Depacketizer from long packets received in HS mode from the DSI-2 host are sent through the DPI FIFO to the Pixel Interface block, which converts them to pixels and sends to the display panel through the DPI bus.

3.3.3.4 DBI/Generic FIFO and Bus Interface

This path is selected in command mode and is bidirectional. Long packets and short packets received from the Depacketizer contain the commands for the off-chip display module that implements the Display Command Set. For DCS or Generic Read commands, the number of data bytes collected for DBI read operations is based on the maximum return packet size settings, and forwarded to the Lane Manager to encapsulate within a packet structure, as described above.

3.3.3.5 AHB Slave Interface

This block allows a processor to configure the IP through programmed IO, and provides for the IP to provide status information to the processor using interrupts.

3.4 Pin Diagram

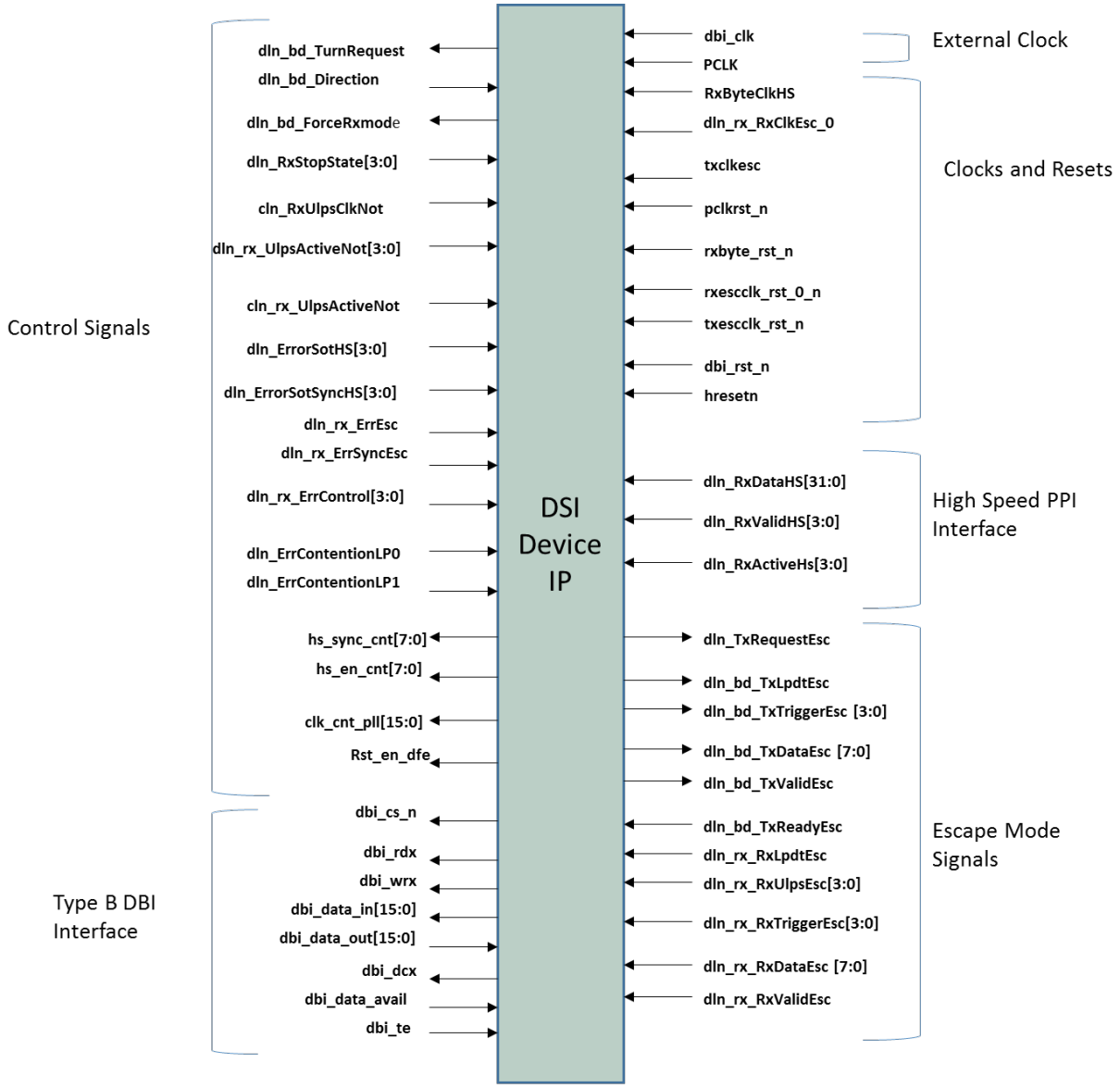

Figure 6: DSI-2 Device (Rx) Pinout

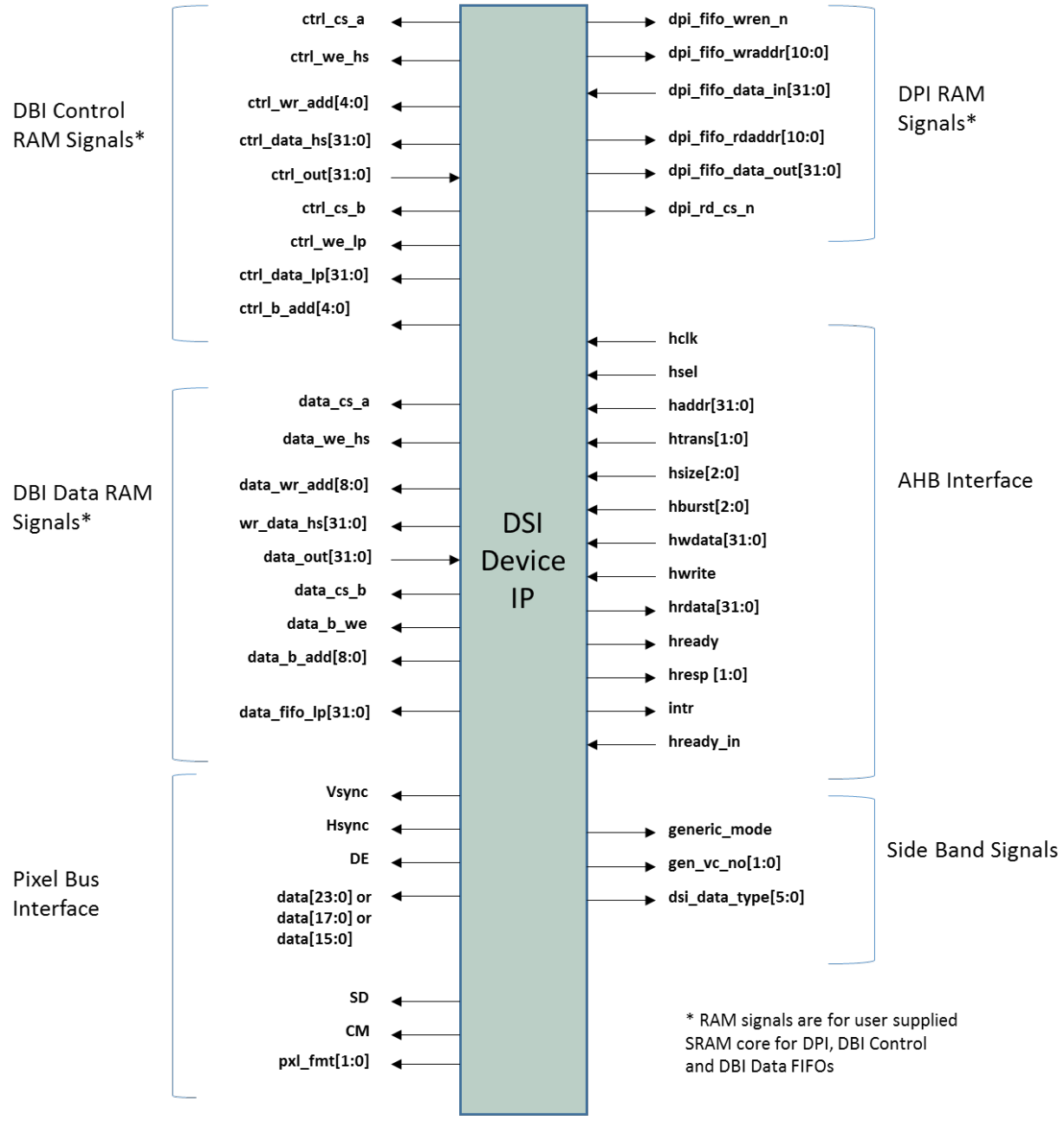

Figure 7 : DSI-2 Device (Rx) Pinout Continued

3.5 SOC Level Integration

3.5.1 IP Deliverables

- Verilog HDL of the IP Core
- User guide
- Gate count estimates available upon request
- Synthesis scripts

3.5.2 Verification Environment

- Comprehensive suite of simulation tests for ease of SoC integration
- Verification components and test files provided
- Verification environment and test suite well documented

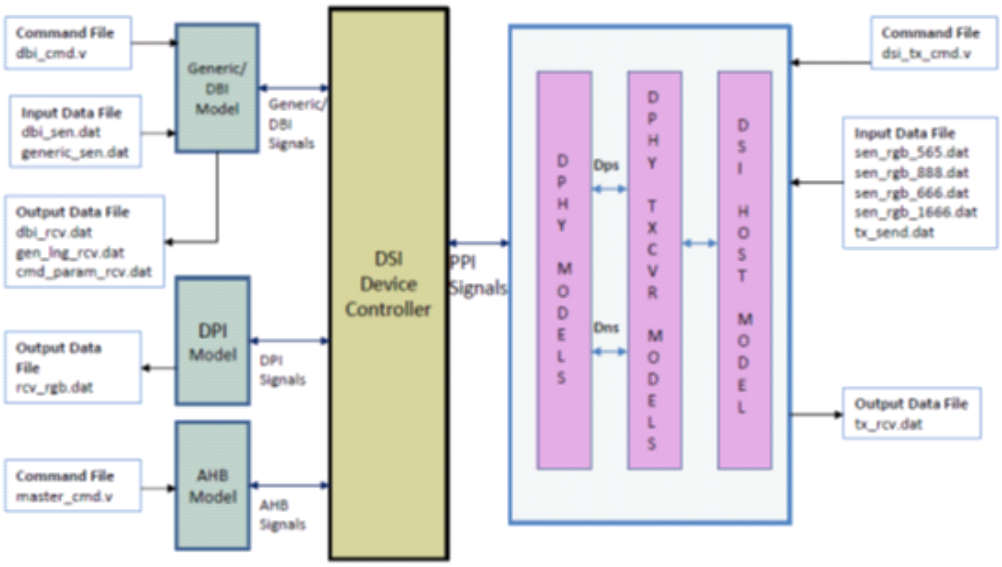

Figure 8: Verification Environment of DSI-2 Device IP

4 C-PHY + D-PHY Combo Physical Interface IP

4.1 Overview

The ever increasing demand for band width for the high resolution cameras resulted in to search for a simple, cost effective, rate efficient PHY which can support above 2.5Gbps. This search resulted into a new kind of PHY, which even at less channel rate provides very high data rate.

CPHY can achieve a very high data rate of 5.71Gbps per lane compared to the 2.5Gbps of DPHY1.2 or 1.5Gbps of DPHY1.1, still maintain the channel rate at 2.5Gsps which is same as DPHY1.2. CPHY achieves this by using a unique encoding mechanism in which 16 bit of input data is encoded into 7 symbols and each symbol is transmitted over a 3 Phase encoded line.

CPHY reuses the similar Low power signaling same as the DPHY. CPHY is designed such a way that it can co-exist sharing the same lines as DPHY. CPHY/DPHY combo IPs will be compatible to operate on the same channels used by DPHY, which offer a much wider area of application and flexibility. It can work with both old DPHY systems and is compatible with new CPHY.

Arasan's ComPHY is a CPHY/DPHY combo universal PHY which can be configured both as Transmitter and Receiver. Arasan's novel and innovative design techniques allowed sharing a number of modules between the CPHY and DPHY with no impact on performance resulting in optimal area and power.

4.2 C-PHY Based Interconnect Architecture

CPHY employs coding scheme in which clock can be recovered from the transmitted data. No separate clock lane is required in the interconnect and the slave will recover the clock from the data stream at the Slave side.

Each data lane is a 3 phase encoded requiring 3 separate line inter connections. Each lane interconnect provides up to 5.71 Gbps with effective data rate of 17.13 Gbps.

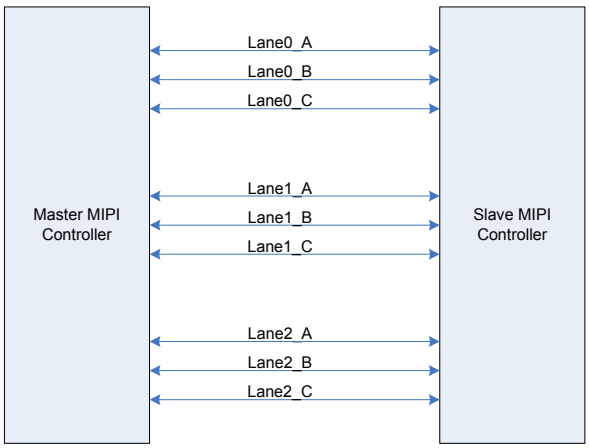

Figure 9: MIPI Link Diagram for CPHY

4.3 C-PHY Lane Architecture

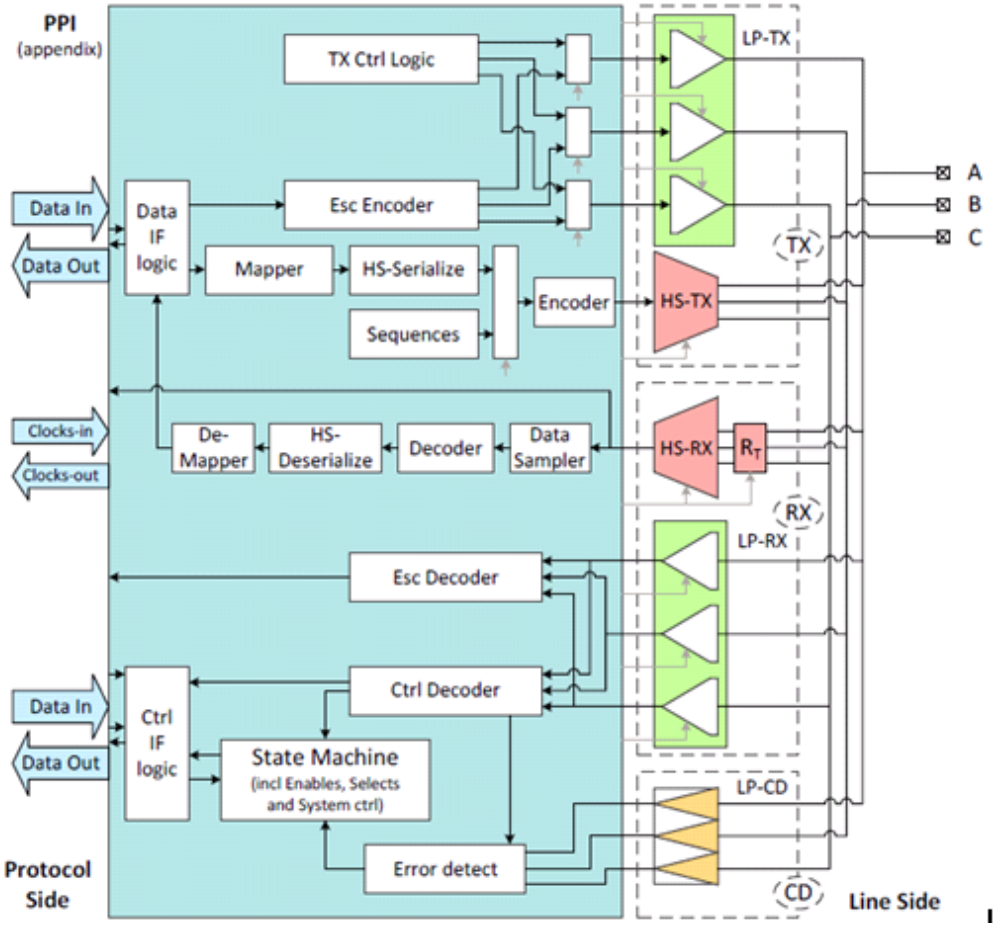

Figure 10: C-PHY Lane Architecture

Each Lane Module has a control and interface logic unit and a transceiver portion to handle 3 Phase High-Speed functions, single-ended Low-Power functions operating on each of the interconnect wires individually. The I/O functions are controlled by the Lane Control and Interface Logic block.

High-Speed signals have a low voltage swing of 250 mV, while Low-Power signals have a large swing of 1.2V. High-Speed functions are used for High-Speed Data traffic. The Low-Power functions are mainly used for control and can have data transfer support.

High Speed data width is 16bit at the PPI side, which is converted to 7 Symbols by the mapper. Each symbol is 3 bits and it is encoded into a 3-phase signal by the encoder driver combination.

Control and Interface Logic, sends and detects start of packet signaling and end of packet signaling on the data lanes. It has a serializer and de-serializer unit to dialog with the PPI / PHY adapter unit. Also it has clock divider unit to source and receive data during parallel data transfers from and to the PPI.

4.4 D-PHY Based Interconnect Architecture

DPHY employs a source synchronous scheme in which the High speed clock is transmitted using a separate channel along with the data lane. The clock maintains quadrature phase relationship to the data lane to ensure maximum margin between the clock and the data lane. Each data lane consists of two wires (Dp/Dn) and data is transmitted as differential signal on the both the edges of the clock.

Each lane interconnect provides up to 2.5 Gbps with effective data rate of 10 Gbps.

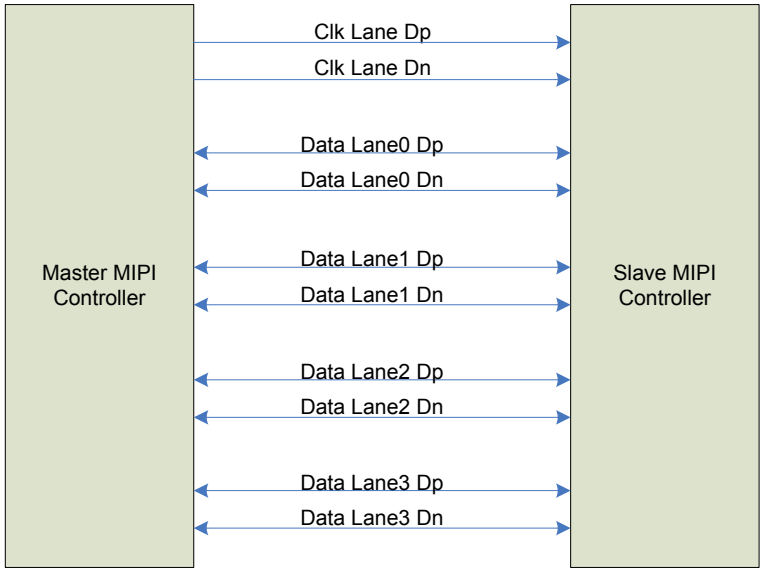

Figure 11: MIPI Link Diagram for DPHY

4.5 C-PHY – D-PHY Pad Table

Table 1: Functional description of D-PHY Pads for Clock Lane

Pin (D-PHY/ C-PHY)	Direction	Description (D-PHY)	Description (C-PHY)
dpck / lane1_A	Bidirectional	Positive polarity of low voltage differential clock signal for transmitter and receiver	Wire A in the 3 wire lane of 1st lane
dnck / lane1_B	Bidirectional	Negative polarity of low voltage differential clock signal for transmitter and receiver	Wire B in the 3 wire lane of 1st lane
dp2 / lane1_C	Bidirectional	Positive polarity of low voltage differential data signal for lane2	Wire C in the 3 wire lane of 1st lane
dn2 / lane2_A	Bidirectional	Negative polarity of low	Wire A in the 3 wire lane of 2nd

		voltage differential data signal for lane2	lane
dp3 / lane2_B	Bidirectional	Positive polarity of low voltage differential data signal for lane3	Wire B in the 3 wire lane of 2nd lane
dn3 / lane2_C	Bidirectional	Negative polarity of low voltage differential data signal for lane3	Wire C in the 3 wire lane of 2nd lane
dp0 / lane0_A	Bidirectional	Positive polarity of low voltage differential data signal for lane0	Wire A in the 3 wire lane of 1st lane
dn0 / lane0_B	Bidirectional	Negative polarity of low voltage differential data signal for lane0	Wire B in the 3 wire lane of 1st lane
dp1 / lane0_C	Bidirectional	Positive polarity of low voltage differential data signal for lane1	Wire C in the 3 wire lane of 1st lane
dn1	Bidirectional	Negative polarity of low voltage differential data signal for lane1	

Table 2: Power Pads

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
VDD_clk	Power	Power pad for the clock lane	Power pad for the data lane0
VSS_clk	Power	Ground pad for the clock lane	Ground pad for the data lane0
VDD_d0d1	Power	Power pad for Data lane 0 and Data lane 1	Power pad for the data lane1
VSS_d0d1	Power	Ground pad for Data lane 0 and Data lane 1	Ground pad for the data lane1
VDD_d2d3	Power	Power pad for Data lane 2 and Data lane 3	Power pad for the data lane2
VSS_d2d3	Power	Ground pad for Data lane 2 and Data lane 3	Ground pad for the data lane2
VDDD	Power	Power pad for the DFE	Power pad for the DFE
VSSD	Power	Ground pad for the DFE	Ground pad for the DFE
VDDLP12	Power	Power pad for low power block	Power pad for low power block

Table 3: Analog Function Trimming Inputs

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
trim_0[31:0]	Input	Trim bits for DPHY	Trim bits for CPHY
trim_1[31:0]	Input	Trim bits for DPHY	Trim bits for CPHY
trim_2[31:0]	Input	Trim bits for DPHY	Trim bits for CPHY
trim_3[31:0]	Input	Trim bits for DPHY	Trim bits for CPHY

Table 4: Clock and Reset Inputs

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
TxClkEsc	Input	Escape mode Transmit Clock. This clock is directly used to generate escape sequences. The period of this clock determines the symbol time for low power signals. This is also the input reference clock for the PLL	Escape mode Transmit Clock. This clock is directly used to generate escape sequences. The period of this clock determines the symbol time for low power signals. This is also the input reference clock for the PLL
enable	Input	Active Low system reset to the module	Active Low system reset to the module
dln_bd_ForceRx mo de	Input	Force Lane Module Into Receive mode / Wait for Stop state. This signal forces the state machine into RX mode.	Force Lane Module Into Receive mode / Wait for Stop state. This signal forces the state machine into RX mode.
dln_ForceTxStop mo de[3:0]	Input	Force Lane Module Into Transmit mode / Generate Stop state. This signal forces STOP signal on the transmit lines	Only the first three bits are used for the CPHY. Force Lane Module Into Transmit mode / Generate Stop state. This signal forces STOP signal on the transmit lines

Table 5: Clock Lane High Speed PPI Interface Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
cln_TxRequestHS	Input	High-Speed Transmit Request and Data Valid for clock lane. For clock Lanes, this active high signal causes the lane module to begin transmitting a high-speed clock	-
cln_RxActiveHS	Output	Receiver Clock Active. This asynchronous, active high signal indicates that a clock Lane is receiving a DDR clock signal	-
TxByteClkHS / TxWordClkHS	Output	High-Speed Transmit Byte Clock. This is used to synchronize PPI signals in the High-Speed transmit clock domain. It is recommended that all transmitting Data Lane Modules share one transmitter's byte clock signal. The frequency of byte clock is exactly 1/8 the High-Speed bit rate This is the txbyteclkhs to which all PPI interface is synchronous for transmitter.	High-Speed Transmit Word Clock. This is used to synchronize PPI signals in the high-speed transmit clock domain. The same clock is shared by all lane modules. The frequency of TxWordClkHS is exactly 1/7 the high-speed symbol rate.
RxByteClkHS / RxWordClkHS	Output	High-Speed Receive Byte Clock. This is used to synchronize signals in the High-Speed receive clock domain. The rxbyteclkhs is generated by dividing the received High-Speed DDR clock This is the byte clock to which all PPI interface is synchro-nous for receiver	High-Speed Receive Word Clock. This is used to synchronize signals in the high-speed receive clock domain. The RxWordClkHS is generated by dividing the recovered high-speed clock.

Table 6: Clock lane Escape PPI interface Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
cln_TxUlpsExit	Input	Transmit ULP Exit Sequence for clock lane. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when tx_ulpsactivenot_clk_n becomes deasserted. txulpsexit_clk is synchronous to txclkesc. This signal is ignored when the Lane is not in the ULP State	-
cln_TxUlpsClk	Input	To force the clock lane to transmit ULPS sequences in the clock line	-
cln_RxUlpsClkNot	Output	Receive Ultra Low-Power mode on Clock Lane. This active low signal is asserted to indicate that the Clock Lane module has entered the Ultra Low-Power mode. The Lane module remains in this mode with RxUlpsClkNot asserted until a Stop state is detected on the Lane Interconnect	-
cln_tx_UlpsActiv e Not	Output	ULP State (not) Active for clock lane. This active low signal i s asserted to indicate that the Lane is in ULP state.	-
cln_rx_UlpsActiv eN ot	Output	ULP State (not) Active for clock lane. This active low signal i s asserted to indicate that the Lane is in ULP state.	-

Table 7: Clock lane PPI Control Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
cln_Rxstopstate	Output	Lane is in Stop state for clock lane. This active high signal indicates that the lane module is currently in Stop state. This is valid for both receivers and transmitters. Note that this signal is asynchronous to any clock in the PPI interface	-

Table 8: Data lane High Speed PPI Interface Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_TxDataHS[47 :0]	Input	High-Speed Transmit Data for data lane. High-speed data to be transmitted. Data is captured on rising edges of transmitted byte clock. First 32 bits are only used for DPHY	High-Speed Transmit Data for data lane. High-speed data to be transmitted. Data is captured on rising edges of TxWordClkHS.
dln_TxRequestHS [3:0]	Input	High-Speed Transmit Request and Data Valid for data lane. A low-to-high transition on dln_TxRequestHS causes the lane module to initiate a Start-of-Transmission sequence. A high-to-low transition on dln_TxRequestHS causes the lane module to initiate an End-of- Transmission sequence. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on txdatahs_0 to be transmitted. The lane module accepts the data when both	Only first three bits are used for the CPHY High-Speed Transmit Request and Data Valid for data lane. A low-to-high transition on dln_TxRequestHS causes the lane module to initiate a Start-of-Transmission sequence. A high-to-low transition on dln_TxRequestHS causes the lane module to initiate an End-of- Transmission sequence. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on dln_TxDataHS to be transmitted. The lane module accepts the data

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
		dln_TxRequestHS and dln_TxReadyHS are active on the same rising TxByteClkHS clock edge. The protocol always provides valid transmit data when txdatahs_0 is active. Once asserted, dln_TxDataHS remains high until the data has been accepted, as indicated by dln_TxReadyHS. dln_TxRequestHS is only asserted while dln_TxRequestEsc is low	when both dln_TxRequestHS and dln_TxReadyHS are active on the same rising TxWordClkHS clock edge. The protocol always provides valid transmit data when txdatahs_0 is active. Once asserted, dln_TxDataHS remains high until the data has been accepted, as indicated by dln_TxReadyHS. dln_TxRequestHS is only asserted while dln_TxRequestEsc is low
dln_TxReadyHS [3:0]	OUTPUT	High-Speed Transmit Ready for data lane. This active high signal indicates that dln_TxDataHS is accepted by the lane module to be serially transmitted. dln_TxReadyHS is valid on rising edges of transmitted byte clock	High-Speed Transmit Ready for data lane. First three bits only used for CPHY This active high signal indicates that dln_TxDataHS is accepted by the lane module to be serially transmitted. dln_TxReadyHS is valid on rising edges of TxWordClkHS
dln_TxSendSync HS[2:0]	Input	-	High Speed Command to Transmit Sync Word. This command signal has the same timing as TxDataHS[15:0] on the PPI, but when TxSendSyncHS is active on a given TxWordClkHS cycle then TxDataHS[15:0] is ignored for any Word Clock cycle where TxSendSyncHS is active.
dln_RxDataHS[47 :0]	OUTPUT	High-Speed Receive Data for data lane. The signal connected to dln_RxDataHS was received first. Data is transferred on rising edges of receiver byte clock Only first 31 bits are used for DPHY	High-Speed Receive Data for data lane. The signal connected to dln_RxDataHS was received first. Data is transferred on rising edges of RxWordClkHS

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_RxValidHS[3:0]	OUTPUT	High-Speed Receive Data Valid for data lane	High-Speed Receive Data Valid for data lane. Only first three bits are used for CPHY
dln_RxInvalidCodeHS[2:0]	Output	-	High-Speed Invalid Code Word Detection. A high-speed status signal that indicates the present word on RxDataHS[15:0] was produced by a group of seven symbols that were not a valid code word.
dln_RxActiveHS[3:0]	OUTPUT	High-Speed Reception Active for data lane. This active high signal indicates that the lane module is actively receiving a high-speed transmission from the lane interconnect.	High-Speed Reception Active for data lane. This active high signal indicates that the lane module is actively receiving a high-speed transmission from the lane interconnect. Only first three bits are used for CPHY

Table 9: Data lane Escape mode PPI Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_TxRequestEsc [3:0]	Input	Escape mode Transmit Request for data lane. dln_TxRequestEsc is only asserted by the protocol while dln_TxRequestHS is low.	Escape mode Transmit Request for data lane. dln_TxRequestEsc is only asserted by the protocol while dln_TxRequestHS is low. Only first three bits are used for the CPHY.
dln_TxUlpsExit[3:0]	Input	Transmit ULP Exit Sequence for data lane. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when ulpsactivenot_0_n becomes	Transmit ULP Exit Sequence for data lane. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when ulpsactivenot_0_n becomes deasserted.

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
		deasserted. dln_TxUlpsExit is synchronous to TxClkEsc. This signal is ignored when the Lane is not in the ULP State.	dln_TxUlpsExit is synchronous to TxClkEsc. This signal is ignored when the Lane is not in the ULP State. Only first three bits are used for CPHY.
dln_TxUlpsEsc[3:0]	Input	Escape mode Transmit Ultra Low Power for data lane. This active high signal is asserted with dln_TxRequestEsc to cause the lane module to enter the ultra low power mode. The lane module remains in this mode until dln_TxRequestEsc is de-asserted. dln_bd_TxLpdtEsc and all bits of dln_bd_TxTriggerEsc are low when dln_TxUlpsEsc is asserted.	Escape mode Transmit Ultra Low Power for data lane. This active high signal is asserted with dln_TxRequestEsc to cause the lane module to enter the ultra low power mode. The lane module remains in this mode until dln_TxRequestEsc is de-asserted. dln_bd_TxLpdtEsc and all bits of dln_bd_TxTriggerEsc are low when dln_TxUlpsEsc is asserted. Only first three bits are used for CPHY
dln_bd_TxLpdtEsc	Input	This signal is used to request a low power data transmission entry in the forward direction.	This signal is used to request a low power data transmission entry in the forward direction.
dln_bd_TxTriggerEsc[3:0]	Input	A 4 bit signal that triggers a trigger sequence in the ESC mode in the forward direction	A 4 bit signal that triggers a trigger sequence in the ESC mode in the forward direction
dln_bd_TxDataEsc [7:0]	Input	In data mode, the 8-bit data to be transmittedin the forward direction.	In data mode, the 8-bit data to be transmittedin the forward direction.
dln_bd_TxValidEsc	Input	A valid signal which qualifies for the data lines.	A valid signal which qualifies for the data lines.
dln_bd_TurnDisable	Input	To avoid the turn around request during the lock up situation	To avoid the turn around request during the lock up situation
dln_bd_Direction	Output	To indicate the direction of the data lane. This signal is used to indicate the current direction of the lane interconnect. When direction_0 =0, the lane is in transmit mode (0=Output). When direction_0 =1, the lane is in receive mode (1=Input)	To indicate the direction of the data lane. This signal is used to indicate the current direction of the lane interconnect. When direction_0 =0, the lane is in transmit mode (0=Output). When direction_0 =1, the lane is in receive mode (1=Input)

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_bd_TurnRequest	Input	This signal is used to request a Turn around operation for a bi-directional lane	This signal is used to request a Turn around operation for a bi-directional lane
dln_rx_RxClkEsc[3:0]	Output	Escape mode Receive Clock for data lane 0. This signal is used to transfer received data to the protocol during escape mode. This "clock" is generated from the two Low-Power signals in the Lane interconnect. Because of the asynchronous nature of Escape mode data transmission, this "clock" may not be periodic	Escape mode Receive Clock for data lane 0. This signal is used to transfer received data to the protocol during escape mode. This "clock" is generated from the two Low-Power signals in the Lane interconnect. Because of the asynchronous nature of Escape mode data transmission, this "clock" may not be periodic. Only first three bits are valid for CPHY

Table 10: Data lane Escape Mode PPI Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_rx_RxUlpsEsc[3:0]	Output	Escape Ultra Low Power (Receive) mode for data lane. This active high signal is asserted to indicate that the lane module has entered the ultra low power mode. The lane module remains in this mode with dln_rx_RxUlpsEsc asserted until a Stop state is detected on the lane interconnect	Escape Ultra Low Power (Receive) mode for data lane. This active high signal is asserted to indicate that the lane module has entered the ultra low power mode. The lane module remains in this mode with dln_rx_RxUlpsEsc asserted until a Stop state is detected on the lane interconnect. Only first three bits are used for the CPHY.
dln_rx_UlpsActiveNot[3:0]	Output	ULPS signal received on the receiver in the bi-directional lane	ULPS signal received on the receiver in the bi-directional lane. Only first three bits are used for the CPHY.
dln_bd_TxReadyEsc	Output	Ready signal for the transmit data lines in reverse direction	Ready signal for the transmit data lines in reverse direction
dln_rx_RxDataEsc[7:0]	Output	The low power mode data in the Escape mode.	The low power mode datain the Escape mode.
dln_rx_RxValidEsc	Output	The ESC mode valid data	The ESC mode valid data
dln_rx_RxTrigger	Output	The Trigger mode receiver	The Trigger mode receiver signal

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
Esc[3:0]		signal	
dln_rx_RxLpdtEsc	Output	The low power data transfer for the first lane	The low power data transfer for the first lane
dln_rx_ErrEsc	Output	Error on the Escape sequence during receiver	Error on the Escape sequence during receiver
dln_rx_ErrSyncEsc	Output	Error in sync esc in the receiver mode	Error in sync esc in the receiver mode

Table 11: Data lane PPI Control Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_RxStopState [3:0]	Output	Lane is in Stop state for data lane. This active high signal indicates that the lane module is currently in Stop state. Note that this signal is asynchronous to any clock in the PPI interface.	Only the first three bits are used for CPHY. Indicates Lane is in Stop state for data lane. This active high signal indicates that the lane module is currently in Stop state. Note that this signal is asynchronous to any clock in the PPI interface.
dln_tx_UlpsActive Not[3:0]	Output	ULP State (not) Active for data lane . This active low signal is asserted to indicate that the Lane is in ULP state.	Only the first three bits are used for CPHY. Indicates ULP State (not) Active for data lane . This active low signal is asserted to indicate that the Lane is in ULP state.
dln_ErrorSotHS[3:0]	Output	Start-of-Transmission (SoT) Error for data lane . If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of receiver's byte clock. This is considered to be a "soft error" in the leader sequence and confidence in the payload data is reduced.	Only the first three bits are used for CPHY. Indicates Start-of-Transmission (SoT) Error for data lane . If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of RxWordClkHS. This is considered to be a "soft error" in the leader sequence and confidence in the payload data is reduced.
dln_ErrorSotSync	Output	Start-of-Transmission	Only the first three bits are used for

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
HS[3:0]		Synchronization Error for data lane 0. If the high-speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this error signal is asserted for one cycle of receiver's byte clock.	CPHY. Indicates Start-of-Transmission Synchronization Error for data lane 0. If the high-speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this error signal is asserted for one RxWordClkHS
TxSkewCalHS	Input	Initiate the periodic deskew burst at the transmitter. A low-to-high transition on TxSkewCalHS causes the PHY to initiate a de-skew calibration. A high-to-low transition on TxSkewCalHS causes the PHY to stop deskew pattern transmission and initiate an end-of-transmission sequence.	-
RxSkewCalHS	Output	High-Speed Receive Skew Calibration, which indicates the successful deskew operation to the upper layer.	-
dln_ErrContentionLP0	Output	Indicates LP0 contention on lane0.	Indicates LP0 contention on lane0.
dln_ErrContentionLP1	Output	Indicates LP1 contention on lane1.	Indicates LP1 contention on lane1.
dln_rx_ErrControl[3:0]	Output	Indicates Error control assertion in corresponding lane	Only the first three bits are used for CPHY. Indicates Error control assertion in corresponding lane

Table 12: Side Band Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_def_dir	Input	Provides the default direction of the bi-directional lane, 1'b1-receive, 1'b0-transmit.	Provides the default direction of the bi-directional lane, 1'b1-receive, 1'b0-transmit.
cln_pll_locked	Output	Pll locked signal from the Dphy	Pll locked signal from the Dphy

Table 13: Clock Lane PPI Control Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_cnt_hs_prep [7:0]	Input	The period for which HS prepare time should be accommodated for data lane in Byte clock period	The period for which HS prepare time should be accommodated for data lane in Word clock period
dln_cnt_hs_zero[7:0]	Input	The period for which HS prepare time should be accommodated for data lane in Byte clock period	The period for which HS prepare time should be accommodated for data lane in Word clock period
dln_cnt_hs_trail[7:0]	Input	The period for which HS Trail time should be accommodated for data lane in Byte clock period	The period for which HS trail time should be accommodated for data lane in Word clock period
dln_cnt_hs_exit[7:0]	Input	The period for which HS Exit time should be accommodated for data lane in Byte clock period	The period for which HS exit time should be accommodated for data lane in Word clock period
dln_rx_cnt[7:0]	Input	Counter that controls the assertion of enable on the DPHY for data lanein Byte clock period	Counter that controls the assertion of enable on the DPHY for data lane in Word clock period
dln_sync_cnt[7:0]	Input	A timeout value used for sync error detector logic for data lane in Byte clock period	A timeout value used for sync error detector logic for data lane in Word clock period
dln_cnt_lpx[7:0]	Input	The time period in which LP states are driven in Byte clock period	The time period in which LP states are driven in Byte clock period
cln_cnt_hs_trail[7:0]	Input	The period for which HS trail time should be accommodated for clock lane in Byte clock period	-
cln_cnt_hs_exit[	Input	The period for which HS exit	-

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
7:0]		time should be accommodated for clock lane in Byte clock period	
cln_cnt_lpx[7:0]	Input	The time period in which LP states are driven in Byte clock period for clock lane	-
cln_cnt_prep[7:0]	Input	The period for which HS prepare time should be accommodated for clock lane in Byte clock period	-
cln_cnt_zero[7:0]	Input	The period for which HS zero time should be accommodated for clock lane in Byte clock period	-
cln_cnt_pll[15:0]	Input	The count value which is used for the PLL lock time	The count value which is used for the PLL lock time

4.6 Hard Macro Deliverables

- GDS-II
- CDL netlist for LVS
- LVS reports
- DRC and Antenna reports
- LIB files
- User guide and integration guides
- LEF
- Scan-inserted netlist for DFT
- Verification environment with behavioral models
- IBIS models

5 D-PHY v1.1 Physical Interface IP

5.1 Overview

To address the explosive growth in the mobile industry, the Mobile Industry Processor Interface (MIPI®) Alliance was created to define and promote open standards for interfaces to mobile application processors. D-PHY is the physical layer specified for several of the key protocols within the MIPI® family of specifications.

The Arasan D-PHY IP core is fully compliant to the D-PHY specification version 1.1. It supports the MIPI® Camera Serial Interface (CSI-2) and Display Serial Interface (DSI) protocols. It is a universal PHY that can be configured as a transmitter, receiver or transceiver. The D-PHY consists of an analog front end to generate and receive the electrical level signals, and a digital back end to control the I/O functions.

The Arasan D-PHY provides a point to point connection between master and slave or host and device that comply with a relevant MIPI® standard. A typical configuration consists of a clock lane and 1-4 data lanes. The master/host is primarily the source of data and the slave/device is usually the sink of data. The D-PHY lanes can be configured for unidirectional or bidirectional lane operation, originating at the master and terminating at the slave. It can be configured to operate as a master or as a slave. The D-PHY link supports a high speed (HS) mode for fast data traffic and a low power (LP) mode for control transactions. In HS mode, the low swing differential signal is able to support data transfers from 80 Mbps to 1.5 Gbps. In LP mode all wires operate as a single ended line capable of supporting 10 Mbps asynchronous data communications.

The Arasan D-PHY IP core implements the PPI interface recommended by the MIPI® working groups to easily interface to the required protocols.

5.2 Features

- Compliant to MIPI Alliance Standard for D-PHY specification Version 1.1. Supports:
- Synchronous transfer at high speed mode with a bit rate of 80-1500 Mb/s
- Asynchronous transfer at low power mode with a bit rate of 10 Mb/s
- Spaced one hot encoding for Low Power [LP] data
- One byte buffer housed inside the core for both data-out and data-in paths.
- One clock lane and up to four data lanes
- Error detection mechanism for sequence errors and contentions
- Transfer of data in high speed mode
- Ultra low power mode, high speed mode and escape mode.
- Contention detection and turnarounds
- Clock divider unit to generate clock for parallel data reception and transmission from and to the PPI unit.

- Activation and disconnection of high speed terminators for reception and transmission.
- Standard PHY transceiver compliant to MIPI Specification
- Standard PPI interface compliant to MIPI Specification.
- Clock lane unidirectional communication
- On-chip clock generation configurable for either transmitter or a receiver
- Testability for Tx, Rx and PLL
- Configurability of PHY as a master or slave
- Core structured to increase the number of data lanes
- High speed mode in Forward communication

5.3 Architecture

5.3.1 D-PHY Based Interconnect Architecture

Physical connectivity between a master and slave component requires a clock lane and, depending on bandwidth needs, one to four data lanes. To support this, a D-PHY has a Clock Lane Module, and one to four Data Lane Modules. Each of these D-PHY Lane Modules communicates via a differential signal pair to a complementary part on the other side of the Lane Interconnect.

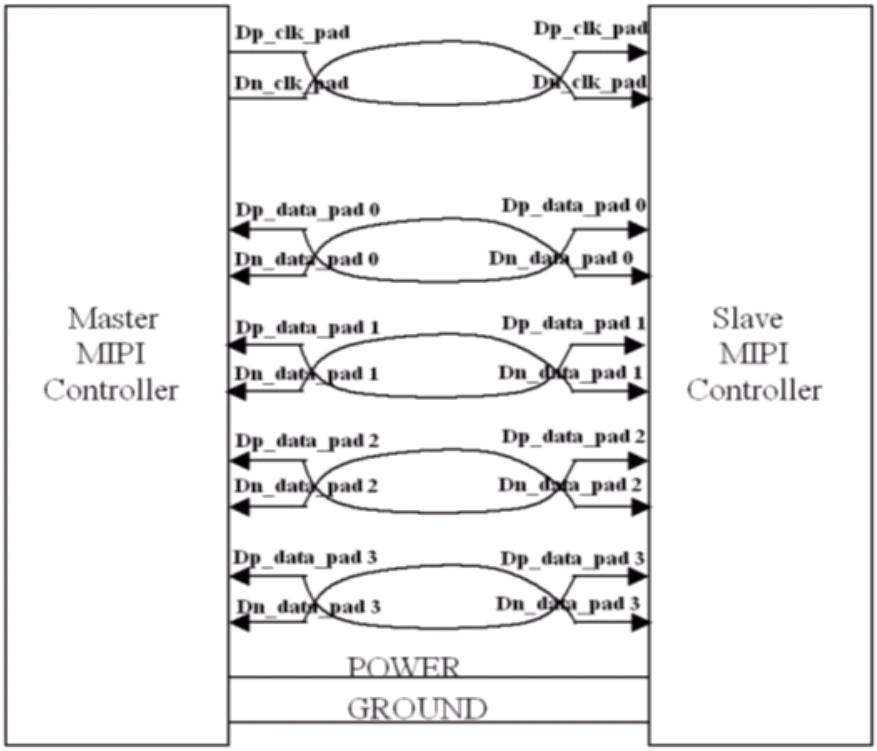

Figure 12: MIPI Link Diagram for Four Data Lanes

5.3.2 D-PHY Lane Architecture

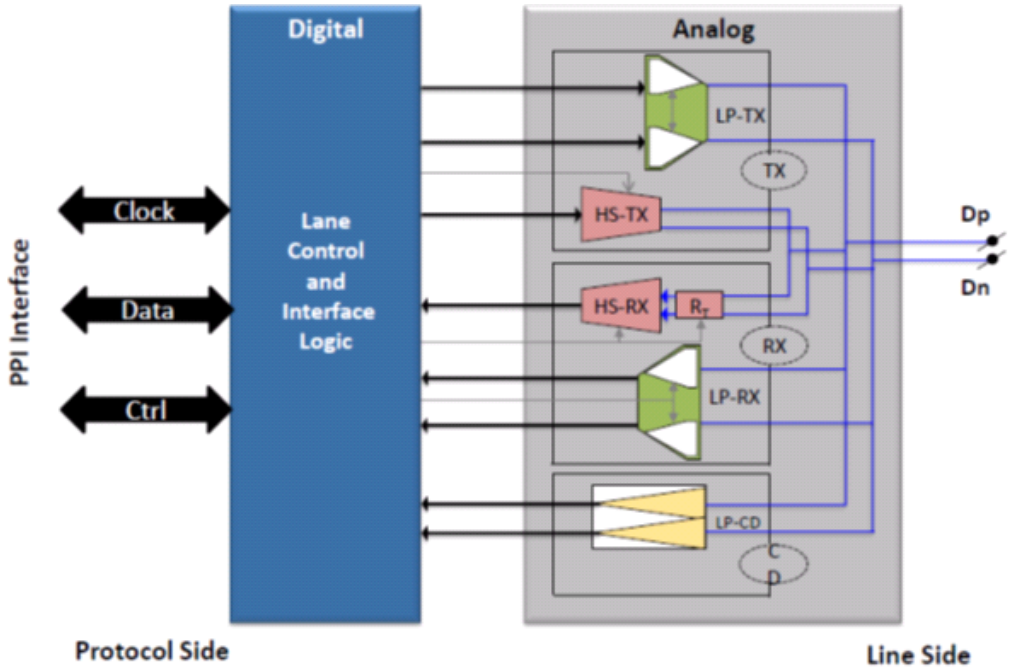

Figure 13: D-PHY Lane Architecture

5.3.2.1 Lane

Each Lane Module has a control and interface logic unit and a transceiver portion to handle differential High-Speed functions utilizing both interconnect wires simultaneously, single-ended Low-Power functions operating on each of the interconnect wires individually and a low power contention detector. The I/O functions are controlled by a Lane Control and Interface Logic block.

5.3.2.2 Signaling

High-Speed signals have a low voltage swing of 200 mV, while Low-Power signals have a large swing of 1.2V. High-Speed functions are used for High-Speed Data traffic. The Low-Power functions are mainly used for control and can have data transfer support.

5.3.2.3 Link

Each link has a Master and a Slave side. The Master provides the High-Speed DDR Clock signal to Clock Lane and is the main data source. The Slave receives the clock signal at the Clock Lane and is the main data sink. This main direction of communication is denoted as the Forward direction. Communication in the opposite direction is called Reverse traffic. Only bi-directional Data Lanes support both forward and reverse communications.

5.3.2.4 Lane Control and Interface Logic

It sends and detects start of packet signalling and end of packet signalling on the data lanes. It has a serializer and de-serializer unit to dialog with the PPI / PHY adapter unit. Also it has clock divider unit to source and receive data during parallel data transfers from and to the PPI.

5.4 Arasan D-PHY Architecture

The transceiver pins of the Arasan D-PHY are compliant to MIPI's transceivers. The lane control and interface logic unit operates with the clock provided by PPI unit during high speed as well as in low power modes of operation in master mode whereas, a separate low power clock is used in slave mode for low power operations and the received high speed clock is used for high speed data transfers.

In Arasan D-PHY digital IP, both Master and slave modes have state machines to generate sequences for switching to high speed, control mode and ultra low power modes. They have deserializer/serializer unit to convert parallel to serial data and vice-versa.

Slave device has sequence observer state machines to know the modes of operation of the lanes. They have sequence error detectors also.

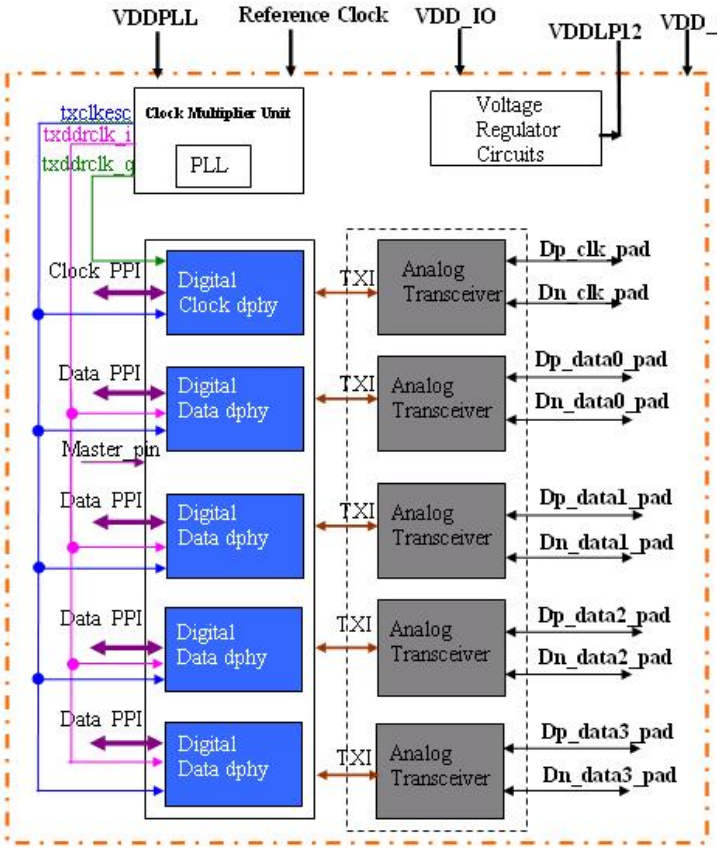

Figure 14: Analog and Digital D-PHY Block Diagram

5.5 D-PHY Pad Table

5.5.1 Functional Description of D-PHY Pads for Clock Lane

Table 14: Functional Description of D-PHY Pads for Clock Lanes

Pin	Direction	Description
dpck	Bidirectional	Positive polarity of low voltage differential clock signal for transmitter and receiver
dnck	Bidirectional	Negative polarity of low voltage differential clock signal for transmitter and receiver

5.5.2 Functional Description of D-PHY Pads for First Data Lane

Table 15: Functional Description of D-PHY Pads for First Data Lane

Pin	Direction	Description
dp0	Bidirectional	Positive polarity of low voltage differential data signal for transmitter and receiver
dn0	Bidirectional	Negative polarity of low voltage differential data signal for transmitter and receiver

5.5.3 Functional Description of D-PHY Pads for Second Data Lane

Table 16: Functional Description of D-PHY Pads for Second Data Lane

Pin	Direction	Description
dp1	Bidirectional	Positive polarity of low voltage differential data signal for transmitter and receiver
dn1	Bidirectional	Negative polarity of low voltage differential data signal for transmitter and receiver

5.5.4 Functional Description of D-PHY Pads for Third Data Lane

Table 17: Functional Description of D-PHY Pads for Third Data Lane

Pin	Direction	Description
dp2	Bidirectional	Positive polarity of low voltage differential data signal for transmitter and receiver
dn2	Bidirectional	Negative polarity of low voltage differential data signal for transmitter and receiver

5.5.5 Functional Description of D-PHY Pads for Fourth Data Lane

Table 18: Functional Description of D-PHY Pads for Fourth Data Lane

Pin	Direction	Description
dp3	Bidirectional	Positive polarity of low voltage differential data signal for transmitter and receiver
dn3	Bidirectional	Negative polarity of low voltage differential data signal for transmitter and receiver

5.5.6 Power Pads

Table 19: Power Pads

Pin	Type	Direction	Description
VDD_clk	Power	InOut	Power pad for Clock lane
VSS_clk	Power	InOut	Ground pad for Clock lane
VDD_d0d1	Power	InOut	Power pad for Data lane 0 and Data lane1
VSS_d0d1	Power	InOut	Ground pad for Data lane 0 and Data lane1
VDD_d2d3	Power	InOut	Power pad for Data lane 2 and Data lane 3
VSS_d2d3	Power	InOut	Ground pad for Data lane 2 and Data lane 3
VDDD	Power	InOut	Power pad for DFE
VSSD	Power	InOut	Ground pad for DFE
VDDLP12	Power	InOut	Power pad for Low power blocks

5.5.7 Functional Description of Trim Bits

Table 20: Ports for Trim_Bits

Pin	Direction	Description
trim_0[31:0]	Input	Trim bits for DPHY
trim_1[31:0]	Input	Trim bits for DPHY
trim_2[31:0]	Input	Trim bits for DPHY
trim_3[31:0]	Input	Trim bits for DPHY

5.5.8 Functional Description of Clock and Reset Unit Input

Table 21: Functional Description of Clock and Reset unit Input signals for clock and data PPI

Pin	Direction	Description
TxClkEsc	Input	Escape mode Transmit Clock. This clock is directly used to generate escape sequences. The period of this clock determines the symbol time for low power signals. This is also the input reference clock for the PLL
enable [Reset]	Input	Active Low system reset to the module.

5.5.9 Functional Description of Data PPI Signals Common to all Data Lanes

Table 22: Functional Description of data PPI signals that are common to all Data Lanes

Pin	Direction	Description
dln_bd_ForceRxmode	Input	Force Lane Module Into Receive mode / Wait for Stop state. This signal forces the state machine into RX mode.
dln_ForceTxStopmode[3:0]	Input	Force Lane Module Into Transmit mode / Generate Stop state. This signal forces STOP signal on the transmit lines.

5.5.10 Functional Description of Clock PPI's Escape Mode Signals

Table 23: Functional Description of Clock PPI's High Speed Interface Signals

Pin	Direction	Description
cln_TxRequestHS	Input	High-Speed Transmit Request and Data Valid for clock lane. For clock Lanes, this active high signal causes the lane module to begin transmitting a high-speed clock.
cln_RxActiveHS	Output	Receiver Clock Active. This asynchronous, active high signal indicates that a clock Lane is receiving a DDR clock signal
TxByteClkHS	Output	High-Speed Transmit Byte Clock. This is used to synchronize PPI signals in the High-Speed transmit clock domain. It is recommended that all transmitting Data Lane Modules share one transmitter's byte clock signal. The frequency of byte clock is exactly 1/8 the High-Speed bit rate This is the txbyteclkhs to which all PPI interface is synchronous for transmitter.

RxByteClkHS	Output	High-Speed Receive Byte Clock. This is used to synchronize signals in the High-Speed receive clock domain. The rxbyteclkhs is generated by dividing the received High-Speed DDR clock This is the byte clock to which all PPI interface is synchronous for receiver.
RxDDRClkHS_0	Output	High speed DDR clock used by the receiver.
cln_TxUlpsExit	Input	Transmit ULP Exit Sequence for clock lane. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when tx_ulpsactivenot_clk_n becomes deasserted. txulpsexit_clk is synchronous to txclkesc. This signal is ignored when the Lane is not in the ULP State
cln_TxUlpsClk	Input	To force the clock lane to transmit ULPS sequences in the clock line.
cln_RxUlpsClkNot	Output	Receive Ultra Low-Power mode on Clock Lane. This active low signal is asserted to indicate that the Clock Lane module has entered the Ultra Low-Power mode. The Lane module remains in this mode with RxUlpsClkNot asserted until a Stop state is detected on the Lane Interconnect
cln_tx_UlpsActive Not	Output	ULP State (not) Active for clock lane. This active low signal is asserted to indicate that the Lane is in ULP state.
cln_rx_UlpsActiveN ot	Output	ULP State (not) Active for clock lane. This active low signal is asserted to indicate that the Lane is in ULP state

5.5.11 Functional Description of Clock PPI's Control Signals

Table 24: Functional Description of Clock PPI's Control Signals

Pin	Direction	Description
cln_Rxstopstate	Output	Lane is in Stop state for clock lane. This active high signal indicates that the lane module is currently in Stop state. This is valid for both receivers and transmitters. Note that this signal is asynchronous to any clock in the PPI interface

5.5.12 Functional Description of Clock PPI's High Speed Interface Signals

Table 25: Functional Description of Data PPI's High Speed Interface signals

Pin	Direction	Description
dln_TxDataHS[31:0]	Input	High-Speed Transmit Data for data lane. High-speed data to be transmitted. Data is captured on rising edges of transmitted byte clock.
dln_TxRequestHS [3:0]	Input	High-Speed Transmit Request and Data Valid for data lane. A low-to-high transition on txrequesths causes the lane module to initiate a Start-of-Transmission sequence. A high-to-low transition on txrequesths causes the lane module to initiate an End-of- Transmission sequence. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on txdatahs_0 to be transmitted. The lane module accepts the data when both txrequesths and txreadyhs are active on the same rising txbyteclkhs clock edge. The protocol always provides valid transmit data when txdatahs_0 is active. Once asserted, txdatahs remains high until the data has been accepted, as indicated by txreadyhs. txdatahs is only asserted while txrequestesc_0 is low
dln_TxReadyHS [3:0]	Output	High-Speed Transmit Ready for data lane. This active high signal indicates that txdatahs_0 is accepted by the lane module to be serially transmitted. txreadyhs_0 is valid on rising edges of transmitted byte clock.
dln_RxDataHS[31:0]	Output	High-Speed Receive Data for data lane. The signal connected to rxdatahs_0 was received first. Data is transferred on rising edges of receiver byte clock.
dln_RxValidHS[3:0]	Output	High-Speed Receive Data Valid for data lane.
dln_RxActiveHS [3:0]	Output	High-Speed Reception Active for data lane. This active high signal indicates that the lane module is actively receiving a high-speed transmission from the lane interconnect.
dln_RxSyncHS[3:0]	Output	Receiver Synchronization Observed for data lane. This active high signal indicates that the Lane module has seen an appropriate synchronization event. In a typical high-speed transmission, rxsynchs_0 is high for one cycle of received byte clock at the beginning of a high-speed transmission when rxactivehs_0 is first asserted, and again for one cycle of received byte clock at the end of a high-speed transmission, just before rxvalidhs_0 returns low.

5.5.13 Functional Description of Data PPI's Escape Mode Signals

Table 26: Functional Description of Data PPI's Escape mode Signals

Pin	Direction	Description
dln_TxRequestEsc [3:0]	Input	Escape mode Transmit Request for data lane . txrequestesc_0 is only asserted by the protocol while txrequesths_0 is low.
dln_TxUlpsExit[3:0]	Input	Transmit ULP Exit Sequence for data lane 0. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when ulpsactivenot_0_n becomes deasserted. txulpsexit_0 is synchronous to txclkesc. This signal is ignored when the Lane is not in the ULP State.
dln_TxUlpsEsc[3:0]	Input	Escape mode Transmit Ultra Low Power for data lane 0. This active high signal is asserted with txrequestesc to cause the lane module to enter the ultra-low power mode. The lane module remains in this mode until txrequestesc_0 is deasserted. txlpdtesc_0 and all bits of txtriggeresc are low when txulpsesc_0 is asserted.
dln_bd_TxLpdtEsc	Input	This signal is used to request a low power data transmission entry in the reverse direction.
dln_bd_TxTriggerEsc[3:0]	Input	A 4 bit signal that triggers a trigger sequence in the ESC mode in the reverse direction.
dln_bd_TxDataEsc [7:0]	Input	In data mode, the 8-bit data to be transmitted in the reverse direction.
dln_bd_TxValidEsc	Input	A valid signal which qualifies for the data lines.
dln_bd_TurnDisable	Input	To avoid the turn-around request during the lock up situation.
dln_bd_Direction	OutPut	To indicate the direction of the data lane. This signal is used to indicate the current direction of the lane interconnect. When direction_0 =0, the lane is in transmit mode (0=Output). When direction_0 =1, the lane is in receive mode (1=Input).
dln_bd_TurnRequest	Input	This signal is used to request a turn-around operation for a bidirectional lane.
dln_rx_RxClkEsc [3:0]	Output	Escape mode Receive Clock for data lane 0. This signal is used to transfer received data to the protocol during escape mode. This "clock" is generated from the two Low-Power signals in the Lane interconnect. Because of the asynchronous nature of Escape mode data transmission, this "clock" may not be periodic.

Pin	Direction	Description
dln_rx_RxUlpsEsc[3:0]	Output	Escape Ultra Low Power (Receive) mode for data lane. This active high signal is asserted to indicate that the lane module has entered the ultra-low power mode. The lane module remains in this mode with rxulpsesc asserted until a Stop state is detected on the lane interconnect.
dln_rx_UlpsActiveNot[3:0]	Output	ULPS signal received on the receiver in the bi-directional lane
dln_bd_TxReadyEsc	Output	Ready signal for the transmit data lines in reverse direction.
dln_rx_RxDataEsc[7:0]	Output	The low power mode data in the Escape mode.
dln_rx_RxValidEsc	Output	The ESC mode valid data.
dln_rx_RxTriggerEsc[3:0]	Output	The Trigger mode receiver signal.
dln_rx_RxLpdtEsc	Output	The low power data transfer for the first lane
dln_rx_ErrEsc	Output	Error on the Escape sequence during receiver
dln_rx_ErrSyncEsc	Output	Error in sync esc in the receiver mode.

5.5.14 Functional Description of Data PPI's Control Signals

Table 27: Functional Description of Data PPI's Control Signals

Pin	Direction	Description
dln_RxStopState[3:0]	Output	Lane is in Stop state for data lane. This active high signal indicates that the lane module is currently in Stop state. Note that this signal is asynchronous to any clock in the PPI interface.
dln_tx_UlpsActiveNot[3:0]	Output	ULP State (not) Active for data lane. This active low signal is asserted to indicate that the Lane is in ULP state.
dln_ErrorSotHS[3:0]	Output	Start-of-Transmission (SoT) Error for data lane. If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of receiver's byte clock. This is considered to be a "soft error" in the leader sequence and confidence in the payload data is reduced.
dln_ErrorSotSyncHS[3:0]	Output	Start-of-Transmission Synchronization Error for data lane 0. If the high-speed SoT leader sequence is corrupted

Pin	Direction	Description
		in a way that proper synchronization cannot be expected, this error signal is asserted for one cycle of receiver's byte clock.
dln_ErrContention LP0	Output	The contention error signal on LP0 line.
dln_ErrContention LP1	Output	The contention error signal on LP1 line.
dln_rx_ErrControl [3:0]	Output	Error control in lane 0 during receiver

5.5.15 Functional Description of Side Band Signals

Table 28: Functional Description of Side Band Signals

Pin	Direction	Description
dln_def_dir	Input	Provides the default direction of the bi-directional lane, 1'b1-receive, 1'b0-transmit.
dln_dpdnswap[3:0]	Input	Enable dp dn swap on data lanes 0 to 3 in HS Tx mode.
cln_pll_locked	Output	Pll locked signal from the Dphy

5.5.16 Functional Description of DFT Signals

Table 29: Functional Description of DFT Signals

Pin	Direction	Description
SCAN_EN	Input	Scan mode Enable.
SCAN_CLK	Input	Scan clock
SA_SCAN	Input	Stuck-At scan mode.
SCAN_IN	Input	Scan input for At-speed scan.
SCAN_OUT	Output	Scan output for At-speed scan.
DFT_sdi_1 to 6	Input	Scan input for At-speed scan.
DFT_sdo_1 to 6	Output	Scan output for At-speed scan.

5.5.17 D-PHY UI Parameter Count Signals

Table 30: D-PHY UI Parameter Count Signals

Pin	Type	Direction	Description
dln_cnt_hs_prep[7:0]	Register	Input	The period for which HS prepare time should be accommodated for data lane[40ns]
dln_cnt_hs_zero[7:0]	Register	Input	count [260ns] for Tclock count.
dln_cnt_hs_trail[7:0]	Register	Input	The period for which HS trailing should be driven for data lane[60ns].
dln_cnt_hs_exit[7:0]	Register	Input	The period for which HS exit state should be maintained for data lane[110ns].
dln_rx_cnt[7:0]	Register	Input	Counter that controls the assertion of enable on the DPHY for data lane
dln_sync_cnt[7:0]	Register	Input	A timeout value used for sync error detector logic for data lane.
dln_cnt_lpx[7:0]	Register	Input	Wait time in byte data for the LPX for data lane.
cln_cnt_hs_trail[7:0]	Register	Input	Wait time in byte clock for the trailing bits for clock lane[60ns].
cln_cnt_hs_exit[7:0]	Register	Input	wait time in byte clock for the exit state for clock lane[110ns]
cln_cnt_lpx[7:0]	Register	Input	wait time in byte clock for the LPX for clock lane.
cln_cnt_prep[7:0]	Register	Input	wait time in byte clock for the prepare time for clock lane[40ns]
cln_cnt_zero[7:0]	Register	Input	wait time in byte clock for the zero state for clock lane[260ns].
cln_cnt_pll[15:0]	Register	Input	The count value which is used for the PLL lock time.
dln_cnt_lpx[7:0]	Register	Input	The period for which the LP state should be driven.

5.5.18 A-BIST Related Signals

Table 31: A-BIST Pins

Pin	Direction	Description
dln_loop_back	Input	Enable A-BIST (loopback BIST)
bist_seed[7:0]	Input	BIST PRBS intiation seed
bist_force_error	Input	Signal is used to introduce errors in the BIST run.

Pin	Direction	Description
bist_en_esc_lp, bist_en_esc_hs	Input	Bist mode selection pins 00-> Reserved 01-> HS Mode 10-> LP Mode 11-> RxClkEsc Generation
bist_err_rx_hs	Output	Error in HS reception
bist_err_rx_hs_sync	Output	Error in RX HS sync
bist_err_rx_esc	Output	Error in LP reception
bist_err_rx_esc_ sync	Output	Error in LP rx sync
bist_done	Output	End of BIST comparison

5.6 Hard Macro Deliverables

- GDS-II
- CDL netlist for LVS
- LVS reports
- DRC and Antenna reports
- LIB files
- User-guide and integration guides
- LEF
- Scan-inserted netlist for DFT
- Verification Environment with behavioral models

6 Services & Support

6.1 Global Support

Arasan Chip Systems provide global support to its IP customers. The technical support is not geographically bound to any specific site or location, and therefore our customers can easily get support for design teams that are distributed in several locations at no extra cost.

6.2 Arasan Support Team

Our technical support is provided by the engineers who have designed the IP. That is a huge benefit for our customers, who can communicate directly with the engineers who have the deepest knowledge and domain expertise of the IP, and the standard to which it complies.

6.3 Professional Services & Customization

At Arasan Chip Systems we understand that no two Application Processors are the same. We realize that often the standard itself needs some tweaks and optimizations to fit your design better. Sometimes, the interface between the IP blocks and your design need some customization. Therefore, we provide professional services and customization to our IP customers. We do not sell our IP blocks as “black box” that cannot be touched. Please contact us for more details on our customization services.

6.4 The Arasan Porting Engine

Analog IP blocks, such as eMMC 5.1 HS400 PHY, are designed for a specific Fab and process technology. Arasan’s analog design team, utilizing its deep domain expertise and vast experience, is capable of porting the PHYs into any specific process technology required by the customer. That is “The Arasan Porting Engine”.

6.5 Pricing & Licensing

Arasan charges a one-time licensing fee, with no additional royalties. The licensing fee gives the right to use our IP for 1 project. Licensing fee for additional projects, using the same IP, is discounted. We also offer unlimited-use license. For any additional information regarding pricing and licensing – please contact our sales at: sales@arasan.com.