Group 04
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COMPARISON REPORT
CO224 LAB 06 -PART 2

INITIAL READING/WRITING PROCESS

Processor with data memory	**Processor with data memory and cache**
Data memory reading/writing will happen. It will take 40(5 clock cycles) time units to read/write process.	Data memory writing, Data memory reading, writing memory block to the cache which is read and writing the data word to the memory/ reading the corresponding data word should be done. This consumes 41 clock cycles

Therefore when comparing Processor with cache and without cache it takes less time to read/ write process without the cache implementation for the first time

READ HIT/WRITE HIT

Processor with data memory	**Processor with data memory and cache**
1.Data memory reading/writing will happen It will take 40 (5 clock cycles)time units to read/write process. 2.Cpu is stalled when reading/writing from the data memory	1.It gets Only one clock cycle to finish the read/write process. Time consumes for, extracting tag,valid bit,dirty bit, to decide hit status and tp reading the corresponding word/ writing the data word to the cache. 2.Cpu is not stalled when reading/writing from the cache

Therefore when comparing Processor with cache and without cache it takes more time to read hit/ write hit process without the cache.

READ MISS/WRITE MISS
DIRTY BIT=0

Processor with data memory	**Processor with data memory and cache**
Data memory reading/writing will happen This takes 40 time units(5 clock cycles)	writing the data word to the memory/reading the corresponding data word should be done. This takes 21 clock cycles

Therefore when comparing Processor with cache and without cache it takes more time to read miss/ write miss(dirty bit=0) process with the cache.

READ MISS/WRITE MISS
DIRTY BIT=1

Processor with data memory	**Processor with data memory and cache**
Data memory reading/writing should be done Takes 40 time units	Data memory writing, Data memory reading, writing memory block to the cache which is read and writing the data word to the memory/ reading the corresponding data word should be done. This consumes 41 clock cycles

Therefore when comparing Processor with cache and without cache it takes more time to read miss/ write miss(dirty bit=1) process with the cache.

So,altogether we can say that the processor with cache implementation is very efficient relative to the without cache implementation when we can obtain high hit rate.