POLYBEE

PARTIE GATEWAY ET ALIMENTATION

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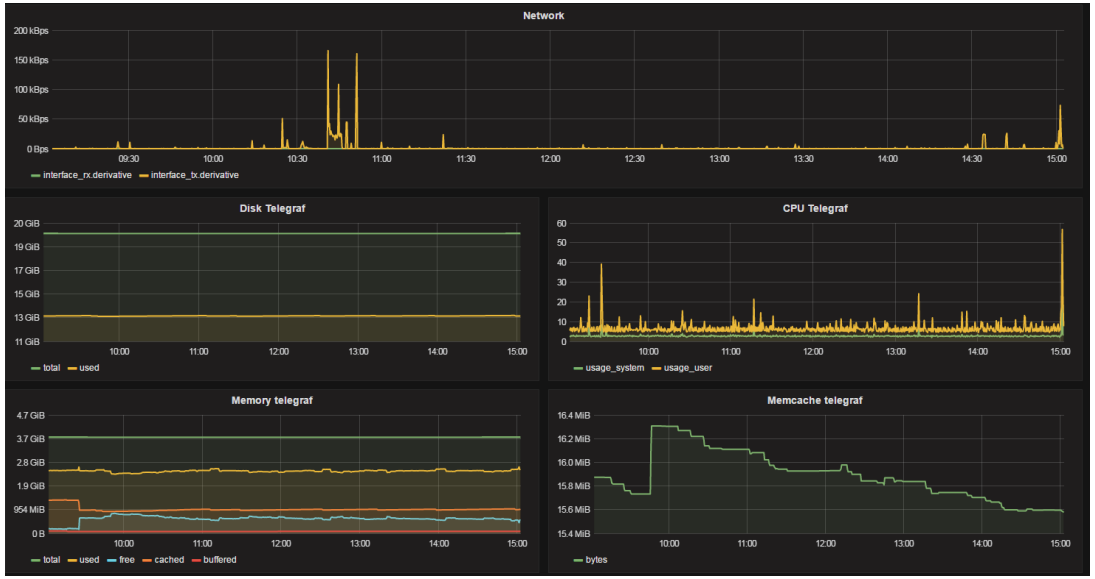
INTRODUCTION



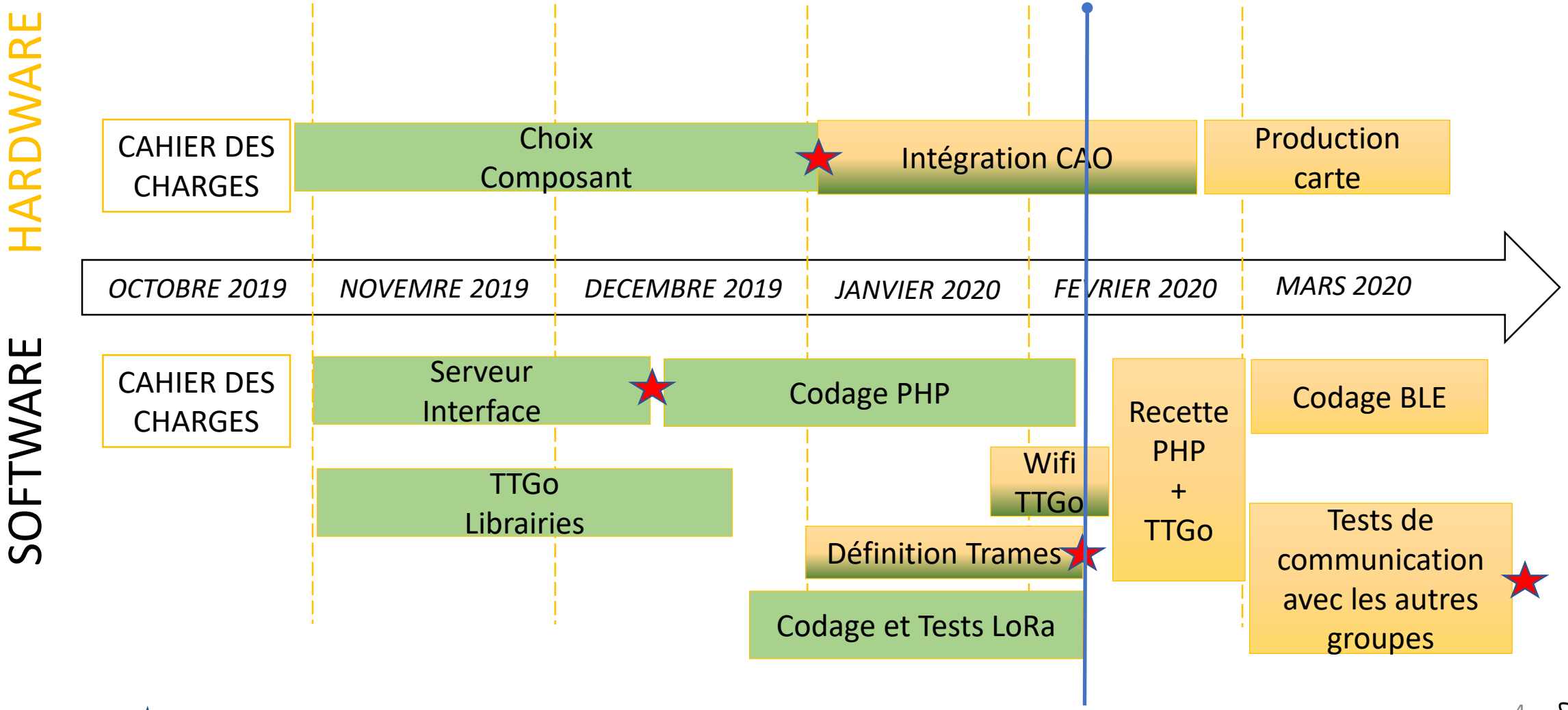
OBJECTIFS : - Communiquer avec vos modules grâce aux carte TTGO LoRa

- Fournir une carte d'alimentation aux différents modules

SOMMAIRE

1. MACRO PLANING
2. HARDWARE
   - Choix des composants
   - Etude des composants
3. SOFTWARE
   - LoRa
   - Versions et compatibilités des cartes TTGo
   - Partie Serveur
     - Comparatif des protocoles
     - Schéma de connectivité
     - Séquences PHP
   - Gateway
     - Séquences Fonctionnelles
4. CONCLUSION

1. MACRO PLANING



Points clé

3. HARDWARE

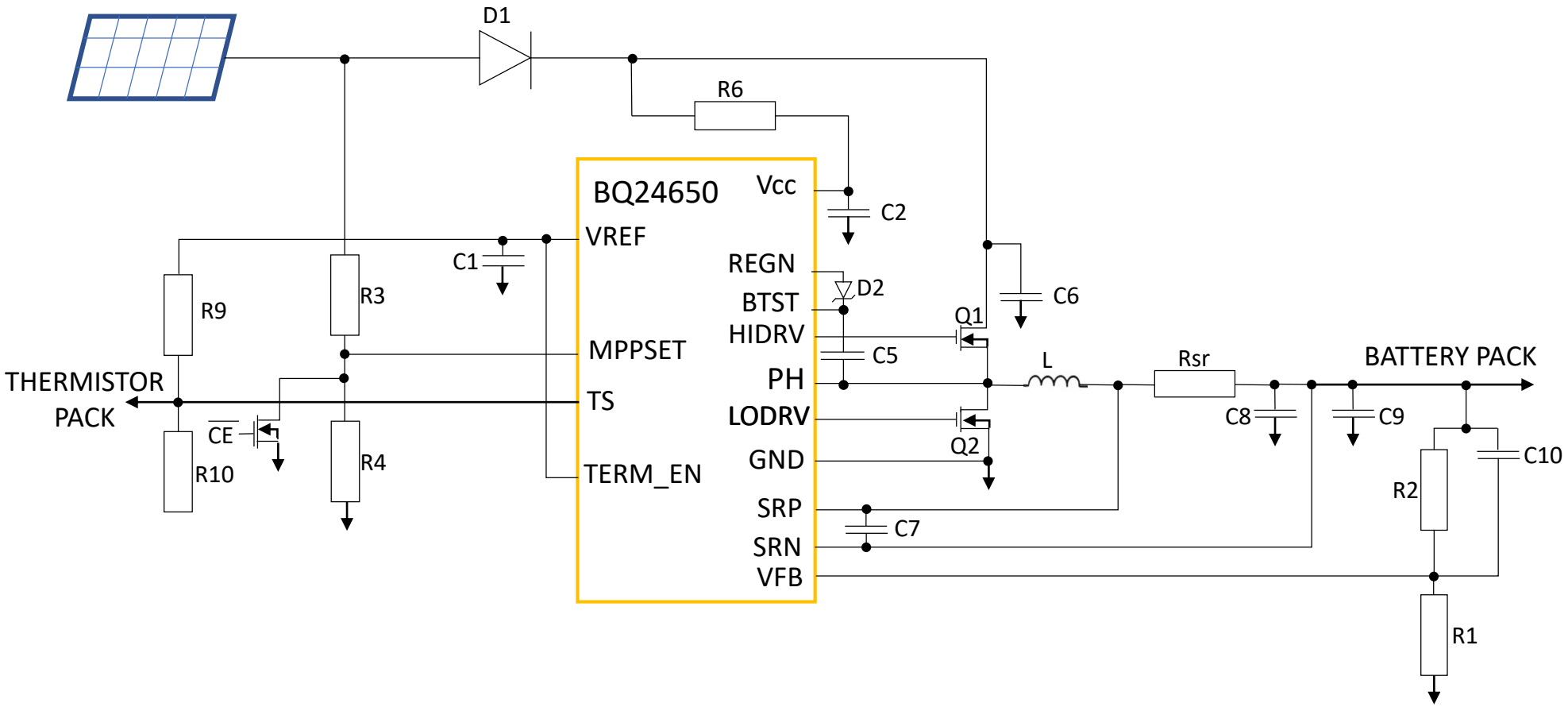
Choix des composants

- Bq24650
  - Panneau solaire
  - Contrôleur de charge

- MAX17263
  - Indicateur de charge :
    - Compteurs de coulomb
    - I2C
  - LiFePO4 jusqu'à 4 éléments en //

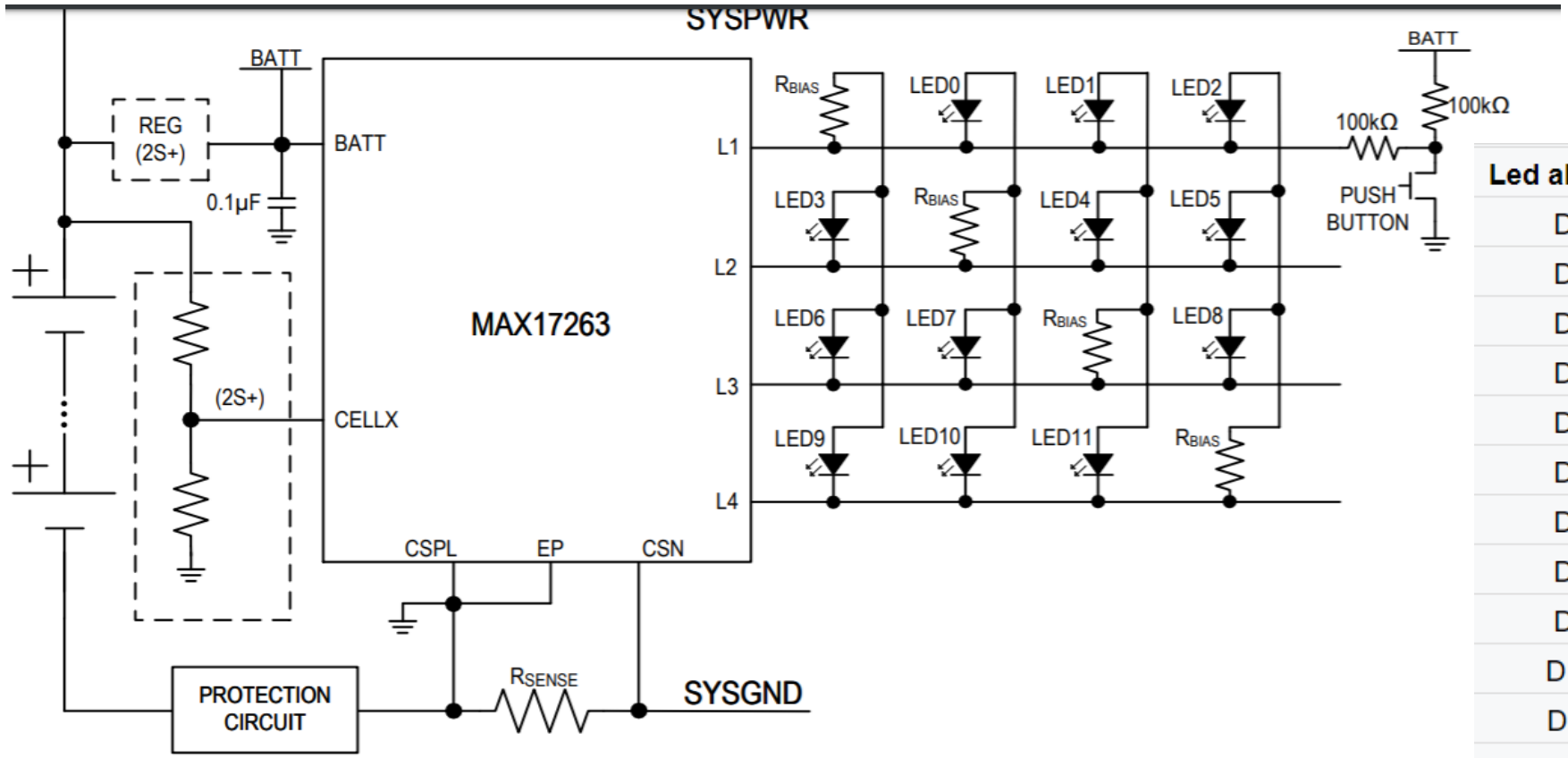
3. HARDWARE

Etude des composants : BQ24650



3. HARDWARE

Etude des composants : MAX17263



Led allumée	L1	L2	L3	L4
D1	H	L	Z	Z
D2	L	H	Z	Z
D3	H	Z	L	Z
D4	L	Z	H	Z
D5	H	Z	Z	L
D6	L	Z	Z	H
D7	Z	H	L	Z
D8	Z	L	H	Z
D9	Z	H	Z	L
D10	Z	L	Z	H
D11	Z	Z	H	L
D12	Z	Z	L	H

4. SOFTWARE

LoRa

- Recherches de librairies
  - Tests d'envois et de réceptions
    - Activation du CRC
      - Programme de mise en trame des données

4. SOFTWARE

Recherche des librairies

- Librairies ESP32: travaille avec les registres de l'esp32 dans l'environnement Arduino
- Adafruit GFX Library: gère l'affichage de l'ecran
- Librairie LoRa: Communiquer avec le module LoRa depuis l'esp32

4. SOFTWARE

Test envoi et réception LoRa

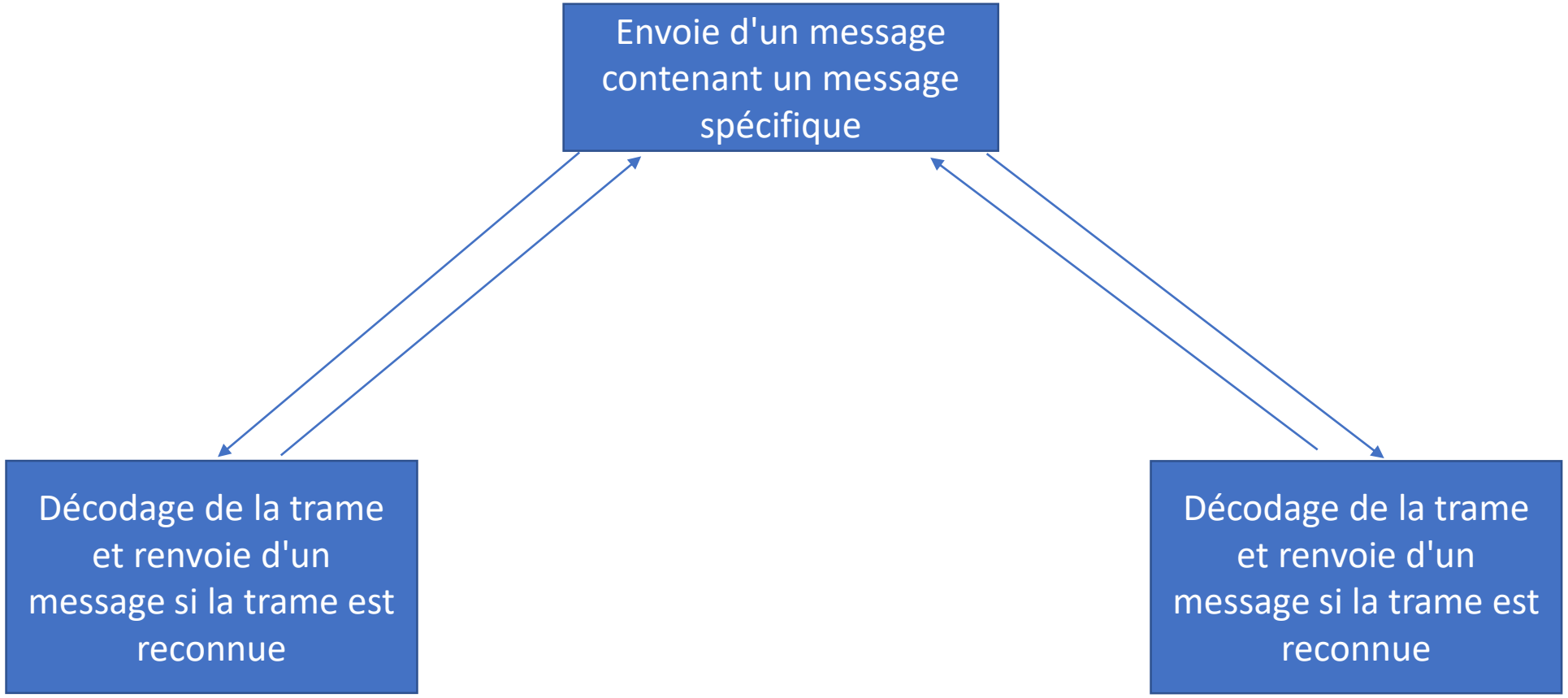
4. SOFTWARE

Lecture CRC dans le registre

RegIrqFlags2 (0x3f)	7	FifoFull	r	-	Set when FIFO is full (i.e. contains 66 bytes), else cleared.
	6	FifoEmpty	r	-	Set when FIFO is empty, and cleared when there is at least 1 byte in the FIFO.
	5	FifoLevel	r	-	Set when the number of bytes in the FIFO strictly exceeds *FifoThreshold*, else cleared.
	4	FifoOverrun	rwc	-	Set when FIFO overrun occurs. (except in Sleep mode) Flag(s) and FIFO are cleared when this bit is set. The FIFO then becomes immediately available for the next transmission / reception.
	3	PacketSent	r	-	Set in Tx when the complete packet has been sent. Cleared when exiting Tx
	2	PayloadReady	r	-	Set in Rx when the payload is ready (i.e. last byte received and CRC, if enabled and *CrcAutoClearOff* is cleared, is Ok). Cleared when FIFO is empty.
	1	CrcOk	r	-	Set in Rx when the CRC of the payload is Ok. Cleared when FIFO is empty.
	0	LowBat	rwc	-	Set when the battery voltage drops below the Low Battery threshold. Cleared only when set to 1 by the user.

4. SOFTWARE

Test du CRC et identification de l'émetteur



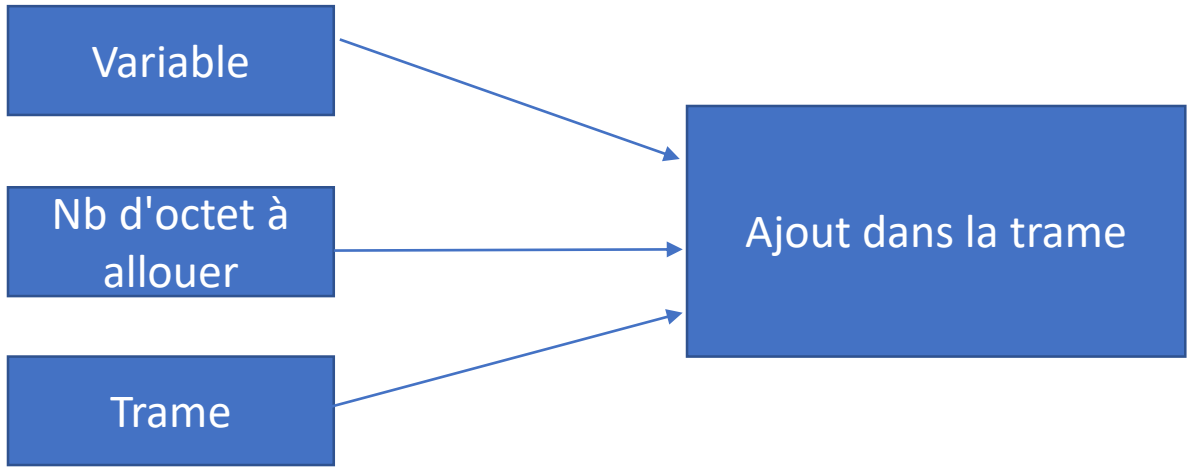
4. SOFTWARE

Définition des différentes trames

Définition des trames à envoyer

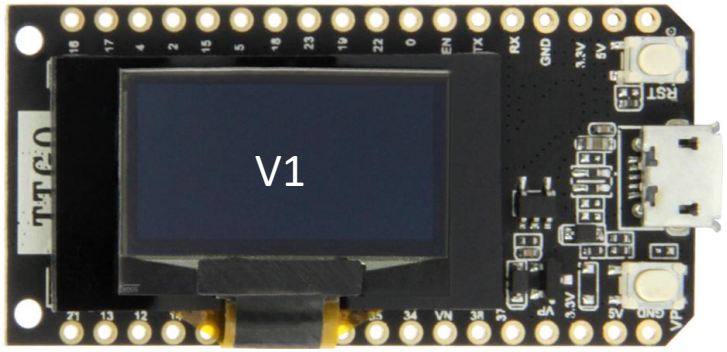
Adresse MAC						Type	n° ruche	octet 1	octet 2	octet 3	octet 4
Addr5	Addr4	Addr3	Addr2	Addr1	Addr0	Meteo	n° ruche	Pression			
						Meteo	n° ruche	pression3	pression2	pression1	pression0

Programme pour mettre en forme la trame en fonction de la taille des variable à rentrer:



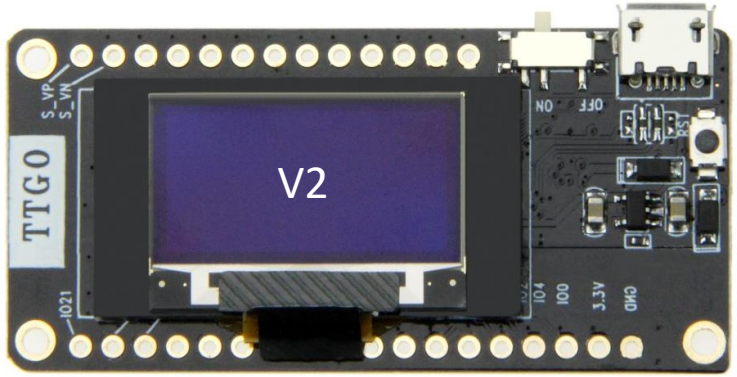
4. SOFTWARE

Versions et compatibilités des cartes TTGo



https://github.com/LilyGO/TTGO-T2-ESP32

ESP32
Wifi
BLE
LoRa
Oled



https://github.com/LilyGO/TTGO-LORA32

ESP32-Pico-D4
+Lecteur carte SD
Wifi
BLE
LoRa
Oled

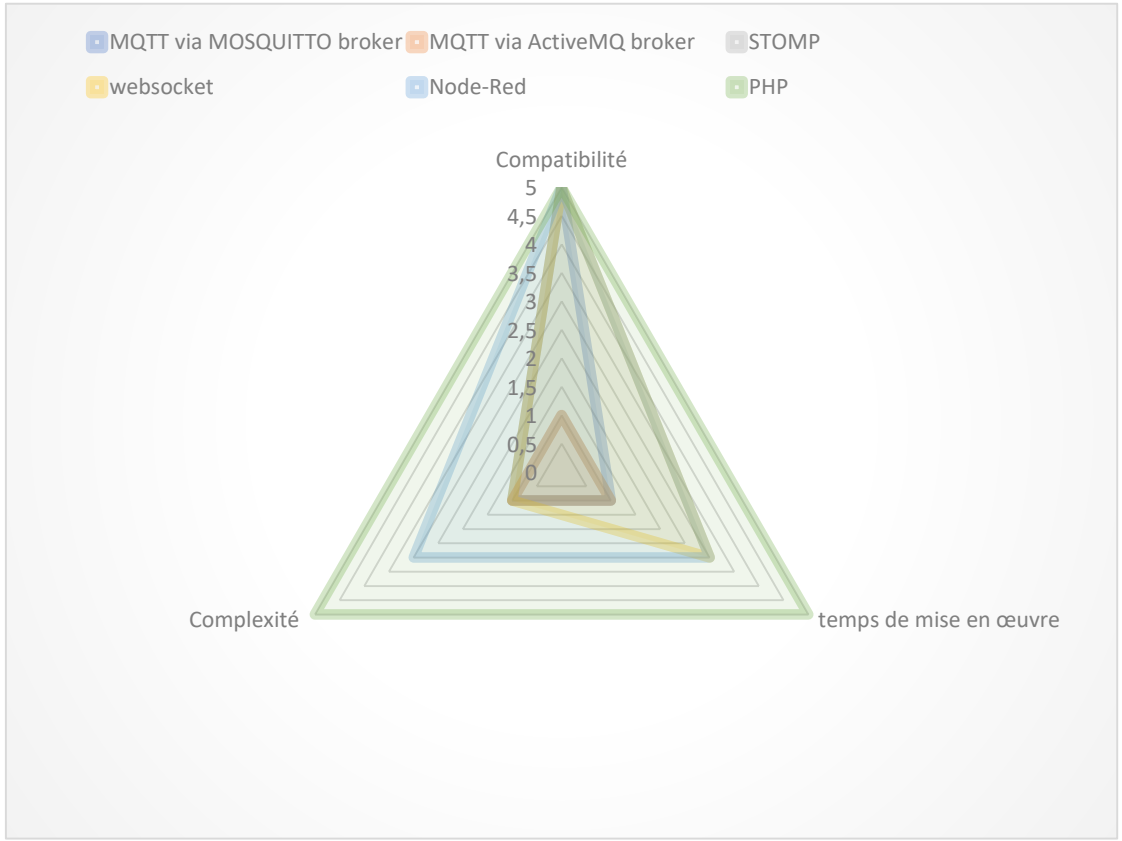
Deux versions différentes

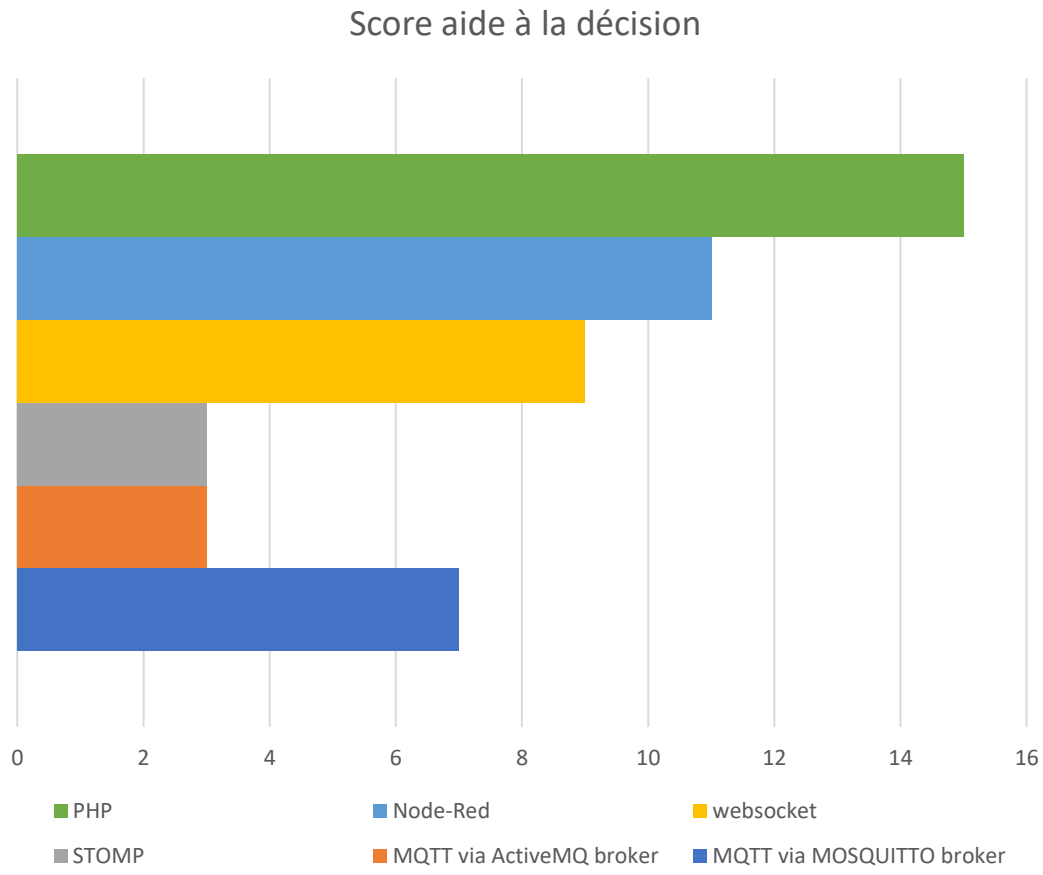
Beaucoup de librairies logicielles V1

Sources officielles fiables

4. SOFTWARE

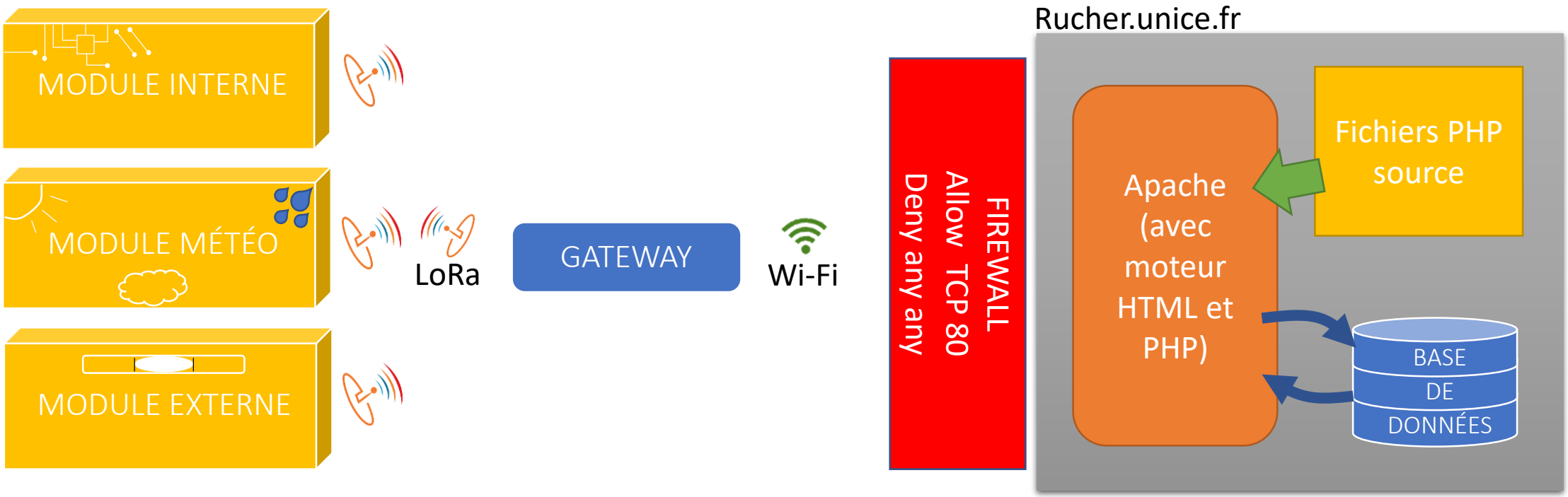
Serveur : Comparatif des protocoles





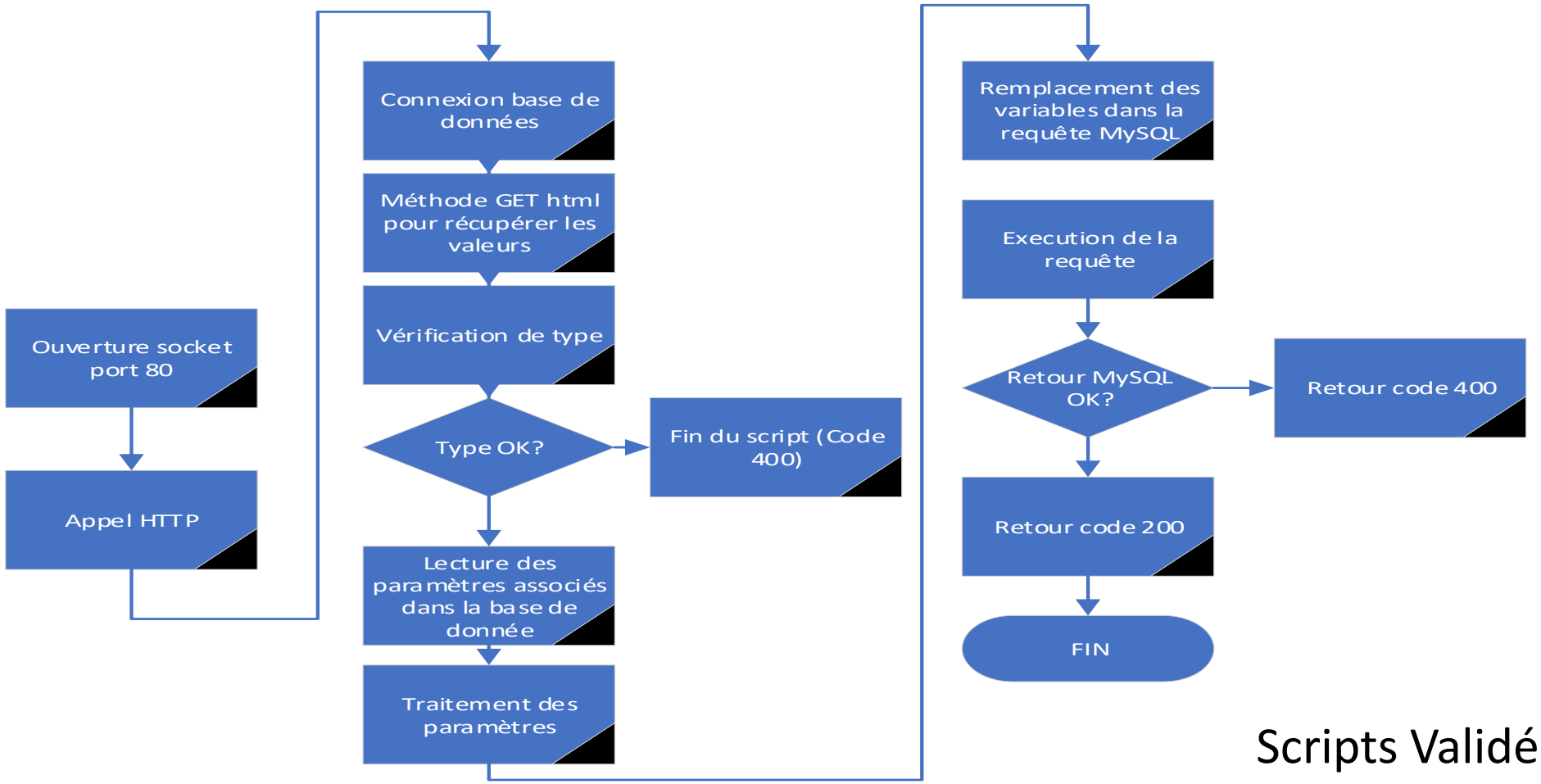
4. SOFTWARE

Serveur : Schéma des connectivités



4. SOFTWARE

Serveur : Séquences PHP

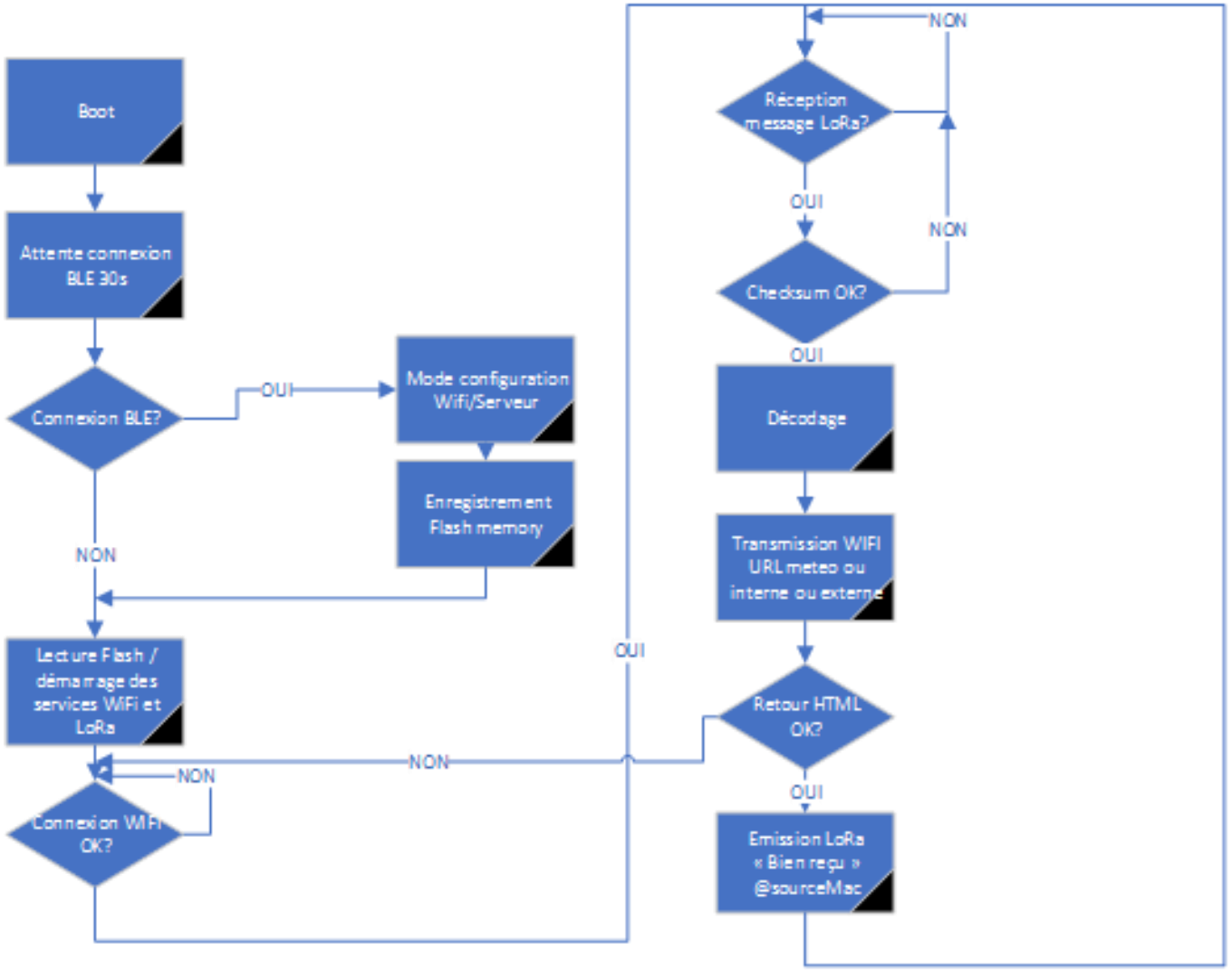


Scripts Validés!

https://fr.wikipedia.org/wiki/Liste_des_codes_HTTP

4. SOFTWARE

Gateway : Séquences fonctionnelles



5. CONCLUSION

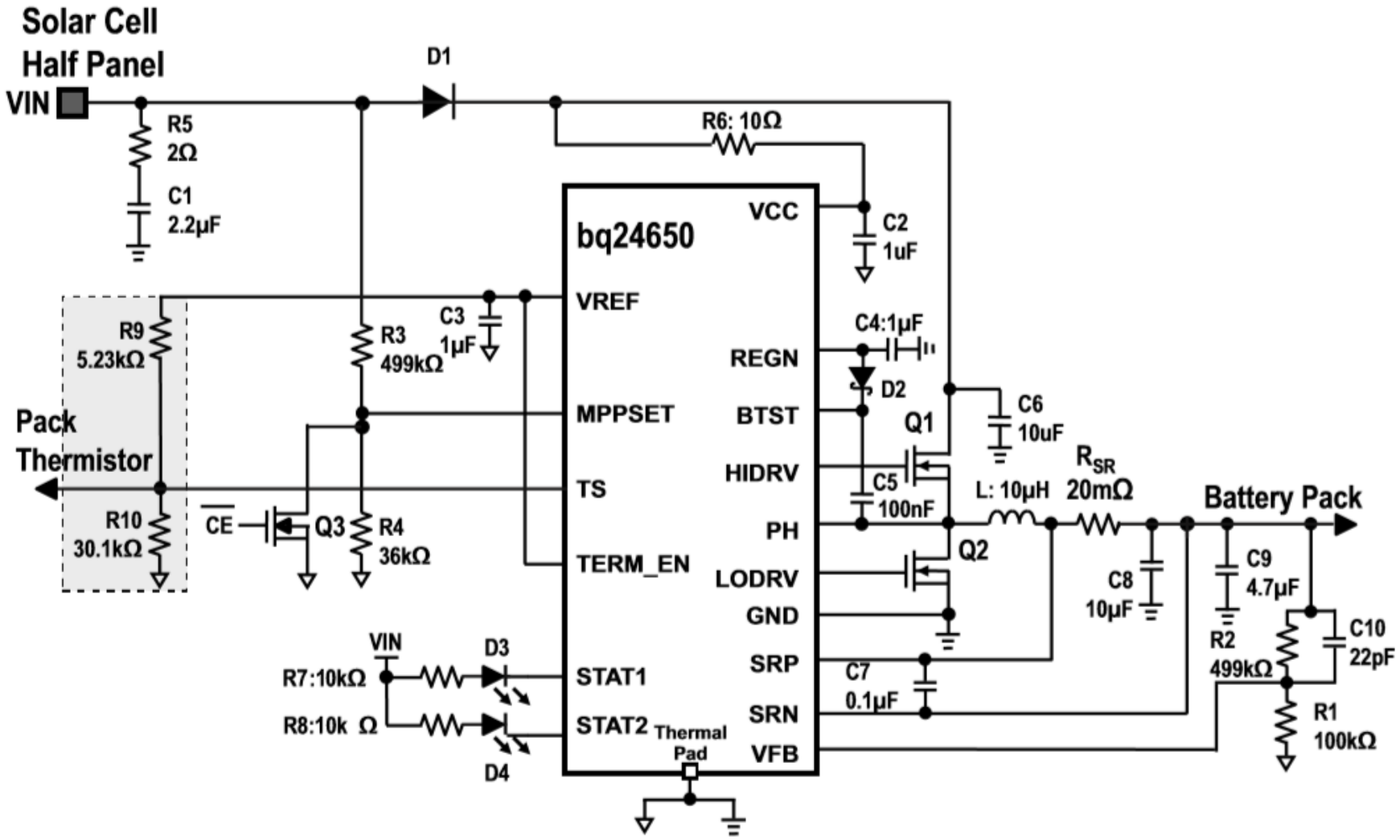
FAIT

- ✓ Composants validés
- ✓ Partie logicielle vers le serveur
- ✓ Format d'échange des trames

A FAIRE

- ➢ Configuration à valider
- ➢ PCB à produire
- ➢ Trames à partager et mettre à jour collectivement
- ➢ Tester les échanges LoRa avec chaque groupe

ANNEXES



ANNEXES

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Pin Functions

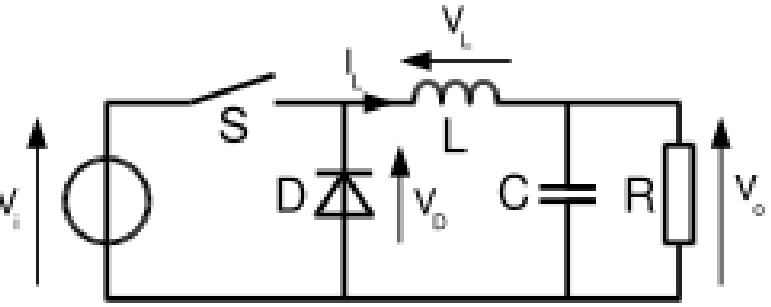
PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VCC	P	IC power positive supply. Place a 1-µF ceramic capacitor from VCC to GND and place it as close as possible to IC. Place a 10-Ω resistor from input side to VCC pin to filter the noise.
2	MPPSET	I	Input voltage set point. Use a voltage divider from input source to GND to set voltage on MPPSET to 1.2 V. To disable charge, pull MPPSET below 75 mV.
3	STAT1	O	Open-drain charge status output to indicate various charger operation. Connect to the cathode of LED with 10 kΩ to the pullup rail. LOW or LED light up indicates charge in progress. Otherwise stays HI or LED stays off. When any fault condition occurs, both STAT1 and STAT2 are HI, or both LEDs are off.
4	TS	I	Temperature qualification voltage input. Connect to a negative temperature coefficient thermistor. Program the hot and cold temperature window with a resistor divider from VREF to TS to GND. A 103AT-2 thermister is recommended.
5	STAT2	O	Open-drain charge status output to indicate various charger operation. Connect to the cathode of LED with 10 kΩ to the pullup rail. LOW or LED light up indicates charge is complete. Otherwise, stays HI or LED stays off. When any fault condition occurs, both STAT1 and STAT2 are HI, or both LEDs are off.
6	VREF	P	3.3-V reference voltage output. Place a 1-µF ceramic capacitor from VREF to GND pin close to the IC. This voltage could be used for programming voltage on TS and the pullup rail of STAT1 and STAT2.
7	TERM_EN	I	Charge termination enable. Pull TERM_EN to GND to disable charge termination. Pull TERM_EN to VREF to allow charge termination. TERM_EN must be terminated and cannot be left floating.
8	VFB	I	Charge voltage analog feedback adjustment. Connect the output of a resistor divider powered from the battery terminals to this node to adjust the output battery voltage regulation.

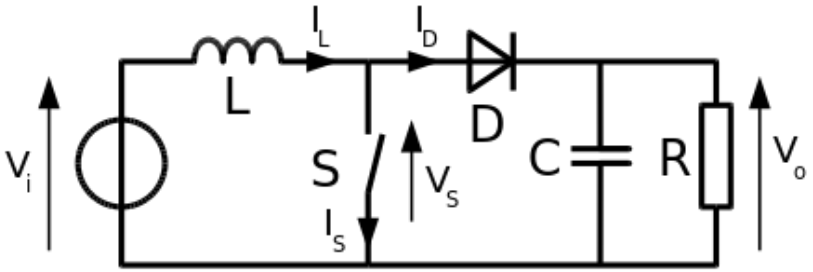
ANNEXES

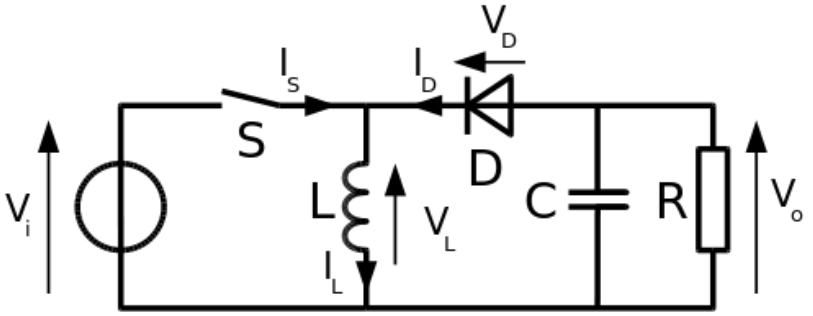
PIN		TYPE	DESCRIPTION
NO.	NAME		
9	SRN	I	Charge current sense resistor, negative input. A 0.1-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. An optional 0.1-µF ceramic capacitor is placed from SRN to GND for common-mode filtering.
10	SRP	P/I	Charge current sense resistor, positive input. A 0.1-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from SRP to GND for common-mode filtering.
11	GND	P	Power ground. Ground connection for high-current power converter node. On PCB layout, connect directly to source of low-side power MOSFET, to ground connection of input and output capacitors of the charger. Only connect to GND through the thermal pad underneath the IC.
12	REGN	P	PWM low-side driver positive 6-V supply output. Connect a 1-µF ceramic capacitor from REGN to GND, close to the IC. Use to drive low-side driver and high-side driver bootstrap Schottky diode from REGN to BTST.
13	LODRV	O	PWM low-side driver output. Connect to the gate of the low-side N-channel power MOSFET with a short trace.
14	PH	P	Switching node, charge current output inductor connection. Connect the 0.1-µF bootstrap capacitor from PH to BTST.
15	HIDRV	O	PWM high-side driver output. Connect to the gate of the high-side N-channel power MOSFET with a short trace.
16	BTST	P	PWM high-side driver positive supply. Connect the 0.1-µF bootstrap capacitor from PH to BTST.
—	Thermal Pad	—	Exposed pad beneath the IC. The thermal pad must always be soldered to the board and have the vias on the thermal pad plane star-connecting to GND and ground plane for high-current power converter. It also serves as a thermal pad to dissipate heat.

ANNEXES

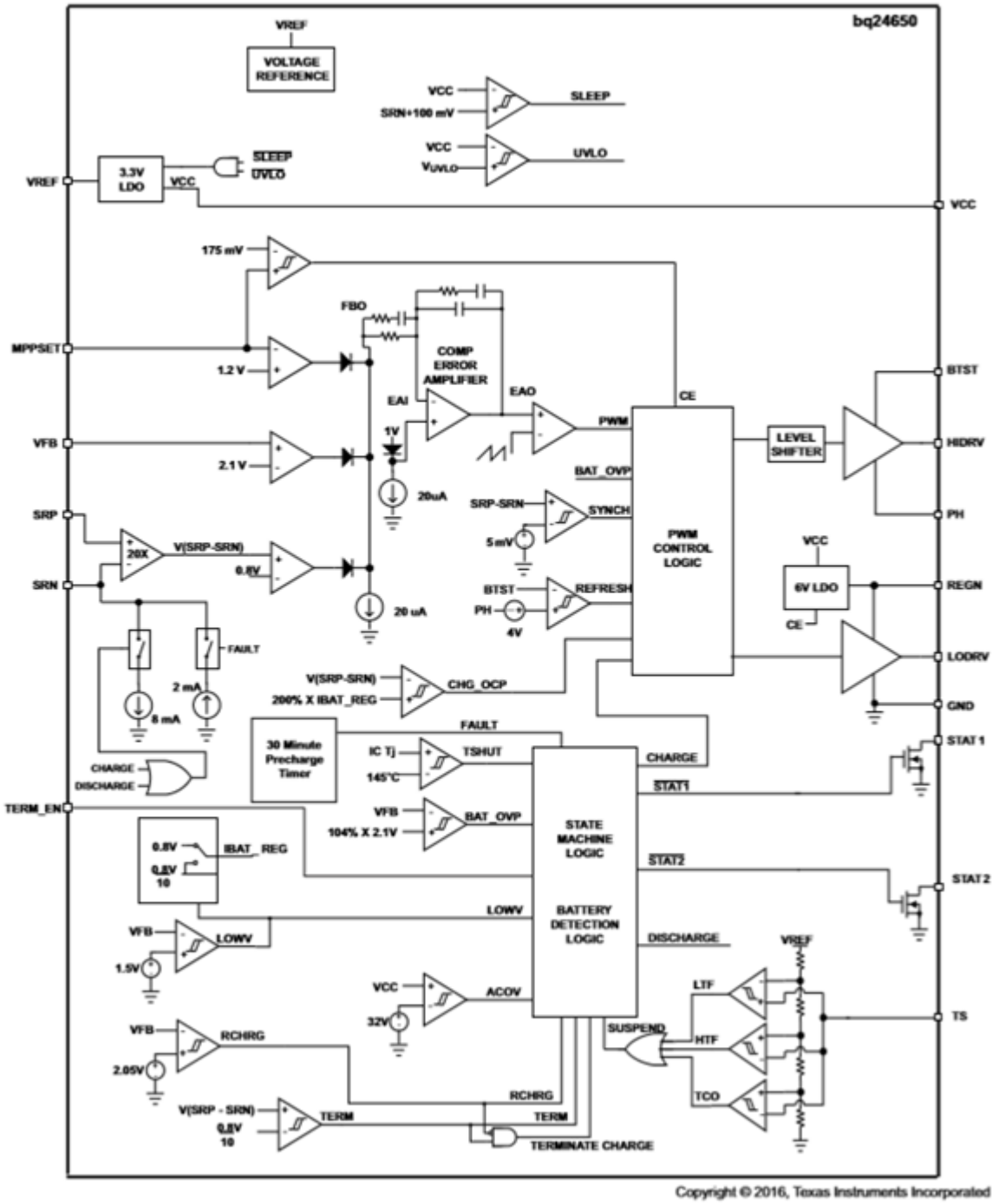
Alimentation a découpage



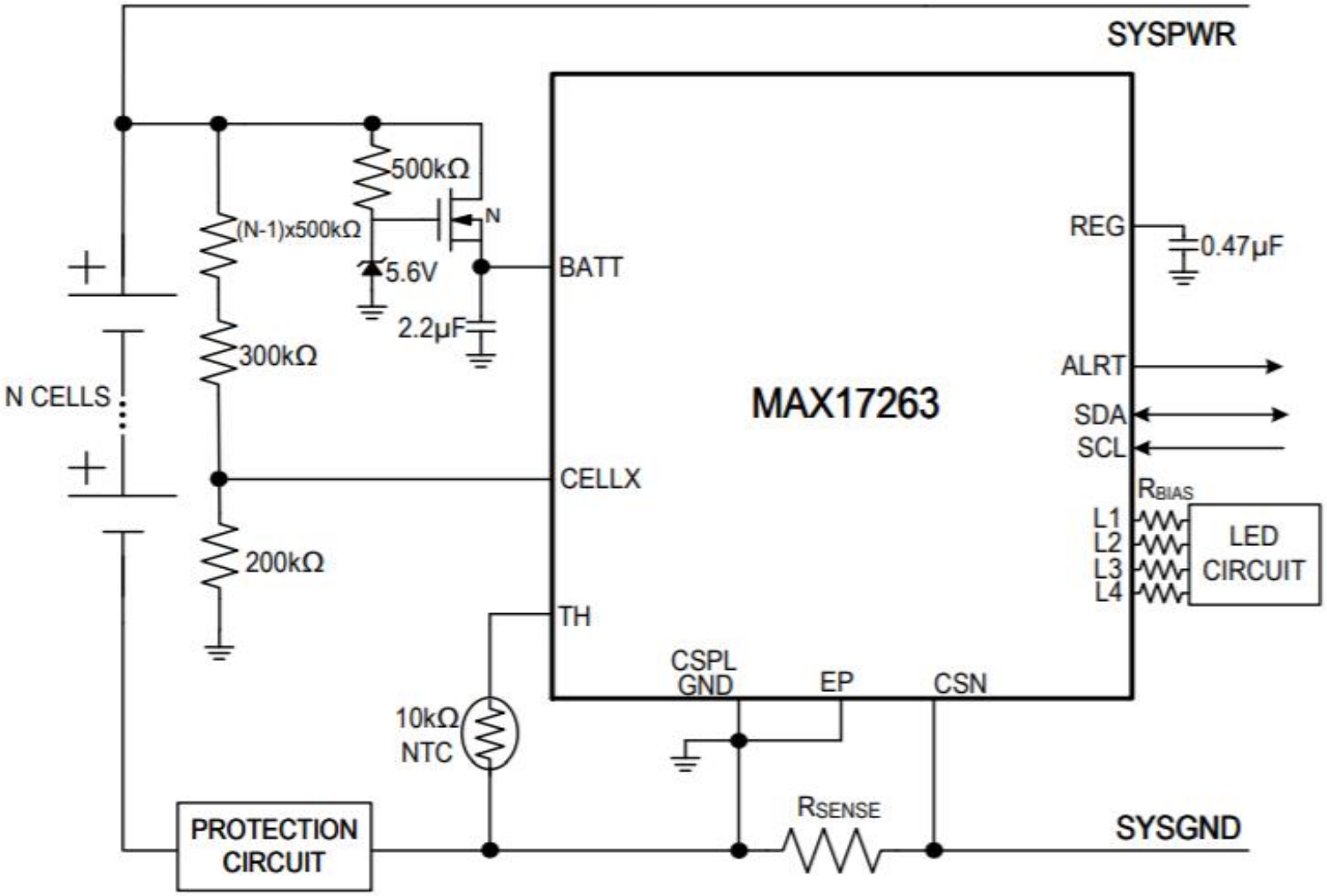




ANNEXES



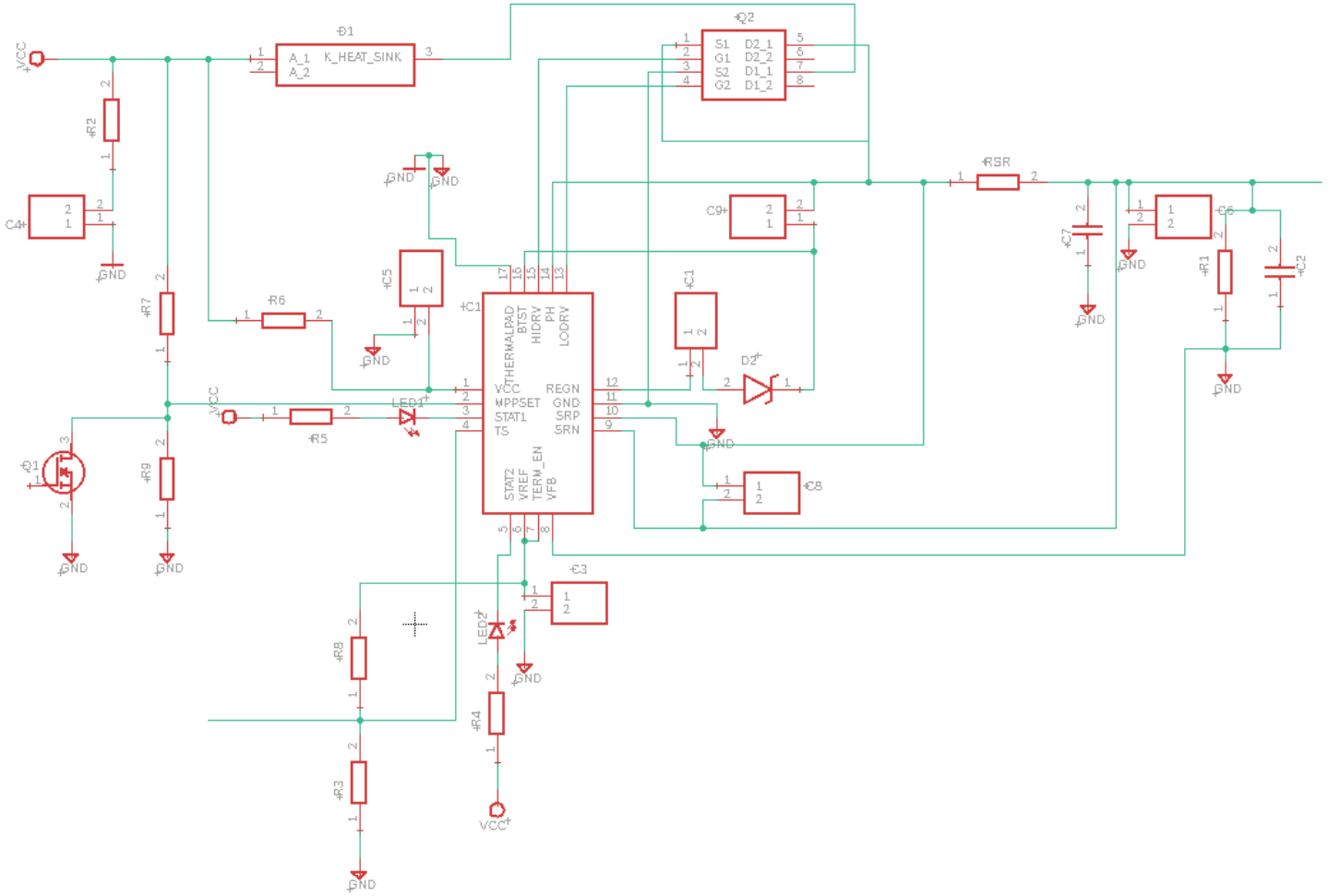
ANNEXES

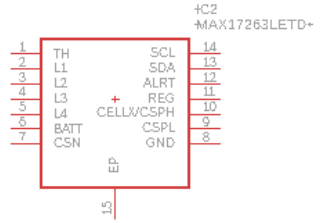

SYSPWR
500kΩ
(N-1)x500kΩ
N
5.6V
2.2µF
BATT
300kΩ
N CELLS
CELLX
200kΩ
TH
10kΩ
NTC
PROTECTION
CIRCUIT
MAX17263
REG
0.47µF
ALRT
SDA
SCL
RBIAS
L1
L2
L3
L4
LED
CIRCUIT
CSPL
GND
EP
CSN
RSENSE
SYSGND

ANNEXES

PIN	NAME	FUNCTION
1	TH	Thermistor Input. Connect a thermistor from TH to GND. TH also provides battery insertion/removal detection. Connect to BATT if not used.
14	SCL	Serial Clock Input. 2-wire clock line. Input only. SCL has an internal pulldown (I_{PD}) for sensing disconnection.
13	SDA	Serial Data Input/Output. 2-wire data line. Open-drain output driver. SDA has an internal pulldown (I_{PD}) for sensing disconnection.
7	CSN	Sense Resistor Negative Sense Point. On start up, the CSN voltage is measured to determine whether it is a high-side or low-side application. For a low-side application, Kelvin connect to the system side of the sense resistor; for a high-side application, Kelvin connect to the cell side of the sense resistor.
10	CELLX/ CSPH	Multiple Function Pin. In multi-cell application, connect to an external voltage divider circuit to measure 40% of 1-cell voltage. In single cell high-side current measurement, Kelvin connect to the system side of the sense resistor. For single cell low-side current measurement application, connect to the BATT pin.
9	CSPL	Low-Side Sense Resistor Positive Sense Point. Kelvin connect to the cell side of the sense resistor.
6	BATT	IC Power Supply. For single cell applications, connect to the positive terminal of a battery cell. For multiple-series cells, connect to an external voltage regulator. Bypass with a 0.1µF capacitor to GND.
8	GND	IC Ground.
11	REG	Internal 1.8V Regulator Output. Bypass with an external 0.47µF capacitor to GND. Do not load externally.
12	ALRT	Alert Output. The ALRT pin is an open-drain active-low output which indicates fuel-gauge alerts. Connect to GND if not used.
2	L1	LED Push/Pull/Tri-state Driver Pin. Input for push-button LED control.
3	L2	LED Push/Pull/Tri-state Driver Pin.
4	L3	LED Push/Pull/Tri-state Driver Pin
5	L4	LED Push/Pull/Tri-state Driver Pin

ANNEXES


D1
A_1
A_2
K_HEAT_SINK
Q2
S1
G1
S2
G2
D2_1
D2_2
D1_1
D1_2
VCC
GND
R2
C4
R7
R6
C5
C1
R5
LED1
Q1
R9
C9
RSR
C7
C6
R1
C2
D2
C8
C3
LED2
R8
R4
R3
THERMALPAD
BTST
HIDRV
PH
LODRV
VCC
MPPSET
STAT1
TS
REGN
GND
SRP
SRN
STAT2
VREF
TERM_EN
VFB


C2
MAX17263LETD+
TH
L1
L2
L3
L4
BATT
CSN
SCL
SDA
ALRT
REG
CELLX/CSPH
CSPL
GND
EP