Controls:	wr	rd	T*R*	clk*R*	mux				adder	IR	T1	T2	PC	Step
Instr					M1	Addr	Mem	Temp						
0. A	1	0	0	0	0	0	1	1	0	1	0	0	1	1
1. MOV *Rd, Rs*	1	1	T*Rs*	clk*Rd*	0	0	1	1	0	0	0	0	0	0
2. MOV M,*Rs*	0	1	T*Rs*	0	0	1	1	1	0	0	0	0	0	0
3. MOV *Rd,*M	1	0	0	clk*Rd*	0	1	1	1	0	0	0	0	0	0
4. HLT	1	1	0	0	0	0	1	1	0	0	0	0	0	1
5. ADD *Rs*	1	1	T*Rs*	clk*Ra*	1	0	1	1	0	0	0	0	0	0
6. ADD M	1	0	0	clk*Ra*	1	1	1	1	0	0	0	0	0	0
7. SUB *Rs*	1	1	T*Rs*	clk*Ra*	1	0	1	1	1	0	0	0	0	0
8. SUB M	1	0	0	clk*Ra*	1	1	1	1	1	0	0	0	0	0
9. JMP d16 Read	1	0	0	0	0	0	1	1	0	0	1	0	1	2
10. JMP d16 Read	1	0	0	0	0	0	1	1	0	0	0	1	1	3
11. PC -> Mem	1	1	0	0	0	0	1	0	0	0	0	0	1	0
12. JNZ d16 Read	1	0	0	0	0	0	1	1	0	0	1	0	1	2
13. JNZ d16 Read	1	0	0	0	0	0	1	1	0	0	0	1	1	3
14. PC -> Mem	1	1	0	0	0	0	1	0	0	0	0	0	1	0
15. JZ d16 Read	1	0	0	0	0	0	1	1	0	0	1	0	1	2
16. JZ d16 Read	1	0	0	0	0	0	1	1	0	0	0	1	1	3
17. PC -> Mem	1	1	0	0	0	0	1	0	0	0	0	0	1	0
18. STA d16 Read	1	0	0	0	0	0	1	1	0	0	1	0	1	2
19. STA d16 Read	1	0	0	0	0	0	1	1	0	0	0	1	1	3
20. *Ra* -> Mem	0	1	T*Ra*	0	0	0	0	0	0	0	0	0	0	0
21. LDA d16 Read	1	0	0	0	0	0	1	1	0	0	1	0	1	2
22. LDA d16 Read	1	0	0	0	0	0	1	1	0	0	0	1	1	3
23. Mem -> *Ra*	1	0	0	clk*Ra*	0	0	0	0	0	0	0	0	0	0
24. LXI rr, Mem->R1	1	0	0	0	0	0	1	1	0	0	1	0	1	2
25. LXI rr, Mem->R2	1	0	0	0	0	0	1	1	0	0	0	1	1	3
26. MVI *Rd*, d8 Read	1	0	0	clk*Rd*	0	0	1	1	0	0	0	0	1	1
27. NOP	1	1	0	0	0	0	1	1	0	0	0	0	0	0