ECE 319 : Digital System Design : Fall 2016

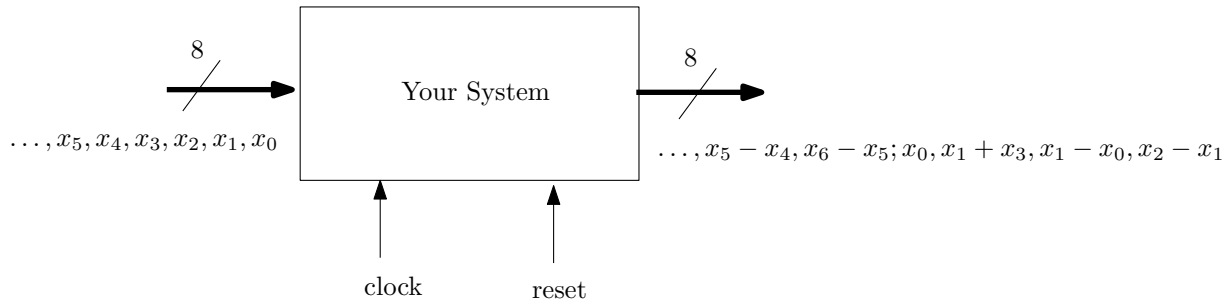
Project I : Due: Oct 10, 2016.

Design a system that accepts an input data stream x_0, x_1, x_2, ... at Port1 and produces a stream of output data points at Port2. Four output points are computed for each set of four input points. The output stream should look like:

$$x_2 - x_1,\ x_1 - x_0,\ x_1 + x_3,\ x_0;\ x_6 - x_5,\ x_5 - x_4,\ x_5 + x_7,\ x_4;\ \ \ldots$$

Note that each set of 4 outputs are computed in exactly the same manner from a corresponding set of 4 inputs.

All data is 8 bit wide and uses 8-bit 2's complement arithmetic. On every clock, one 8-bit data sample enters and one 8-bit data sample leaves the system.



Your system should have a high throughput and should consume a small amount of power.

Submit a report on your design that includes at the minimum:

- Problem statement
- Design approach
- The complete design including datapath sketch and control description.
- Verilog code for the system (including good comments) and the test-bench.
- Simulation waveforms of your system.
- Estimate of system speed.

Name the source file containing modules for your system and the test bench "proj1.v". This file should have two modules, proj1 and proj1_tb (the testbench). Name the input data file used in the simulation "proj1.dat". Identify yourself clearly in the program header. Upload only your proj1.v file to the coursesite by 11:59, October 10th. Late penalty will apply to submissions after the due date. (For this purpose, the date stamp on the web submissions is considered as the submission date). Submit your report in class on Oct 12th.