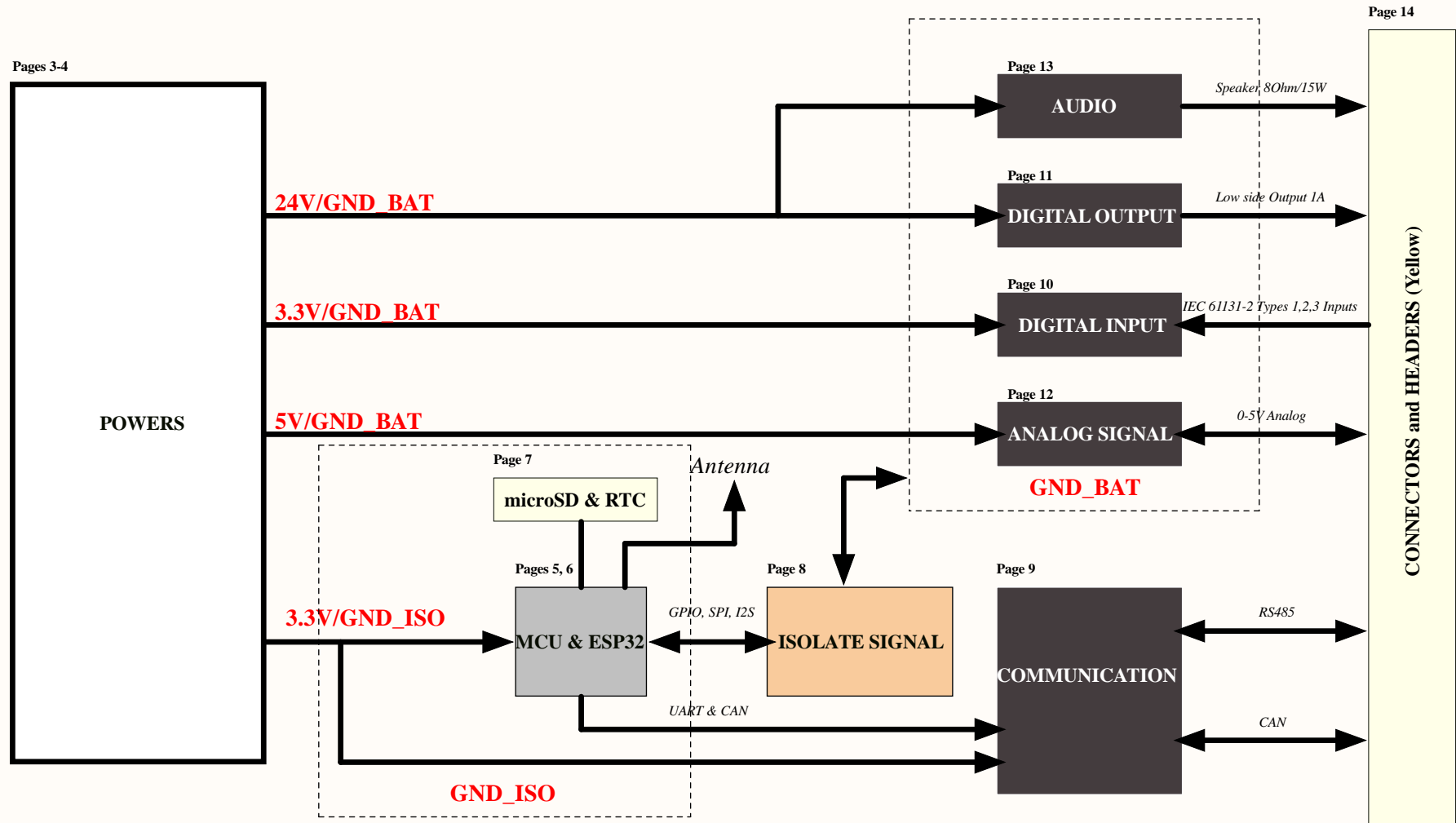


# Main

## (Block Diagram)



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Title:	Main	Variant:	[No Variations]
Page Contents:	[02] - BLOCK DIAGRAM.SchDoc		Checked by
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Main

Variant: [No Variations]

1/17/2022  
V1I1

CHECKED

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2	BLOCK DIAGRAM	12	ANALOG SIGNAL	22	.....	32	.....
3	POWER HIGH STAGE	13	AUDIO	23	.....	33	.....
4	POWER LOW STAGE	14	CONNECTOR	24	.....	34	.....
5	MCU	15	DOC REVISTION HISTORY	25	.....	35	.....
6	WIRELESS	16	.....	26	.....	36	.....
7	LOG	17	.....	27	.....	37	.....
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9	COMMUNICATION	19	.....	29	.....	39	.....
10	DIGITAL INPUT	20	.....	30	.....	40	.....

DESIGN CONSIDERATIONS

DESIGN NOTE:  
Example text for informational  
design notes .

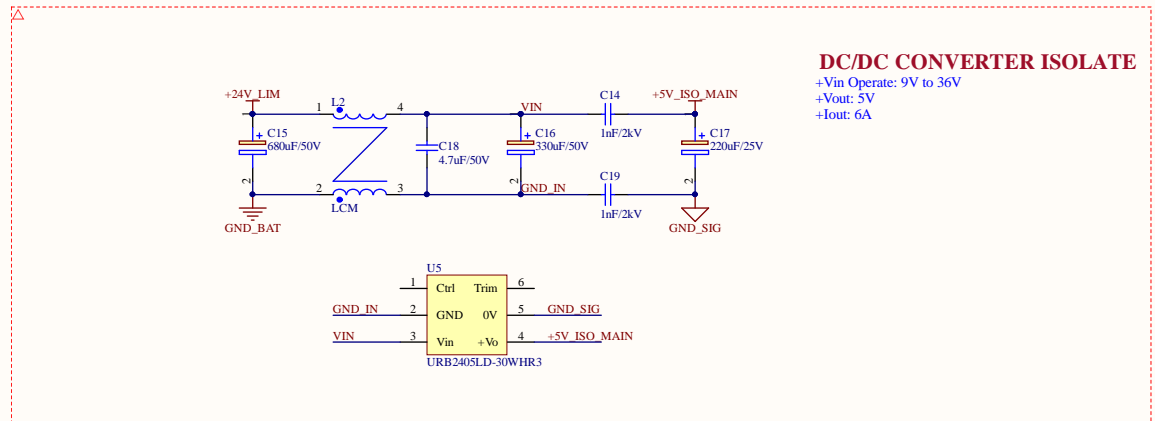
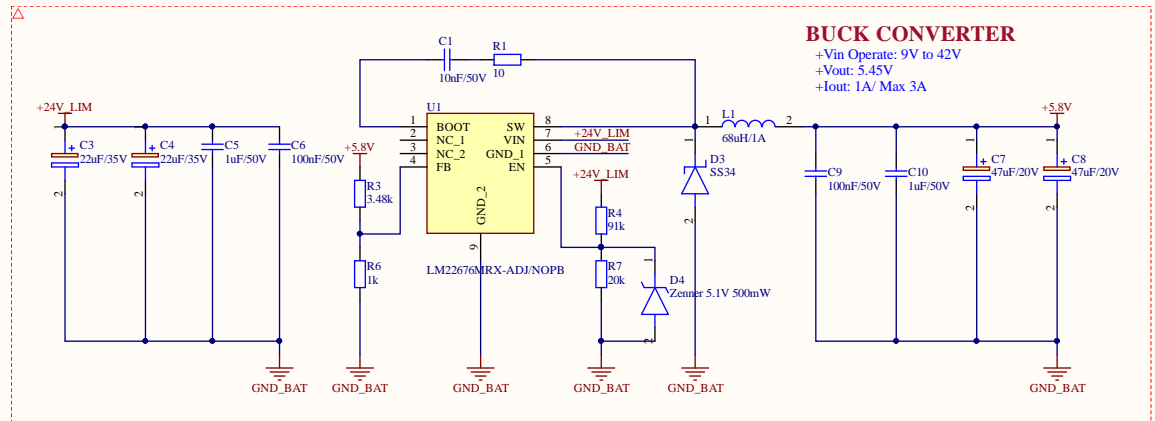
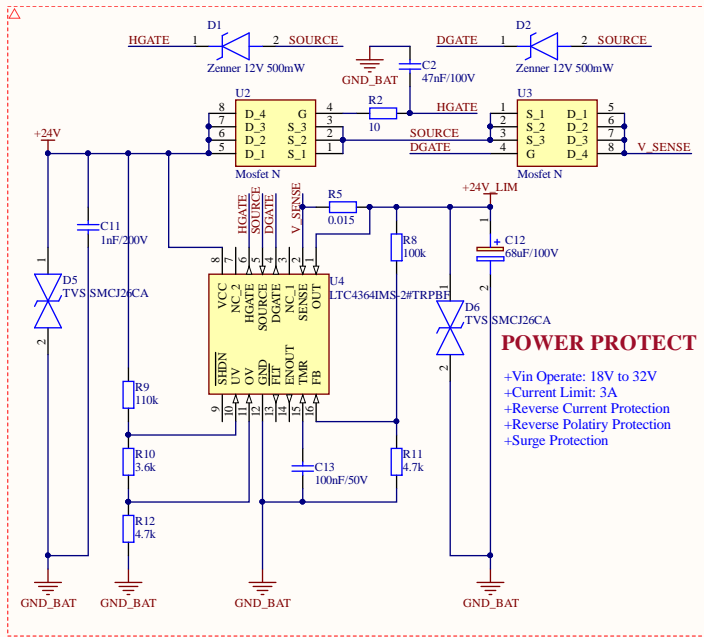
DESIGN NOTE:  
Example text for critical  
design notes.

DESIGN NOTE:  
Example text for cautionary  
design notes.

LAYOUT NOTE:  
Example text for critical  
layout guidelines.

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Title:	Main	Variant:	[No Variations]
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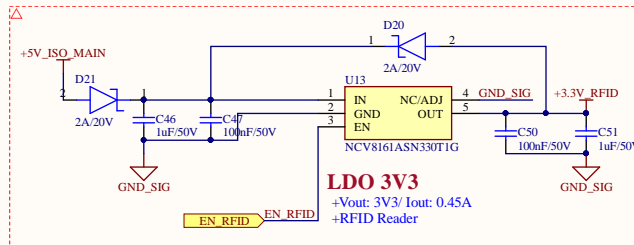
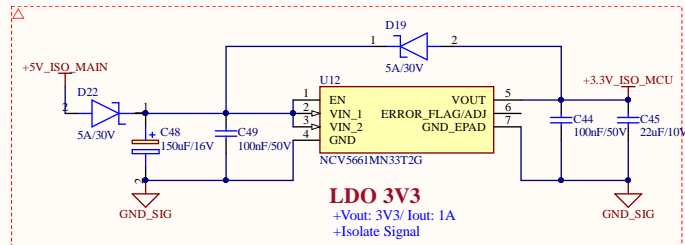
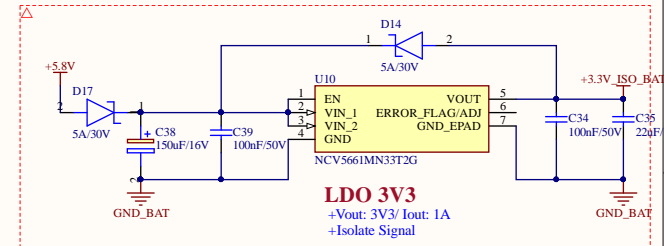
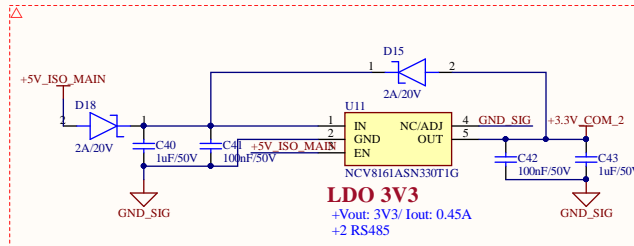
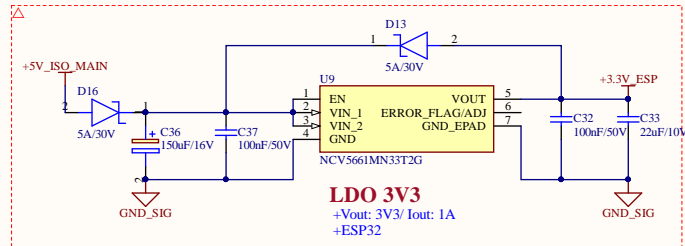
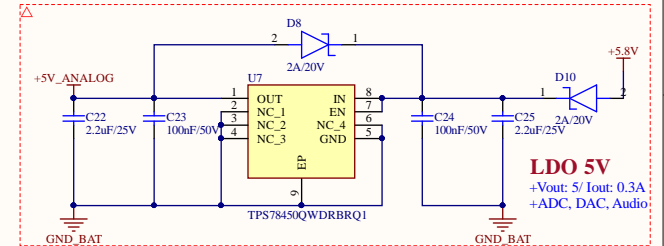
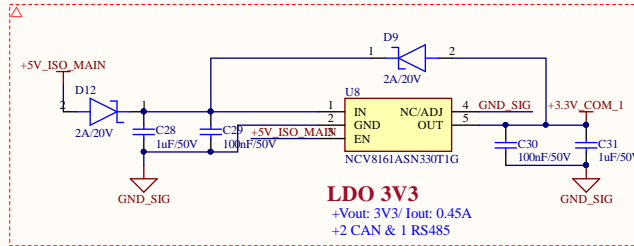
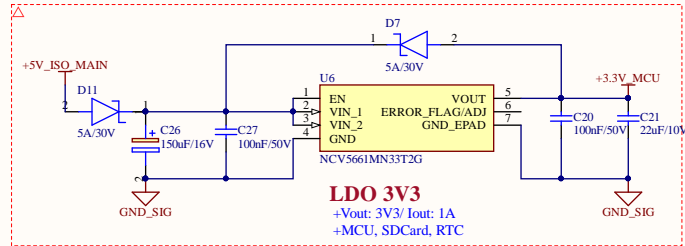
## POWER HIGH STAGE



DESIGN NOTE:  
+Power protect OV, UL, OC, reverse, surge.  
+DC/DC Converter Buck 5.6V/2A.  
+DC/DC Converter Isolate 5V/6A.

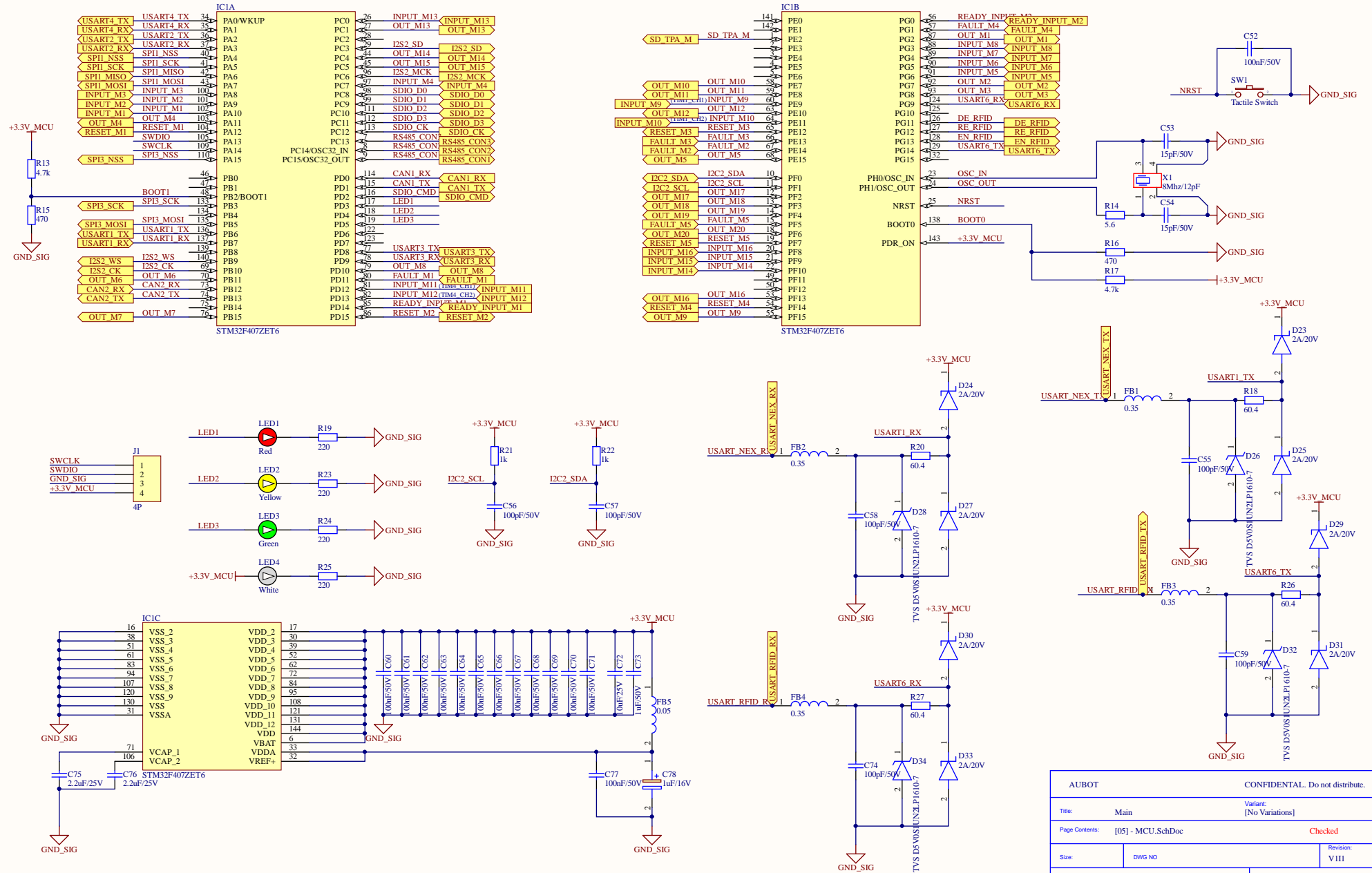
AUBOT		CONFIDENTIAL. Do not distribute.	
Title: Main		Variant: [No Variations]	
Page Contents: [03] - POWER HIGH STAGE.SchDoc		Checked	
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# POWER LOW STAGE

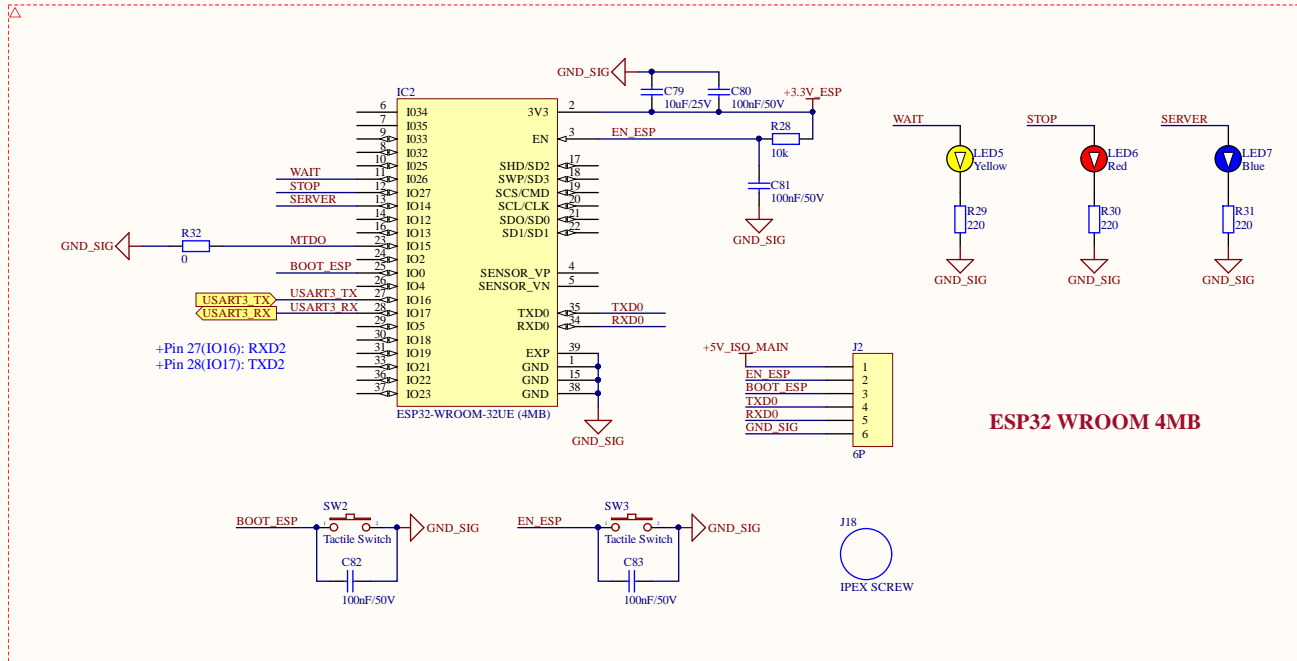


AUBOT		CONFIDENTIAL. Do not distribute.	
Title:	Main	Variant:	[No Variations]
Page Contents:	[04] - POWER LOW STAGE.SchDoc		Checked
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# MCU



# WIRELESS

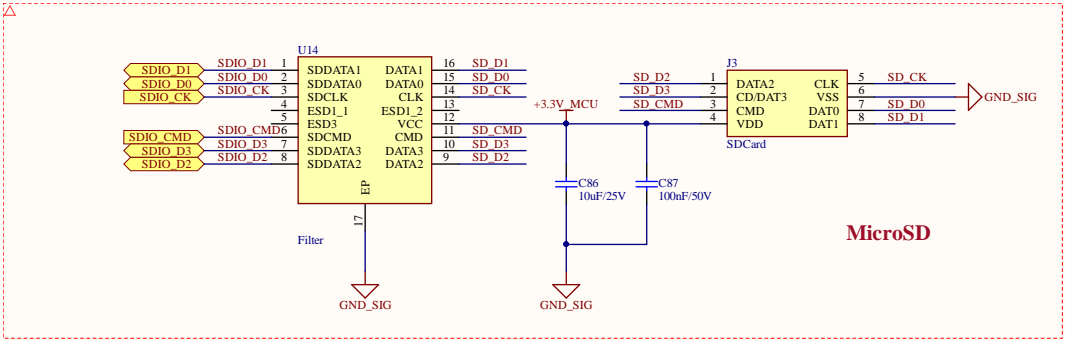
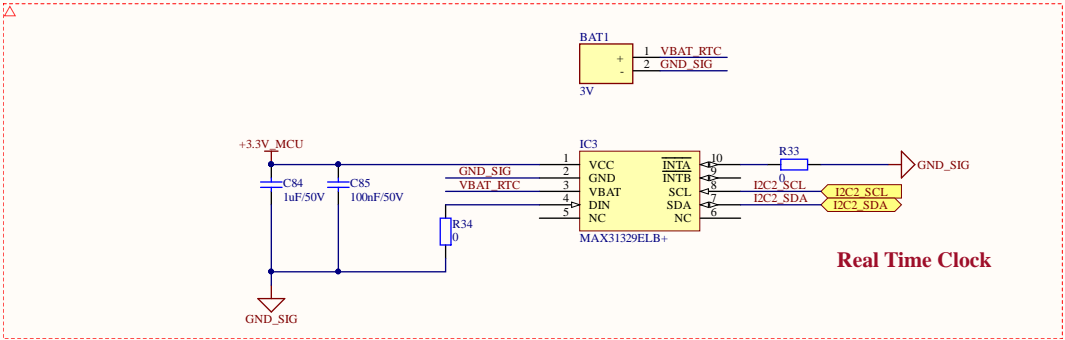


ESP32 WROOM 4MB

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Title: Main			Variant: [No Variations]		
Page Contents: [06] - WIRELESS.SchDoc			Checked		
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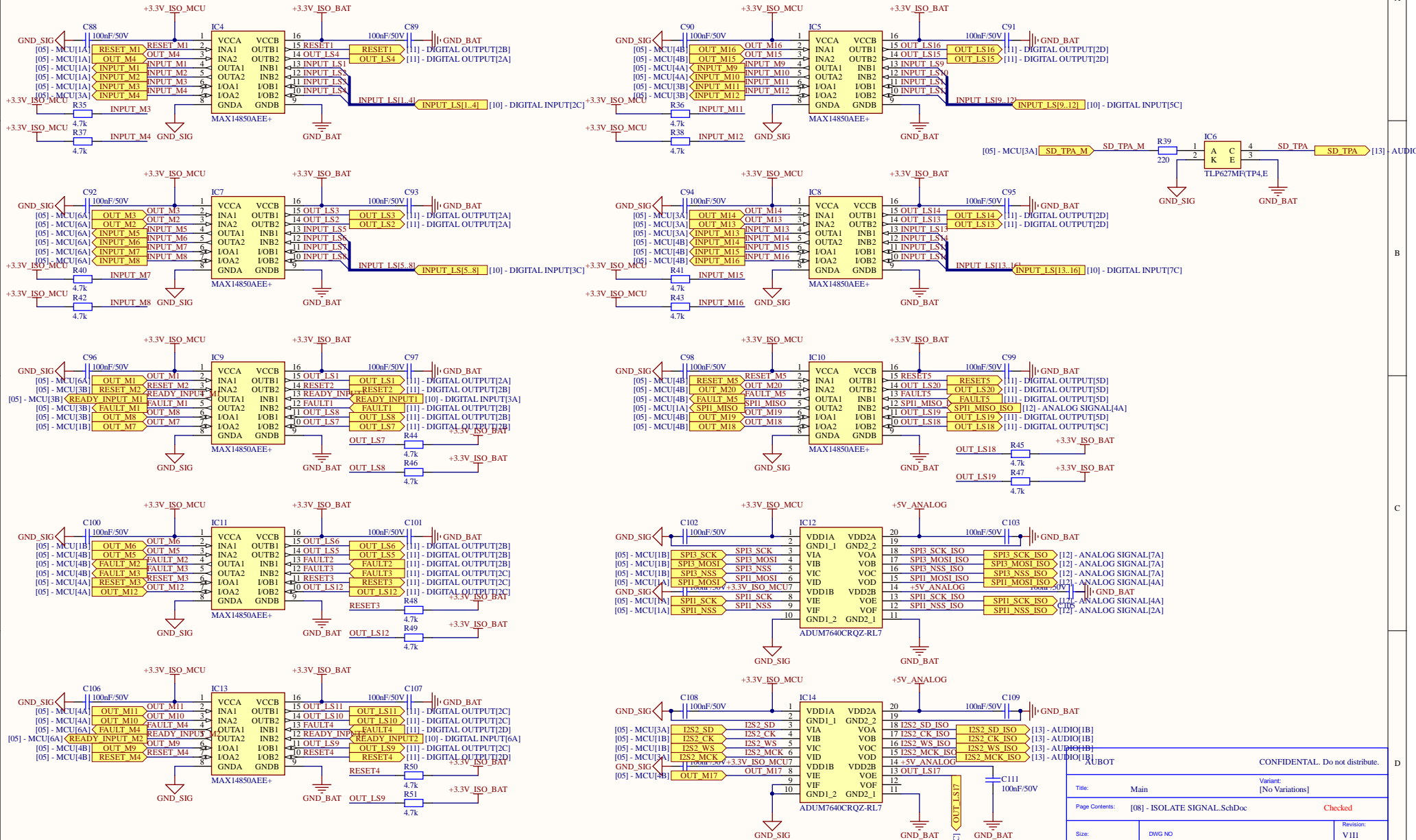
LOG



CONFIDENTIAL & SECRET

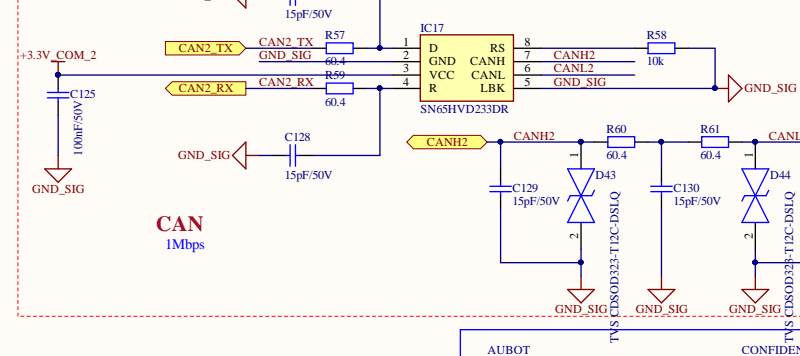
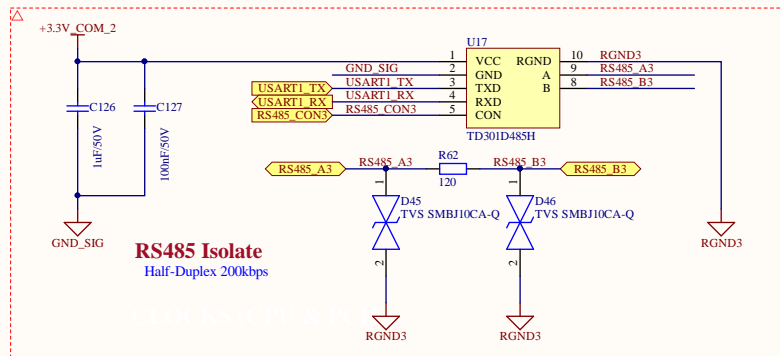
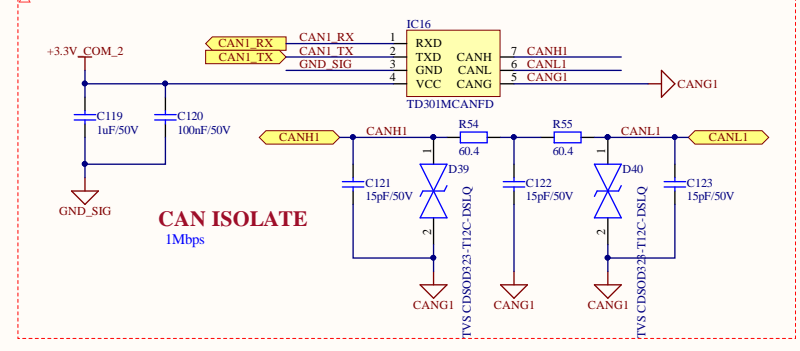
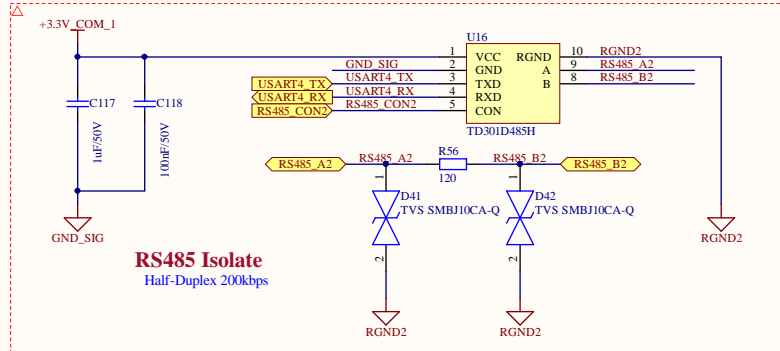
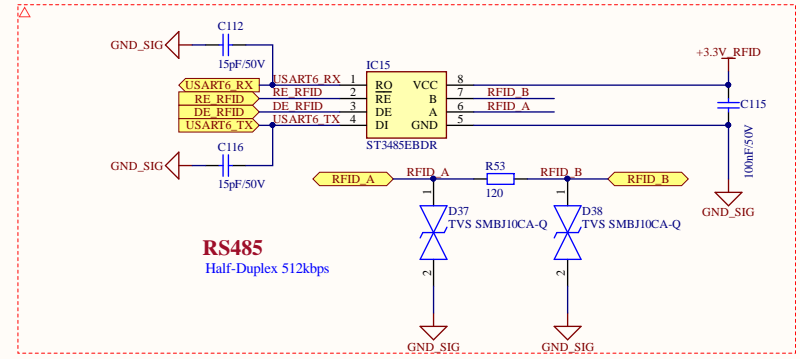
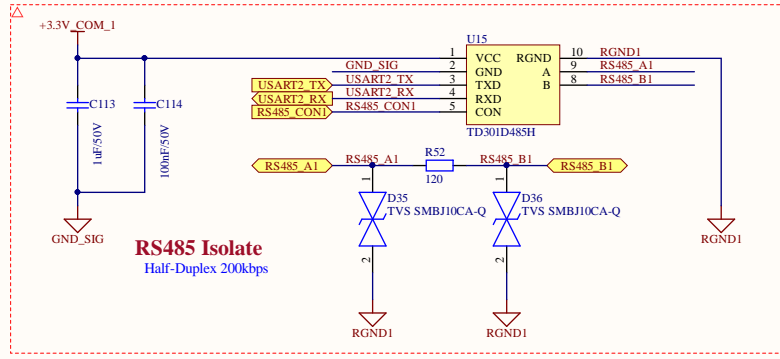
AUBOT			CONFIDENTIAL. Do not distribute.		
Title: Main			Variant: [No Variations]		
Page Contents: [07] - LOG.SchDoc			Checked		
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# ISOLATE SIGNAL





# COMMUNICATION



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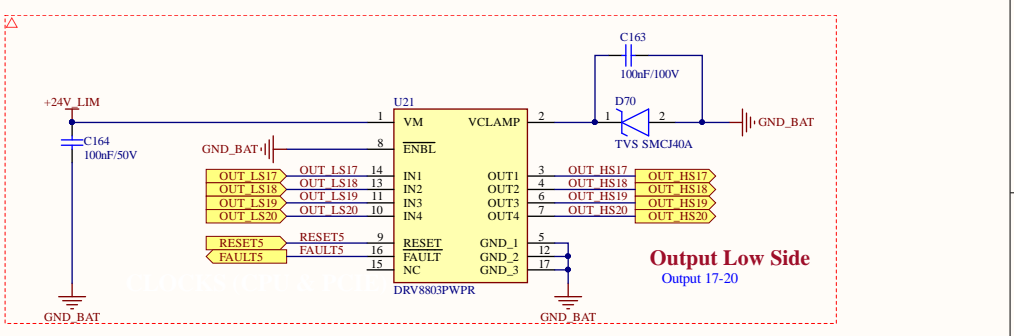
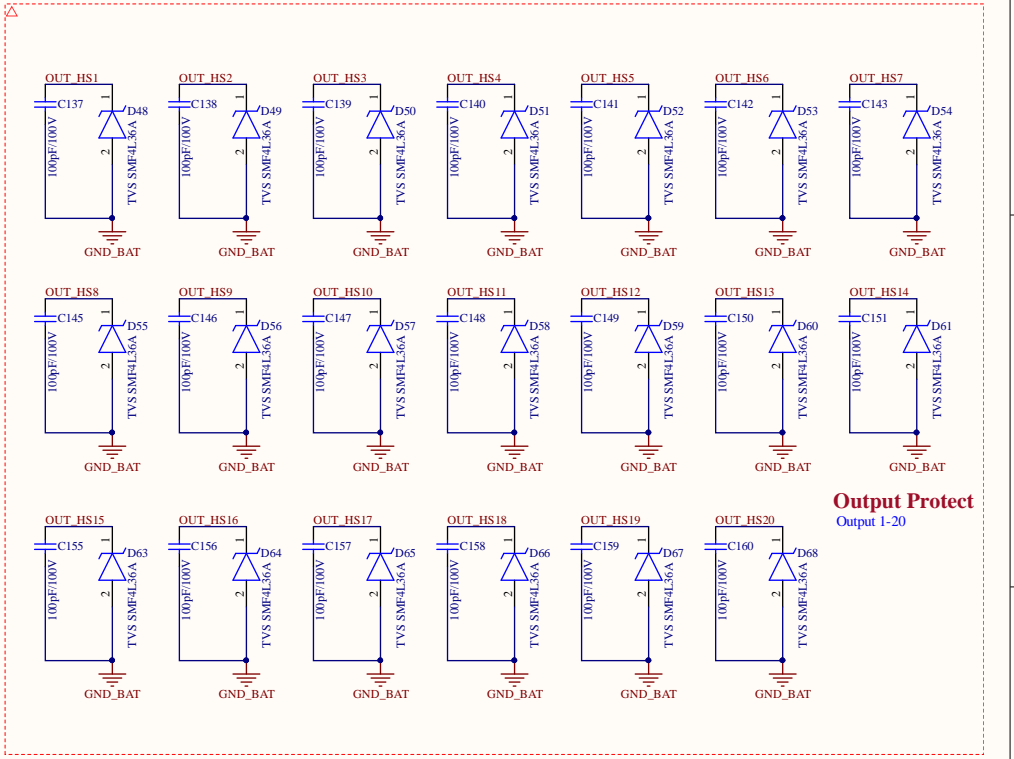
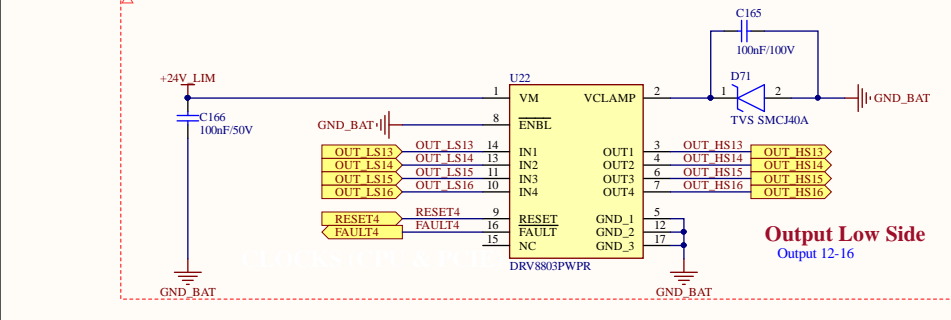
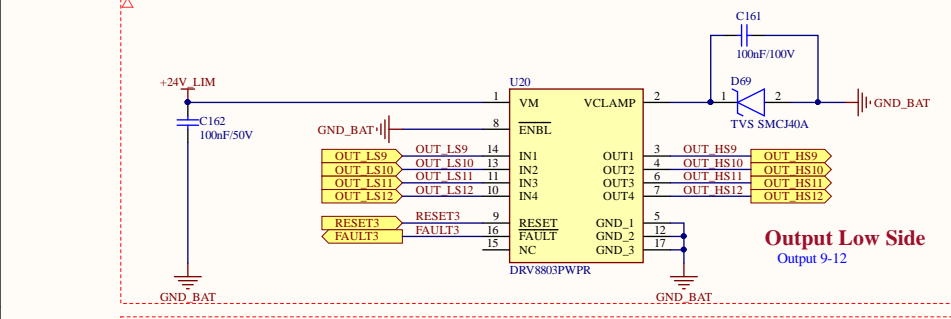
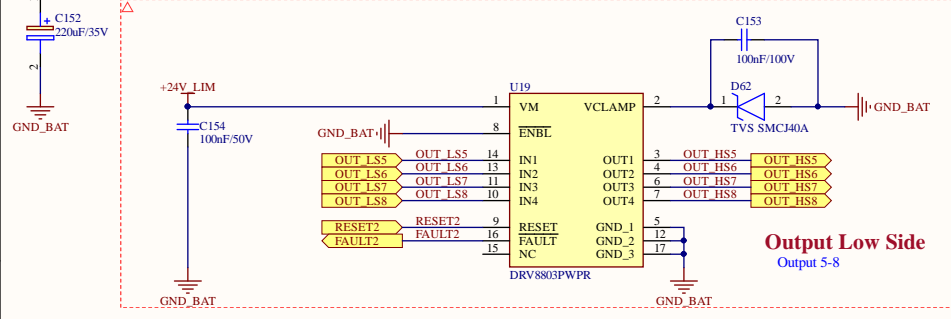
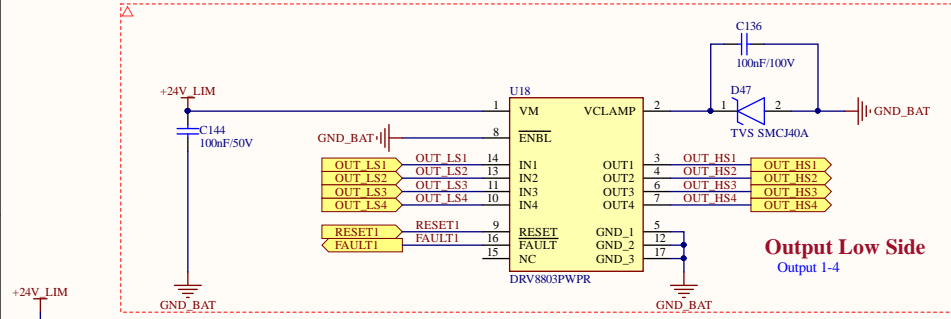
## A



D

D

# DIGITAL OUTPUT

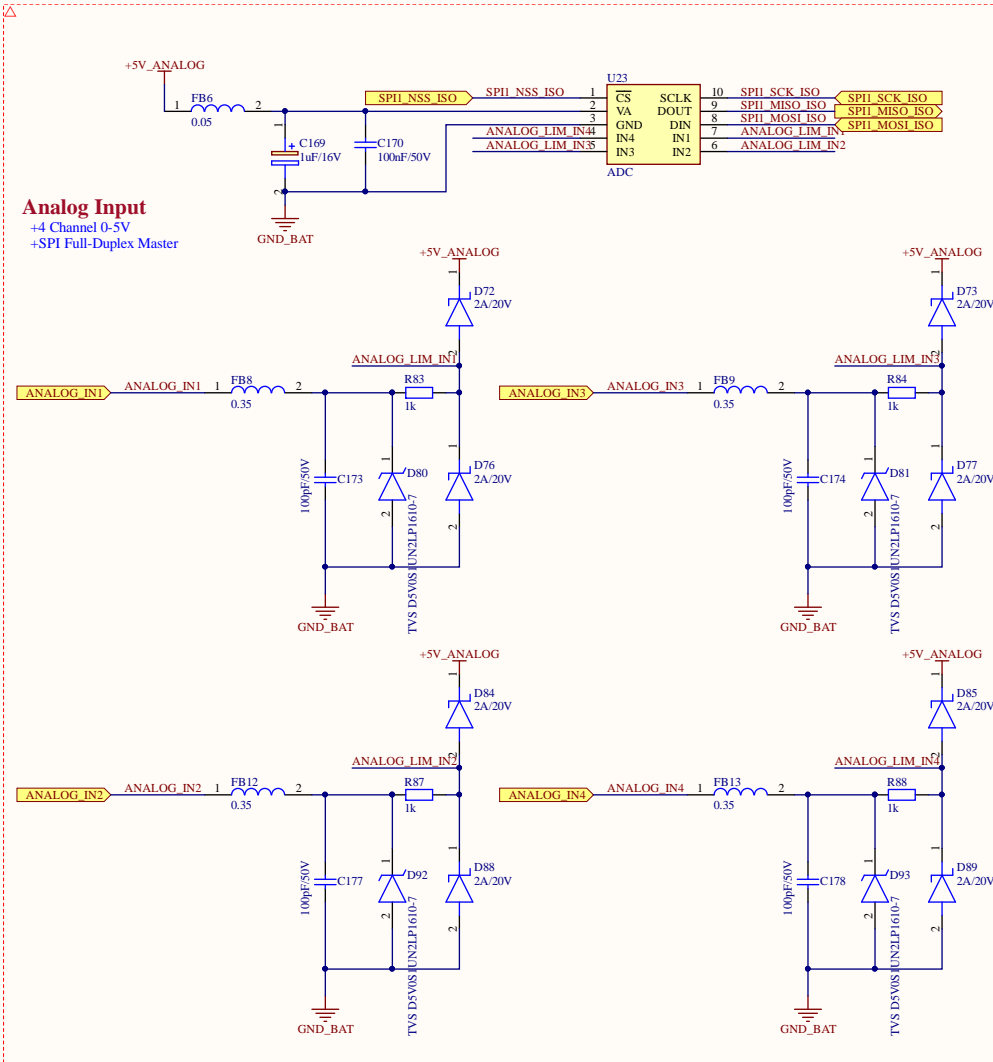


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Title:	Main	Variant:	[No Variations]
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# ANALOG SIGNAL

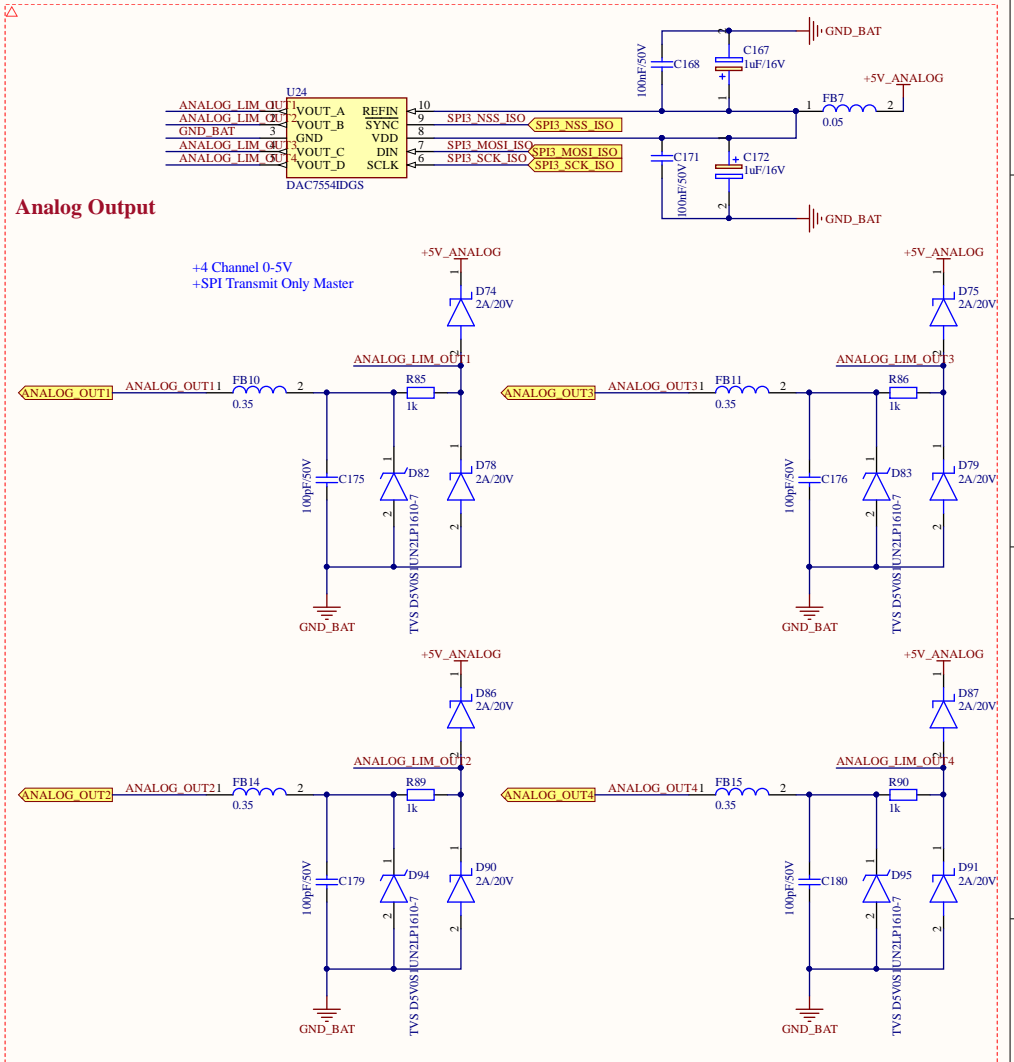
## Analog Input

+4 Channel 0-5V  
+SPI Full-Duplex Master



## Analog Output

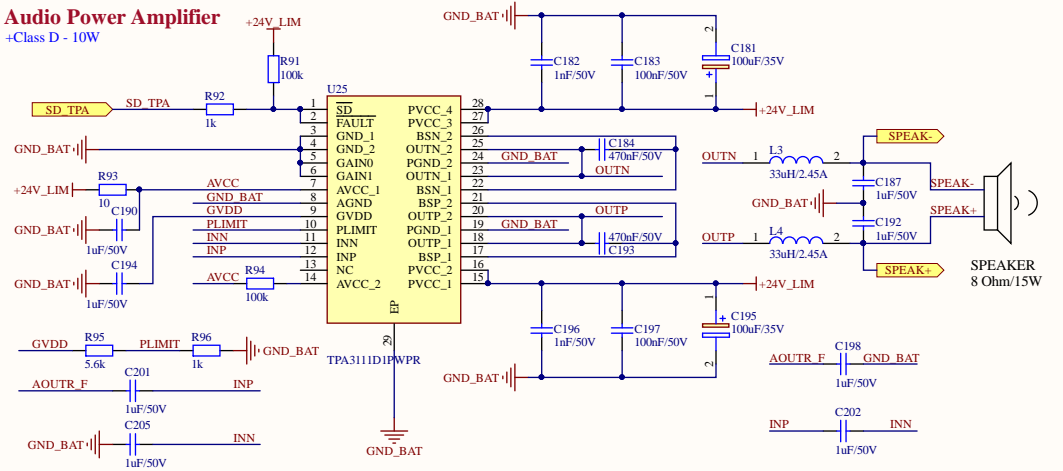
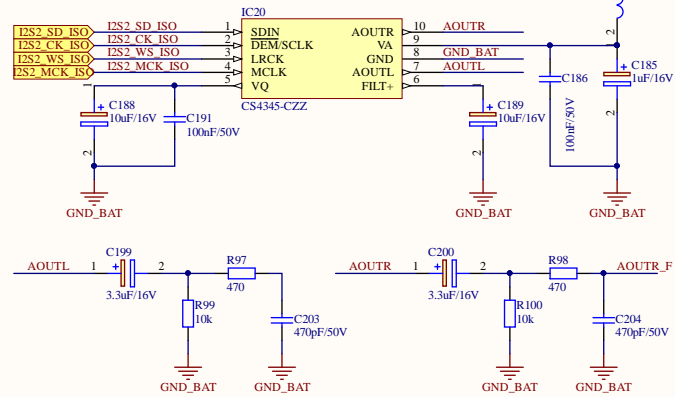
+4 Channel 0-5V  
+SPI Transmit Only Master



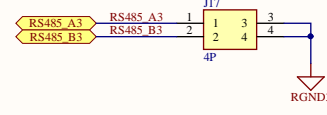
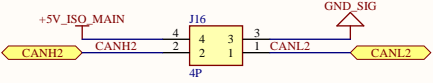
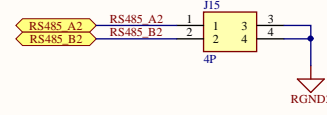
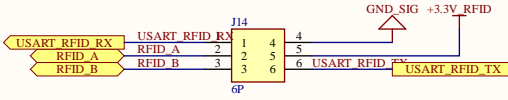
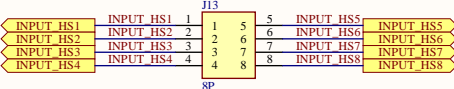
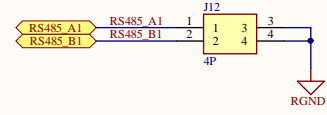
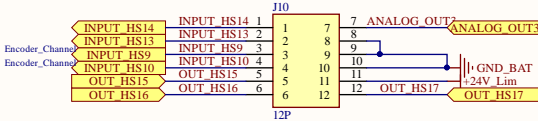
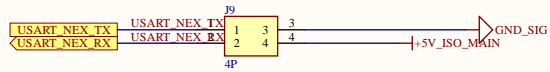
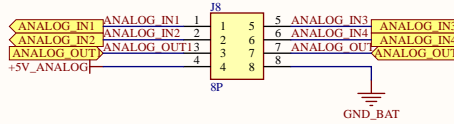
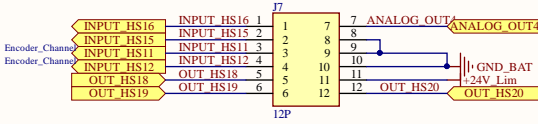
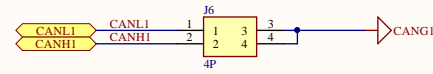
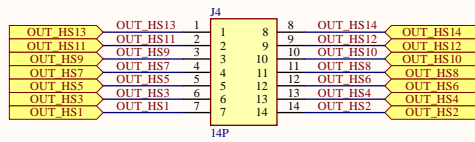
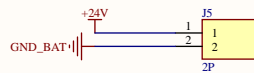
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## Audio Power Amplifier

+Class D - 10W



# CONNECTOR



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# DOC: REVISION HISTORY

CLOCKSPOT & PCH

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Designator  
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Designator  
[02] - BLOCK DIAGRAM.SchDoc

Designator  
[03] - POWER HIGH STAGE.SchDoc

Designator  
[04] - POWER LOW STAGE.SchDoc

Designator  
[05] - MCU.SchDoc

Designator  
[06] - WIRELESS.SchDoc

Designator  
[07] - LOG.SchDoc

Designator  
[08] - ISOLATE SIGNAL.SchDoc

Designator  
[09] - COMMUNICATION.SchDoc

Designator  
[10] - DIGITAL INPUT.SchDoc

Designator  
[11] - DIGITAL OUTPUT.SchDoc

Designator  
[12] - ANALOG SIGNAL.SchDoc

Designator  
[13] - AUDIO.SchDoc

Designator  
[14] - CONNECTOR.SchDoc

Designator  
[15] - DOC REVISION HISTORY.SchDoc

MAIN NOTES

Set Project Parameters

1) Go to Project -> Project Options -> Parameters

2) Set Company, Project and VersionRevision

Mark Not Fitted Components as  
NF

Net Class Example

① Net Class

ClassName: PCIE

Differential signal example

DIFF100

TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Title

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

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