Schematic

V_{dd}

100nF   10k Ohm

470 Ohm

PIC

MCLR/Vpp/RE3	1	28	RB7/ICSPDAT
RA0	2	27	RB6/ICSPCLK
RA1	3	26	RB5
RA2	4	25	RB4
RA3	5	24	RB3
RA4	6	23	RB2
RA5	7	22	RB1
Vss	8	21	RB0
RA7	9	20	VDD
RA6	10	19	Vss
RC0	11	18	RC7
RC1	12	17	RC6
RC2	13	16	RC5
RC3	14	15	RC4

470 ohms
470 ohms
470 ohms
470 ohms
470 ohms
470 ohms
470 ohms

PIC
PIC

100Kohms
100Kohms

100nF

V_{in}
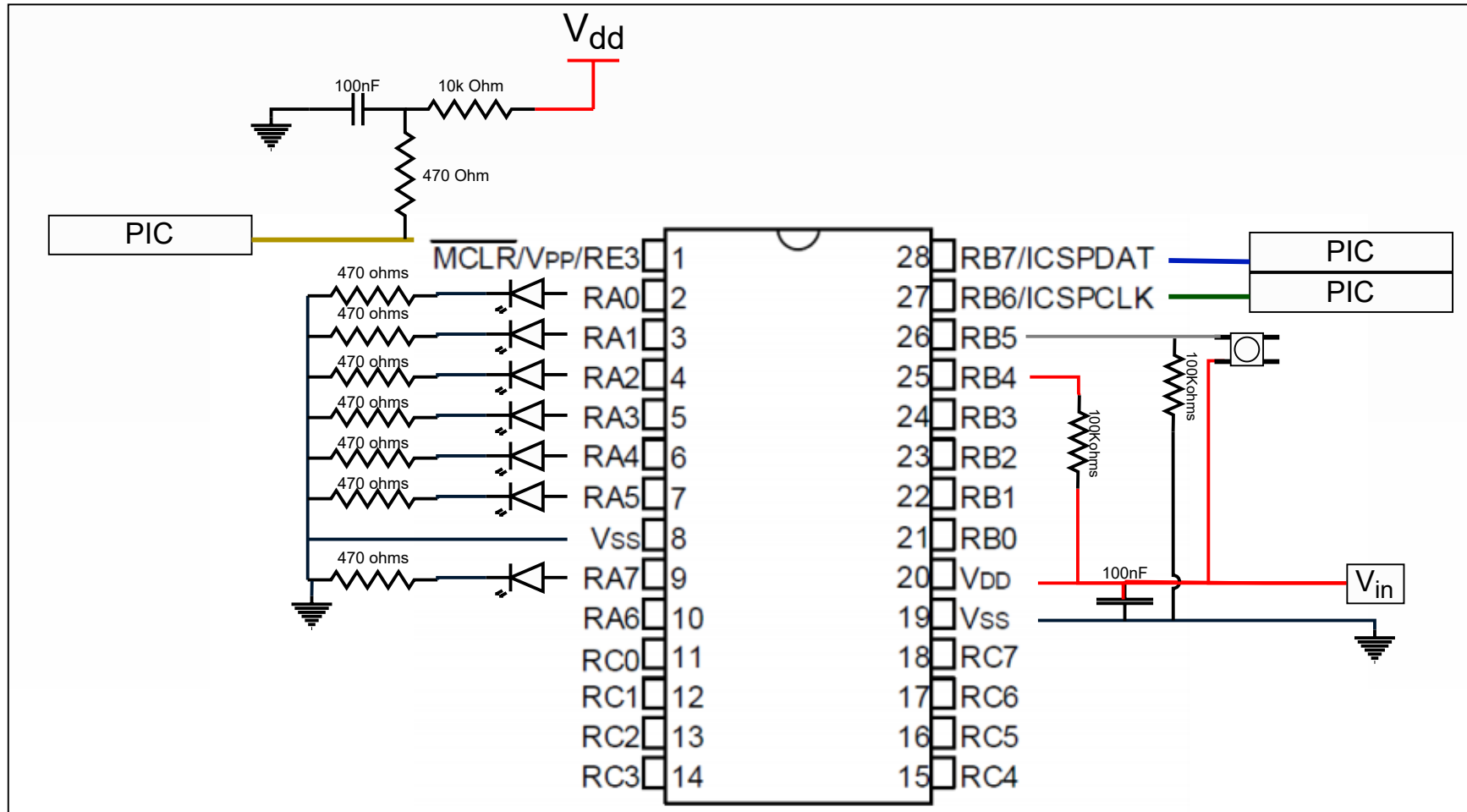
Mock code flow

```
//** Part 1 **//
GPIOsetup
{
  -set LATA 0:7 to outputs
  -set RB5 AND RB4 to inputs
  -clear LATA and PORTB
}

userapprun
{
  if(LATA == Max number)
  {
   LATA = lowest number
  }

  if(RB5 == 1)
  {
   LATA++
  }

}

//////////////////////////////////////////////////////////////
//////////////////////////////////////////////////////////////
** Part 2 **//
GPIOsetup
{
   -set LATA 0:7 to outputs
   -set RB5 AND RB4 to inputs
   -clear LATA and PORTB
}

userapprun
{
  if(RB5 == 1 and the previous state was 0)
  {
   LATA++
   set previous state to 1 (add a delay if theres too much bounce as a temporary solution)
  }

  if(RB5 is 0)
  {
  previous state = 0
  }
}
```

Circuit