Summary: Design-oriented estimation of thermal noise in switched-capacitor circuits (TCAS-1 2005)

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1. Introduction

Noise is a major limitation of the performance of switched- capacitor (SC) circuits. This noise is categorized as intrinsic noise and extrinsic noise. In this paper, we focus on intrinsic noise that occurs in MOS transistors. Intrinsic noise consists of thermal noise and flicker noise.

Thermal noise is caused by the thermal motion of channel carriers, which leads to irregular fluctuations in the drain current. The representation of thermal noise varies according to the operating point of MOSFET

1) triode region

$$S_{\mathrm{vt}}(f) = 4kTR_{\mathrm{on}}(\mathrm{V}^2/\mathrm{Hz}).$$

2) saturation region

$$S_{\mathrm{it}}(f) = \frac{8}{3}kTg_m(\mathrm{A}^2/\mathrm{Hz})$$

Flicker noise occurs due to trapping and release of charge carriers in the channel. It can be approximated by the following equation.

$$S_{\mathrm{vf}}(f) = \frac{K}{WLf}(\mathrm{V}^2/\mathrm{Hz})$$

2. Thermal noise effects in COMOS OP AMP

2-1. Estimation of input-referred thermal noise in an OP AMP

As an op-amp example, the differential pair is illustrated together with thermal noise current sources.

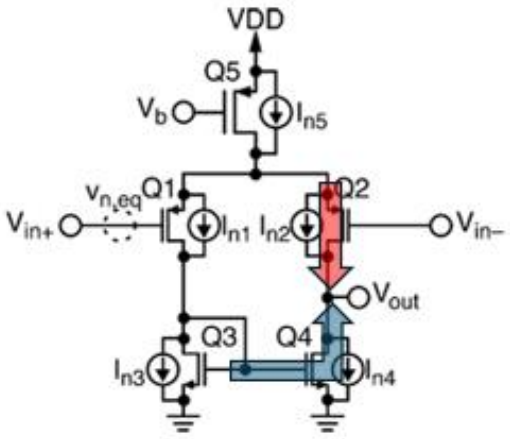


Fig. 1. Noise sources in a simple CMOS op-amp.

Tail current noise is equally divided along two signal paths, resulting in cancellation at the output node. Therefore, the tail current noise source does not contribute to the output. On the other side, total input-referred thermal noise voltage PSD is represented by the following equation, which considers the noise sources of the input devices (Q1, Q2) and the load devices (Q3, Q4). This equation is derived using the superposition principle.

$$S_{vt}(f) = \frac{16KT}{3g_{m1}}\left(1 + \frac{g_{m3}}{g_{m1}}\right) \cong \frac{16KT}{3g_{m1}}\ [V^2/Hz]$$

From this equation, it can be concluded that transconductance of the input device (gm1) must be greater than gm3 to minimize input-referred thermal noise voltage.

2-2. Output thermal noise in negative feedback circuit

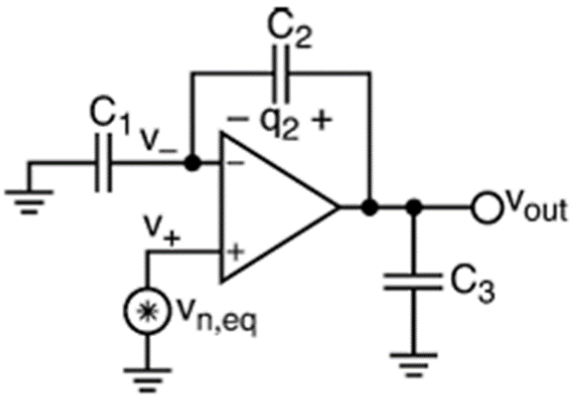


Fig. 2. Op-amp with capacitive feedback and capacitive loading.

The closed-loop transfer function of this circuit is derived as follows.

$$H(s) = \frac{V_{\text{out}}(s)}{V_{+}(s)} = \frac{G_0}{1 + s\tau}.$$ $\tau = \frac{C_0}{\beta g_{m1}}$[s] : settling time

The input-referred thermal voltage noise passes through a first order low-pass filter, resulting in filtered noise at the output node. the key conclusion is that the **settling time can be controlled by the capacitance of SC circuit.**

The total output thermal noise is represented as the following equation.

$$\overline{v_{\text{out}}^2} = \int_0^\infty S_{\text{vt}}(f)|H(j2\pi f)|^2 df = \left(\frac{16kT}{3g_{m1}}\right)\left(\frac{G_0^2}{4\tau}\right)$$

Substituting the values derived above for G_0 and tau gives

$$\overline{v_{\text{out}}^2} = \left(\frac{4kT}{3}\right)\left(\frac{1 + C_1/C_2}{C_0}\right) = \frac{4}{3}\frac{kT}{\beta C_0}$$

Total output PSD is independent of gm1 in contrast to input PSD, because the transfer function cancels out gm1.

If capacitance is chosen such that C2=0 and B=1 to minimize the total output PSD, then it follows that.

$$\overline{v_{\text{out}}^2} = \frac{4kT}{3C_0}.$$

In this case, **where C2>>C1(say B=1),** and the **capacitance C3 should be maximized to minimize the total output PSD.**

3. Sampled thermal noise

In Fig2, v_n is processed by a first-order filter with transfer function of SC circuit.

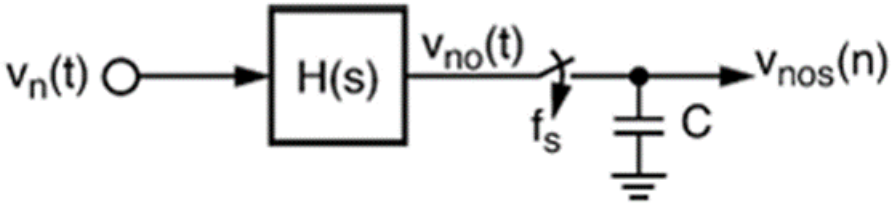


Fig. 3. Noise signals in a sampled system.

Consequently, the output PSD Vno has a 3-dB frequency at 2pi(Bgm1)/C0, and the noise power follows that

$$\overline{v_{\mathrm{no}}^2} = \frac{G_0^2 S_v}{4\tau}.$$

The vnos is sampled as Vno at the clock rate fs, and exhibits a transient response characterized by e^(-t/tau).

Sampling clock rate fs must satisfy the following equation to prevent any change in the bit assigned by the ADC.

$$\frac{f_{3\ \mathrm{dB}}}{f_s} > \frac{(N+1)\ln 2}{\pi}$$

The bandwidth of SC circuit is determined by the SNR condition. Therefore, fs should be reduced to satisfy settling error requirement. However, decreasing fs raises noise floor, which in turn increases Snos. **There is a trade off between Snos and the settling error requirement**.

$$S_{\mathrm{nos}}(f) = \frac{\overline{v_{\mathrm{no}}^2}}{f_s/2} = \frac{G_0^2 S_v}{2\tau f_s}.$$

4. Noise effects in an SC integrator

In this chapter, the thermal noise of switch is considered.

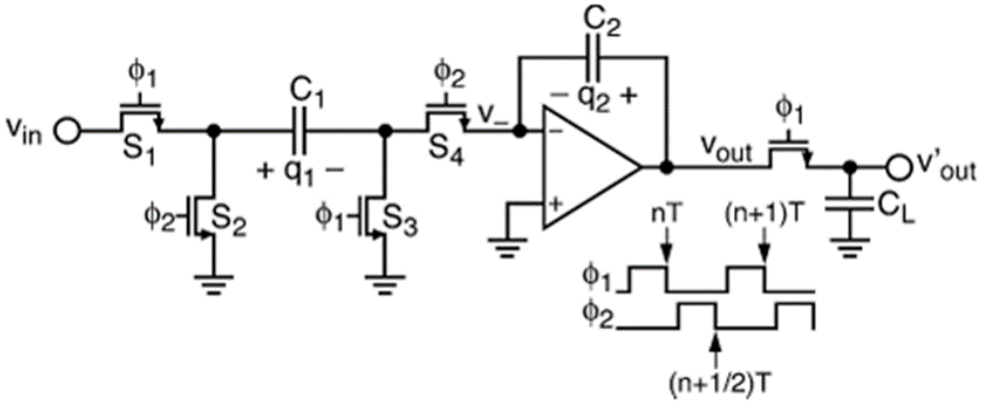
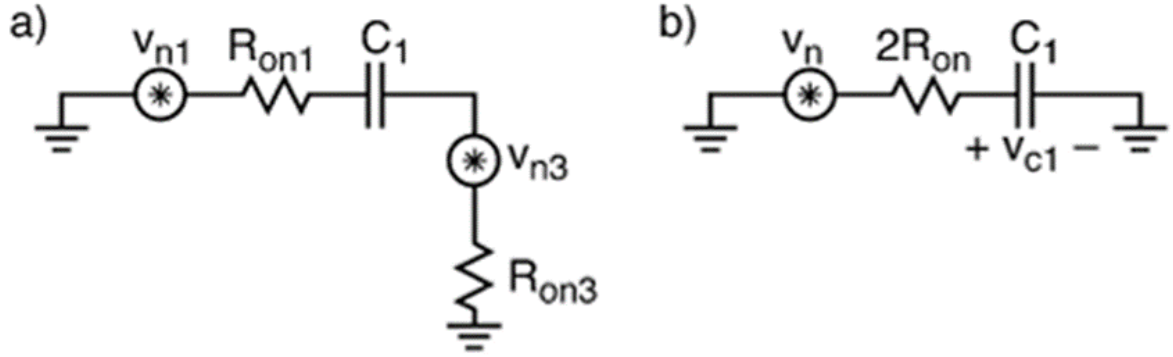


Fig. 4. A stray-insensitive SC integrator.

4-1) φ_1 is High

The equivalent circuit of Fig. 4 is illustrated, where a) is simplified to b).



The PSD assigned to C1 by vn is given as follows.

$$S_{c1}(f) = \frac{8KTR_{on}}{1+(2\pi f\tau_0)^2}\ [V^2/\text{Hz}] \qquad \text{Let } \tau_0 = 2R_{on}C_1$$

Let us consider only the amplitude aspect. The total noise power assigned to C1 is shown below.

$$\overline{v_{c1}^2} = \frac{8kTR_{\text{on}}}{4\tau_0} = \frac{kT}{C_1}$$

Consequently, C1 should be maximized to reduce the noise effect of the switch at C1.

4-2) φ_2 is High

The equivalent circuit of Fig. 4 is illustrated.

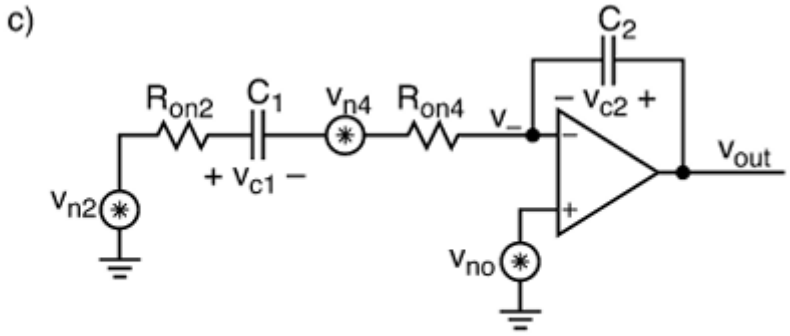


Fig. 5. Noise analysis for the integrator in Fig. 4.

It can be transformed to (b) by a small signal model(a)

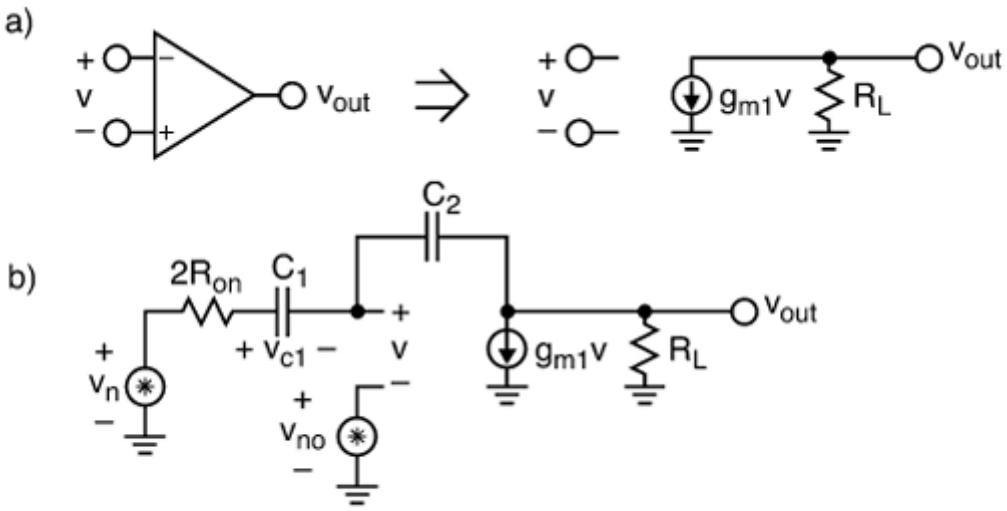


Fig. 6. Noise analysis for a single-stage amplifier.

Let's assume R_L is infinite. The noise voltage across C1 is determined as shown below

$$V_{c1}(s) = \frac{V_n(s) - V_{\text{no}}(s)}{1 + s\tau}$$

$$\tau = (2R_{\text{on}} + 1/g_{m1})C_1.$$

Applying the superposition principle, the total noise power due to the switch and the op-amp across C1 is shown below, respectively.

$$\overline{v_{c1,\text{sw}}^2} = \frac{S_n(0)}{4\tau} = \frac{8kTR_{\text{on}}}{4(2R_{\text{on}} + 1/g_{m1})C_1} = \frac{kT/C_1}{1 + 1/x}.$$

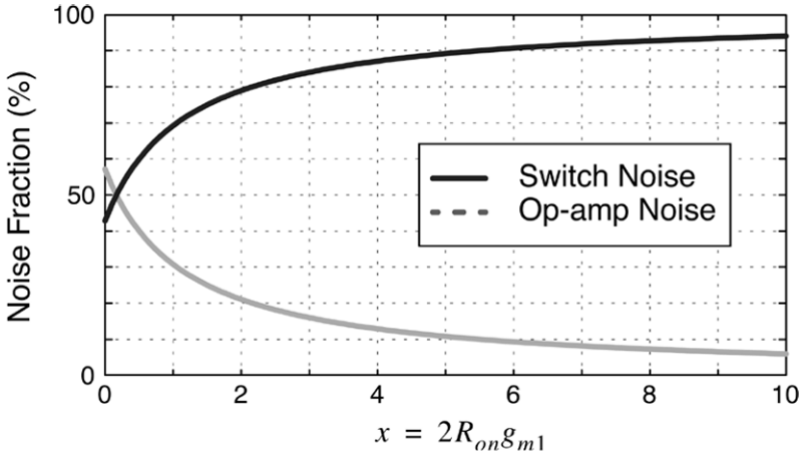
$$\overline{v_{c1,\text{op}}^2} = \frac{S_{\text{no}}}{4\tau} = \frac{(16/3)kT/g_{m1}}{4(2R_{\text{on}} + 1/g_{m1})C_1} = \left(\frac{4}{3}\right)\frac{kT/C_1}{1 + x}.$$

Here, x is 2Ron*gm1. Then, the total noise power is given by

$$\begin{aligned}\overline{v_{c1}^2} &= \frac{kT}{C_1}\left(1 + \frac{x}{1+x} + \frac{4/3}{1+x}\right) \\ &= \frac{kT}{C_1}\left(\frac{7/3 + 2x}{1+x}\right) = \frac{2kT}{C_1}\left(1 + \frac{1/6}{1+x}\right).\end{aligned}$$

By this equation, we can derive the following discussion.

If x is much larger than 1, the switch noise dominates the total noise across C1 when φ_2 is high. On the other hand, if x is much smaller than 1, the op-amp noise dominates. Consequently, x should be set such that x>>1 to minimize total noise across C1 to 2KT/C1.



However, this condition(x>>1) causes significant power consumption by generating large currents in the circuit. Therefore, we can consider an alternative option by maximizing C1. Let's compare the minimum cap design with the minimum power design. The size of C1 in the minimum power design is only about 17% larger than the other case. **This illustrates the trade-off between power consumption and circuit size to minimize the noise across C1**.

We can derive the increased noise charge of C2 by considering the noise charge of C1. Since C1 and C2 are connected in series, C2 acquires the same additional noise charge as C1.

$$\overline{(\Delta v_{c2})^2} = \frac{kTC_1}{C_2^2}\left(\frac{7/3+2x}{1+x}\right)$$

From the above discussion, we can draw the following conclusion: **when x >>1**, the total noise power across C1 is determined by the input capacitance C1. Therefore, **a large input cap generates more noise at the input**

$$\overline{q_{c2}^2} = 2kT(C_{1a} + C_{1b} + \cdots).$$

4-3) When φ_1 is High, the total output thermal noise power caused by input-referred noise of the op-amp

This was already discussed in chapter 3.

4-4) Noise modeling

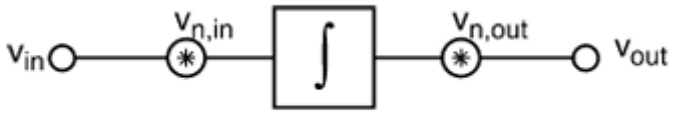


Fig. 8. Equivalent noise sources for the integrator of Fig. 4.

The Vn,in is discussed in 4-1) and 4-2). The Vn,out is discussed in 4-3).

4-5) Determine time constant and C1 to minimize the noise across C1.

The MS value of Vc1 is inversely proportional to tau and gm1.

$$g_{m1} = \frac{kT}{\tau \overline{v_{c1}^2}}(7/3 + 2x)$$

To make Vc1 is small, we should choose x<<1 and make tau as large as allowed, as discussed in chapter 3.

$$\tau = [(2\ln 2)(N+1)f_s]^{-1}.$$

Let's **assume x<<1**. Then, gm1 can be found as following equation.

$$g_{m1} \approx \frac{7}{3}\frac{kT}{\tau \overline{v_{c1}^2}}$$

Where **the permissible MS value of Vc1 is again determined by N and fs**. Finally, in this case, **C1 can be calculated as follows**.

$$C_1 = \frac{g_{m1}\tau}{x+1} \approx \frac{7}{3}\frac{kT}{\overline{v_{c1}^2}}.$$

5. Single-ended versus differential circuits

Let's consider following circuit to compare noise performance between single-ended and fully differential circuit.

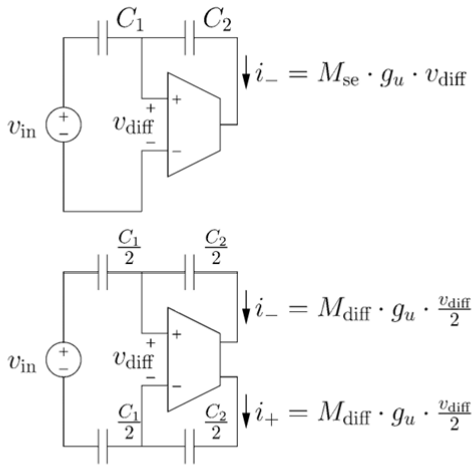


Fig. 9. Topology and main properties of the single-ended and fully-differential circuits.

The time-constants for the two topologies are derived as follows, respectively.

$$\tau_{se} = \frac{C_1}{M_{se} \cdot g_{m1}} \ , \ \tau_{diff} = \frac{C_1/2}{M_{diff} \cdot g_{m1}}$$

Here, M_{se} and M_{diff} are multiplication factors applied to the transconductance of unit-sized transistor, and g_u represents the transconductance of the unit-sized transistor.

To ensure the same time-constant, M_{diff} is set to $M_{se}/2$. We are now ready to compare the noise performance by setting the same total capacitance C1+C2 and time-constant.

The total noise power of the single-ended circuit was already derived in chapter 4. Likewise, in the case of fully differential circuits, the noise power can also be determined using same process. The ratio of the differential circuit's noise level to that of the single-ended circuit is given as follows.

$$\frac{\overline{v_{n,\text{diff}}^2}}{\overline{v_{n,\text{se}}^2}} = 4 \cdot \frac{(1+x) - 1/6}{(1+x) + 1/6} \simeq 2.8 \text{ for } x \ll 1.$$

It can be concluded that the noise floor of differential circuits is approximately 4.5 dB higher than that of single-ended. However, their dynamic range is only about 1.5dB (6-4.5=1.5) higher, since the full-scale swing of the differential circuit is twice that of the single-ended one. Additionally, the dynamic range of the differential circuit will be improved by an extra 3 dB because it drives twice as much capacitance as the single-ended circuit. Consequently, the **total noise power in differential circuits is higher than the single-ended case, while consuming only half the power and improving dynamic range(3+1.5=4.5dB)**.

(It is a good approximation within -3dB frequency.)

Therefore, fully differential circuits are preferred not only because they suppress even-order harmonic distortion and are more robust to extrinsic noise, but also because they allow a longer battery life and smaller chip size.

6. Integrator noise analysis example

The noise Contribution of $v_{n,out}$ is negligible at the output. It can be calculated through various simulation tools.

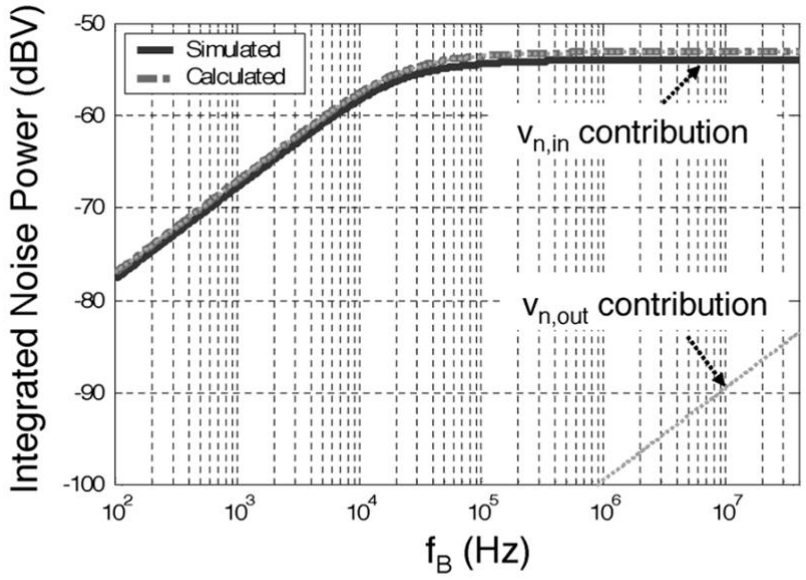


Fig. 10. Calculated and simulated integrated noise powers at the output of an integrator.

(Here, f_B is signal band.)

This conclusion ensures the theory discussed earlier.

7. Thermal noise effects in a delta-sigma loop

The theorems discussed are applied to the design of a second-order low-distortion delta-sigma modulator, as shown in Fig.11. Here, H(z) represents SC integrators.

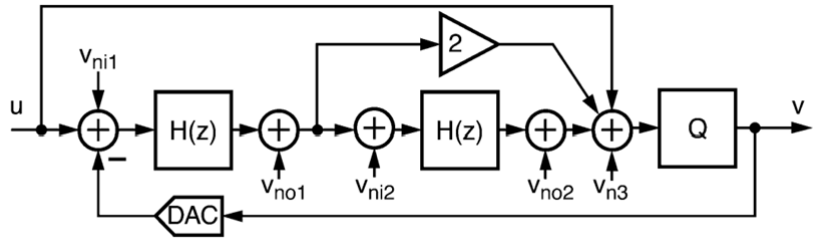


Fig. 11. Noise sources in the feedforward topology.

First, we decide on OSR, the maximum signal power, and the desired bit resolution.

Then, the total permissible noise power can be determined.

Second, we derive the total permissible input-referred thermal noise power by assigning 75%

of noise power to thermal noise.

Third, we determine the desired number of quantizer bits by assigning 10% of the total noise power to the shaped in-band quantization noise.

7-1) Find the minimum acceptable value of C_{s1}, ,C_{s2}, and $C_{f1,2,3}$.

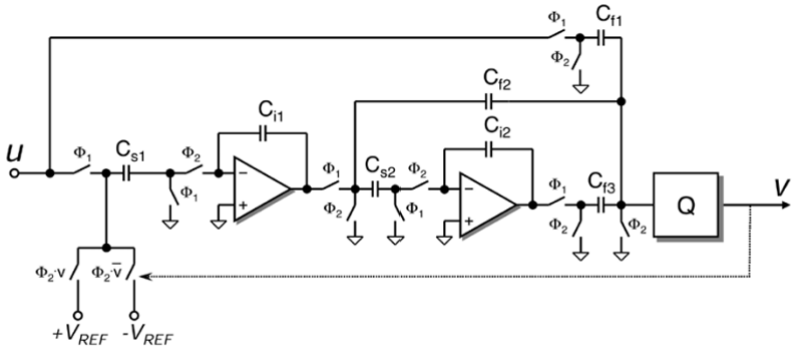


Fig. 12. Schematic of the feedforward topology.

There are five SC branches (C_{s1}, C_{s2}, and $C_{f1,2,3}$).

The ratio of the feedback capacitors is adjusted by arbitrarily selecting only one of them, since the feedback cap determines the signal transfer ratio of each integrator input.

C_{s1} and C_{s2} are then selected to minimize the input referred noise. According to chapter 2, C_{i1} and C_{i2} should be chosen to be larger than C_{s1} and C_{s2} to minimize the total output PSD.

Since all noise sources are sampled with white noise PSDs at the sampling frequency. The PSD of the j-th source can be expressed as follows.

$$S_{vj} = \frac{\overline{v_j^2}}{f_s/2}.$$

According to chapter 4, The MS value of the input-referred noise voltage of the first integrator is given as follows.

$$\overline{v_{\mathrm{ni1}}^2} = \left(\frac{kT}{C_{s1}}\right)\frac{7/3+2x}{1+x}.$$

Let the effective load capacitance as follows, during clock phase $\varphi 1$.

$$C_{01} = \frac{C_{s2} + C_{f2}(C_{f1} + C_{f3})}{C_{f1} + C_{f2} + C_{f3}}$$

And then, the MS value of the noise source at the output of the first integrator is given as follows.

$$\overline{v_{\mathrm{no}\,1}^2} = \frac{4}{3}\frac{kT}{C_{01}} \qquad (43)$$

The MS noise voltages at the input and output of the second integrator can be derived through similar processes.

The combining noise contribution at the quantizer input is given as follows.

$$\begin{aligned}\overline{v_{n3}^2} &= \frac{2kT}{C_{f1}}\left(1+\frac{C_{f2}}{C_{f1}}+\frac{C_{f3}}{C_{f1}}\right)\\ &= \frac{2kT}{C_{f1}}(1+2+1) = \frac{8kT}{C_{f1}}. \qquad (44)\end{aligned}$$

(assume $C_{f1}=C_{f2}/2=C_{f3}$)

The transfer function of SC integrator is known that

$$H(z) = \frac{z^{-1}}{1-z^{-1}} \qquad (45)$$

By using the superposition principle in the block diagram, the transfer function from the input of the first integrator to the output of the modulator can be found.

$$\mathrm{NTF}_{i1}(z) = \frac{H^2+2H}{1+2H+H^2} = 2z^{-1}-z^{-2}. \qquad (46)$$

Using the same principle, we can derive three additional NTFs.

$$\mathrm{NTF}_{o1}(z) = \frac{H+2}{1+2H+H^2} = (1-z^{-1})(2-z^{-2}). \qquad (47)$$

$$\mathrm{NTF}_{i2}(z) = \frac{H}{1+2H+H^2} = z^{-1}(1-z^{-1}). \qquad (48)$$

$$\mathrm{NTF}_3(z) = \mathrm{NTF}_{o2}(z) = \frac{1}{1+2H+H^2} = (1-z^{-1})^2. \qquad (49)$$

The corresponding frequency responses are shown in Fig.13.

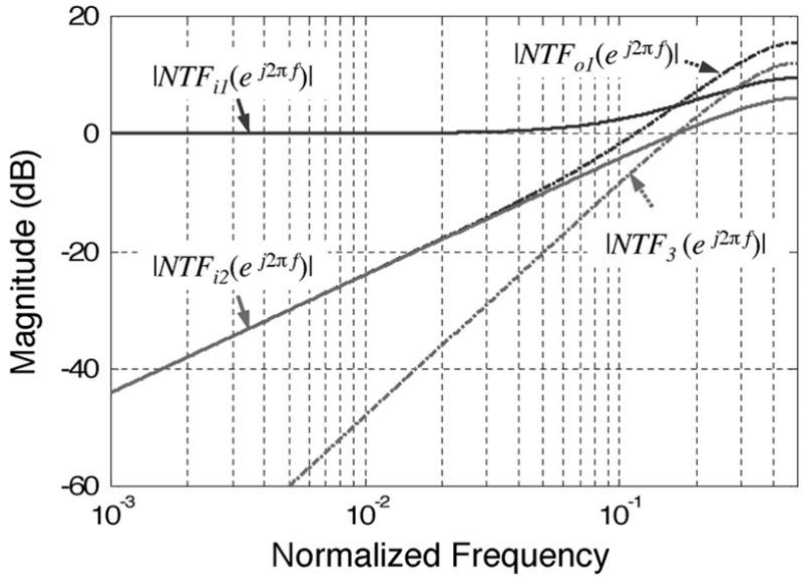


Fig. 13. Frequency responses of the noise power transfer functions.

In the signal band, NTF_{i1} dominates the noise power at the output. (since feedback gain B is smaller than that of the others.)

Integrate all noise PSDs, multiplied by the corresponding power transfer function, from dc to the signal band edge.

$$\overline{N_{i1}^2} = \frac{2\overline{v_{\text{ni1}}^2}}{f_s} \int_0^{f_s/(2\text{OSR})} |\text{NTF}_{i1}|^2 df$$

$$= \overline{v_{\text{ni1}}^2}\left[\frac{5}{\text{OSR}} - \frac{4}{\pi}\sin\left(\frac{\pi}{\text{OSR}}\right)\right] \quad (50)$$

$$\overline{N_{o1}^2} = \overline{v_{\text{no1}}^2}\left[\frac{14}{\text{OSR}} + \frac{4}{\pi}\sin\left(\frac{\pi}{\text{OSR}}\right)\cos\left(\frac{\pi}{\text{OSR}}\right) - \frac{18}{\pi}\sin\left(\frac{\pi}{\text{OSR}}\right)\right] \quad (51)$$

$$\overline{N_{i2}^2} = \overline{v_{\text{ni2}}^2}\left[\frac{2}{\text{OSR}} - \frac{2}{\pi}\sin\left(\frac{\pi}{\text{OSR}}\right)\right] \quad (52)$$

$$\overline{N_3^2} = \left(\overline{v_{\text{no2}}^2} + \overline{v_{n3}^2}\right)\left[\frac{6}{\text{OSR}} - \frac{8}{\pi}\sin\left(\frac{\pi}{\text{OSR}}\right) + \frac{2}{\pi}\sin\left(\frac{\pi}{\text{OSR}}\right)\cos\left(\frac{\pi}{\text{OSR}}\right)\right]. \quad (53)$$

With OSR>>1, we can apply Maclaurin series, which simplifies the expression.

$$\overline{N_{i1}^2} \approx \frac{\overline{v_{\mathrm{ni1}}^2}}{\mathrm{OSR}}, \tag{54}$$

$$\overline{N_{o1}^2} \approx \overline{v_{\mathrm{no1}}^2}\frac{\pi^2}{3\mathrm{OSR}^3} \tag{55}$$

$$\overline{N_{i2}^2} \approx \overline{v_{\mathrm{ni2}}^2}\frac{\pi^2}{3\mathrm{OSR}^3} \tag{56}$$

$$\overline{N_3^2} \approx \left(\overline{v_{\mathrm{no2}}^2} + \overline{v_{n3}^2}\right)\frac{\pi^4}{5\mathrm{OSR}^5}. \tag{57}$$

By summing the noise power from all noise sources at the output, the total output thermal noise can be derived as follows.

$$\begin{aligned}\overline{v_{\mathrm{th}}^2} = {} & 7.24\times10^{-2}\frac{kT}{C_{s1}} + 1.35\times10^{-4}\frac{kT}{C_{01}} \\ & + 2.31\times10^{-4}\frac{kT}{C_{s2}} + 7.73\times10^{-7}\frac{kT}{C_{02}} \\ & + 4.64\times10^{-6}\frac{kT}{C_{f1}}.\end{aligned} \tag{58}$$

Since the first term dominates, the minimum value of C_{s1} can be approximated as follows.

$$C_{s1} \approx 7.24\times10^{-2}\frac{kT}{\overline{v_{\mathrm{th}}^2}} = 0.16\ \mathrm{pF}. \tag{59}$$

Note that the above simplification from (50)~(53) to (54)~(57) is made possible by the high OSR.

8. Conclusion

In chapters 1 to 4, We studied how to design the input-referred noise of an op-amp and how the noise is processed by the switched-capacitor circuit. We also identified optimized circuit parameters to minimize noise while satisfying the settling time requirement. In chapter 5, the reasons for choosing differential pair can be understood from the various advantages compared to the single-ended circuit. In chapter 6 and 7, we cover a practical example that leads to an optimized design by minimizing both noise and cap.

References: Design-oriented estimation of thermal noise in switched-capacitor circuits | IEEE Journals & Magazine | IEEE Xplore