Digital Integrated Circuits
Design Project Supplementary Data

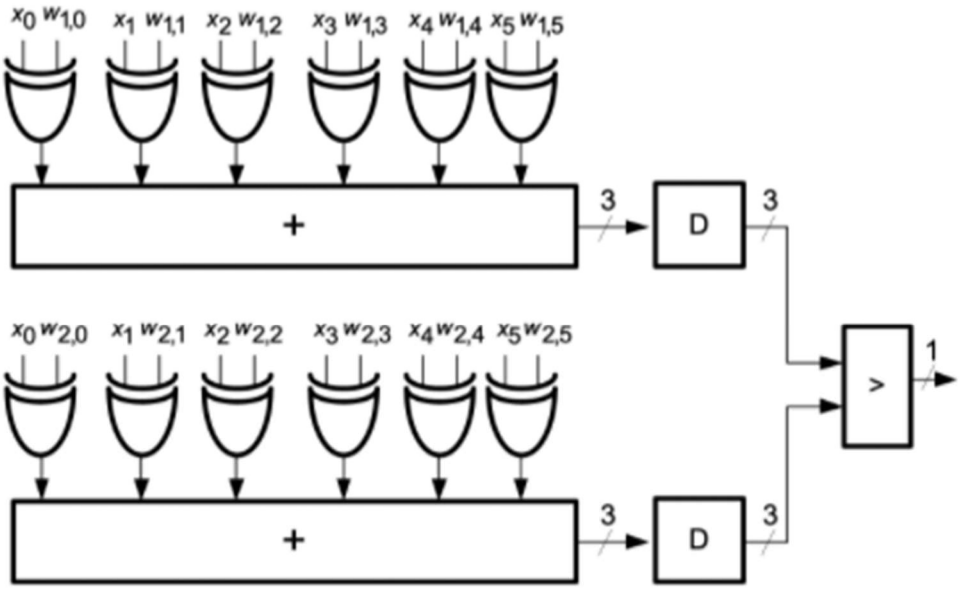


Figure 1. Block diagram of a simple binary classifier.

w1 100101
w2 001011

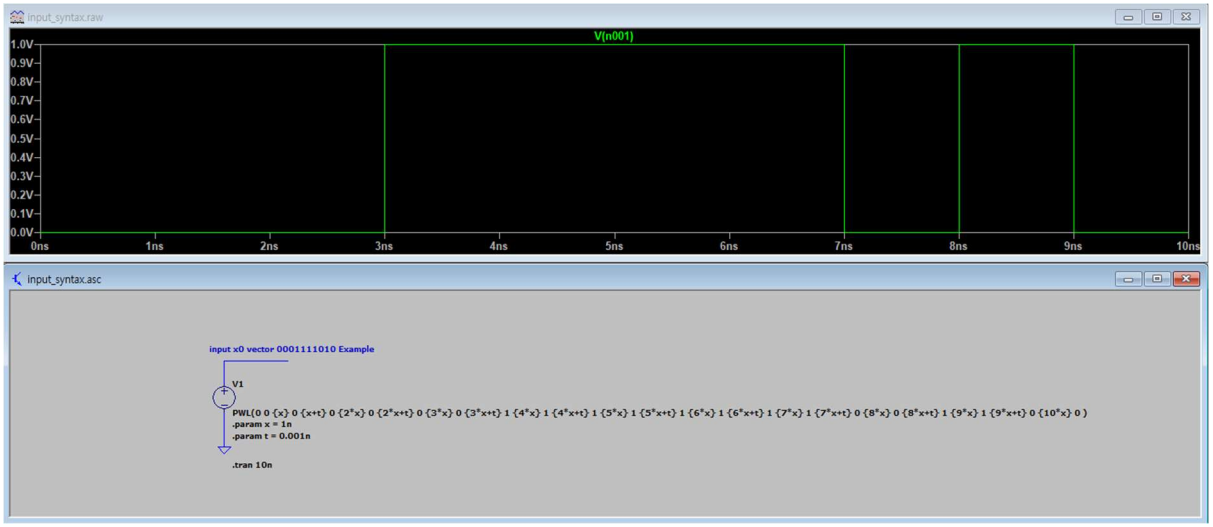
"x(bit number : 5,4,3,2,1,0)"	d1	d2	d1<d2	d1>d2	d1=d2
001100	3	3	0	0	1
000100	2	1	0	1	0
000000	3	1	0	1	0
000111	2	3	1	0	0
101001	2	4	1	0	0
100101	0	2	1	0	0
111111	3	3	0	0	1
100010	3	4	1	0	0
011111	4	5	1	0	0
111100	3	3	0	0	1

x5 PWL(0 0 {x} 0 {x+t} 0 {2*x} 0 {2*x+t} 0 {3*x} 0 {3*x+t} 0 {4*x} 0 {4*x+t} 1 {5*x} 1 {5*x+t} 1 {6*x} 1 {6*x+t} 1 {7*x} 1 {7*x+t} 1 {8*x} 1 {8*x+t} 0 {9*x} 0 {9*x+t} 1 {10*x} 1)
x4 PWL(0 0 {x} 0 {x+t} 0 {2*x} 0 {2*x+t} 0 {3*x} 0 {3*x+t} 0 {4*x} 0 {4*x+t} 0 {5*x} 0 {5*x+t} 0 {6*x} 0 {6*x+t} 1 {7*x} 1 {7*x+t} 0 {8*x} 0 {8*x+t} 1 {9*x} 1 {9*x+t} 1 {10*x} 1)
x3 PWL(0 1 {x} 1 {x+t} 0 {2*x} 0 {2*x+t} 0 {3*x} 0 {3*x+t} 0 {4*x} 0 {4*x+t} 1 {5*x} 1 {5*x+t} 0 {6*x} 0 {6*x+t} 1 {7*x} 1 {7*x+t} 0 {8*x} 0 {8*x+t} 1 {9*x} 1 {9*x+t} 1 {10*x} 1)
x2 PWL(0 1 {x} 1 {x+t} 1 {2*x} 1 {2*x+t} 0 {3*x} 0 {3*x+t} 1 {4*x} 1 {4*x+t} 0 {5*x} 0 {5*x+t} 1 {6*x} 1 {6*x+t} 1 {7*x} 1 {7*x+t} 0 {8*x} 0 {8*x+t} 1 {9*x} 1 {9*x+t} 1 {10*x} 1)
x1 PWL(0 0 {x} 0 {x+t} 0 {2*x} 0 {2*x+t} 0 {3*x} 0 {3*x+t} 1 {4*x} 1 {4*x+t} 0 {5*x} 0 {5*x+t} 0 {6*x} 0 {6*x+t} 1 {7*x} 1 {7*x+t} 1 {8*x} 1 {8*x+t} 1 {9*x} 1 {9*x+t} 0 {10*x} 0)
x0 PWL(0 0 {x} 0 {x+t} 0 {2*x} 0 {2*x+t} 0 {3*x} 0 {3*x+t} 1 {4*x} 1 {4*x+t} 1 {5*x} 1 {5*x+t} 1 {6*x} 1 {6*x+t} 1 {7*x} 1 {7*x+t} 0 {8*x} 0 {8*x+t} 1 {9*x} 1 {9*x+t} 0 {10*x} 0)

➢ Simulation data

In the design project, each simulation has to simulate 6 parallel bit stream for estimation.

There are examples of W and X vectors in the attached text file, and examples of how to implement bitstream using the PWL type voltage source in the attached .asc file.



Attached .asc simulation window

The .asc file attached to the post is a simulation example in which the 0001111010 signal is input sequentially according to the system clk.

Parameter x : parameter for 1 Bit time

Parameter t : parameter for Rising/Falling time