Digital Integrated Circuits (001)
Design Project 2021 Winter

Background

A common problem in machine learning applications is to classify a data vector ***x*** into two classes -- class 1 and class 2. This is called a binary hypothesis problem, e.g., classification of ECG signals into normal or abnormal categories. Class 1 and class 2 are represented by weight vectors $\boldsymbol{w_1}$ and $\boldsymbol{w_2}$. First a feature extractor computes the distance between ***x*** and $\boldsymbol{w_1}$ and between ***x*** and $\boldsymbol{w_2}$. This step results in two scalars called features, i.e., the two distances. Next, the minimum of the two distances is computed and the index of the weight vectors is output as the class into which the data vector ***x*** has been classified.

Project

The goal of this project is to design a simple binary classifier. Figure 1 shows the block diagram of the classifier to be implemented along with the data precisions. Here, the data and weight vectors are binary, and the distance measures being computed is the well-known Hamming Distance (HD).

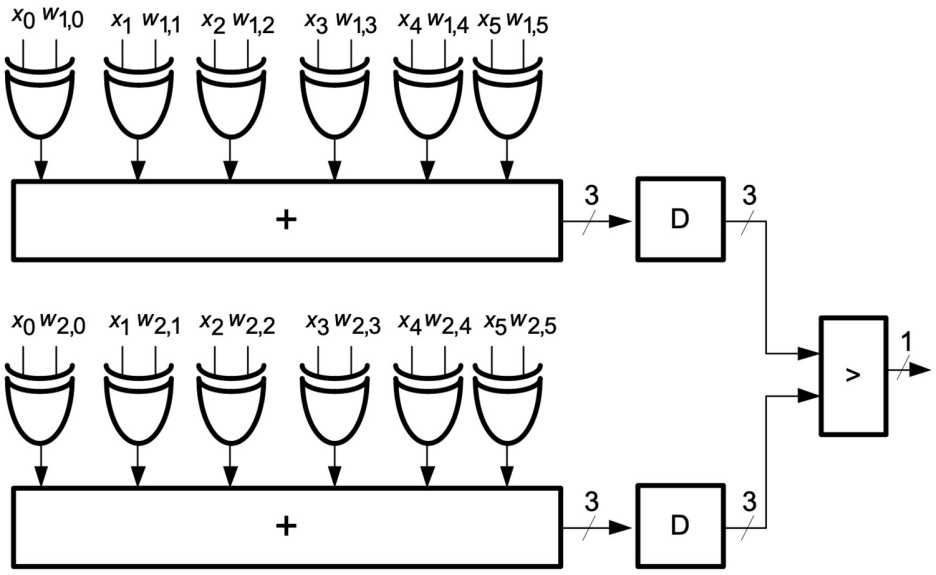


Figure 1. Block diagram of a simple binary classifier.

You can assume a global input clock with rise and fall times ~10ps, $\boldsymbol{x} = [x_0, \ldots, x_{N-1}]$, $\boldsymbol{w_1} = [w_{1,0}, \ldots, w_{1,N-1}]$, and $\boldsymbol{w_2} = [w_{2,0}, \ldots, w_{2,N-1}]$ are the input vector, the first and the second weight vectors, respectively. The comparator output will be 1(high) when the Hamming distances are the same. Assume that N = 6. The following circuits need to be designed:

- XOR gates
- Adder with six 1-bit inputs and a 3-bit output
- 3-bit comparator block
- Registers (Flip-flops)

The design goal is to minimize the Energy-Delay Product (*EDP*):

$$EDP = E \times T_p$$

where E is the average energy per clock cycle and T_p is the critical path delay of the classifier.

Because the energy consumption is input-pattern dependent, an input data set will be provided to measure the average energy and to prove the correctness of the design. To measure T_p, you should identify the critical path in your design, determine the input sequence that excites this critical path. Then, you need to simulate your circuit with this critical input to obtain T_p.
To minimize *EDP*, you can tune the supply voltage, clock frequency, logic style, and transistor sizing. You may employ pipelining or parallelization techniques if these help reduce the *EDP*.

Deliverables

- Project Report: The report should be no longer than 10 pages including the following:
    - Gate-level and transistor-level schematics of each gate with the transistor dimensions indicated.
    - SPICE simulations to show: 1) correct functionality, 2) energy measurement results, and 3) critical path delay measurement.
    - Description of design process and decisions made, e.g. choice of logic family, adder, comparator, and latch architectures, steps/optimizations taken to minimize *EDP*, and any unique design choices made.
    - Overall discussion of your design with sufficient details
- SPICE netlist files:
    - Testbench for measuring energy consumption and checking circuit functionality
    - Techbench for measuring critical path delay

Grading

- 60%: Technical quality of your design (completeness, correct functionality, *EDP* minimization, analysis, etc.)
- 10%: *EDP* minimization results
- 30%: Clarity and exposition of your written report

References

1) hamming distance

https://en.wikipedia.org/wiki/Hamming_code

2) Adder

https://en.wikipedia.org/wiki/Adder_(electronics)

3) Comparator

https://en.wikipedia.org/wiki/Digital_comparator

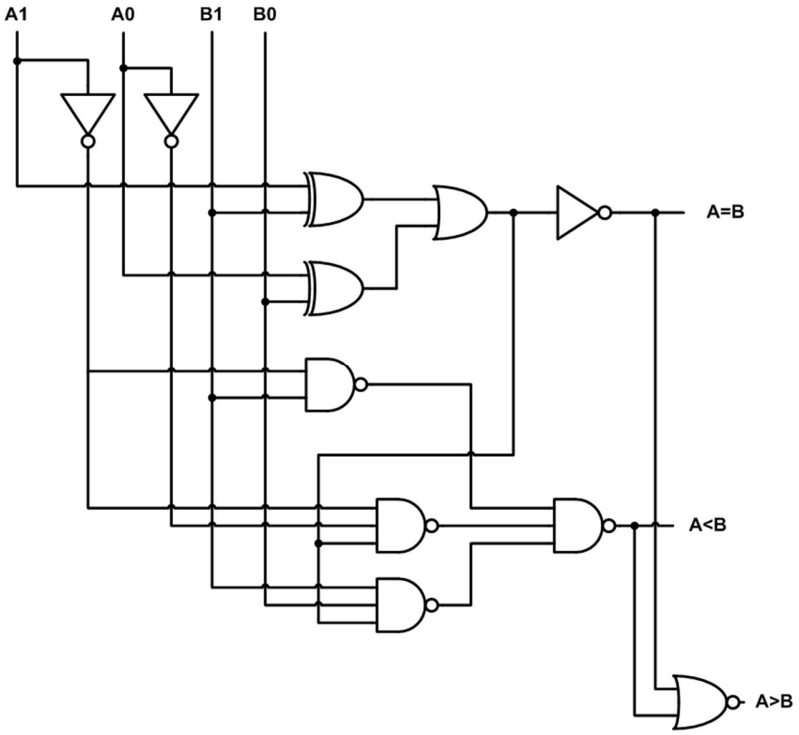
4) n-bit Comparator

https://electronicscoach.com/digital-comparator.html

https://www.elprocus.com/digital-comparator-and-magnitude-comparator/

5) 2-bit Comparator Example

Shown below is an example for a 2-bit comparator. You don’t have to use it.


A1
A0
B1
B0
A=B
A<B
A>B