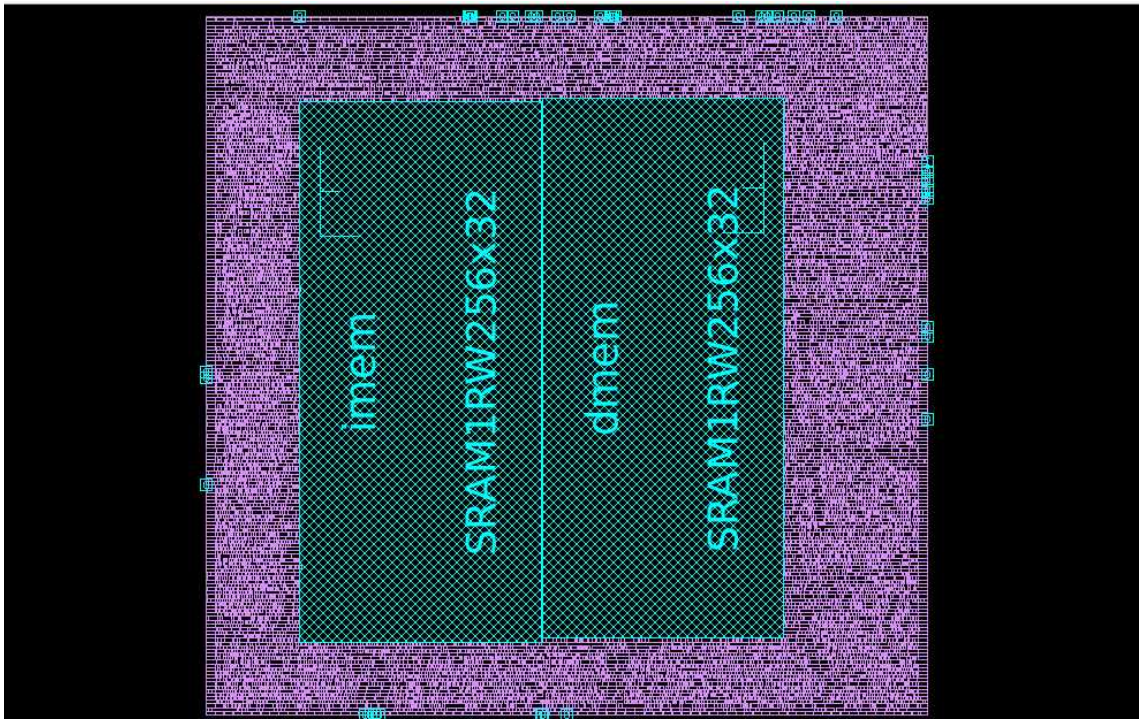
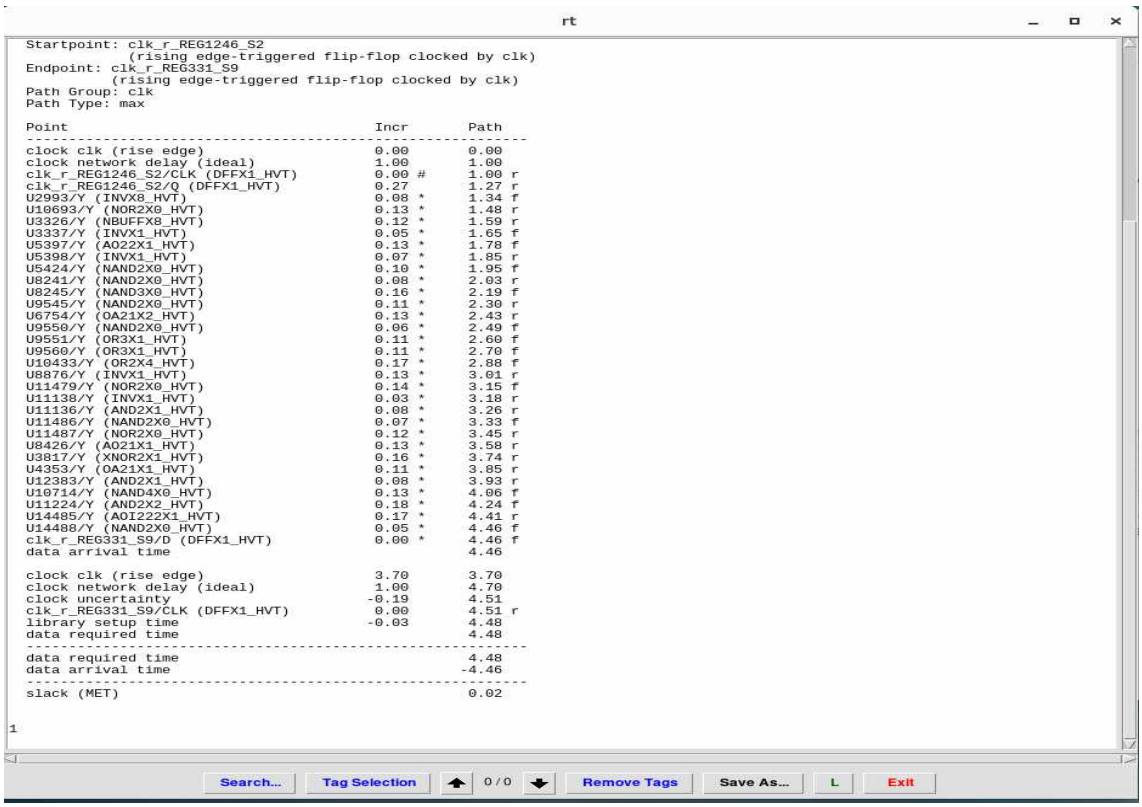
## 프로젝트 결과

## 1. 주기 3.7, 다이의 크기 330/330으로 설정했을 때 결과

Schematic




setup-time



constraint

```
  max_transition

                          Required        Actual
  Net                    Transition     Transition        Slack
  ---------------------------------------------------------------
  n16784                     0.12           0.12           0.00  (VIOLATED: increase significant
digits)
  n17175                     0.12           0.12           0.00  (VIOLATED: increase significant
digits)
  n17106                     0.12           0.12           0.00  (VIOLATED: increase significant
digits)

  ---------------------------------------------------------------
  Total                     3                 -0.01

  max_capacitance

                          Required        Actual
  Net                    Capacitance    Capacitance       Slack
  ---------------------------------------------------------------
  n19227                    32.00          33.73          -1.73  (VIOLATED)

  ---------------------------------------------------------------
  Total                     1                 -1.73

  max_leakage_power

                          Required        Actual
  Design                 Leakage Power  Leakage Power     Slack
  ---------------------------------------------------------------
  mips                       0.00       538432064.00   -538432064.00
                                                                (VIOLATED)


1
```

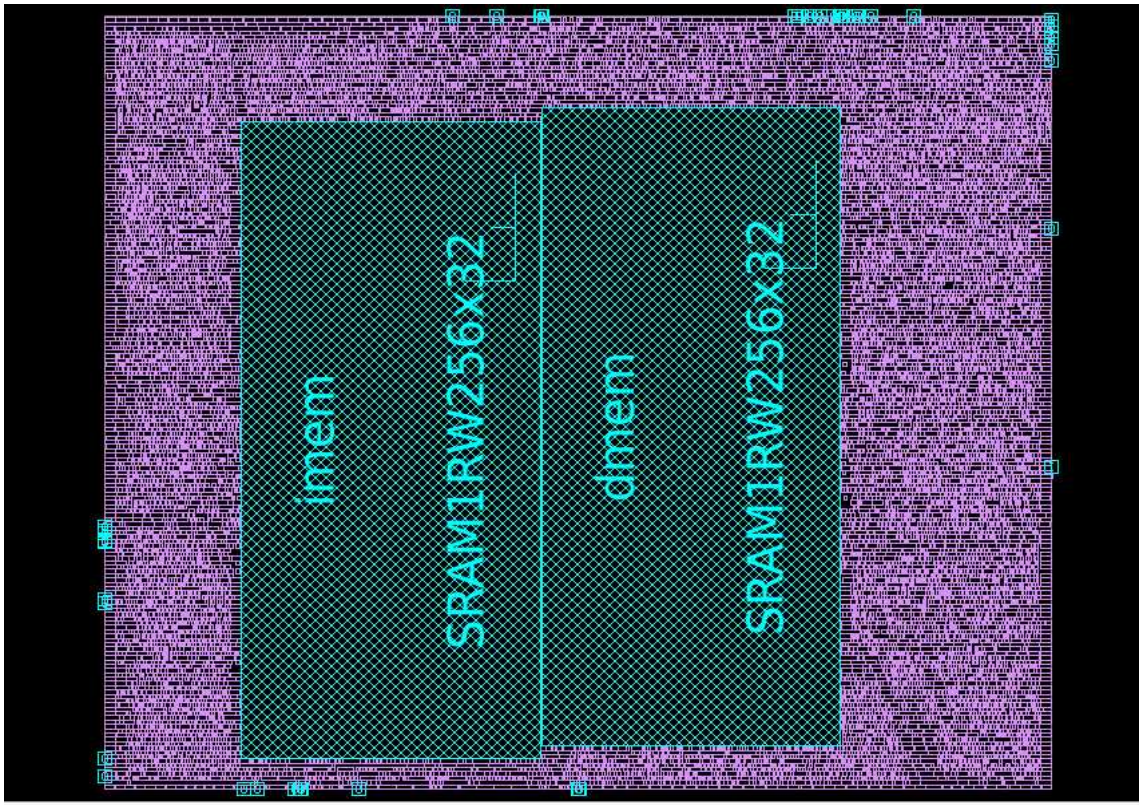
Formaility

```
***************************** Guidance Summary ******************************
                                    Status
Command                 Accepted   Rejected  Unsupported  Unprocessed  Total
-------------------------------------------------------------------------------
architecture_netlist:          1          0            0            0          1
boundary            :          1          0            0            0          1
boundary_netlist    :          1          0            0            0          1
change_names        :         23          0            0            0         23
checkpoint          :          1          0            0            0          1
datapath            :          1          0            0            0          1
environment         :          8          0            0            0          8
instance_map        :          3          0            0            0          3
mark                :          2          0            0            0          2
merge               :          4          0            0            0          4
reg_constant        :          2          0            0            0          2
reg_merging         :         26          0            0            0         26
replace             :          7          0            0            0          7
retiming            :       7128          0            0            0       7128
retiming_finished   :          1          0            0            0          1
ungroup             :          3          0            0            0          3
-------------------------------------------------------------------------------
Total               :       7212          0            0            0       7212
```

결과정리 – 현재 환경에 대한 최적화를 진행했음에도 setup time margin이 많이 부족한걸 확인, 최적화를 하는 과정에서 셀들의 배치가 기존에 verilog로 작성된 배치보다 많이 변화된 것을 볼 수 있음.

## 2. 주기 3.7, 다이의 크기 340/340으로 설정했을 때 결과

Schematic




setup-time

```
Point                                          Incr       Path
-------------------------------------------------------------
clock clk (rise edge)                          0.00       0.00
clock network delay (ideal)                    1.00       1.00
clk_r_REG1287_S2/CLK (DFFX2_HVT)               0.00 #     1.00 r
clk_r_REG1287_S2/QN (DFFX2_HVT)                0.21       1.21 f
U13714/Y (INVX4_RVT)                           0.08 *     1.29 r
U2615/Y (INVX8_HVT)                            0.08 *     1.38 f
U11568/Y (OAI22X1_HVT)                         0.14 *     1.52 r
U5131/Y (OR2X1_HVT)                            0.08 *     1.60 r
U5269/Y (OAI21X1_HVT)                          0.19 *     1.79 f
U5149/Y (AND2X1_HVT)                           0.13 *     1.93 f
U5151/Y (INVX1_HVT)                            0.05 *     1.97 r
U5152/Y (NAND2X0_HVT)                          0.05 *     2.03 f
U10280/Y (NAND2X0_HVT)                         0.09 *     2.12 r
U5155/Y (NAND2X0_HVT)                          0.07 *     2.19 f
U5156/Y (OAI21X1_HVT)                          0.15 *     2.34 r
U5192/Y (OR3X1_HVT)                            0.11 *     2.44 r
U10867/Y (OR3X1_HVT)                           0.10 *     2.54 r
U5355/Y (OR2X4_HVT)                            0.16 *     2.70 r
U12802/Y (NAND2X0_HVT)                         0.20 *     2.90 f
U5112/Y (OAI21X2_HVT)                          0.24 *     3.14 r
U11335/Y (AO21X1_HVT)                          0.12 *     3.26 r
U11236/Y (AO21X1_HVT)                          0.13 *     3.39 r
U3436/Y (INVX1_HVT)                            0.07 *     3.46 f
U3254/Y (OAI21X1_HVT)                          0.18 *     3.64 r
U3587/Y (AOI21X1_HVT)                          0.16 *     3.80 f
U14741/Y (XOR2X1_HVT)                          0.15 *     3.95 r
U14748/Y (OA21X1_HVT)                          0.11 *     4.06 r
U3567/Y (AOI21X1_HVT)                          0.11 *     4.17 f
U14752/Y (NAND2X0_HVT)                         0.04 *     4.21 r
clk_r_REG487_S3/D (DFFX2_HVT)                  0.00 *     4.21 r
data arrival time                                         4.21

clock clk (rise edge)                          3.50       3.50
clock network delay (ideal)                    1.00       4.50
clock uncertainty                             -0.17       4.32
clk_r_REG487_S3/CLK (DFFX2_HVT)                0.00       4.32 r
library setup time                            -0.10       4.22
data required time                                        4.22
-------------------------------------------------------------
data required time                                        4.22
data arrival time                                        -4.21
-------------------------------------------------------------
slack (MET)                                               0.01
```

constraint

```
****************************************
Report : constraint
         -all_violators
Design : mips
Version: T-2022.03-SP2
Date   : Tue Apr 22 21:34:37 2025
****************************************


   max_transition

                            Required        Actual
   Net                     Transition     Transition        Slack
   -----------------------------------------------------------------
   add_x_9/B[15]                0.12           0.12         -0.01  (VIOLATED)
       PIN :    clk_r_REG12_S4/Q
                                0.12           0.12         -0.01  (VIOLATED)
   n22785                       0.12           0.12          0.00  (VIOLATED: increase significant digits)
   add_x_9/B[23]                0.12           0.12          0.00  (VIOLATED: increase significant digits)
   add_x_9/B[17]                0.12           0.12          0.00  (VIOLATED: increase significant digits)
   add_x_9/B[18]                0.12           0.12          0.00  (VIOLATED: increase significant digits)
   n17179                       0.12           0.12          0.00  (VIOLATED: increase significant digits)
   n17135                       0.12           0.12          0.00  (VIOLATED: increase significant digits)
   n17842                       0.12           0.12          0.00  (VIOLATED: increase significant digits)
   n17077                       0.09           0.09          0.00  (VIOLATED: increase significant digits)

   -----------------------------------------------------------------
   Total                    9                 -0.01

   max_leakage_power

                            Required        Actual
   Design                 Leakage Power  Leakage Power     Slack
   -----------------------------------------------------------------
   mips                         0.00       557491456.00   -557491456.00
                                                                (VIOLATED)


1
```

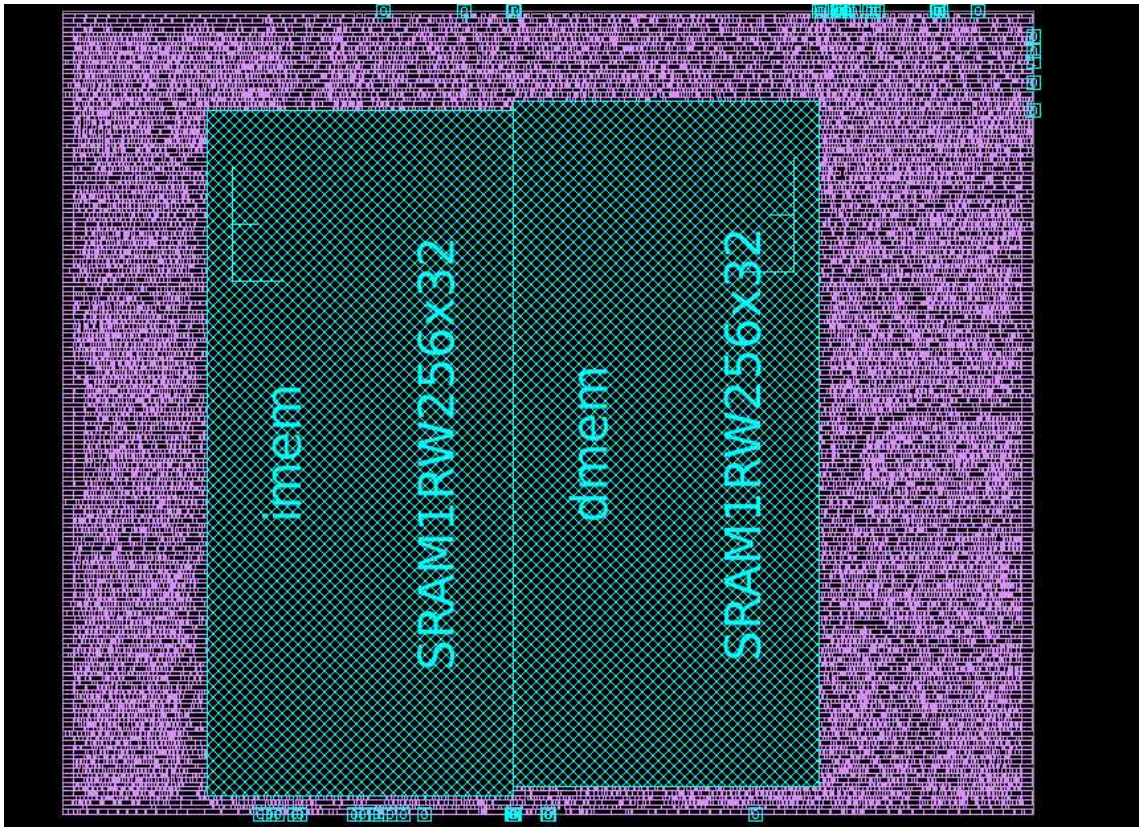
Formaility

```
****************************** Guidance Summary ******************************
                                        Status
Command                  Accepted   Rejected  Unsupported  Unprocessed  Total
-------------------------------------------------------------------------------
architecture_netlist:           1          0            0            0          1
boundary             :          1          0            0            0          1
boundary_netlist     :          1          0            0            0          1
change_names         :         23          0            0            0         23
checkpoint           :          1          0            0            0          1
datapath             :          1          0            0            0          1
environment          :          8          0            0            0          8
instance_map         :          3          0            0            0          3
mark                 :          2          0            0            0          2
merge                :          4          0            0            0          4
reg_constant         :          2          0            0            0          2
reg_merging          :         26          0            0            0         26
replace              :          7          0            0            0          7
retiming             :       7128          0            0            0       7128
retiming_finished    :          1          0            0            0          1
ungroup              :          3          0            0            0          3
-------------------------------------------------------------------------------
Total                :       7212          0            0            0       7212
```

결과정리 – 두 번째 테스트로 주기는 그대로 하고 다이의 크기만을 증가시켰지만 여전히 setup time margin은 여전히 부족하지만 Formaility를 비교해보면 전 실험과 동일한 결과가 나오고 constraint 결과를 비교했을 때 다이의 크기가 증가하면 constraint에서 capcitance가 줄어들었음을 확인 할 수 있었음

## 3. 주기를 3.5, 다이의 크기를  330/330으로 설정했을 때

Schematic




setup-time

```
Point                                          Incr       Path
-------------------------------------------------------------
clock clk (rise edge)                          0.00       0.00
clock network delay (ideal)                    1.00       1.00
clk_r_REG1287_S2/CLK (DFFX1_HVT)               0.00 #     1.00 r
clk_r_REG1287_S2/QN (DFFX1_HVT)                0.23       1.23 f
U2850/Y (INVX4_HVT)                            0.10 *     1.33 r
U2963/Y (NAND2X0_HVT)                          0.16 *     1.49 f
U12455/Y (INVX4_HVT)                           0.11 *     1.60 r
U12462/Y (INVX4_HVT)                           0.11 *     1.71 f
U6532/Y (AO22X1_HVT)                           0.12 *     1.84 f
U6946/Y (OR2X1_HVT)                            0.12 *     1.95 f
U7008/Y (NOR2X0_HVT)                           0.11 *     2.07 r
U7009/Y (OR2X1_HVT)                            0.07 *     2.14 r
U7012/Y (NAND3X0_HVT)                          0.10 *     2.24 f
U7013/Y (INVX1_HVT)                            0.07 *     2.31 r
U13048/Y (OA22X1_HVT)                          0.12 *     2.43 r
U7043/Y (NAND2X0_HVT)                          0.06 *     2.49 f
U7044/Y (OR3X1_HVT)                            0.09 *     2.58 f
U7079/Y (OR3X1_HVT)                            0.10 *     2.68 f
U7382/Y (NOR2X0_HVT)                           0.14 *     2.82 r
U8524/Y (INVX8_HVT)                            0.11 *     2.93 f
U12374/Y (INVX1_HVT)                           0.07 *     3.00 r
U6656/Y (NAND4X0_HVT)                          0.19 *     3.19 f
U5497/Y (OR3X1_HVT)                            0.19 *     3.37 f
U12769/Y (AND2X1_HVT)                          0.08 *     3.45 f
U3889/Y (OR2X1_HVT)                            0.08 *     3.53 f
U10947/Y (INVX1_HVT)                           0.03 *     3.56 r
U5414/Y (AND2X2_HVT)                           0.12 *     3.68 r
U12305/Y (NAND2X0_HVT)                         0.07 *     3.75 f
U10950/Y (NAND4X0_HVT)                         0.06 *     3.81 r
U10417/Y (AOI22X1_HVT)                         0.13 *     3.94 f
U6920/Y (AND2X4_HVT)                           0.15 *     4.08 f
U12682/Y (OAI22X1_HVT)                         0.13 *     4.21 r
clk_r_REG30_S13/D (DFFX1_HVT)                  0.00 *     4.21 r
data arrival time                                         4.21

clock clk (rise edge)                          3.50       3.50
clock network delay (ideal)                    1.00       4.50
clock uncertainty                             -0.17       4.32
clk_r_REG30_S13/CLK (DFFX1_HVT)                0.00       4.32 r
library setup time                            -0.07       4.26
data required time                                       4.26
-------------------------------------------------------------
data required time                                       4.26
data arrival time                                       -4.21
-------------------------------------------------------------
slack (MET)                                              0.05

1
```

constraint

```
max_transition

                         Required        Actual
Net                     Transition      Transition        Slack
-----------------------------------------------------------------
add_x_9/B[12]              0.12            0.12           0.00  (VIOLATED: increase significant digits)
add_x_9/B[29]              0.12            0.12           0.00  (VIOLATED: increase significant digits)
add_x_9/B[13]              0.12            0.12           0.00  (VIOLATED: increase significant digits)
n17275                     0.12            0.12           0.00  (VIOLATED: increase significant digits)

-----------------------------------------------------------------
Total                    4                 -0.01

max_leakage_power

                         Required        Actual
Design                  Leakage Power  Leakage Power     Slack
-----------------------------------------------------------------
mips                       0.00       553073920.00   -553073920.00
                                                                (VIOLATED)
```

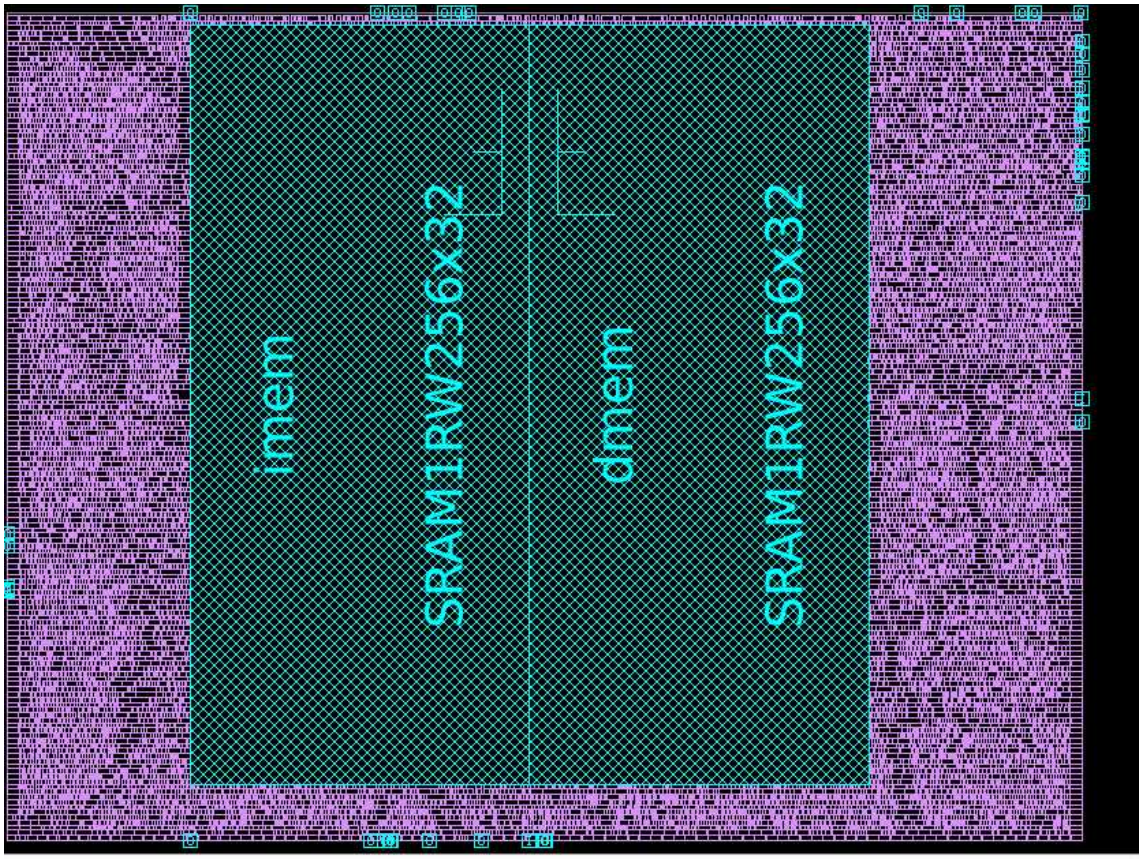
Formaility

```
***************************** Guidance Summary ******************************
                                        Status
Command                  Accepted   Rejected  Unsupported  Unprocessed  Total
-------------------------------------------------------------------------------
architecture_netlist:           1          0            0            0          1
boundary            :           1          0            0            0          1
boundary_netlist    :           1          0            0            0          1
change_names        :          23          0            0            0         23
checkpoint          :           1          0            0            0          1
datapath            :           1          0            0            0          1
environment         :           8          0            0            0          8
instance_map        :           3          0            0            0          3
mark                :           2          0            0            0          2
merge               :           4          0            0            0          4
reg_constant        :           2          0            0            0          2
reg_merging         :          26          0            0            0         26
replace             :           7          0            0            0          7
retiming            :        8190          0            0            0       8190
retiming_finished   :           1          0            0            0          1
ungroup             :           3          0            0            0          3
-------------------------------------------------------------------------------
Total               :        8274          0            0            0       8274
```

결과정리 – 다이의 크기는 첫 번째 실험과 동일하지만 주기를 짧게 바꾸었더니 Formaility에서는 재배치된 셀들의 숫자가 늘어났으나 동작에는 이상이 없었고, constraint에서는 값들이 줄었으며 setup-time margin 증가하였으나 많이 증가하였으나 마진의 값의 차이가 크지 않음을 확인

## 4.주기를 3.5,다이의 크기를 360/270으로 설정했을 때

Schematic




setup-time

| Point | Incr | Path |
|---|---|---|
| clock clk (rise edge) | 0.00 | 0.00 |
| clock network delay (ideal) | 1.00 | 1.00 |
| clk_r_REG1156_S7/CLK (DFFX2_HVT) | 0.00 # | 1.00 r |
| clk_r_REG1156_S7/QN (DFFX2_HVT) | 0.21 | 1.21 r |
| U9152/Y (NBUFFX4_HVT) | 0.11 * | 1.32 r |
| U2654/Y (INVX8_HVT) | 0.10 * | 1.42 f |
| U2890/Y (NBUFFX4_HVT) | 0.14 * | 1.56 f |
| U3139/Y (NAND2X0_HVT) | 0.07 * | 1.63 r |
| U3140/Y (OA21X1_HVT) | 0.10 * | 1.73 r |
| U3143/Y (NAND2X0_HVT) | 0.06 * | 1.79 f |
| U3144/Y (OR3X1_HVT) | 0.10 * | 1.90 f |
| U6417/Y (OR2X1_HVT) | 0.09 * | 1.99 f |
| U8300/Y (NBUFFX8_HVT) | 0.12 * | 2.11 f |
| U6607/Y (NAND2X0_HVT) | 0.14 * | 2.25 r |
| U6085/Y (OAI21X1_HVT) | 0.20 * | 2.45 f |
| U9513/Y (AO21X1_HVT) | 0.08 * | 2.53 f |
| U9419/Y (AO21X1_HVT) | 0.13 * | 2.66 f |
| U5613/Y (AOI21X1_HVT) | 0.18 * | 2.84 r |
| U9059/Y (OA21X1_HVT) | 0.14 * | 2.98 r |
| U4279/Y (OAI22X1_HVT) | 0.14 * | 3.11 f |
| U6952/Y (AO22X1_HVT) | 0.08 * | 3.20 f |
| U6837/Y (XOR2X1_HVT) | 0.15 * | 3.34 r |
| U8918/Y (OR2X1_HVT) | 0.08 * | 3.43 r |
| U6671/Y (AND4X4_HVT) | 0.24 * | 3.66 r |
| U8586/Y (INVX2_HVT) | 0.06 * | 3.72 f |
| U7591/Y (AND2X1_HVT) | 0.09 * | 3.81 f |
| U8075/Y (NAND2X0_HVT) | 0.05 * | 3.86 r |
| U8076/Y (OA21X1_HVT) | 0.10 * | 3.96 r |
| U8077/Y (AO22X1_HVT) | 0.12 * | 4.07 r |
| clk_r_REG519_S20/D (DFFX1_HVT) | 0.00 * | 4.07 r |
| data arrival time | | 4.07 |
| | | |
| clock clk (rise edge) | 3.50 | 3.50 |
| clock network delay (ideal) | 1.00 | 4.50 |
| clock uncertainty | -0.17 | 4.32 |
| clk_r_REG519_S20/CLK (DFFX1_HVT) | 0.00 | 4.32 r |
| library setup time | -0.08 | 4.25 |
| data required time | | 4.25 |
| data required time | | 4.25 |
| data arrival time | | -4.07 |
| slack (MET) | | 0.18 |

constraint

```
max_transition

                         Required        Actual
Net                     Transition     Transition        Slack
-------------------------------------------------------------
n21459                       0.09           0.09         -0.01  (VIOLATED)
    PIN :   clk_r_REG1193_S7/Q
                             0.09           0.09         -0.01  (VIOLATED)
n17511                       0.09           0.09         -0.01  (VIOLATED)
    PIN :   clk_r_REG1221_S7/Q
                             0.09           0.09         -0.01  (VIOLATED)
n17399                       0.12           0.12          0.00  (VIOLATED: increase significant digits)
n17047                       0.12           0.12          0.00  (VIOLATED: increase significant digits)

-------------------------------------------------------------
Total                     4                 -0.02

max_leakage_power

                         Required        Actual
Design                  Leakage Power  Leakage Power     Slack
-------------------------------------------------------------
mips                         0.00       507576640.00   -507576640.00
                                                                (VIOLATED)


1
```

Formaility

```
***************************** Guidance Summary ******************************
                                        Status
Command                  Accepted   Rejected  Unsupported  Unprocessed  Total
-------------------------------------------------------------------------------
architecture_netlist:           1          0            0            0          1
boundary             :          1          0            0            0          1
boundary_netlist     :          1          0            0            0          1
change_names         :         23          0            0            0         23
checkpoint           :          1          0            0            0          1
datapath             :          1          0            0            0          1
environment          :          8          0            0            0          8
instance_map         :          3          0            0            0          3
mark                 :          2          0            0            0          2
merge                :          4          0            0            0          4
reg_constant         :          2          0            0            0          2
reg_merging          :         26          0            0            0         26
replace              :          7          0            0            0          7
retiming             :       8190          0            0            0       8190
retiming_finished    :          1          0            0            0          1
ungroup              :          3          0            0            0          3
-------------------------------------------------------------------------------
Total                :       8274          0            0            0       8274
```

결과정리 – 첫 번째 테스트와 비교했을 때 주기를 짧게하고 최적화된 다이의 크기를 사용을 했을 때 setup-time margin이 확연히 증가했다는 사실로 미루어 보았을 때 각 Schematic마다 차이는 존재하나 면적과 칩속도를 최적화하는데의 기준은 처음에는 굉장히 타이트하게 잡아서 margin 값이 적더라도 최적화하는 과정을 거쳐서 넉넉한 마진과 다이의 크기를 정할수있도록 하는 것 중요하다는 걸 알게됨. 그리고 나머지 값들을 비교했을 때 constraint는 이변이 것의 없었지만 capitence가 사라진걸 볼 수 있고  Formaility또한 앞서 했던 테스트처럼 변화가 것이 없는 것을 보임.

## 3. 프로젝트 느낀점

실제 verilog로 구현한 mips를 Front-End과정을 적용하는 이번 프로젝트를 통해서 정리해보면서 Front-End과정에서는 Front-End과정에 대한 지식만을 요구하는 것이 아닌 다른 단계 즉 RTL,Front-End(Pi),Back_end(Pd)에 대한 모든 지식이 요구가 된다는 것을 알게 되었으며 실제 시놉시사의 디자인 컴파일러를 사용함에 따라서 실제 업무에 대한 이해도를 늘릴 수 있는 시간이 되었으며 이 프로젝트를 통해서 업무에 대한 지식과 경험이 왜 필요한지 경험자와 비경험자와 왜 차이가 존재 할 수밖에 없는지 등을 알 수 있는 프로젝트여서 이 분야에 대한 흥미를 더 불러드릴 수 있는 시간이었다.