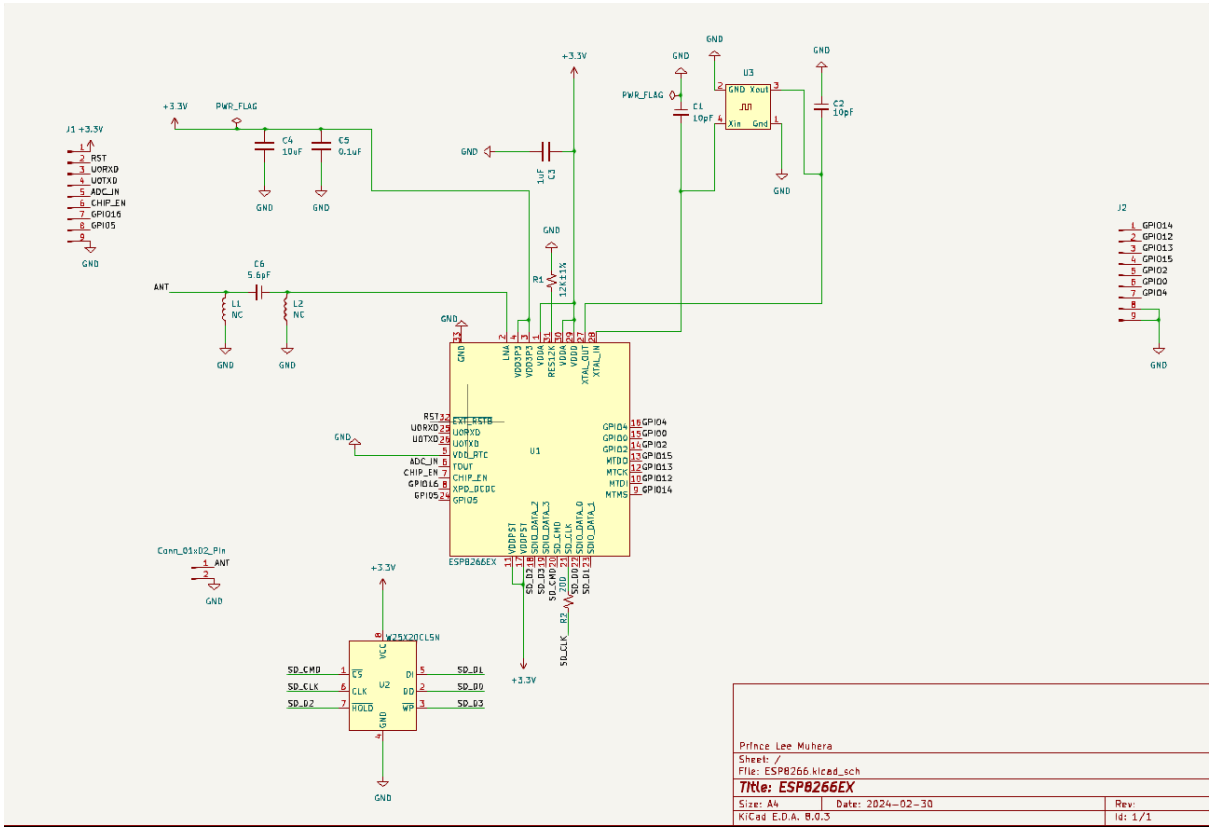
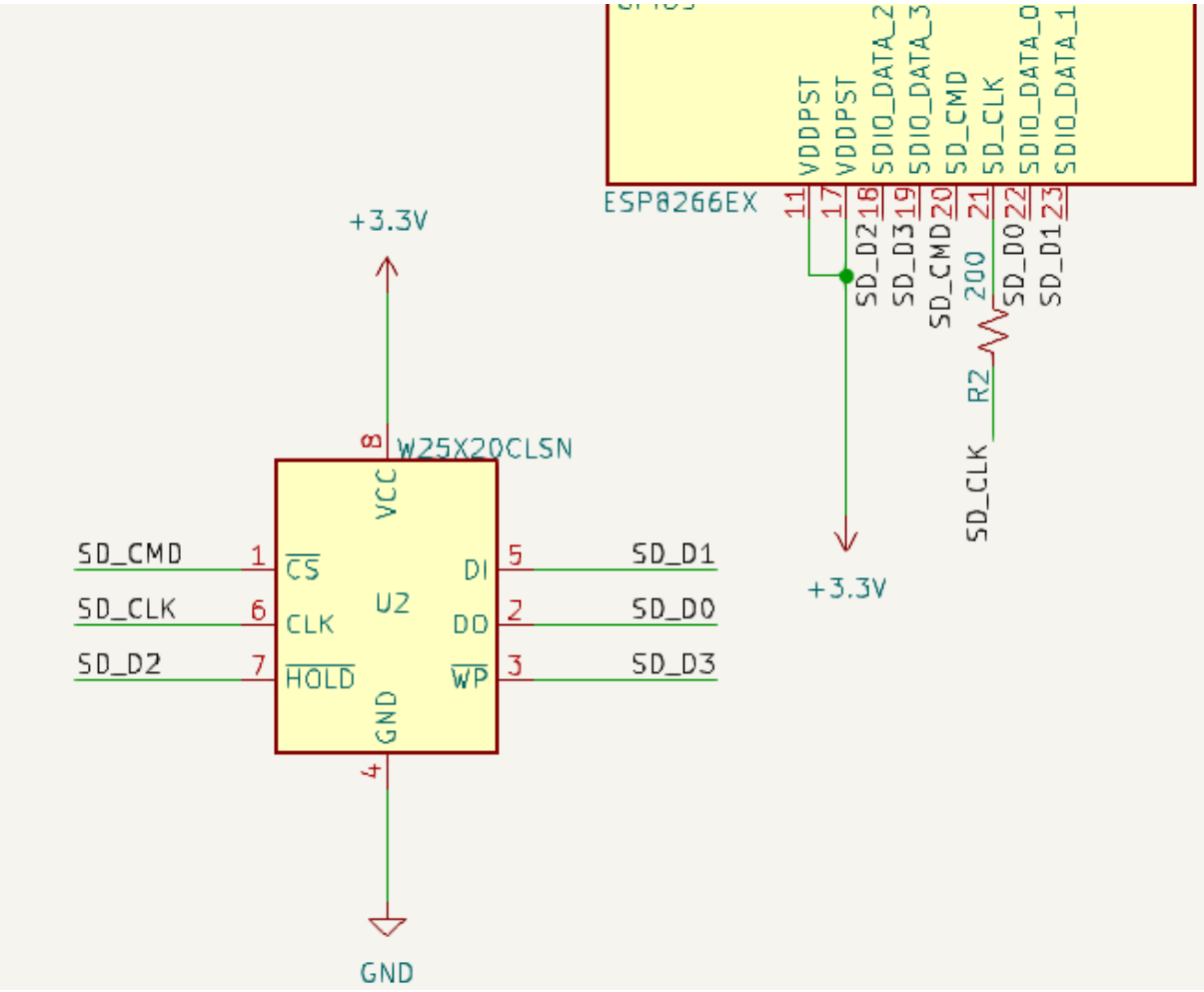
ESP8266EX

Schematic



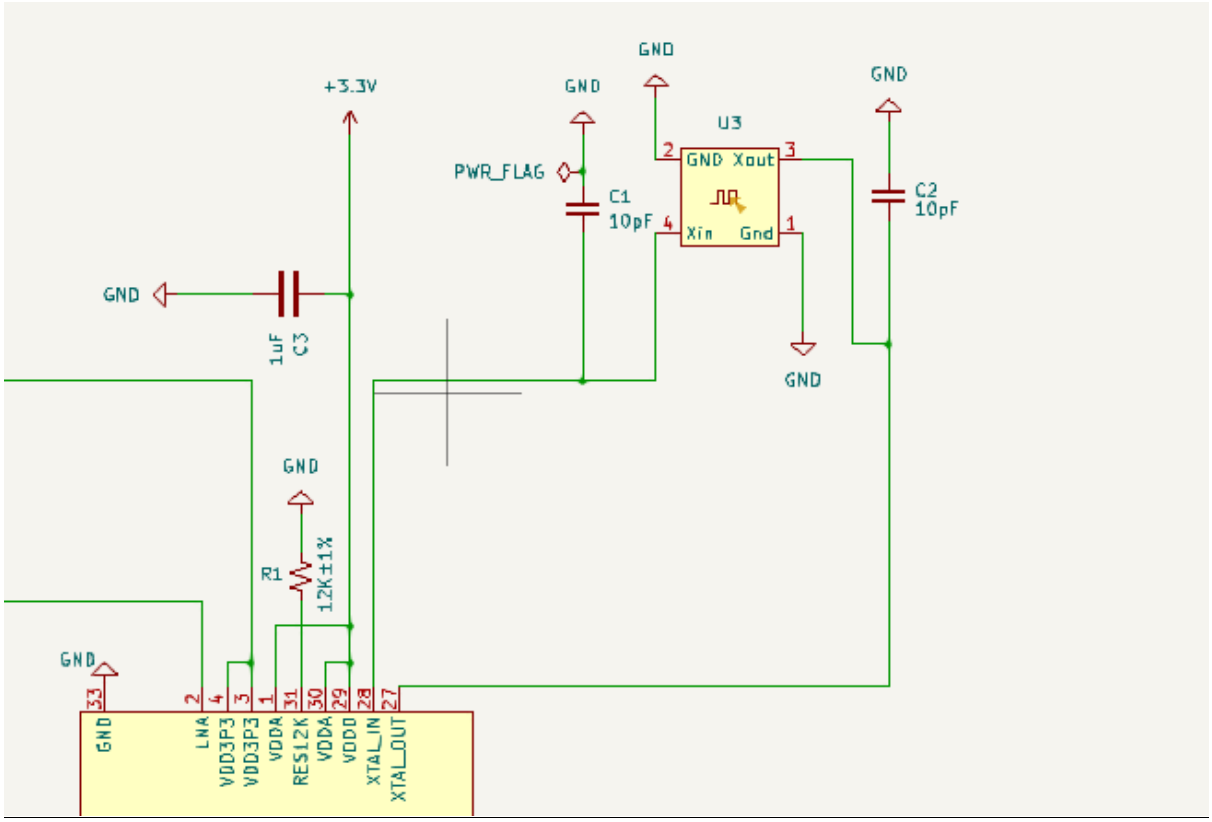
Flash

The resistor is connected to the SLD_CLK pin via serial port so as to reduce cross-talk and also lower driving current. It creates a voltage divider network with the parasitic capacitance of the trace and the pin. This voltage divider network reduces the voltage swing on the SD_CLK pin and consequently reduces the cross-talk.



Crystal Oscillator

The values of the two capacitors can be flexible, ranging from 6pF to 22pF, however, the specific capacitive values of C1 and C2 depend on further testing and adjustment on the overall performance of the whole circuit. Normally, the capacitive values of C1 and C2 are within 10pF if the crystal oscillator frequency is 26MHz, while the values of C1 and C2 are 10pF.



RF section

If the antenna is approaching 50 ohms then no matching is required since the output impedance of pin 2 is 50 ohms. However cheap antennas do not have 50 ohms impedance, so the N – type matching is there to help with the matching.

The resistance measured at the terminals of the antenna accounts for the power that is radiated from the antenna which is primarily the “radiation resistance”.

Antenna exhibits two types of noise:

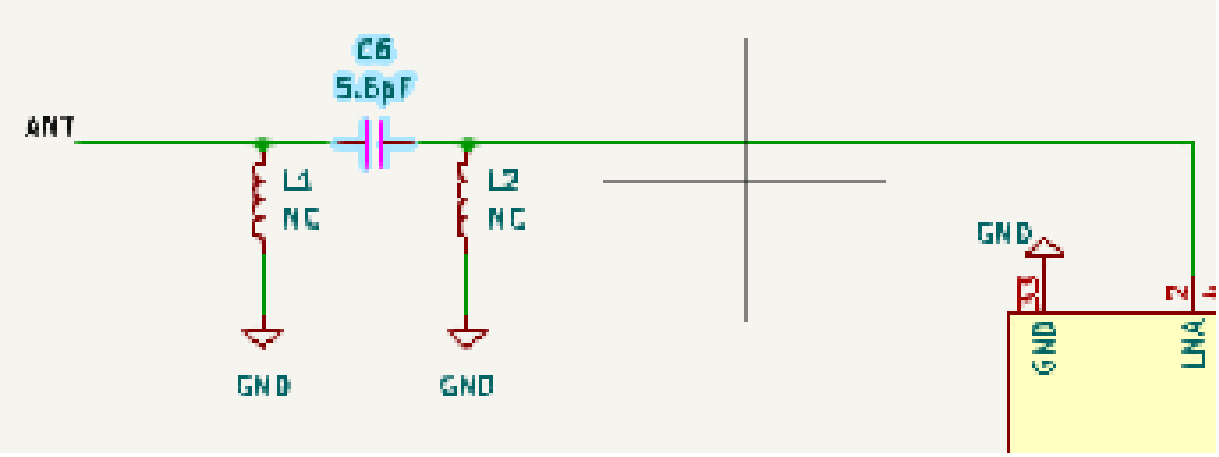
i) Thermal noise generated from ohmic resistance
ii) The noise received from external sources (anybody with Temperature greater then 0K radiates noise energy). This is known as noise temperature.

$T_A = \frac{V^2}{4kRB}$ where T_A = noise temeperature

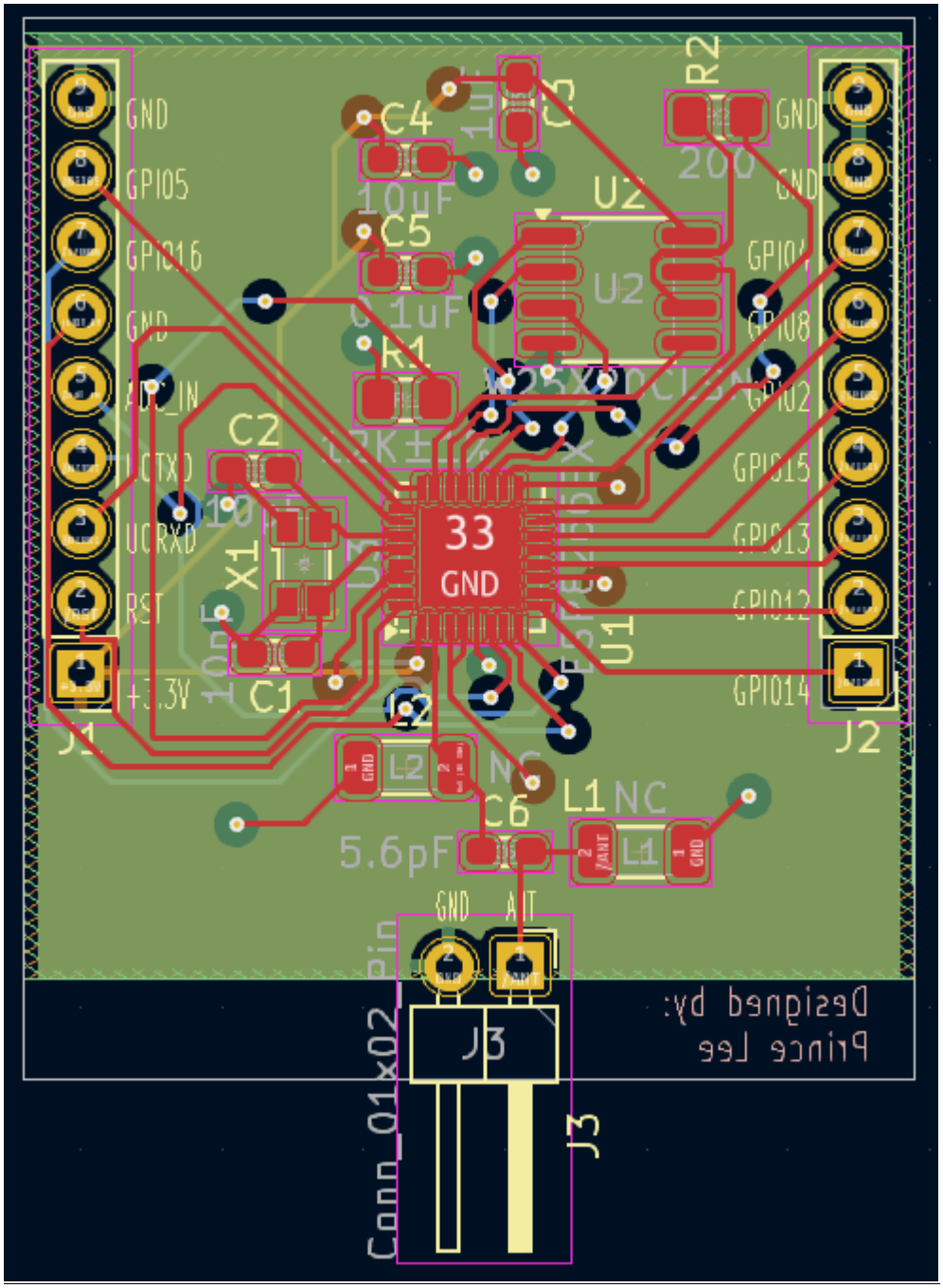
V = noise voltage

R = resistance of the antenna

B = Bandwidth



Routing

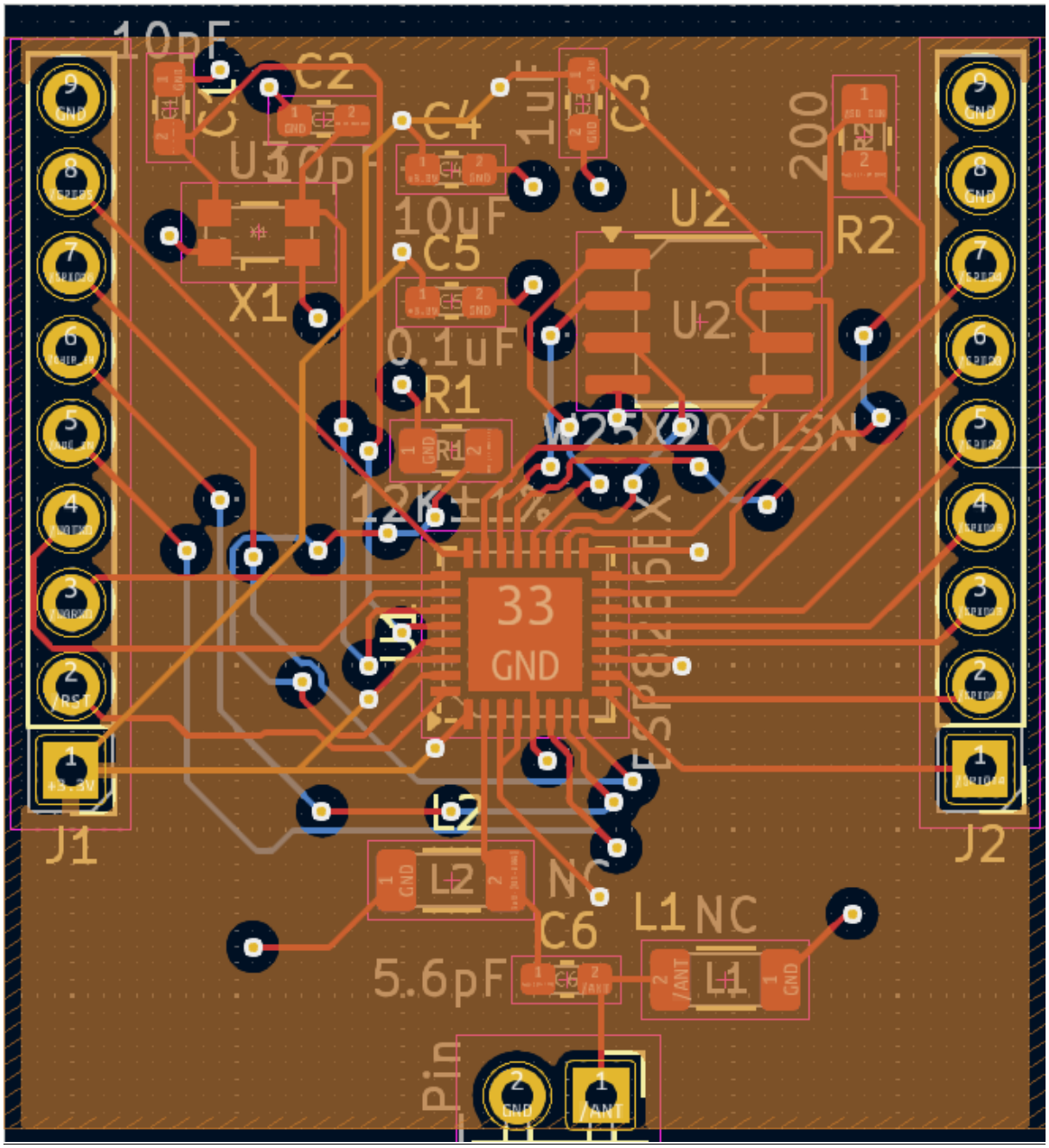


This is a four layer board. The layers details are as follows:

1. First layer: signal lines and components are placed here
2. Second layer: GND layer and no signal lines are placed here. Vias are used to connect GND signals in other layers.
3. Third layer: Pwr layer. Vias also used to connect to power signals
4. Bottom layer: Used for signal lines only.

Power Supply

Power lines should be placed on the third layer. When the power lines reached the pins of the chipset, VIAs are needed so that the power lines can go through the layers to connect the pins of the chipset on the TOP layer

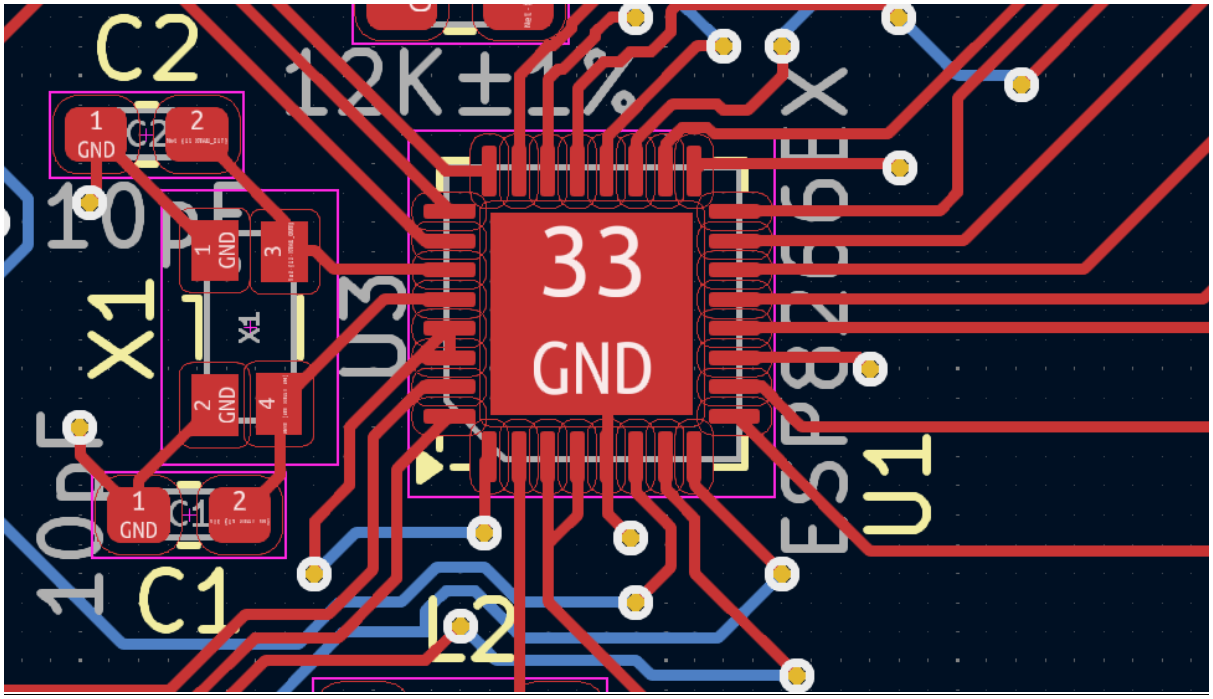


Crystal Oscillator

Crystal oscillator should be placed adjacent to the XTAL Pins, the connection lines shouldn't be too long, and should be wrapped up for shelter.

The input and output lines cannot be punched, cannot cross the layers or be crossed. The input and output bypass capacitor should be located near the chip; never set it on the lines.

No high frequency digital signal lines shall be placed under the four layers of the crystal oscillators. The best choice is that no signal lines is placed under the crystal oscillator. The TOP layer where is crystal oscillator is placed should be as large as possible.



RF section

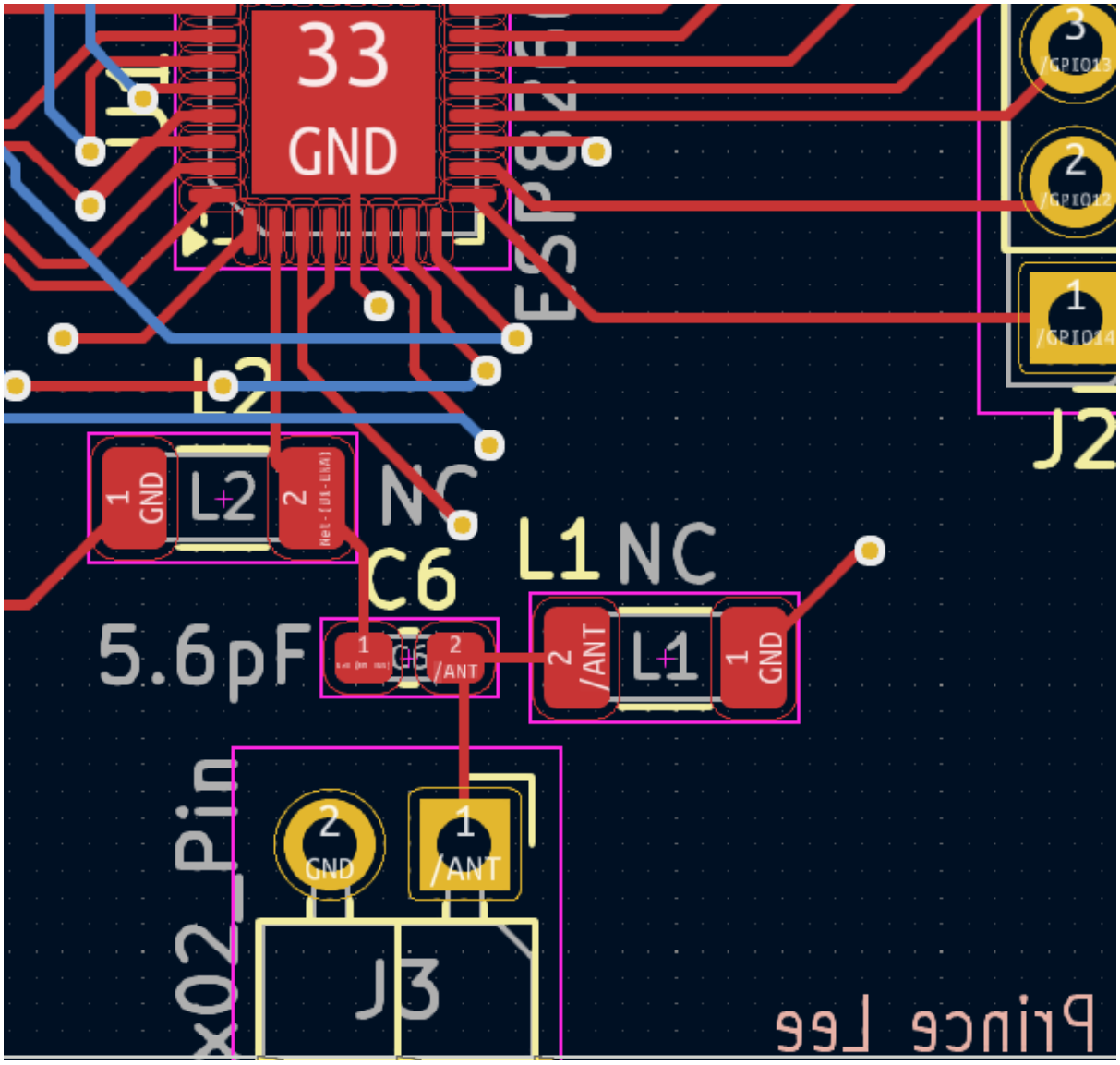
RF lines connecting the chip and antenna should not cover drills.

RF antenna should be set away from high frequency transmitting devices, such as crystal oscillators.

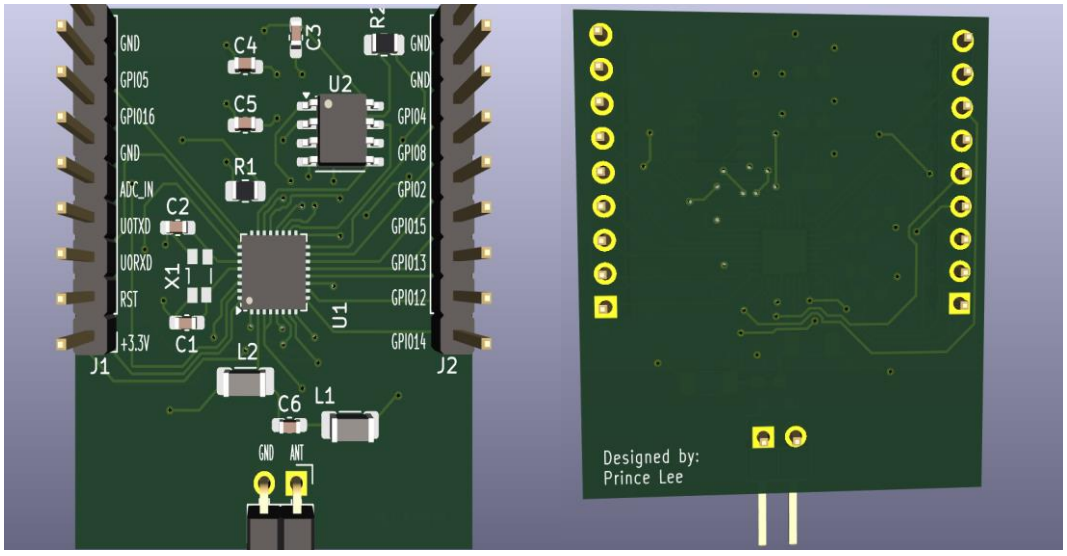
RF lines should not be set at a 45 degree angle. (any sudden change in direction can create impedance mismatches and cause signal reflection.)

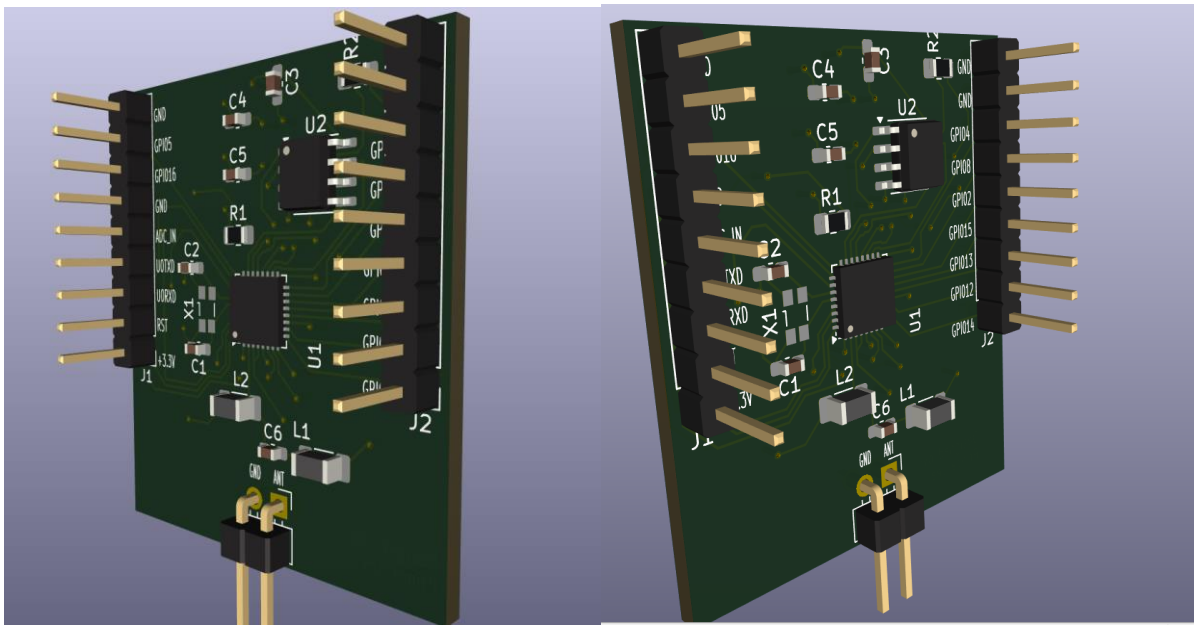
RF lines width should not be less than 6 mil.

No signal lines of high frequency should be set near RF lines. (incl. clock lines, crystal oscillator operates at 26MHz, clk signal lines etc)


33
GND
L2
GND
NC
C6
5.6pF
L1 NC
/ANT
GND
J3
J2
Prince Lee

3D view


GND
GPIO5
GPIO16
GND
ADC_IN
U0TXD
U0RXD
RST
+3.3V
J1
C4
C3
C5
U2
R1
C2
X1
U1
C1
L2
C6
L1
GND
ANT
J2
GPIO4
GPIO8
GPIO2
GPIO15
GPIO13
GPIO12
GPIO14
Designed by:
Prince Lee


C4
C3
U2
C5
R1
C2
X1
C1
U1
L2
C6
L1
J1
J2
GND
GPIO5
GPIO16
ADC_IN
U0TXD
U0RXD
RST
+3.3V
GND
ANT
C4
C3
U2
C5
R1
C1
L2
L1
GND
GPIO4
GPIO8
GPIO2
GPIO15
GPIO13
GPIO12
GPIO14
J2
GND
ANT