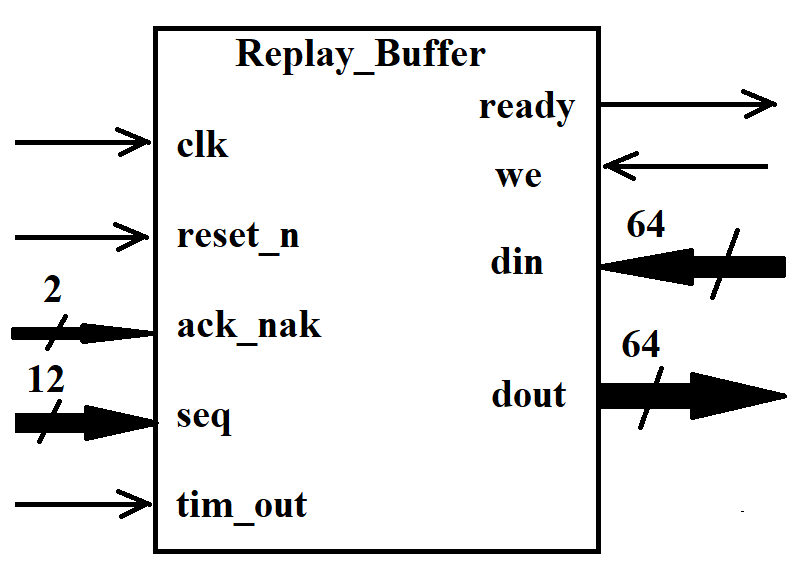
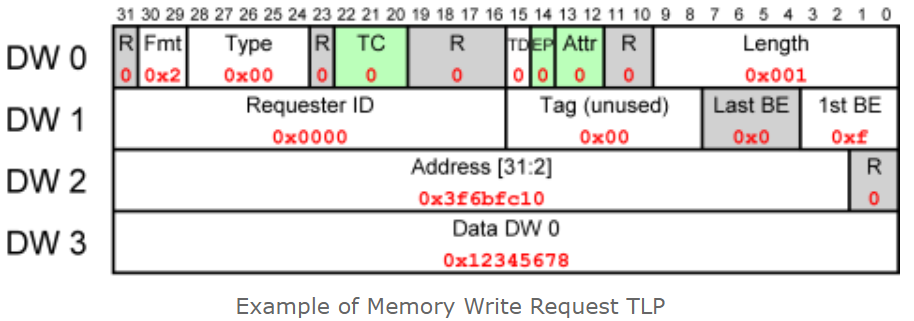
Design an 8kB (1024x64 bits) replay buffer used inside the PCIe transaction layer which runs at clock frequency of 250 MHz with 64-bit data bus width.

The diagram of the replay buffer is shown below:



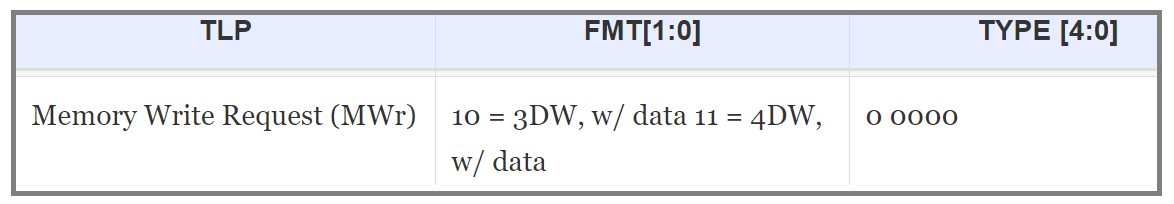
|  |  |  |
| --- | --- | --- |
| Names | Ports | Description |
| clk | input | 250 MHz clock |
| reset\_n | input | Synchronous low active reset |
| ack\_nak | 2-bit input | 00: ACK/NAK DLLP are not received  01: ACK DLLP is received  10: NAK DLLP is received |
| seq | 12-bit input | 12-bit sequence number received with the ACK/NAK DLLP |
| tim\_out` | 1-bit input | 1: the replay timer timeout occurs  0: the replay timer does not have timeout |
| ready | 1-bit output | 1: The replay buffer can accept new TLP packets from the transaction layer  0: The replay buffer can not accept new TLP packets from the transaction layer |
| we | 1-bit  Input | 1: new TLP packets including sequence number and LCRC information can be copied into  the replay buffer.  0: writing is not allowed. |
| din | 64-bit input | 64-bit input data bus |
| dout | 64-bit output | 64-bit data sent out from the replay buffer for transmission to the receiver |

1). Example of Memory Write Request TLP



Suppose that the CPU wrote the value 0x12345678 to the physical address 0xfdaff040 using 32-bit addressing. The packet could then consist of four 32-bit words (4 DWs, Double Words) as follows:

So the packet was transmitted as 0x40000001, 0x0000000f, 0xfdaff040, 0x12345678.



The TD bit is zero, indicating that there is no extra CRC on the TLP data (TLP Digest).

The Length field has the value 0x001, indicating that this TLP has one DW (32-bit word) of data.

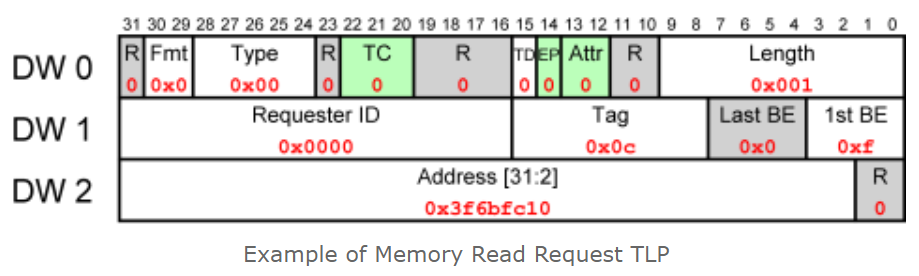
The Requester ID field says that the sender of this packet is known by having ID zero — it’s the Root Complex (the PCIe port closest to the CPU).

The 1st BE field (1st Double-Word Byte Enable) allows to choose which of the four bytes in the first data DW are valid, and should be written. Set as 0xf in our case, it marks that all four bytes are written to.

The Last BE field must be zero when Length is unity, since the first DW and the last is the same one.

The Address field is simply the address to which the first data DW is written. Well, bits 31-2 of this address. Note that the two LSBs of DW 2 in the TLP are zero, so DW 2 actually reads the write address itself. Multiply 0x3f6bfc10 by four, and you get 0xfdaff040.

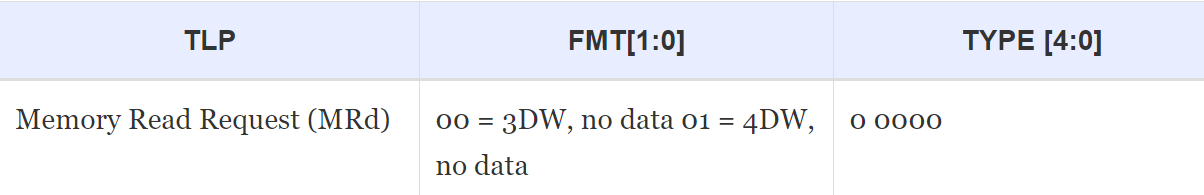
2).  Example of Memory Read Request TLP:



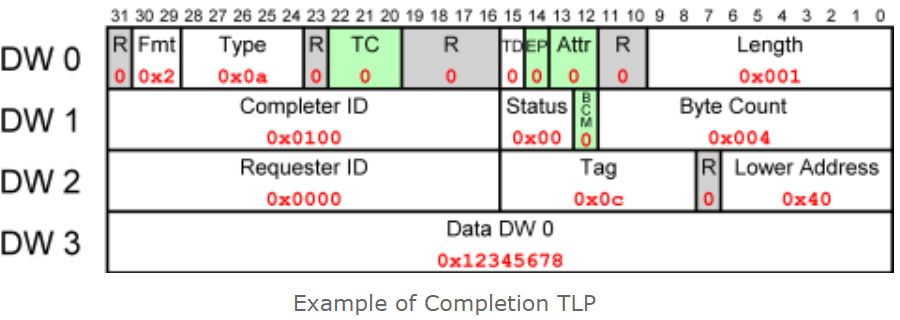
So this packet consists of the 3 DWs 0x00000001, 0x00000c0f, 0xfdaff040. It tells the peripheral to read one full DW at address 0xfdaff040, and to return the result to the bus entity whose ID is 0x0000.

0xFDAFF040   = “11111101101011111111000001000000”

0x3f6bfc10     = “111111011010111111110000010000”



3). Example of Completion TLP.



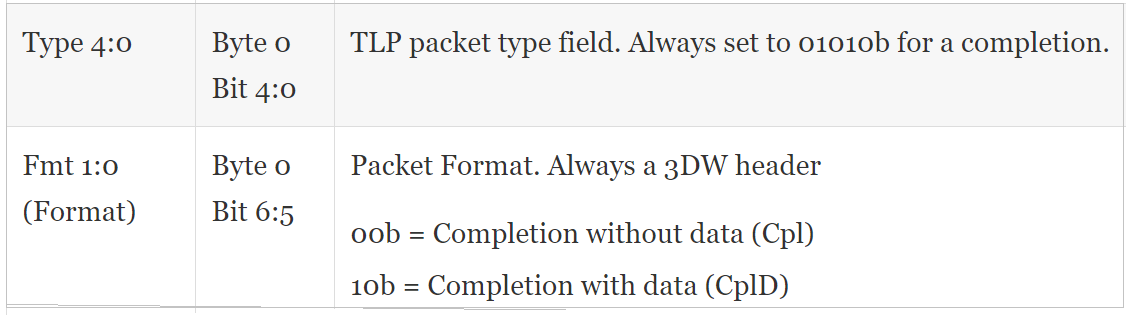
So the TLP consists of 0x4a000001, 0x01000004, 0x00000c00, 0x12345678. The packets basically says “tell bus entity 0x0000 that the answer to its Request to entity 0x0100, which was tagged 0x0c, is 0x12345678.”

The Length field has the value 0x001, indicating that this TLP has one DW (32-bit word) of data.

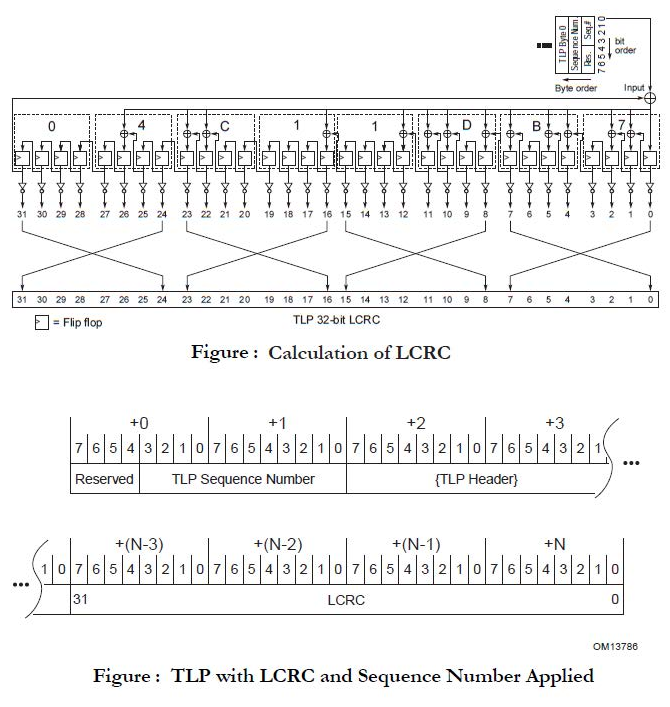
The BCM field is always zero when a packet does not origin from a bridge with PCI-X.

The Status field is zero, indicating that the Completion was successful.

Lower Address field is the 7 least significant bits of the address, from which the first byte in this TLP was read. It’s 0x40 in this case, coming from the lower bits of 0xfdaff040. This field can be useful with multiple TLP completions.



PCIe 32-bit LCRC Diagram:



In your final project report, you need to show

1. Manually created TLP Packets.
2. Verilog design of LCRC and testbench simulation to show the created LCRC bits for each TLP packet.
3. Replay buffer Verilog design and testbench.

You can use Synopsys VCS or Xilinx ISE simulation tool.

You can also use Altera tool for this project.