D2AFE: Implementing A Pilot Tone Injection Scheme for Diamond 2 .

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1 Introduction

The Diamond 2 CDR [1] states that a new μTCA based Fast Orbit Feed-Back (FOFB) power supply architecture will be developed using a centralised computation node and a 24 channel distributed fibre communications network.There will be 252 BPMs around the ring and the system is aimed at achieving a unity gain bandwidth of 1kHz compared to 140Hz for Diamond-1. In order to service demands for turn by turn data and high Fast Acquisition data rates, for the higher bandwidth, the CDR recommends adopting a low noise (less than 20dB noise figure) analogue front end located in the tunnel with pilot tone injection using frequencies around 1MHz from the bunch frequency. The Sampling ADC would be located in the CIA within a μTCA FMC card. Cabling loss between the AFE and the ADC is expected to be up to 6dB. This report details the design of the analogue front end for diamond-2 (D2AFE).

A block diagram of the Diamond-2 Orbit Feedback system is shown in figure 1. The 4 BPM signals are passed to the AFE where a pilot tone is added and the signals are filtered and amplified/attenuated to match the ADC input. They are then passed on coax cables up to the Cell μTCA processor. Processed samples are then pushed to the core μTCA processor where the corector currents are computed and distributed to all cells. Up to 12 BOMs per cell and 24 cells are supported on the double star topology. The internal block diagram for the AFE is shown in figure 2. The 4 inputs from a BPM are low pass filtered, combined with a pilot signal, bandpass filtered and amplified and then filtered further to remove out of band noise. The outputs are monitored with a log detector for diagnostics. The attenuators can be controlled remotely over a multidrop RS485 bus which also provides monitoring of RF output level and channel temperature.

2 Radiation Assessment

As the AFEs are to be located in the storage ring tunnel it is important to understand the ionizing radiation environment. Reported radiation effects on Flash memory based devices [2] indicated typical failure at around 20krads total dose and no significant change in parametric measurements below 5krad. General analogue electronics will withstand 10-20 krad before significant parametric changes.

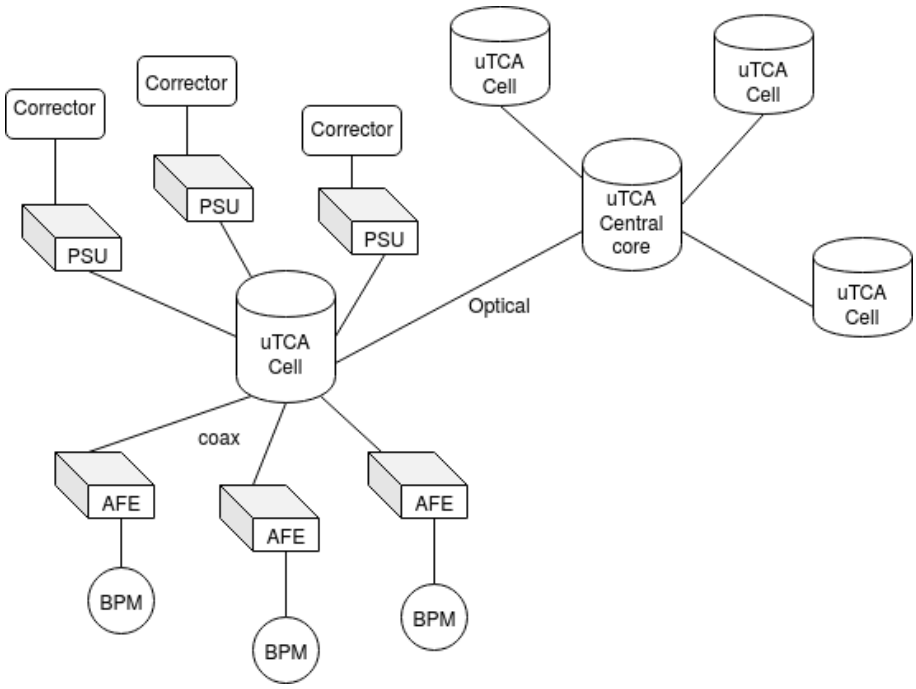

Figure 1: Diamond-2 Orbit Feedback System

Radiation tests have been carried out [3] in high loss locations within Diamond-1 and indicate an upper limit for radiation dose of 176 rads/yr or less than 2.6krads over a 15 year operating life. The AFEs will be located in lower radiation zones close to ground level so should see much less than 5krads over the operating life of Diamond-2.

3 Power and Remote Management

The AFE requires DC power for the RF amplifiers and controllable attenuators plus the microcontroller used to manage the attenuators. The Cell processor needs to be able to communicate with the AFE microcontroller to manage the attenuators and collect diagnostic data. One solution considered was to have an Ethernet MAC in the AFE and provide power using Power over Ethernet. The drawback with this solution was the need for digital clocks at 125MHz (4th harmonic would be inband) to support Ethernet and the need for switching converters to extract DC from the Ethernet inputs.

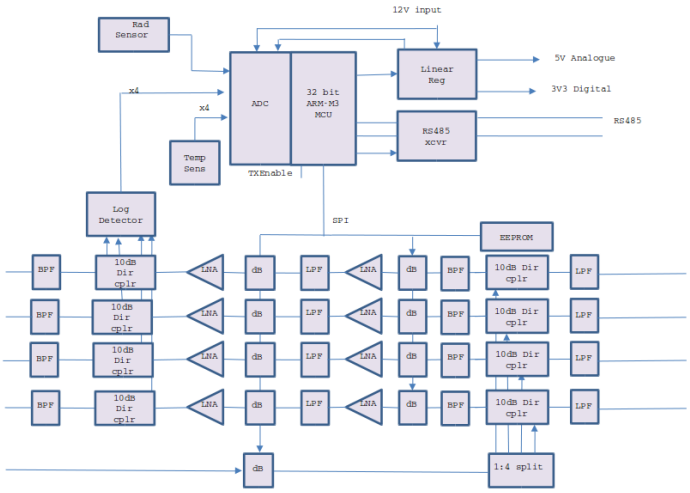

Figure 2: AFE Block Diagram

Both of these could compromise the low noise performance of the AFE so PoE was rejected in favour of a seperate DC power feed from the CIA and linear regulation in the AFE. Remote communications would use a multidrop RS485 bus running at 115.2kBaud which can support up to 1200m UTP cable spans and would be daisy chained along all of the AFEs in the cell. Each RS485 node would terminate on a 32 bit ARM Cortex-M3 microcontroller that would manage the AFE functions. The RS485 address and the optional bus termination can be set on each AFE using an 8 way DIP switch on the PCB. An optional fast RF trip mode can be enabled by the DIP switch that will force all attenuators to latch in high loss mode if the output RF Voltage exceeds 4Vpp for more than 500nsec. A purely analogue mode can also be selected via the DIP switch that sets the attenuators from data stored in EEPROM on power up, enables the RF amplifiers and then places the microcontroller in SLEEP mode disabling all digital clocks.In analogue mode there is no remote access.

The Power management system is shown in figure 3. The polyfuse is a resettable 24V 1.5A protection device with 1.5sec trip time for an 8A

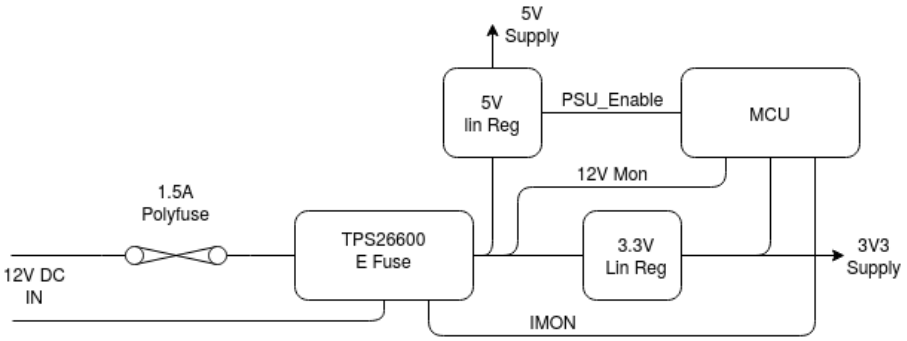

Figure 3: Power Management

Parameter	Value
Baudrate	115.2kBaud
No of bits	8
Parity	no
stop bits	1

Table 1: Serial Port parameters

fault current. It will trip at 3A and hold the maximum current at 1.5A once tripped. It is intended to protect the DC wiring from excessive fault currents. The TPS26600 Efuse is an active protection device which provides -60V reverse polarity blocking, +5.5V under voltage lockout, +15V to + 60V over voltage lockout with 6μsec response ,1.5A current limiting and 1.7Volts/Amp current monitoring.

The output of the Efuse is passed to a linear regulator to provide a 3.3V +/-1% 100mA digital supply rail primarily to power the MCU which can then enable the higher power 5V regulator to power the RF elements of the board.

Once the power initialization is complete the MCU downloads operating parameters from an on board EEPROM via SPI, and enables a 115.2 kBaud UART interface as per table 2 to start an RS485 slave at a 4 bit address determined by a DIP switch on the PCB.The RS485 bus can be resistively terminated via one of the DIP switch contacts or daisy chained to the next AFE in the cell. If the DIP switch address is set to 0 the analogue mode is selected and the processor placed in SLEEP once the RF channels are set up.

A custom half duplex RS485 pinout for the RJ45 connectors (A+ to pin 6, B- to pin 3) has been chosen to ensure that one of the twisted pairs within a standard Ethernet cable can be used whilst guarding against accidental connection of a Power over Ethernet source to the connected cables. Further protection against PoE is provided by a resistive network to ensure that PoE fails the detection test and will hence not connect the 48V power. Accidental connection of 10,100 or 1000 base T Ethernet will not cause any damage. Note that the commonly used Moxa terminal servers allocate wires from different twisted pairs (pins 4 and 6) in their pinout convention so is likely to have EMI issues and degraded performance over long cables. If connecting to a Moxa terminal server a cross connect will be needed. Operation of 115.2kbaud RS485 using the chosen pinouts and twisted pair configuration has been tested over 900m of CAT6 UTP with no issues. The comms elements are shown in figure 4.

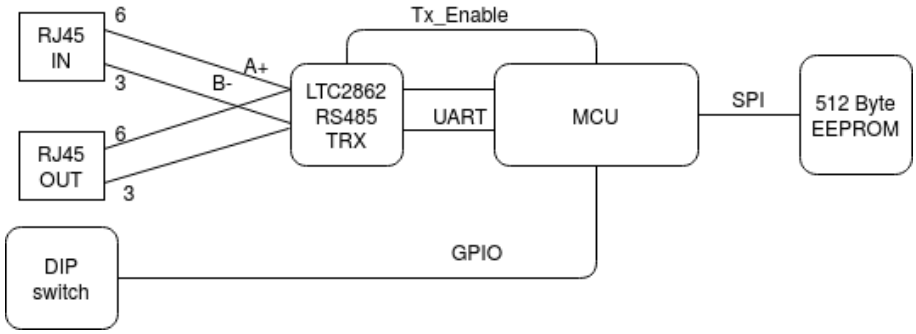

Figure 4: RS485 Communications Interface

4 Micro Controller Unit

An STM32 implementation of the Arm Cortex M3 microcontroller was chosen as it is widely available at low cost and can be programmed with gcc compiler and debug tools that are freely available. In order to accomodate 14 ADC channels and adequate Flash memory the STM32F103RBTX processor was chosen. It uses an 8MHz external crystal that is multiplied up to yield a 78 MHz internal clock. The configuration of the available MCU peripherals is shown in figure 5

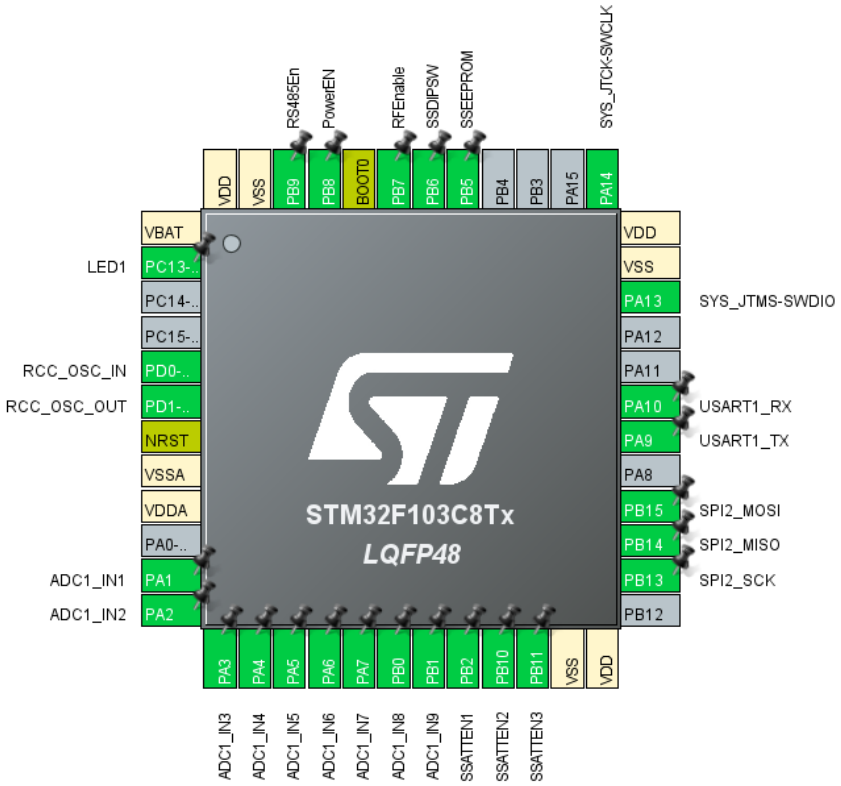

Figure 5: MCU Configuration

5 EEPROM

An M95040 4Million write cycle 1kbit serial EEPROM is available on the PCB. It is accessed via SPI and is also connected to the J7 header to allow direct write independant of the MCU. This would enable data entry at manufacture if required. The memory is aranged in 32 pages of 16 bytes. A page write cycle takes 5msec to complete. The pages are allocated as per table 2

6 RF Channels

The RF section contains a 1:4 splitter to distribute the pilot signal and 4 identical band pass amplified channels carrying the BPM signals and injected pilot as shown in figure 6.

Page	Contents	Page	Contents
0	ch 1,2 Temperature cal	16	spare
1	ch 3,4 Temperature cal	17	spare
2	ch 1,2 RF cal	18	spare
3	ch 3,4 RF cal	19	spare
4	Rad sense and 12V Mon cal	20	spare
5	5V Mon and current cal	21	spare
6	MCU temp and 3V mon cal	22	spare
7	Equipment ID string	23	spare
8	Cal ID string	24	spare
9	Attenuator settings	25	spare
10	spare	26	spare
11	spare	27	spare
12	spare	28	spare
13	spare	29	spare
14	spare	30	spare
15	spare	31	spare

Table 2: EEPROM Pages

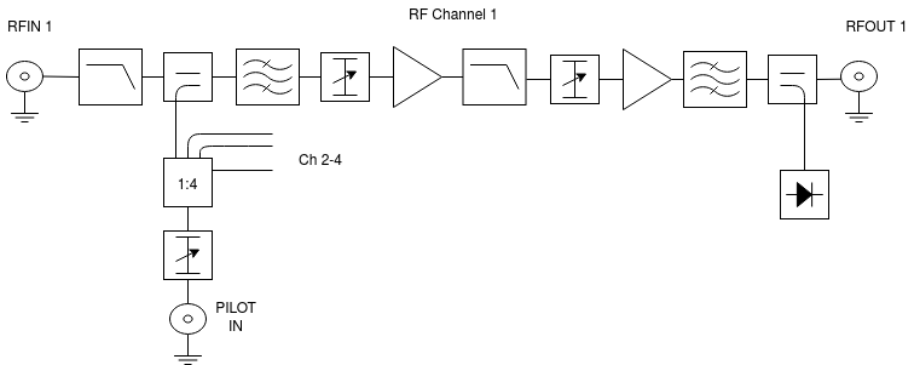

Figure 6: RF Channels

The RF input is low pass filtered by a Johanson 0500LP15A500 surface mount ceramic low pass filter. This device has a 2W input power rating, a 3dB bandwidth of 700MHz insertion loss of 0.7dB at 500MHz and >30dB rejection at all harmonics of 500MHz to at least 5GHz.It removes the broadband high energy spikes from the raw BPM input. After low pass filtering a minicircuits ADC-10-4 surface mount directional coupler is used to insert the pilot tone.This has a forward loss of 0.9dB,11dB coupling loss and 25dB directivity at 500MHz. Following the directional coupler is a Temwell TT67553F-500M helical band pass filter with a 15MHz passband and 2.1dB midband insertion loss. After the band pass filter is an IDT F1953 digital step attenuator with 1.2dB minimum insertion loss at 500MHz. The minimum loss upstream of the first RF amplifier is hence $0.7dB + 0.9dB + 2.1dB + 1.2dB = 4.9dB$. The amplifier is a Qorvo TQP3M9036 GaAs pHEMT 22.5dB gain 0.38dB noise figure low noise amplifier. The lowest achievable noise figure is hence approximately 6dB. A second low pass filter is used to supress out of band noise and prevent down stream intermodulation in the second amplifier. An identical attenuator + amplifier combination forms a 2nd gain stage and is followed by a 2nd bandpass filter to remove spurious signals that might be aliased back into band in the direct digital downconversion following the ADC. An output directional coupler and logarithmic detector are used to provide a diagnostic measure of the mean RF output power. The amplifier output 1dB compression is at +20dBm so the likely maximum AFE output power is +17dBm which could generate 4.5Vpp into the ADC when output cable losses are neglected or 2.25Vpp after 6dB cable losses.

7 Monitoring the RF Channels

Each RF channel has an LM45 temperature sensor located close to the 2nd low noise amplifier and connected to an ADC channel on the MCU. This has an absolute temperature accuracy of +/-2C near 25C and a 10mV/C linear temperature slope offset by 250mV at 25C. Combined with the 12 bit ADC in the MCU this provides +/-0.04 deg C resolution. Simple offset and slope calibration in the firmware can improve the accuracy and channel tracking.

The RF amplifiers are powered from an LT1764 5V 3 Amp linear regulator. The absolute accuracy +/-5% limited by +/-3.5% voltage reference and +/-1.5% due to the feedback resistors. The 5V output is monitored and fed back to the MCU via a potential divider with +/-2% accuracy including the reference variation.

The 12V input to the regulators is also monitored via a potential divider and ADC channelto an accuracy of +/-6%.

The RF amps have typical gain temperature dependance of 0.004dB/deg C. The RF attenuators 0.003dB/deg C. There is no information on the LPF temperature dependance so assuming full spec variation over 25C to 85C then the upper bound is 0.012dB/deg C. The directional coupler also has no temperature data so under the same assumption yields 0.015dB/deg C.likewise for the helical filters at 0.033dB/deg C. On a root sum of squares basis the expected variation in RF gain over temperature is 0.03dB/deg C. Under worst case linear addition that could rise to 0.082dB/deg C.

The pilot only temperature dependance is one attenuator + one 1:4 splitter estimated as 0.021 dB/deg C. That may need to be calibrated as changes will directly degrade pilot tone operation. It might be worth considering an additional temperature monitor for the pilot channel in future versions.

The total ionizing radiation dose is monitord using a p channel mosfet biassed for constant current and monitoring for changes in gate threshold voltage. This needs to be calibrated.

The RF output power is monitored using a directional coupler with nominally 11dB coupling loss and an AD8307 logarithmic detector. At least 67dB dynamic range at 500MHz from +17dBm (RF amps in compression) to -50 dBm output is available, with +/-1dB linearity, via a linear in dB voltage signal to an ADC channel. The output response time is 400nsec allowing it to be used for fast signal overload trip.

A fast RF trip facility is provided that detects an RF overvoltage at the outputs using the AD8307 outputs, TLV3202 high speed comparators and a

ADC Channel	Signal
1	Ch1 Temperature
2	Ch2 Temperature
3	Ch3 Temperature
4	Ch4 Temperature
5	Ch1 RF Output
6	Ch2 RF Output
7	Ch3 RF Output
8	Ch4 RF Output
9	Rad Sensor
10	12V Monitor
11	5V Monitor
12	Current Monitor
16	MCU Temperature
17	3V3 monitor

Table 3: ADC Channels

2.5v bandgap reference. A 4 channel set reset flip flop is implemented with discrete 74VHC132M gates (3.9nsec propagation delay per gate) followed by a 74LVC2G125 line driver to pull the attenuator MODE pin low on all attenuators. The parallel inputs are set to operate at maximum attenuation in this mode. From a step overvoltage on the RF outputs to the attenuators settling at max attenuation is approximately 500nsec. The SR flip flop can be reset by disabling the RF amplifiers and re-enabling them using an RS485 command. The threshold for the trip circuit is set in hardware as 4Vpp output. The ooutput from the line driver is passed through a pair of DIP switch contacts to allow it to be disabled if not required.

The available analogue diagnostic signals are shown in table 3.

8 Mechanical

The PCB will be a 240mm x 170mm 6 layer board mounted on the girder with a heatsink to air. The girder is not being used for a thermal path as carbon fibre girders are under consideration for Diamond 2. The conceptual view of the mechanics can be seen in figure 7.

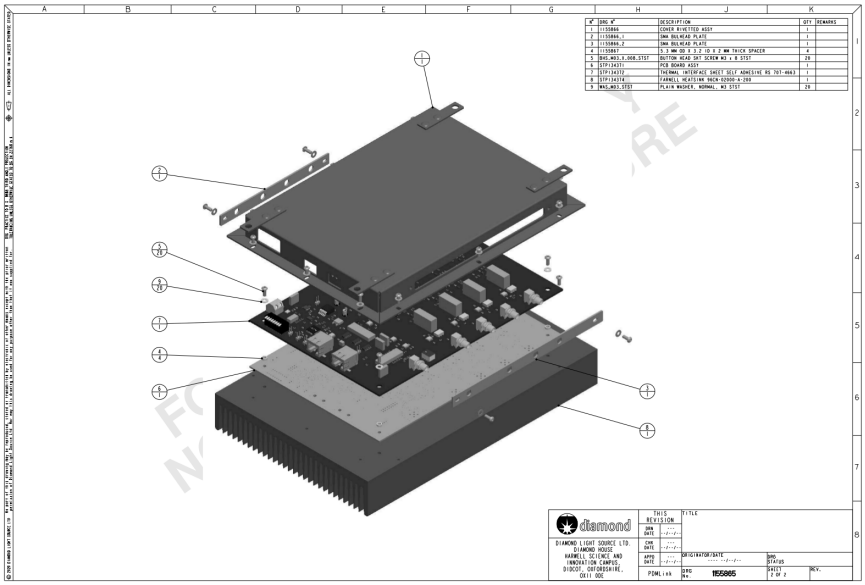

Figure 7: Mechanical Design Concept (Source:Ljubo Zaja)

9 Firmware Architecture

The embedded control firmware for the PCB is written in C using the gcc based STM32Cube IDE, STM32 HAL framework and the STM32CUBE configuration tool to set up the hardware interfaces. The final executable image is generated in intel .hex format and can be uploaded using a number of Flash programming tools although the STM32CUBE programmer and ST/link hardware is the preferred route.

The firmware implements a simple command-response protocol as shown in figure 8. On reset the initial vector table is set up using assembler which then calls the C main function. The Hardware Abstraction Layer (HAL) is then initialized to enable calls to the ST library of hardware interfaces rather than direct register IO. All hardware interfaces are then initialized (code autogenerated by the STMCUBE tool). Following this the endless loop of (1) poll all ADC channels then (2) check for RS485 command and execute is run.

An interupt driven UART interface collects incoming characters from the RS485 link and enters them in a circular input buffer. If a valid termination

character ($CR0x0D$) is received then the $inbuf.cmd\_available$ flag is set to 1 and the $inbuf.cmd\_string$ holds the buffer location of the command. If there are unsent characters in the output buffer the RS485 transmitter is enabled and the character is loaded into the UART for transmission.

The Parse and Execute blocks are implemented in the Command Line Interpreter CLI.c source file. The available commands in the syntax
$< node >< command >< param1 >< param2 >< param3 >< CR >$
are shown in table 4. The Node ID XX must be between 00 and 16 with 00 being the broadcast address to all nodes.Delimiters are spaces and the number of parameters is variable depending upon the command.

The initial prototype firmware load used 47KB of Flash and 11KB of RAM which is approximately 37% of the available resources on the chosen MCU.

10 Using the AFE for Pilot Distribution

A high level pilot signal (+8dBm) must be provided to each AFE. This can be generated using a further AFE as a pilot distributor. Refering to figure 6 if the RF inputs are terminated and a low level (0dBm) pilot applied to the pilot input the RF outputs can produce in excess of +16dBm. using 4 passive 1:4 splitters these can produce 16 x +10dBm pilots for a complete cell from a single reference input.

Node	Command	param1	param2	param3	Note
XX	help				print a command list
XX	reset				software reset
XX	ver				print version and compile date
XX	status				print human readable status information
XX	atten	ch#	1 or 2	attendB	set attenuation
XX	mode	1,2 or 3			set operating mode
XX	rfon				enable the RF amplifiers
XX	rfoff				disable the RF amplifiers
XX	vcc5on				enable the 5V to RF amplifiers
XX	vcc5off				disable the 5V to RF amplifiers
XX	ack				return an ack string
XX	eid				return the equipment ID string
XX	calid				return the calibration ID string
XX	caldata	offset	value1	value2	upload a cal data pair
XX	savecal				save the current cal set to EEPROM
XX	loadcal				load the cal set from EEPROM
XX	mkeid				enter device id string
XX	mkcalid				enter cal id string
XX	defcal				load the default cal set
XX	ping				poll device and return EID string
XX	mon				return the machine readable status string

Table 4: RS485 Commands

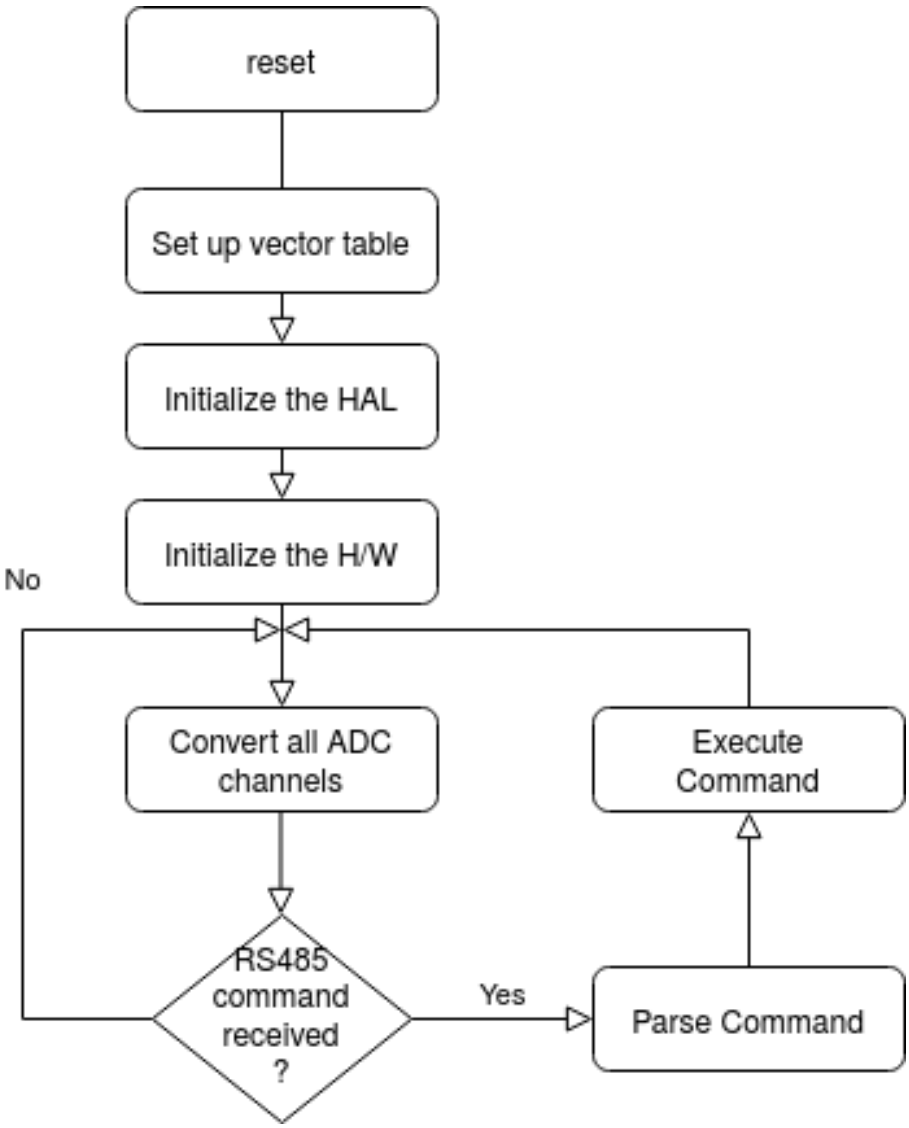

Figure 8: Main programme

References

[1] Diamond, "Diamond-2 conceptual design report,"

[2] D. N. Nguyen, "Radiation effects on advanced flash memories," *IEEE Transactions on Nuclear Science, 46 (6), 1744 (1999).*

[3] A. Morgan, “radiation testing in diamond-1,”