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- Veröffentlichung von Inhalten nur nach Freigabe

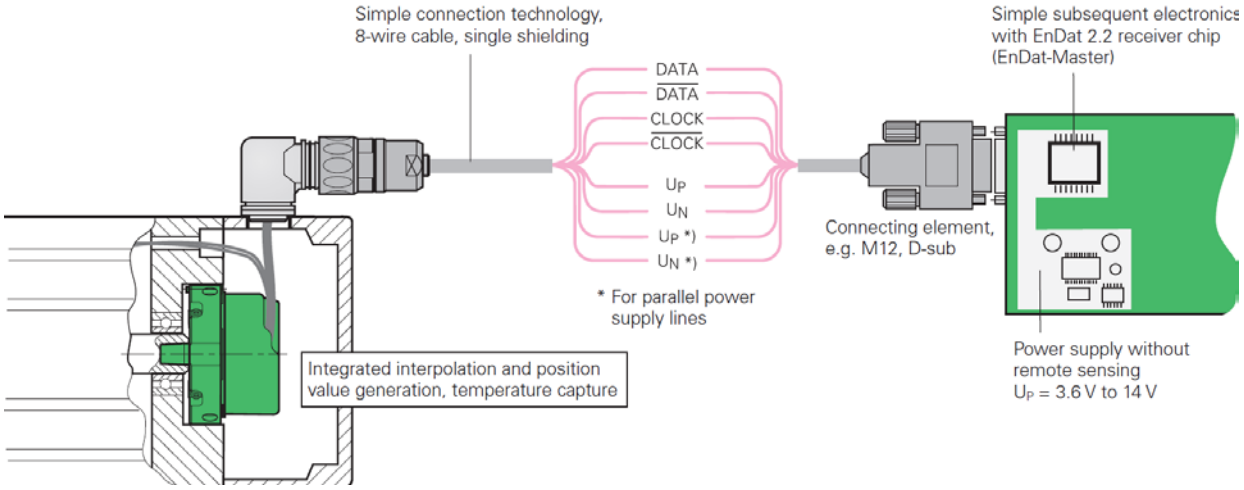
EnDat Master

- Introduction
- EnDat Master FPGA Versions
- Functional Safety
- EnDat Master in the Microcontroller
- EnDat Master from other Manufacturers
- CRC Calculation for Microcontroller-Based Solutions

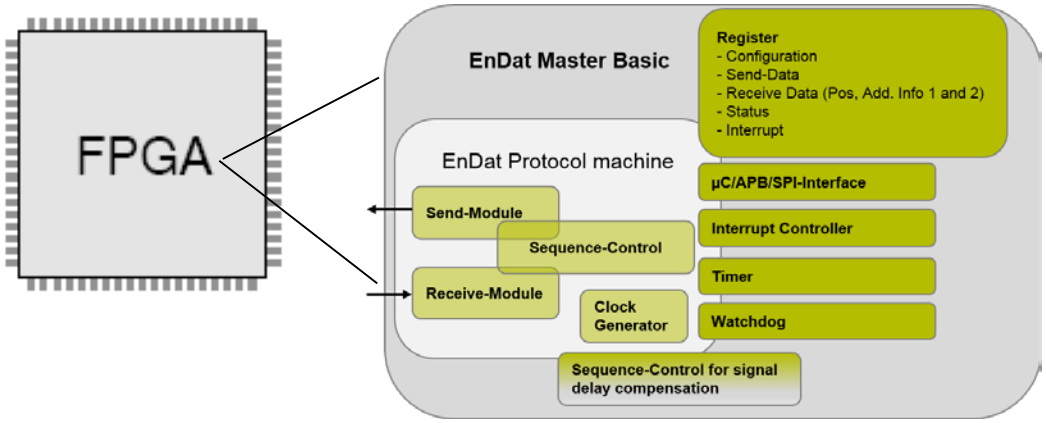
Further information see at
www.heidenhain.de → Documentation → Fundamentals→ Interfaces→ EnDat 2.2

EnDat Master

- The EnDat Master handles the communication with EnDat encoders from HEIDENHAIN. This simplifies the transmission of position data and additional data to the higher-level application. The EnDat Master can be integrated via either a microcontroller or an FPGA (Field Programmable Gate Array) or ASIC.
- Solutions with a microcontroller are used when the desired clock frequencies are relatively low. HEIDENHAIN can provide a sample code for the implementation of EnDat 2.1 mode commands when integration in a microcontroller is planned. There are now also microcontroller-based solutions with integrated EnDat Master, such as from Texas Instruments, Renesas, or Hilscher.
- Integration in an FPGA or ASIC is usually chosen if high transmission frequencies with pure serial data transfer are the goal. Various versions are available for integration in an FPGA or ASIC.



EnDat Master –FPGA Versions–



- EnDat Master Safe
- EnDat Master Basic
- EnDat Master Reduced
  (EnDat Master Mini see separate slide)
- EnDat Master Light

EnDat Master “light” and “reduced” contain only the EnDat protocol machine and the sequential control for compensating the run time.

	EnDat 2.2 Master		EnDat 2.2 Master	
	“light”	**“reduced” (base for “Mini”)**	**“Basic”**	**“Safe”**
Logic counts	Approx. 160	Approx. 650	> 2100	> 6300
For use with	All EnDat 2.2 encoders: Linear, angle and rotary encoders with photoelectric, inductive and magnetic scanning			
	Only absolute encoders	Incremental and absolute encoders with battery back up		
Additional data 1 and 2	No	Yes		
Support for Functional Safety	No	See Functional Safety without EnDat Master Safe		Yes (pure serial)
Bus interface included	No		Yes	
Properties	VHDL example code (covers only part of the EnDat functions). Suitable for implementation in subsequent electronics to only limited extent	Only pure EnDat functionality (EnDat protocol machine) integrated. Advisable, e.g. for multi-channel applications. Code was tested in a sample application	Encapsulated code block (tested by HEIDENHAIN); designed for short “time-to-market” and simple operation	Master for functional safety applications (corresponds to Master Basic with expansions)

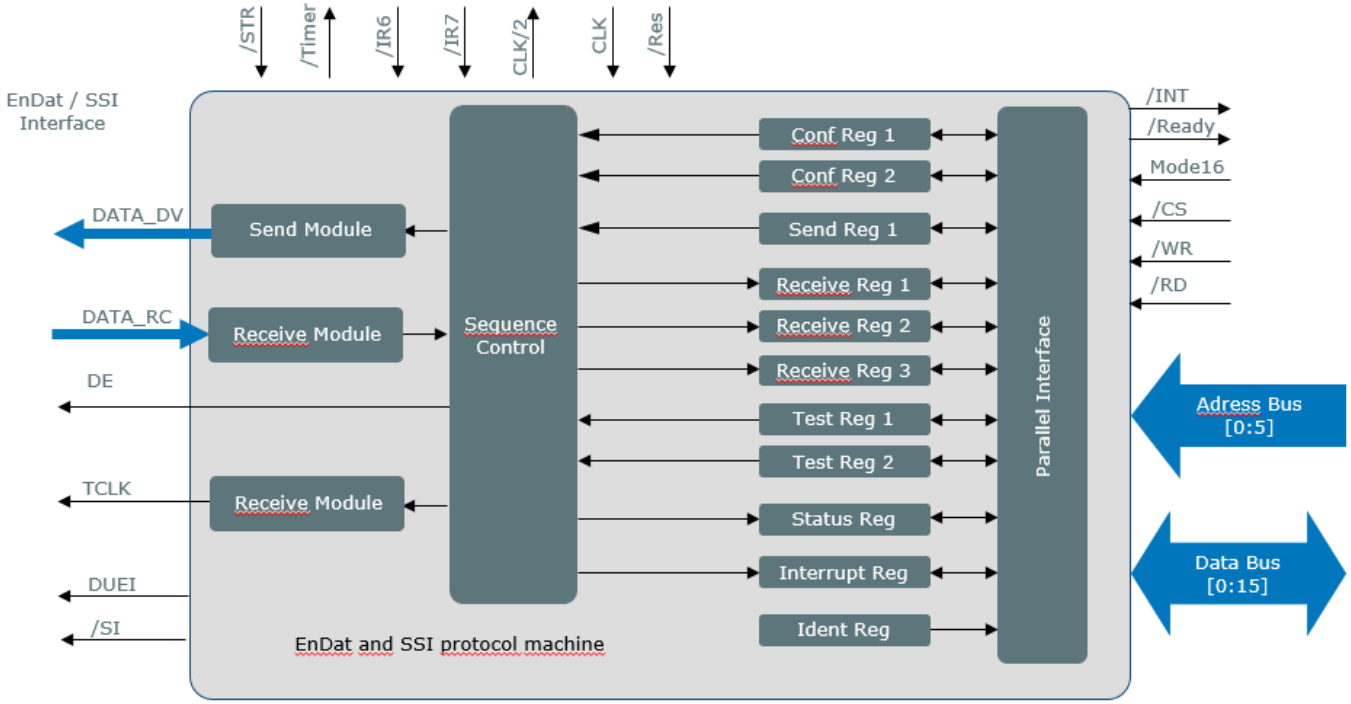
EnDat Master –FPGA Versions–

Design	EnDat Master Light	EnDat Master Reduced	EnDat Master Mini	EnDat Master Basic			EnDat Master Safety	
Interface output	No [5]	No [5]	SPI	8/16 bits (bidirectional)	32 bits (APB)	SPI	2 x 8/16 bits (bidirectional)	2 x 32 bits (APB)
Functionality	State Machine (EnDat 2.1) [1]	State Machine (EnDat 2.1) [1]	Master Reduced + Register interface + Control logic + SPI	Basic Functionality			Basic Functionality (incl. functional safety)	
Functional safety	No	Yes, see “Non-safe Master”; t_M measurement not included	Yes, see “Non-safe Master”; t_M measurement is included	Yes, see “Non-safe Master”; t_M measurement is included			Yes	
Combination with customer's own blocks	Yes	Yes	No	No	Yes	No	No	Yes
Resource consumption [3]	≈ 160	≈ 650	Lattice MachXO2	≈ 2435	≈ 2322	≈ 2548	≈ 6610	≈ 6260
Delay compensation	Synchronized to start bit+fixed waiting times	Synchronized to start bit+waiting time (based on measurement of propagation time)		Measurement of propagation time+compensation when loading data to shift register				
Scope of delivery **VHDL (source code/Verilog)** **Simulation environment** [2] **Documentation** **Netlists**	 Yes/No No Brief document. –	 Yes/Yes No Yes –	 Yes / No No Yes Lattice MachXO2	 Yes/No Yes Yes [4] Yes[6]	 No	 Yes[6]	 Yes/No Yes Yes [4] –	
ID	–	1244442	1279637	1244440			1244441	

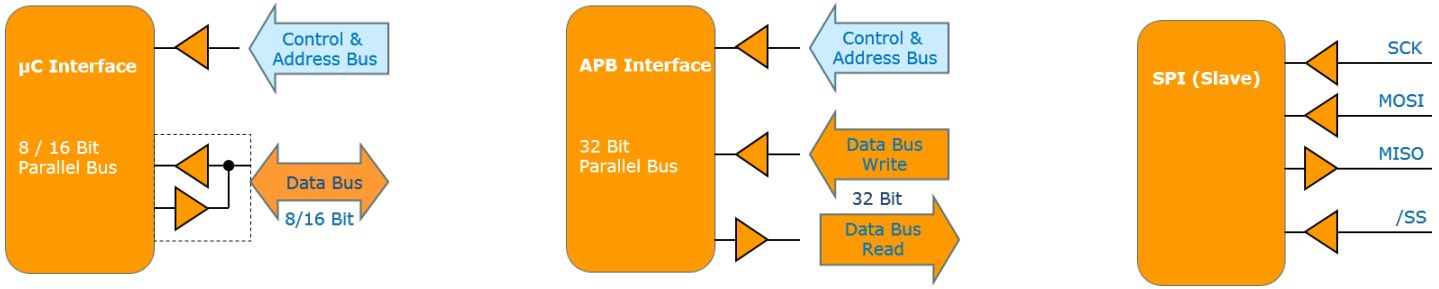
1) The customer himself must implement the microcontroller interface as well as the necessary registers (for the configuration of the EnDat master as well as outputting of the data)
2) Simulation environment consisting of simulation script, testbench, stimuli, and references
3) Estimated indication of the logic elements; Altera-based; data from reference implementation
4) Including software examples for commissioning
5) Internal signal interface (customer must implement the output interface and registers for configuration, sending and receiving data, etc.)
6) Intel (Altera): MAX10 and Xilinx: Spartan 6

EnDat Master FPGA –Registers & Interfaces–

- Basic register structure of EnDat Master (example with microcontroller interface)



- Principle block diagram of output interfaces



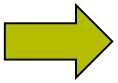
EnDat 2.2 Implementation

- Physical layer
  - RS-485 with clock and data ➔ 2x RS-485 transceiver required

- Application layer
  - Effort for application layer
    - Commissioning of Master and encoder (parameter handling)
    - Requesting data, such as: position, temperature, diagnostic data, …
    - Functional safety (black channel)

- EnDat Master: implementation with microcontroller
  - Advantage: Costs
  - Constraints
    - Usually only a restricted clock frequency can be realized with “standard microcontroller”
      ➔ Sufficient cycle time?
    - Delay compensation cannot be implemented or only to a limited degree
      ➔ EnDat 2.2 functionality cannot be implemented
      ➔ EMC behavior is influenced

- EnDat Master: Implementation with FPGA
  - Disadvantage: Costs
  - Advantage: EnDat 2.2 can be implemented without or only with minor restrictions

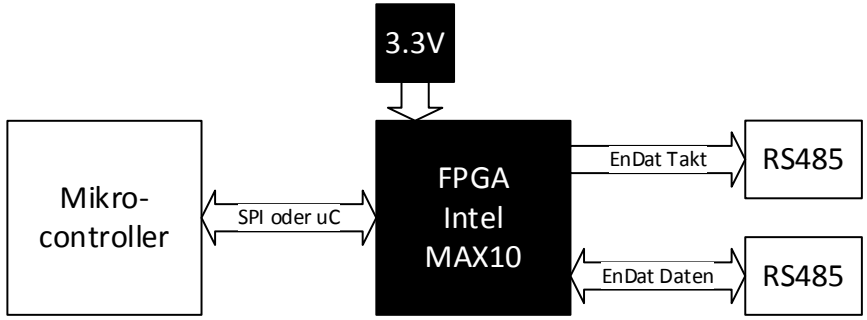


How can it be implemented economically?

EnDat Master FPGA –Low-cost FPGA–

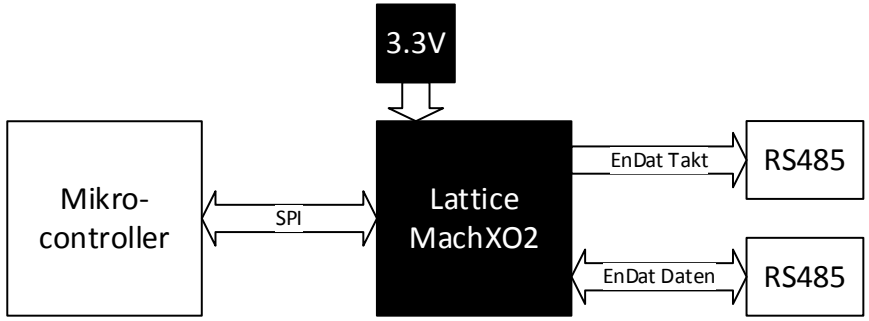
Implementation example EnDat Master Basic: Intel (formerly Altera) MAX10 as 10M04 (4k LE) variant

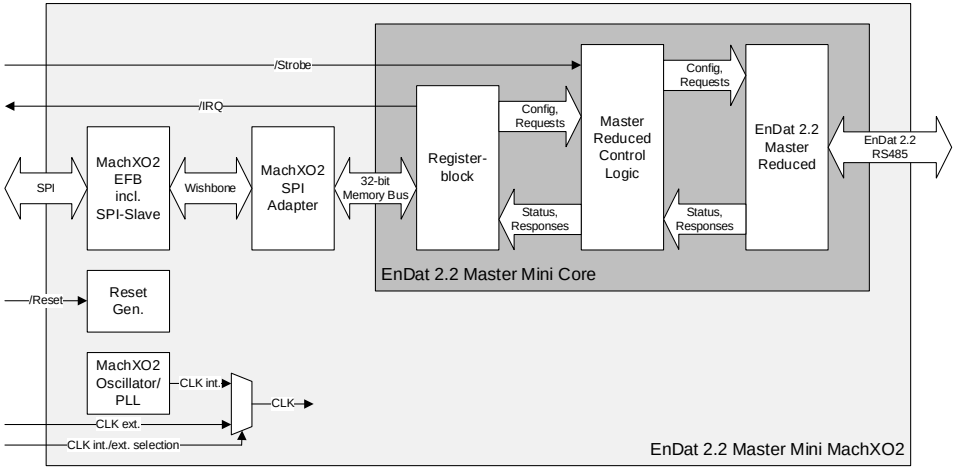
- FPGA
  - Integrated configuration memory
  - One supply voltage
  - Internal oscillator
- Possibilities
  - EnDat 2.2 Master Basic with SPI or microcontroller interface
  - Support of “safety with non-safe Master”
- Approximate prices of MBGA-153 (8 x 8 mm²) housing
  - 1000 units 10M04SCM153C8G ~ 5 US$
  - 10 000 units 10M04SCM153C8G ~ 4 US$
- Further housing versions
  - EQFP-144 (22 x 22 mm²), no BGA
  - UBGA-169 (11 x 11 mm²)
  - MBGA-153 (8 x 8 mm²)
- Constraints
  - Maximum EnDat clock frequency: 8 MHz



EnDat Master “Mini”: Lattice MachXO2 as XO2-1200 (1k LE) variant

- FPGA
  - Integrated configuration memory
  - One supply voltage
  - Internal oscillator
  - SPI integrated
- Possibilities
  - EnDat-Master Reduced with SPI connection
  - Functional Safety according to “safety with non-safe Master” is possible
- Approximate price of QFN-32 (5 x 5 mm²) housing
  - 1000 to 5000 units
    LCMXO2-1200HC-4SG32C < 2 US$
- Constraints
  - Maximum EnDat clock frequency: 8 MHz





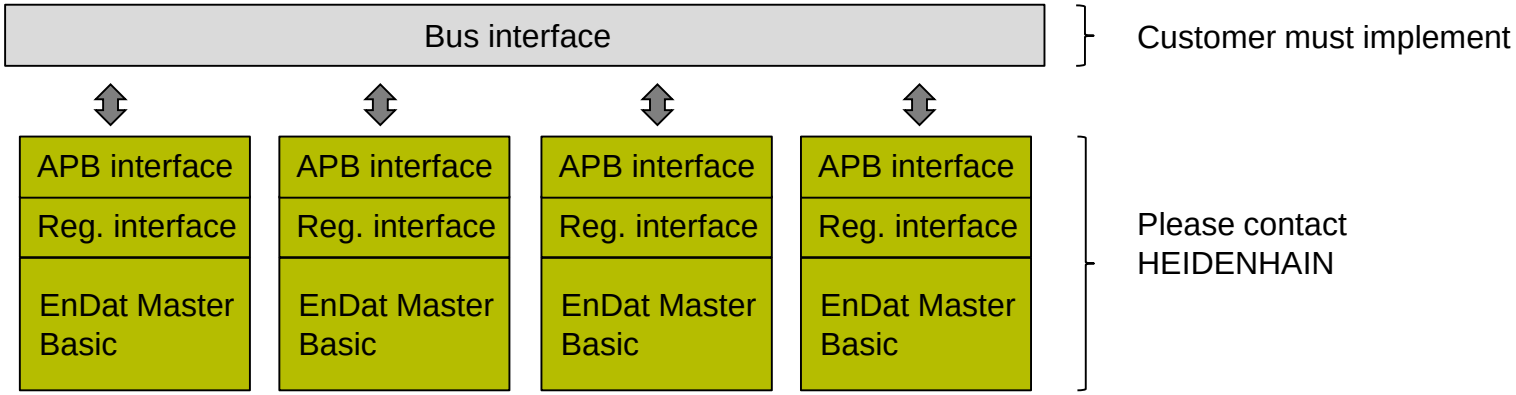
EnDat Master FPGA –Multi-Channel–

Multi-Channel Master using EnDat Master Basic (example shows four channels)

- EnDat Master Basic
- Register interface and APB interface is included
- Customer must add:
  - Bus interface

- Pro
  - Less design and testing effort
  - Bus interface: i.e. APB to SPI is available

- Con
  - Solution usually has more logistical elements (LE) compared to EnDat Master Reduced solution



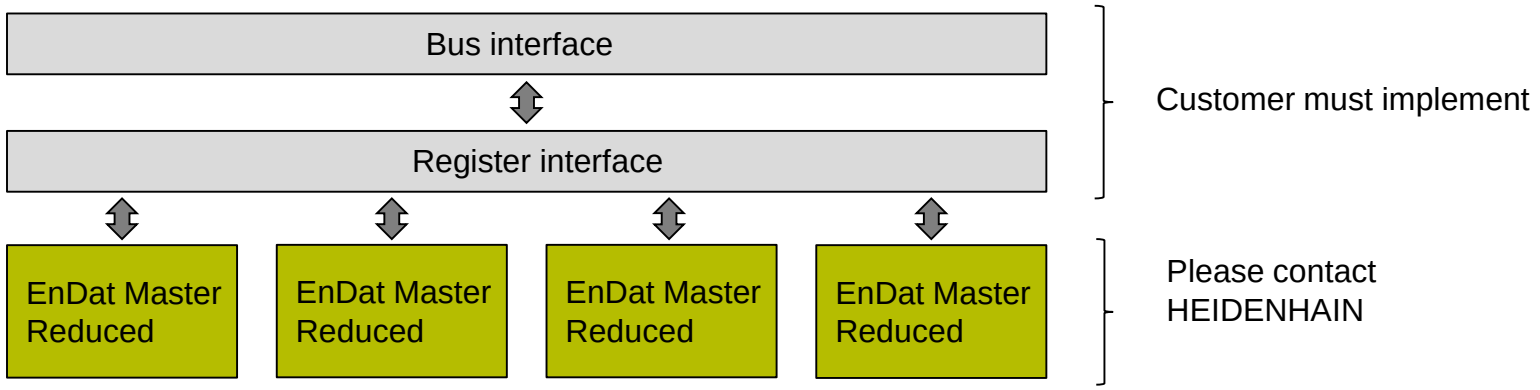
EnDat Master FPGA –Multi-Channel–

Multi-Channel Master using EnDat Master Reduced (example shows four channels)

- EnDat Master Reduced is delivered as VHDL code
- Customer must add:
  - Register interface
  - Bus interface

- Pro
  - Solution usually has fewer LE compared to EnDat Master Basic solution
  - Register interface can be tailored to customer requirements

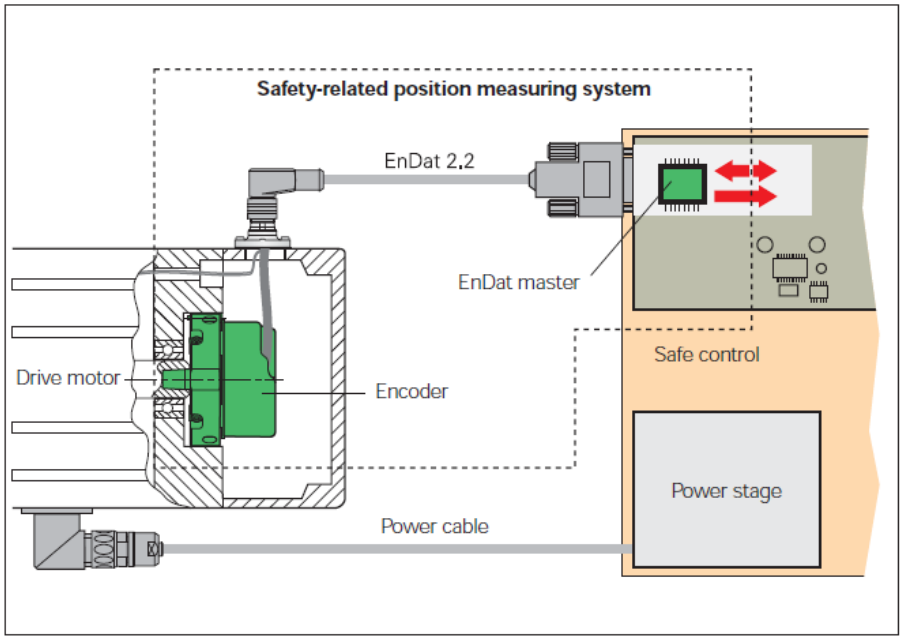
- Con
  - More design and testing effort



EnDat Master Functional Safety

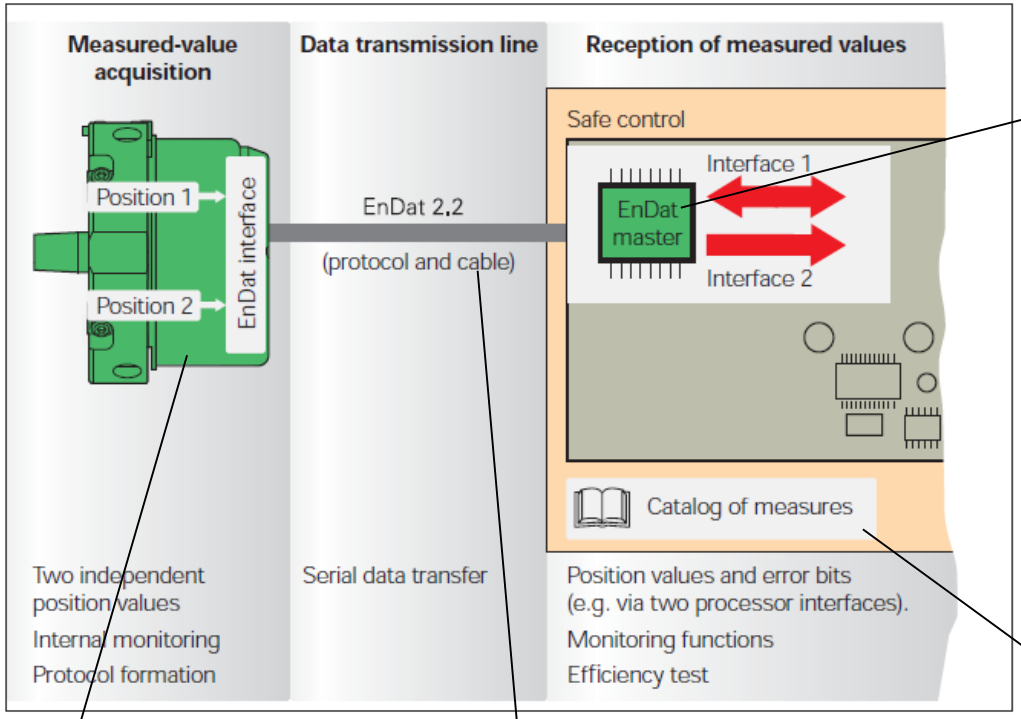
In practice, the complete “safe drive” system consists of:

- Safety-related position measuring system
- Safety-oriented control
  - EnDat Master with monitoring functions (EnDat Master Safe, see figure below) or
  - EnDat Master without monitoring functions (EnDat Master Standard)
- Power stage with motor power cable and drive
- Physical connection between encoder and drive (e.g. shaft connection/coupling)



	ECN 1325 Singleturn	EQN 1337 Multiturn
Safety-related data	Applicable as single-encoder system in the control loop for applications of the control category • SIL 2 (Safety Integrated Level) as in DIN EN IEC 61508 • PL2 (Performance Level) as in DIN EN ISO 13849 • Category 3 according to EN 954-1 Safe in the singleturn range	
PFH	≤ 1 x 10^{-8} Probability of failure per hour	
Angular error of the safe position	≤ ± 0.7° (9 bits)	

EnDat Master Functional Safety



EnDat Master

- Position values and error bits via two processor interfaces
- Monitoring functions
- Efficiency tests

Note:

- The EnDat Master and the package of measures are independent of the encoder (rotary, linear, angle encoder)

- Two independent position values
- Internal monitoring
- Protocol generation
- Serial data transfer (EnDat22 + HEIDENHAIN cable)
- Measures for safe control

The integration of safety functions in a technical device only works if the encoder functions with the safety-oriented application.
EnDat 2.2 is only one of the factors in achieving this goal.

Use of EnDat Master Safe

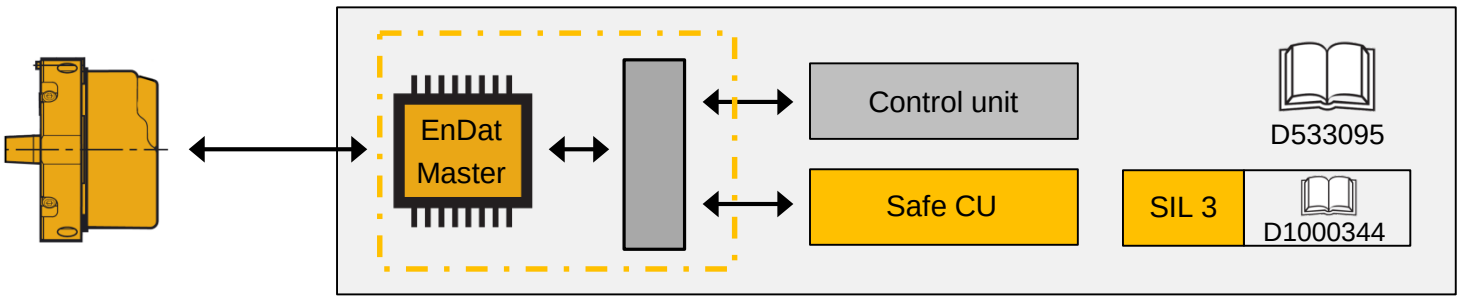
- The EnDat Master performs preprocessing and verification of the safety information
- Safety functions are performed by the EnDat Master and safe control
- Up to SIL 3 is possible (but only with EnDat Master Safe)

Benefits:

- EnDat Master relieves the safe CU
- EnDat Master buffers safety information (decoupling of the cycle times of safety and control)
- Safety functions in EnDat Master are pretested and verified

Disadvantages:

- EnDat Master is a part of the safety chain
  → Decoupling of the pure control functions and safety function is laborious and depends on the control design and safety design.
- EnDat Master must be certified (and with it usually the FPGA)
- Size of the EnDat Master



EnDat Master Functional Safety

Use of a non-safe EnDat Master

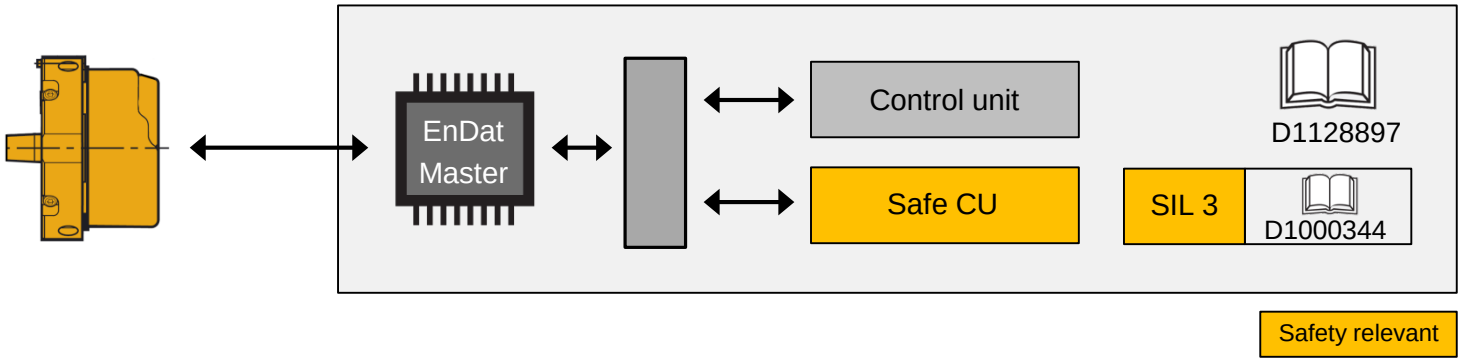
- The EnDat Master transfers the complete EnDat communication for evaluation to the safe CU.
  As a supplement, a measurement of the so-called “recovery-time t_M” is required. This measurement is a diagnostic function, not a safety function
- The EnDat Master does not modify the data and also does not perform any safety functions
- The EnDat Master is not a part of the safety chain
- Up to SIL 3 is possible

Benefits:

- The EnDat Master is not a part of the safety chain:
  → Certification of the EnDat Master is not necessary
  → Decoupling of control functions and safety functions
- Easy integration into a wide range of safety architectures
- Size of the EnDat Master

Disadvantages:

- The safe CU has to evaluate all data of the EnDat transmission because there is no preprocessing of the data in the EnDat Master (safe CU has to process the data in the control cycle)
  → The interface with the safe CU must be designed appropriately and the safe CU must process the data quickly enough.



EnDat Master Microcontroller-Based Implementation

EnDat 2.2 Master Microcontroller-Based Implementation

- Solutions with a microcontroller are used when the desired clock frequencies are relatively low.
- HEIDENHAIN can provide a sample code for the implementation of EnDat 2.1 mode commands when integration in a microcontroller is planned. The EnDat signals CLOCK and DATA are generated using GPIOs. An adaptation to the respective microcontroller is necessary.
- There are only very limited options for using SPI or UART blocks, since due to the flexible protocol structure (designed for little overhead) and the delay compensation, they would need to be followed by a very fast and flexible configuration.
- There are now also microcontroller-based solutions with integrated EnDat Master, such as from Texas Instruments, Renesas, or Hilscher. For more information, see “Other manufacturers”.

CRC calculation for micro-controller based solutions

- According to the EnDat Specification, the algorithm for calculating the CRC is optimized for FPGA
- Table-based solutions can be an advantage for microcontroller-based implementations or applications for functional safety (microcontroller is used to check the CRC). A sample code is available from HEIDENHAIN for this application.

EnDat Masters from Other Manufacturers

EnDat 2.2 Master

- Refer to the HEIDENHAIN website:
  http://www.heidenhain.de/de_EN/documentation/fundamentals/interfaces/endat-22/endat-Master/

- The following FPGA-based Master packages are available from HEIDENHAIN (also see previous slide)
  - EnDat Master Reduced — VHDL source code
  - EnDat Master Basic — SPI, APB, and microcontroller Interface, VHDL source code, simulation script
  - EnDat Master Safe — APB and microcontroller Interface, VHDL source code, simulation script
  - EnDat Master Mini — Special design for FPGA Lattice MachXO2 based on EnDat Master Reduced

- Microcontroller-based
  - Solutions with integrated EnDat Master (SoC-based)
    - Texas Instruments
    - Renesas
    - Hilscher
    - Analog Devices
  - Microcontroller in general: EnDat realized by means of software
    - Example code is available but must be adapted to the respective microcontroller

Recommendations for connecting the RS-485 Transceivers to the FPGA

- Two signals are required for EnDat communication:
  - Clock (unidirectional) and Data (bidirectional)

- The signals are transmitted to the measuring device via RS-485 transceiver.
  For requirments respectively recommendations on RS-485 transceivers see the relevant FAQ at
  www.heidenhain.de → Documentation → Fundamentals→ Interfaces→ EnDat 2.2 → FAQ

- For the connection of the RS-485 Transceiver to the FPGA there are recommendations from HEIDENHAIN regarding:
  - Pull-up respectively Pull-down resistors
  - Connection of Enable-Pins
  - Termination resistors
  - …

- The above recommendations must be adapted to the resprective general conditions of the customer electronics. For individual consultation, please contact your HEIDENHAIN contact person.