Boyi Li-Vera

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ECE graduate student (graduating Dec 2026) with hands-on experience in RTL design, HLS-based FPGA implementation, and hardware verification using SystemVerilog and Vitis HLS. Seeking full-time roles in Design Verification, RTL Design, or Hardware Engineering.

EDUCATION

University of California, Irvine Expected Dec 2026
M.S. Electrical & Computer Engineering

University of California, Riverside June 2024
B.S. Electrical Engineering | Minor in Computer Science
Coursework: Computer Architecture, SOC Design, Heterogeneous Integration Systems, Analog IC Design

TECHNICAL SKILLS

RTL & Verification: SystemVerilog, Verilog, RTL design, testbenches, SVA assertions, waveform debugging
EDA & Tools: Vitis HLS, ModelSim, Verilator, Icarus Verilog, Xilinx Vivado, Cadence Virtuoso / Spectre, Yosys
Scripting & Automation: Python, C++, TCL, Jupyter

EXPERIENCE

Quality Engineer Intern — Panasonic Avionics June – Sept 2025
Irvine, CA

- Automated four hardware quality workflows in Python, reducing processing time by 40% and improving traceability across hardware qualification records.
- Collaborated with cross-functional teams on avionics hardware qualification including documentation review, data validation, and compliance tracking.

PROJECTS

FPGA Neural Network Accelerator — Vitis HLS / C++ / Python 2025
AMD KR260 FPGA | EECS 221 Course Project | github.com/Leeboy0/EECS221-HLS

- Implemented a multilayer perceptron (MLP) for MNIST digit classification on the AMD KR260 FPGA using Vitis HLS; trained and quantized the model in Python, then wrote C++ HLS source synthesized to RTL.
- Developed a C++ testbench to validate functional correctness pre- and post-synthesis, applying HLS pragmas to optimize pipeline latency and resource utilization.

RV32I Single-Cycle CPU — Verilog / SystemVerilog 2025
github.com/Leeboy0 | Self-directed project

- Designed a 32-bit RV32I processor including ALU, control unit, register file, and memory interfaces; developed SystemVerilog testbenches to verify instruction execution and control flow.
- Caught edge cases in branch and load/store instructions via directed testing and waveform-based debugging; validated cycle-accurate functionality across the full RV32I base ISA.

45nm CMOS Op-Amp Design — Cadence Virtuoso Dec 2024
Cadence Spectre simulation | Graduate coursework

- Designed a three-stage CMOS op-amp achieving 350 MHz GBW, >60° phase margin, and 3.5 Vpp output swing at 12 mW power consumption.
- Iterated on transistor sizing and frequency compensation networks in Cadence Virtuoso with Spectre simulation to meet all performance targets.