Boyi Li-Vera

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SUMMARY

ECE graduate student with hands-on RTL/FPGA design and verification experience in SystemVerilog. Seeking a Summer 2026 internship in Design Verification, RTL Design, or Hardware Engineering.

EDUCATION

University of California, Irvine Expected Dec 2026
M.S. Electrical & Computer Engineering

University of California, Riverside June 2024
B.S. Electrical Engineering | Minor in Computer Science
Coursework: Heterogeneous Integration Systems, Semiconductor Devices, SOC Design, Analog IC Design, Computer Architecture

TECHNICAL SKILLS

RTL & Verification:	SystemVerilog, Verilog, RTL design, testbenches, SVA assertions, functional coverage, waveform debugging
EDA & Tools:	Verilator, Icarus Verilog, Xilinx Vivado, Yosys, Cadence Virtuoso / Spectre
Scripting & Automation:	Python, TCL, test automation, regression scripting
Hardware Interfaces:	UART, SPI, I2C, CAN

EXPERIENCE

Quality Engineer Intern — Panasonic Avionics June – Sept 2025
Irvine, CA

- Automated four hardware quality workflows using Python, reducing processing time by 40% and improving traceability across hardware qualification records.
- Supported cross-functional teams in avionics hardware quality processes including documentation review, data validation, and compliance tracking.

Student Researcher — Lawrence Livermore National Laboratory June – July 2022
Riverside, CA

- Preprocessed a 150+ feature dataset in Python; built and compared scikit-learn ML models achieving 85%+ accuracy in predicting small molecule inhibitors.
- Accelerated drug discovery by evaluating model accuracy and efficiency trade-offs across multiple classification algorithms.

PROJECTS

RV32I Single-Cycle CPU — Verilog / SystemVerilog June 2025

- Designed 32-bit RV32I processor including ALU, control unit, register file, and memory interfaces; developed SystemVerilog testbenches to verify instruction execution and control flow.
- Caught edge cases in branch and load/store instructions via directed testing and waveform-based debugging; validated cycle-accurate functionality across the full RV32I base ISA.

45nm CMOS Op-Amp Design — Cadence Virtuoso Dec 2024

- Designed a three-stage CMOS op-amp achieving 350 MHz GBW, >60° phase margin, and 3.5 Vpp output swing at 12 mW power consumption.
- Implemented and verified the design in Cadence Virtuoso with Spectre simulation, iterating on transistor sizing and frequency compensation networks.

Sequential FSM Design — SystemVerilog May 2022

- Designed a clock-synchronous FSM in SystemVerilog to control data flow through logic gates and latches.
- Developed testbenches with SystemVerilog assertions to verify FSM behavior across clock frequencies; validated correctness via waveform analysis in Icarus Verilog.