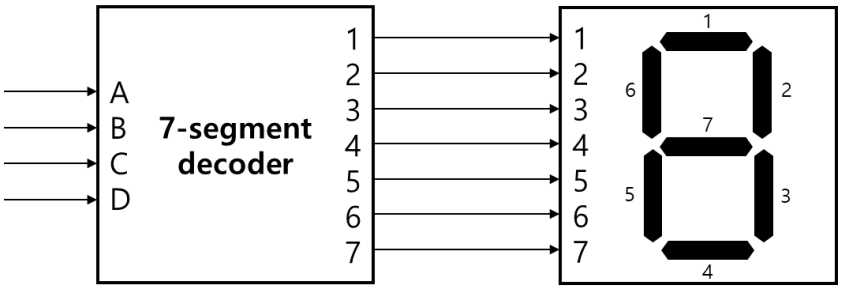
[EE303A] Digital System Design	

Lab #2

- 반드시 마감 기한을 지켜주세요.
  Please keep the due date in mind.
- 질문이 있으면 (홍성민, seongminhong@kaist.ac.kr)로 연락주세요.
  If you have any question, feel free to mail TA (seongminhong@kaist.ac.kr).

- This project's purpose is to understand the combinational logic. This project is to design 7-segment decoder as below figure.
- Write your code on "decoder.v".
- Testbench code tests 10 cases (number 0~9). Each case is 1 point and full score is 10 points.



Input (0~9)				Output to 7-segment (0: led off, 1: led on)							Decimal number
D	C	B	A	1	2	3	4	5	6	7	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	1	0	1	1	9