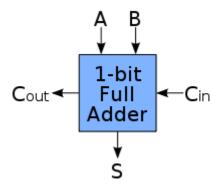
## Lab #3

Due date: 05/28 23:59

- 반드시 마감 기한을 지켜주세요.
   Please keep the due date in mind.
- 질문이 있으면 Lab 3 담당 조교 (최원종, starwars2008@kaist.ac.kr)로 연락주세요.

  If you have any question, feel free to mail TA. (WonJong Choi, starwars2008@kaist.ac.kr)
  - This project's purpose is to understand the combinational logic. This project is to design two logic. First, design 1-bit full adder as below figure. Second, design 2-bit multiplier using designed 1-bit full adder.
  - Write your code on "fa1b.v" and "mul2b.v".
  - Testbench code tests 10 cases (0x0, 1x1, 1x2, 1x3, ...., 3x2, 3x3). Each case is 1 point and full score is 10 points.



<1-bit Full adder>