[EE303A] Digital System Design **Due date : 05/15 23:59**

Verilog Lab #1

Overview

Lab 1 is a baby project that teaches you the basics of Verilog language. You are going to learn how to write a Verilog code and how to simulate it. In Lab1, you are required to implement an Arithmetic Logic Unit (ALU) by using Verilog language. **You should submit your ALU.v code through KLMS until the due date.** Good luck and have fun! (❁´◡`❁)

Files

You are given two files and You only need to change ALU.v. **You do not need to change TB.v.**

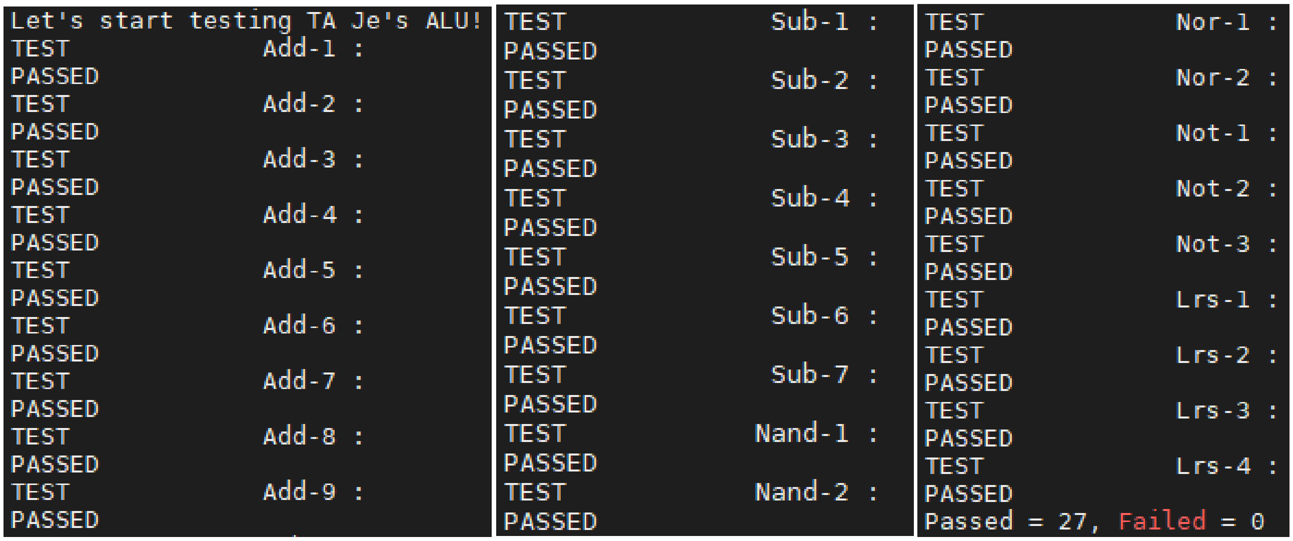
1. ALU.v : This is where you implement the ALU module.
2. TB.v : A Testbench file which you can test and grade your ALU module.

ALU Design

1. Inputs and outputs are 16-bit signed binary numbers.
2. Operation selection signals are 3-bit binary numbers. Those are defined in TB.v like ADD_SEL, SUB_SEL…
3. Overflow must be detected. For Add & Sub operation, the ALU should be able to handle overflow. Cout must be one if overflow happens; otherwise, Cout should be zero.

Simulation output & Grading

The TA will grade your lab assignment with TB.v, which is already given to you. If you pass all the tests in TB.v, you will get a full score. Your score is determined by how many tests you pass. If you pass the all the tests in TB, you can have the same output screen like TA did shown below. **If you have any question, please contact to TA Je Yang (yangje@kaist.ac.kr)**



```
Let's start testing TA Je's ALU!
TEST                  Add-1 :
PASSED
TEST                  Add-2 :
PASSED
TEST                  Add-3 :
PASSED
TEST                  Add-4 :
PASSED
TEST                  Add-5 :
PASSED
TEST                  Add-6 :
PASSED
TEST                  Add-7 :
PASSED
TEST                  Add-8 :
PASSED
TEST                  Add-9 :
PASSED
```

```
TEST                  Sub-1 :
PASSED
TEST                  Sub-2 :
PASSED
TEST                  Sub-3 :
PASSED
TEST                  Sub-4 :
PASSED
TEST                  Sub-5 :
PASSED
TEST                  Sub-6 :
PASSED
TEST                  Sub-7 :
PASSED
TEST                 Nand-1 :
PASSED
TEST                 Nand-2 :
PASSED
```

```
TEST                  Nor-1 :
PASSED
TEST                  Nor-2 :
PASSED
TEST                  Not-1 :
PASSED
TEST                  Not-2 :
PASSED
TEST                  Not-3 :
PASSED
TEST                  Lrs-1 :
PASSED
TEST                  Lrs-2 :
PASSED
TEST                  Lrs-3 :
PASSED
TEST                  Lrs-4 :
PASSED
Passed = 27, Failed = 0
```