Structure of RIDECORE repository

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2016/03/24

```
|-README.md \#Introduction, Quick Start and How to Use
|-LICENCE \#LICENCE of RIDECORE, vscale, and memgen
| |-document_jp.pdf \#Document of RIDECORE in Japanese
| |-document_en.pdf \#Document of RIDECORE in English
| |-RISC-V-subset.pdf \#executable instruction of RIDECORE
|-src
| |-fpga \#RIDECORE source code and .xdc file for synthesize
    |-singlecyc \#RISC-V single cycle processor
    | |-sim \#Makefile Only
    | |-bin \#Binary of application
       |-verilog \#Source code and testbench
    |-ridecore \#RIDECORE testbench
       |-sim \#Testbench and Makefile
        |-app \#Applications for RIDECORE in C
       |-bin \#Binary of application
|-toolchain
  |-memgen-v0.9 \#memgen for RISC-V
```

図 1 Structure of RIDECORE repository

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pipe(pipeline.v)
|-pipeline_if(pipeline_if.v)
| |-imem(imem.v)
| |-btb(btb.v)
| | |-ram_sync_1r1w(ram_sync.v)
\perp
| |-gshare_predictor(gshare.v)
  |-true_dualport_ram(dualport_ram.v)
|-tag_generator(tag_generator.v)
|-decoder(decoder.v)
|-sourceoperand_manager(srcopr_manager.v)
|-rrf_freelistmanager(rrf_freelistmanager.v)
|-arf(arf.v)
| |-ram_sync_nolatch4r2w(ram_sync_nolatch.v)
|-rrf(rrf.v)
|-src_manager(src_manager.v)
|-imm_gen(imm_gen.v)
|-brimm_gen(brimm_gen.v)
|-rs_requestgenerator(rs_reqgen.v)
|-allocateunit(pricenc.v)
|-oldest_finder8(oldest_finder.v)
|-rs_alu(rs_alu.v)
|-alloc_issue_ino(alloc_issue_ino.v)
| |-search_begin(search_be.v)
| |-search_end(search_be.v)
|-rs_ldst(rs_ldst.v)
|-rs_branch(rs_branch.v)
|-rs_mul(rs_mul.v)
|-exunit_alu(exunit_alu.v)
| |-src_a_mux(srcsel.v)
| |-src_b_mux(srcsel.v)
| |-alu(alu.v)
|-dmem(dmem.v)
|-storebuf(storebuf.v)
| |-search_begin(search_be.v)
| |-search_end(search_end.v)
|-exunit_ldst(exunit_ldst.v)
|-exunit_mul(exunit_mul.v)
| |-multiplier(multiplier.v)
|-exunit_branch(exunit_branch.v)
| |-alu(alu.v)
|-miss_prediction_fix_table(mpft.v)
|-reorderbuf(reorderbuf.v)
```

☑ 2 Source code tree of RIDECORE