VLSI
Lab exercise 2

Students:

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מספר חשבון: rg18

שעות עבודה: 70 שעות.

תאריך הגשה: 10.7.2025

Go through report files, and **submit**:

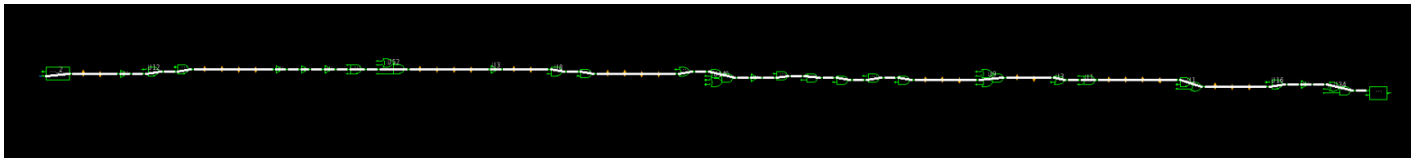
1. For maximum delay
   (a) What is the maximum delay? What is the slack[5]? Is the slack feasible or violating? How many gates and registers are involved in this path?
   (b) What are clock-to-out time, $t_{clk \to out}$, and setup time, t_{setup}, of the register? Note: you may choose any register for any sort of time (or mix), Please pay attention clock-to-out time could be extracted explicitly from timing report.
   (c) Report the critical path.[6] Which top-level blocks of the design are part of this path? Include a print-screen of the schematic view with this path highlighted.

a. Max delay = 3.06 [ns]
Slack = 1.14 [ns]
The slack is violating, because it is negative.
The number of gates and registers involved in this path: 33.

b. $t_{clk \to out} = 0.25\ [ns]$
$t_{setup} = 0.08[ns]$

c. Top-level blocks involved in this path:

1. cont/statelogic – source state register and initial logic
2. cont/outputlogic – control signal generation
3. controller – routes control signals
4. datapath_WIDTH8_REGBITS3 – datapath logic
5. mux4_WIDTH8 – multiplexer for ALU inputs
6. condinv – conditional inverter
7. mux2 – operand selection
8. alu_WIDTH8 – arithmetic logic unit
9. adder_DW01_add_1 – internal adder logic
10. zerodetect_WIDTH8 – zero detection logic
11. flopenr_WIDTH8 – destination PC register block



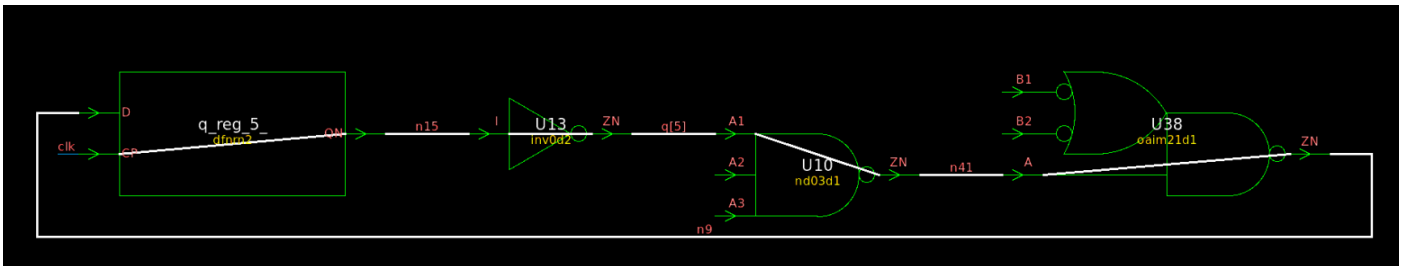
2. For minimum delay
   (a) What is the minimum delay? What is the slack?
   (b) What is hold time, t_{hold}?
   (c) How many gates are involved? Are there any particularities in this path?
   (d) Include the report the critical path for min-delay and a print-screen of the schematic view with this path highlighted.

a. Max delay = 0.41 [ns]
Slack = 0.44 [ns]

b. $t_{hold} = -0.03\ [ns]$

c. The number of gates and registers involved in this path: 3.
The particularities in this path are:

1. Instead of checking that delays don't exceed a maximum (as in setup analysis), we're verifying that signals aren't arriving too early and breaking the hold requirement.
2. The path begins and ends at the same flip-flop q_reg_5_, revealing that the signal travels through internal or combinational circuitry and loops back into the same register.
3. Since the slack is positive, even the fastest possible propagation won't violate the hold time, so this path is safe.



3. For area and fanout
   (a) What is the obtained area? Does it meet the constraint?
   (b) Which constraints influence the area and how?
   (c) In the console type `report_net_fanout -threshold 10`. What are the nets with fanout larger than 10? Would you reckon impose fanout constraints, if so, why?

a. The obtained area is: 2266.12
Since it is bigger than the required area is 2000, it does not meet the construction requirements.

b. Constraints that influence the area include timing constraints and the complexity of the combinational logic.
Timing constraints, such as clock period and input/output delays, can force the synthesizer to use faster (and therefore larger) gates to meet the required performance.
In addition, the structure of the combinational logic itself affects the number of gates needed, which directly impacts the total area of the circuit.

c.

```
Net                 Fanout   Attributes   Capacitance   Driver
-------------------------------------------------------------------------
clk                    140   dr               2.67      clk
1
design_vision>
```

The clock net has a fanout of 140, as it drives nearly all components in the circuit.
In our view, it is not recommended to constrain the clock's fanout, since the clock must be distributed to all sequential elements.
Limiting its fanout could interfere with proper clock distribution and lead to incorrect or unbalanced timing across the design.

Submit:

5. Compose a table (as shown below) and summarise results of each update step.

5.

Update	Max delay [ns]	Power	Area
Fanout 4	2.97	5.9759 mW	1962.724799
Period 12 [nsec]	6.53	916.2281 uW	1770.071278
Area 1800	6.53	916.2281 uW	1770.071278
Ultra compiler	6.57	936.4200 uW	1518.777931

6. Explain how and why each of the aforementioned updates affects the results. Relate to period, area and power.
7. What can you say about the hierarchical organisation while compiling with Ultra and without it? Why does it improve the results?

6.

(a) Fanout 4 (from Fanout 1):
Raising the fanout limit allowed the tool to reduce buffer insertion, which improved timing (delay), and significantly reduced power and area by minimizing unnecessary gates.
(b) Period 12 ns (with Fanout 4):
Relaxing the clock period gave the tool more flexibility to use slower, smaller gates. This increased delay, but reduced power and area, since aggressive optimizations were no longer needed.
(c) Area constraint 1800 (with Fanout 4 + Period 12):
The design already met the area requirement, so this constraint had no effect. Delay, power, and area stayed the same.
(d) Ultra Compiler (with all previous constraints):
Enabling the Ultra compiler (useUltra=1) slightly increases the max delay (to 6.57 ns) and power (to 936.4 μW) compared to the previous step but achieves a significant reduction in area (down to 1518.8). This shows that Ultra aggressively optimizes for area, sometimes at a small cost to delay and power, resulting in a more efficient layout.

7.

It can be observed that the design no longer maintains a hierarchical structure, with all blocks placed on the same level. This flattening of the hierarchy leads to significant improvement in area.

Compile again, view the reports, answer and **submit**:

9. View the final netlist (*mips.v*) and answer accordingly:
   (a) Give an example of different types of NAND and NOR gates are used (at least 2 of each).
   (b) What is the difference between these gates?
   (c) Give an example of different registers. What is (are) the difference(s) between them?

9.

a. example of NAND:

```
nd02d0 U358 ( .A1(n276), .A2(n280), .ZN(dp_rf_n13) );
nd03d1 U472 ( .A1(n285), .A2(n284), .A3(n283), .ZN(dp_rf_n9) );
```

example of NOR:

```
nr02d0 U364 ( .A1(dp_ra2[2]), .A2(n458), .ZN(n496) );
nr04d0 U378 ( .A1(cont_statelog_n65), .A2(cont_state[3]), .A3(n286), .A4(n388), .ZN(n275) );
```

b.

- nd02d0: A NAND gate with two inputs, A1 and A2, and an output labeled ZN.
- nd03d1: A NAND gate that has three inputs - A1, A2, and A3- and produces an output ZN.
- nr02d0: A NOR gate with two inputs, A1 and A2, and an output ZN.
- nr04d0: A NOR gate featuring four inputs- A1, A2, A3, and A4 -and an output ZN.

The prefixes **nd** and **nr** denote NAND and NOR gates respectively, while the numbers that follow specify how many inputs each gate has. The suffixes like **d0**, **d1**, etc., typically refer to a particular technology library or design style, which might affect characteristics such as timing or power behavior in the specific fabrication process or simulation environment.

c. For example:

```
denrq1 dp_ir0_q_reg_0_ ( .D(memdata[0]), .ENN(n226), .CP(clk), .Q(funct[0]));
denrq1 dp_ir2_q_reg_7_ ( .D(memdata[7]), .ENN(n224), .CP(clk), .Q(dp_ra1[2]));
```

The register dp_ir0_q_reg_0_ outputs to funct[0], which functions as a control signal within the circuit. On the other hand, the register dp_ir2_q_reg_7_ outputs to dp_ra1[2], serving as a datapath signal. The difference in how their outputs are used defines their distinct roles—one influences control logic, while the other handles data processing.

Submit:

11. What is the purpose of power rings and stripes in a chip? Which phenomena do they prevent/reduce?

11. Power rings and supply stripes on an integrated circuit are implemented to avoid parasitic effects from long-distance power routing. By establishing these localized power distribution paths, the length of each connection between circuitry and its supply rails is kept to a minimum. This arrangement enhances the efficiency of power delivery, lowers voltage drop across the network, and keeps signals stable by reducing extra resistance and inductance in the power lines.

Observe the output in the terminal, answer and **submit**:

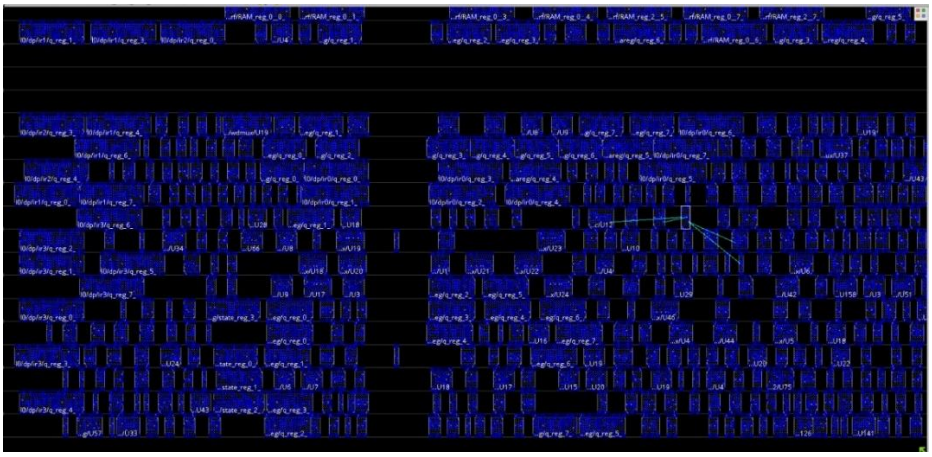
12. Compose a table (as shown below), summarise metal information. Supportive information may be present in your terminal.

Update	Direction (H/F/V)	Length μm	Number of Vias
M1	1H	0	2394
M2	2V	17136	3313
M3	3H	19803	38
M4	4V	1015	5
M5	5H	86	0
TOP_M (M6)	6V	0	0

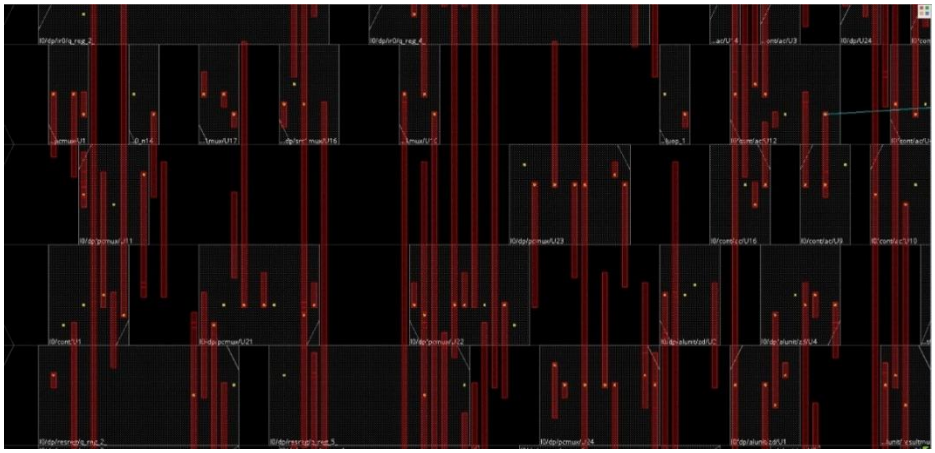
13. Zoom in into the design, which metals (of metals 1 to 4) are aligned to the grid? The grid could be seen in light grey colour. Please attach images of each metal, and grid.

13.

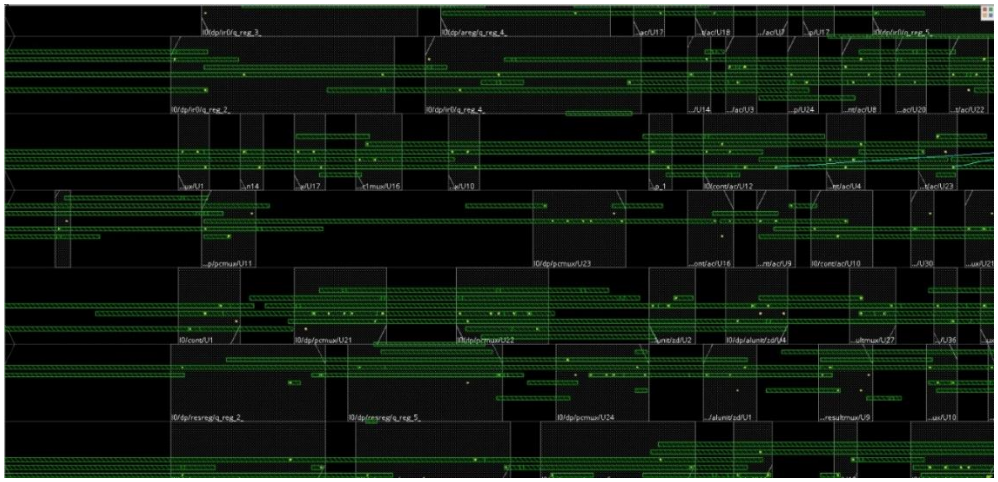
M1:



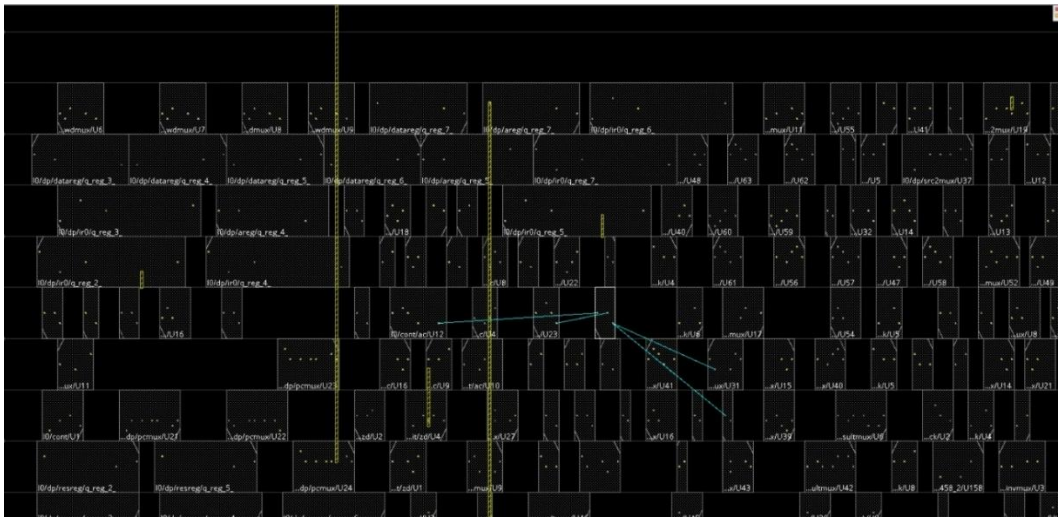
M2:



M3:



M4:



14. Select a cell (does not matter which), open its attributes and explain:
    (a) What is the meaning of orientation of a cell? Do you think this information is important? If so, why one would choose a certain orientation? You may support your answer with images from layout.
    (b) What are the possible statuses of a cell? Explain the difference between placed, unplaced, fixed and cover. Hint: Press 'Ctrl+f', choose 'Find the object on the whole design', choose 'Status' under 'Property', choose the status under 'Value' and click 'Find'.
    (c) Give an example (of a cell or a design) for 2 statuses of your choice.

14.

a)

The orientation of a cell describes how it's rotated or flipped within the chip layout. For example, a cell might be placed normally, upside down, or mirrored. This matters because it affects how the cell connects to power rails and to neighboring cells. Designers often alternate orientations between rows to save space and align the VDD and VSS connections more efficiently. Choosing the right orientation helps with routing, power delivery, and overall area usage. Incorrect orientation may lead to connectivity issues or poor alignment with adjacent cells.

b)

The possible statuses of a cell in the layout are:

1. Placed:
Cells that have been assigned a location in the layout during the placement phase. Their positions are still flexible and may change during further optimization.

2. Unplaced:
Cells that are part of the design but do not yet have a physical location. These are waiting to be placed in the layout in later steps.

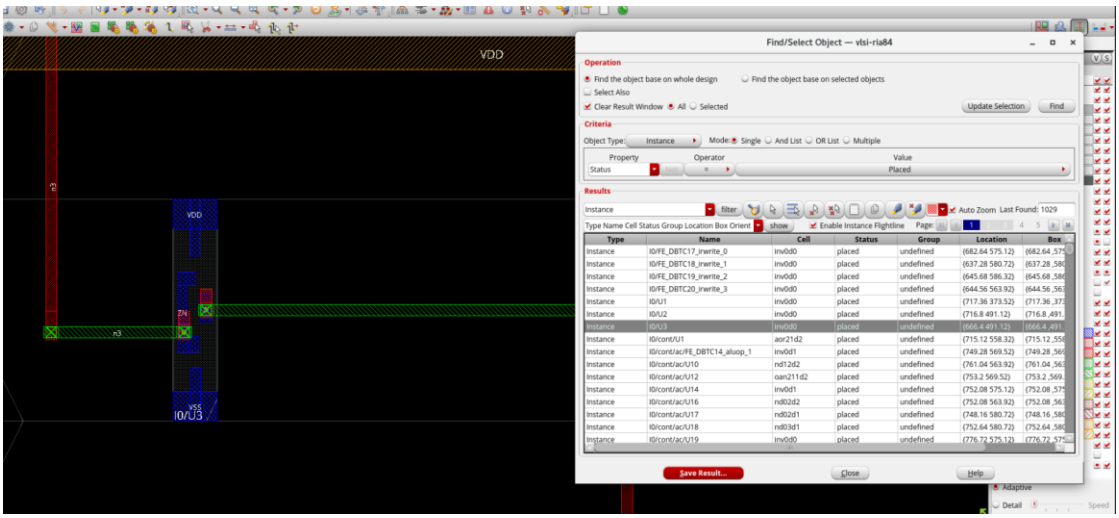
3. Fixed:
Cells that are placed in a specific location and cannot be moved by the tool automatically. They can only be repositioned manually if needed.

4. Cover:
Cells that are completely locked in place. They cannot be moved either manually or by automated tools, ensuring their position stays unchanged.

c)

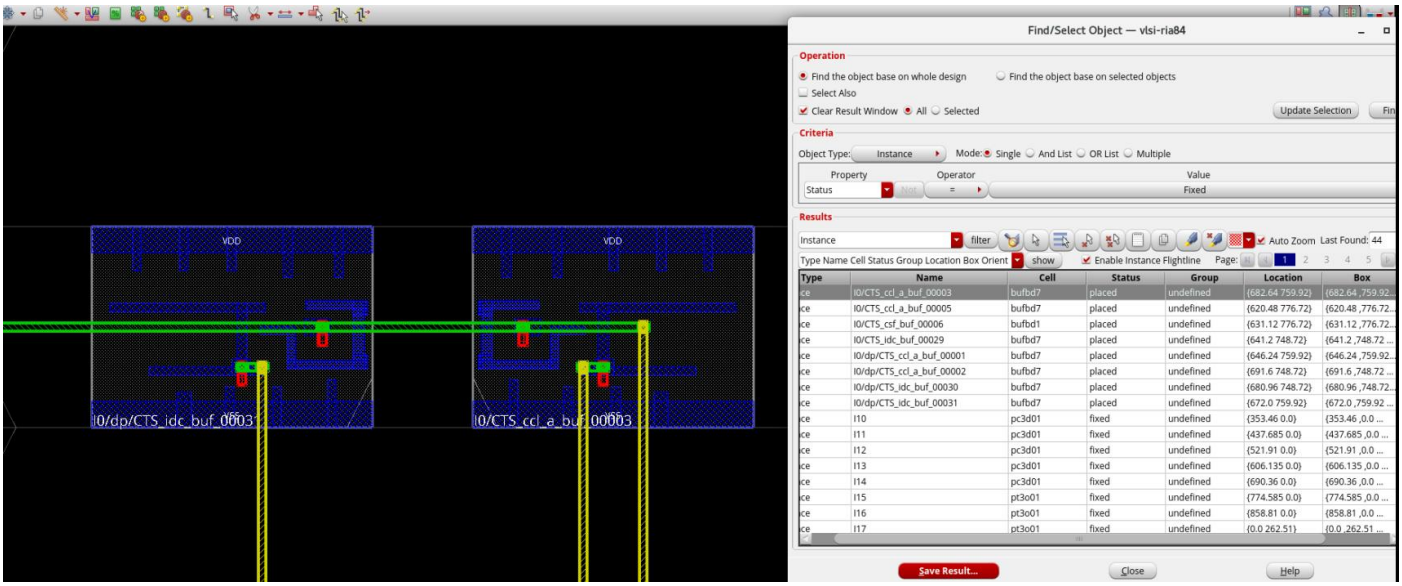
Placed:
These are cells positioned near the center of the layout during the placement stage. Their locations are chosen to allow optimization for area, power efficiency, and timing performance.

For example:



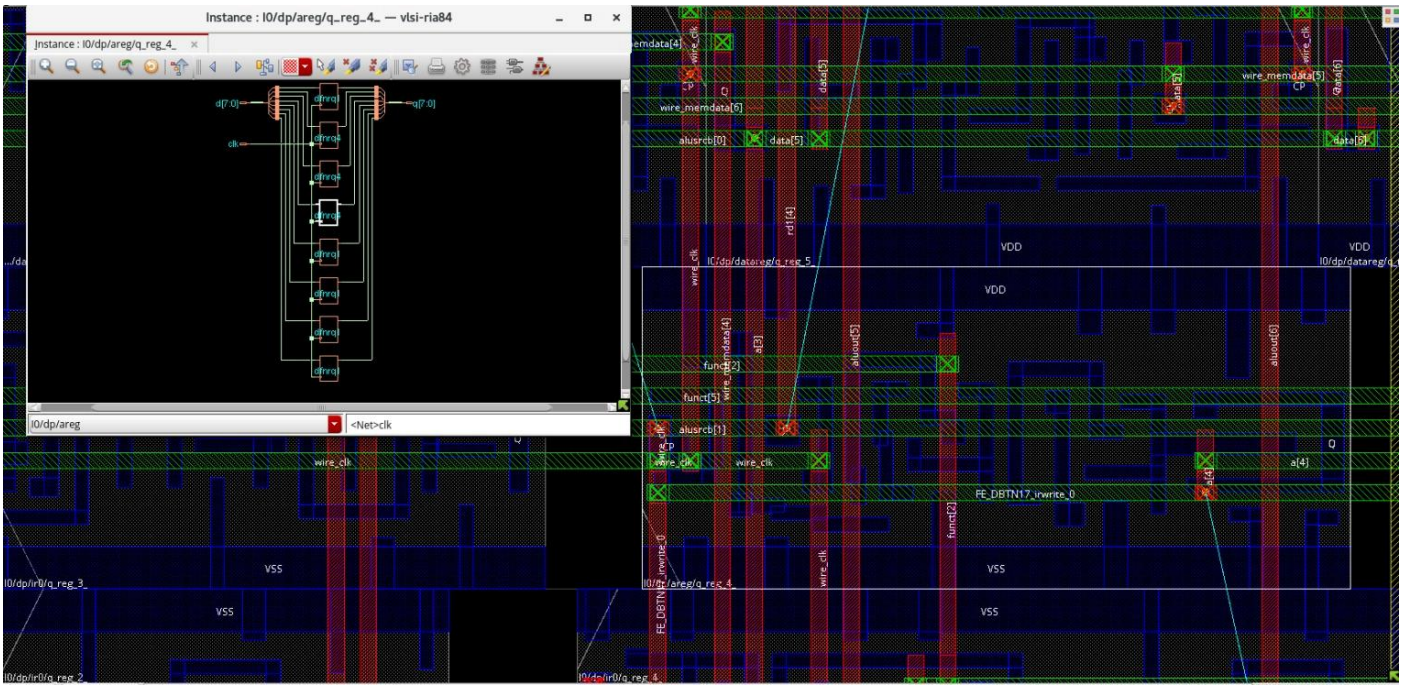
Fixed:
These are rectangular cells typically placed along the edges of the design. They are usually used for I/O pins or power connections and must stay in place to ensure the correct operation of the chip.

For example:

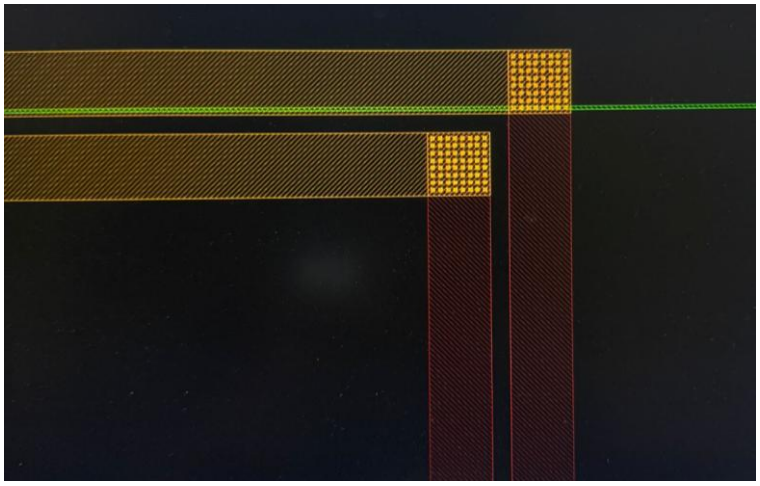


15. Select a cell (it does not matter which), attach an image showing its schematic next to its layout.
16. Zoom into ring corner and attach an image showing the vias in the corners.

15.



16.



Submit:

17. Submit a report of the critical path (If you prefer, you can add a screenshot of this report). What is the critical path slack? Is it the same path in behavioural synthesis? If not, explain why.
18. Search for the critical path obtained in the behavioural synthesis, what is its delay? Submit the report of this path. Hint: Use `report_timing -from [starting point] -to [end point]`, when writing a point, please write instance only, without its port. You can also write the points as they are observed, for example, in **your** *reg2reg* reports
(e.g., `I0/cont_statelog_state_reg_0_/CP` **or** `I0/cont/statelog/state_reg_0_/CP`).

17.

```
#####################################################################################
Calculate delays in BcWc mode...
Start delay calculation (fullDC) (1 T). (MEM=2450.55)
*** Calculating scaling factor for Max libraries using the default operating condition of each library.
Total number of fetched objects 692
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2464.14 CPU=0:00:00.1 REAL=0:00:01.0)
End delay calculation (fullDC). (MEM=2464.14 CPU=0:00:00.1 REAL=0:00:01.0)
Path 1: MET Setup Check with Pin I0/dp/pcreg/q_reg_7_/CP
Endpoint:   I0/dp/pcreg/q_reg_7_/D           (^) checked with  leading edge of
'clk'
Beginpoint: I0/cont/statelog/state_reg_0_/QN (^) triggered by  leading edge of
'clk'
Path Groups: {clk}
Analysis View: SlowView
Other End Arrival Time          -0.516
- Setup                          0.109
+ Phase Shift                    9.000
= Required Time                  8.375
- Arrival Time                   5.109
= Slack Time                     3.265
     Clock Rise Edge                      0.000
     + Clock Network Latency (Ideal)     -0.516
     = Beginpoint Arrival Time           -0.516
     +-------------------------------------------------------------------------------------------------------------------+
     |                      Instance                      |     Arc      |   Cell   | Delay | Arrival | Required |
     |                                                    |              |          |       |  Time   |   Time   |
     |----------------------------------------------------+--------------+----------+-------+---------+----------|
     | I0/cont/statelog/state_reg_0_                      | CP ^         |          |       |  -0.516 |    2.749 |
     | I0/cont/statelog/state_reg_0_                      | CP ^ -> QN ^ | dfnrn1   | 0.368 |  -0.148 |    3.117 |
     | I0/cont/statelog/U7                                | I ^ -> ZN v  | inv0d0   | 0.225 |   0.077 |    3.342 |
     | I0/cont/outputlog/FE_DBTC15_state_3                | I v -> ZN ^  | inv0d0   | 0.340 |   0.417 |    3.682 |
     | I0/cont/outputlog/U38                              | A1 ^ -> ZN v | nd02d0   | 0.151 |   0.568 |    3.833 |
     | I0/cont/outputlog/U45                              | I v -> ZN ^  | inv0d0   | 0.199 |   0.767 |    4.032 |
     | I0/cont/outputlog/U28                              | A2 ^ -> ZN v | nd12d1   | 0.107 |   0.873 |    4.138 |
     | I0/cont/outputlog/U31                              | I v -> ZN ^  | inv0d0   | 0.427 |   1.300 |    4.566 |
     | I0/cont/ac/U16                                     | A1 ^ -> ZN v | nd02d1   | 0.144 |   1.444 |    4.710 |
     | I0/cont/ac/U10                                     | A2 v -> ZN ^ | nd12d1   | 0.301 |   1.746 |    5.011 |
     | I0/dp/alunit/binv/invmux/FE_DBTC28_alucontrol_2    | I ^ -> ZN v  | inv0d0   | 0.294 |   2.039 |    5.304 |
     | I0/dp/alunit/binv/invmux/U18                       | A2 v -> Z v  | aor22d1  | 0.303 |   2.342 |    5.607 |
     | I0/dp/alunit/addblock/add_1_root_add_458_2/U80     | A1 v -> Z v  | or02d1   | 0.204 |   2.546 |    5.811 |
     | I0/dp/alunit/addblock/add_1_root_add_458_2/FE_DBTC | I v -> ZN ^  | inv0d0   | 0.180 |   2.726 |    5.991 |
     | 27_n34                                             |              |          |       |         |          |
     | I0/dp/alunit/addblock/add_1_root_add_458_2/U147    | A2 ^ -> ZN v | nr02d1   | 0.110 |   2.836 |    6.101 |
     | I0/dp/alunit/addblock/add_1_root_add_458_2/U89     | A1 v -> Z v  | an02d1   | 0.156 |   2.993 |    6.258 |
     | I0/dp/alunit/addblock/add_1_root_add_458_2/U126    | A2 v -> ZN ^ | nd12d1   | 0.075 |   3.067 |    6.332 |
     | I0/dp/alunit/addblock/add_1_root_add_458_2/U133    | A1 ^ -> ZN v | nd02d1   | 0.076 |   3.144 |    6.409 |
     | I0/dp/alunit/addblock/add_1_root_add_458_2/U115    | A2 v -> ZN ^ | nd12d1   | 0.069 |   3.213 |    6.478 |
     | I0/dp/alunit/addblock/add_1_root_add_458_2/U151    | A1 ^ -> ZN v | nd02d1   | 0.104 |   3.317 |    6.582 |
     | I0/dp/alunit/resultmux/U27                         | B1 v -> ZN v | oaim21d1 | 0.233 |   3.550 |    6.815 |
     | I0/dp/alunit/zd/U3                                 | A2 v -> Z v  | or02d1   | 0.253 |   3.802 |    7.067 |
     | I0/dp/alunit/zd/U1                                 | A2 v -> ZN ^ | nr13d1   | 0.214 |   4.016 |    7.281 |
     | I0/cont/U1                                         | B1 ^ -> Z ^  | aor21d1  | 0.193 |   4.209 |    7.475 |
```

The critical path slack is 3.265(ns), which is longer than the behavioral slack which is 0.87 [ns].

The reason for the difference is that behavioral synthesis provides only estimated timing, without considering the physical implementation of the design. It does not account for placement, routing, parasitics, or actual cell delays. On the other hand, STA after placement includes real physical data, which often allows more accurate slack calculations. Therefore, it is expected and normal that the slack changes, and the critical path may also differ.

18.

The critical path that is obtained in the physical is not the same as in behavioural synthesis. In the behavioural as we can see in the report down here:

Startpoint: cont_statelog_state_reg_0_

Endpoint: dp_pcreg_q_reg_2_

Critical Path Delay (Data Arrival Time): 7.98 ns

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
Design : mips
Version: S-2021.06-SP4
Date   : Sun Jun 22 19:32:40 2025
****************************************

Operating Conditions: tsl18fs120_typ   Library: tsl18fs120_typ
Wire Load Model Mode: enclosed

  Startpoint: cont_statelog_state_reg_0_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: dp_pcreg_q_reg_2_
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mips               4000                  tsl18fs120_typ
```

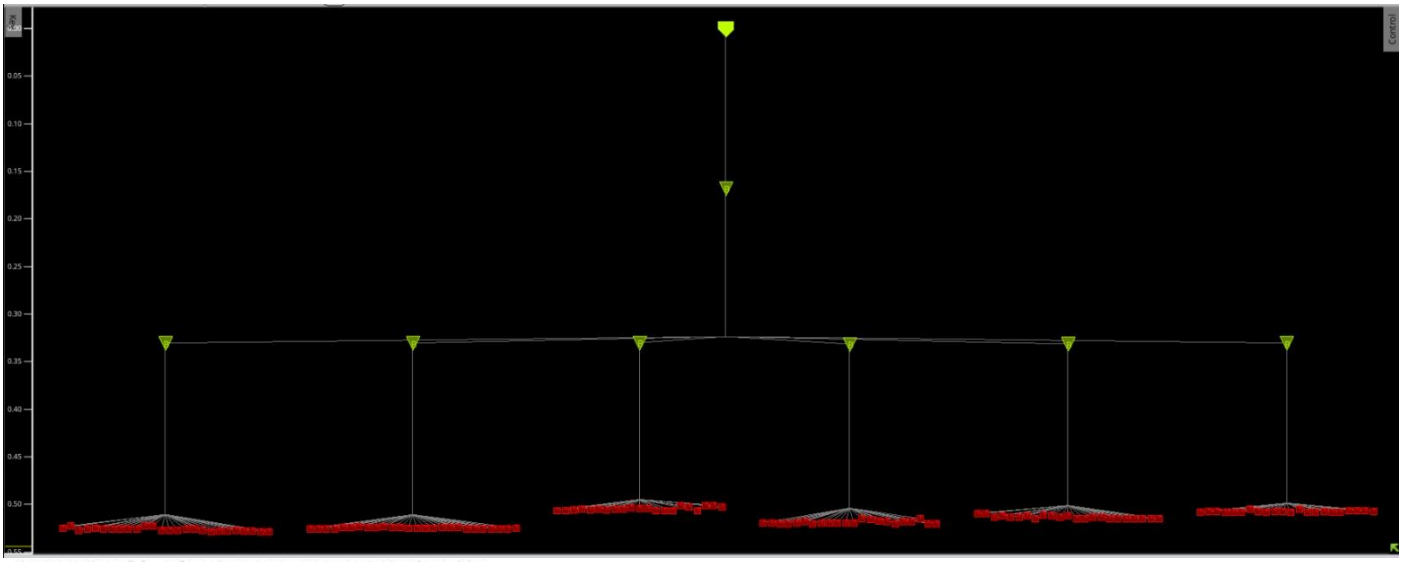
```
  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mips               4000                  tsl18fs120_typ

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  cont_statelog_state_reg_0_/CP (dfnrq1)                  0.00       0.00 r
  cont_statelog_state_reg_0_/Q (dfnrq1)                   0.43       0.43 f
  U407/ZN (inv0d0)                                        0.93       1.36 r
  U409/ZN (nd04d0)                                        0.26       1.62 f
  U336/ZN (inv0d0)                                        1.01       2.63 r
  U410/ZN (aoi21d1)                                       0.10       2.73 f
  U367/ZN (inv0d0)                                        1.03       3.76 r
  U368/ZN (inv0d0)                                        0.63       4.39 f
  U417/ZN (aoi22d1)                                       0.35       4.74 r
  U353/CO (ad01d0)                                        0.25       4.99 r
  U307/ZN (inv0d0)                                        0.10       5.08 f
  U440/ZN (aoi21d1)                                       0.24       5.33 r
  U498/CO (ad01d0)                                        0.20       5.53 r
  U317/ZN (nr02d0)                                        0.09       5.61 f
  U332/ZN (nd02d0)                                        0.11       5.73 r
  U345/ZN (nd02d0)                                        0.17       5.89 f
  U441/ZN (aon211d1)                                      0.23       6.12 r
  U443/ZN (nd03d1)                                        0.08       6.20 f
  U444/ZN (aon211d1)                                      0.07       6.27 r
  U324/Z (xr03d1)                                         0.36       6.63 f
  U445/ZN (aoi221d1)                                      0.23       6.86 r
  U447/ZN (aoim211d1)                                     0.07       6.93 f
  U529/ZN (aoi31d1)                                       0.20       7.13 r
  U316/ZN (nr02d0)                                        0.11       7.25 f
  U339/ZN (inv0d0)                                        0.63       7.87 r
  U540/ZN (oai22d1)                                       0.10       7.98 f
  dp_pcreg_q_reg_2_/D (dfnrb1)                            0.00       7.98 f
  data arrival time                                                  7.98

  clock clk (rise edge)                                   9.00       9.00
  clock network delay (ideal)                             0.00       9.00
  dp_pcreg_q_reg_2_/CP (dfnrb1)                           0.00       9.00 r
  library setup time                                     -0.15      S 8.85
  data required time                                                S 8.85
  --------------------------------------------------------------------------
  data required time                                                 8.85
  data arrival time                                                 -7.98
  --------------------------------------------------------------------------
  slack (MET)                                                       0.87
```

Explore the CTS debugger, answer and **submit**: (Hint: Go to 'View → Enable clock path browser'.)

19. How many buffers were introduced to satisfy the requirements? Please include a figure as evidence to support your answer. What is the purpose of buffers in CTS?
20. What is the average skew between the FFs? Please include a figure as evidence to support your answer. Considering the max/min delay timing analysis, would this skew work? Answer quantitatively.

19.

Num of buffers is 8.



```
Setting all clocks to propagated mode.
External - Set all clocks to propagated mode done. (took cpu=0:00:00.6 real=0:00:00.6)
Clock DAG stats after update timingGraph:
  cell counts      : b=8, i=0, icg=0, dcg=0, l=0, total=8
  sink counts      : regular=140, enable_latch=0, load_capacitance=0, antenna=0, node_sink=0, total=140
```

Buffers help distribute the clock signal evenly and reduce clock skew, so all components get the clock at the same time.

20.

Clock Path Browser

Timing Corner	Skew Group	Skew	Min Delay	Max Delay	Min Pin	MinPath Level	Max Pin
FastDC:hold.early	top	0.019	0.252	0.270	...M_reg_1__0_/CP	5	...reg/q_reg_5_/CP
FastDC:hold.late	top	0.019	0.252	0.271	...M_reg_1__0_/CP	5	...reg/q_reg_5_/CP
SlowDC:setup.early	top	0.027	0.499	0.526	...M_reg_1__0_/CP	5	...reg/q_reg_5_/CP
SlowDC:setup.late	top	0.027	0.500	0.527	...M_reg_1__0_/CP	5	...reg/q_reg_5_/CP

The average skew between FF is:

$$average_{skew} = \frac{0.019 + 0.019 + 0.027 + 0.027}{4} = 0.023\ [ns]$$

Let's check the setup condition:

In our case $T = 9\ ns$

$$T + t_{skew} \geq t_{clk \to out} + t_{pd_{CL}} + t_{setup}$$

$$9 + 0.023 \geq 5.109 + 0.109$$

$$9.023[ns] \geq 5.218[ns]$$

The setup condition is good.

$$t_{hold} + t_{skew} \leq t_{cd}$$

$$0.016 + 0.023 \leq 0.011$$

$$0.039[ns] \leq 0.011[ns]$$

The setup requirement is met with plenty of margin, but the hold requirement fails. Therefore, this skew value is not acceptable.

Submit:

21. Why are odd metal layers routed horizontally and even metal layers routed vertically?
22. Why are VSS and VDD lines placed in an interleaved manner?

21.

Odd metal layers run horizontally while even layers run vertically, minimizing overlap between adjacent layers and thus reducing parasitic capacitance.

22.

VSS and VDD lines are interleaved to prevent one supply from crossing another, keeping power and ground paths distinct. This arrangement reduces noise, balances current flow, and minimizes voltage drops for stable performance.

Submit:

23. Compose a table (as shown below) and summarise results of each frequency.

Frequency	Max corner total power	Min corner total power
Section 2.7 frequency		
100 [MHz]		
200 [MHz]		

24. View and submit the *.rpt* file in Innovus directory. Which cell has the largest power consumption? Why so?

23.

Frequency	Max corner total power [mW]	Min corner total power [mW]
Section 2.8 freq	6.489	8.583
100 [MHz]	6.441	8.524
200 [MHz]	6.878	9.059

24.

The cell which has the largest power consumption is *I*5, which is likely responsible for receiving the clock signal. This cell usually functions as a port, continuously toggling the clock signal and forwarding it to the other components. Because the clock signal switches states frequently, this cell operates at a much higher switching activity compared to other cells in the design, resulting in significantly higher power consumption.