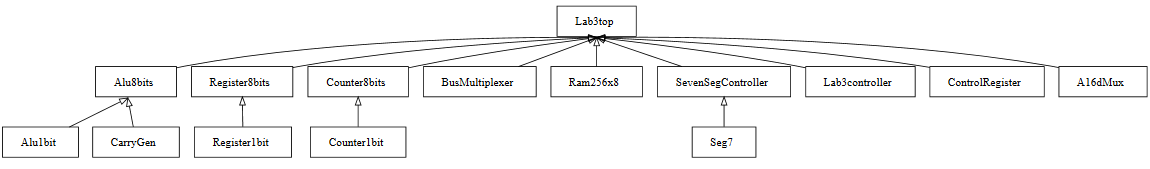
CEG2136 Lab 4 Pre-Lab Questions

1. 

2. Only one register will place an output on the data bus at a time because the BusMultiplexer is an 8x1 Mux, acting as a selector (one mux output at a time).

3. The reset signals are asynchronous because sometimes you have to clear the AC but not the rest.

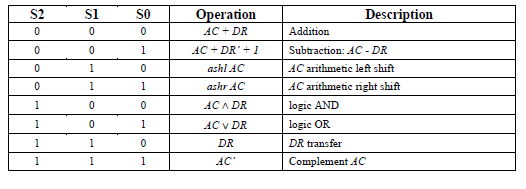
4. If a *load* and a *reset* signal are sent simultaneously sent to a register, the register is cleared, because clear sets both AND gates (in register1bit) to 0, which makes OR 0 (and it’s a D flip-flop).

5. The AR is directly connected to the memory because the AR stores the address of the operand or the operand (or the address of the address of the operand) itself to be fetched from memory

6. They all need to be incremented at various times.

7. Highest to lowest priority: Reset, Load, Increment, because if *clear* is 1, all AND gates are 0, and if *load* is 1, *increment* AND gate is 0 (in counter8bits).

8. No, because the value from memory must be loaded into the DR first, because it is the only register connected to the AC.

9. (see below)