

KENYA METHODIST UNIVERSITY

FACULTY OF COMPUTING AND INFORMATICS

DEPARTMENT OF COMPUTER SCIENCE

**Trimester : 2nd Trimester 2017**

**Course code : BIT 112 /CISY 201 EVEING EXAM**

**Course Name : COMPUTER ARCHITECTURE AND ORGANIZATION**

**Instructions**

**Answer QUESTION ONE AND ANY OTHER TWO QUESTIONS**

**QUESTION 1**

1. Distinguish between the following pair of terms as used in computer science:
2. Computer architecture and computer organization (2 marks)
3. Structure and function (2 marks)
4. Explain the general structure of a computer system stating specific roles of individual components (6 marks)
5. What are the two locality principles observed with respect to user programs? How are these principles exploited in computer design? (4 marks)
6. Using an illustration explain the structure of the Von Newman machine (6 marks)
7. What is an interrupt? Using a diagram explain an instruction cycle with an interrupt.

(4 marks)

1. Briefly describe RAID technology (6 marks)

**QUESTION 2**

1. What is a Bus? (2 marks)
2. Explain **three** Busses as used in computer design (3 marks)
3. What is virtual memory? Explain its need (4 marks)
4. Explain the differences between a multi-processor system and a multi-computer system

(4 marks)

1. Briefly discuss computer evolution and performance (7 marks)

**QUESTION 3**

1. What is cache memory? (2 marks)
2. Briefly outline cache memory operation (5 marks)
3. Using suitable diagrams, illustrate single cache and three level cache organizations

(6 marks)

1. A computer system has a 128 byte cache. It uses four-way set-associative mapping with 8 bytes in each block. The physical address size is 32 bits, and the smallest addressable unit is 1 byte.
2. Draw a diagram showing the organization of the cache and indicate how physical addresses are related to cache addresses. (5 marks)
3. To what block frames of the cache can the address 000010AF16  be assigned

(2 marks)

**QUESTION 4**

1. What is an instruction cycle? Draw a well labelled instruction cycle state diagram.

(8 marks)

1. Design a very simple CPU for an instruction set that contains only the following four instructions: lw(load word), sd(store word), add and jump(un conditional branch) assuming that the instruction formats are similar to the MIPPS architecture. In case you assume a different format please indicate the instruction formats. Show all the components, links and control signals in the data path. Show only the minimal hardware requirements to implement the instructions. (8 marks)
2. For each instruction in (b) above show the steps involved and the values of the control signals for a single cycle implementation. (4 marks)