Lab 02 - First Verilog

In this lab, you've learned how to do an initial and simple design in Verilog to learn the Vivado tooling and process involved in RTL/FPGA design.

Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

Lab Summary

Summarize your learnings from the lab here.

Lab Questions

1 - Describe the stages of building a Verilog project in Vivado.

When creating a project, you need to add some specifications about your project. What board you are using, how you are going to use the board, etc.
First you need to select a directory for the project to be saved, and specify a type of project. For this lab, we used an RTL project.
Second you need to add some files that you will be flashing to the board.
Third, you need to add some constraints.
Then you need to select what board you are going to use, and for this lab we're using the Basys3.

2 - What is the value in looking at the elaborated design schematic?

Its a good visualization of the physical logic gates in the board, and can help you understand the inner workings of the chip.

3 - Why should we simulate our designs frequently? What does the simulation do?

It’s always a good idea to check your work before you flash it to the physical hardware in case you mess it up by accident and brick your device. Simulating allows us to run the program in a safe environment.

Code Submission

Upload a .zip of all your code or a public repository on GitHub.