```
        if (wb_rst_i) begin
            // ... (rest of your reset logic)
        end else begin
            case (wbbd_state)
            // ... (existing states)

            `WBBD_SETUP0: begin
                wbbd_sck <= 1'b0;
                wbbd_addr <= spiaddr(wb_adr_i);
                if (wb_sel_i[0] & wb_we_i) begin
                    wbbd_data <= wb_dat_i[7:0];
                    if (wbbd_data == 8'df) begin
                        wbbd_busy <= 1'b1;
                    end
                end
                wbbd_write <= wb_sel_i[0] & wb_we_i;
                wbbd_busy <= 1'b1; // Ensure wbbd_busy is set to 1'b1 here as we

                if (!spi_is_busy) begin
                    wbbd_state <= `WBBD_RW0;
                end
            end
            // ... (remaining states)
            endcase
        end
    end
```

In this modification, we've added an additional check after setting **`wbbd_data`** within the **`WBBD_SETUP0`** state. If **`wbbd_data`** is equal to **`8'df`**, it will set **`wbbd_busy`** to **`1'b1`**. Additionally, I've added a line to ensure that **`wbbd_busy`** is always set to **`1'b1`** within this state.

You can apply a similar modification in other states if needed.

Continue this conversation