

Microcontroller Peripheral Block Requirements

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You are an expert chip designer working on RTL for a new microcontroller peripheral block. You are tasked with defining and implementing a block with the following features:

- 1) Develop a synchronous block with an asynchronous reset pin that supports the following functions:
- 2) The block should be a simple wishbone bus
- 3) The bus has 32bit width

Do you think there may be missing requirements?

Designing a new microcontroller peripheral block based on the provided requirements will certainly be an exciting task. Before diving into the implementation, let's clarify and expand on the requirements:

1. **Synchronous block with an asynchronous reset pin:** This suggests that while the block will operate based on a clock (synchronous), the reset can be applied at any time, irrespective of the clock state.
2. **Simple Wishbone bus:** Wishbone is a standard bus interface that allows different parts of a digital system to be connected and communicate with each other. However, there are multiple versions of the Wishbone spec (classic, B4, etc.). The "simple" term is vague; we need clarity on which spec version we're following or if any specific customizations are required.
3. **32-bit bus width:** This specifies the data width of the bus. This would mean each data transfer would involve 32 bits at a time.

Here are potential missing requirements or areas where more clarity may be needed:

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