All pertinent documents will be added to GitHub under the alias “LegallyKF5RCL”

The Initial goal is to get the chip modules up and working, then progress can be made developing software code. The follow modules are needed: SPI, UART, ADC.

Module operations needed:

SPI – Chip Select, Data Out, Clock.

UART – TX and RX lines.

ADC – 2 channels, 10 bit conversions.

Module hardware specifications

SPI

Chip select: 1 GPIO.

Data out: SDO1 pin.

Clock: SCK1 pin.

UART

TX: 1 GPIO

RX: 1 GPIO

ADC

2 Channels: 2 GPIO’s

First, I need to get UART up and working first. This will allow for robust debugging, and will be critical at early stages to verify the working status of other modules. To achieve this I will first get UART TX to operate properly. This way, at the least the chip can talk to me. Next RX will give me the ability to talk to the chip. To complete this task item and for verification sake, the chip will be programmed to echo any message that I send to the chip; performed in a debugging mode with warning messages included.

The final stage will be a filter in order to remove the sharp steps from changing the DAC. Without trying to teach myself how to make a feasible high-pass filter, I’m gong to try a parallel RC circuit in simulation first.

Errors

There is a bizarre error in my Debugging routines. When I write to the SPI1BUF, UART prints out 0xFF. As of this commit, this is no longer a problem.

An error was occurring because I was trying to write to UART\_TX buffer too fast after setting up the module. After Inserting a delay of 0xFFFF \* 2 instruction cycles, it fixed itself.